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碩 士 論 文

先進 VLSI 元件中遠程庫倫散射引起電子遷移率衰減之研究

Investigation of Remote Coulomb Scattering Induced Mobility Degradation in Advanced VLSI Devices

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摘要

本文探討了在先進 VLSI 元件中，遠程庫倫散射引起電子遷移率衰減的情形。在高介電場效電晶體中，我們觀察到了電子遷移率衰減的情形。藉由兩種頻率電荷幫浦方法，我們顯示了電子遷移率的衰減是由高介電層內的缺陷所引起的。我們用了一個分析方程式來計算遠程庫倫散射電子遷移率，藉此來模擬遠程庫倫散射的效應。藉著對 SONOS 使用均勻電子寫入的方式，我們確認了電子遷移率會因遠程庫倫散射而衰減。我們的結果顯示了電子遷移率衰減會隨著面際氧化層厚度微縮而變嚴重。

為了瞭解遠程庫倫散射如何影響隨機電報訊號，我們在 SONOS 元件中做了隨機電報訊號的量測。藉著控制寫入窗口，在 SONOS 元件中我們觀察了在不同寫入窗口下的隨機電報訊號。我們觀察到在較大寫入窗口下，隨機電報訊號的振幅比較小。詳細的模型對我們仍然不是很清楚，而且需要更多的研究。

Investigation of Remote Coulomb Scattering Induced Mobility Degradation in Advanced VLSI Devices

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Abstract.

The remote Coulomb scattering (RCS) induced mobility degradation in advanced VLSI devices is investigated. Mobility degradation in HK dielectric MOSFETs is observed. By two-frequency charge pumping method, we show that the mobility degradation is caused from the HK bulk traps. An analytical equation for RCS mobility is calculated to simulate the RCS effect. By using SONOS FN programming, we confirm that the mobility will by reduced by RCS. Our result shows that mobility will be severely limited by RCS as interfacial oxide thickness (IOT) scaling.

Try to know that how RCS effect affects random telegraph signal (RTS) noise, the RTS noise is characterized in SONOS flash memories. By controlling program window, the RTS noise at different program window is observed in SONOS flash memories. The amplitude of

RTS at larger program window is smaller. The detailed model is still puzzling and needed more investigation.

謝誌

本篇論文完成，首先要感謝指導教授汪大暉教授。汪大暉教授提供了良好的實驗儀器及研究環境，使我們可以進行許多先進元件的研究。他紮實且深入的研究訓練，加上嚴謹的研究態度，讓我獲益良多。

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最後要感謝我的父母、家人，在求學期間給我的鼓勵和支持，有了他們經濟上支持、無怨無悔的付出與關心，才能讓我完成我的碩士學位。

2007.6

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Figure Captions

Chapter 1

Introduction

Metal-oxide-semiconductor field-effect transistors have been greatly scaled by reducing the thickness of their gate insulators. High-permittivity dielectrics, as an alternative of conventional SiO_2 gate oxide, are widely investigated for their capability to reduce gate-leakage current for the same electrical capacitance. However, the high-κ gate dielectric itself poses other problems, such as the mobility degradation. It has been suggested that the mobility loss is a combination of several physical mechanisms, namely: remote coulomb scattering (RCS), remote soft-optical phonon scattering (RPS), material parameter variations, or inhomogeneity (thickness, roughness, and permittivity). In high-κ gate stack, a good explanation for this finding is that the Coulomb potential which is induced by the fixed charge at the dielectric/SiO_2 interface is responsible for the scattering.

The RCS originates from charged defects located in the high-κ dielectric. The mobility will be severely limited by RCS as reducing the interfacial oxide thickness (IOT). However, the high-κ performance targets require an EOT reduction, which implies IOT scaling. Thus, the RCS effect will become an important mechanism of mobility degradation in HK dielectric MOSFETs as interfacial oxide thickness further reduces.

Chap 2 starts with the fundamentals of remote coulomb scattering mechanism. In the beginning, the RCS mechanism studied by other people will be reviewed briefly. After that, a simple analytical equation used to model remote coulomb scattering mobility is introduced. Finally, measurement setups of split CV which we use to measure mobility will be shown and introduced.

Chap 3 deals with the mobility degradation due to remote coulomb scattering in HK dielectric MOSFET. Bulk traps generation after stress in HK dielectric MOSFETs will be reviewed in the beginning. Next, the mobility degradation in HK dielectric MOSFETs will be characterized after different FN stress. Then additional bulk traps in HK dielectric MOSFETs generated by FN stress will be checked by a charge pumping method.

In Chap 4, we will measure channel mobility in SONOS flash memories with different bottom oxide thickness to model remote coulomb scattering. First, the mobility in SONOS flash memories with bottom oxide 30A under different FN programming is measured. Second, the mobility in SONOS flash memories with bottom oxide 20A under different FN programming is measured. Then, using the analytical equation introduced in Chap 2 to model the RCS mobility which we measured in SONOS flash memories, we can confirm that RCS plays a more severely role in mobility degradation in bottom oxide scaling.

In Chap 5, random telegraph noise in SONOS flash memories is characterized. First, the RTS theory is discussed. Then measurement setups of RTS will be shown and introduced. Next, RTS measurement under different FN programming will be shown. Subsequently, we find a correlation between the fractional RTS amplitude and RCS induced mobility degradation. Finally, we will give a conclusion in Chap 6.

Chapter 2

Fundamentals of Remote Coulomb Scattering

2-1 Introduction

Remote coulomb scattering in Ⅲ-Ⅴ heterostructure semiconductors has been studied [1]-[4] extensively, and Coulomb scattering due to fixed charges inside the gate stacks in advanced VLSI devices has been treated similarly. The mobility lowering has been observed in ultrathin gate oxide MOSFETs as shown in Fig 2.1 made by Shin-ichi Takagi [5]. It has been suggested that remote Coulomb scattering may lead to severely mobility degradation in HK dielectric MOSFETs in interfacial oxide scaling [6]. In the beginning, the RCS mechanism will be introduced. Then, an analytical equation for modeling RCS mobility and how the equation is derived will be presented. Finally, the measurement setup of split CV which we use to measure mobility will be shown.

2-2 RCS Model

The remote Coulomb scattering originates from charged defects inside the gate stacks. This is because these charges are distant from the channel, so carriers do not directly collide with them. Nevertheless, the paths of the carriers are affected by the potential disturbance created by these charges. A model of HK dielectric MOSFETs is proposed to explain the mobility reduction in terms of fixed charges [7], as shown in Fig 2.2. We can see that charged defects inside the gate stacks will introduce a flat band voltage shift and mobility reduction in HK dielectric MOSFETs(a) and in a SONOS cell(b).

2-3 Analytical Equation for RCS Mobility

In this thesis, we use an analytical equation made by C. HAMAGUCHI [8] to calculate RCS mobility. Here the detail of how to derive the equation and the approximated result will be presented.

The scattering rate of two-dimensional electron gas (2DEG) was derived by ionized impurities along the theoretical treatment made by Ando et al. An impurity located at (r_i,z_i) will produce a potential energy given by the following relation for $z_i < 0$

$$V(r,z) = \sum_i V_i(r - r_i, z - z_i) \qquad \text{Eq (2.1)}$$

$$V_i(r,z) = -\frac{e^2}{4\pi\varepsilon_{av}\sqrt{(r-r_i)^2 + (z-z_i)^2}} \qquad \text{Eq (2.2)}$$

where ε_{av} is an average dielectric constant of the insulating layer and substrate material. Because there is a transition layer at the interface, the dielectric constant does not change abruptly and diverge at the interface. Instead, it changes gradually on an atomic scale. It is thus reasonable to use an average dielectric constant at the interface.

We assume that electrons only occupy the lowest subband with wave function $\zeta_0(z)$ and the subband energy ξ_0. We make a Fourier transformation of the effective potential and take into account the screening of the potential energy by the 2DEG.

$$v_q(z_i) = -\frac{1}{L^2}\frac{e^2}{2\varepsilon_{av}q}F(q,z_i) \qquad \text{Eq (2.3)}$$

$$F(q,z_i) = e^{-q|z_i|}\int_0^\infty e^{-q|z_i|}\left|\zeta_0(z)\right|^2 dz \qquad \text{Eq (2.4)}$$

we also use Fang-Howard variational wave function for the ground state of the 2DEG.

$$\zeta_0(z) = \sqrt{\frac{b^3}{2}} z e^{-bz/2} \qquad \text{Eq (2.5)}$$

where b is the variational parameter. We neglect the higher subbands and the intersubband scattering, so the calculated results are valid only qualitatively.

Electron mobility is influenced by the oxide-charge distribution profile [9]. Now we assume that the ionized remote impurities are uniformly distributed from $z = -d_s$ to $z = -(d_s + d_n)$ in the gate stack layer. Then the relaxation time due to RCS is written as

$$\frac{1}{\tau_{rmt}} = \frac{2\pi}{\hbar} \sum_{k'} \int_{-(d_s+d_n)}^{-d_s} L^2 N_n(z_i) dz_i \times \left| v_{k-k'}(z_i) \right|^2 (1 - \cos\theta_{kk'}) \delta[\xi(k) - \xi(k')] \qquad \text{Eq (2.6)}$$

where $\theta_{kk'}$ is the angle between the wave vectors of 2DEG k and k', and the energy of the 2DEG is given by $\xi(k) = \hbar^2 k^2 / 2m^*$. Summation with respect to k' is evaluated by using integral with respect to k, $\sum_{k'} = L^2/(2\pi)^2 \int d^2k'$. When the ionized remote impurities is uniformly distributed with density N_n, the equation is reduced to

$$\frac{1}{\tau_{rmt}} = \frac{2\pi}{\hbar} \frac{L^2}{(2\pi)^2} \int d^2k' L^2 N_n \int_{-(d_s+d_n)}^{-d_s} dz_i \times \left| v_{k-k'}(z_i) \right|^2 (1 - \cos\theta_{kk'}) \delta[\xi(k) - \xi(k')] \qquad \text{Eq (2.7)}$$

where we used the conservation laws for the wave vectors of 2DEG $k' = k \pm q$ and the energy $\xi(k') = \xi(k)$. Assuming that $q = b$, the ground state wave function may approximate as $F(q, z_i)$; $\exp(-q|z_i|)$. And the relaxation time can be given as：

$$\frac{1}{\tau_{rmt}} = \frac{N_n m^*}{8\pi\hbar^3} \frac{e^4}{\varepsilon_{av}^2} \frac{1}{k^3} \int_0^{\pi/2} d\theta \frac{\sin\theta}{[\sin\theta + Q_s/2k]^2} \times \{\exp[-4d_s k \sin\theta] - \exp[-4(d_s + d_n)k \sin\theta]\}$$

Eq (2.8)

The electron mobility may be evaluated as： $\mu_{rmt} = \frac{e}{m^*} \tau_{rmt}$ Eq (2.9)

For non-degenerate 2DEG, the approximated result is given by

$$\mu_{rmt} = \frac{60\sqrt{2}\pi^{3/2}\varepsilon_{av}{}^{2}(k_B T)^{3/2}}{N_n\sqrt{m^*}e^3} \times \frac{1}{\int_0^{\pi/2} d\theta \frac{\sin\theta}{[\sin\theta + Q_s/2k]^2} \times \{\exp[-4d_s k\sin\theta] - \exp[-4(d_s + d_n)k\sin\theta]\}} \quad \text{Eq (2.10)}$$

where k is approximated by $k = [2m^* k_B T/\hbar^2]^{1/2}$ and $Q_s = e^2 N_s/2\varepsilon_{av}k_B T$ is the screening factor.

Energy band diagrams of AlGaAs/GaAs heterostuctures and SONOS flash memories are shown in Fig 2.3.RCS mobility as a function of sheet density N_s can be easily evaluated in the above equation, once we know the impurity density N_n and ε_{av} the average dielectric constant of the insulating material and the substrate material.

2-4 Mobility Measurement by Split CV

Split CV is one of the most commonly used techniques for measuring MOSFET inversion layer mobility. The effective inversion channel electron mobility (μ_{eff}) and the effective field (E_{eff}) were extracted from current-voltage and capacitance-voltage measurements using the equations below：

$$\mu_{eff} = \frac{L}{W}\frac{\triangle I_{ds}}{\triangle V_{ds}}\frac{1}{Q_{inv}(V_{gs})} \quad \text{Eq (2.11)}$$

$$E_{eff} = \frac{Q_{dep} + \eta Q_{inv}}{\varepsilon_{si}} \quad \text{Eq (2.12)}$$

where V_{gs} is the gate voltage, L and W are the length and the width of the inversion channel respectively, I_{ds} is the source-to-drain current, Q_{inv} is the

inversion charge, Q_{dep} is depletion charge, $\eta = \frac{1}{2}$ for electron, ε_{si} is the permittivity of the silicon.

Fig 2.4 shows the measurement setup we used for mobility measurements of advanced VLSI devices at room temperature. Usually C_{gc} and hence Q_{inv} are obtained at V_{ds} = 0 V in the split CV method. In order to avoid significant error in the mobility value, small voltage values V_{ds} = 20 mV、40mV have been used for the measurement of I_{ds} while Q_{inv} is still obtained at V_{ds} = 0 V. With suitable controlled bias condition during measurement, the channel mobility versus effective field curve will be extracted.

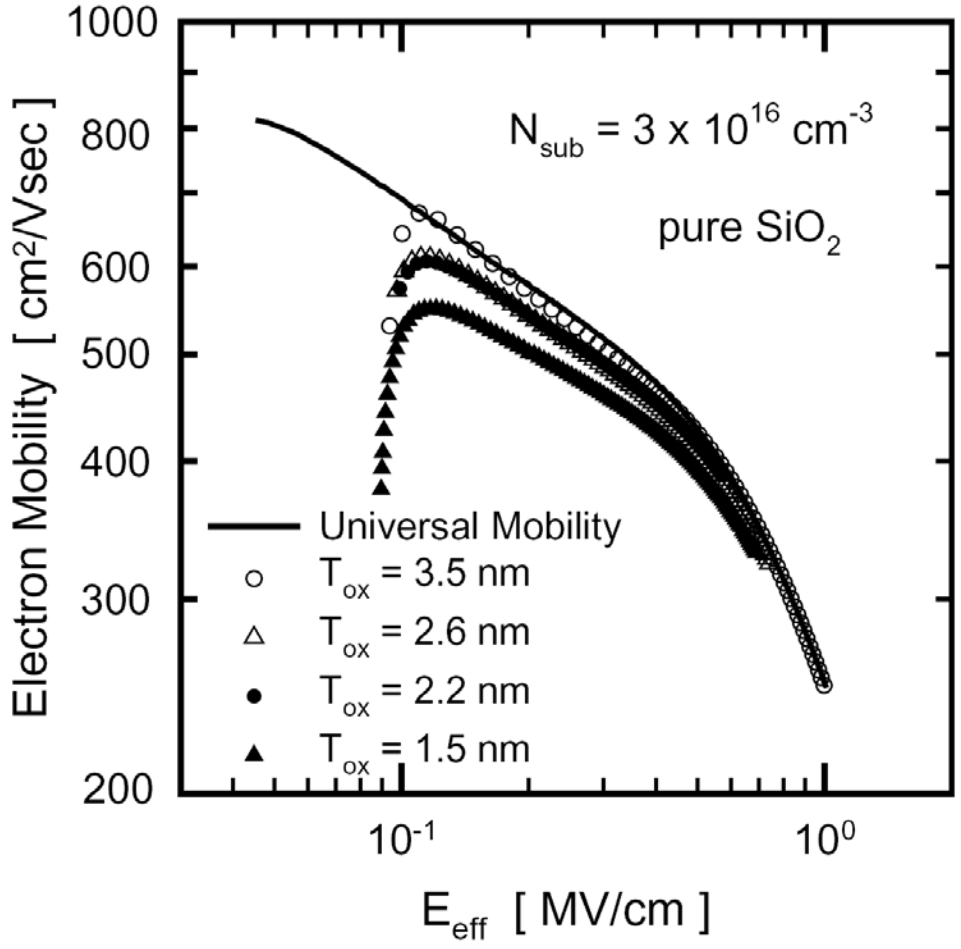

Fig 2.1 Inversion layer electron mobility as a function of E_{eff} with T_{ox} of 3.5–1.5 nm. The solid line denotes the universal mobility.

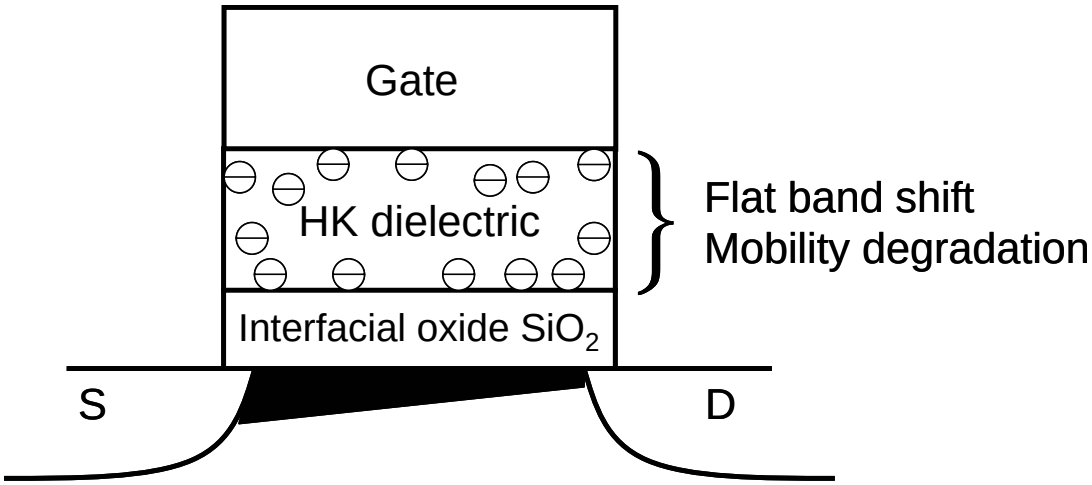

Fig 2.2(a) Illustration of fixed charges in HK dielectric MOSFETs.

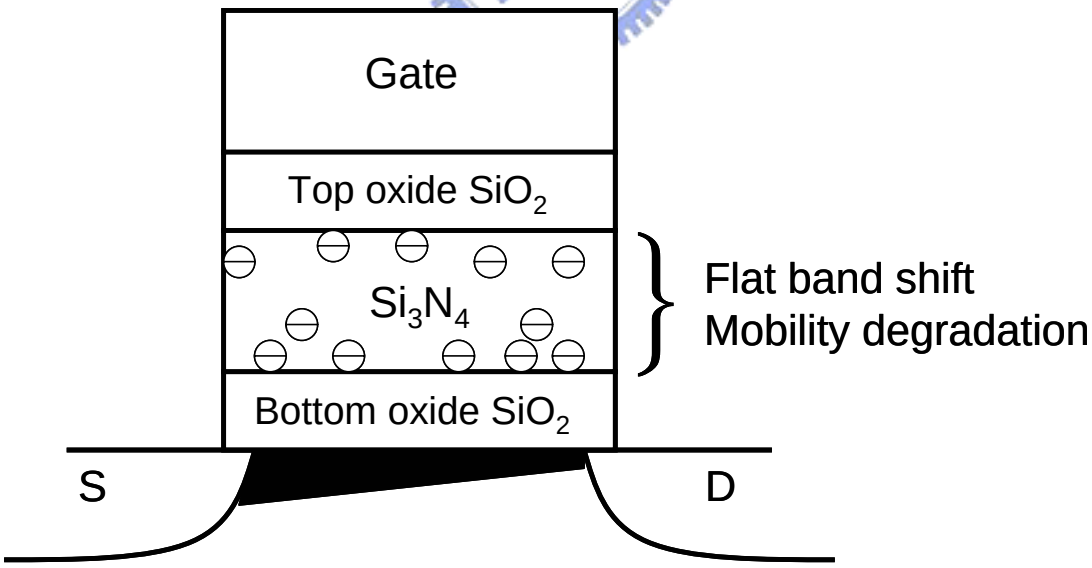

Fig 2.2(b) Illustration of remote charges in SONOS flash memories.

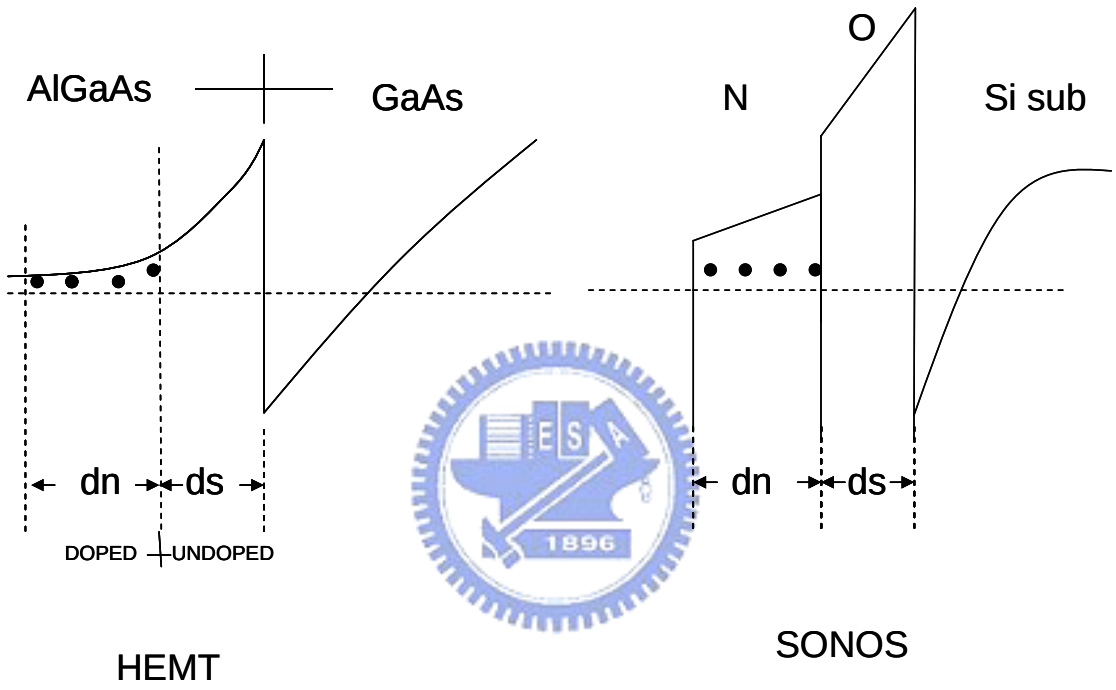

Fig 2.3 Band diagram in HEMT and SONOS.

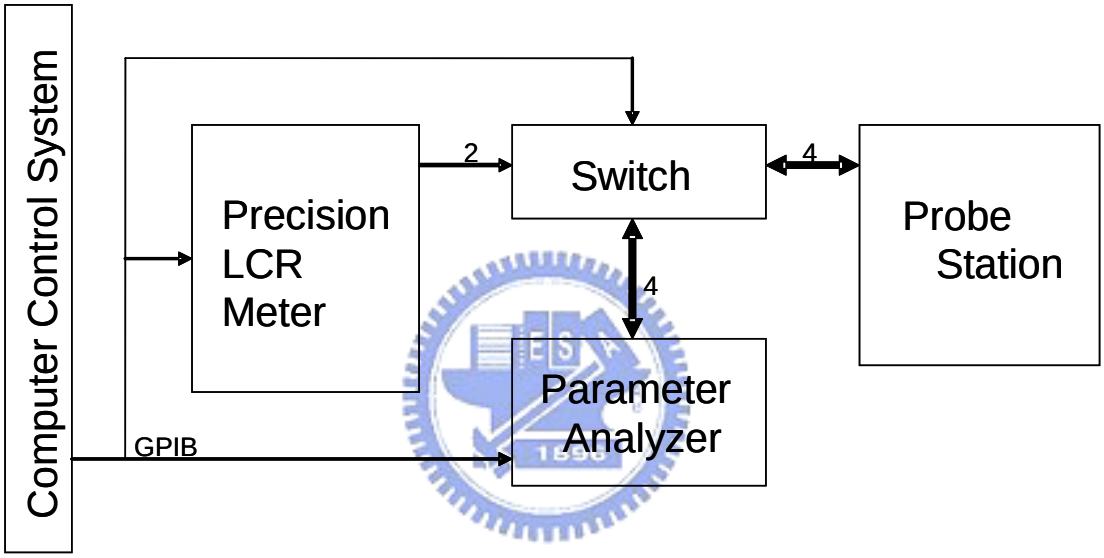

Fig 2.4 The block diagram of measurement setups for split CV

Chapter 3

Characterization of Mobility Degradation in HK Dielectric MOSFETs

3-1 Introduction

High-k dielectrics will be introduced in the 45nm node to achieve the EOT specifications of ITRS. But high-k stacked transistors were reported with low mobility. The main cause for the low mobility has been proposed to be remote Coulomb scattering caused by charges in the high-k dielectric. Stress induced additional bulk traps in high-k dielectric will be reviewed first. After introducing the HK MOSFETs we used in this work, channel mobility-effective field curves will be measured before and after stress.

3-2 Devices

The gate stack in our measured devices consists of a poly-Si gate electrode, HfSiON as high-k layer with physical thickness of 2.5nm, and an interfacial SiO_2 layer with thickness of 1.4nm. The transistors have an equivalent oxide thickness (EOT) of 1.8nm, a gate length of 0.6μm, and a gate width of 100μm.

3-3 Bulk Traps Generation after Stress in HK Dielectric MOSFETs

High-k traps will be generated after a certain stress time. Charge pumping(CP) is usually used to measure the dielectric interface trap density. By modifying the CP

frequency, we can estimate the growth of HK bulk trap density. At higher frequency(f=1MHz), only fast Si/SiO_2 interface traps are sensed, but at lower frequency, deeper traps in HK bulk are also pumped. The high-k trap density is obtained by subtracting trap density measured at lower frequency(f=2kHz) and at higher frequency(f=1MHz). Therefore, high-k trap growth can be characterized by a two-frequency charge pumping technique [10]. The experimental procedure is described in Fig 3.1. As shown in Fig 3.1 and Fig 3.2 made by Chien-Tai Chan [11]. We can see bulk trap generation after stress from a charge pumping measurement.

Here we generated different HK bulk traps in devices by stressing the HK dielectric MOSFETs for different time. The HK bulk-defect density was checked by two-frequency charge pumping measurement. The device gate area was $100\times0.6\,\mu m^2$ (W×L) in order to avoid geometric effect. N_{HK} value has been deduced from the variation of the defects pumped at low (f=2kHz) and at high (f=1MHz) frequencies. The obtained bulk HfO_2 trap density is calculated by means of the equation below:

$$N_{HK}=\frac{1}{Aq}\left[\frac{I_{cp}(@2kHz)}{2kHz}-\frac{I_{cp}(@1MHz)}{1MHz}\right] \qquad \text{Eq (3.1)}$$

where N_{HK} in the above equation denotes the number of traps per unit area.

N_{it} value has been extracted from charge pumping measurement at sufficiently high (f=1MHz) frequency. The values of N_{HK} and N_{it} before stress, after 100s stress and after 500s stress with stress voltage V_g=2V have been reported in Table 3.1. The post-stress device has a higher bulk-defect density than the pre-stress device and the interface state density has almost no difference between the post-stress and the pre-stress devices. We notice that for PBTI stress, the interface trap generation is very limited, while HfO_2 bulk trap generation is large. This means that with suitable

controlled bias condition, we can generate only HK bulk traps.

3-4 Mobility Degradation due to RCS in HK Dielectric MOSFETs

In order to confirm whether the mobility lowering in HK MOSFETs is related to the charged defects located in the HK dielectric layer, the mobility in HK MOSFETs after different stress was examined by split CV method. In the previous section, we characterize the HK bulk-defect density (N_{HK}) and the interface state density (N_{it}). Now, we observe the impact on the peak mobility for the devices after different stress.

All measurements reported were performed at room temperature(~300K). For CV measurement, the frequency was 100kHZ. The source-to-drain current curves were measured at V_{ds} =20mV. The device gate area was $100 \times 0.6\,\mu m^2$ (W×L).

The effective mobility is plotted in Fig 3.3 as a function of the effective field for devices before stress, after 100s stress and after 500s stress with stress voltage V_g=2V. A difference of approximately 18% in peak mobility is observed between the samples. As expected, the peak mobility decreases as stress time increases. Since N_{it} value is the same between the samples, the experimental results mean that the observed μ_{eff} lowering becomes more significant with an increase in N_{HK}, which is consistent with the existing theoretical model of remote coulomb scattering.

The reduced mobility in MOSFETs with HK gate dielectrics was previously reported for an earlier stage of integration. The natural interpretation of this reduction is that it is due to charging, whether by interface traps or fixed charges. A recently developed theory for RCS solves this problem [13] and agrees well with the results of experiments [14]-[15] and quantum Monte Carlo simulations [12]-[16].

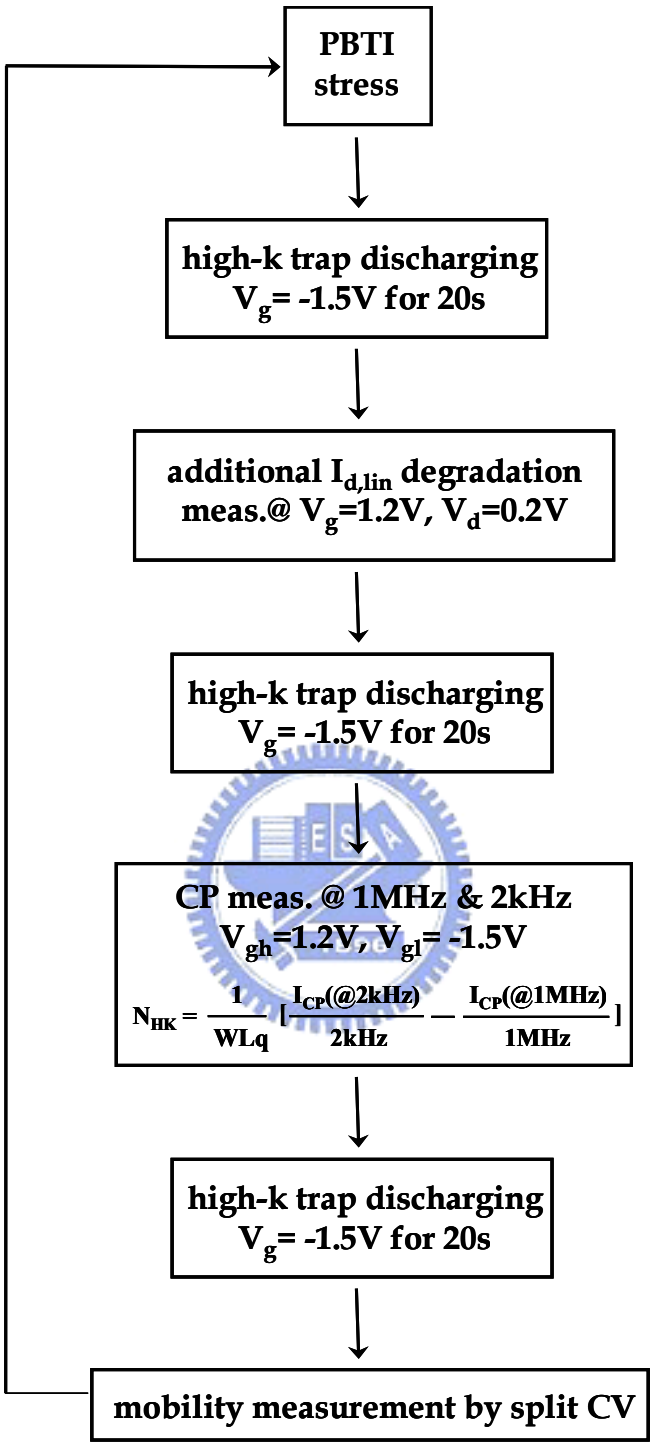

Fig. 3.1 The characterization procedure of the two-frequency charge pumping technique and mobility extracted by split CV.

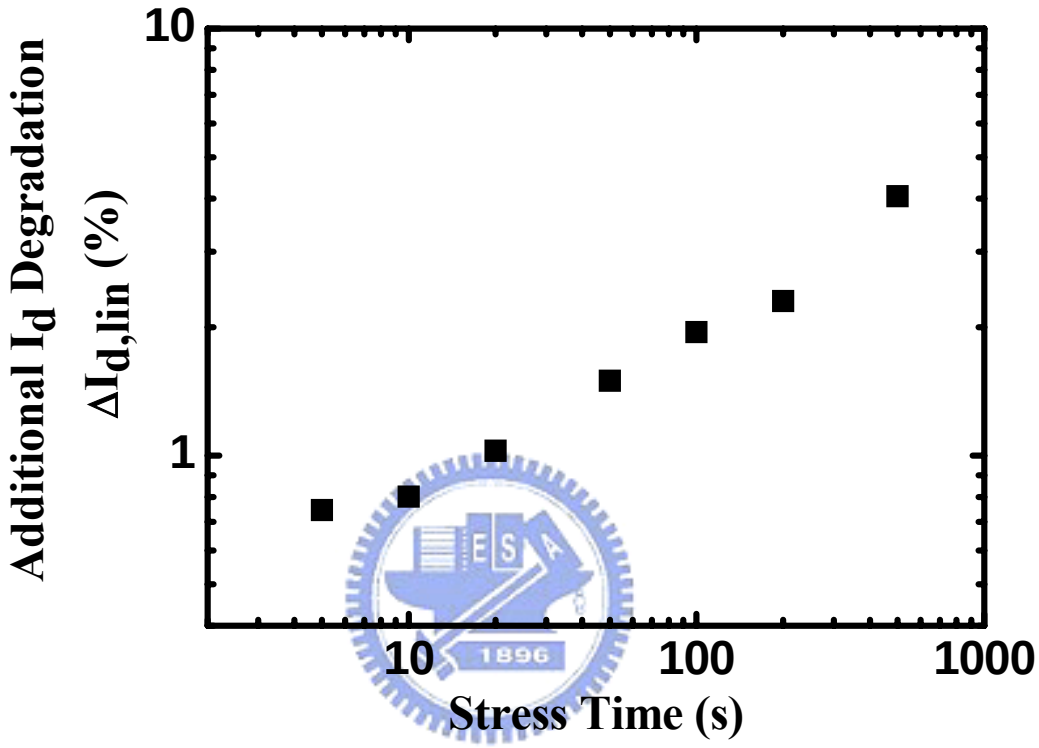

Fig 3.2 The drain current degradation rate after different stress time.
The stress condition is V_g=2.2V, T=25C.

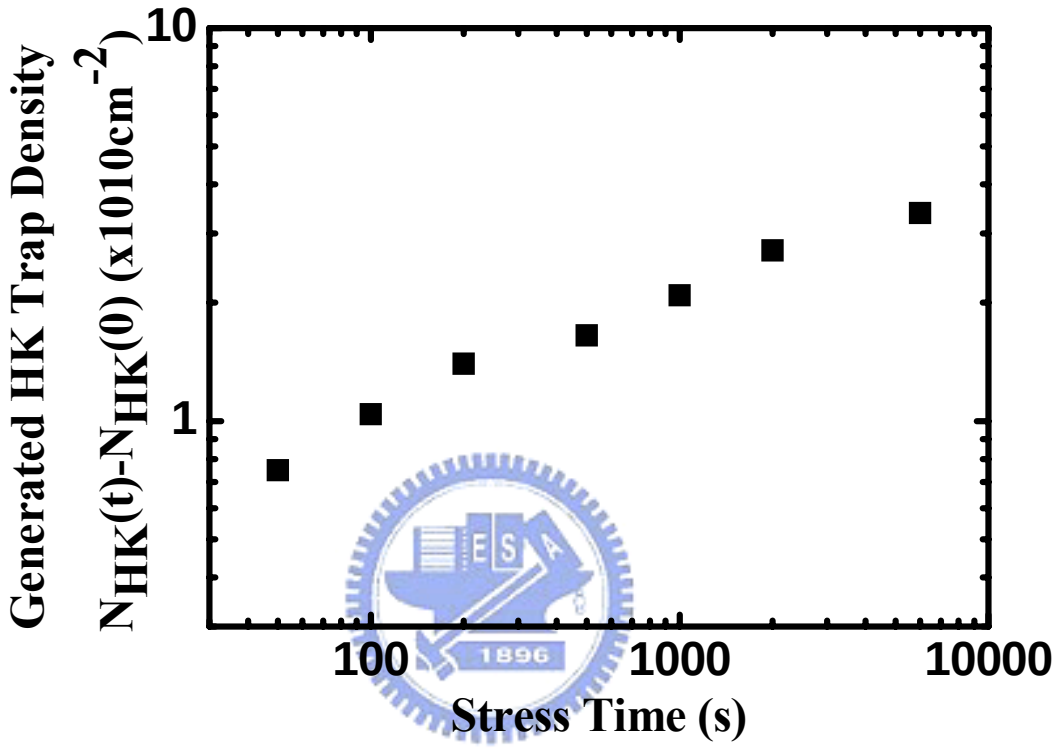

Fig. 3.3 Generated high-k trap density versus stress time from the two-frequency CP techniques. The stress condition is V_g=2.2V, T=25C.

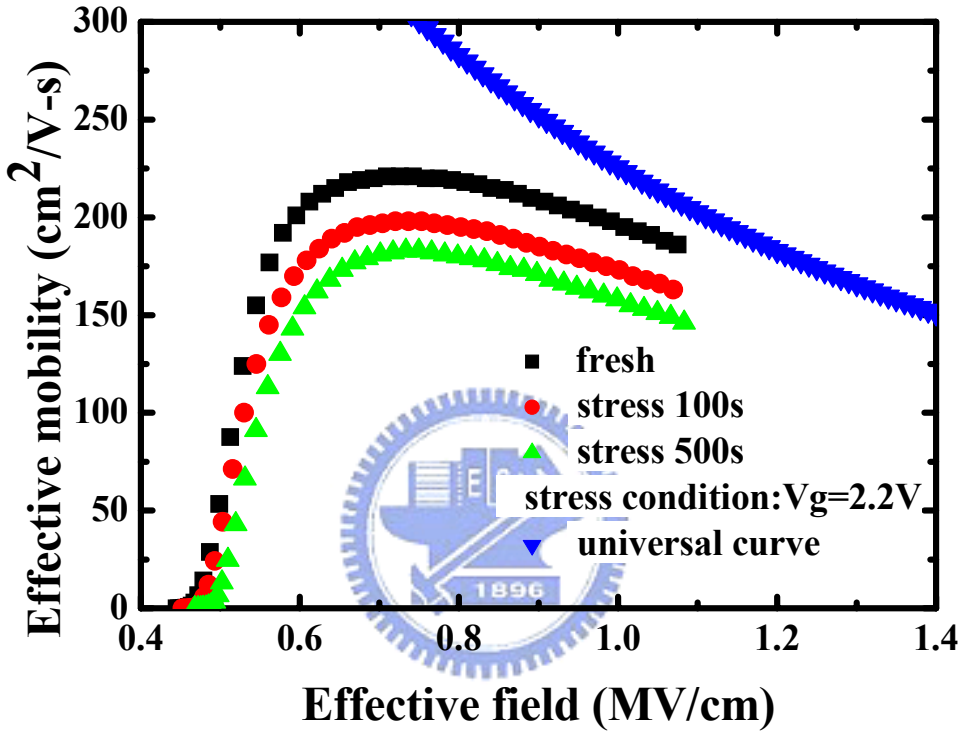

Fig 3.4 Electron effective mobility measured in HK dielectric MOSFET as a function of E_{eff} under different stress times.

Stress time(s)	0	100	500
Peak μ ($cm^2 \cdot V^{-1} \cdot s^{-1}$)	221	198	183
Nhk($\times 10^{10} cm^{-2}$)	3.57	3.86	5.49
Nit($\times 10^{10} cm^{-2}$)	3.29	3.38	3.45
Peak μ / Peak μ_0		89.6%	82.8%
Nhk/Nhk_0		1.08	1.54
Nit/Nit_0		1.02	1.04

$$N_{HK} = \frac{1}{Aq}\left[\frac{I_{cp}(@2kHz)}{2kHz} - \frac{I_{cp}(@1MHz)}{1MHz}\right]$$

Table 3.1 Interface trap sheet densities and bulk trap sheet densities for different stress times extracted from CP measurement.

Chap 4

Characterization of Mobility Degradation in SONOS Flash Memories

4-1 Introduction

To get a clearer picture of RCS mechanism, we will measure mobility-effective field curves in SONOS flash memories after different FN programming. Furthermore, to study the spacer thickness dependence of remote coulomb scattering, we perform mobility measurement at different programming window in SONOS flash memories with bottom oxide 30A and 20A, respectively. Then a comparison between the experimental and calculated RCS mobility will be presented.

4-2 Mobility Degradation in SONOS Flash Memories

The SONOS cell is made of nMOSFET with an oxide-nitride-oxide stack gate dielectrics. Charges can be stored in the nitride layer by uniform injection as shown in Fig 4.1. Uniform injection(FN injection) has uniform electron storage. Here we use FN injection to program uniform charges in the nitride layer which is the same as the remote charges distribution in our RCS model.

It should be noted here that, in addition to remote charges, interface states can be Coulomb scattering centers influential to the inversion-layer mobility. Interface state density has been checked by charge pumping measurement on devices with bottom oxide=30A, W=10 μm and L=1 μm (in order to prevent geometric effect) as shown in Fig. 4.2. It shows that the interface traps density of the devices under FN

programming is about the same.

The device in our experiment are SONOS flash memories with a top oxide of 40A, a nitride layer of 30A, a gate length of 10 μm and a gate width of 10 μm. Two devices with different bottom oxide thickness (30A and 20A, respectively) are measured.

Fig. 4.3 and Fig. 4.4 show the E_{eff} dependence of the inversion-layer mobility for bottom oxide 30A and 20A, respectively. As programmed charges increases, the mobility degradation is more significant in both cases as predicted in the RCS model. Assuming that N_{fix} is much smaller than programmed charges, we can take fresh device as reference sample without RCS. Peak mobility degradation in various programmed conditions has been reported in Table 4.1. Programmed charge density can be estimated from threshold voltage shift by N_n ; $C_{ox} \cdot \Delta V_{th} / A \cdot t_{nitride}$. The Peak mobility are 296 cm^2/Vs and 303 cm^2/Vs for the fresh devices with bottom oxide thickness 30A and 20A, respectively. A degradation of approximate 20% in peak mobility is observed in a SONOS cell with bottom oxide 30A at threshold voltage shift 0.7V. A degradation of approximate 40% in peak mobility is observed in a SONOS cell with bottom oxide 20A at threshold voltage shift 0.8V. Comparing the mobility degradation in SONOS flash memories with different bottom oxide thickness, we can see that the mobility degradation is more severe in SONOS flash memories with thinner bottom oxide.

4-3 Comparison between the Experimental and the Calculated Data

In this section, the experimental and calculated results are compared. The additional mobility component between fresh and programmed samples is defined as

$$\mu_{rmt} = (\frac{1}{\mu_{eff}} - \frac{1}{\mu_{ref}})^{-1} \qquad \text{Eq (4.1)}$$

following Mathiessen's rule, where μ_{ref} is the fresh sample mobility taken as reference. From the equation above, we can extract μ_{rmt} from measurement data. The calculated mobility of 2DEG limited by the remote charged defects evaluated from the Eq (2.9) that has been mentioned in section 2-3.

For the calculation, we need to know four parameters: d_s(bottom oxide thickness), d_n(distributed programmed charge thickness), N_s(channel electron surface density which can be extracted from split CV measurement), N_n(programmed charge volume density; $C_{ox} \cdot \Delta V_{th} / A \cdot t_{nitride}$ where $t_{nitride}$ is the thickness of nitride layer). The only fitting parameter is d_n, the thickness where the remote charges is uniformly distributed. The experimental RCS mobility is extracted by taking the fresh device as reference sample and using Mathiessen's rule. The calculated RCS mobility as a function of N_n for bottom oxide 30A is plotted in Fig. 4.5 with $N_s = 3.14 \times 10^{12} cm^{-2}$, and fitting parameter $d_n = 40A$, while the experimental data are plotted by the solid circles, where μ_{rmt}=5398 cm^2/Vs for N_n=1.34×10^{18} cm^{-3}, μ_{rmt}=1810 cm^2/Vs for N_n=2.69×10^{18} cm^{-3} and μ_{rmt}=1022 cm^2/Vs for N_n=3.77×10^{18} cm^{-3}. The calculated RCS mobility as a function of N_n for bottom oxide 20A is plotted in Fig. 4.6 with $N_s = 2.55 \times 10^{12} cm^{-2}$, and fitting parameter $d_n = 40A$, while the experimental data are plotted by the solid circles, where μ_{rmt}=1737 cm^2/Vs for N_n=1.39×10^{18} cm^{-3}, μ_{rmt}=606 cm^2/Vs for N_n=3.49×10^{18} cm^{-3} and μ_{rmt}=367 cm^2/Vs for N_n=5.51×10^{18} cm^{-3}.

The calculated RCS mobility, with the assumption of $N_s = 3\times10^{12}$ cm^{-2} , $N_i = 2\times10^{12}$ cm^{-2} and $d_n = 20A$ can be plotted as a function of bottom oxide thickness from 0.5 to 3.5nm as shown in Fig. 4.7. RCS mobility is a strong function of the bottom oxide thickness, and RCS mobility decreases when the thickness is reduced, as expected. We can see that as device scaling down, RCS may be a serious limitation for low-EOT achievement.

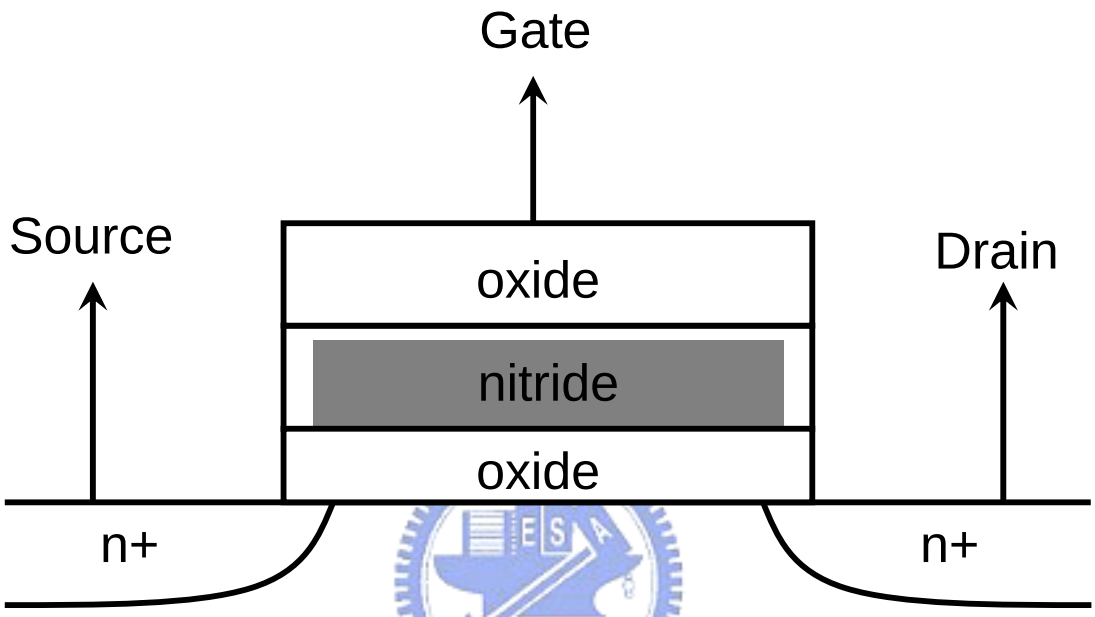

Fig 4.1 Schematic representation of the SONOS structure and uniform charge storage.

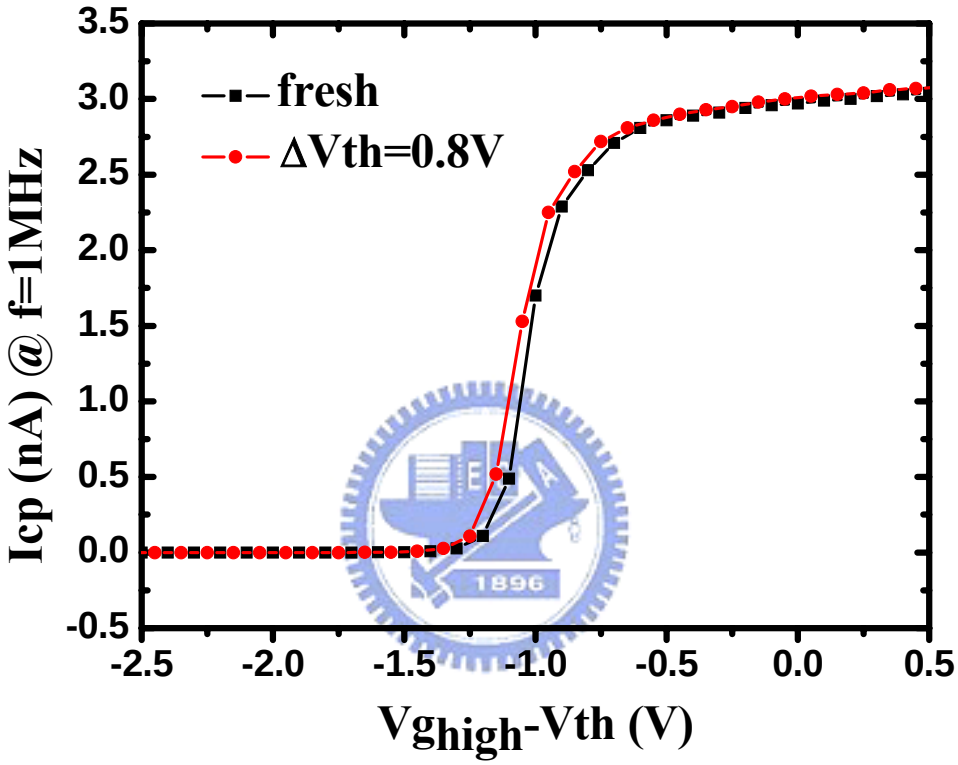

Fig 4.2 Charge pumping current versus the gate overdrive voltage in CP measurement for fresh device and the device with programmed 0.8V threshold voltage shift. The value of Dit has almost no difference.

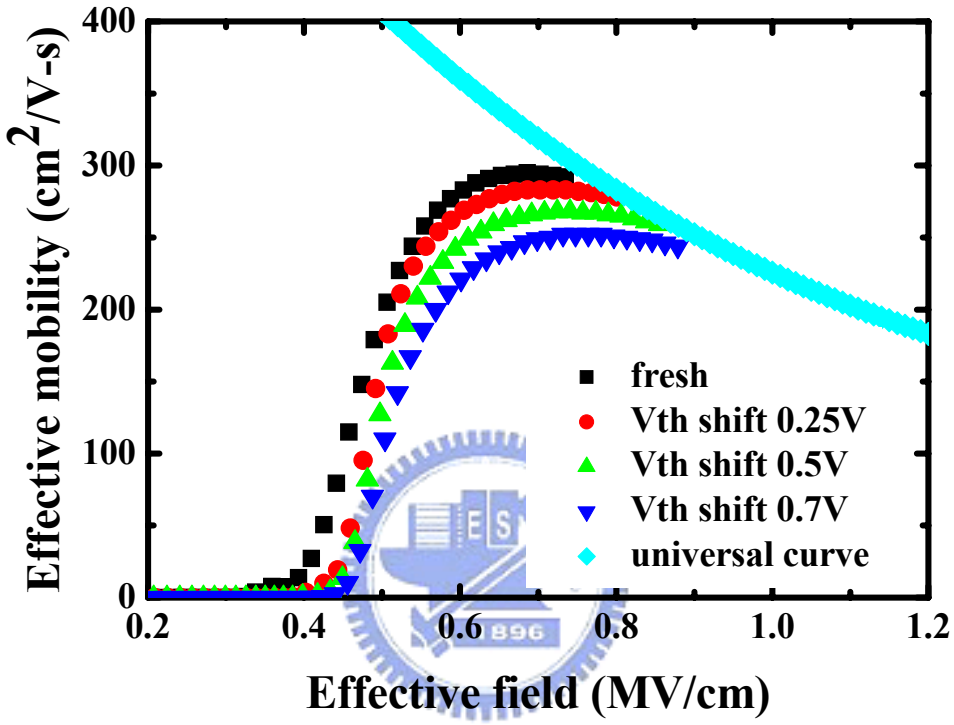

Fig 4.3 Electron effective mobility measured as a function of E_{eff} in SONOS flash Memories with bottom oxide 30A after different programmed threshold voltage shift.

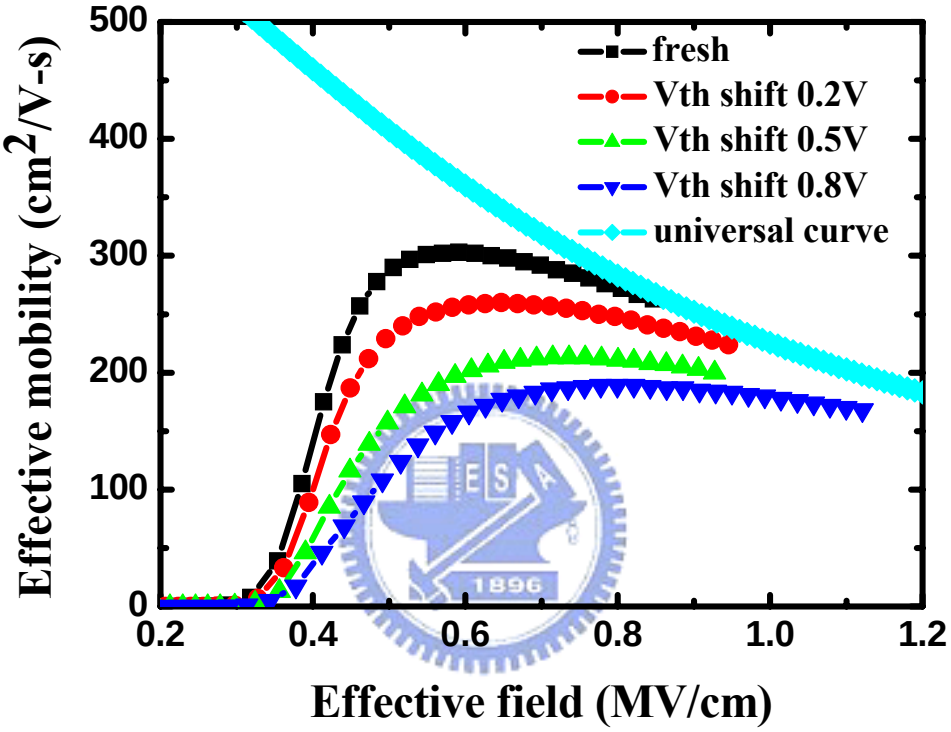

Fig 4.4 Electron effective mobility measured as a function of E_{eff} in SONOS flash Memories with bottom oxide 20A after different programmed threshold voltage shift.

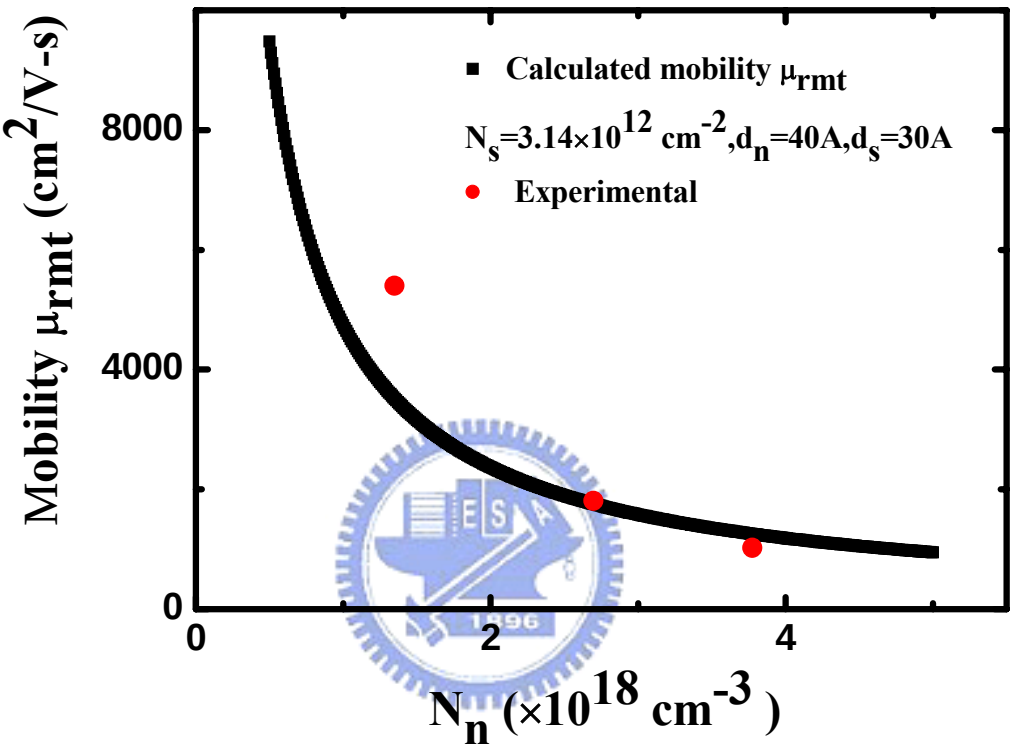

Fig 4.5 Calculated mobility μ_{rmt} of 2DEG limited by the remote coulomb scattering in SONOS flash memories is plotted as a function of programmed charge density N_n. The circular dots are measurement data from SONOS flash memories with bottom oxide thickness Tox=30A.

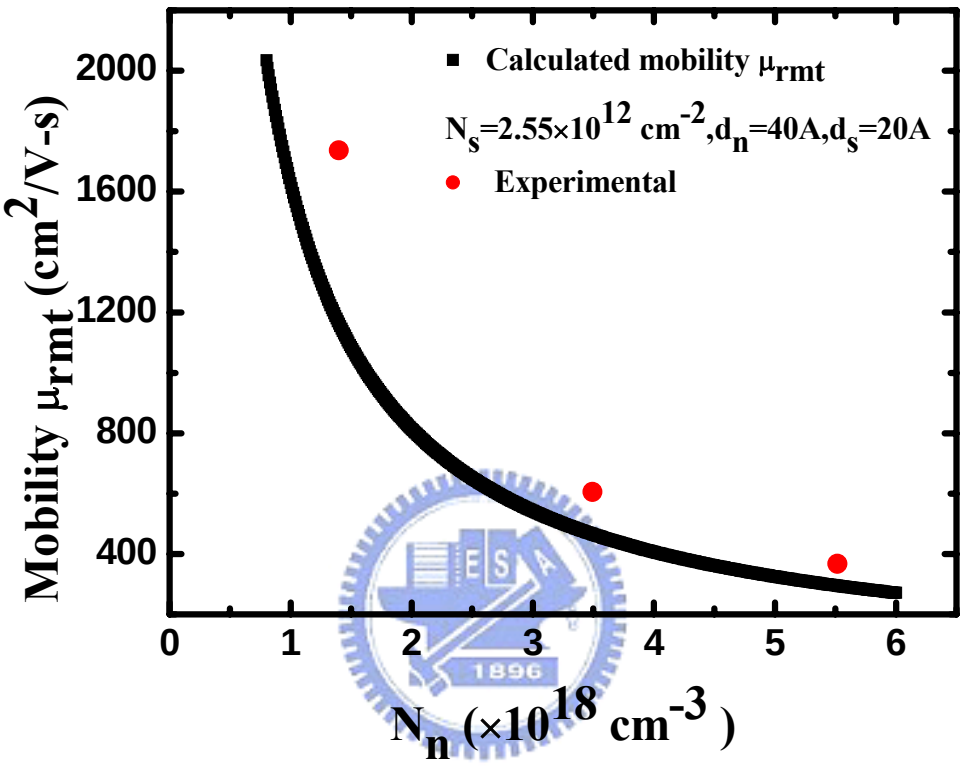

Fig 4.6 Calculated mobility μ_{rmt} of 2DEG limited by the remote coulomb scattering in SONOS flash memories is plotted as a function of programmed charge density N_n. The circular dots are measurement data from SONOS flash memories with bottom oxide thickness Tox=20A.

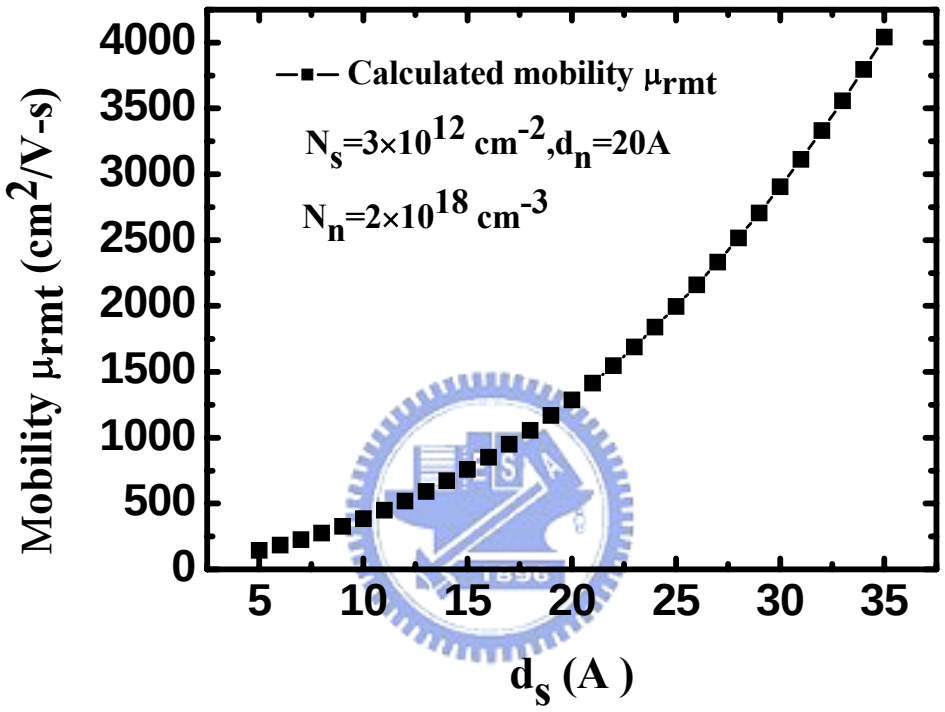

Fig 4.7 Calculated remote coulomb mobility as a function of oxide thickness(d_s) with assumption of $N_s = 3\times10^{12}$ cm^{-2} , $N_i = 2\times10^{12}$ cm^{-2} and d_n=20A.

		△Vth=0	△Vth=0.25	△Vth=0.5	△Vth=0.7
Bottom oxide=30A	Programmed charge density ($(\times 10^{18} cm^{-3}$)		1.35	2.7	3.77
	Peak μ ($cm^2 \cdot V^{-1} \cdot s^{-1}$)	295	283	268	252
	$\frac{Peak\ \mu}{Peak\ \mu_0}$		95.9%	90.8%	85.4%
		△Vth=0	**△Vth=0.2**	**△Vth=0.5**	**△Vth=0.8**
Bottom oxide=20A	Programmed charge density ($\times 10^{18} cm^{-3}$)		1.4	3.49	5.52
	Peak μ ($cm^2 \cdot V^{-1} \cdot s^{-1}$)	303	260	213	189
	$\frac{Peak\ \mu}{Peak\ \mu_0}$		85.8%	70.3%	62.4%

Table 4.1 Peak mobility in SONOS flash memories with bottom thickness 30A, 20A after different programmed charge density.

Chapter 5

Characterization of Random Telegraph Signal in SONOS Flash Memories

5-1 Introduction

Trapping of a single carrier charge in defect states near the Si/gate dielectric interface and related local modulation in carrier density and mobility will have a profound effect on the drain current in such devices. This problem will be exacerbated by the higher defect density in high-k dielectric materials, which are expected to replace SiO_2 in the gate stack somewhere between the 65 and 45 nm technology nodes. Current fluctuations on such a scale will become a seriours issue, not only as a source of excessive low-frequency noise in analog and mixed-mode circuits, but also in dynamic random access memory and static random access memory and other digital application.

Depending on the device geometry, a single or few discrete charges trapped in hot carrier, radiation or bias temperature stress created defect states will be sufficient to cause significant performance degradation in nanometer scale MOSFETs. For MOSFETs with very small channel area, it is possible to have only one oxide trap in the vicinity of surface Fermi level over the entire channel. Thus, individual traps can be observed in their neutral or charged state and the current fluctuation between two discrete levels. The study of random telegraph signal (RTS) noise in submicrometer MOS transistors offers the unique opportunity of studying the trapping/detrapping behavior of a single interface trap.

From the previous chapters, we observe the large influence of RCS effect on mobility degradation in high-k MOSFETs and SONOS devices. However, it is still unclear that how RCS effect affects RTS amplitude. By easily controlling program window in SONOS devices, it provides a good opportunity to investigate these interesting phenomena. First, the RTS theory will be discussed. Second, RTS measurement setups will be shown. Finally, RTS noise in SONOS flash memories under different FN programming will be characterized.

5-2 RTS Theory

Fig 5.1 displays a typical time domain trace of the drain current illustrating the three main RTS parameters. In small enough devices, normally, only trap energy level within a few kT from the Fermi level would make current fluctuation. k and T are the Boltzmann's constant and equilibrium temperature, respectively. Traps with energy levels several kT below the Fermi level would be permanently filled while traps with energy levels several kT above the Fermi level would be permanently empty, resulting in negligible noise power.

Up to now, the discrete change in current has generally been modeled as the superposition of two effects that occurs when the trap changes its state: the effect of number fluctuation of free channel carriers $\Delta \mathrm{N}$, and the mobility fluctuation $\Delta \mu$ described as [17]

$$\frac{\Delta I_d}{I_d} = \frac{\Delta N}{N} \pm \frac{\Delta \mu}{\mu} = -\frac{1}{W \cdot L}[\frac{1}{N} \pm \alpha\mu] \qquad \text{Eq (5.1)}$$

in strong inversion. Here, N is the channel carriers per unit area. It is assumed that the mobility is limited by oxide charge scattering with a coefficient α. The sign in front of the mobility fluctuation is determined by the type of the trap, i.e., a repulsive or an

attractive scattering center. For an acceptor trap, the high level corresponds to the trap in a neutral state while the low level corresponds to the negatively charged state. Therefore, the RTS are completely determined by the up and down times and its amplitude.

5-3 Measurement of RTS Noise

RTS noise is characterized by three parameter：the average of the high and low time constants and magnitude of the current fluctuation, the range of the time constants is from mili–seconds to seconds. In order to obtain a reasonable estimate of high and low states of RTS, a micro–second measurement system is needed. Fig 5.2 shows the basic circuit we used for our measurements of nano–scaled MOSFETs at room temperature. Fig 5.3 shows the photograph of our micro–second RTS noise measurement system. The MOSFET bias voltage（V_D,V_G）are all controlled by batteries with tuning resistor, V_{SUB} is connected to Agilent-4155C Semiconductor Parameter Analyzer, and V_S is connected to a virtual grounded amplifier and will be converted to source current with a 100$k\Omega$ feed back resistor. With fast enough circuit sampling rate, the current fluctuation will be extracted and shown on oscilloscope.

5-4 RTS Measurement under Different FN Programming

The device in our experiment are SONOS flash memories with a top oxide of 4nm, a nitride layer of 4nm, a bottom oxide of 3nm, a gate length of 0.12μm and a gate width of 0.09μm.

Utilizing the fast transient measurement setups [18], RTS pattern under different program window is shown as Fig 5.4. We can see that as the FN programming V_{th}

increasing, the RTS amplitude will decrease. The read current level is controlled near 7μA in the strong inversion region for the same channel carrier number.

The fractional RTS amplitude for different programmed V_{th} shift were listed in Table 5.1. From Eq 5.1, we know that the fractional RTS amplitude was contributed by correlated fluctuation in channel carrier number and mobility. In the linear region of operation, above threshold, $N \approx C_{ox}(V_{gs} - V_{th})/q$,where C_{ox} is the oxide capacitance per unit area, V_{gs} is the gate-to-source voltage and V_{th} is the threshold voltage. In our experiment, V_{th} ; $1.4V$, the carrier number in the entire channel is about 362 and the number fluctuation ; $0.28\% = 3.71\%$. So in our experiment, the component of number fluctuation can be almost ignored. This suggests that the fractional RTS amplitude is attributed to mobility fluctuation.

The amplitude of RTS at a lager program window is smaller. This means that the contribution of $\frac{\mathrm{V}\mu_{eff}}{\mu_{eff}}$ is smaller. The mobility measurement we made in Chap 4 shows that the channel mobility will be reduced after FN programming. We can deduce that the degradation of $\Delta\mu$ caused by RCS effect is more severe than the degradation of μ induced by RCS effect. This result may be explained from the degree of RCS. Single charge plays less and less contribution to mobility fluctuation as the program charge increases. Thus, the program charge plays a relative larger part on the degradation of channel mobility at larger programming window. The detailed model is still puzzling and more investigation is needed.

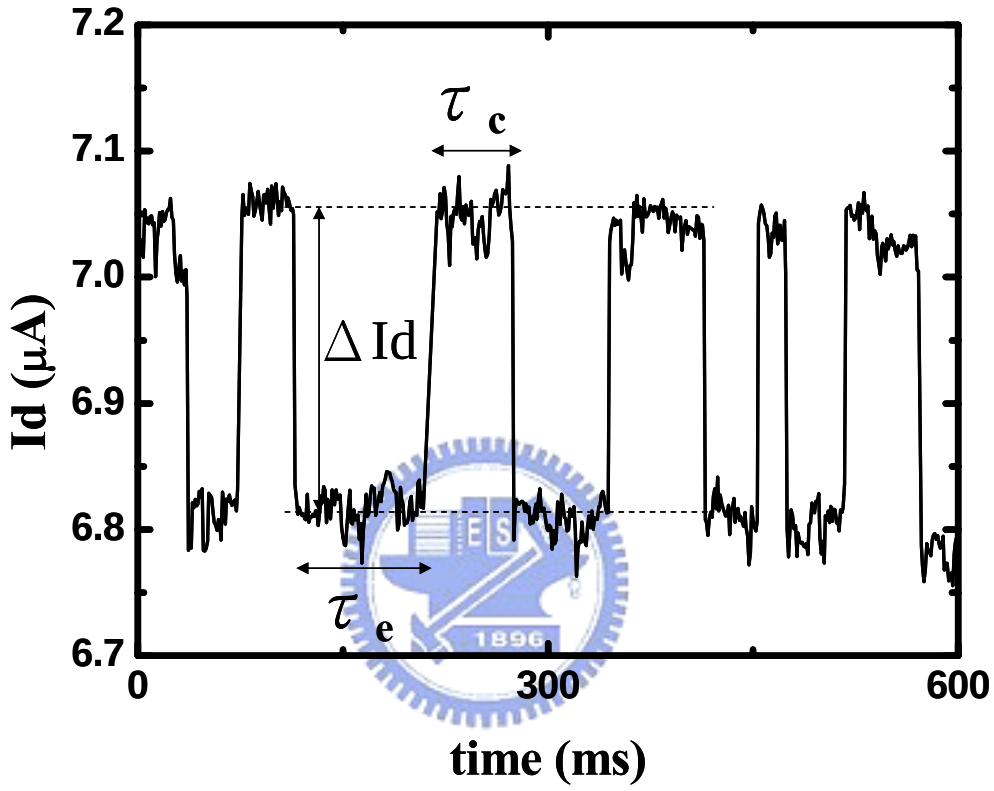

Fig 5.1 Typical time domain plot of the drain current for RTS noise.
Illustration of the three major parameters of RTS noise.

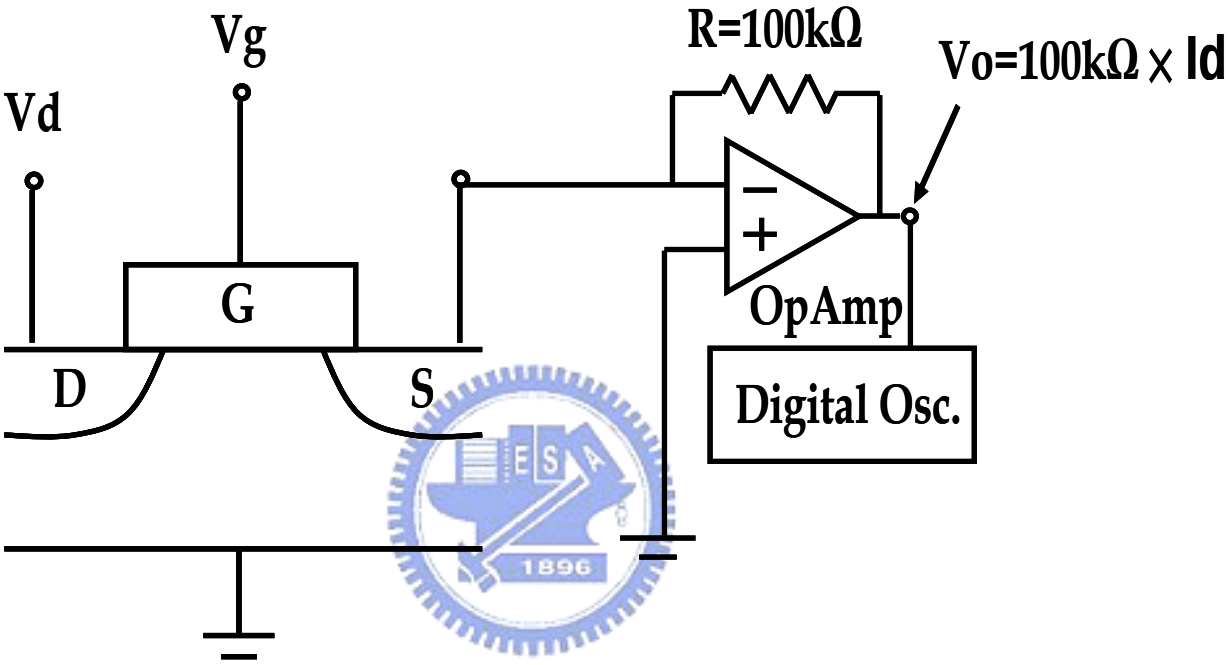

Fig 5.2 Block diagram of experimental setup used for the measurement of RTN in MOSFETs

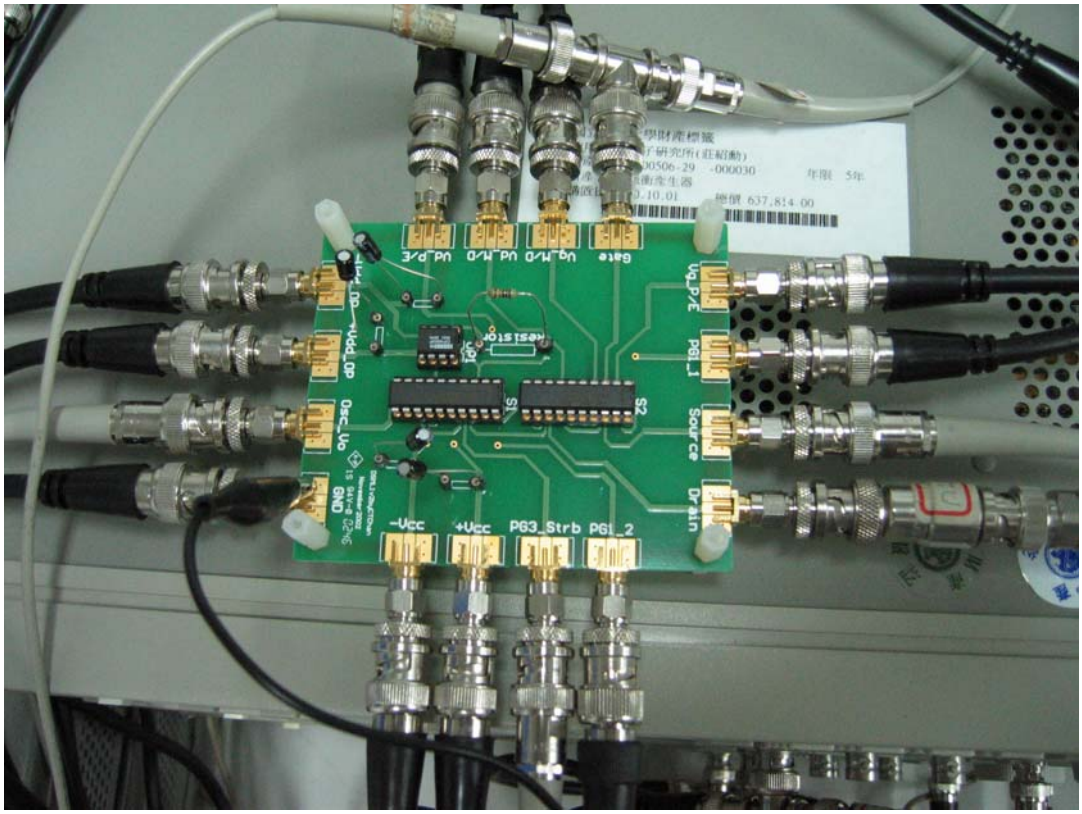

Fig. 5.3 The photograph of our micro-second measurement system

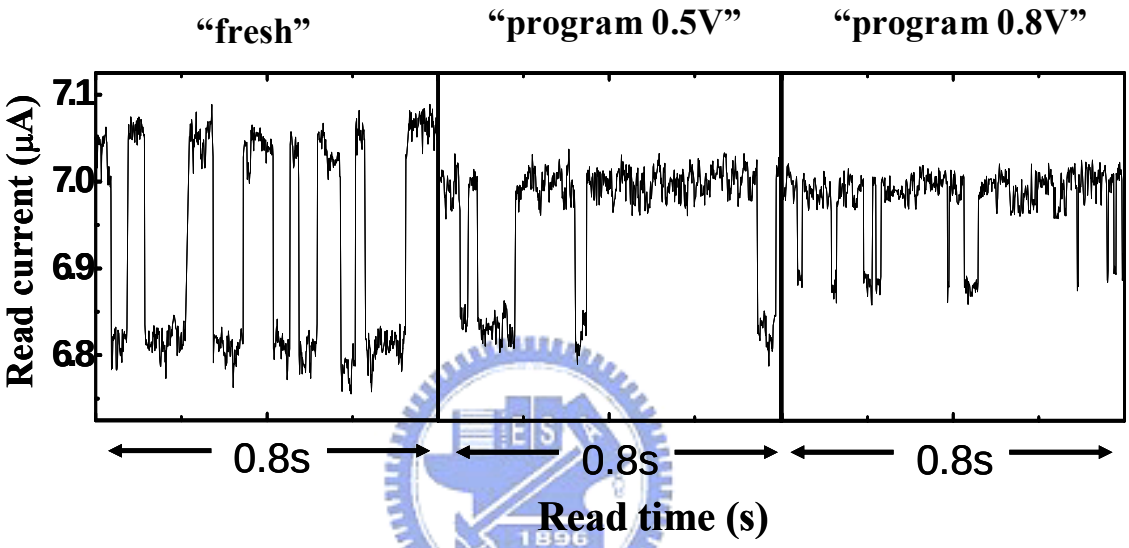

Fig 5.4 Comparison of RTN amplitude in three different programmed Vth shift in a SONOS cell.

	Base current	RTN amplitude	I_d fluctuation
Fresh sample	6.933 μ A	257nA	3.71%
Program 0.5V	6.914 μ A	154nA	2.23%
Program 0.8V	6.931 μ A	103nA	1.49%

Table 5.1 The fractional RTN amplitude under different FN programmed threshold voltage shift observed at almost the read current ; $7\mu A$.

Chapter 6

Conclusion

The study has characterized RCS induced mobility degradation in advanced devices. With suitable bias condition, we can generate only HK bulk traps in HK dielectric MOSFETs. Interface trap density and HK bulk trap density have been extracted by a two-frequency charge pumping method. We have shown that the mobility is reduced as HK bulk trap density increases in HK dielectric MOSFETs.

An experimental evidence of RCS induced mobility degradation is obtained in SONOS flash memories with different bottom oxide thickness. In order to simulate the RCS mobility dependence of bottom oxide thickness, a RCS mobility calculated by 2DEG theory is compared with experimental data. We find that the mobility will be significantly reduced as bottom oxide is further scaled.

To find the relation between RCS and mobility fluctuation on RTS, RTS measurement in SONOS flash memories was characterized. The fractional RTS amplitude corresponding to mobility fluctuation decreases after FN programming. The model is still puzzling and more investigation is needed.

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碩士論文題目:

先進 VLSI 元件中遠程庫程散射引起

電子遷移率衰減之研究

Investigation of Remote Coulomb Scattering Induced Mobility Degradation in Advanced VLSI Devices