國立交通大學

電子工程學系　　　電子研究所碩士班

碩士論文

應用不同金屬閘極和源極汲極離子佈植於二氧化鈰奈米微晶粒之 SONOS 記憶體研究

The Study of High-K CeO_2 Nanocrystal Flash Memory with Different Metal Gates and Source/Drain Implantations

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應用不同金屬閘極和源極汲極離子佈植於二氧化鈰奈米微晶粒之SONOS記憶體研究

學生：余明爵　　　　指導教授：雷添福　博士

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摘　要

在本論文的第二章中，我們討論金屬閘極的功函數在經過不同溫度的退火處理所產生的變化。我們利用一組有系統的數學算式來萃取準確的金屬閘極功函數。我們期望在記憶體抹除操作時，金屬閘極的功函數可以在減少經由阻障介電質的EBT (eliminating electron back tunneling)現象中扮演重要的角色。

在本論文的第三章中，我們提出金屬閘極的功函數對於高介電係數二氧化鈰奈米微晶粒作為記憶體元件的電荷捕捉層的衝擊。我們利用不同的閘極材料應用在高介電係數二氧化鈰奈米微晶粒作為電荷捕捉層的記憶體元件上，來探討元件抹除效率的提升。

在本論文的第四章中，我們提出一個利用高介電係數二氧化鈰奈米微晶粒作為電荷捕捉層的高效能非揮發性記憶體。在資料保存期間的嚴重漏電流問題，可以藉由奈米微晶粒的元件結構有效減少。因為奈米微晶粒在穿隧氧化層中彼此分離，因此存在奈米微晶粒中的電子不會一條漏電路徑就全部漏光。因此奈米微晶

粒元件結構的穿隧氧化層厚度可以繼續微縮，來達到更快的寫入速度和更低的操作偏壓。另外我們改變不同的源極汲極離子佈植來達到更優越的記憶體特性。

The Study of CeO_2 Nanocrystal SONOS Memory with Different Metal Gates and Source/Drain Implantations

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ABSTRACT

In chapter 2 , we discuss the dependence of metal gate work functions on the different annealing temperatures. we found a systematic methodology to extract the accurate work function of metal gates .We expect metal gate work-function can play a key role in eliminating electron back tunneling (EBT) through the blocking dielectric during the erase operation.

In chapter 3, we have carry out a study on the impact of metal gate work function on the memory properties of high-k CeO_2 nanocrystal based CTF memories. Schemes to improve erase efficiency of high-k CeO_2 nanocrystal CTF memory devices with different metal gates are discussed.

In chapter 4, we purpose a high performance nonvolatile memory with high-k CeO_2 nanocrystal charge trapping layer. The serious leakage problem during retention can be eliminated by utilizing a nanocrystal memory structure. The electrons stored on the nanocrystal directly above the defect chain will be affected since the nanocrystals are separated from each other within the gate oxide dielectric. The tunnel oxide thickness in the nanocrystal memory device can be reduced to allow faster programming and lower voltage operation. We also use different source/drain implantation approaches to achieve superior memory characteristics.

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首先要向指導教授雷添福博士致上最大的謝意，我的論文在老師的關心指導下才得以順利完成。老師採取信任的態度，讓學生自由發揮創意做實驗，在報告進度時提供了寶貴的意見，讓我在這兩年學到了研究的精神和做事的方法。

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Chapter 1

Introduction

1-1 Overview of Flash Memory

Semiconductor memory is an indispensable component of modern electronicsystems. It is used in personal computers, cellular phones, digital cameras, smart-media, networks, automotive systems, global positioning systems.

The memories based on complementary metal-oxide-semiconductor (CMOS) technology can be divided into two main categories by whether the storage data can be affected by the power supply.

The volatile memory: like SRAM and DRAM .

SRAM memory can retain the stored information as long as the power is on, drawing very little current. However, the information will be lost when the power is turned off, so SRAM is not a nonvolatile memory.

A Dynamic Random Access Memory (DRAM) cell consists of one transistor and one capacitor . Compared to flash memory, DRAM has much faster program/read speed with very low operating voltage, while flash memory needs 1us to 1ms programming time and high programming voltage. Unfortunately, DRAM is a volatile memory.

The non-volatile memory: this kind memory will keep the storage data even if the power supply is off, like electrically programmable read only memory (EPROM), electrically erasable programmable read only memory (EEPROM), and the flash memory. Fig. 1-1 shows the semiconductor memory.

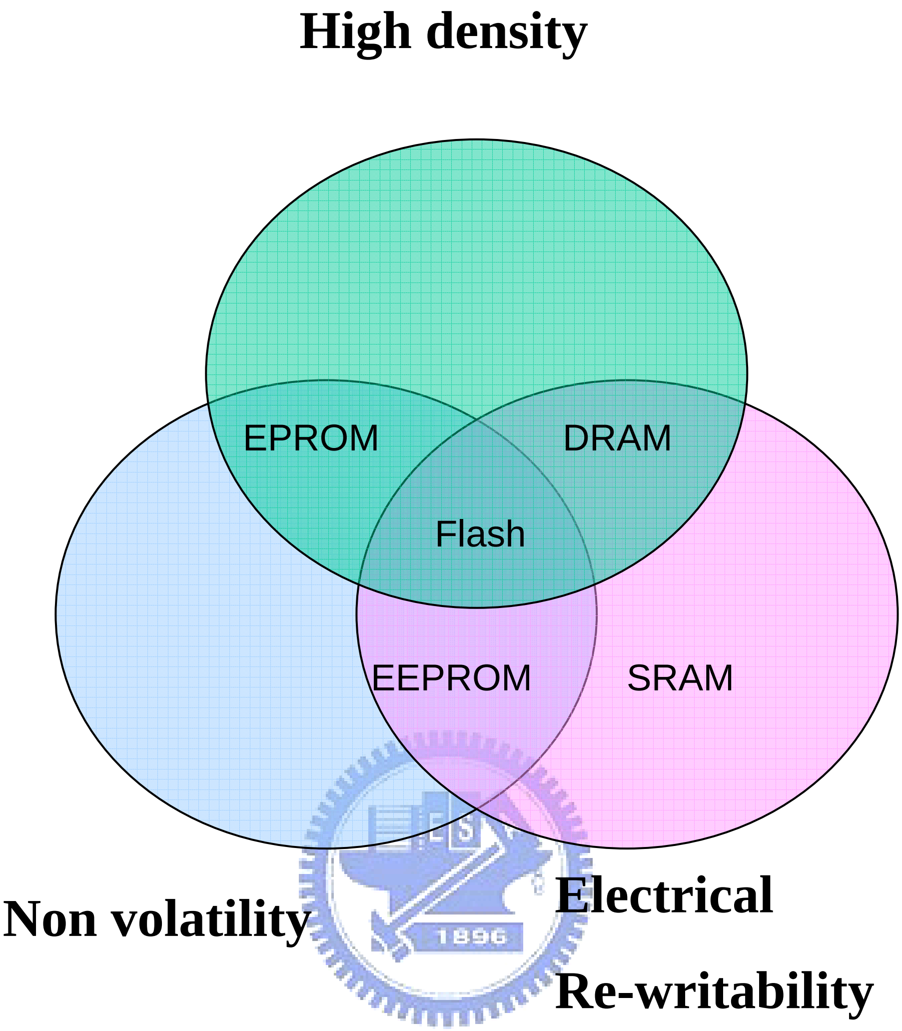

Fig. 1-1 The semiconductor memory .

The most explosive growth field of the semiconductor memory is the Flash memory. The advantages of Flash memory are that it can be electrically written more than 100K program and erase cycles.

S. M. Sze and D. Kahng, invented the first floating-gate (FG) nonvolatile semiconductor memory in 1967.The conventional FG memory used polysilicon as a charge storage layer surrounded by the dielectric. As depicted in Fig. 1-2. Figure 1-3 shows a typical current versus gate voltage characteristic of an erased FG memory and its V_t shift when the FG memory is programmed.

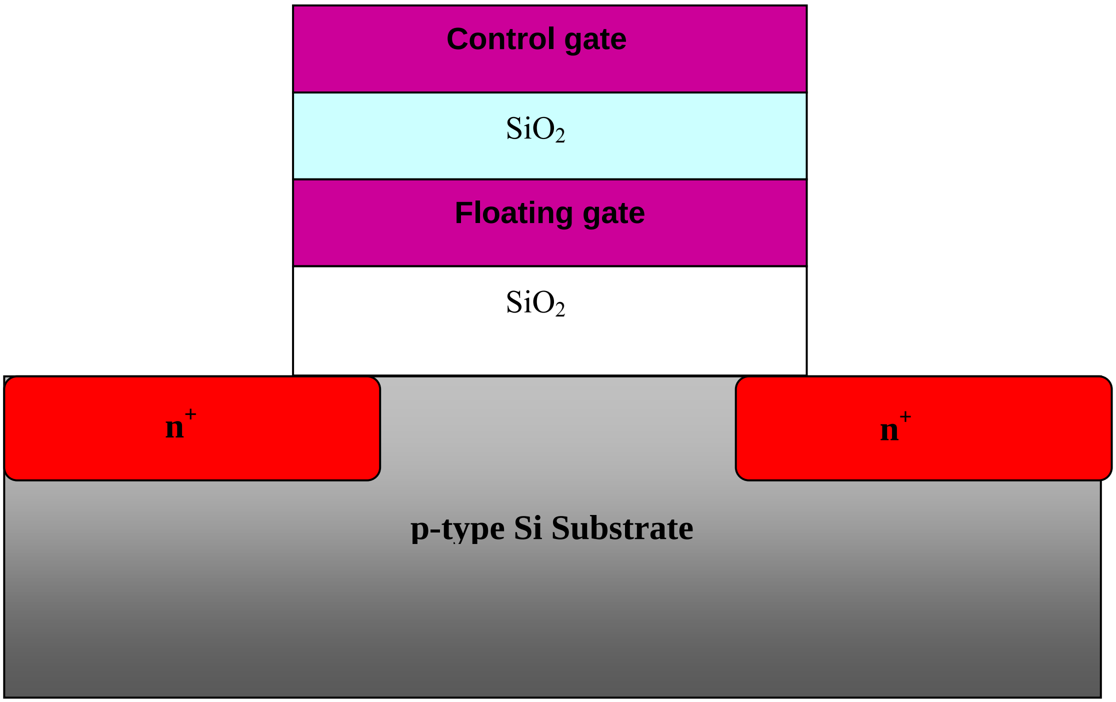

Fig. 1-2 The floating gate (FG) structure. The polysilicon is used as floating gate to storage data.

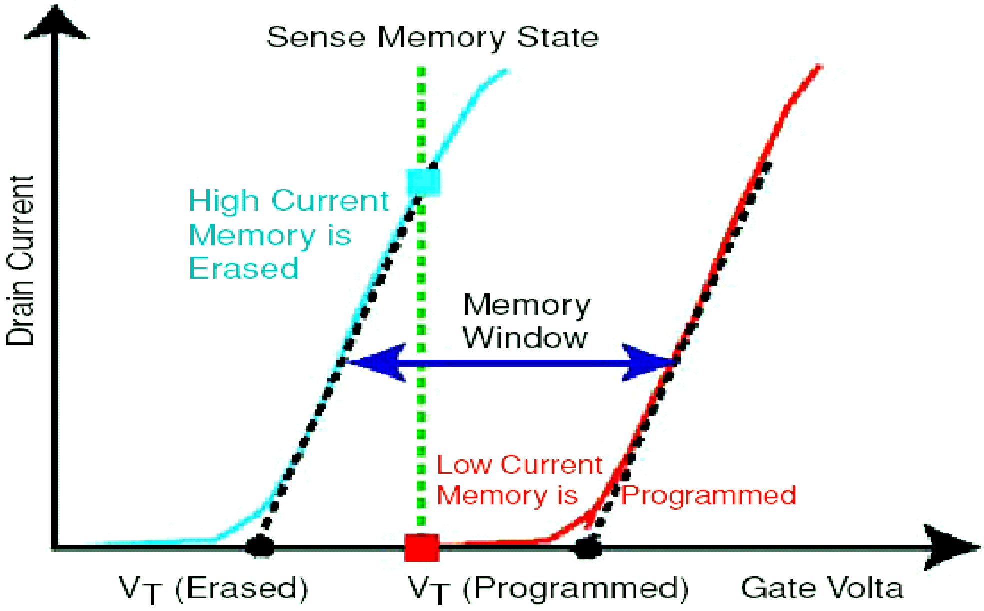

Fig. 1-3 Current-voltage characteristic of a memory device in the erased and programmed state, showing the Vt shift and the memory window.

The FG structure can achieve high densities, good program/erase speed and good reliability for Flash memory application. However, the FG memory has several drawbacks. First, the Flash memory needs thick tunnel oxide (8~10nm) to provide superior retention and endurance characteristics, so it causes high operation voltage, slow P/E speed, and poor scalability. Second, because the polysilicon floating-gate is conductive, the total charges stored in floating-gate will be easily leaked directly through the tunnel oxide when the tunnel oxide is damaged during P/E cycles. In order to improve the write/erase speed of a floating-gate device, the thickness of the tunnel oxide must be reduced. The tunnel oxide must be less than 25Å in order to achieve 100 ns write/erase time for a reasonable programming voltage (<10 V). Unfortunately, the retention time will be too short. Stress induced leakage current (SILC) will further degrade the retention time.

The floating gate memory requires thick tunnel oxide to prevent charge loss through the defect. In order to solve the scaling issue of FG memory, the poly Si-Oxide-Nitride-Oxide-Silicon (SONOS) memory has been studied recently. SONOS memory has better charge retention than floating gate memory when floating gate tunneling oxide is below 10nm due to its isolated deep-level traps. Hence, a leakage path in the tunneling oxide will not cause the discharge of the memory cell. The structure of SONOS memory is shown in Fig. 1-4. The SONOS memory uses silicon nitride as charge trapping layer, and the band diagram is shown in Fig. 1-5.

In the SONOS memory, electrons are stored in the physically discrete traps (labeled with the trap energy level of Et) below the nitride conduction band. In this device, the electrons cannot move freely between the discrete trap locations, hence the SONOS memory device is very robust against the defects inside the tunnel oxide and has better endurance than the floating gate flash memory. Electrons can be thermally de-trapped into the nitride conduction band and then tunnel back to the channel. This thermal de-trapping rate is exponentially reduced with a deep trap energy level. For these reasons, the SONOS flash memory can have much better retention time than the floating gate flash memory. A tunnel oxide of 3nm is thick enough to guarantee 10 years retention time in the SONOS flash memory

When we apply a positive voltage on the gate, the band will bend downward, the electrons in the Si-sub conduction band will tunnel through the tunneling oxide and trapped in the charge trapping layer. Before electrons are trapped in the nitride, they must degrade the program speed. Besides this, the trapped electron back tunneling may also occur. To solve these problems, the high-k materials are the possible candidates to replace the traditional silicon nitride as charge trapping layer.

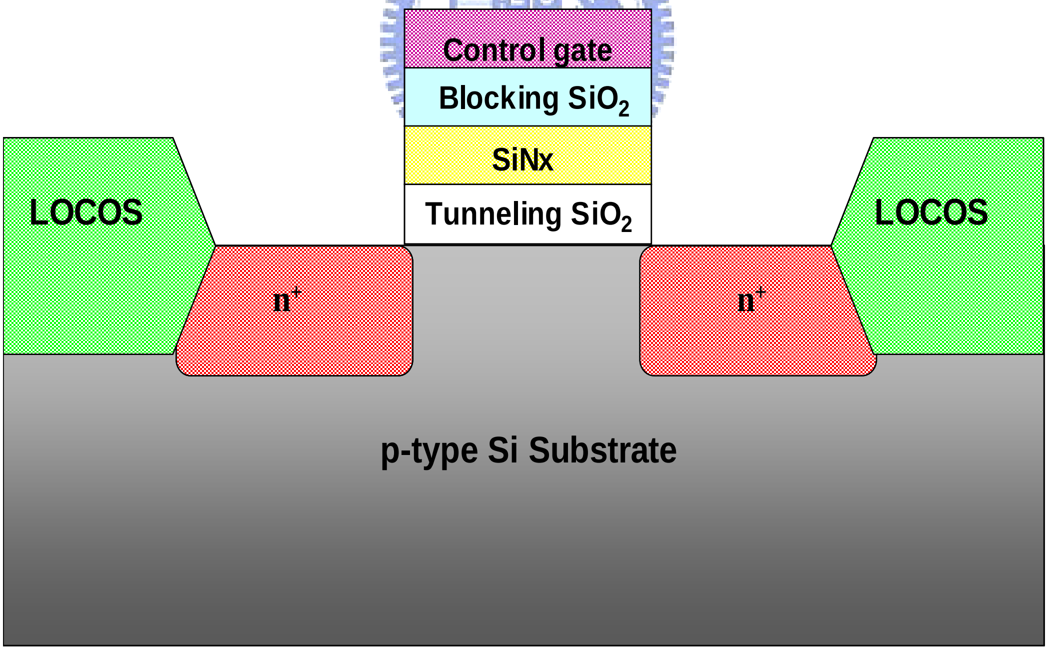

Fig. 1-4 The conventional SONOS memory structure. Silicon nitride is used as charge trapping layer.

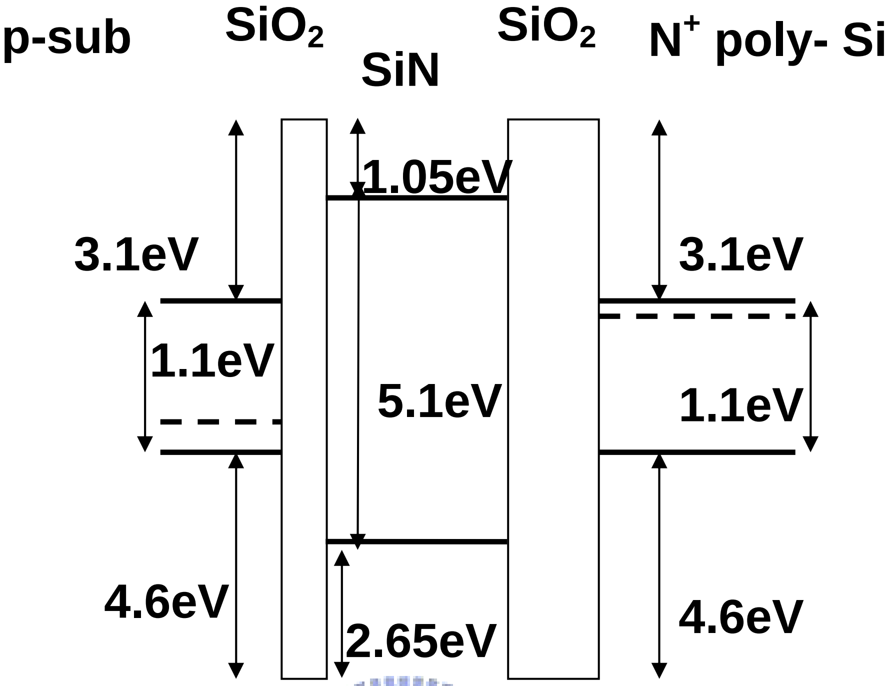

Fig. 1-5 The band diagram of nitride- based SONOS memory.

The advantages of high-k material are smaller barrier height between silicon substrate and high-k charge trapping layer and more trapping sites than silicon nitride. The smaller barrier height can get faster program speed under the same stress condition. More trapping sites can achieve larger Vth shift for larger memory window. Thus, it is beneficial to use a high-k material as the charge trapping layer in a SONOS-type memory device. It provides more deep level trapping sites in the high-k material than in silicon nitride. It is desirable to choose a high-k material with small barrier height with silicon substrate and deep trapping level as charge trapping layer to achieve high program/erase speed and good reliability due to deep trapping level. In addition, high-k material has large dielectric constant, a wide band gap, high trap site density, so it is suitable for SONOS-type memory application.

1-2 Motivation

The serious leakage problem during retention can be eliminated by utilizing a semiconductor nanocrystal memory structure. Only the electrons stored on the nanocrystal directly above the defect chain will be affected since the nanocrystals are separated from each other within the gate oxide dielectric. Hence the tunnel oxide thickness in the nanocrystal memory device can be reduced to allow faster programming and lower voltage operation. In this thesis, we have designed a high performance nonvolatile memory with high-k CeO_2 nanocrystal charge trapping layer. Use this high-k layer replace the silicon nitride layer in the SONOS structure can gain many advantages. We also use several different source/drain implantation approaches to achieve superior characteristics in terms of large memory window, high program/erase speed, long retention time, low disturbance, and reduce off-state leakage current.

From the papers, we find the impact of metal work function (Φ_M) on memory properties of charge-trap-flash memory devices. Theoretical and experimental studies show that high Φ_M metal plays a key role in eliminating electron back tunneling (EBT) through the blocking dielectric during the erase operation. Therefore we choose suitable temperatures to anneal different metal gates, and apply these metals to n-channel SONOS memories.

1-3 Thesis Organization

In this thesis, we study the performance of the SONOS-type memory device used CeO_2 high-k dielectric as charge trapping layer

In Chapter 1, we introduce the background of the flash memory and explain why SONOS-type memory with high-k charge trapping layer is studied to replace the traditional floating gate memory.

In Chapter 2, we fabricate MoN and TaN capacitors, measuring C-V, I-V, and RES characteristics. And then we extract the flat band voltages of C-V curves, and metal work functions of MoN, TaN under different annealing temperatures.

In Chapter 3, we fabricate n-channel SONOS type memories by using CeO_2 charge trapping layer. And then we replace poly-Si gate with metal gate, discussing the electrical experiments. The results reveal that the program/erase speed and disturbances of our devices have good characteristics.

In Chapter 4, we fabricate SONOS type memory by using CeO_2 charge trapping layer and use different source/drain implantation approaches to achieve superior characteristics. We discuss the electrical experiments, and the results reveal that the program/erase speed, retention and disturbances of our devices have good characteristics.

At the end of this thesis, we make a conclusion in Chapter 5.

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Chapter 2

Physical and Electrical properties of MoN and TaN MOS Capacitors

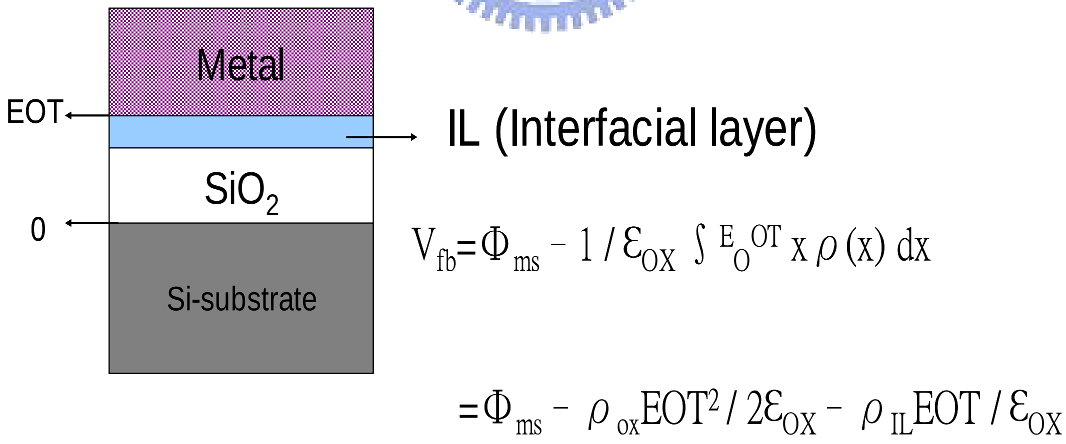
2-1 Introduction

The problems of polysilicon (poly-Si) gate depletion, high gate resistance, high gate tunneling leakage current, and boron penetration into the channel region become more severe as the channel length and gate-oxide thickness are aggressively reduced. Therefore, there is immense interest in metal gates and alternative gate dielectrics with high permittivity. Metal gates with work functions near the conduction and valence band edges of Si are desired for the N- and P-MOSFETs, respectively. An accurate understanding of the top interface of the gate dielectric, i.e., the metal–dielectric or the poly-Si–dielectric interface is important to achieving precise control of gate work functions and threshold voltages in transistors with high-k gate dielectrics.

In this work, we discuss the dependence of metal gate work functions on the different annealing temperatures. We found a systematic methodology to extract the accurate work function of metal gates. This methodology consists of the interfacial layer and decouples the impact of charges from the work function. We expect metal gate work-function can play a key role in eliminating electron back tunneling (EBT) through the blocking dielectric during the erase operation.

2-2 Experimental

Figure 2-1 schematically depicts the process flow of the proposed MIS capacitors. The fabrication process of the MoN and TaN MOS capacitors were started on n-type and p-type, 5-10 Ω cm, (100) 150mm silicon substrates. First, various silicon dioxide thickness (3.3nm, 10.6nm, 17.7nm, 35.1nm) were deposited by chemical vapor deposition in horizontal furnace system. In order to observe the effect of metal gate work function on memory properties, various metal materials on silicon dioxide with various thicknesses were prepared. Therefore MoN and TaN metals were deposited by sputtering method with pure Mo target and pure Ta target in the nitrogen and argon gas ambient. After that, the samples went through metal RTA treatment in N_2 ambient at various temperatures ($500^{O}C$, $600^{O}C$, $700^{O}C$) for 30 sec. Then all samples went through metal RTA treatment in N_2 ambient at $900^{O}C$ for 20 sec. Finally the backside of the samples was deposited with Al by sputtering method with pure Al target.



$$V_{fb}=\Phi_{ms}-1/\varepsilon_{OX}\int_{0}^{EOT}x\,\rho(x)\,dx$$

$$=\Phi_{ms}-\rho_{ox}EOT^2/2\varepsilon_{OX}-\rho_{IL}EOT/\varepsilon_{OX}$$

Fig. 2-1 The process flow of the MoN and TaN MOS capacitors.

2-3 Results and Discussion

In this section, the physical and electrical characteristics of MoN and TaN MOS capacitors were discussed.

Fig. 2-2 shows the relation of flat band voltage and effective oxide thickness (EOT) for TaN MOS Capacitors. First, we have four thicknesses of TaN MOS capacitors, annealing them at different temperatures. Then we measure C-V curves, using a systematic methodology to extract the accurate flat band voltage of TaN MOS capacitors, as depicted in Fig. 2-2.We found three lines were intercepted in the same point. Because thermal budget of 900°C is larger than that of 500°C, 600°C,and 700°C. We also found that if TaN metal did not go to a pre-annealing step (such as 500°C,600°C ,700°C) to densify metal before treatment in N_2 ambient at 900°C for 20 sec, the characteristics of TaN MOS capacitors will very bad. The slope of three lines stands for effective oxide charge.

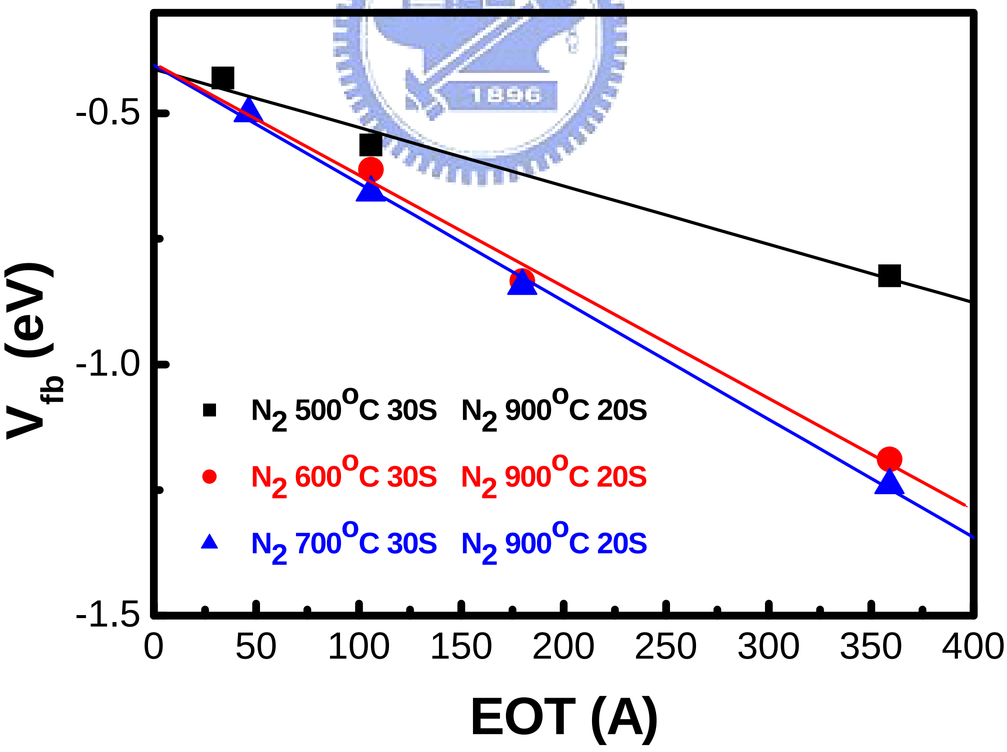


Fig. 2-2 The relation of flat band voltage and effective oxide thickness (EOT) under different annealing conditions for TaN MOS capacitors.

Fig. 2-3 shows the relation of flat band voltage and effective oxide thickness (EOT) for MoN MOS Capacitors. Like TaN MOS Capacitors we measure C-V curves, using a systematic methodology to extract the accurate flat band voltage of MoN MOS capacitors, as depicted in Fig. 2-3. Unlike TaN MOS Capacitors, if MoN metal did not go to a pre-annealing step (such as 500^{o}C and 600^{o}C) to densify metal before treatment in N_2 ambient at 900^{O}C for 20 sec, the characteristics of MoN MOS capacitors will not bad. The slope of three lines stands for effective oxide charge.

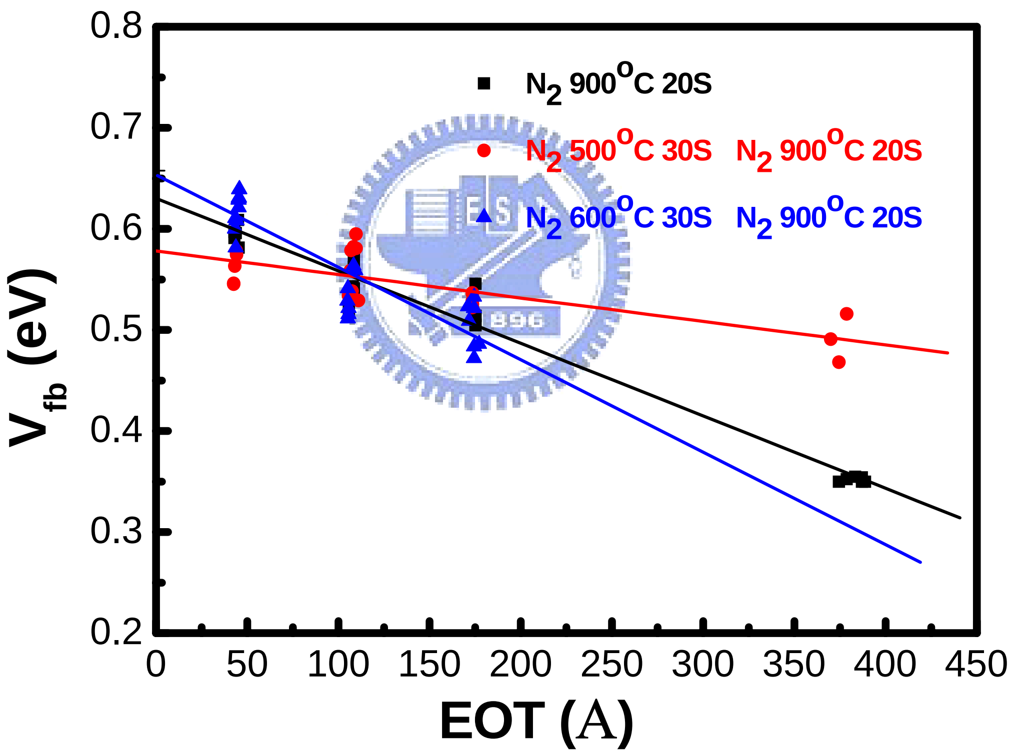


Fig. 2-3 The relation of flat band voltage and effective oxide thickness (EOT) under different annealing conditions for MoN MOS capacitors.

Fig. 2-4 shows work function of TaN metal and current density at Vg = 1V under different annealing conditions. From Fig. 2-2, intercept at Y-axis, when EOT=0 the value of flat band voltage can extract work function of TaN . It shows almost the same work function value. The right Y-axis show the current density at Vg = 1V , TaN metal did not go to a pre-annealing step (such as 500°C ,600°C ,700°C) to densify metal before treatment in N_2 ambient at 900°C for 20 sec , which has the maximum leakage current density . Another TaN metal went to a 700°C pre-annealing step, which has the minimum leakage current density.

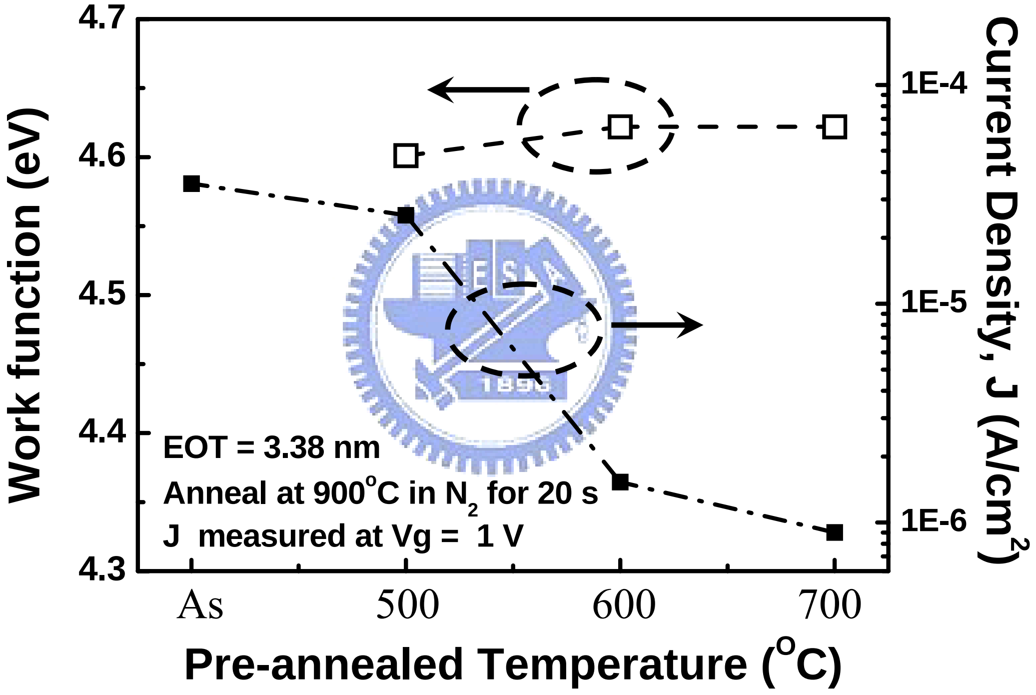


Fig. 2-4 Work function of TaN metal and current density at Vg = 1V under different annealing conditions.

Fig. 2-5 shows work function of MoN metal and current density at Vg = -1V under different annealing conditions. From Fig. 2-3, intercept at Y-axis, when EOT=0 the value of flat band voltage can extract work function of MoN. The metal work function value ranges about 0.1eV (about 4.9eV~5eV). The right Y-axis show the current density at Vg = -1V , MoN metal went to a 500°C pre-annealing step to densify metal before treatment in N_2 ambient at 900°C for 20 sec , which has the maximum leakage current density . Another MoN metal went to a 600°C pre-annealing step, which has the minimum leakage current density.

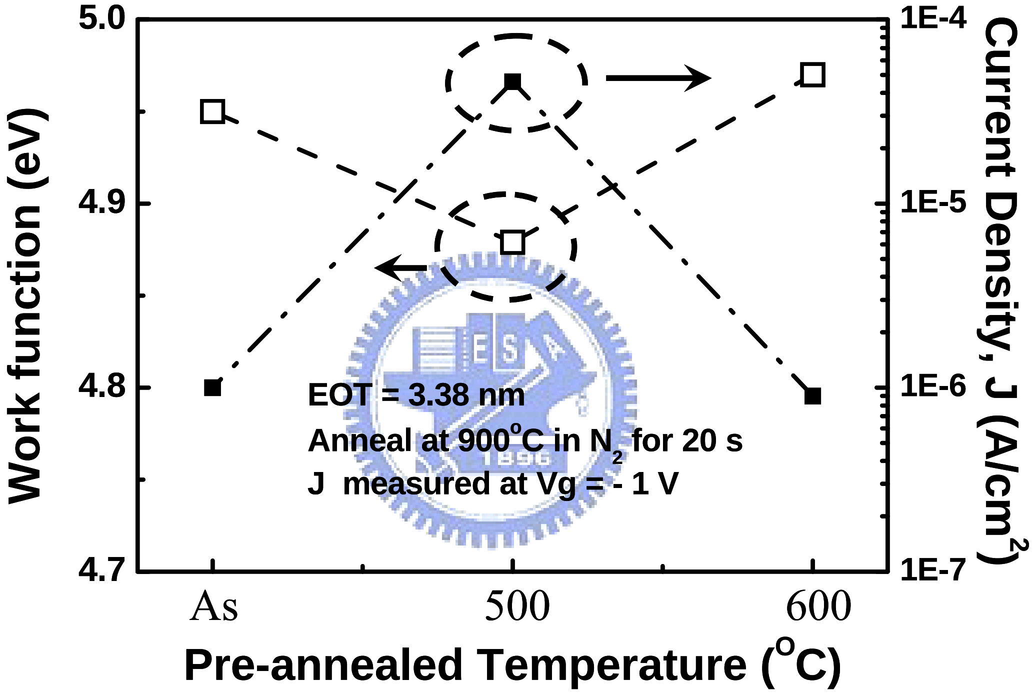


Fig. 2-5 Work function of MoN metal and current density at Vg = - 1V under different annealing conditions.

From the above pictures, we plot a table to show work function and current density for different metal and annealing conditions. As depicted in Table2-1.

Material	Condition (^{O}C)	WF (eV)	Jg atV=1V (A/cm^{-2})
MoN	AS→900	4.95	9.99E-07
MoN	500→900	4.879	4.59E-05
MoN	600→900	4.97	9.01E-07
TaN	500→900	4.601	2.54E-05
TaN	600→900	4.622	1.53E-06
TaN	700→900	4.622	9.00E-07

Table 2-1 Work function and current density for TaN and MoN metal.

2-4 Summary

In this chapter, we found the work function of TaN was about 4.6eV. It located at the midgap of energy level, so we choose a 700^{o}C pre-annealing step to densify metal and then treatment at 900^{O}C for 20 sec to fabricate NMOS and PMOS. In the other hand, for MoN metal we choose a 600^{o}C pre-annealing step to densify metal and then treatment at 900^{O}C for 20 sec to fabricate NMOS.

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Chapter 3

Characteristics of High-K CeO_2 Nanocrystal Memory with Different Metal Gates

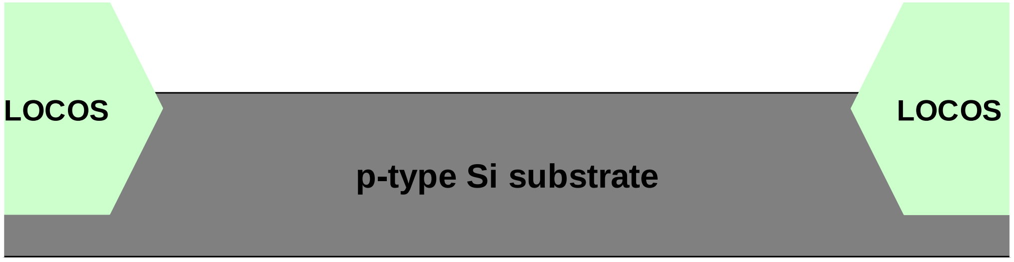
3-1 Introduction

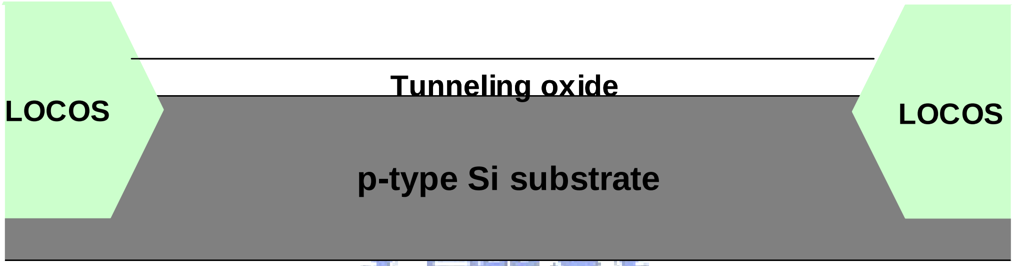
Charge trapping flash(CTF) memory devices have received considerable attention due to the detrimental coupling effect among adjacent cells in sub-50nm NAND type floating gate flash memory devices. Nitride based CTF memory devices have several advantages such as fast programming, low power operation, high density integration, good reliability characteristics, and high compatibility with conventional CMOS technology. However, it is difficult to satisfy the NAND specifications of low erase state Vth of –3V from 1V at –18V for 2ms and good retention characteristics because the current through the tunnel dielectric thickness critically affects both properties and the electron back tunneling (EBT) during erase operation limits the low erase state Vth . EBT is known to a serious concern for meeting specification of NAND devices using Fowler-Nordheim (FN) program and erase schemes. The experimental studies show that high work-function metal gate and high permittivity (high-K) dielectric play a key role in eliminating electron back tunneling (EBT) through the blocking dielectric during the erase operation.

In this work, in order to reconcile this conflicting behavior, we have carried out a study on the impact of work function of metal gate and high permittivity (high-K) dielectric on the memory properties of CeO_2 based CTF devices. Techniques to improve erase efficiency of CTF memory devices with different metal gates by using n-channel CeO_2 based CTF devices are discussed. In the past, n-channel flash cells were widely used in the design of flash memory products. However, the requirement of high voltage operation for channel-hot-electron (CHE) programming results in a large power consumption. In order to improve it, the p-channel flash cell has been suggested for low voltage and low power applications. A more matured p-channel cell using band-to-hand tunneling induced hot electron injection (BBHE) has later been proposed .We demonstrate reliability enhancement for n-channel and p-channel flash cells.

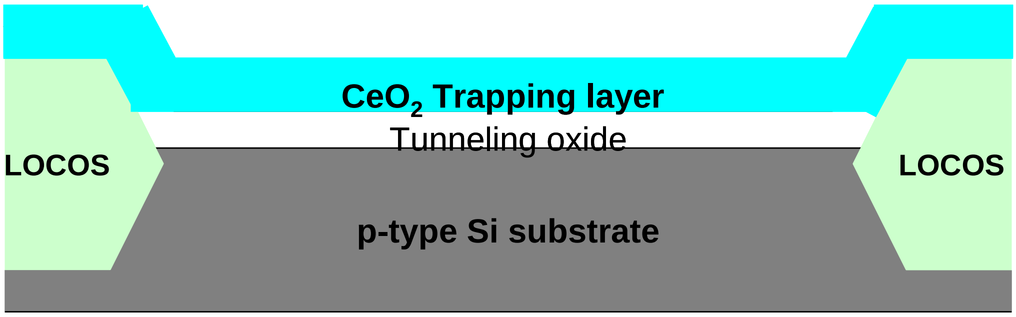
3-2 Experimental

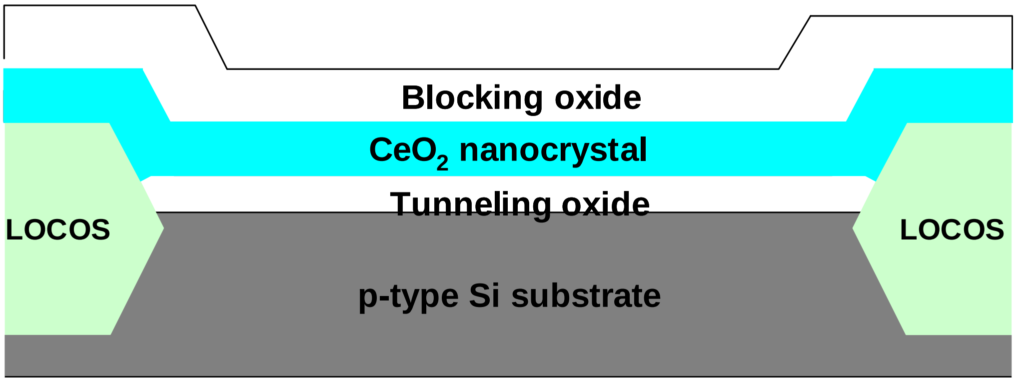
Figure 4-1 schematically depicts the process flow of the proposed SONOS flash memory. The fabrication process of the CeO_2 nanocrystal memory devices involved was started with the LOCOS isolation process on p-type and n-type, 5-10 Ω cm, (100) 150mm silicon substrates. First, a 3 nm thick tunnel oxide was thermally grown at $1000^{O}C$ in vertical furnace system. The trapping layer of CeO_2 layer was deposited by dual E-gun method with CeO_2 target . After that, the samples went through RTA treatment in O_2 ambient at $900^{O}C$ for 1 minute. A blocking oxide of about 20 nm thick was then deposited by high density plasma chemical vapor deposition (HDPCVD) . After that, the sample went through RTA treatment in O_2 ambient at $900^{O}C$ for 1 minute. For control samples, a 200 nm thick poly-silicon was deposited to serve as the gate electrode by LPCVD. In addition another metal gates 100nm MoN and TaN were deposited by sputtering method with pure Mo target and pure Ta target in the nitrogen and argon gas ambient. Then, gate electrode was patterned. For NMOSFET ,the source/drain and gate were doped by self-aligned P ion implantation at the dosage and energy of 5×10^{15} ions/cm^{-2} and 25 KeV, then the substrate contact was patterned and the sub-contact was implanted with BF_2 at the dosage and energy of 5×10^{15} ions/cm^{-2} and 40 KeV . For PMOSFET ,the source/drain and gate were doped by self-aligned BF_2 ion implantation at the dosage and energy of 5×10^{15} ions/cm^{-2} and 25 KeV, then the substrate contact was patterned and the sub-contact was implanted with P at the dosage and energy of 5×10^{15} ions/cm^{-2} and 40 KeV. After these implantations, for NMOSFET the dopants were activated at $950^{O}C$ for 20 sec, For PMOSFET the dopants were activated at $950^{O}C$ for 10 sec. The rest of the subsequent standard CMOS procedures were complete for fabricating the CeO_2 high-k memory devices.

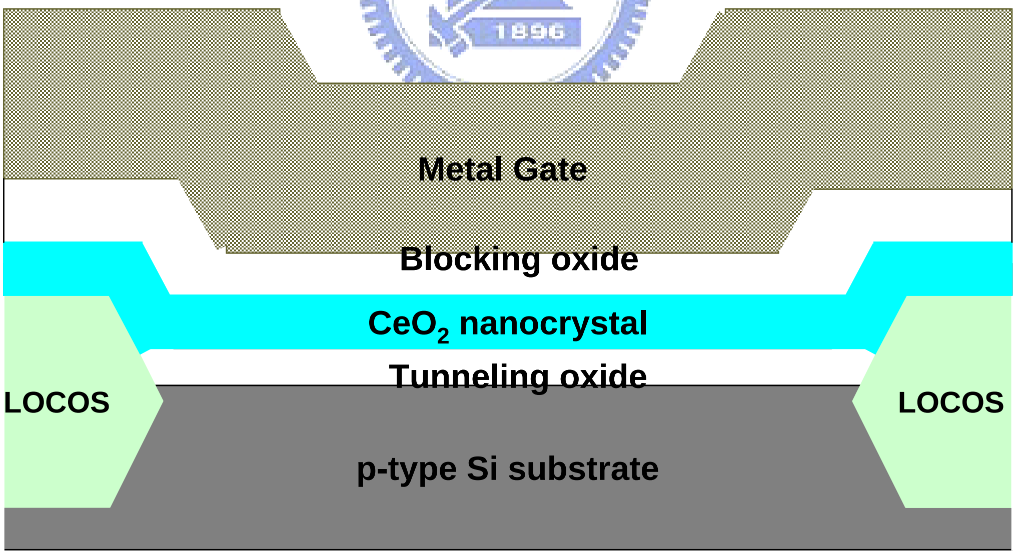


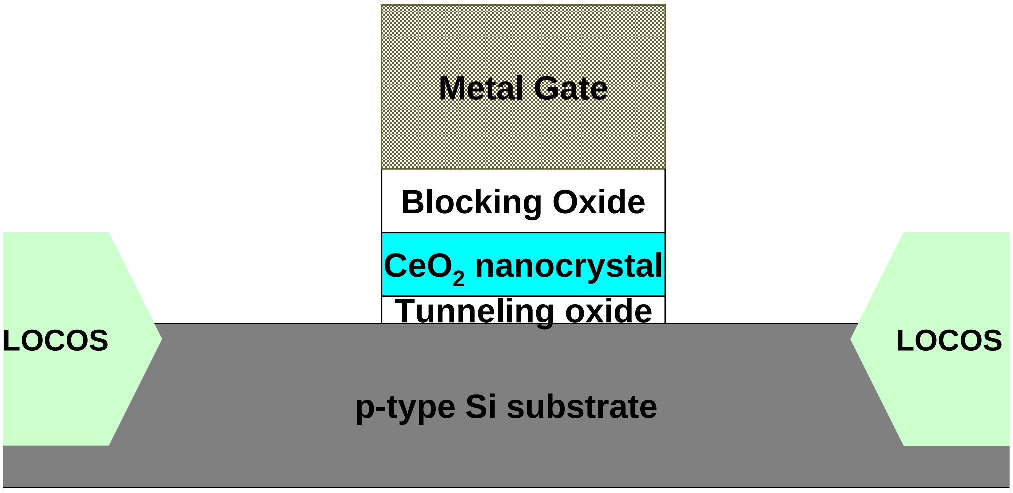


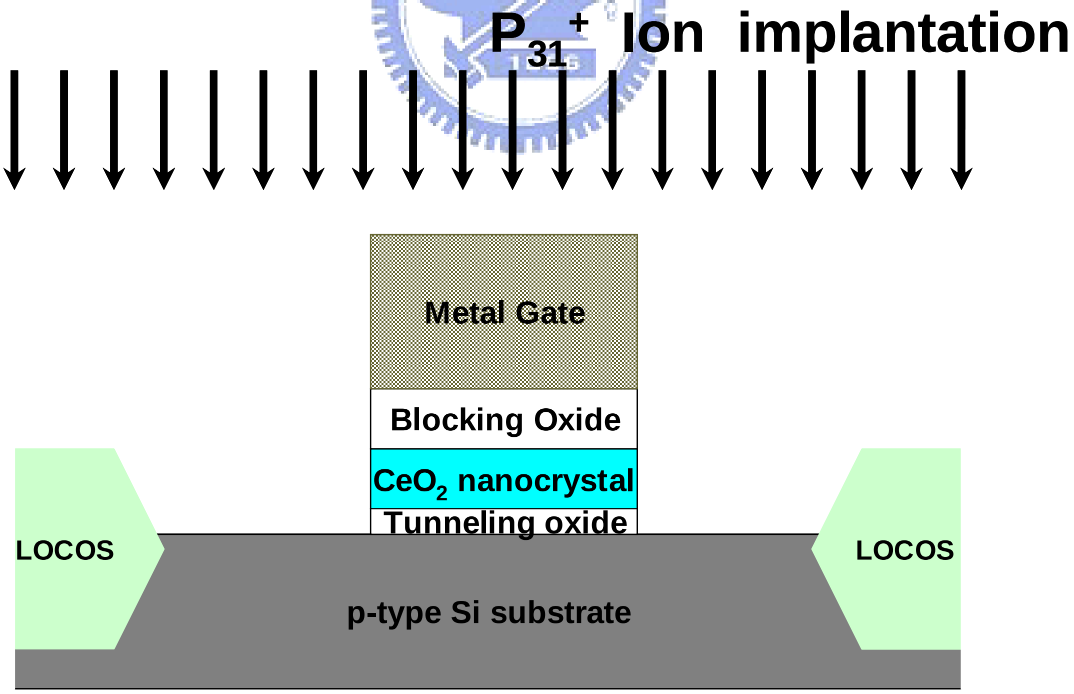
O_2 RTA $900^{O}C$ 60sec
form CeO_2 nanocrystal




Blocking oxide
CeO_2 nanocrystal
Tunneling oxide
LOCOS
LOCOS
p-type Si substrate


Metal Gate
Blocking oxide
CeO_2 nanocrystal
Tunneling oxide
LOCOS
LOCOS
p-type Si substrate


Metal Gate
Blocking Oxide
CeO_2 nanocrystal
Tunneling oxide
LOCOS
LOCOS
p-type Si substrate


P_{31}^{+} Ion implantation
Metal Gate
Blocking Oxide
CeO_2 nanocrystal
Tunneling oxide
LOCOS
LOCOS
p-type Si substrate

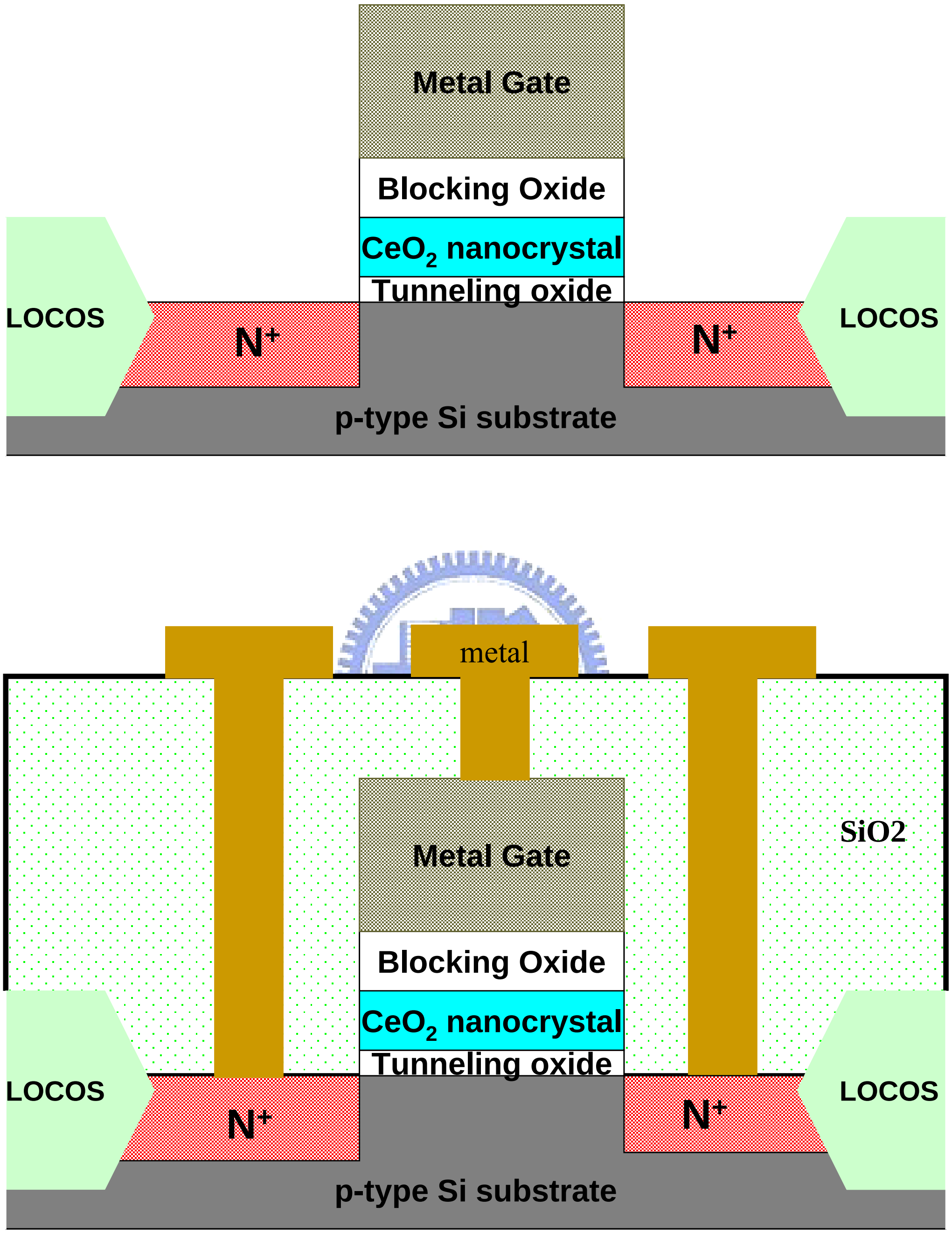


Fig. 3-1 The process flow of the metal gate flash memory and the cross-section of the metal gate flash memory .

3-3 Results and Discussion

In this section, the electrical characteristics of metal gate high-k CeO_2 nanocrystal SONOS-type memory were discussed.

3-3-1 Id-Vg Curve

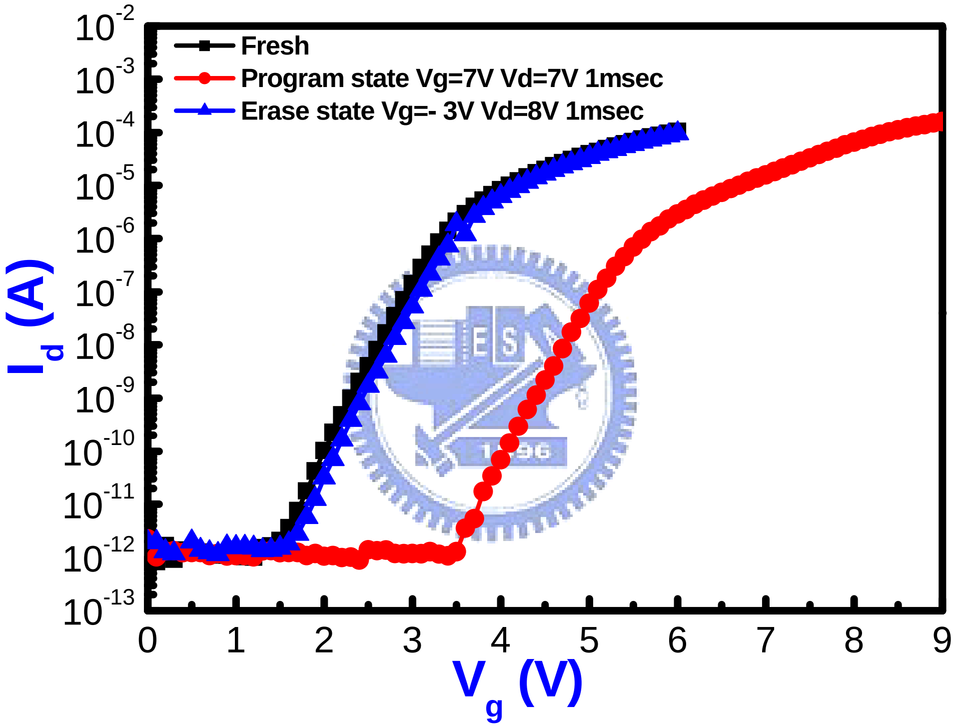


Fig. 3-2 The Id-Vg curves of the MoN metal gate flash memory in the programmed and erased state.

Figure 3-2 shows the Id-Vg curve of the device under program and erase operations. We use channel hot electron injection (CHEI) to program and band to band hot hole to erase (BTBHH). The program condition is Vg= 7V, Vd= 7V with 1 msec stress. The erase condition are Vg= -3V, Vd= 8V with 1 msec stress. The Vth after programming shifts about 2V from the original fresh state. After erasing, the Vth shifts leftward 1.9V. So the memory window is about 2V.

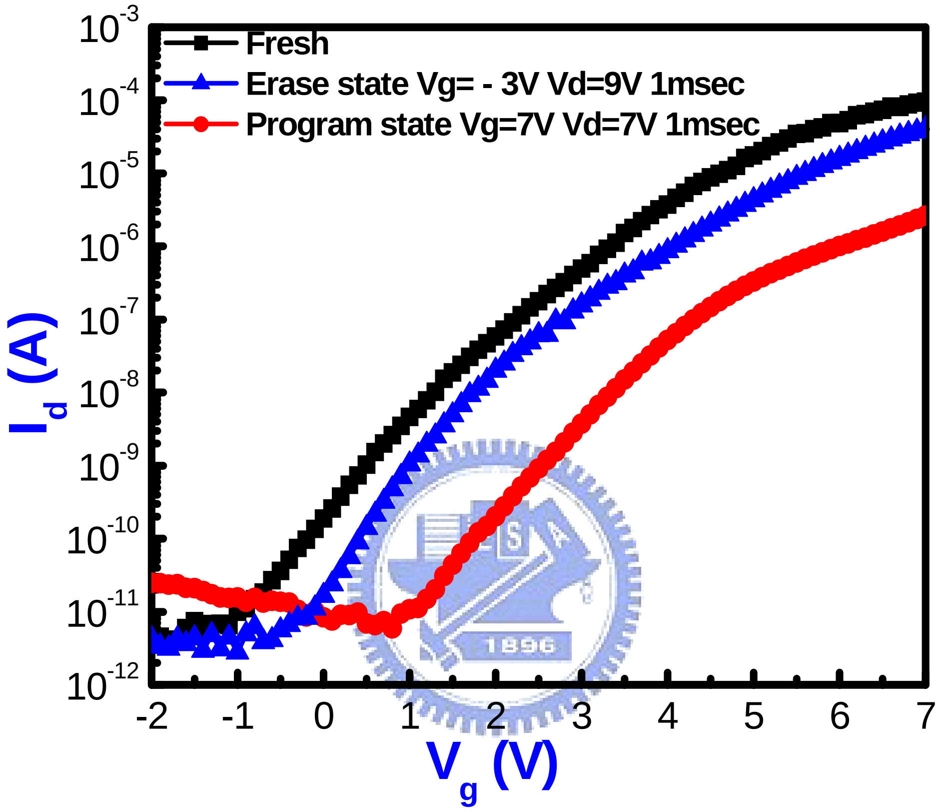


Fig. 3-3 The Id-Vg curves of the TaN metal gate flash memory in the programmed and erased state.

Figure 3-3 shows the Id-Vg curve of the device under program and erase operations. We use CHEI to program and BTBHH to erase. The program condition is Vg= 7V, Vd= 7V with 1 msec stress. The erase condition are Vg= -3V, Vd= 9V with 1 msec stress. The memory window is about 2V.

3-3-2 Program and Erase Speed

For the high-k CeO_2 nanocrystal SONOS-type flash memory with MoN metal gate, the program speed is shown in Fig.3-4.

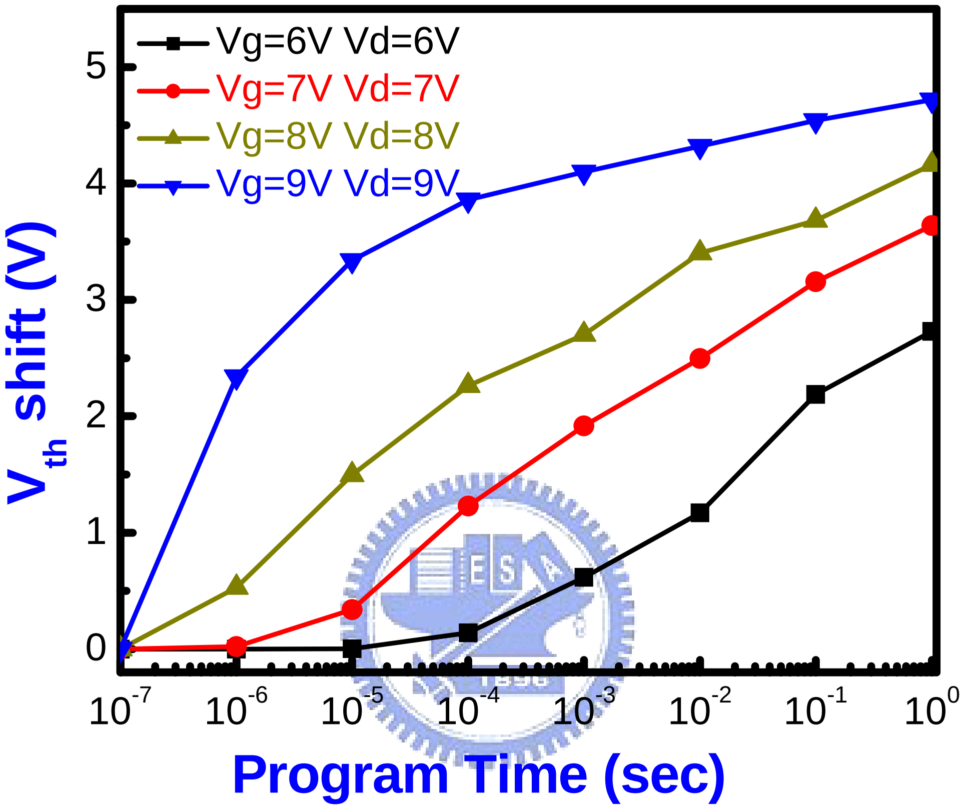


Fig. 3-4 The program speed curves of high-k CeO_2 nanocrystal SONOS-type flash memory with MoN metal gate.

We show four different stress conditions: Vg=6V,Vd=6V ; Vg=7V,Vd=7V; Vg=8V,Vd=8V ; Vg=9V,Vd=9V. As Fig. 3-4 shows, the condition Vg=7V, Vd=7V, 1 msec cause Vth shift about 2V; and the condition Vg=8V, Vd=8V, 0.1 msec cause Vth shift over 2V. Its memory window is > 4V. At large voltage (such as > Vg=9V, Vd =9), the program speed is very fast within short time. Like the condition Vg=9V, Vd =9V, 1 usec cause Vth shift 2.3V.

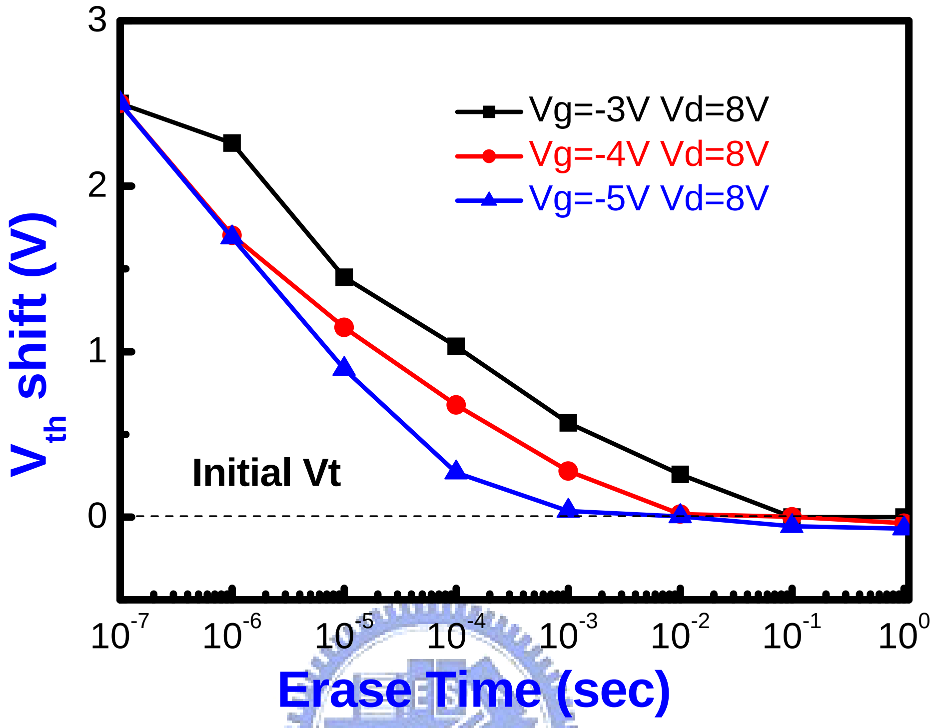


Fig. 3-5 The erase speed curves of high-k CeO_2 nanocrystal SONOS-type flash memory with MoN metal gate.

Figure 3-5 shows the erase speed of the MoN metal gate device. For Vg= -3V, -4V, and -5V with the same Vd =8V. We can see all stress conditions the Vth shift > 2V in 10msec. The final erase state is below the initial state. Therefore it shows no electron back tunneling (EBT) and a little over-erase.

For the high-k CeO_2 nanocrystal SONOS-type flash memory with TaN metal gate, the program speed is shown in Fig.3-6. We show three different stress conditions: Vg=5V, Vd=5V; Vg=6V, Vd=6V; Vg=7V, Vd=7V. As Fig. 3-6 shows, the condition Vg=7V, Vd =7V, 1 msec cause Vth shift about 2V. Its memory window is > 5V.

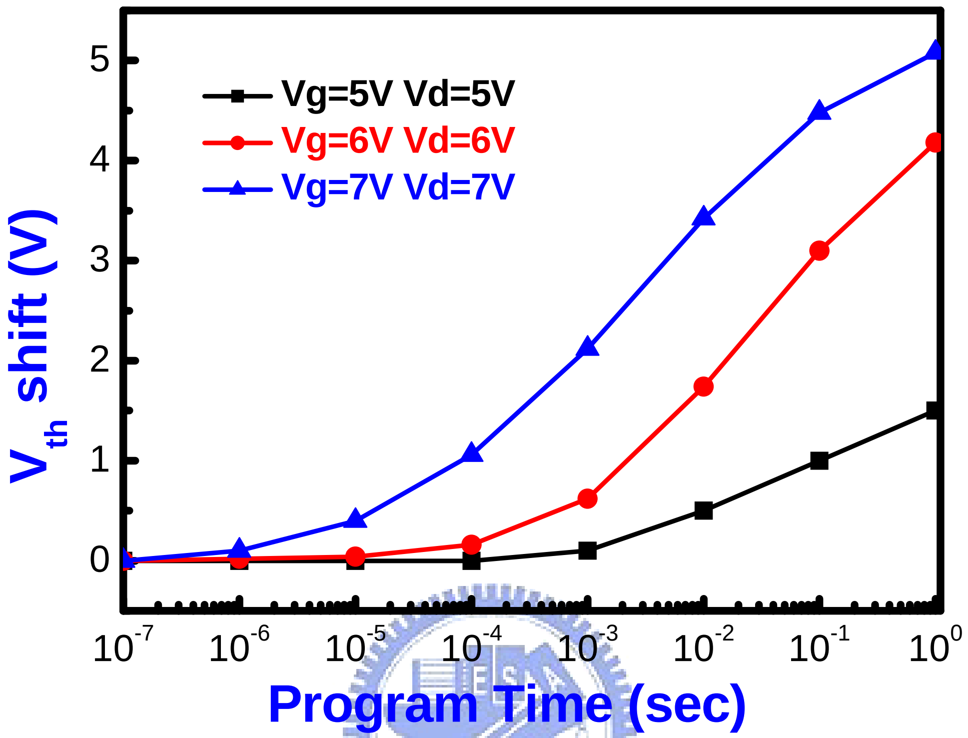


Fig. 3-6 The program speed curves of high-k CeO_2 nanocrystal SONOS-type flash memory with TaN metal gate.

Figure 3-7 shows the erase speed of the TaN metal gate device. For Vg= -3V, -4V, and -5V with the same Vd=9V. We can see all stress conditions the Vth shift > 2V in 10msec. And Vt shift of -2V can be achieved with Vg=-4 Vd=9V t <1ms .The final erase state is below the initial state. Because it has no electron back tunneling (EBT), so it shows over-erase under large erase voltage (such as Vg= -4V ,Vd=9V and Vg= -5V ,Vd=9V).

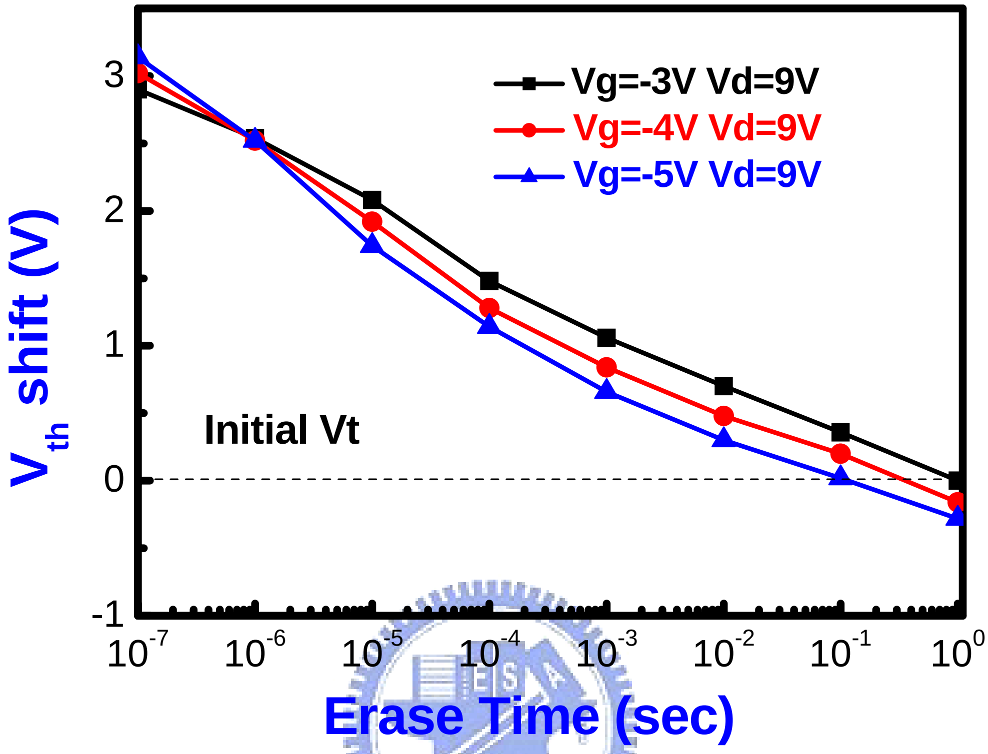


Fig. 3-7 The erase speed curves of high-k CeO_2 nanocrystal SONOS-type flash memory with TaN metal gate.

Figure 3-8 shows the erase speed of the N^+-poly and MoN metal gate device. To be clearly understood EBT phenomenon, we use F-N tunneling mechanism to erase. For N^+-poly gate, we can see a little Vth shift under small voltage (Vg=-15V). And EBT phenomenon occurs when we apply large voltage to it (Vg=-18V). For MoN metal gate, it has no EBT under whether large nor small voltage. It shows reasonable erase speed for MoN metal gate device.

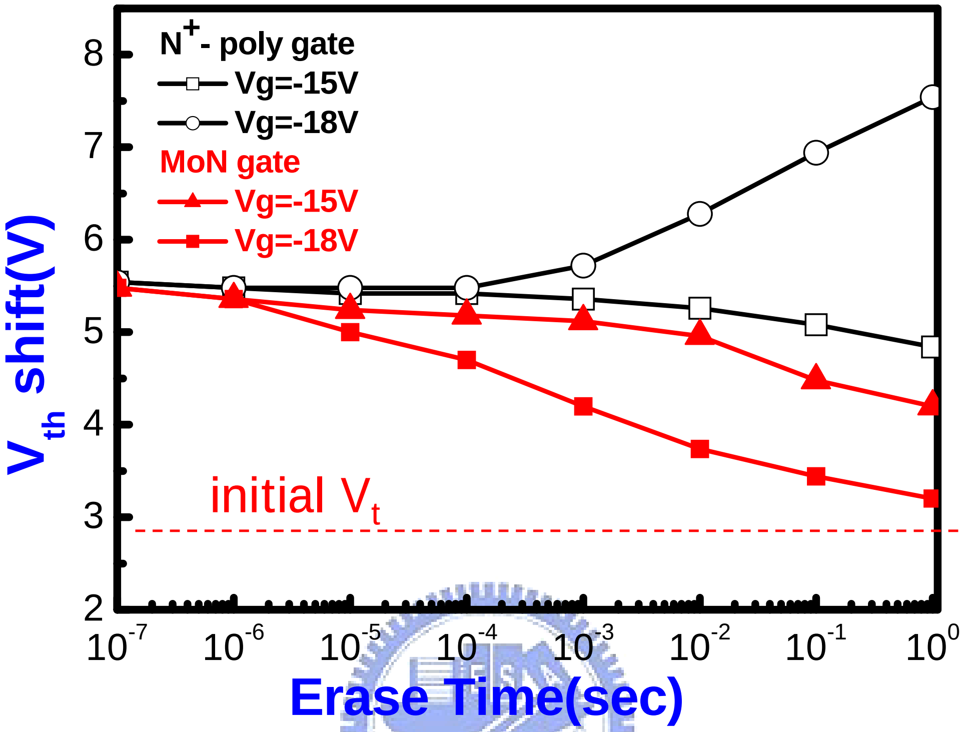


Fig. 3-8 The erase speed curves of N^+-poly and MoN gate CeO_2 nanocrystal memory with F-N tunneling mechanism.

3-3-3 Data Retention Characteristic

Fig. 3-9 is the data retention characteristic of MoN metal gate high-k CeO_2 nanocrystal SONOS memory measured at 25°C. We find the small charge loss with time .The curve shows only 5 % charge loss as measure time up to 10^4 sec and 13% charge loss up to 10^8 sec at 25°C. We infer the small charge loss at room temperature is from the electron deep trap of high-k CeO_2 nanocrystal. We prove that sputtering MoN and TaN metal will not damage the blocking oxide and CeO_2 layer, so it shows good retention characteristic.

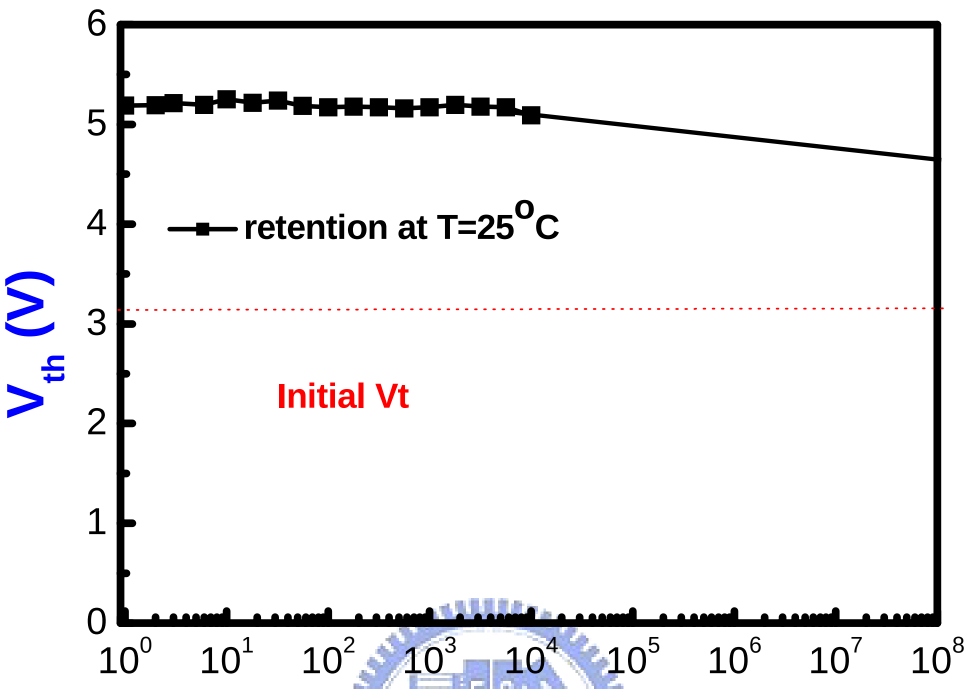


Fig. 3-9 Retention characteristic of MoN metal gate high-k CeO_2 nanocrystal SONOS-type flash memory at 25^{O}C.

3-3-4 Disturbance Measurement

Figure 3-10 shows the gate disturbance measurement of the MoN metal gate device for three stress conditions: Vg=7V, Vg= 9V and Vg=11V with Vd =Vs=Vb=0V. And Figure 3-11 shows the gate disturbance measurement of the TaN metal gate device for three stress conditions: Vg=6V, Vg= 8V and Vg=10V with Vd =Vs=Vb=0V. The applied gate voltage will attract electrons in the substrate tunneling to the CeO_2 layer by FN tunneling mechanism and result into Vth increase. After 1000 sec stress, the fresh state Vth are almost the same. It shows almost no gate disturbance after 1000 sec stress.

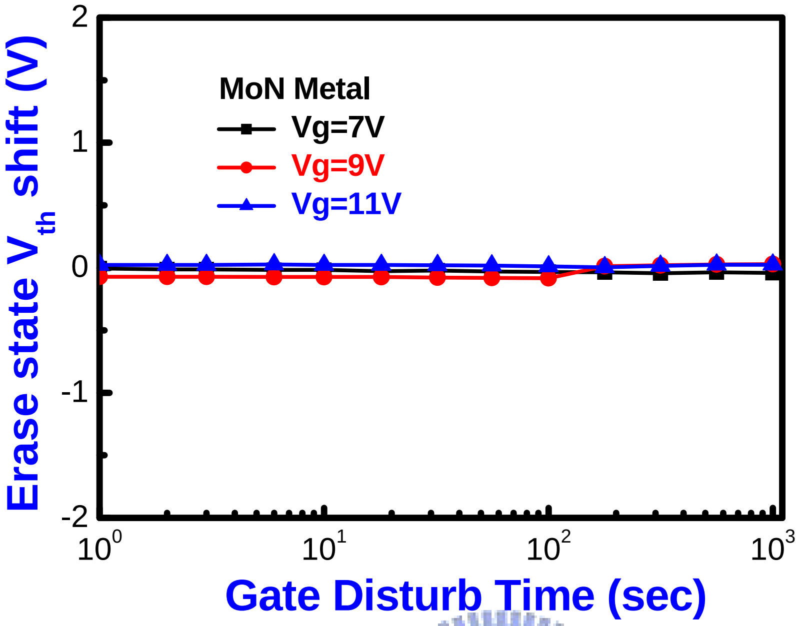


Fig. 3-10 The gate disturbance characteristics of MoN metal gate device.

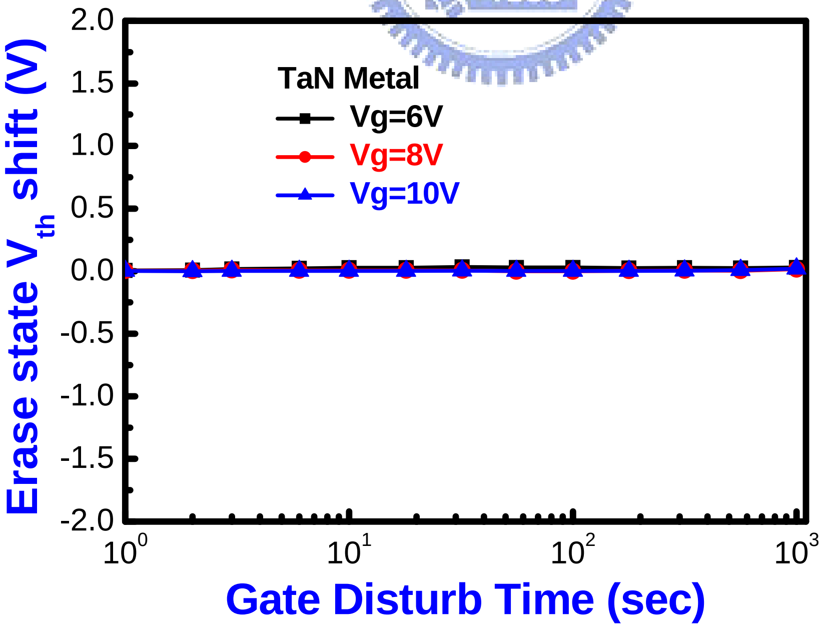


Fig. 3-11 The gate disturbance characteristics of TaN metal gate device.

Figure 3-12 shows the read disturbance measurement of the MoN metal gate device. And Figure 3-13 shows the read disturbance measurement of the TaN metal gate device. The measurement conditions are all fixed Vg=4V with different Vd= 2V, 3V, and 4V for 1000 sec stress. The stress caused the fresh state Vth increase almost 0V. It shows almost no read disturbance after 1000 sec stress.

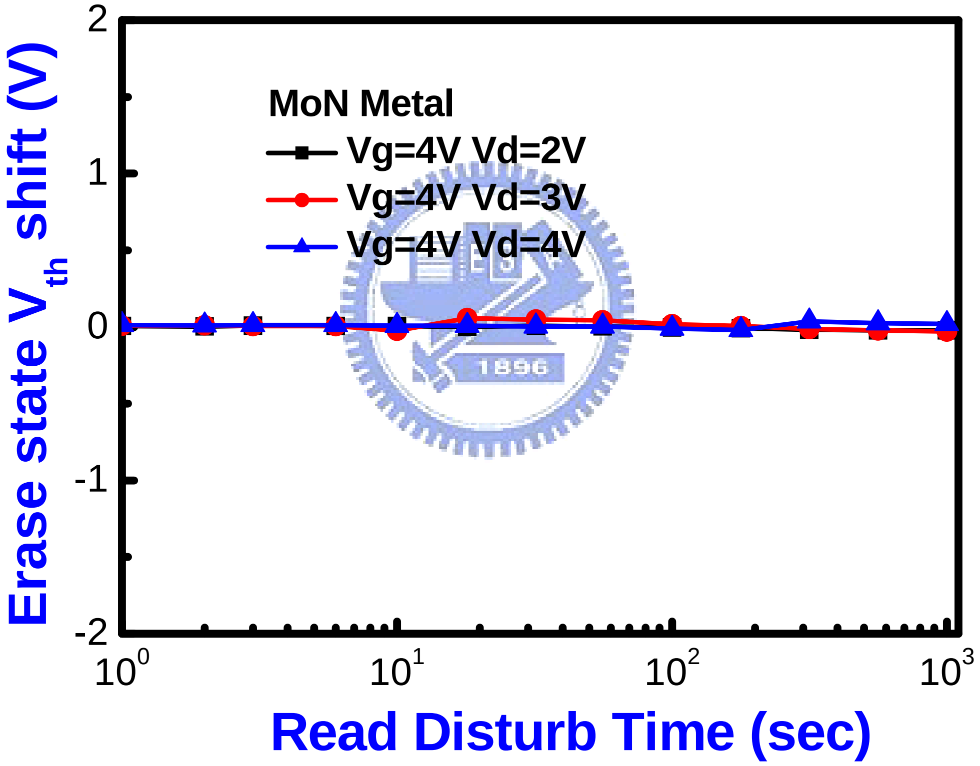


Fig. 3-12 The read disturbance characteristics of MoN metal gate device.

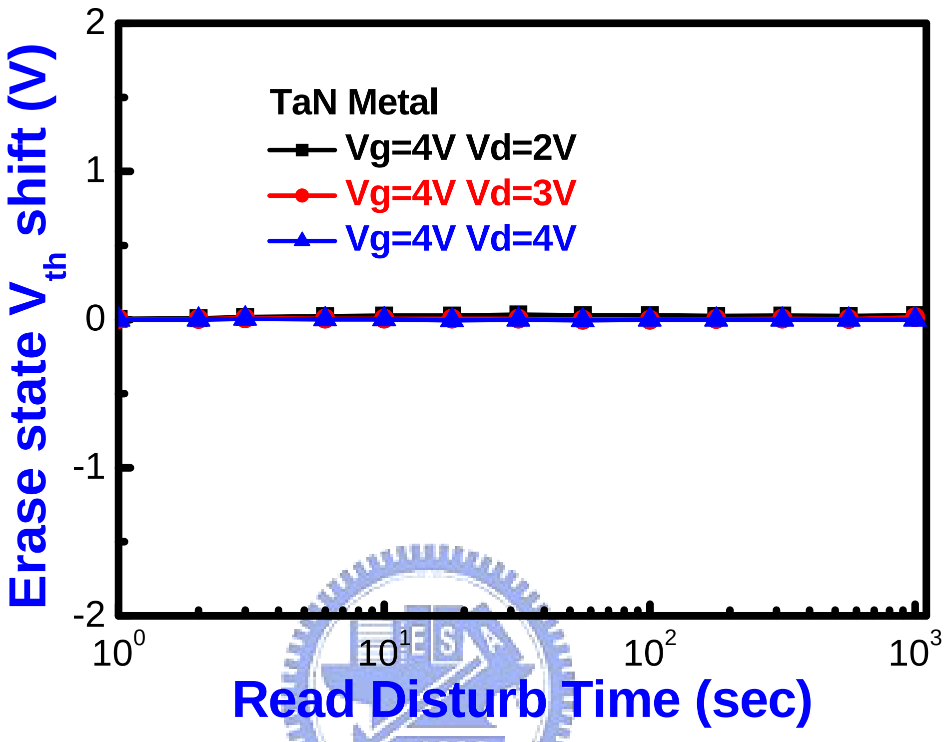


Fig. 3-13 The gate disturbance characteristics of TaN metal gate device.

3-3-5 Physical Characteristics

Fig. 3-14 shows the X-ray diffraction (XRD) characteristic of MoN metal gate device. The incident angle ranges from 15 degree to 60 degree. We find signal intensity peak appears at 32.85 degree. By searching the data base, we find the rate between Mo and N element is 1:1.

Fig. 3-15 shows the X-ray diffraction (XRD) characteristic of TaN metal gate device. The incident angle ranges from 15 degree to 60 degree. We find signal intensity peak appears at 33 degree. By searching the data base, we find the rate between Ta and N element is 2:0.86.

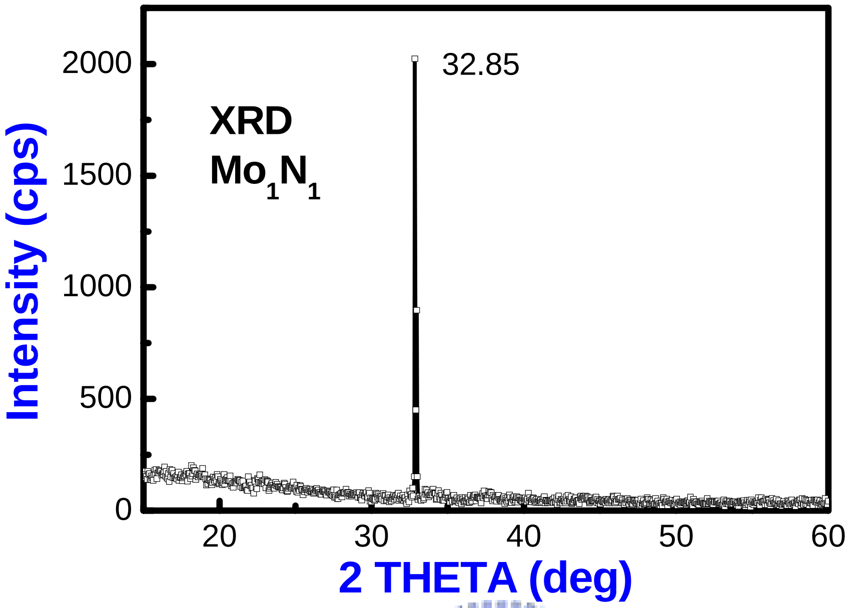


Fig. 3-14 The XRD characteristic of MoN metal gate device.

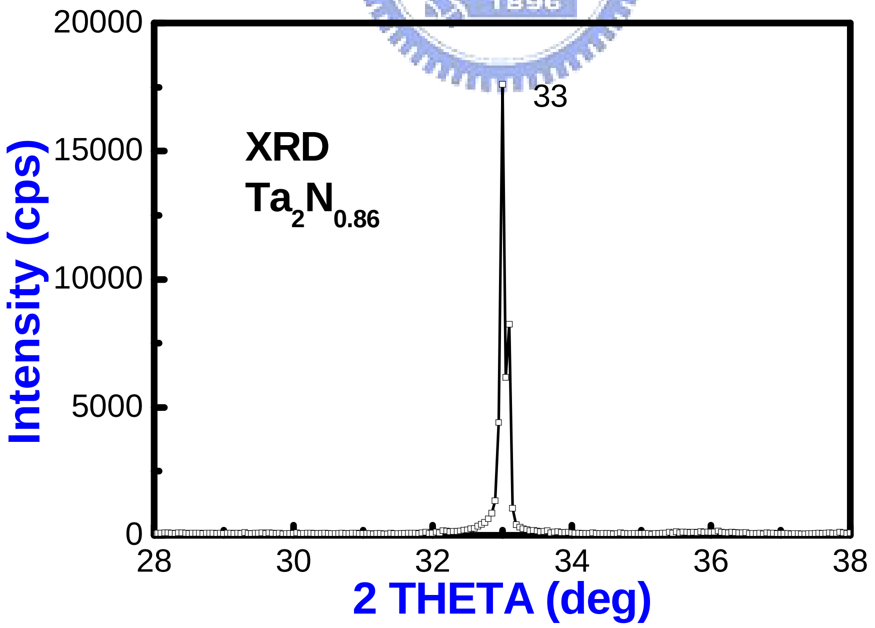


Fig. 3-15 The XRD characteristic of TaN metal gate device.

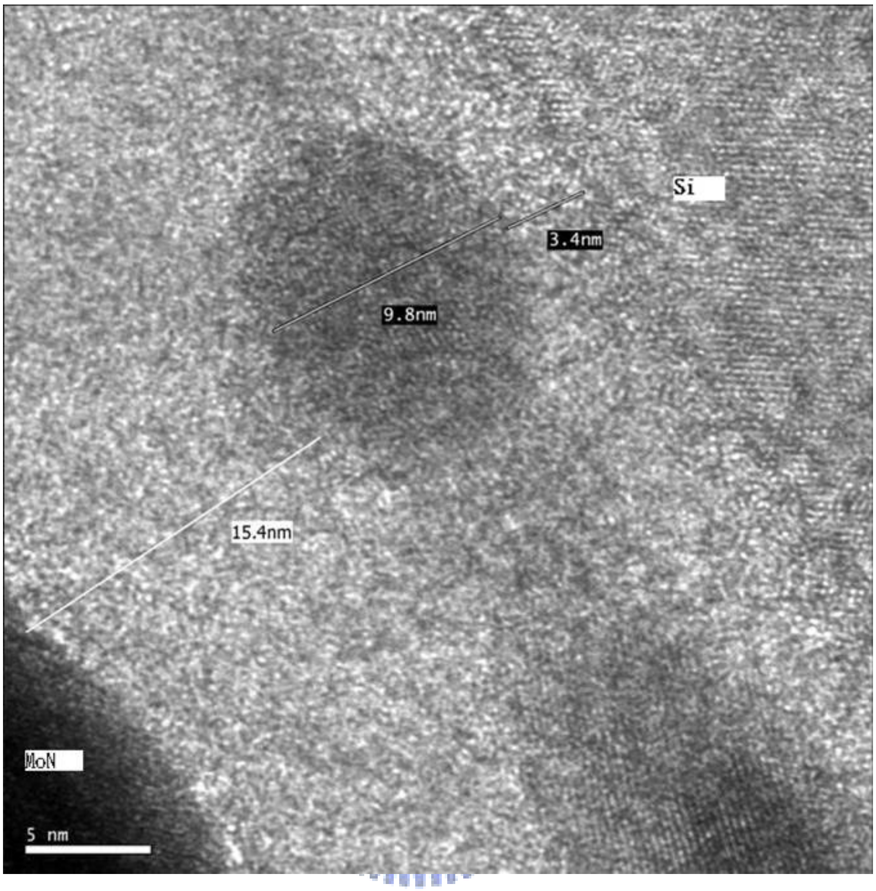


Fig. 3-16 The TEM image of MoN metal gate device.

Fig. 3-16 shows the cross-section-view high resolution tunneling electron microscopy (HRTEM) of MoN metal gate device. From the image, the isolation of the nanocrystals prevents the formation of effective conductive paths between adjacent nodes. The thickness of the tunnel oxide and blocking oxide are about 3.4nm and 15.4nm, and the thickness of the MoN metal is about 93.2nm. The nanocrystal size ranges from 7.5nm to 9.8nm.

3-4 Summary

In this chapter, we replace conventional poly-Si gate with metal gate MoN, TaN. We have shown the electric curves, like Id-Vg, program speed, erase speed, and small disturbance. We improve erase efficiency of high-k CeO_2 nanocrystal memory with different metal gates by using p-channel and n-channel devices .We also demonstrate the quality of high-k CeO_2 nanocrystal with some good characteristics.

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Chapter 4

Characteristics of High-K CeO_2 Nanocrystal Memory with Different Source/Drain Implantations

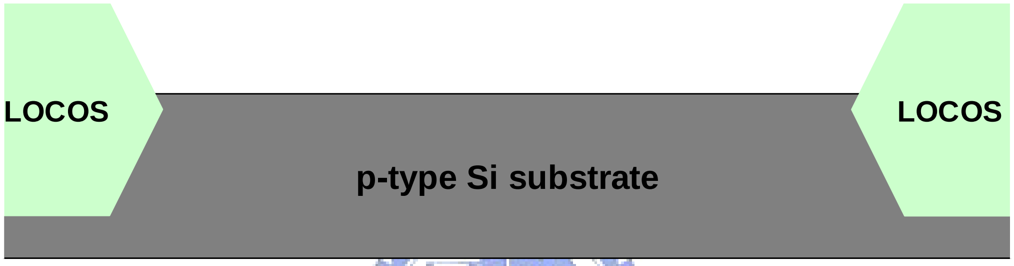
4-1 Introduction

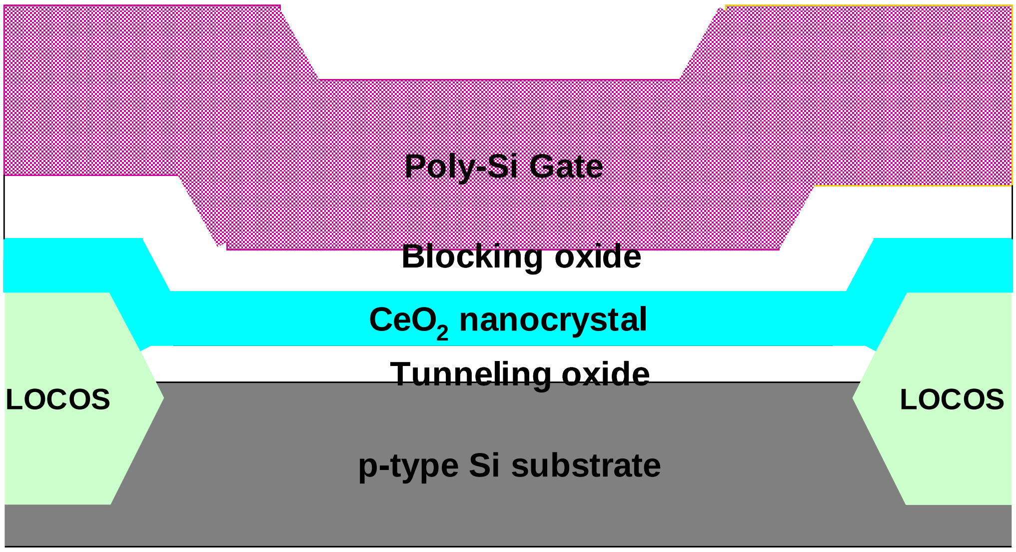
Recently SONOS-type memory has received considerable interest as one of the most promising candidates to replace the conventional floating-gate flash memory. Because as the tunnel oxide thickness is scaled below 80 Å, the stress-induced leakage current (SILC) has become such a severe problem that it will be a formidable challenge for floating-gate devices to meet the ten-year retention requirement. However, for the SONOS device, due to its discrete charge trapping nature, it is more robust to SILC since there is no lateral charges movement to discharge the whole memory as one single defect is generated in the tunnel oxide. In addition SONOS memory has low operation voltage, better endurance, and good compatibility with conventional CMOS process. However, achieving fast programming and long retention at the same time remains to be one challenge for SONOS devices. Various approaches have been proposed for improving the SONOS performance and reliability.

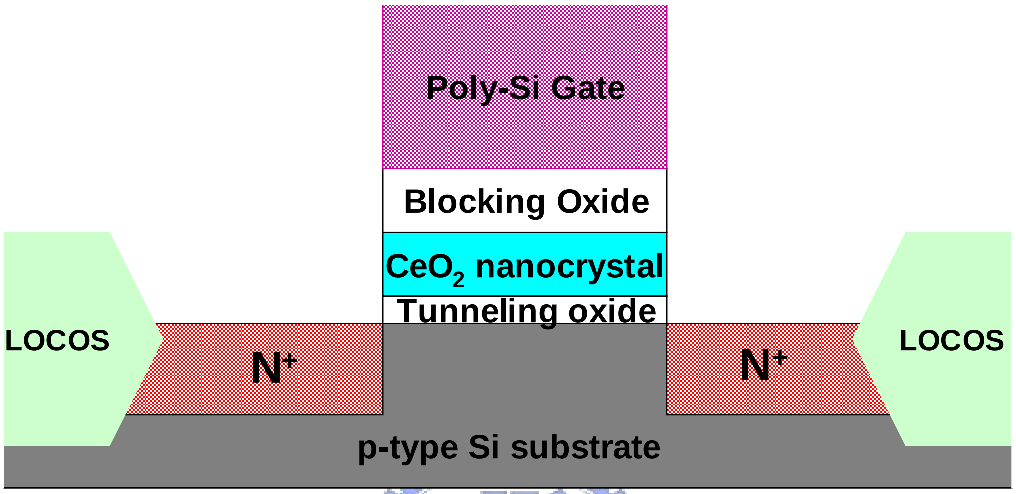
In this work, we purpose a high performance nonvolatile memory with high-k CeO_2 nanocrystal charge trapping layer. The serious leakage problem during retention can be eliminated by utilizing a nanocrystal memory structure. The electrons stored on the nanocrystal directly above the defect chain will be affected since the nanocrystals are separated from each other within the gate oxide dielectric. The tunnel oxide thickness in the nanocrystal memory device can be reduced to allow faster programming and lower voltage operation. We also use different source/drain implantation approaches to achieve superior memory characteristics.

4-2 Experimental

Figure 4-1 schematically depicts the process flow of the proposed SONOS flash memory.






Poly-Si Gate
Blocking Oxide
CeO_2 nanocrystal
Tunneling oxide
LOCOS
N^+
N^+
LOCOS
p-type Si substrate

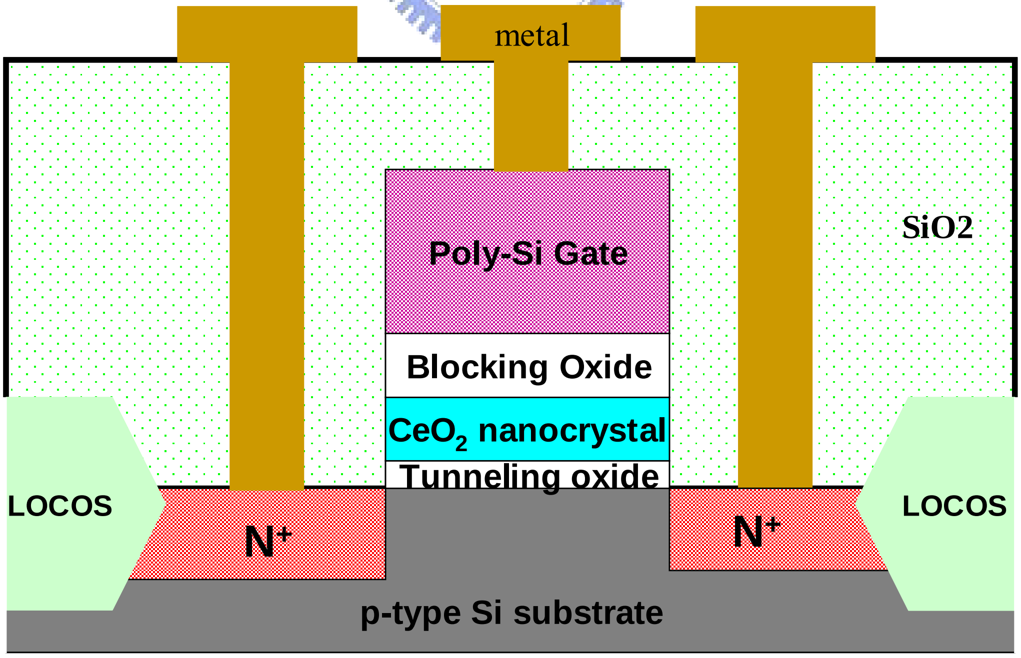
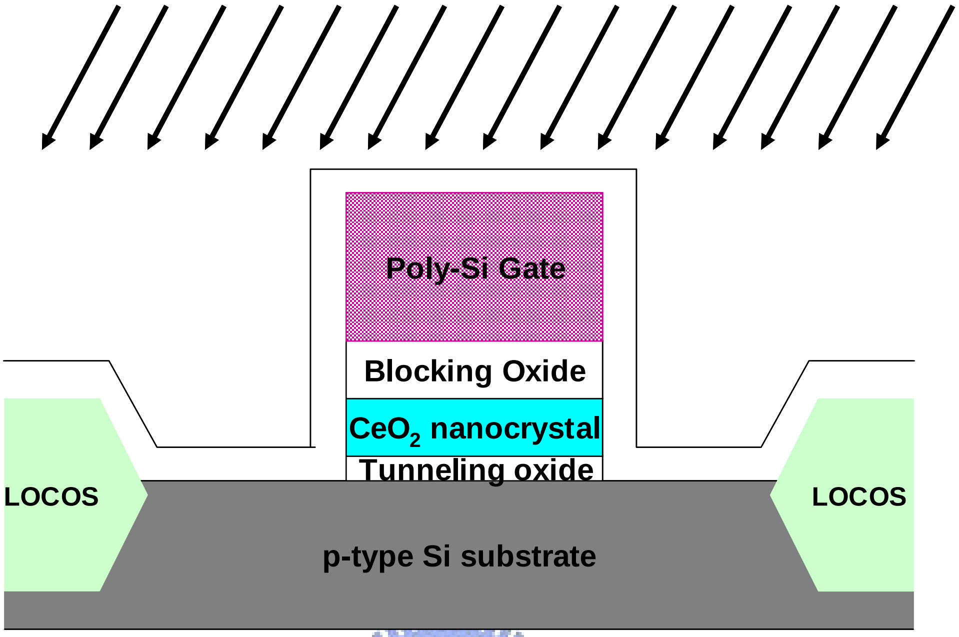

metal
SiO2
Poly-Si Gate
Blocking Oxide
CeO_2 nanocrystal
Tunneling oxide
LOCOS
N^+
N^+
LOCOS
p-type Si substrate

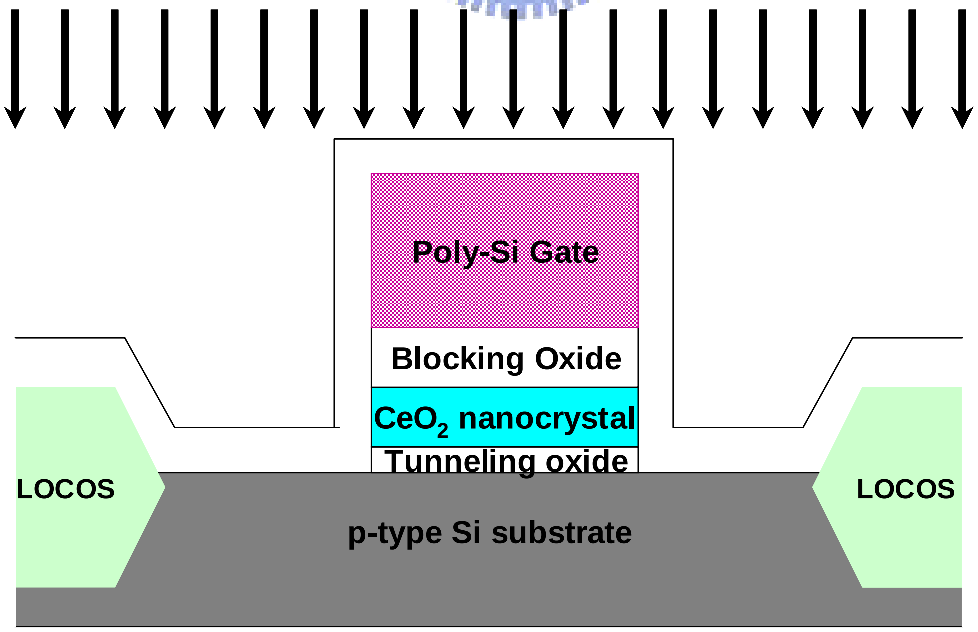
Fig. 4-1 The process flow of the flash memory and the cross-section of the flash memory (control samples).

The fabrication process of the CeO_2 nanocrystal memory devices involved was started with the LOCOS isolation process on p-type, 5-10 Ω cm, (100) 150mm silicon substrates. First, a 2 nm thick tunnel oxide was thermally grown at 1000^{O}C in vertical furnace system. The trapping layer of CeO_2 layer was deposited by dual E-gun method with CeO_2 target. After that, the samples went through RTA treatment in O_2 ambient at 900^{O}C for 1 minute. A blocking oxide of about 20 nm thick was then deposited by high density plasma chemical vapor deposition (HDPCVD). After that, the sample went through RTA treatment in O_2 ambient at 900^{O}C for 1 minute. Then, a 200 nm thick poly-silicon was deposited to serve as the gate electrode by LPCVD. Then, gate electrode was patterned and the source/drain and gate were doped by self-aligned P ion implantation at the dosage and energy of 5×10^{15} ions/cm^{-2} and 25 KeV, then the substrate contact was patterned and the sub-contact was implanted with BF_2 at the dosage and energy of 5×10^{15} ions/cm^{-2} and 40 KeV. After these implantations, the dopants were activated at 950^{O}C for 20 sec. The rest of the subsequent standard CMOS procedures were complete for fabricating the CeO_2 high-k memory devices. The above are control samples.

BF$_2$ ion implantation



P_{31}^{+} ion implantation



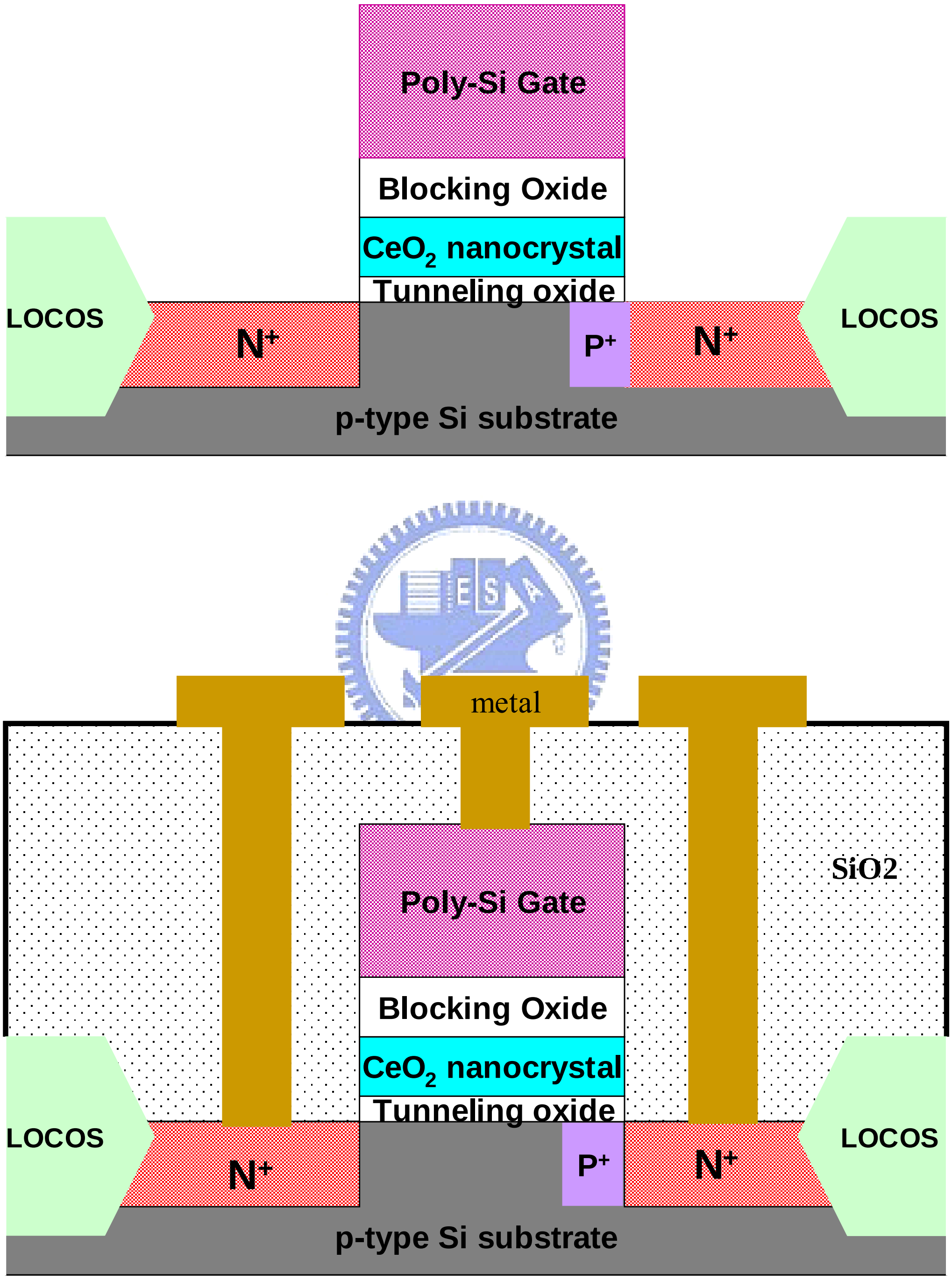


Fig. 4-2 The process flow and the cross-section of the asymmetry source/drain

flash memory (asymmetry S/D).

Figure 4-2 schematically depicts the process flow of the asymmetry source/drain SONOS flash memory. We changed the source/drain implantation with BF_2 ion implantation at the dosage and energy of 5×10^{13} ions/cm^{-2} and 25 KeV (twist angle: 72 degree, tilt angle: 30degree), then doped by P ion implantation at the dosage and energy of 5×10^{15} ions/cm^{-2} and 25 KeV (twist angle: 0 degree, tilt angle: 0 degree). Then the substrate contact was patterned and the sub-contact was implanted with BF_2 at the dosage and energy of 5×10^{15} ions/cm^{-2} and 40 KeV. After these implantations, the dopants were activated at 950^{O}C for 20 sec. The rest of the subsequent standard CMOS procedures were complete for fabricating the CeO_2 high-k memory devices.

4-3 Results and Discussion

In this section, the electrical characteristics of high-k CeO_2 nanocrystal SONOS-type memory were discussed.

4-3-1 Id-Vg Curve

Figure 4-3 shows the Id-Vg curves of the device under program and erase operations.

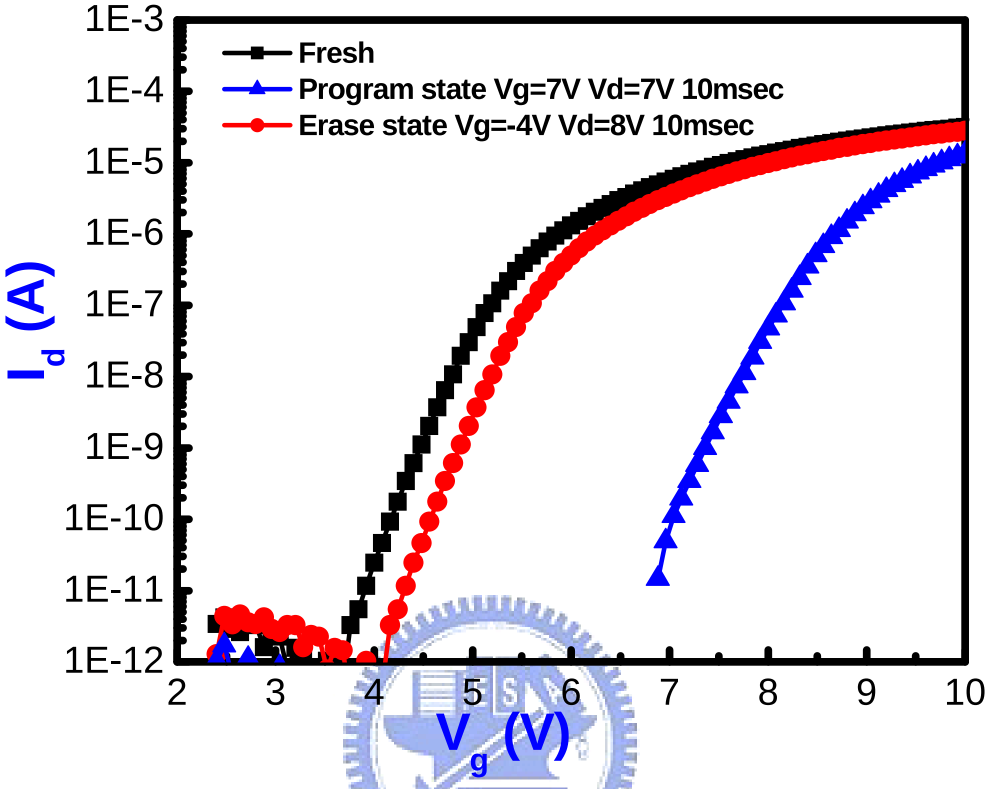


Fig. 4-3 The Id-Vg curves of the high-k CeO_2 nanocrystal SONOS-type flash memory in the programmed and erase state.

We use channel hot electron injection (CHEI) to program and band to band hot hole to erase (BTBHH). The program condition is Vg= 7V, Vd= 7V with 10 msec stress. The erase condition are Vg= -4V, Vd= 8V with 10 msec stress. The Vth after programming shifts about 3V from the original fresh state. After erasing, the Vth shifts leftward about 2.7V. So the memory window is about 3V. We think the Vth shift rightward is due to electron trapping in the high-k CeO_2 nanocrystal layer. The band offset is the reason why trapping occurred. During programming, the electrons in the substrate gain energy from the applied voltage Vg and Vd. If the energy is enough to cross the energy barrier, the hot electrons will inject to the high-k CeO_2 nanocrystal charge trapping layer and be trapped. This causes the Vth change. When erasing, we apply a negative gate voltage and positive drain voltage to generate hot hole in the substrate. If the hot hole in the substrate achieves enough energy to cross the energy barrier, it can reach the high-k CeO_2 nanocrystal charge trapping layer and cause the Id-Vg curve shift toward left.

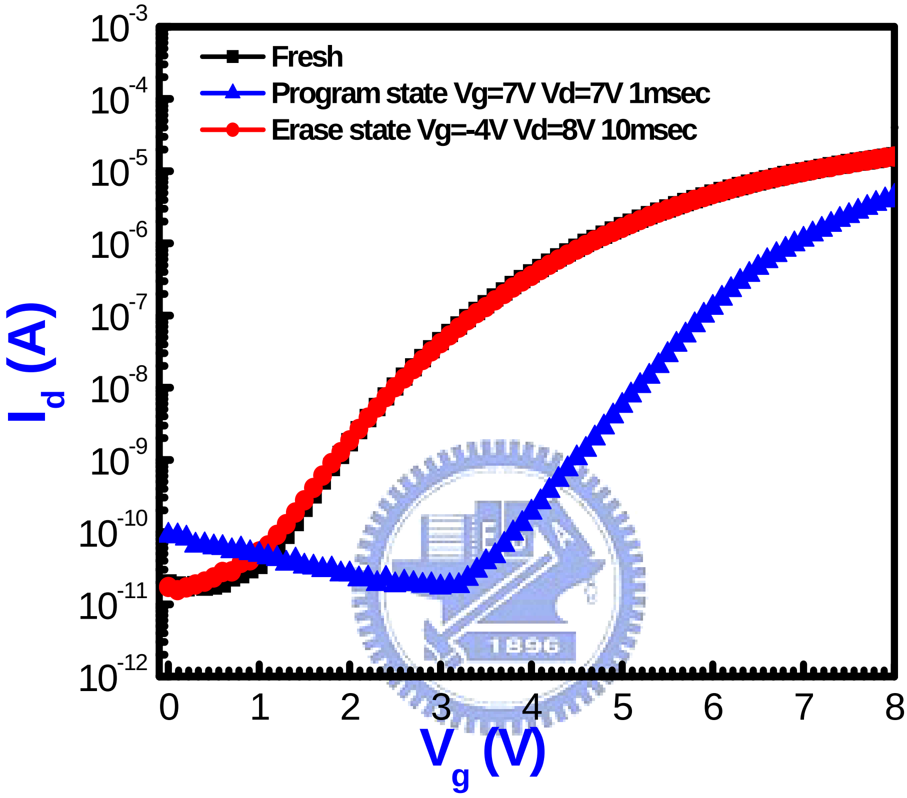


Fig. 4-4 The Id-Vg curves of the asymmetry source/drain high-k CeO_2 nanocrystal SONOS-type flash memory.

Figure 4-4 shows the Id-Vg curves of the device under program and erase operations. We use channel hot electron injection (CHEI) to program and band to band hot hole to erase (BTBHH). The program condition is Vg= 7V, Vd= 7V with 1 msec stress. The erase condition are Vg= -4V, Vd= 8V with 10 msec stress. The Vth after programming shifts about 2.3V from the original fresh state. After erasing, the Vth shifts leftward about 2.3V. So the memory window is about 2.3V.

4-3-2 Program and Erase Speed

For the control samples, the program speed is shown in Fig. 4-5.

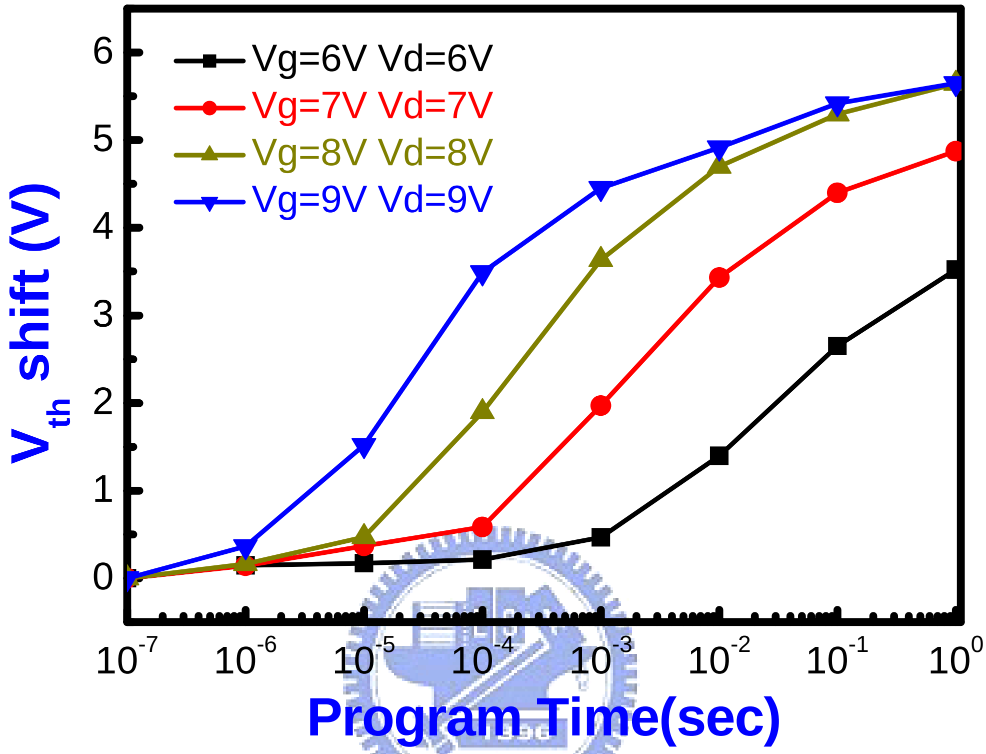


Fig. 4-5 The program speed curve of high-k CeO_2 nanocrystal SONOS-type flash memory.

We show four different stress conditions: Vg=6V,Vd=6V ; Vg=7V,Vd=7V; Vg=8V,Vd=8V ; Vg=9V,Vd=9V. As Fig. 4-5 shows, the condition Vg=7V, Vd=7V, 1 msec cause Vth shift 2V; and the condition Vg=8V, Vd=8V, 0.1 msec cause Vth shift 2V. With the Vg and Vd increasing, the Vth shift also increases and the program speed is faster; memory window is > 5V. This is because as the gate voltage become more positive for programming, more hot electrons are generated .So more and more hot electrons can be trapped in the charge trapping layer. Hence, the Vth shift increases as gate voltage and drain voltage increases.

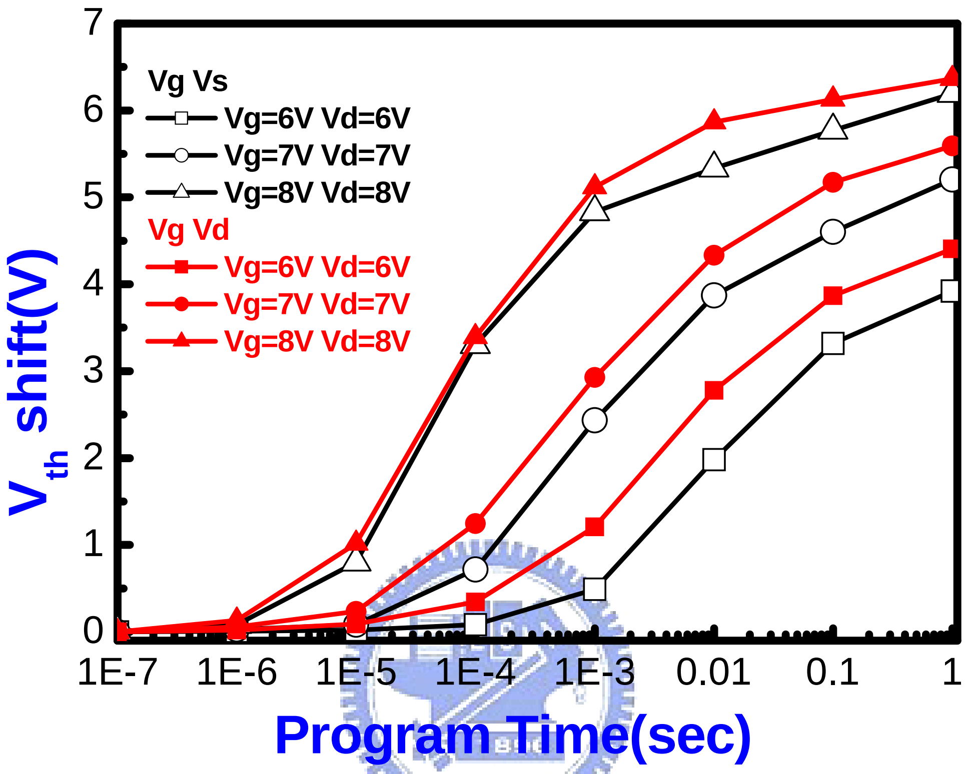


Fig. 4-6 The program speed curves of asymmetry source/drain high-k CeO_2 nanocrystal SONOS-type flash memory.

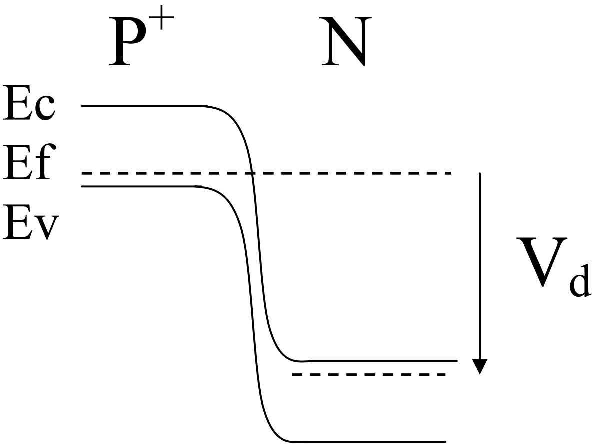


Fig. 4-7 The band diagram of P^+-N junction at reverse bias.

Figure 4-6 shows the program speed of the asymmetry source/drain device. First, define n-type only region as source; define n-type and p-type region as drain. We show three different stress conditions: Vg=6V,Vd=6V ; Vg=7V,Vd=7V; Vg=8V,Vd=8V ; compare with Vg=6V,Vs=6V ; Vg=7V,Vs=7V; Vg=8V,Vs=8V . As Fig. 4-5 shows, both the condition Vg=7V, Vd=7V and the condition Vg=7V, Vs=7V, 1 msec cause Vth shift > 2V. With the Vg and Vd,Vs increasing, the Vth shift also increases and the program speed is faster; memory window is > 6V. Hence, the Vth shift increases as gate voltage and drain voltage, source voltage increases. When the drain voltage applies to the drain region, the p^+-n junction is at reverse-biased condition, so band bending becomes more serious and then occurs zener breakdown, as depicted in Fig. 4-7. Therefore near drain region more and more electron hole pairs generate, so more and more hot electrons can be trapped in the charge trapping layer. In Fig. 4-8, we prove high drain current under the same drain and gate voltage the asymmetry source/drain device than the normal source/drain device. It means more and more electron hole pairs generate.

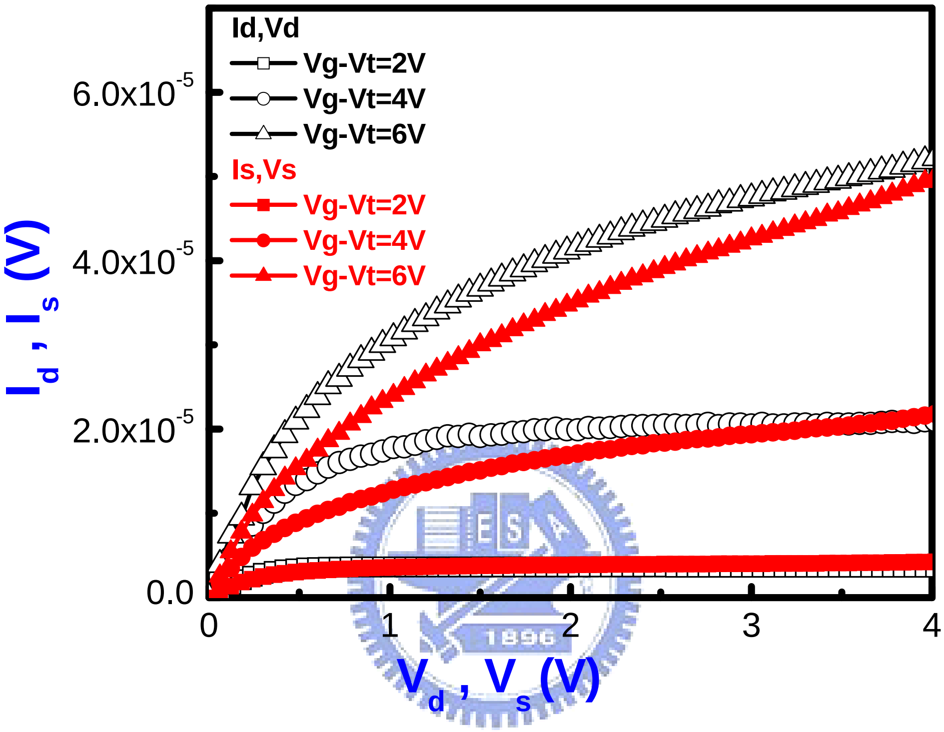


Fig. 4-8 The Id-Vd, Is-Vs curves of the asymmetry source/drain high-k CeO_2 nanocrystal SONOS-type flash memory.

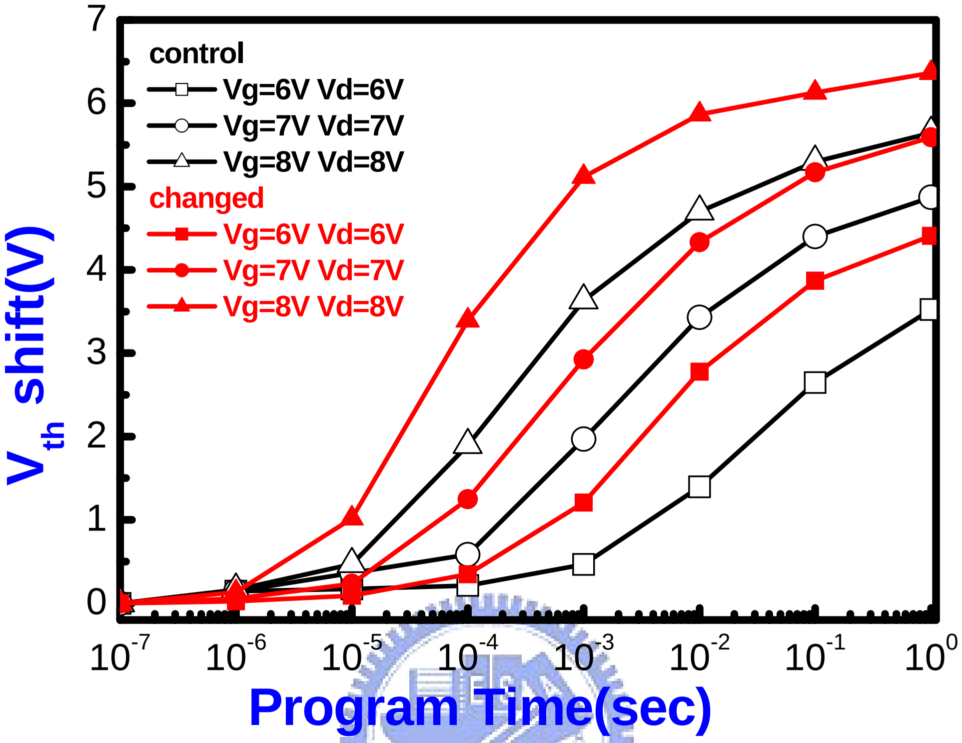


Fig. 4-9 The program speed curve of normal and asymmetry source/drain high-k CeO_2 nanocrystal SONOS-type flash memory.

Figure 4-9 shows the program speed of the control device and asymmetry source/drain device. We show three different stress conditions: Vg=6V,Vd=6V ; Vg=7V,Vd=7V; Vg=8V,Vd=8V . With the Vg and Vd,Vs increasing, the Vth shift also increases and the program speed is faster; memory window is > 6V. Hence, the Vth shift increases as gate voltage and drain voltage increases. Compared with control samples, the band bending of the p^+-n junction at reverse-biased condition is more serious and occurs zener breakdown. Therefore more electron hole pairs generate, more hot electrons can be trapped in the charge trapping layer. So the program speed of the asymmetry source/drain device is faster than control device. We prove this comment with Fig. 4-10.

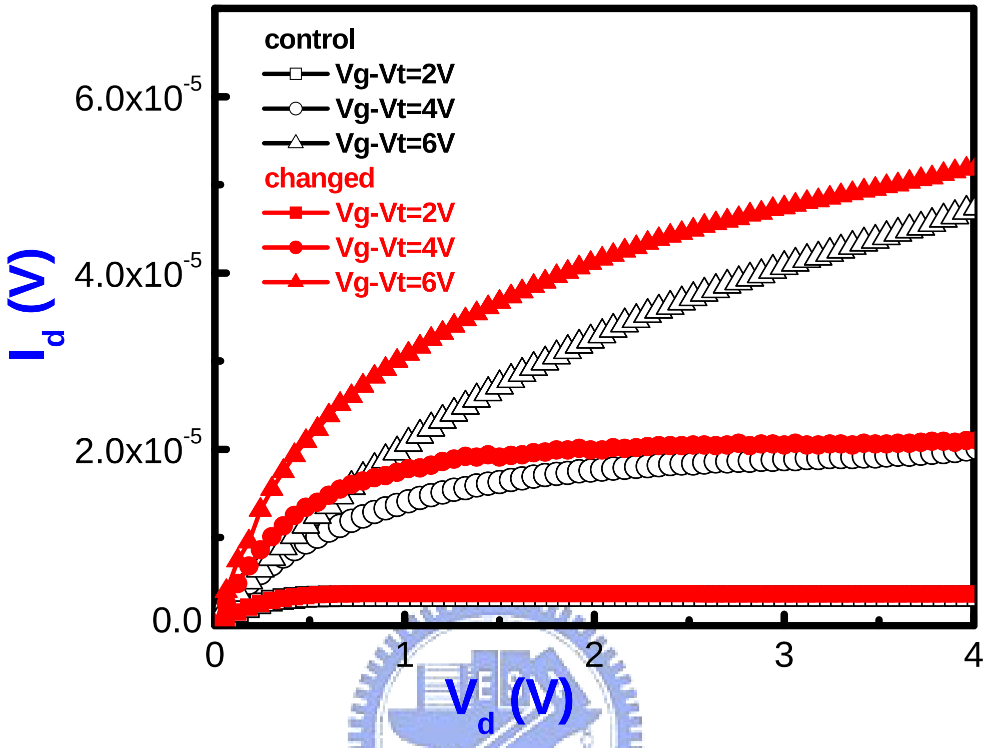


Fig. 4-10 The Id-Vd curves of normal and asymmetry source/drain high-k CeO_2 nanocrystal SONOS-type flash memory .

Figure 4-11 shows the normalized erase speed of the device. For Vg= -3V, -4V, and -5V with the same Vd=8V. We can see as the gate voltage becomes more negative, the Vth shift a little more; and all stress conditions the Vth shift > 2.5V in 10msec. For Vd= 6V, 7V, and 8V with the same Vg= -4V. We can see as the drain voltage becomes more positive, the Vth shift more. Hence, the Vth shift increases as gate voltage increases or drain voltage increases. Drain voltage influnces the erase speed is large than gate voltage.

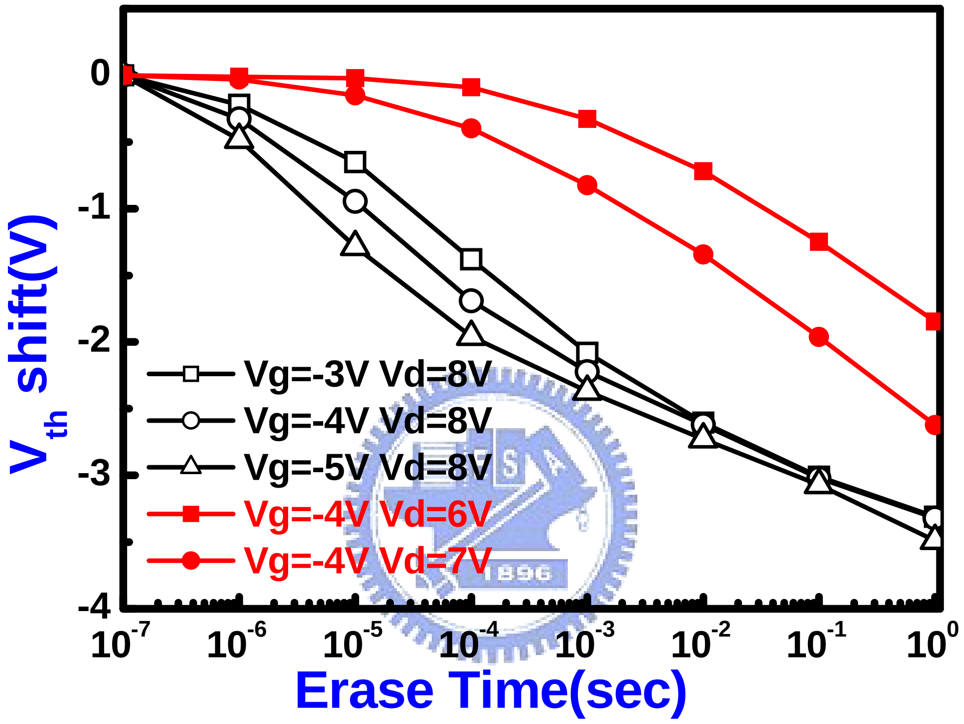


Fig. 4-11 The erase speed curve of high-k CeO_2 nanocrystal SONOS-type flash memory.

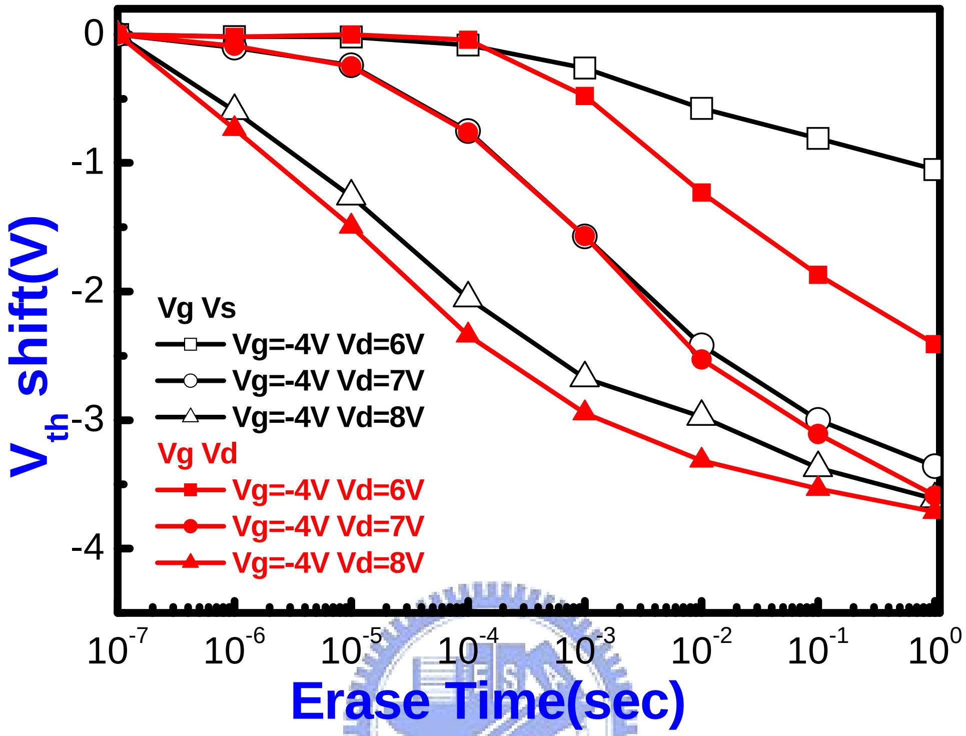


Fig. 4-12 The erase speed curve of asymmetry source/drain high-k CeO_2 nanocrystal SONOS-type flash memory.

Figure 4-12 shows the normalized erase speed of the asymmetry source/drain device. For Vd= 6V, 7V, and 8V with the same Vg= -4V. At low voltage (6V), the band bending of high-dose P^+-N junction at reversed bias is more serious than that of low-dose P-N junction at reversed bias .So more and more electron hole pairs generate near drain region than that near source region. The erase speed of condition Vg= -4V, Vd= 6V is more faster than condition Vg= -4V, Vs= 6V. At high voltage, the band bending of high-dose P^+-N junction and low-dose P-N junction at reversed bias are all serious. Therefore the erase speeds of them are almost the same.

Figure 4-13 shows the erase speed of the control device and asymmetry source/drain device. For Vd= 6V, 7V, and 8V with the same Vg= -4V. This is also because the band bending of high-dose P^+-N junction (asymmetry source/drain) at reversed bias is more serious than that of low-dose P-N junction (control samples) at reversed bias. Therefore the erase speed of the asymmetry source/drain device is faster than control samples.

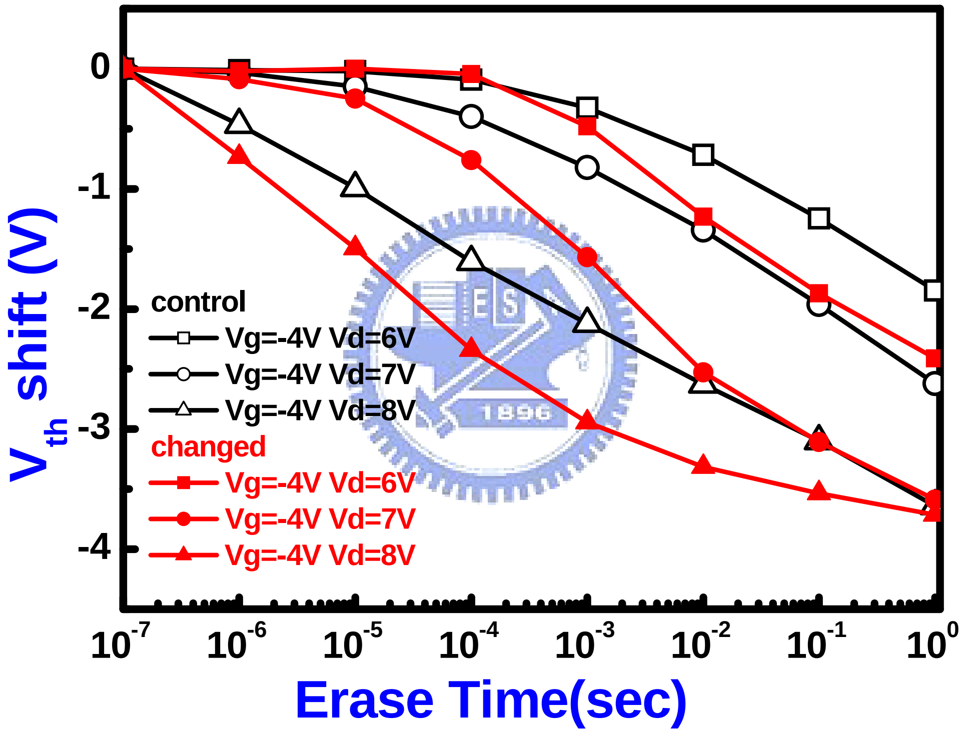


Fig. 4-13 The erase speed curves of normal and asymmetry source/drain high-k CeO_2 nanocrystal SONOS-type flash memory.

4-3-3 Data Retention Characteristic

Fig. 4-14 is the data retention characteristic of high-k CeO_2 nanocrystal SONOS memory measured at 25°C. We find the small charge loss with time .The curve shows only 8.5 % charge loss as measure time up to 10^4 sec and 16% charge loss up to 10^8 sec at 25°C. We infer the small charge loss at room temperature is from the electron deep trap of high-k CeO_2 nanocrystal charge trapping layer mentioned above.

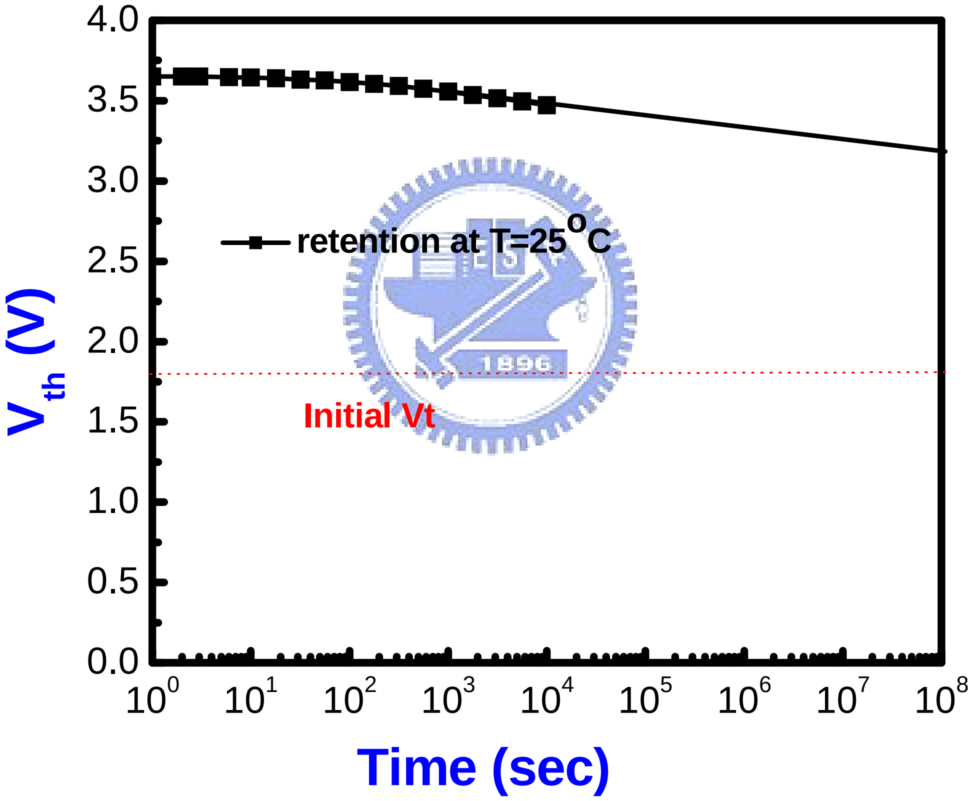


Fig. 4-14 Retention characteristic of the high-k CeO_2 nanocrystal SONOS-type flash memory at 25°C.

4-3-4 Disturbance Measurement

Figure 4-15 shows drain disturbance measurement of the normal and asymmetry source/drain high-k CeO_2 nanocrystal device. We applied two stress conditions: Vd =6V and Vd=8V with Vg=Vs=Vb=0V to the device. From the Fig. 4-12, we can see little Vth loss after 1000 sec stress for normal device, the programmed state Vth loss is 0.15V at Vd=6V and 0.23V for Vd=8V for the asymmetry source/drain device.

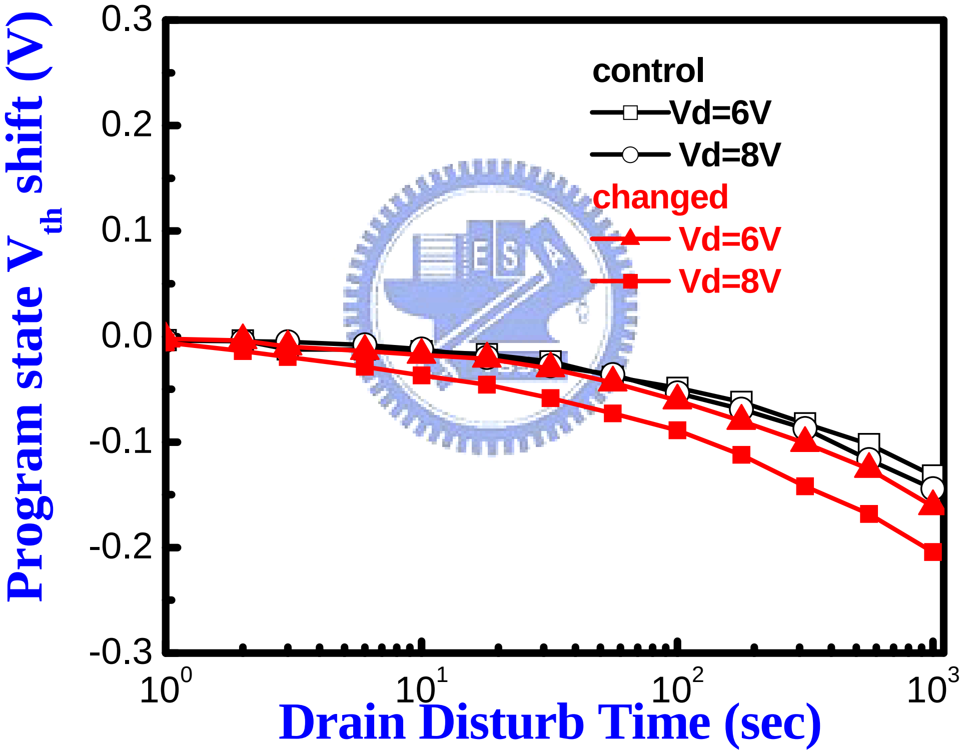


Fig. 4-15 Drain disturbance characteristics of normal and asymmetry source/drain high-k CeO_2 nanocrystal SONOS-type flash memory.

4-4 Summary

In this chapter, we propose a new source/drain implantation method for high-k CeO_2 nanocrystal SONOS memory. We have shown the electric curves, like Id-Vg, program/erase speed, charge retention, and drain disturbance. We demonstrate the quality of high-k CeO_2 nanocrystal with some good characteristics in terms of large memory window, long charge retention time due to deep trap level in the CeO_2 layer, and small drain disturbance.

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Chapter 5

Conclusions

The thesis of “The Study of High-K CeO_2 Nanocrystal Flash Memory with Different Metal Gates and S/D Implantations” was proposed. The results of each chapter are summarized as below.

In chapter 2, we discuss the dependence of metal gate work functions on the different annealing temperatures. We found a systematic methodology to extract the accurate work function of metal gates. We found the work function of TaN was about 4.6eV. It located at the midgap of energy level, so we choose a 700°C pre-annealing step to densify metal and then treatment at 900°C for 20 sec to fabricate NMOS. In the other hand, for MoN metal we choose a 600°C pre-annealing step to densify metal and then treatment at 900°C for 20 sec to fabricate NMOS.

In chapter 3, we replace conventional poly-Si gate with MoN and TaN metal gates. We have shown the electric curves, like Id-Vg, program speed, erase speed and disturbances. We improve erase efficiency of high-k CeO_2 nanocrystal memory with different metal gates by using n-channel devices .We also demonstrate the quality of high-k CeO_2 nanocrystal with some good characteristic in terms of large memory window, long charge retention time, and small gate disturbance and read disturbance.

In chapter 4, we propose a new source/drain implantation method to high-k CeO_2 nanocrystal SONOS memory. We have shown the electric curves, like Id-Vg, program/erase speed,charge retention, and drain disturbance .We demonstrate the quality of high-k CeO_2 nanocrystal with some good characteristics in terms of large memory window, long charge retention time due to deep trap level in the CeO_2 nanocrystal, and small drain disturbance.

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The Study of High-K CeO_2 Nanocrystal Flash Memory with Different Metal Gates and Source/Drain Implantations

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