國立交通大學

電子工程學系　電子研究所

碩 士 論 文

低溫複晶矽薄膜電晶體的電容模型及其頻率響應

Capacitance Model and its Frequency Response of Low-Temperature Polycrystalline Silicon Thin Film Transistors

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摘要

近年來低溫複晶矽薄膜電晶體已經引起大量的研究，其應用的方向是相當廣泛的。當低溫複晶矽薄膜電晶體應用為驅動電路時，將操作於閘極交流信號。因此低溫複晶矽薄膜電晶體對於元件在閘級交流信號下的頻率響應就具有相當大的重要性。

在本篇論文中，我們使用準分子雷射製作低溫複晶矽薄膜電晶體，利用電容-電壓量測和阻抗分析儀研究準分子雷射製作的複晶矽薄膜電晶體，其中，調變在不同準分子雷射能量密度下的複晶矽薄膜品質，我們觀察電容在不同的閘極偏壓下對頻率的變化，因此，從薄膜本身的特性，建立出以物理意義為根本的電容模型。

在電容-電壓量測下，我們針對空乏區研究其頻率響應，並且在高頻操作狀

態下觀察到量測的電容值急遽下降。因此，除了考慮到薄膜缺陷造成在不同頻率下的電容變化，也把從重摻雜的源極跟汲極端往通道中央提供的橫向流動的載子，所造成的特徵電容和特徵電阻引入；此處的特徵電容跟特徵電阻可由電導-頻率的峰值來計算。此外，利用兩個和缺陷相關的模擬參數，就能模擬出在空乏區中，各個閘極偏壓下的電容-頻率曲線；而其模擬結果與實驗數據都相當吻合。模擬結果也說明了在不同閘極偏壓下缺陷狀態的反應時間，以及橫向載子流動所形成的電阻。當閘極偏壓越靠近元件導通區時，缺陷狀態的反應時間越快，薄膜的特徵電阻越小。

Capacitance Model and its Frequency Response of Low-Temperature Polycrystalline Silicon Thin Film Transistors

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Abstract

In recent years, low temperature polycrystalline silicon thin-film transistors (TFTs) have been investigated extensively for their wide applications. The low temperature polycrystalline TFTs are operated under gate alternating current signal. Therefore, the studies of frequency response of low temperature polycrystalline TFTs under gate alternating signal become very important.

In this thesis, the low temperature polycrystalline silicon TFTs fabricated by the excimer laser annealing (ELA) are analyzed by the measurements of the capacitance-voltage (C-V) and impedance analyzer. Here, by adjusting different poly silicon crystalline film qualities due to different excimer laser energy densities, the variation of the measured capacitance under different gate biases is observed. Hence, according to the film properties, the physically-based capacitance model was

proposed.

Under the C-V measurement, we focus on the frequency response in the depletion region, and observe the measured capacitance decreases drastically under high frequency operation. Consequently, we not only study the capacitance variation under different frequency caused by the defects existing in the thin film, but also introduce the characteristics capacitance (C_{poly}) and the characteristics resistance (R_{poly}) due to the carrier lateral flow from the heavily doped source and drain to the channel; R_{poly} and C_{poly} can be extracted by the peak of conductance-frequency (G/f-f) curves. Besides, two fitting parameters related to the traps are used to model the C-V curves under each gate bias in the depletion region. Good agreements are found when comparing the modeling results and the experimental data.

The proposed capacitance model also illustrates the response time of the trap states and R_{poly} under different gate biases. As gate bias approaches the turn-on region, the response of the trap states becomes faster, and R_{poly} becomes smaller.

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邵而康

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Contents

Table Captions

Figure Captions

Chapter 1.

Chapter 2.

Chapter 3.

Chapter 1

Introduction

1.1 An overview of poly-Si TFTs technology

In recent years, polycrystalline silicon thin film transistors (poly-Si TFTs) have drawn much attention because of their widely applications on active matrix liquid crystal displays (AMLCDs) [1]-[3]. On the other hand, poly-Si TFTs have been applied to some memory devices such as dynamic random access memories (DRAMs) [4], static random access memories (SRAMs) [5], electrical programming read only memories (EPROM) [6], and electrical erasable programming read only memories (EEPROMs) [7]. Besides, linear image sensors [8], thermal printer heads [9], photodetector amplifier [10], scanner [11], neutral networks [11] have also adopted poly-Si TFTs technology. Within these, the application in AMLCDs is the most primary trend, which leads to a rapid development of poly-Si TFT technology.

Compared to amorphous silicon (a-Si) TFTs, the major attraction of applying poly-Si TFTs in AMLCDs lies in the greatly improved carrier mobility in poly-Si film which usually exceeds 100 cm^2 / Vs by present mature technology and the capability of integrating the pixel switching elements, panel array, and peripheral driving circuit on the same substrates [12]-[14]. Furthermore, because of the higher mobility of

poly-Si TFTs, the dimension of the poly-Si TFTs can be designed smaller than that of a-Si TFTs to achieve high density and high resolution AMLCDs.

In order to make high performance poly-Si TFTs, low-temperature technology is required for the commercial flat-panel displays (FPD) on inexpensive glass substrate, whereas the maximum process temperature is limited to less than 600 $^{\circ}C$[15]. There are three major low-temperature a-Si crystallization methods to achieve high performance poly-Si thin film: solid phase crystallization (SPC), excimer laser crystallization (ELC), and metal-induced lateral crystallization (MILC). The SPC method has the advantage of good uniformity and smooth interface, but the throughput is limited by the long crystallization time. In recent years, ELC has been used to crystallize the a-Si to poly-Si with lower temperature compared to SPC. In addition, the ELC method does not require a long time crystallization process, so it is suitable for mass production with high throughput. However, the roughness and uniformity of poly-Si film are important issues that may degrade the electrical characteristics if the laser energy is not accurately controlled.

1.2 RPI CV model of Poly-Si TFT

In RPI AC models, the grain boundary and intra-grain trap states in poly-Si result the gate to source/drain capacitance ($C_{G\text{-}SD}$) of a TFT in a function of measurement

frequency. Here, the source and drain terminals were shorted to ground, and a small signal is applied to the gate of the device. The frequency dispersion phenomenon can be comprehended by considering the transmission line model that is illustrated in Fig.1-2-1. A typical analysis of the effective circuit model forms complex impedance between the gate and source/drain terminals which depends on different frequencies. For single crystalline silicon transistors, the impedances are very small due to high mobility. Therefore the capacitance is almost independent of frequency. Besides, previous research also referred to later flow transmission line model [16]-[17], and introduced the influence of depletion capacitance (C_D). These statements indicated the variation of measured capacitances with different frequencies primarily arises from a frequency response associated with the later flow of carriers into and out of the channel from adjacent source and drain region.

However, the defects existed at the interface between gate oxide and poly-Si film, the grain boundary defects and the intra-grain defects are other factors to affect the device performance which are likely to respond to the small ac signal. Because of the response time of these defects, the measured capacitance is also a function of frequency in the depletion region. Therefore, the effect of trap capacitance (C_t) should be taken into account, where C_t is in parallel with C_D.

1.3 Motivation

Most of the previous studies have focused on the analysis of the defect density within the energy bandgap, the dependence of mobility on different biases, film qualities, environment temperatures, and the extraction of effective parasitic resistance by drain current-gate voltage (I_D-V_G) measurement. In addition, in recent years, the fabrication technology of poly-Si TFTs have been improved a lot. Due to high mobility and small dimension of device which could be fabricated on the glass substrate, these characteristics had attracted the industry to apply poly-Si TFTs to high frequency peripheral circuit.

Here, we would like to propose an effective circuit model which is based on physical mechanism and relates to the previous researches to extract some of the physical parameters such as C_D, C_t and R_t by C-V, C-f and G-f measurement. Thus, in this thesis, we focus on the defects and the characters of the poly-Si films which respond to small ac signal by C-V, C-f measurement.

1.4 Thesis Outline

This thesis is organized into the following manner.

In chapter 1, a brief overview of poly-Si TFTs for various kinds of applications is introduced, and several popular laser crystallization technologies are described. Then,

RPI CV model of Poly-Si TFTs and the other background studies are discussed briefly. Finally, the motivation of this work is expressed.

In chapter 2, detailed fabrication processes of ELA and SPC poly-Si TFTs are introduced, respectively. The measuring conditions are described concisely.

In chapter 3, the discussion is divided into three parts: First, the phenomena of the C-V and C-f curves are analyzed. Second, an equivalent circuit model is proposed to illustrate each effective capacitance and resistance. Moreover, the methods of the parameters extraction are explained. Finally, the fitting results of the proposed model are compared with the measured capacitance. Besides, the dependence of these parameters on gate bias is discussed.

In chapter 4, the conclusions are given including the physical mechanism of the proposed capacitance model and the explanation of the phenomenon of the frequency response.

Chapter 2

Experimental Procedures

2.1 The device fabrication process

In this experiment, typical top-gate, coplanar self-aligned poly-Si TFTs are fabricated by ELA method.

The schematic cross sectional view of these devices are shown in Fig.2-1-1, Fig.2-1-1(a) and Fig.2-1-1(b) are n-type with lightly doped drain (LDD) structure and p-type poly-Si TFTs, respectively; the fabrication process is described below.

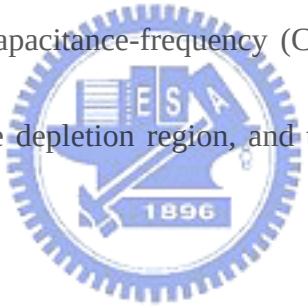
First, buffer layer was deposited on the glass substrate to prevent the diffusion of impurities existing in the glass substrate from the silicon layer. Then, undoped 50 *nm* thick amorphous-Si layer were deposited on buffer layer. After that, amorphous-Si films were recrystallized by ELA method under several different laser energies; here, the laser energy densities are 340 mJ/cm^2, 360 mJ/cm^2, and 380 mJ/cm^2, respectively. The recrystallized poly-Si films were patterned into the active islands with different dimensions. Afterward, the gate insulator was deposited; a 50 *nm*-thick oxide layer was deposited on the poly-Si film, and then a 20 *nm*-thick nitride layer was deposited on the oxide layer. Next, phosphorus ions and boron ions were implanted to form the n^+, n^-, and p^+ source/drain regions and these dopants were activated by thermal process. Finally, metal layer was deposited and then patterned for the source/drain and

gate regions as the metal pads.

In our experiment, we compared several C-V and C-f measurement results under three different ELA laser energies.

2.2 C-V and C-f measurement

In our experiment, HP4156 was applied to measure the current-gate voltage (I_D-V_G) in order to check the device performances. Besides, HP4284 was used to measure C-V under several frequencies which range from 10 *kHz* to 1 *MHz*. In addition, we also measured capacitance-frequency (C-f) by HP4194 in several gate voltages that are biased in the depletion region, and the measured frequencies were from1 *kHz* to 15 *MHz*.



Chapter 3

Results and Discussions

3.1 The observation of C-V and C-f curve

3.1.1 C-V curve analysis

As we could observe that the measured $C_{G\text{-}DS}$-V curves gradually increase from turn-off region, depletion region, to turn-on region in Fig.3-1-1(a), and the frequency dispersion phenomenon appears in the depletion region shown in Fig.3-1-1(b). The laser energy density of ELA poly-Si TFTs is 380 mJ/cm^2 which provides excellent device performance. Other measured C-V curves of different laser energy densities are also shown in Fig.3-1-2(a) and Fig.3-1-2(b), which are 360 mJ/cm^2 and 340 mJ/cm^2, respectively. The frequency dispersion phenomenon in the depletion region becomes more and more serious; it is because of the degradation of the poly silicon films under these laser conditions. Fig.3-1-3 is the images of Scanning Electron Microscope (SEM) which is capable of producing high-resolution images of poly silicon film surface. We find that the grains of poly silicon films in Fig.3-1-3(a) are more uniform and larger than that in Fig.3-1-3(b) and Fig.3-1-3(c). The trap response time listed in Table.1 is extracted while V_G bias is in the middle of the depletion region. The dependence of activation energy extracted from I_D-V_G measurement on

V_G is shown in Fig.3-1-4, where the dimension of these poly-Si TFTs are identical; W/L = 600μm /6μm. The activation energies of these three different device which the laser energy densities are 340 *mJ/cm*^{2}, 360 *mJ/cm*^{2}, *and* 380 *mJ/cm*^{2} are about the same; 0.65 *eV.* As device turn on, activation energies decrease to zero. Here, we could observe that when the laser energy density is 380 *mJ/cm*^{2}, the activation energy of the device decreases faster and more steeply than the other ones. In other words, the poly-Si film recrystallized in this condition which has larger and more uniform grains results in better film quality and fewer trap states for the carriers to fill compared to the other device recrystallized under 360 *mJ/cm*^{2} and 340 *mJ/cm*^{2}. Fig.3-1-5 shows the method of trap density extraction presented by modified Levinson theory [18]; the gentler the curve is, the fewer trap charges the film contains. Therefore, Levinson theory also identifies that when the laser energy density is 380 *mJ/cm*^{2}, poly-Si film has better quality than that recrystallized by the other two conditions. Fig.3-1-6 shows the C-f fitting curves based on our proposed capacitance model that will be mentioned later and the measured capacitance converted from C-V. Here, we suppose the phenomenon is mainly affected by the defects which are trapped in the bandgap trap states. Because of the response time of the carriers released from trap states to conduction are different in each gate bias; meanwhile, the frequency of ac signal is low enough for the carriers injected from source/drain to respond. Therefore, we

hardly observe the capacitance caused by the carriers that are capable of following the small ac signal from10 *kHz* to several hundred *kHz*. When frequency increases to 10 *MHz* as shown in Fig.3-1-7, which is ELA p-type poly-Si TFT with W/L=600μm /6μm. the measured capacitance reduces dramatically and achieves a specific saturation value in the turn-on region. It's because of the carriers provided from source/drain that are unable to penetrate into the whole intrinsic poly-Si channel which means the carriers only partially respond to the channel region near the source/drain region and beneath the gate oxide. Fig.3-1-8 shows the C-V curve of the device with channel length as 600 μm, the capacitance value degrades when the frequencies are from 100 *kHz* to 10 *MHz*. Comparing Fig.3-1-8 to Fig.3-1-7, the capacitance degradation phenomenon of the device with channel length as 600 μm biased in the turn-on region becomes severer due to the carriers provided from source/drain merely respond to an effective small areas which are adjacent to the source/drain region. Fig.3-1-9 shows C-V curve of n-type poly-Si TFT with W/L=600μm /6μm and LDD structure; the LDD length is 0.75 μm. The capacitance degradation phenomenon in the turn-on region is not as severe as p-type one, but still decreases obviously as frequency increases to 10 *MHz*. We attribute the variation between n-type and p-type device to the differences of the mobility between electrons and holes; the effective mass of electron is about four times lighter than that of hole, therefore, electrons are more

capable of following the small ac signal under high frequency operation than holes such as to penetrate into the middle of the channel region and respond.

3.1.2 C-f curve analysis

The measured C-f curves of ELA p-type poly-Si TFT which dimension is W/L=600μm /6μm are shown in Fig.3-1-10. Here, the gate biases are within the depletion region. All the measured capacitances under these gate biases decrease slightly from 1 *kHz* to 1 *MHz*, respectively; then decrease drastically as the frequency increases over 1 *MHz*. The frequency of ac signal is too high for the carriers to inject from the source/drain region to respond to the whole channel. In other words, the reduced capacitance value is observed because the carriers are gradually incapable of following the small ac signal over 1 *MHz.* For that reason, we consider when the frequency increases around to 15 *MHz*, there must be an additional effect to reduce the measured capacitance, and this effect has to be taken into account especially in high frequency condition.

The same phenomenon also occurs in the device with channel length as 600 μm shown in Fig.3-1-11, but the capacitance decreases drastically in lower frequency which ranges roughly from 10 *kHz* to 100 *kHz*. We can observe that as frequency increases above 1 *MHz*, this device does not work due to it can't sustain good

performance under high frequency operation. Fig.3-1-12 shows the C-f curve of n-type poly-Si TFT with W/L=600μm /6μm and LDD structure; the LDD length is 0.75 μm. Different from p-type poly-Si TFTs, the capacitance degradation phenomenon should be occurred above 15 *MHz* because we observe all the capacitance values biased in the depletion region keep decreasing but do not achieve small specific constants respectively. Therefore, the capacitance should be degraded as the frequency extends over 15 *MHz*, which corresponds to the supposition: electrons are more capable of following the small ac signal under high frequency operation than holes. In other words, n-type poly-Si TFTs are more promising in high frequency operation than p-type ones due to higher carrier mobility.

3.2 The proposed equivalent circuit model

3.2.1 The capacitance equivalent circuit model of the Poly-Si TFT

A capacitance equivalent circuit model is proposed shown in Fig.3-2-1. The equivalent circuit shown in Fig.3-2-1(a) is adaptable for short channel device; on the other hand, the equivalent circuit shown in Fig.3-2-1(b) is complete model which also can be applied for long channel poly-Si TFTs. In the effective device capacitor, a highly resistive intrinsic poly-Si channel capacitance and resistance have to be considered in the model. C_i represents the geometric capacitance of the insulator layer

which the area is the product of device width and length; R_{poly} and C_{poly} are the characteristics resistance and capacitance of the carrier lateral flow in the channel, respectively. C_D represents the capacitance of depletion. C_t and R_t are the capacitance and the resistance which result from the trap states in the depletion region and connect in parallel with C_D. C_{ct} and R_{ct} are the capacitance and the resistance which result from the trap states in the channel. Here, the trap states are caused by interface defects, grain boundary defects, and intra-grain defects. Besides, the specific response time constant of charge trapped in the trap state is the multiplication of R_t and C_t, and is a function of gate bias due to the relative position from trap state level to conduction.

In the turn-off region, C_t is also neglected because carriers can be supplied neither from the heavily doped source/drain regions nor from the intrinsic poly-Si bulk. Therefore, there is no frequency response under the strong reverse gate bias. In addition, C_{poly} is expected to be absent due to the intrinsic poly-Si bulk is fully depleted. Therefore, only a series combination of C_i and C_D is regarded as the capacitance equivalent circuit.

In the turn-on region, because a large number of carriers are injected from the heavily doped source/drain regions and accumulated at the interface, the amount of charges that are trapped at all these trap states can be neglected in comparison to the amount of injected carriers in the turn-on operating conditions. Therefore, the reason

why only C_i is observed as the frequency swept below several hundred *kHz* in C-V and C-f measurements is the carriers form a thin, highly concentrated layer which acts like a capacitor plate equal in area to the gate. However, in the high frequency region which is nearly over 1 *MHz*, a series combination of C_i and C_{poly} is expected to explain the decreasing measured capacitance due to resistance-capacitance (RC) time constant of poly-Si. In other words, the frequency is too high for the carriers to charge and discharge, hence, R_{poly} and C_{poly} are important parameters that should not be ignored under high frequency operating conditions.

In device depletion region, as we observed the C-f curve in Fig.3-1-5, C_{poly} and R_{poly} still affect the drastic degradation of measured capacitance in high frequency region, on the other hand, C_t and R_t should be considered in the equivalent circuit model especially when frequency ranges from 1 *kHz* to 1 *MHz* because the number of defect trapped charges is comparable to the number of mobile charges supplied by source/drain region in the intrinsic poly-Si channel. Hence, C_t and R_t that are in parallel with C_D can describe why the measured capacitance has a subtle decrease roughly below 1 *MHz*. Consequently, the effective capacitance of the equivalent circuit model is given by:

$$C(\omega) = \frac{C_1 C_2}{C_1 + C_2}\left[1 + \frac{C_1 / C_2}{1 + \omega^2 R_{poly}^2 (C_1 + C_2)^2}\right] \quad (1)$$

, where

$$C_1 = \frac{C_i C_P}{C_i + C_P} \tag{2}$$

$$C_2 = C_{poly} + \frac{C_{ct}}{1+\omega^2 R_{ct}^2 C_{ct}^2} \tag{3}$$

$$C_P = C_D + \frac{C_t}{1+\omega^2 R_t^{\,2} C_t^{\,2}} \tag{4}$$

The capacitance depends strongly on the change of frequency in the turn-on region and the depletion region; here, we focus on the discussion of the frequency response in the depletion region, and the equations shown above indicate that capacitance is a function of frequency under the depletion operating conditions related to carrier lateral flow and trap response time.

3.2.2 Methods of device parameter extraction

In our studies which focus on the analysis in the depletion region, main parameters are extracted from C-f and conductance-frequency (G/f-f) curves. In low frequency region, the value of measured capacitance at 1 *kHz* is the value of C_p in series with C_i. Here C_P is the summation of C_D and C_t affected by frequency. Therefore, R_t and C_t are the fitting parameters that we determine to describe the phenomenon of the slightly decreasing capacitance. In high frequency region, we regard the value of measured capacitance as C_{poly} at 15 *MHz*. Besides, according to

equation (1), C_1 calculated from the effective capacitance of C_i and C_P, is larger than C_{poly} at least by one order in the depletion region; hence C_{poly} can be neglected, and R_{poly} can be obtained by the peaks of the G/f-f curves shown in Fig.3-2-2 under different gate biases. Fig.3-2-2 shows the G/f-f curve of p-type poly-Si TFT with W/L=600μm /6μm biased under depletion region. In addition, the response time constant of the trap level is the product of R_t and C_t. Fig.3-2-3 shows the G/f-f curve of p-type poly-Si TFT with W/L=600μm /600μm, R_{poly} under each gate bias is still obtained by the peak of the curve. However, the curve in the device with channel length as 600 μm is asymmetric, which is considered an envelope formed by two curves, and caused by the trap states in the channel. Therefore, C_{ct} and R_{ct} are the fitting parameters that we determine to describe the phenomenon of the lingeringly decreasing capacitance. Besides, the response time constant of the channel trap level is the product of R_{ct} and C_{ct}.

3.3 The fitting results and the dependence of parameters on gate bias

Fig.3-3-1 shows the curves fitted by the equivalent model and the measured data of ELA p-type poly-Si TFT which dimension is W/L=600μm /6μm under each gate bias. We can see this model for short channel device is very similar to the measured value. The dependence of R_{poly} on gate bias is shown in Fig.3-3-2, as V_G is biased

from the depletion region to the turn-on region, R_{poly} decreases swiftly and almost reaches a specific constant value. The comparison of R_{poly} under two different lengths is shown in Fig.3-3-3, a prominent difference in the depletion region near the turn-off region can be observed. Furthermore, under the same gate bias, R_{poly} of longer channel length device is larger which means the carrier lateral flow response to the change of the channel length. The dependence of the trap response time which is the product of R_t and C_t on gate bias is shown in Fig.3-3-4. We can observe that the trap response time becomes faster as V_G is biased from the depletion region to the turn-on region. In other words, the trap charges are easier to release from the trap level to conduction. Fig.3-3-5 shows the curves fitted by the equivalent model and the measured data of ELA p-type poly-Si TFT which dimension is W/L=600μm /600μm under each gate bias. This model for long channel device is still similar to the measured value. However, some deviations occur in smaller gate biases, such as -2.5 *V*, -3 *V*. It is because the value of C_p defined at 1 *kHz* is not correct; the accurate C_p should be calculated less than 1 *kHz* as the capacitances reach individually stable values. Thus, lower measured frequency and less noise are required. Fig.3-3-6 shows the channel trap response time, similarly, τ_{ct} is the product of R_t and C_t on gate bias. We can observe that channel trap response time becomes faster as V_G is biased from the depletion region to the turn-on region which corresponds to the tendency of τ_t.

Chapter 4

Conclusion

In this thesis, we studied capacitance model and its frequency response of poly-Si TFTs. We introduced a physically-based equivalent circuit to illustrate the dependence of capacitance on frequency and gate bias. Here, we focused on the depletion region due to the drastic frequency response. For device with channel length as 6 μm, the slight decrease in measured capacitance under low frequency condition which ranges from 1 *kHz* to about 1 *MHz* results from the defects existing in the poly-Si film. As frequency increases over 1 *MHz*, the ac signal is too high for the carriers to inject from the source/drain region to respond in the whole channel. Therefore, the reduced capacitance can attribute to the influence of the characteristics resistance (R_{poly}) and capacitance (C_{poly}) of the carrier lateral flow in the channel area which are considered connecting in series with an effective capacitance; the effective capacitance is combined by the insulator capacitance and depletion capacitance in series connection. The fitting curves calculated using the proposed model explained the measured capacitance very well.

As a result of the dependence of carrier lateral flow on frequency, R_{poly} extracted from G/f-f is an effective parameter to explain the degradation of capacitance under

high frequency operation.

As the device dimensions scaled down, the influence of the characteristics resistance and capacitance of the carrier lateral flow in the channel area is not obvious but still can not be neglected, especially under high frequency operating conditions. On the contrary, R_{poly} is affected by the long channel length because the carriers can not totally respond to the whole channel area under high frequency operation; thus, R_{poly} has much larger variation compared to the shorter channel one. We can observe that τ_t becomes faster as V_G is biased from the depletion region to the turn-on region. In other words, these trap charges are easier to release from the trap level to conduction.

In conclusion, the effects of defects, device dimension, gate bias and frequency are considered in the proposed capacitance model. With the proposed equivalent circuit, we can develop physically-based C-V model for LTPS TFTs to replace current empirical C-V model in SPICE tool.

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Table.1

mJ/cm^2	340	360	380
V_G (V)	-2.0	1.5	-1.7
τ_t (s)	5.31E-06	2.92E-06	1.23E-06

The response time of ELA p-type poly-Si TFTs fabricated under different excimer laser energy densities. W/L=600μm /6μm.

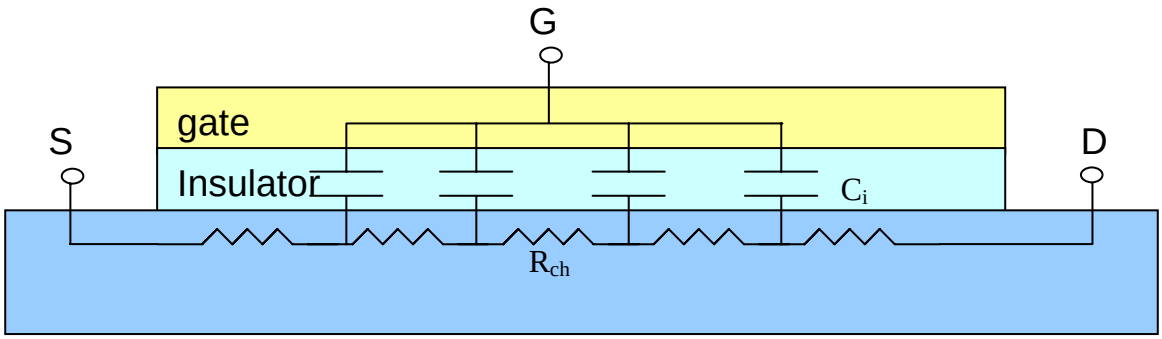


Fig.1-2-1 Transmission line model proposed by RPI.

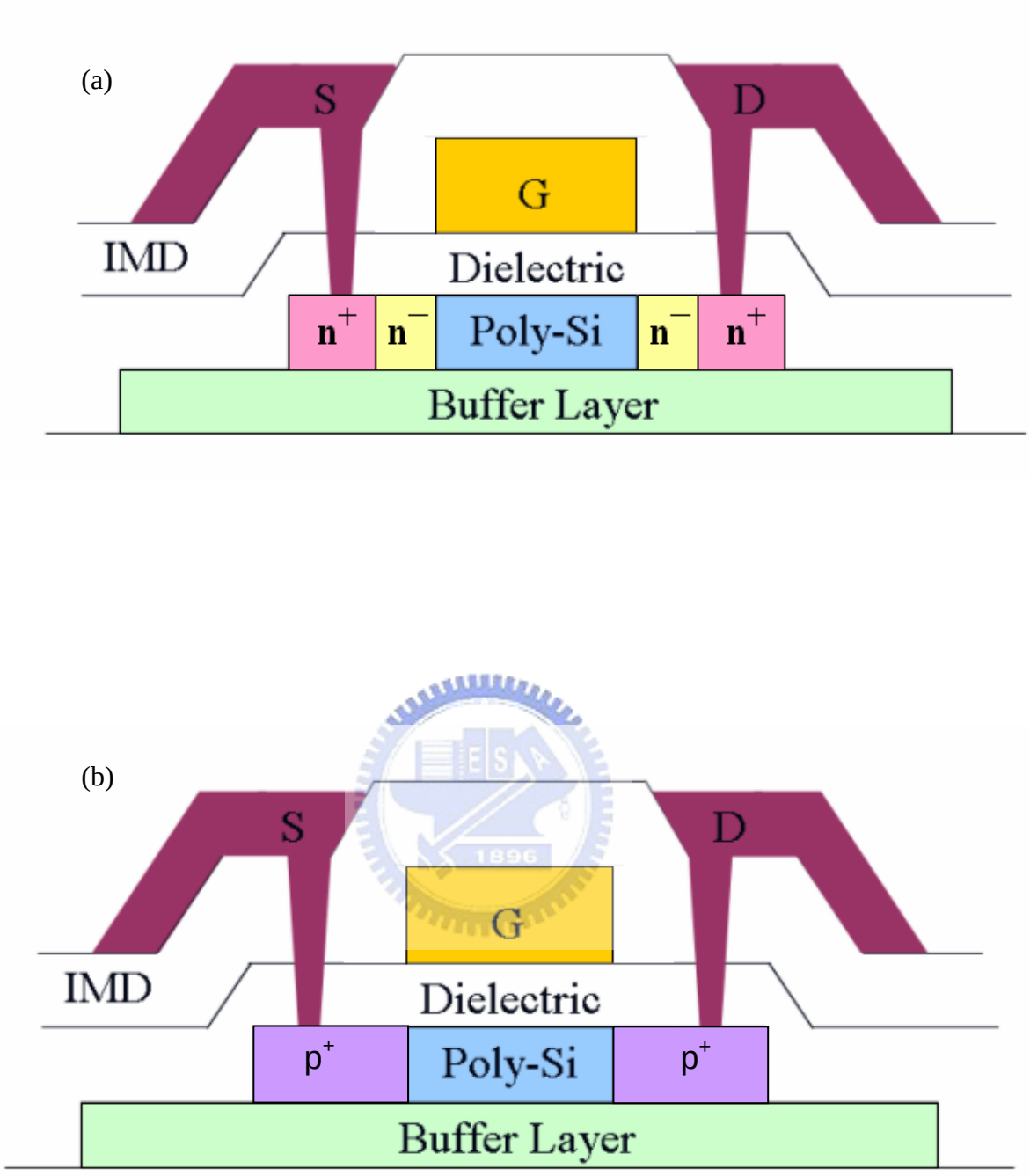


Fig.2-1-1 The schematic cross sectional view of Poly-Si TFT.(a) is n-type ELA poly-Si TFT, (b) is p-type ELA poly-Si TFT.

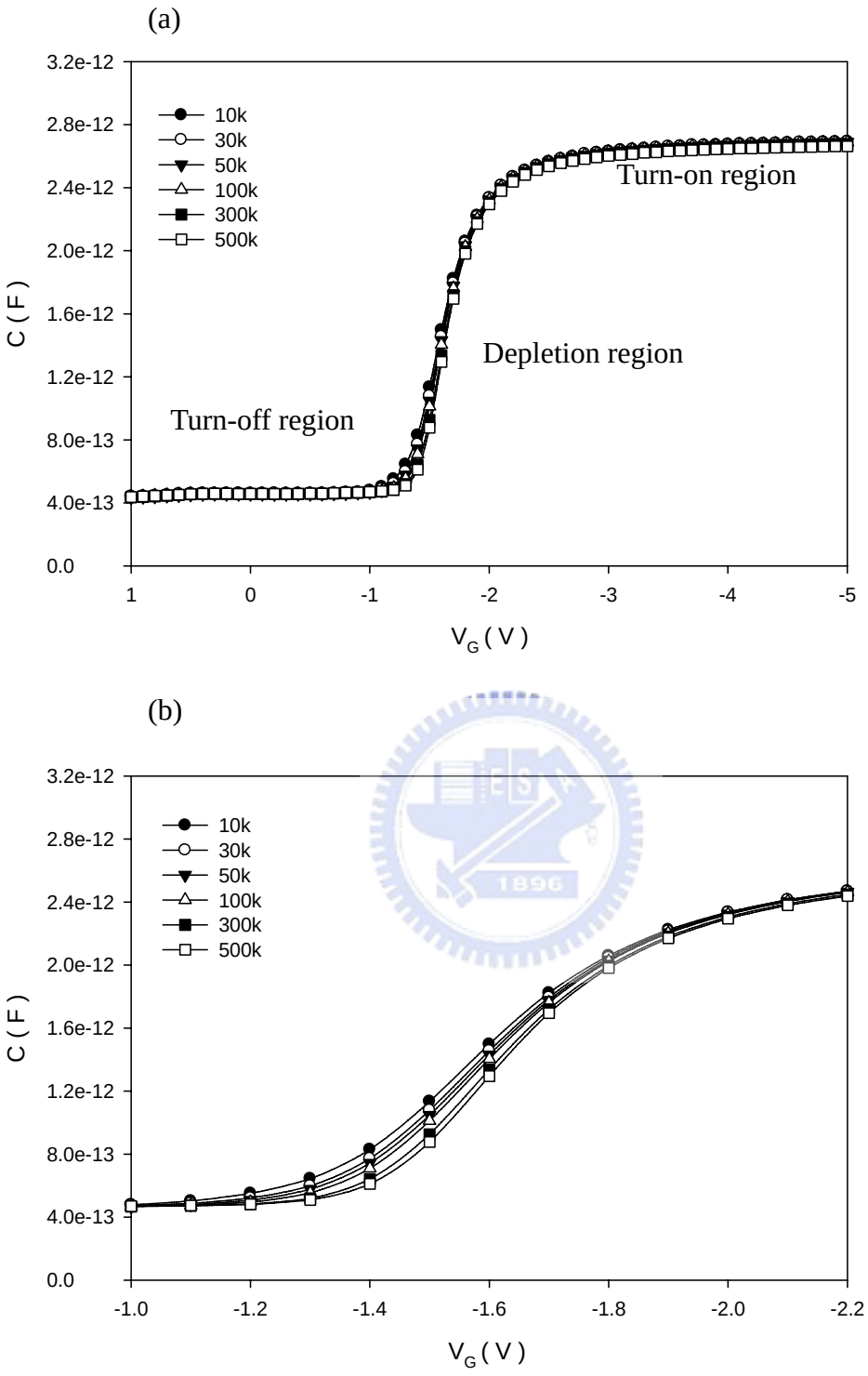


Fig.3-1-1 (a) C-V curves of ELA p-type poly-Si TFT. W/L=600μm /6μm. Frequency is from 10k to 500 *kHz*. ELA laser energy is 380 mJ/cm^2. (b) V_G is from -1*V* to -2.2*V*.

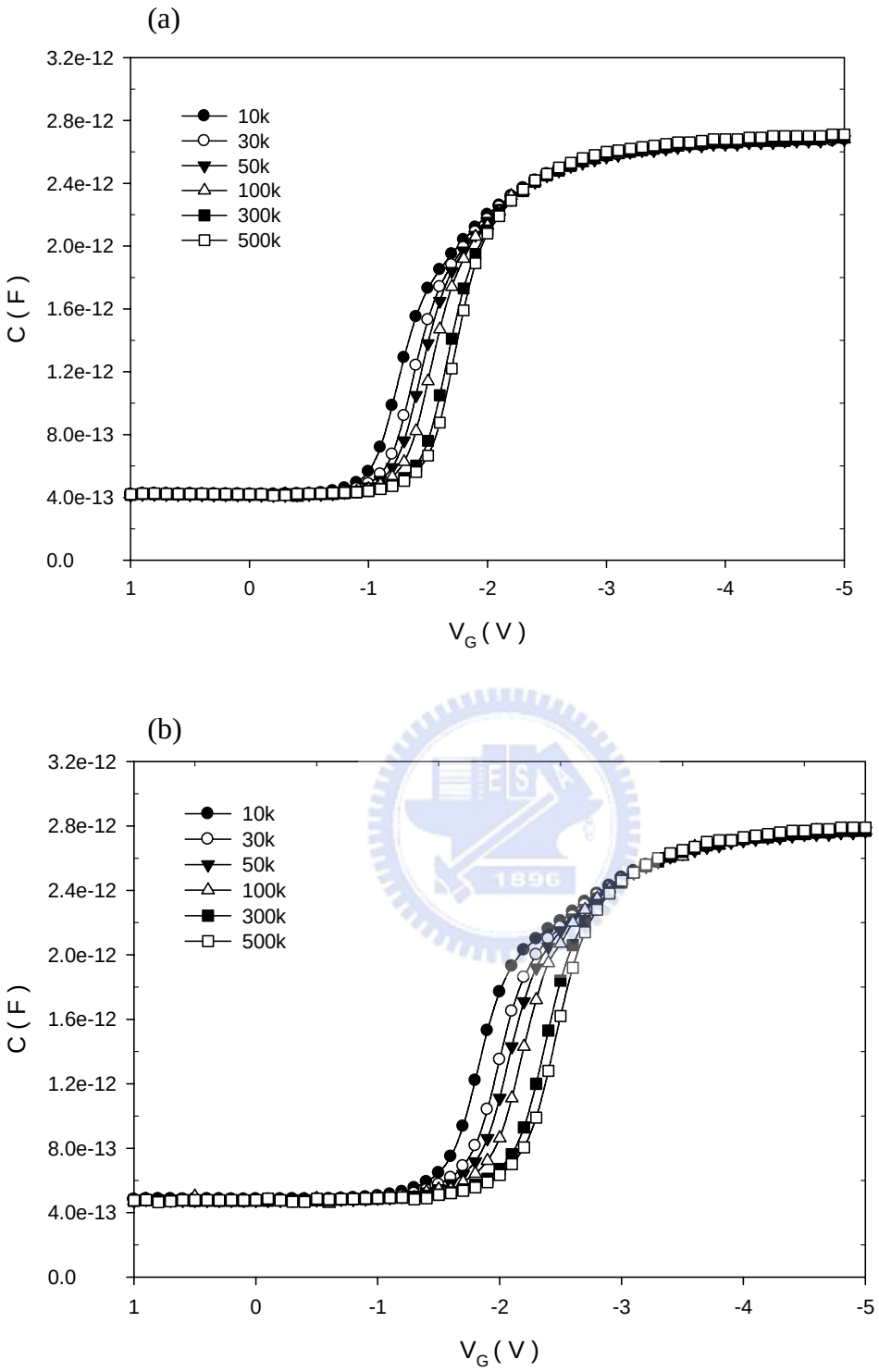
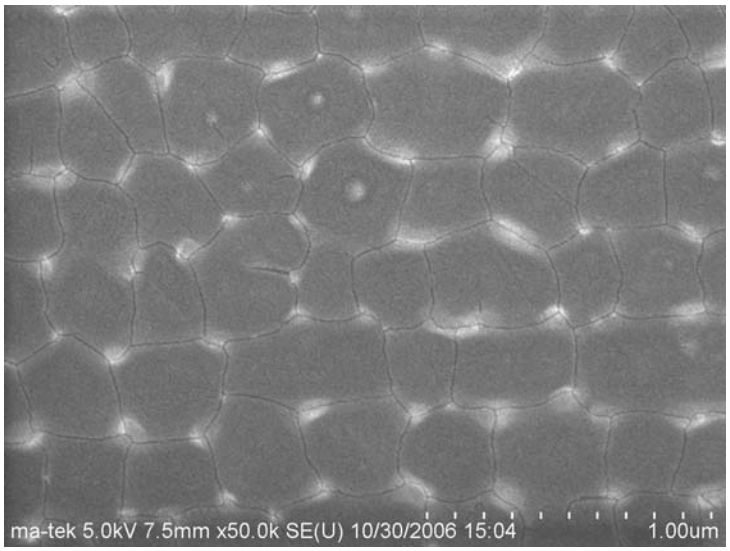
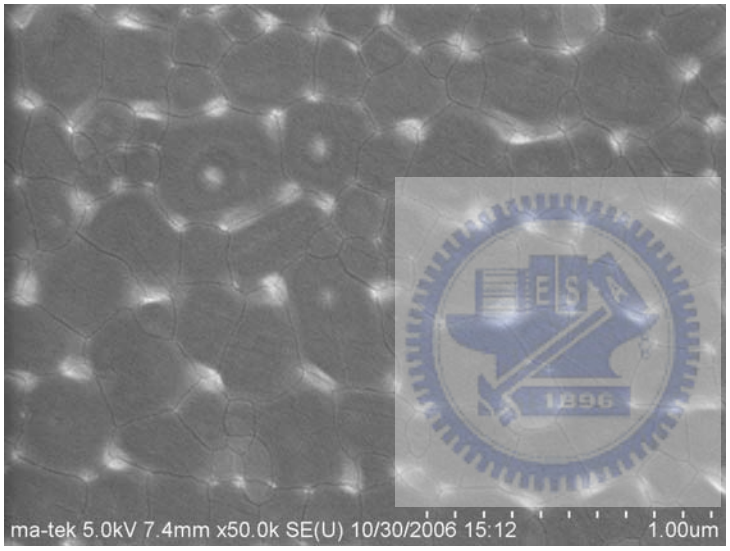


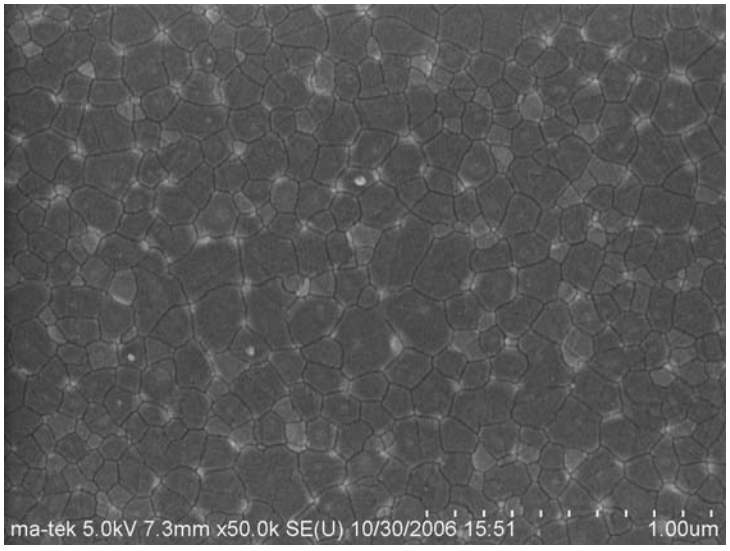
Fig.3-1-2 C-V curves of ELA p-type poly-Si TFT. W/L=600μm /6μm. Frequency is from 10k to 500 *kHz*. ELA laser energy of (a) is 360 mJ/cm^2, of (b) is 340 mJ/cm^2.



(a)



(b)



(c)

Fig.3-1-3 SEM images of poly silicon film. ELA laser energy of (a) is 380 mJ/cm^2, (b) is 360 mJ/cm^2, (c) is 340 mJ/cm^2.

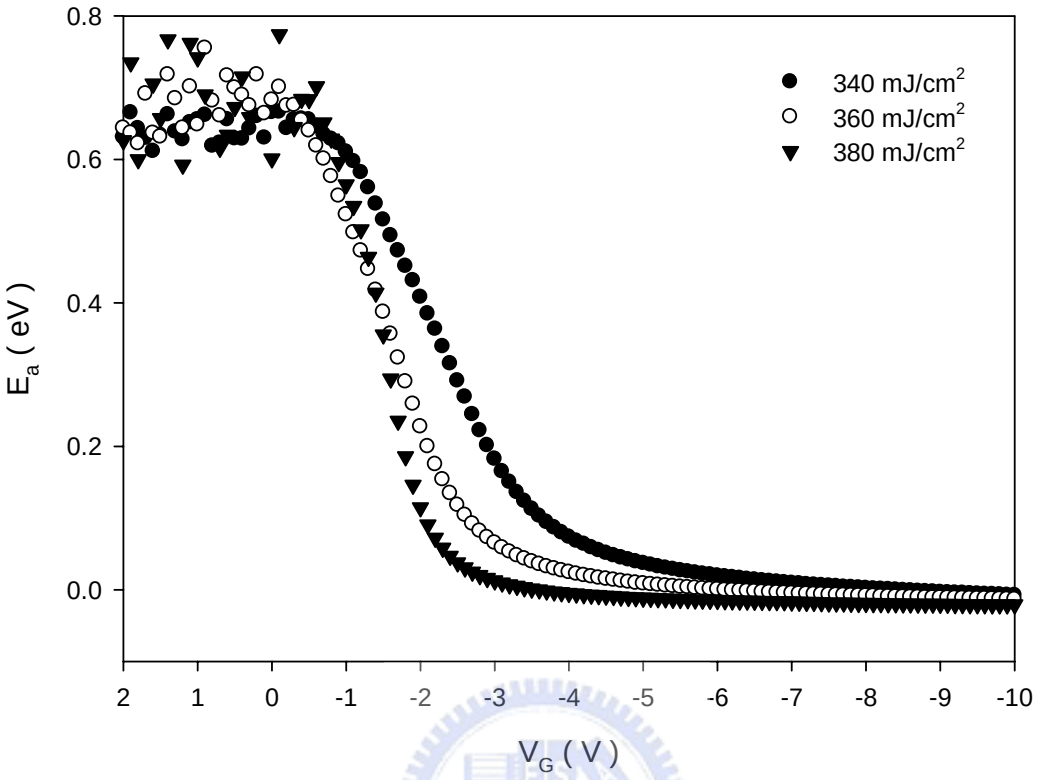


Fig.3-1-4 The dependence of activation energy on gate voltage under three laser energy densities. These are ELA p-type poly-Si TFTs. W/L=600μm /6μm.

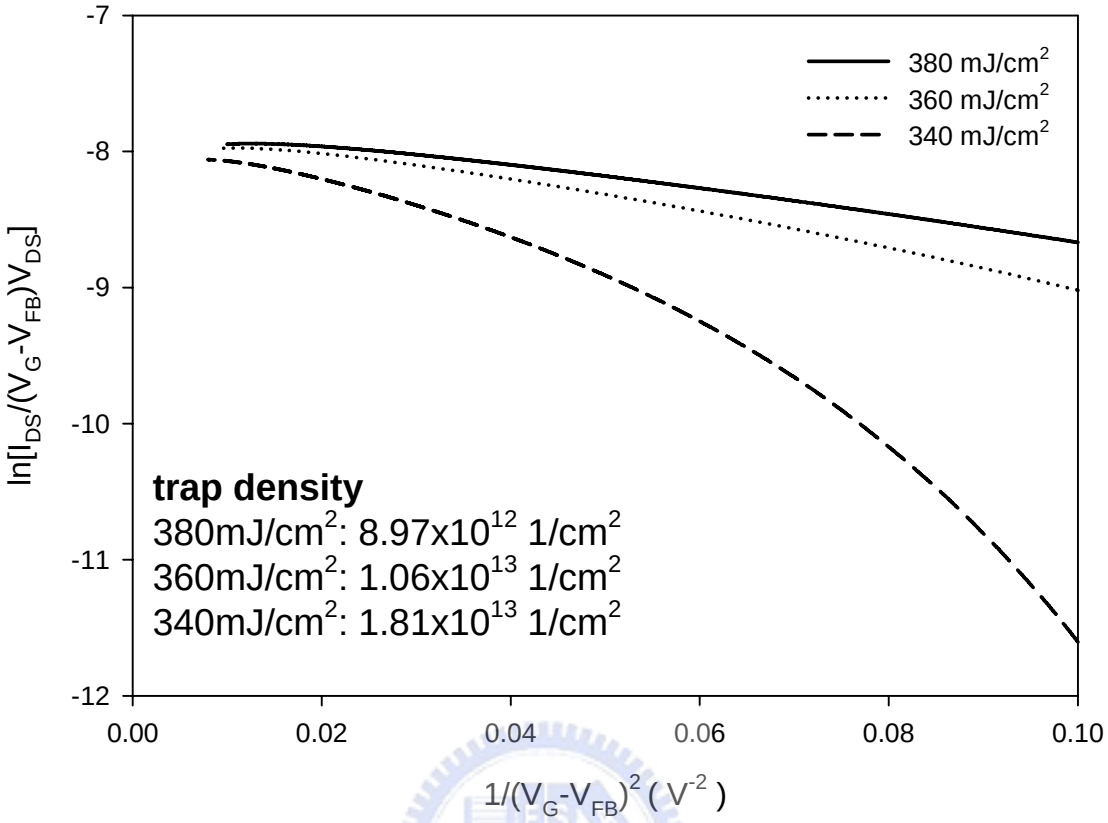


Fig.3-1-5 Trap density extraction by modified Levinson theory under three laser energy densities. These are ELA p-type poly-Si TFTs. W/L=600μm /6μm.

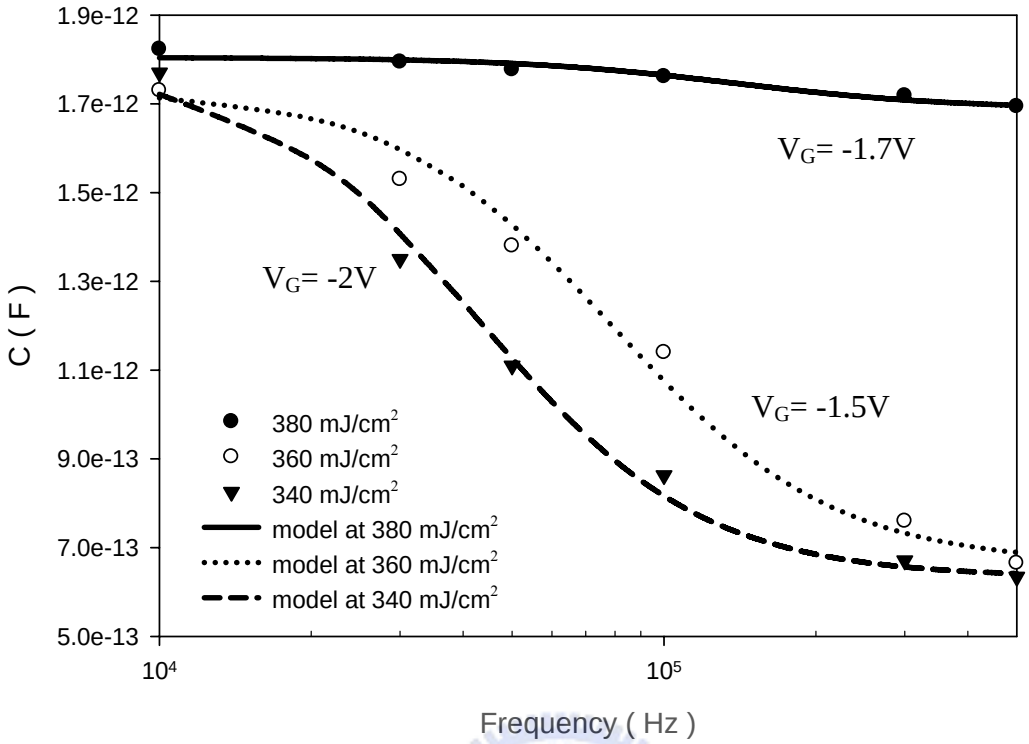


Fig.3-1-6 C-f curves of ELA p-type poly-Si TFT. W/L=600μm /6μm. ELA laser energy is 380 *mJ/cm*^{2}, 360 *mJ/cm*^{2}, and 340 *mJ/cm*^{2}.

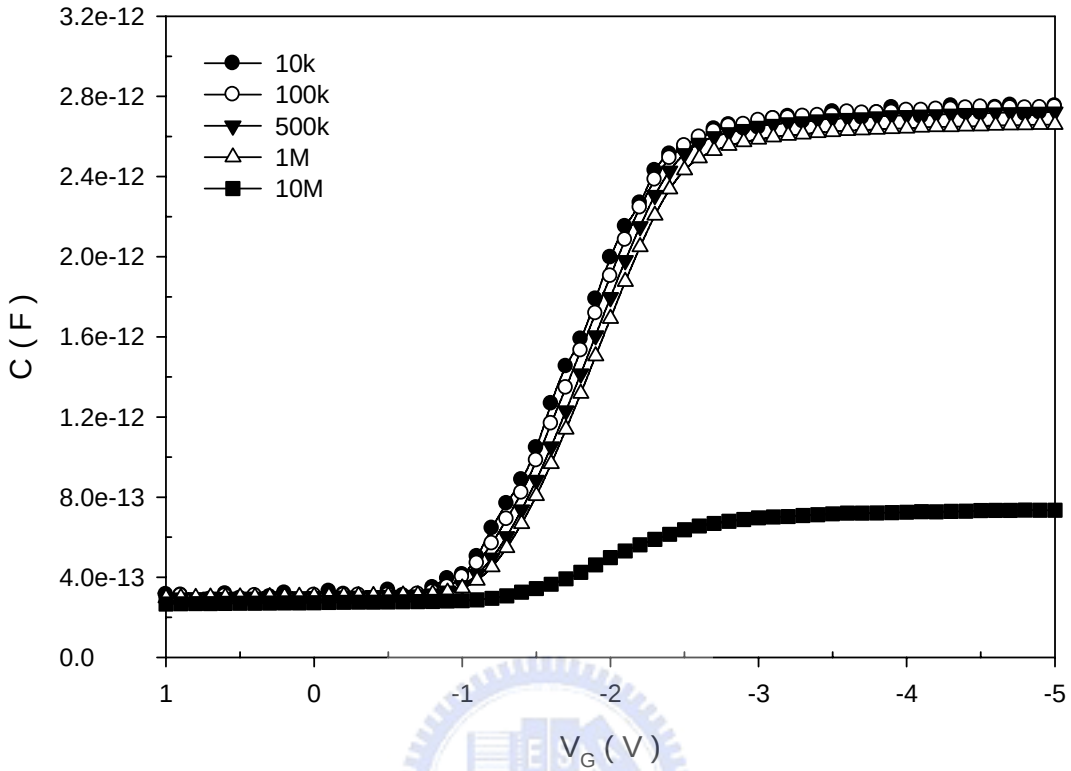


Fig.3-1-7 C-V curves of ELA p-type poly-Si TFT. W/L=600μm /6μm. Frequency is from 10k to 10 *MHz*. ELA laser energy is 380 mJ/cm^2.

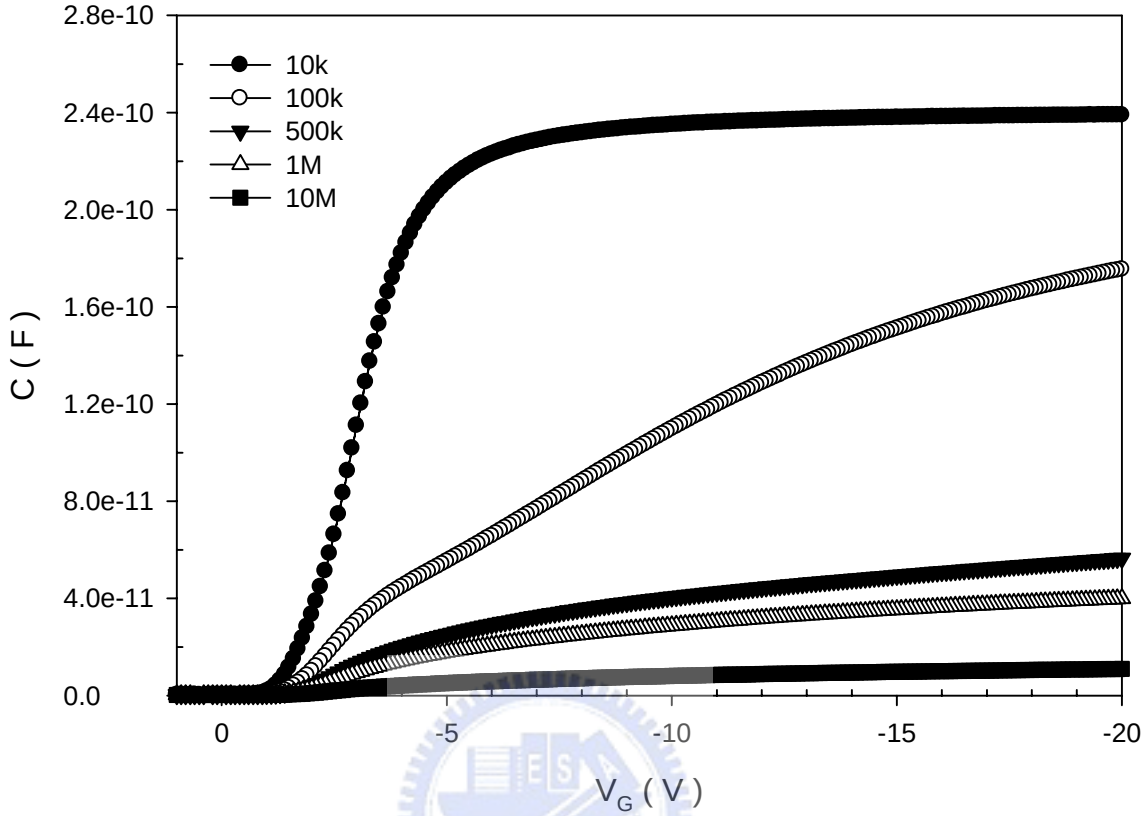


Fig.3-1-8 C-V curves of ELA p-type poly-Si TFT. W/L=600μm /600μm. Frequency is from 10k to 10 *MHz*. ELA laser energy is 380 mJ/cm^2.

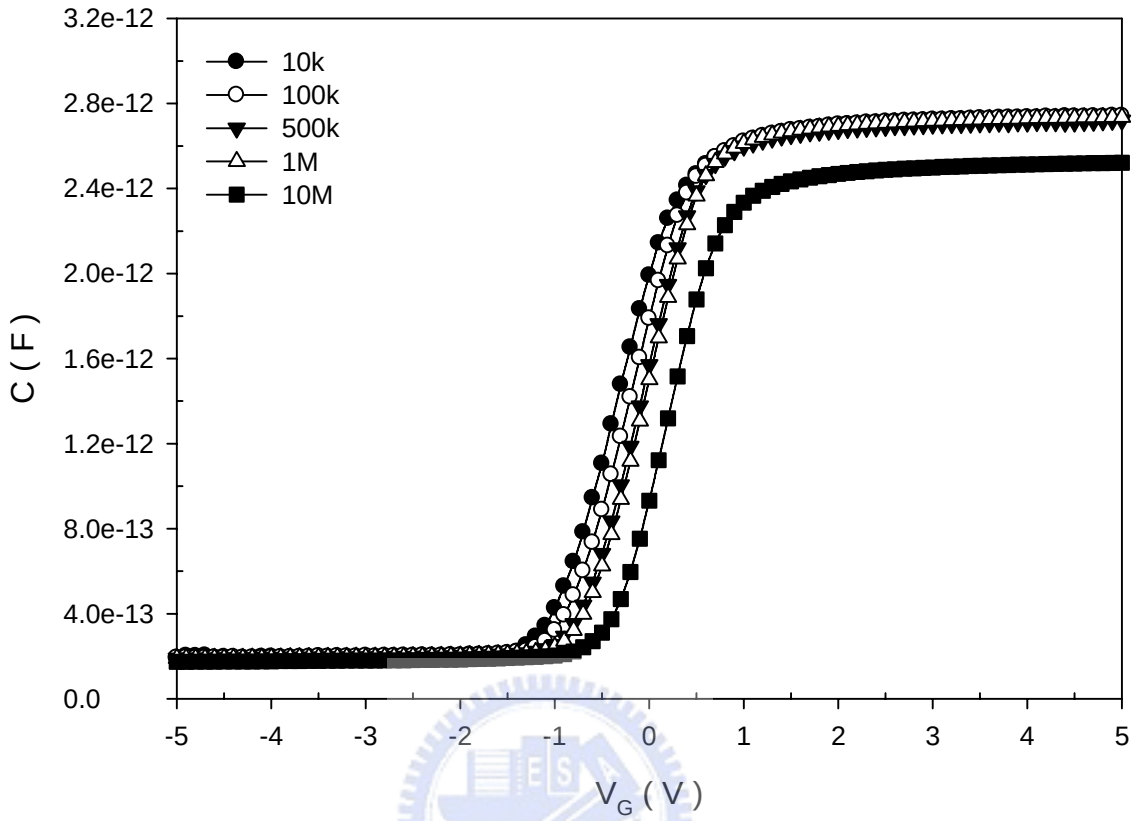


Fig.3-1-9 C-V curves of ELA n-type poly-Si TFT. W/L=600μm /6μm. LDD=0.75 μm. Frequency is from 10k to 10 *MHz*. ELA laser energy is 380 mJ/cm^2.

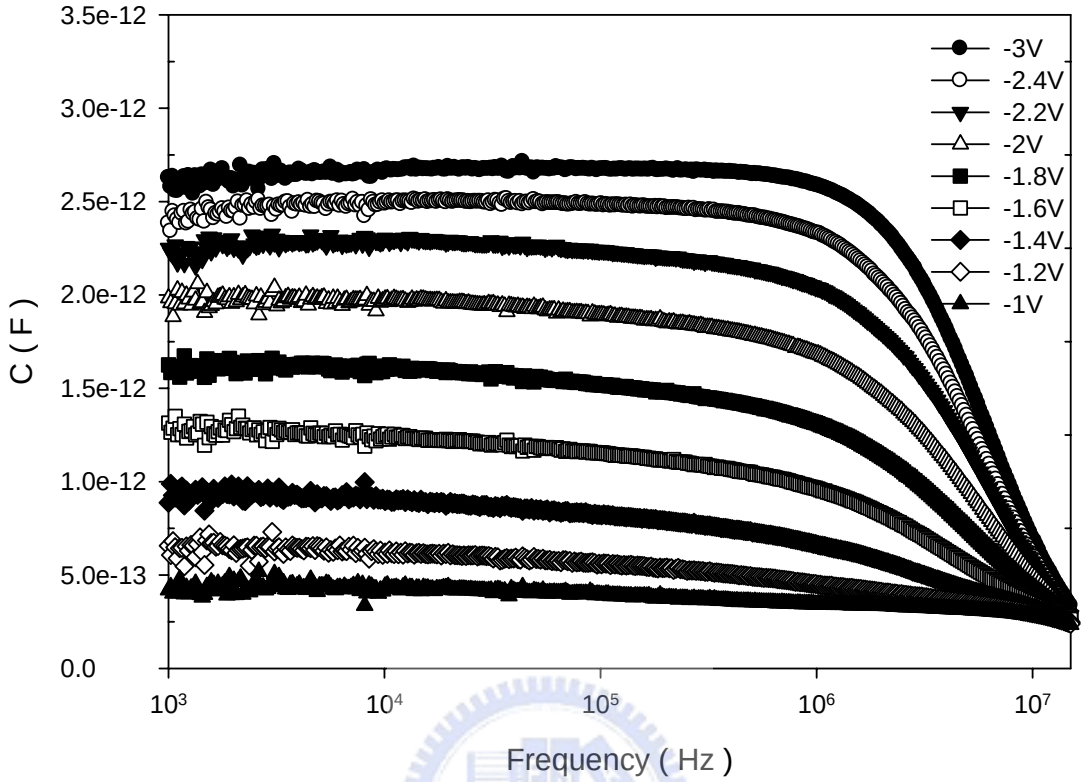


Fig.3-1-10 C-f curves of ELA p-type poly-Si TFT. W/L=600μm /6μm. V_G is biased from -1 *V* to -3 *V*. ELA laser energy is 380 mJ/cm^2.

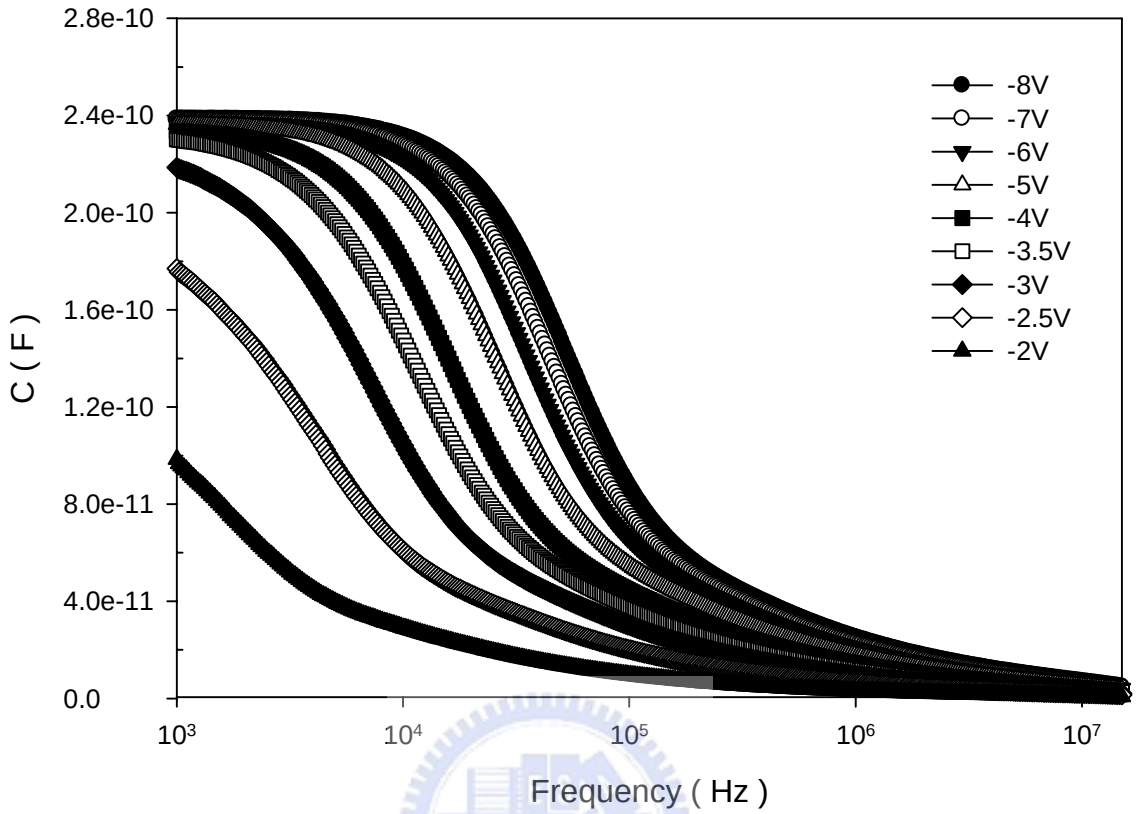


Fig.3-1-11 C-f curves of ELA p-type poly-Si TFT. W/L=600μm /600μm. V_G is biased from -2 *V* to -8 *V*. ELA laser energy is 380 mJ/cm^2.

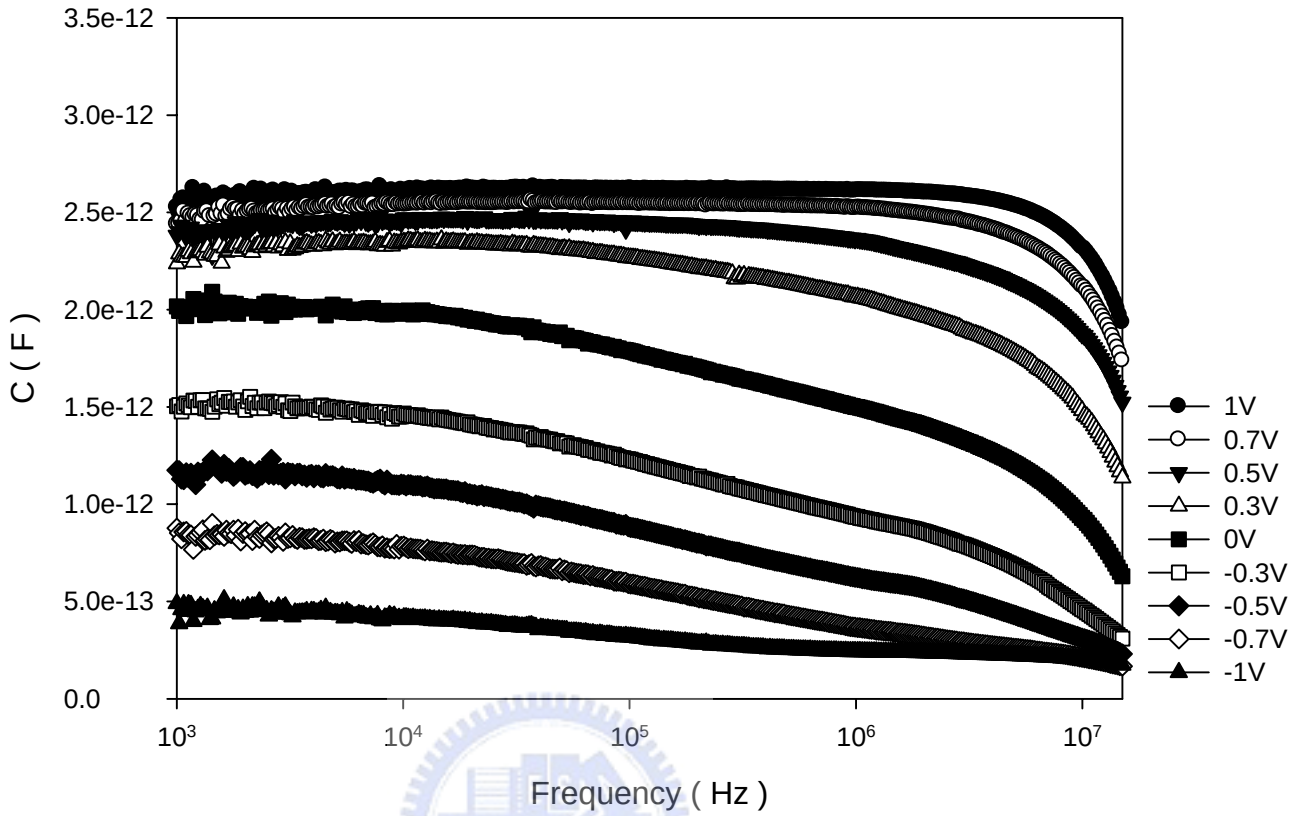
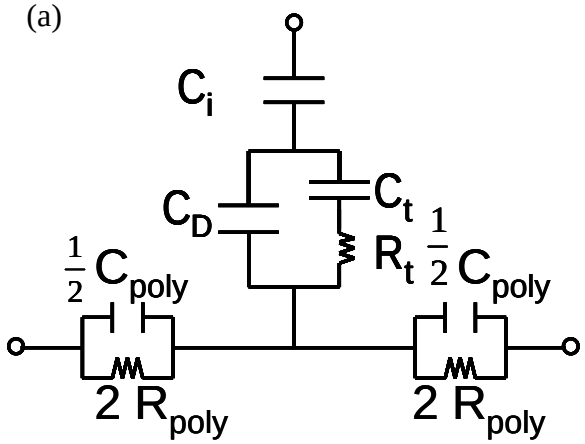


Fig.3-1-12 C-f curves of ELA n-type poly-Si TFT. W/L=600μm /6μm. LDD=0.75 μm. V_G is biased from -1 *V* to 1 *V*. ELA laser energy is 380 mJ/cm^2.

(a)



(b)

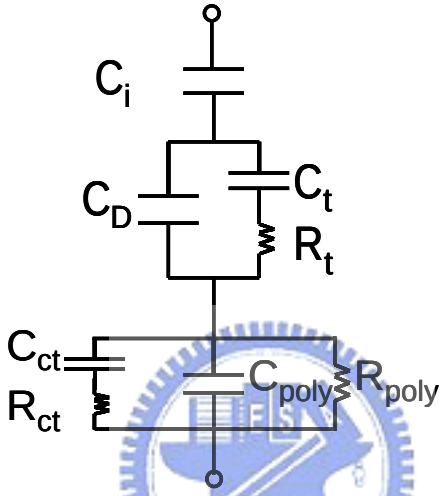


Fig.3-2-1 (a) Capacitance equivalent circuit model of poly-Si TFTs for short channel. (b) Capacitance equivalent circuit model of poly-Si TFTs.

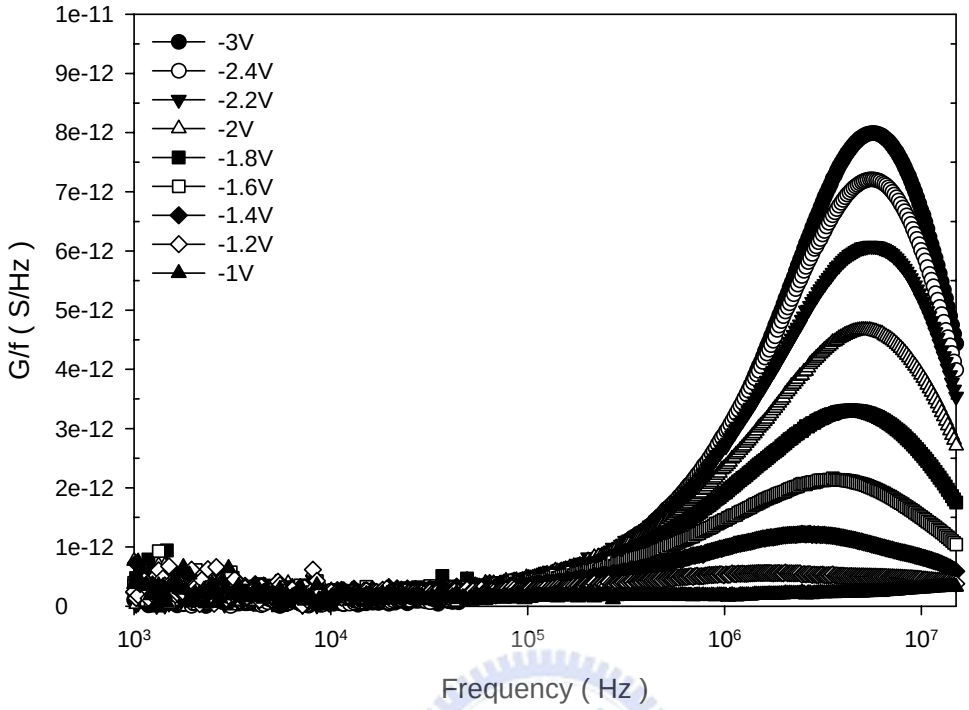


Fig.3-2-2 G/f-f curves of ELA p-type poly-Si TFT. W/L=600μm /6μm. ELA laser energy is 380 mJ/cm^2. V_G is from -1V to -3V.

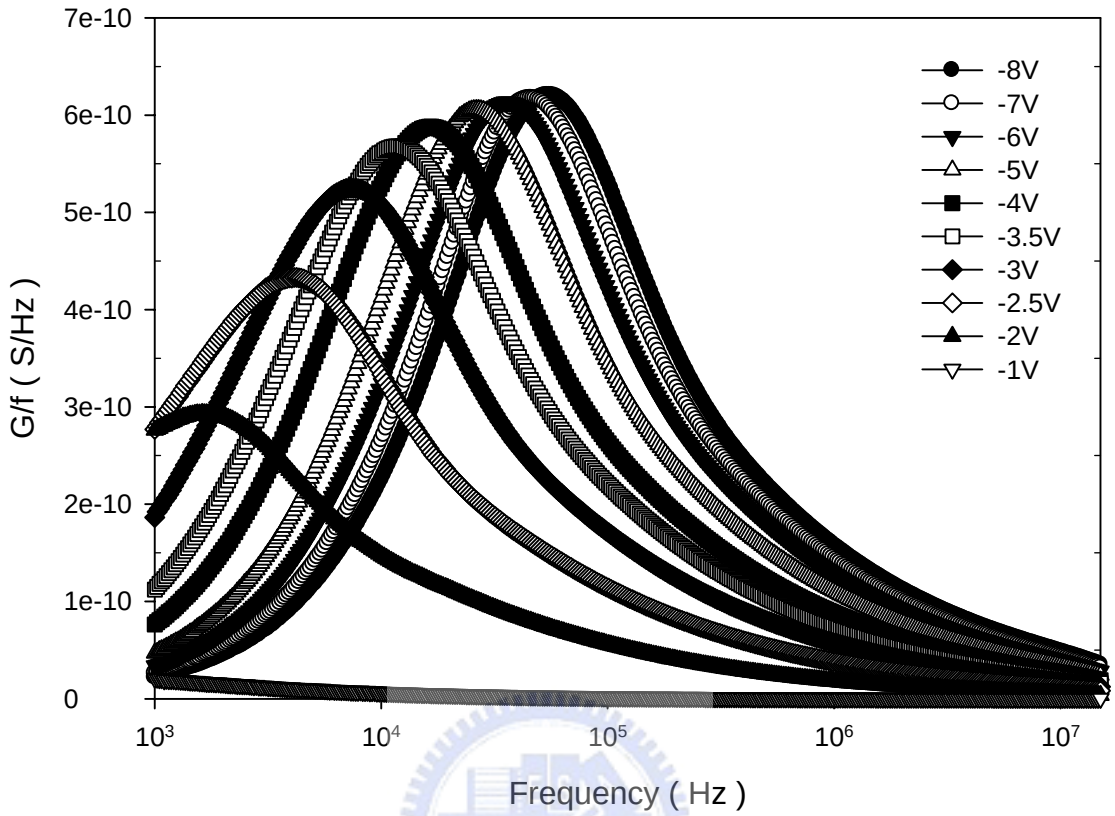


Fig.3-2-3 G/f-f curves of ELA p-type poly-Si TFT. W/L=600μm /600μm. ELA laser energy is 380 mJ/cm^2. V_G is from -1V to -8V.

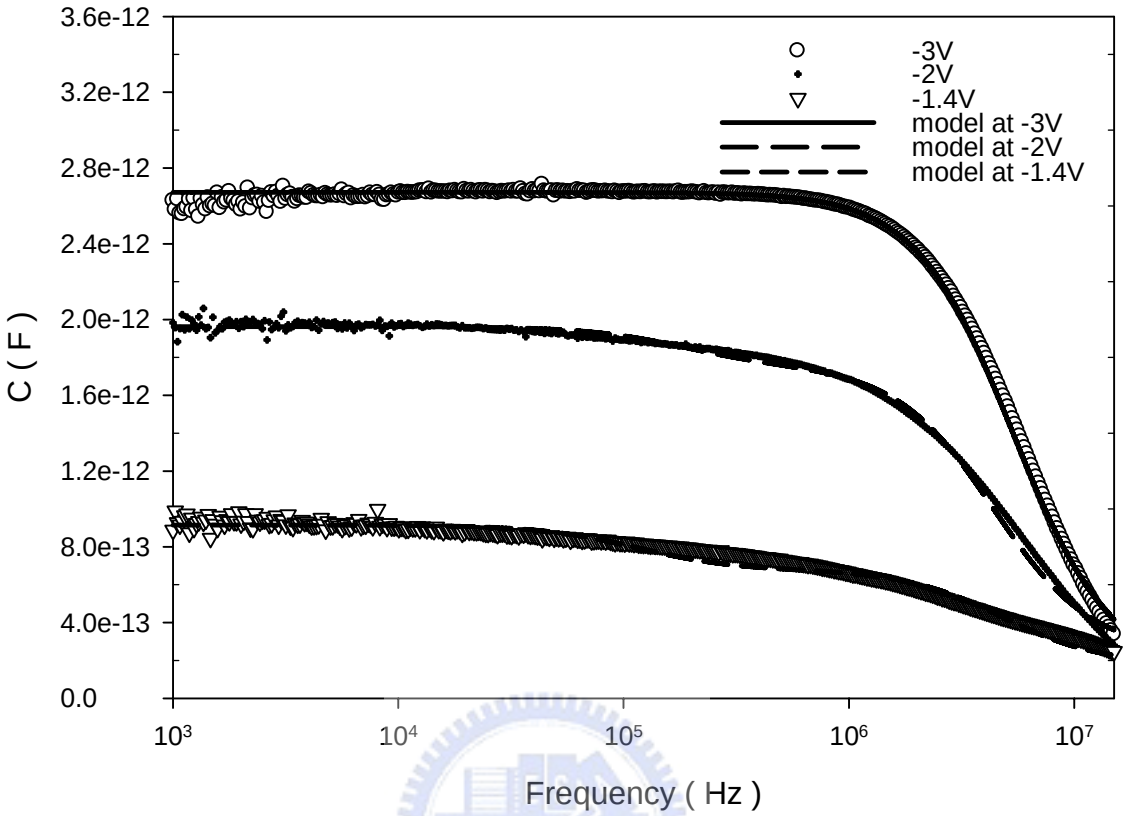


Fig.3-3-1 The curves are calculated using the model. ELA p-type poly-Si TFT. W/L=600μm /6μm. ELA laser energy is 380 mJ/cm^2.

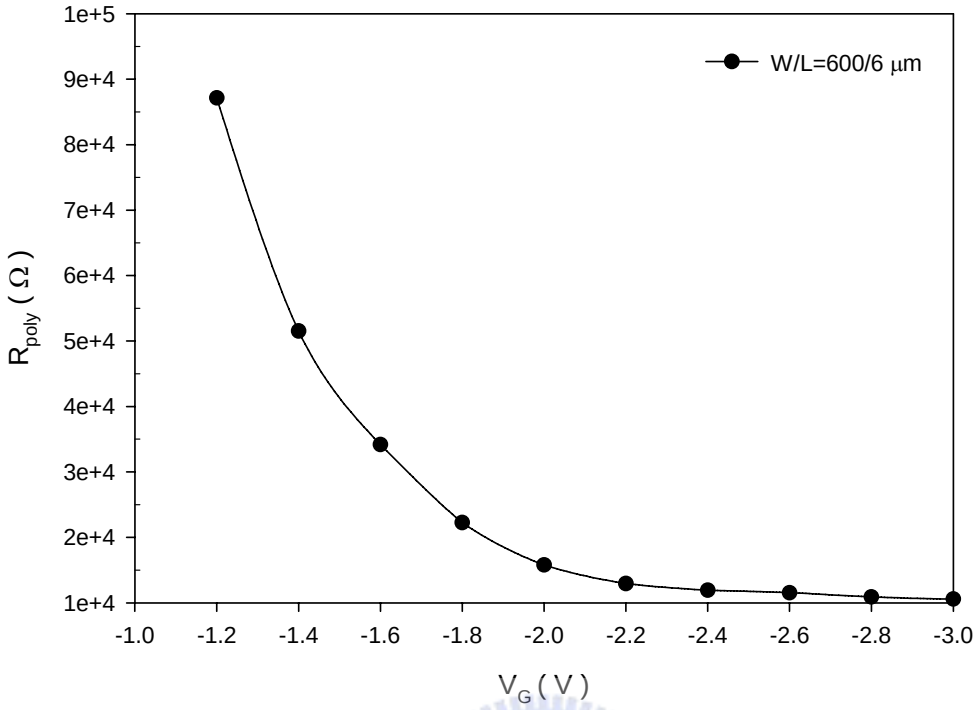


Fig.3-3-2 Extracted R_{poly} of ELA p-type poly-Si TFT. W/L=600μm /6μm.

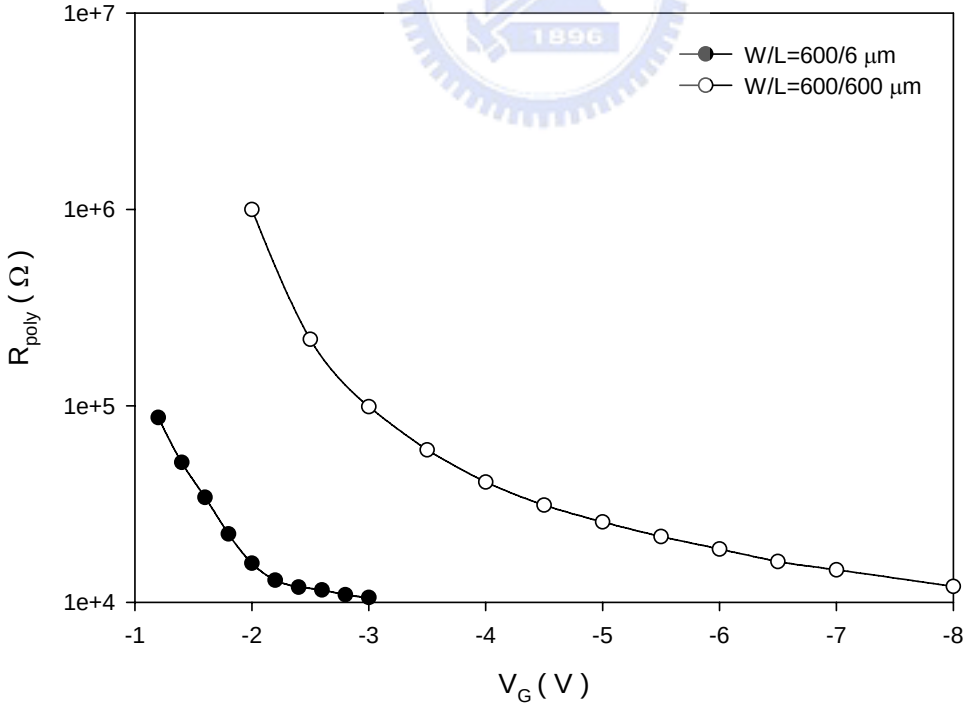


Fig.3-3-3 Extracted R_{poly} of ELA p-type poly-Si TFT. W/L=600μm /6μm, and 600μm /600μm.

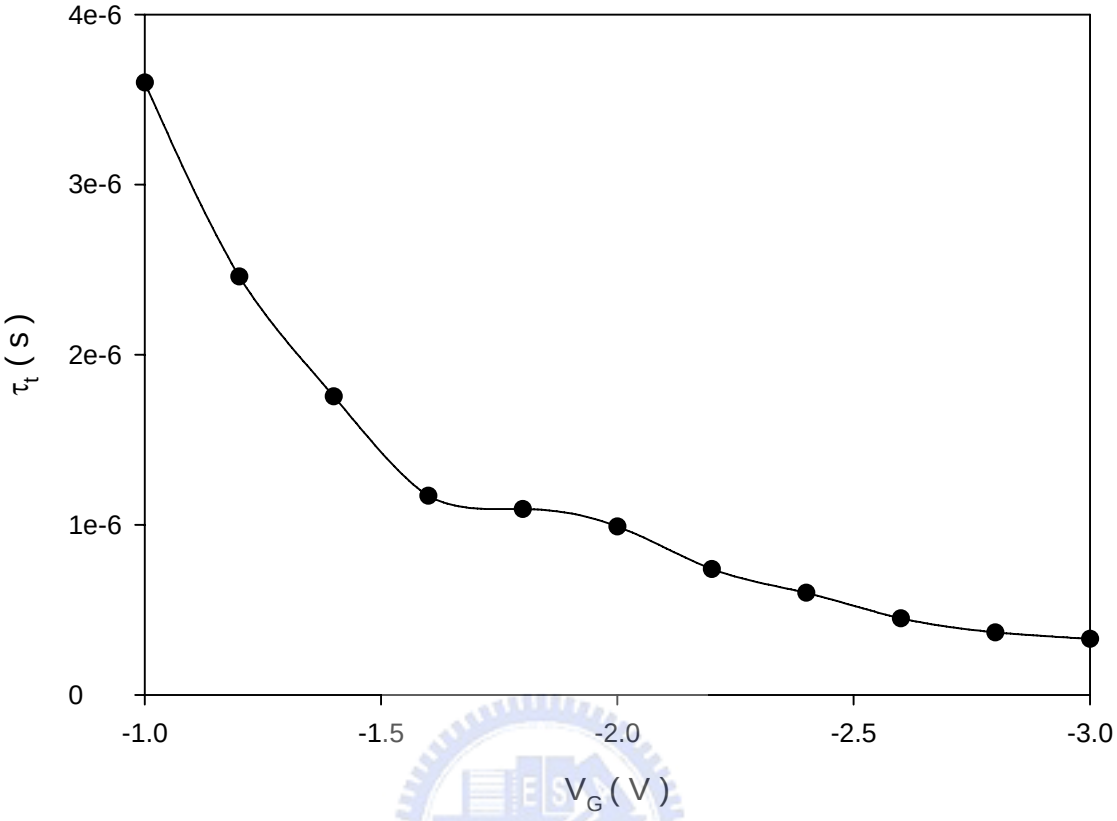


Fig.3-3-4 Trap response time of ELA p-type poly-Si TFT. W/L=600μm /6μm.

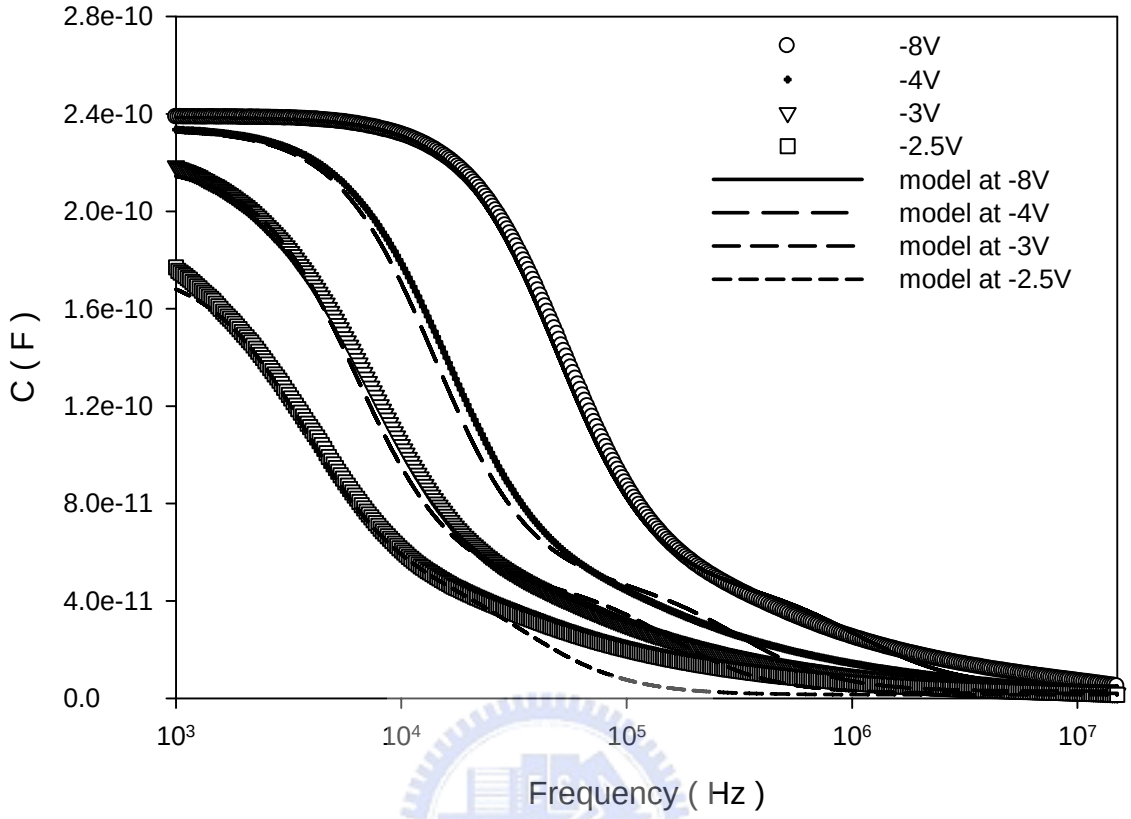


Fig.3-3-5 The curves are calculated using the model. ELA p-type poly-Si TFT. W/L=600μm /600μm. ELA laser energy is 380 mJ/cm^2.

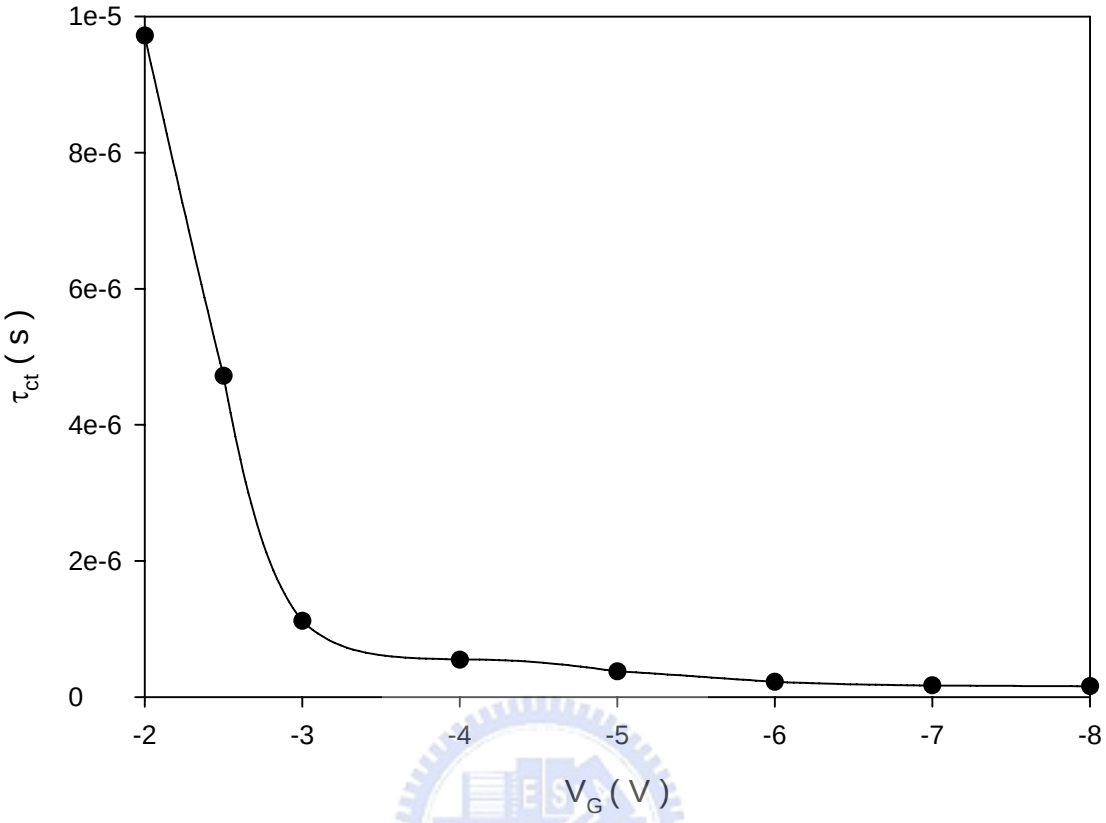


Fig.3-3-6 Channel trap response time of ELA p-type poly-Si TFT. W/L=600μm /600μm.

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(2005.09-2007.06)

論文題目：

低溫複晶矽薄膜電晶體的電容模型及其頻率響應

Capacitance Model and its Frequency Response of Low-Temperature Polycrystalline Silicon Thin Film Transistors