國立交通大學

電子工程學系電子研究所

碩士論文

先進奈米元件結構
於光感測與太陽能電池之研究

The Research of Advanced Nanodevice Structures for Photo-Sensing and Solar Cell Application

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中華民國 九十六 年 十 月

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碩 士 論 文

A Thesis

Submitted to Department of Electronics Engineering & Institute of Electronics

College of Electrical and Computer Engineering

National Chiao Tung University

in partial Fulfillment of the Requirements

for the Degree of

Master

in

Electronic Engineering

October 2007

Hsin-Chu, Taiwan, Republic of China

中華民國九十六年十月

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摘　要

在本論文中，使用硒化鎘量子點和金奈米粒子，透過離子作用力建構多層光感測奈米元件結構於矽基板上。在掃描式電子顯微鏡的觀察下，證明其結構成功生長於矽基板上。在製程上，利用lift-off技術成功在電極上定義出奈米粒子和量子點所要的圖樣。最後在結合硒化鎘量子點和金奈米粒子的奈米結構中，照射 375 nm雷射光以及 0.16 mW/ cm^2日光燈後，在各種偏壓下有固定的光電流增加。在此研究中，在 0.16 mW/ cm^2日光燈照射下，可得到奈米元件的效率為 0.67%，最大光電流為 1.02nA，光電流體積密度 $1.334*10^{-23}A/nm^3$，單位體積產生功率為 $2.45*10^{-25}W/nm^3$。

在此同時，並做了三維方向的奈米元件探討(元件寬度、元件長度、元件層數)，實驗的結果發現元件長度的減少以及層數的增加有助於效率的提升，但是元件層數並非呈現線性的增加，而是在結構層數為八層之後開始會有飽和的現象。此外，以上的現象可以利用“奈米蕭特基二極體和電阻陣列”模型成功地解釋之，我們可以利用 HSPICE 去模擬此三維模型發現有同樣的現象。

最後，我們發現 24 層的金奈米粒子/硒化鎘量子點奈米結構之“太陽能電池效率”至少為先前金奈米粒子/硒化鎘奈米結構相關研究的 5 倍，且在我們理想的模型推導下，可以推得高效率太陽能電池。

The Research of Advanced Nanodevice Structures for Photo-Sensing and Solar Cell Application

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ABSTRACT

In this work, we used CdSe QDs and Au NPs to construct the multi-layer photo-sensing nanodevice structures on a silicon substrate through ionic interaction. By the SEM views, the CdSe QDs and Au NPs successfully deposited on the silicon substrate. In the nanodevice process, the lift-off technology was successfully utilized to define the pattern of the Au NPs and CdSe QDs. Finally, the Au / CdSe nanodevices were illuminated by the 375 nm laser diode and the 0.16 mW/ cm^2 daylight lamp. As a result, the multi-layer nanostructure composed of CdSe QDs and Au NPs, there was constant photocurrent increment to the current measured in the dark for each voltage bias after illumination with 375 nm laser and the 0.16 mW/ cm^2 daylight lamp. In this work, under 0.16 mW/ cm^2 daylight lamp illumination, the solar cell efficiency is 0.67%% . The maximum photocurrent is 1.02nA. The highest PVD (photocurrent volume density) is $1.334*10^{-23}A/nm^3$. The power volume density is $2.45*10^{-25}W/nm^3$.

Meanwhile, the 3-dimension (width, length and the number of the layer) nanodevice efficiency investigation was executed. The shorter and thicker devices would benefit the performance of the solar cell efficiency. However, increasing the number of the layer would cause the saturation

phenomenon when the number of the layer is more than eight. Besides, the above characteristics can be explained by the “nano-Schottky-diodes and resistor array” model. We can obtain the same phenomenon as using HSPICE to simulate the three dimensional model.

In conclusion, we found that the“solar cell efficiency”of the 24-layered Au NPs / CdSe QDs nanostructure is at least 5 times better than the previous work of the Au NPs / CdSe QDs nanodevices. The solar cell can achieve high efficiency based on our model calculation.

ACKNOWLEDGEMENTS

首先，感謝我的兩位指導教授，吳重雨老師與李耀坤老師，在這兩年來對我的耐心指導與諄諄教誨，讓我能夠順利完成碩士學業。記得剛進來交大唸電子研究所時，對於奈米科技的相關研究極俱陌生，深怕自己無法勝任接替廖廷偉學長的再續研究，研究過程中遇到種種挫折與失敗，多虧兩位指導教授的鼓勵與教誨，讓我可以循序漸進，完成此論文。在積體電路設計上，再次感謝吳重雨老師以他淵博的專業知識，給予我指導與啟發，讓我充分學習到分析電路的技巧；在生化領域上，萬分感謝李耀坤老師細心教導，充實我在生化方面的專業知識，使我受益良多。其次要感謝論文口試的評審委員，許鉦宗教授、謝志成教授對我的論文提出了許多寶貴的建議，使這篇論文的內容更加完整。真的很感謝您們！

接下來要感謝應化所陳登銘老師實驗室的黃靜萍學姐，在我碩士兩年的研究過程中給予最大的幫忙與經驗分享，讓我在研究的路途中走的更加順利；也感謝李耀坤老師實驗室的可欣學長，在我研究遇到挫折時給予鼓勵。感謝電子所羅正忠老師實驗室的建宏、正凱、宏仁，在製程上編幫助我解決不少問題。感謝電子所崔秉鉞老師實驗室的玉仁，對於製程技術上的建議。感謝奈米所許鉦宗老師實驗室的柏鈞學長，指導我設計光罩。我只能說認識你們真好；百忙之中抽空幫我照 SEM 的奈米所博士班陳蓉萱學姊；半導體中心 SEM 陳聯珠小姐，你們總是給予我不求回報的幫助，真的很感謝你們！當然還要感謝 307 實驗室的學長姊：林俐如學姊、陳勝豪學長、王文傑學長、蘇烜毅學長、虞繼堯學長、陳煒明學長、蔡夙勇學長、張志遠學長們給予我的指教幫忙和研究上的經驗傳承。同時也要感謝維德、晏維、國忠、順維、柏宏、松諭、巧伶、宗裕、世豪、鯉魚、小王，陪伴我度過這段溫馨的研究生活，增添了許多歡笑與回憶；還有幫忙我許多的學弟：政邦，以及其他學弟妹國權、威宇、建銘、筱妊，謝謝你們，也祝你們研究順利，早日畢業!

最後，要感謝我的父母以及所有的親戚朋友們，感謝您們在我研究生活的兩年中給予莫大的加油鼓勵，讓我可以順利完成碩士學業。還有要感謝雅姿，在我面對龐大壓力時給我的鼓勵。最後把我的論文研究成果獻給在天上的外公、外婆，希望我所認識的朋友都可以過的平平安安。

廖廷偉

誌於 風城交大　2007 秋

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FIGURE CAPTIONS

CHAPTER 1

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TABLE FOR FULL TEXT OF CHEMICAL REAGENTS

Simplified Form	Full Text (or Synonyms)	Formula	Molecular Weight
TMSPED	N-[3-(trimethoxysilyl)propyl]-ethylene diamine	$C_8H_{22}N_2O_3Si$	222.36
APTES	3-aminopropyltriethoxysilane	$C_9H_{23}NO_3Si$	221.37
PDDA	Poly(diallyldimethylammonium chloride)	$(C_8H_{16}ClN)_n$	
Tyramine	4-(2-Aminoethyl)phenol	$C_8H_{11}NO$	137.18
AET	2-aminoethane thiol	$C_2H_7NS.HCl$	113.61

CHAPTER 1

Introduction

1.1 Background

Over the past three decades into today's powerful disciplines and knowledge that allow the engineering of advanced technical device has been developed based on fundamental chemistry, biotechnology and material science. They are focus on current approaches emerging at the intersection of materials research, nanosciences, and molecular biotechnology. The novel and highly interdisciplinary field of chemistry is closely associated with both the chemical and physical properties of organic and inorganic nanoparticles (NPs), as well as to the various aspects of molecular cloning, recombinant DNA and protein technology, and immunology. Today's materials research is used to develop instruments and techniques for basic and applied studies of fundamental biological processes [1]. The pioneering work of Pedersen, Cram, and Lehn on supramolecular aggregates held together by weak non-covalent interactions in a highly interdisciplinary effort has developed over the past 30 days into a well-established discipline. Supramolecular chemistry concerns the investigation of nature's principles to produce fascinating complex and functional molecular assemblies, as well as the utilization of these principles to generate novel device and materials, potentially useful for sensing, catalysis, transport, and other applications in medicinal or engineering science. In this area, the enormous advance attained so far is illustrated impressively by comparing materials used in last centuries electrical devices such as millimeter-sized copper wires to today's submicrometer-sized optical and electronical parts, comprised of modern conducting and electro-luminescent

organic polymers [1]. The significant property of nanotechnology is its "interdisciplinary nature". The chemistry is the central science for the development of applied disciplines such as material science and biotechnology as shown in Figure 1.1. Material science, which is based on classic chemical research fields and engineering technologies, has led to enormous advances in tailoring advanced modern materials, such as ceramics, nanoclusters, and conducting polymers. For biotechnology combined with tailored biomolecules, like proteins, nucleic acids, compartments, and organelles. We can merge these disciplines to take advantage of the improved evolutionary biological components to generate new smart materials and develop future nanodevices composed of various advanced modern materials [1].

As we can see in Figure 1.2, both biotechnology and materials science meet at the same length scale. A gap currently exists in the engineering of small-scale devices. Whereas conventional top-down processes hardly allow the production of structures smaller than about 100 nm, the limits of regular bottom-up processes are in the range of about 2-5 nm. Their own dimensions show a result, two different types of compounds appear to be suited for addressing that gap: (1) biomolecular components, such as proteins and nucleic acids, and (2) colloidal NPs comprised of metal and semiconductor materials. The main concepts in the development of human civilization are the conventional *top-down processes*. As human technology develops, people tend to fabricate more and more delicate tools or functional devices. However, this strategy will eventually reach a limit that people cannot easily go beyond based on available technologies. For example, the structural dimensions of computer microprocessors are currently in the range of about 65 nm, which is already the highest level of conventional top-down technology. "There is plenty of room at the bottom", as Nobel physicist Richard Feynman pointed out more than 40 years ago, which best describes the central idea of nanotechnology [1]. Today's nanotechnology research puts a great

emphasis on the development of bottom-up, which concern the self-assembly of molecular and colloidal building blocks to create larger, functional device. Inorganic NPs are particularly attractive building blocks for the generation of larger superstructure. Such NPs can be prepared readily in large quantities from various materials by relatively simple methods. It can be controlled the sizes of the NPs from one to several hundred nanometers. Most often, the particles are comprised of metals, metal oxides, and semiconductor materials, such as Ag_2S, CdS, CdSe, and TiO_2. The NPs have highly interesting optical and electrical properties, which are very different from those of the corresponding bulk materials and which often depend strongly on the size of particles in a highly predictable way. Moreover, some types of NPs can be considered as "artificial atoms" since they are obtainable as highly perfect nanocrystals, which can be used as building blocks for the assembly of larger two- and three-dimensional structures [1].

Inorganic NPs are attractive building blocks for the construction of nanostructured materials and devices with adjustable physical and chemical properties. With a variety of inorganic NPs now at hand, the identification of chemical methods for the selective linkage of these nano-building blocks to produce nanostructured aggregates, or clusters, of controllable structure becomes increasingly important. The amine modified SiO_2 and carboxylic acid modified Au and CdSe NPs has been self-assembly in aqueous solution to give well-defined core-shell type cluster, whose composition can be controlled with the pH. Ligand modified 50 nm SiO_2, 7 nm Au, and 6 nm CdSe NPs were employed for the electrostatic assembly [2]. Transmission electron micrographs of SiO_2@Au and SiO_2@CdSe composites formed at the indicated solution pH values are shown in Figure1.3 and 1.4, respectively.

Recently, semiconductor NPs are being vigorously investigated as new materials for traditional electronic and optical applications, as chemical and biological sensors,

and as building blocks for conceptually novel molecule-based devices. Most of these practical implementations of nanotechnology will require the immobilization of NPs on various substrates in the form of thin films. One of the new techniques that can be used for NP processing in thin films is the layer-by-layer assembly on polyelectrolyte has been proposed. It affords a high degree of structural control and quality of the coatings. [3]. However, the forces that make the assembly to happen are similar to those that involve in the interaction between molecules, such as hydrogen bonds, coulombic force, and Van der Waals force [1] [2] [3].

In general, with work involving self-assembly processes, nucleotides with various lengths were employed to take advantage of their self-recognition and self-assembly abilities [4]. The synthesis of ~ 15 nm Au NPs by Citrate Reduction method and ~ 5 nm CdSe NPs by Tyramine-modification method was reported in literatures, which provide negative-charged and positive-charged on the surface of the NPs, respectively [4][5]. For further study, the resulting solution consisting of Tyramine-modified CdSe NPs was vacuumed to dryness and re-dissolved in D.I. water [6]. In order to modify the silicon oxide substrate provide amino groups ($-NH3^{+}$) for assembling of Colloidal Au NPs, the silicon oxide substrate was immersed in a 10% N-[3-(trimethoxysily)propyl] ethylene diamine (TMSPED) / methanol solution for several time and further washed by methanol to remove excess TMSPED [7]. Recent research in several of nanodevices / nanostructures with unique optical and electrical properties has increased significantly. Among these nanodevices / nanostructures, semiconductor NPs exhibited spectacular size-dependent properties when the particles size is less than 10 nm, and producing the quantum-effect [8]-[10]. As the particles size becomes smaller, the band gap becomes larger, resulting in the blue shift of UV-visible absorption spectrums [11]. For metal NPs, the Fermi level lies at the center of one continuous band. As a result in literatures, across the entire

size range, the optical and electrical behaviors of metal NPs are described using classical equations for corresponding bulk metal material rather than quantum mechanical concepts [12]. Most recently, a 350 nm diameter Au-CdSe-Au nanowires were fabricated using a template growth method, and can function as sensitive photo sensors, which can potentially be massively multiplexed in devices of small size [13]. However, the fabrication process and the electrofluidic alignment method of nanowires as described in the study were not feasible with conventional silicon chip. Consequently, since the potential application of this device on silicon chip is severely limited, a new nanomaterials and/or a new process for the fabrication of nanodevice on silicon chips arise. The process of assembling negative-charged Au NPs and positive-charged CdSe NPs onto the silicon chip has been developed and proposed in [14].

1.2 Reviews on Nanodevice

Several of the assembly processes, inorganic nanoparticles (NPs) and nanoclusters are the most attractive ones. Recently, the researches on the synthesis, characterization and applications of inorganic NPs have been increasing significantly. The inorganic NPs have some advantages: (1) Many well-developed synthesis methods of the NPs have been proposed, which are often simple and cheap for large quantity preparation. (2) The NPs have their unique optical, electronic, and catalytic properties, which are quite different from those of their corresponding bulk materials. For example, when the size of NP becomes smaller than its Bhor exciton radius (~6 nm for CdSe NP), the photo-excited electrons are delocalized. (3) The size of NPs, conventionally ranging from one to hundreds of nanometers, is particularly suitable

for them to serve as building blocks for the assembly of larger nanostructures and contact closely with the micro systems, like the silicon chips.

In this section, we review some significant experiments about nanodevices composed of nanomaterials or NPs. One of the methods to construct nanodevices is the self-assembly techniques, which provide a means to realize structures such as quantum dots (QDs), NPs and other electronic / optoelectronic device configurations. Because these techniques do not rely on lithography to realize the specific nanostructures and assemblies, they can represent efficient, high throughput fabrication approaches. For self-assembled semiconductor structures, the electronic device functionality has been limited by the difficulty in achieving suitable interfaces for passivating and contacting the resulting islands or dots [15]. A patterning method of trapping and deposition of NPs in a submicron narrow gap have been developed in recently year. It demonstrated a light-emitting device, which consists of NPs trapped in the gap of lateral electrodes. The CdSe/ZnS NPs in the solvent were electrostatically trapped as a dielectric material in the gap by lateral electric field. The NPs were deposited in the gap as the solvent was evaporating. Electroluminescence from the NPs in the gap was observed when current was applied through the lateral electrodes [16]. Fig 1.5(a) shows a schematic diagram of the method. It was able to fabricate an ultra small light source smaller than the wavelength of visible light. This small light source can be applied to optical devices, such as scanning probes, integrated photonic crystals, and so on. The fabrication process of the submicron sized light source was shown in Figure 1.5(b). At first, an electrode structure on p-type SOI was made with DRIE (The Alcatel A601E), and then a submicron gap was fabricated by cutting the electrode structure with Focused Ion Beam (FIB) that can enable us to fabricate a submicron narrow gap easily. Next, the wafer was immersed in NPs solution of toluene solvent, and applied the voltage to the gap between the lateral

electrodes to trap NPs. At last, wafer was annealed at 400℃ to remove excess organic molecules such as toluene and TOPO. After annealing, junctions between p-type Si and CdSe/ZnS NPs were built [16].

The synthesis of quasi-one-dimensional (1D) nanostructures has been developed, many of which have interesting electronic, optical, and chemical sensor properties that derive from size, composition, and shape. One-component systems are now quite common, but there are few examples of methods for synthesizing multi-component 1D materials composed of organic and inorganic materials. The hybrid multi-component (i.e. organic-inorganic) nanorods that have either diode or resistor properties has been proposed in [17]. In a typical experiment, the synthesis of segmented metal-polymer nanorods by electrochemical deposition of gold into alumina templates, followed by electrochemical polymerization of pyrrole (Ppy). During the electrodeposition process, it can control the length of each block by monitoring the charge. Other metals (e.g. Ag and Cd) with low work functions and inorganic semiconductors (e.g. CdSe), also can be deposited on top of the polymer block and polyaniline can be used in place of polypyrrole. This allows one to prepare multi-component rod structures with tailorable electronic properties that derive from the choice of the individual compositional blocks. For the Au portions of the nanostructure (contacts 1-2 and 3-4) exhibit linear I-V characteristics and bulk metallic behavior at room temperature as shown in Fig. 1.7(A), and demonstrate Ohmic behavior. For the Au-Ppy-Au system, one can see dark Ppy domains sandwiched between two bright segments of gold as shown in Fig. 1.6(A). Significantly, Fig. 1.7(B) shows the I-V measurements across the Ppy block of the Au-Ppy-Au nanorod (2-3 and 1-4 contacts) also exhibit a highly reproducible, linear response at room temperature but nonlinear behavior at low temperature (<175 K), characteristic of a semiconductor. The I-V curves and the corresponding electrical

conductivities provide two important observations. First, the conductivity of the polymer block at room temperature is 6 orders of magnitude lower than the metallic blocks, and all data are consistent with Ohmic contact between the Ppy-Au junctions. Second, the I-V response for the Au-Ppy-Au nanorod becomes slightly nonlinear as the temperature decreases [Fig. 1.7(B)]. Since the Ppy for the nanostructures discussed herein were generated by oxidative polymerization, they are p-type semiconductor. Continuously, four-segment nanorods (Au-Ppy-Cd-Au) also can be prepared via an analogous procedure [Fig. 1.6(B)]. I-V measurements on devices constructed from single Au-Ppy-Cd-Au rods exhibit "diode" behavior at room temperature as shown in Fig. 1.7(C), and the typical response is asymmetric and non-Ohmic. In the forward bias, there is a positive voltage on the Au block adjacent to the Ppy and negative potential on the Au block interfaced with the Cd block. Therefore, holes move from the Ppy block to the Cd block during the forward bias. In reverse bias, current does not flow until the bias overcomes the breakdown potential (-0.61 V). The turn-on voltage for these diode nanorods is approximately 0.15V. The I-V characteristics of the Au-Ppy-Cd-Au nanorods at room temperature suggest that an Schottky-like junction is formed at Ppy/Cd due to the difference in work functions of the two materials and an Ohmic junction at the Ppy/Au interface due to the similarity in work functions for the two materials. It is a powerful method for deliberately producing structures with desirable electrical properties with a straightforward synthetic procedure that offers a high degree of reproducibility [17]. These structures could be useful for a wide range of electronic and sensor devices.

Now, we will introduce the state of current and coming solar photovoltaic technologies and their further development. The emphasis is on R&D advances and cell and module performances, with indications of the limitations and strengths of crystalline (Si and GaAs) and thin film (a-Si:H, Si, $Cu(In,Ga)(Se,S)_2$, CdTe). The

contributions and technological pathways for *now and near-term* technologies (silicon, III–V, and thin films) and status and forecasts for next-next generation photovoltaic (organics, nanotechnologies, multi-multiple junctions) are evaluated. Recent advances in concentrators, new directions for thin films, and materials/device technology issues are discussed in terms of technology evolution and progress. Insights to technical and other investments needed to tip photovoltaic to its next level of contribution as a significant clean-energy partner in the world energy portfolio [18]. The research progress over the past 25–30 years has been substantial and steady, as shown in Fig. 1.8. Photovoltaic is poised at what may be its most critical tipping point; the one that will cause this technology to "spread like wildfire" as it finally becomes a major part of our world's energy portfolio.

Recently, in order to provide innovative strategies for designing next generation energy conversion devices, people efforts to design ordered assemblies of semiconductor and metal NPs as well as carbon nanostructures. Renewable energy such as solar radiation is ideal to meet the projected demand but requires new initiatives to harvest incident photons with higher efficiency, for example, by employing nanostructured semiconductors and molecular assemblies. Dye sensitization of mesoscopic TiO_2 has been widely used in this context. Power conversion efficiencies up to 11% have been achieved for such photochemical solar cells. Semiconductors such as CdS, PbS, Bi_2S_3, CdSe, and InP, which absorb light in the visible, can serve as sensitizers as they are able to transfer electrons to large band gap semiconductors such as TiO_2 or SnO_2. CdSe quantum dots (QDs) have been assembled onto mesoscopic TiO_2 films by using bifunctional surface modifiers (SH-R-COOH) [19]. During visible light excitation, CdSe QDs inject electrons into TiO_2 nanocrystallites. The injected charge carriers in a CdSe-modified TiO_2 film can be collected at a conducting electrode to generate a photocurrent. The TiO_2-CdSe

composite, when employed as a photoanode in a photoelectrochemical cell, exhibits a power conversion efficiency of 12%. Significant loss of electrons occurs due to scattering as well as charge recombination at TiO_2/CdSe interfaces and internal TiO_2 grain boundaries. Fig. 1.9 shows the assembled TiO_2 and CdSe NPs using bifunctional surface modifiers of the type HS-R-COOH. Fig. 1.10 shows the sequence of steps followed.

One approach to facilitating electron transport in nanostructured semiconductor films involves applying a positive bias to the working electrode. The photocurrent generated at different applied potentials for OTE/TiO_2 and OTE/TiO_2/CdSe electrodes is shown in Fig. 1.11. Excitation of TiO_2 and TiO_2/CdSe films was carried out using light with wavelengths greater than 300 and 400 nm, respectively. Both films show anodic photocurrents when subjected to band gap excitation. The observed photocurrents increase as the potential is swept toward positive values. The potential at which we observe zero current is a measure of the flat band potential and reflects the maximum attainable open-circuit voltage (V_{oc}). We observe zero current at potentials of -0.78 and -0.88 V vs. SCE for TiO_2 and TiO_2/CdSe films, respectively. The 100 mV shift represents the improved energetic of the TiO_2/CdSe films and shows the advantage of using composite nanostructures for boosting V_{oc} [19].

1.3 Motivation

As we have discussed previously, interactive forces between molecules, such as hydrogen bonds, Van der Waal force, and coulombic force, are also effective for NPs and play an important role in the assembly process. The researches on the synthesis of organic and inorganic NPs have been increased significantly. Among the semiconductor NPs, CdSe QDs or QDs is the most suitable for harvesting light energy

in the visible region of the solar spectrum. So many researchers always choose the CdSe QDs or QDs to realize the nanodevices, optical devices, and solar-like devices. Recently, the photo-sensing nanodevice composed of negative-charged Au and positive-charged Tyramine-CdSe QDs has been developed and proposed. This functional nanodevice composed of inorganic NPs directly on the surface of silicon chip is the simplest and most effective process and without damage of the circuits in silicon chip. However, the method of Tyramine modification on CdSe QDs will seriously damage the optical and electrical properties of CdSe NPs. Therefore, it is important to develop more efficient methods. In our works, we propose another modify method of CdSe QDs and follow the 'dipping-and-washing' process to improve the performance of Au / CdSe nanodevice, continuously, we also construct another nanodevice composed of CdSe-modified QDs based on "self-assembly technology".

Meanwhile, to correctly define the pattern of the QDs and NPs, lift-off process was utilized for this purpose. Finally, three dimension nanodevice model is simulated by HSPICE. It successfully explains the phenomenon of the characteristics of the nanodevice. The power conversion efficiency can achieve 40% based in our ideal interference on the basis of the 3-D nanodevice model.

1.4 THESIS ORGANIZATION

The background has been introduced in section 1.1, including the basic concepts, the trend of nanotechnology development in the world, the synthesis methods of Au and CdSe QDs, and several of assembly methods of NPs on silicon substrate. Then, we have some reviews on the most representative experiments about nanodevices

based on nanomaterials, QDs, and NPs in section 1.2. At last, the motivations of this work and thesis organization will be proposed in section 1.3 and section 1.4.

In chapter 2, the fabrication technology will be discussed, including the process flow and the nanodevice structure design concepts. In section 2.1 and 2.2, the synthesis of Au NPs and CdSe QDs will be introduced. Then, the physical characteristics of the nanodevices will be demonstrated. In section 2.4, some experiments of the environment factors were tested to optimize the reaction conditions. In section 2.5, the electrode process with the lift-off technology will be proposed to solve the unexpected NPs and QDs. In section 2.6, the self-assembly technology of the nanodevice process is announced.

In chapter 3, experimental results will be showed and discussed. First, the measurement environment is introduced in the section 3.1. Secondly, the nanostructure physical characteristics would be demonstrated, for example, SEM view and absorption / emission Spectra. Thirdly, different layer Au / CdSe (AET-CdSe and PDDA-CdSe) Nanodevice would be measured. Then, the results would be showed and discussed in section 3.3. Next, Nanodevice solar cell efficiency would be estimated in section 3.5. Finally, using HSPICE software to construct the nanodevice model was executed in section 3.6. The simulation result fits the nanodevice measurement results, and it also could explain the electrical characteristics of the different dimension nanodevice.

In chapter 4, a linear regulator is designed to target the low voltage conditions and integrated with the CdSe / Au nanoparticle solar cell. The relevant analysis is introduced to design the system, and the TSMC 2P4M CMOS 0.35um technology is used to implement the linear regulator. Finally, the measurement result of the linear regulator chip is showed and discussed.

In chapter 5, the conclusions and future works are given in section 5.1 and 5.2.

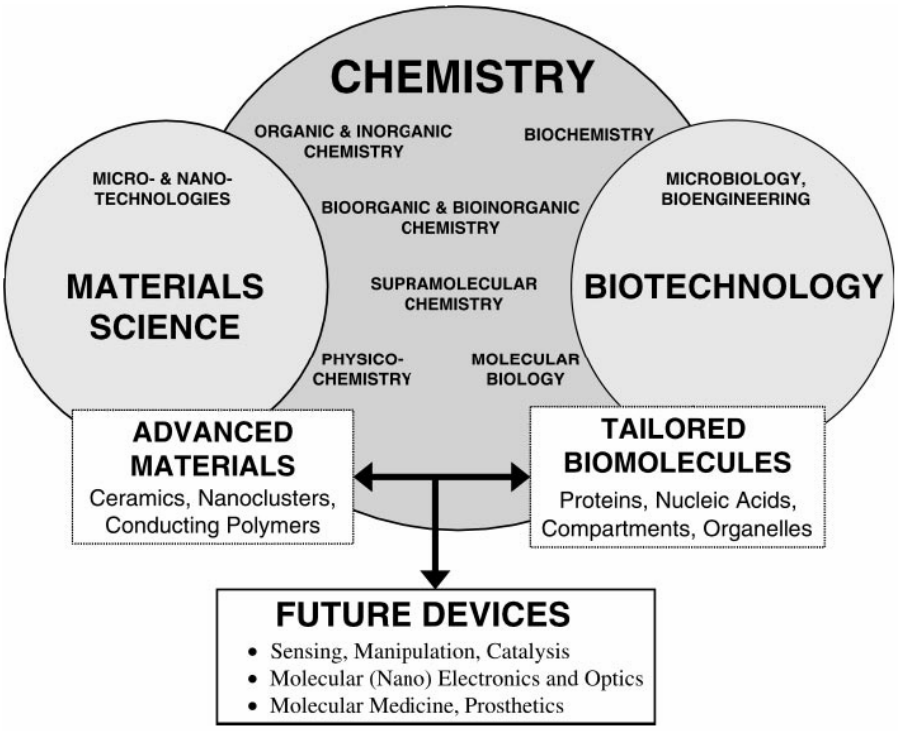


Figure 1.1 Chemistry is the central science for further applications such as materials science and biotechnology. The combination of advanced materials and tailored biomolecules will produce the future nanodevices [1].

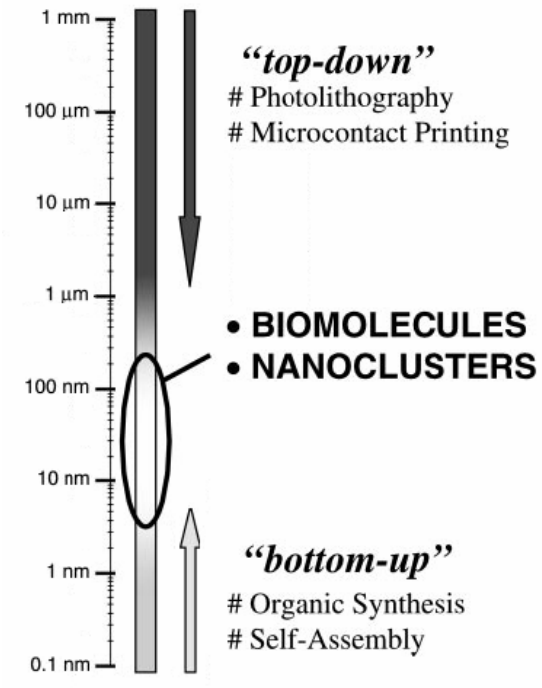


Figure 1.2 A gap currently exists in the engineering of small-scale devices. The top-down processes will have their limit below 100 nm, and the bottom-up processes will also have a limit at 2~5 nm. The gap will be filled by nanoclusters and biomolecules [1].

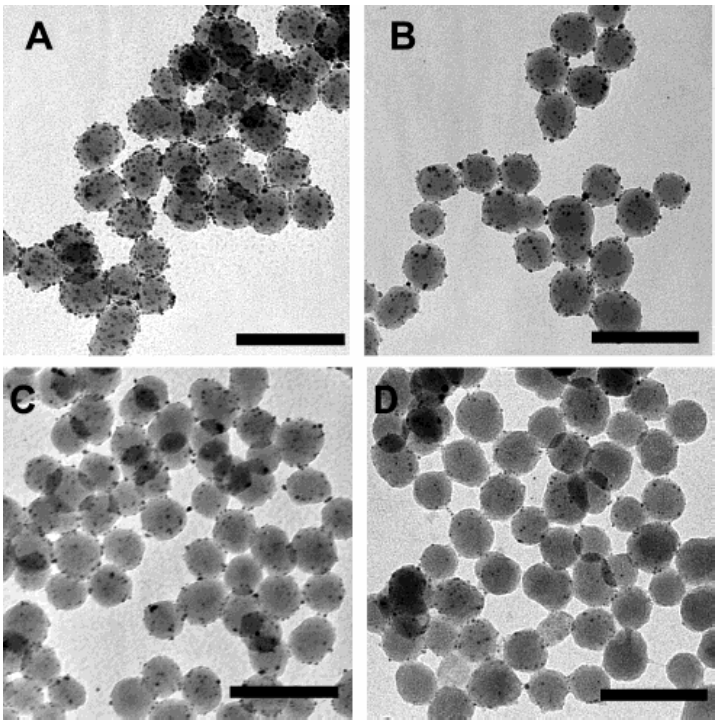


Figure 1.3 The TEM images of SiO_2@Au NP clusters synthesized at (A) pH=8.4, (B) pH=8.6, (C) pH=10.2, (D) pH=11.1. The scale bar for all micrographs is 200 nm [2].

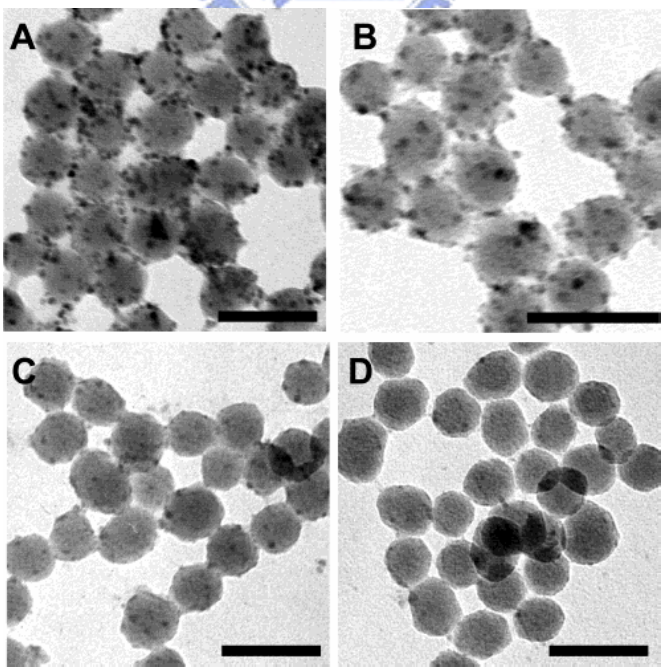
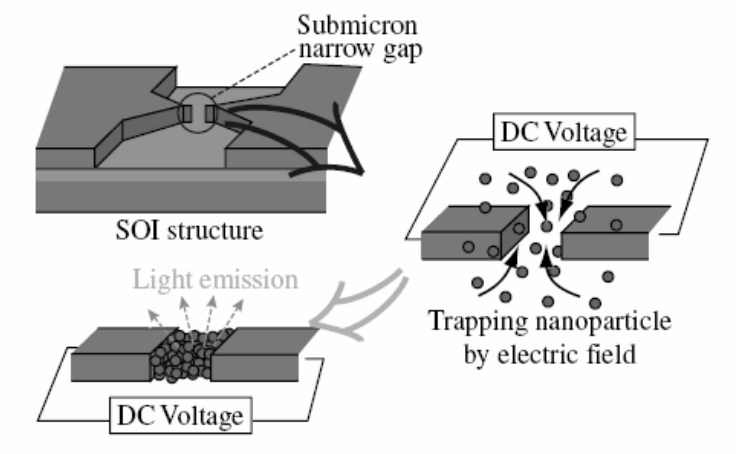
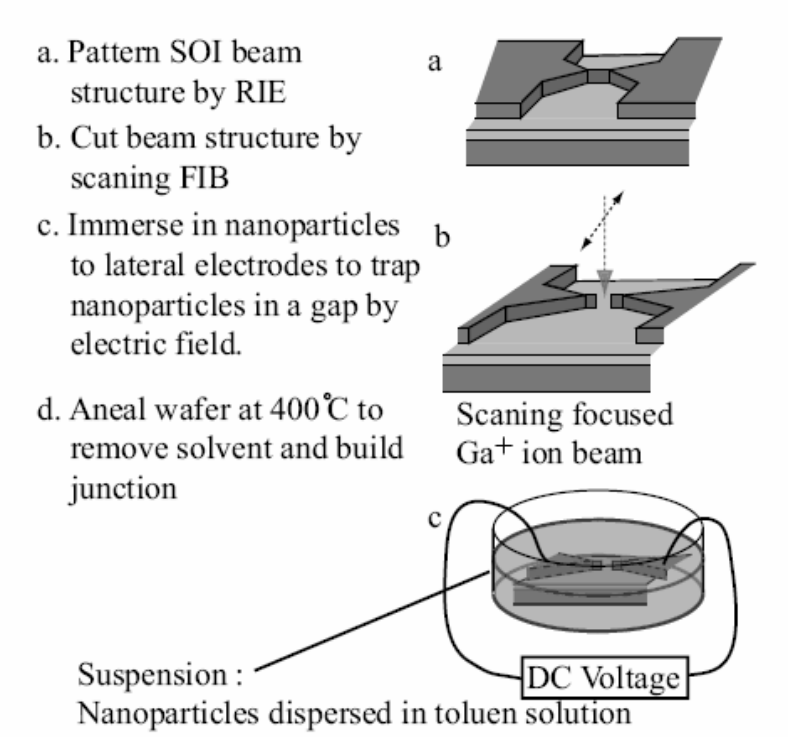


Figure 1.4 The TEM images of SiO_2@CdSe NP clusters synthesized at (A) pH=6.8, (B) pH=7.2, (C) pH=10.2, (D) pH=11.1. The scale bar for all micrographs is 100 nm [2].



(a)



(b)

Figure 1.5 (a) The schematic diagram of trapping NPs in a submicron narrow gap (5 μm * 5 μm * 1 μm) and a submicron sized light source. (b) The fabrication process of a submicron sized light source based on SOI and CdSe QDs [16].

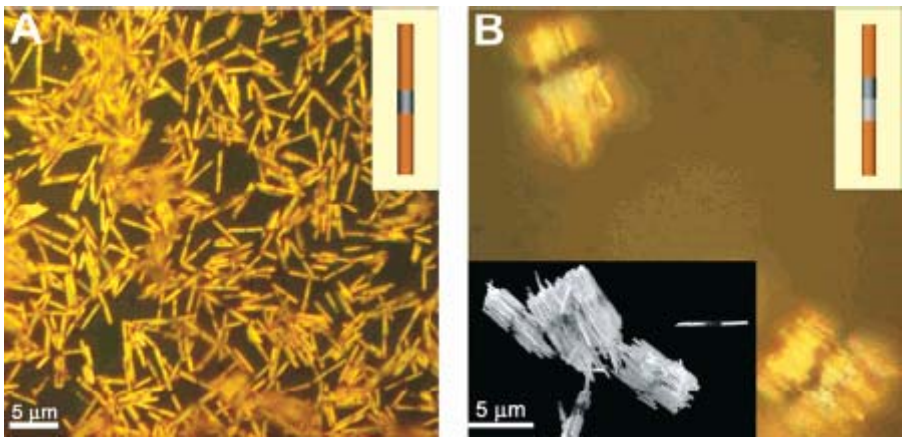


Figure 1.6 (A) Optical microscope image of Au-Ppy-Au rods. (B) Optical microscope image of Au-Ppy-Cd-Au rods. The lower left inset shows the corresponding FESEM image [17].

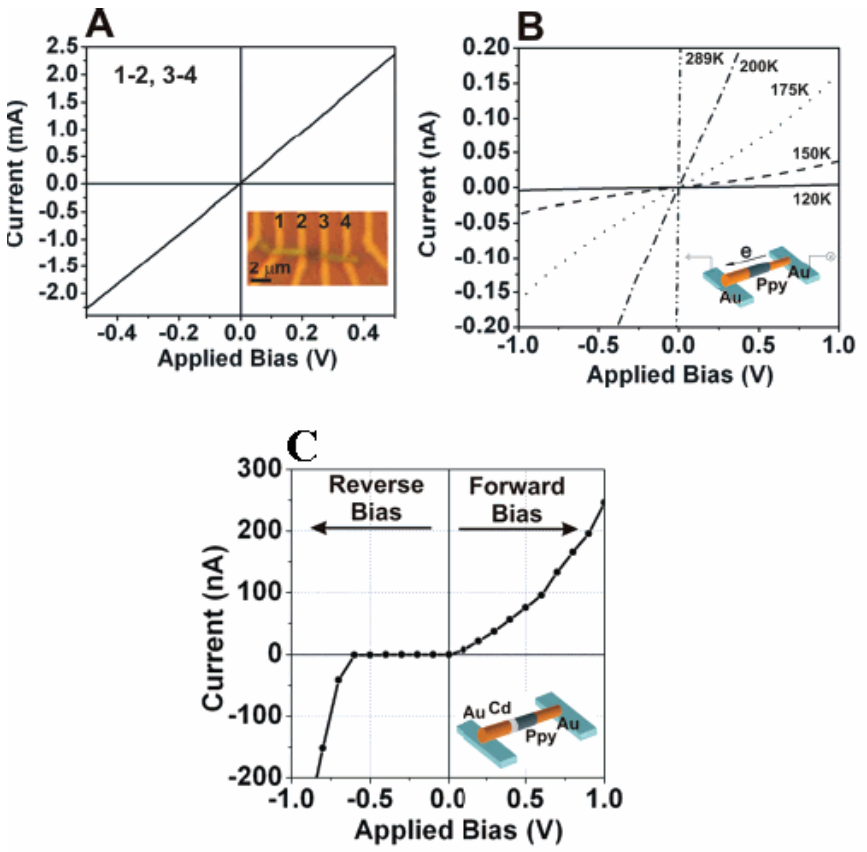


Figure 1.7 The measurement results of I-V characteristics. (A) For the gold blocks (1-2, 3-4) within a single nanorod at room temperature. Inset shows the optical microscope image (1000 magnification) of a single Au-Ppy-Au rod on microelectrodes. (B) Temperature-dependent I-V curves for measurements across electrodes 2 and 3. (C) For a single Au-Ppy-Cd-Au rod at room temperature [17].

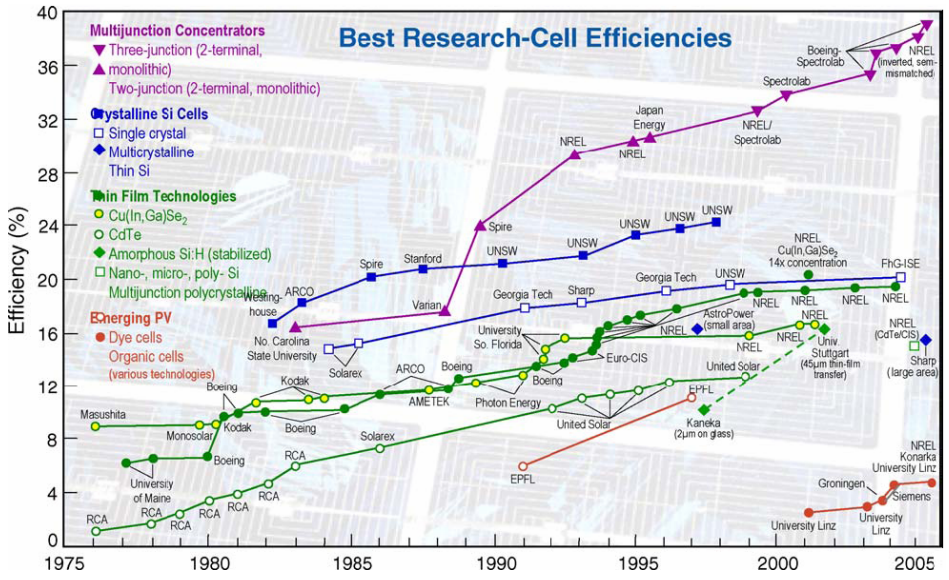


Figure 1.8 The efficiency evolution of best research cells by several of technology types. This table identifies those cells that have been measured under standard conditions and confirmed at one of the word's accepted centers for standard solar-cell measurements [18].

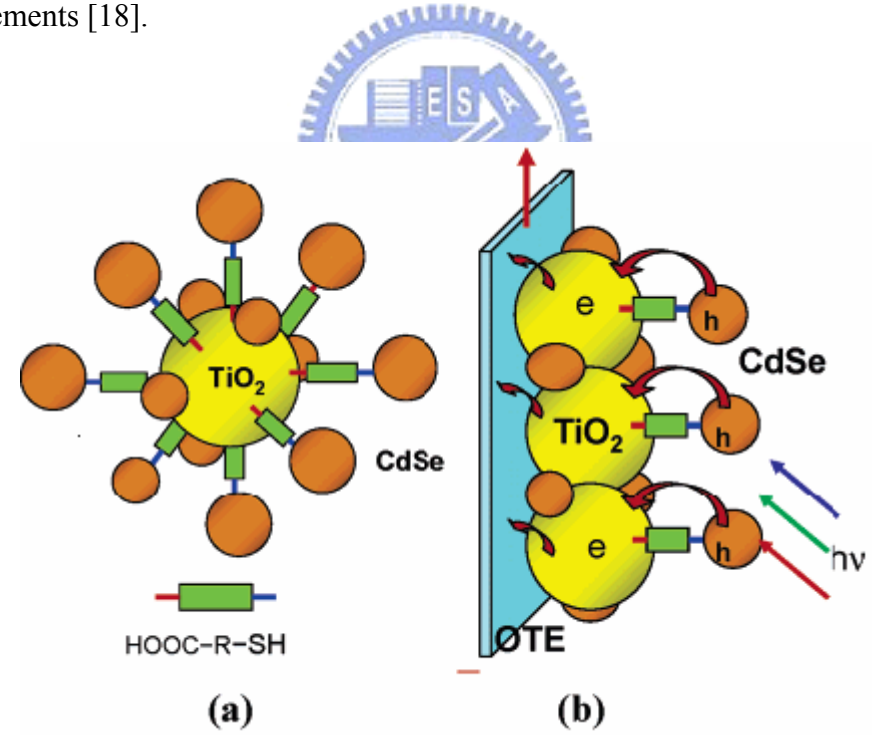


Figure 1.9 (a) Linking CdSe QDs to TiO_2 particles with bifunctional surface modifier (HS-R-COOH); (b) Light harvesting assembly composed of TiO_2 film functionalized with CdSe QDs on Optically Transparent Electrode (OTE) [19]. (Not to scale)

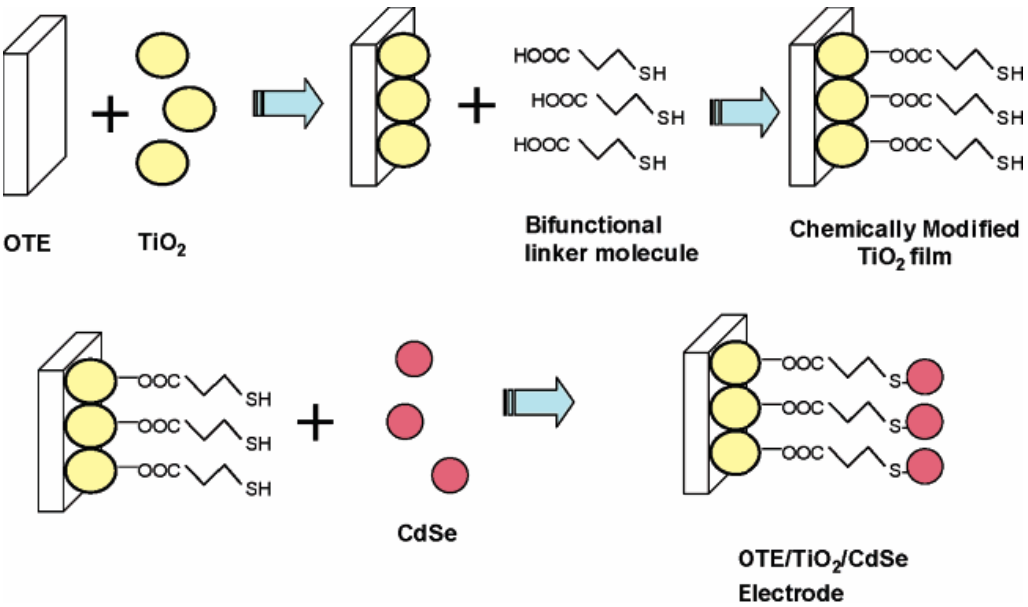


Figure 1.10 The sequence of steps for linking CdSe QDs to TiO_2 surface with a bifunctional surface modifier [19].

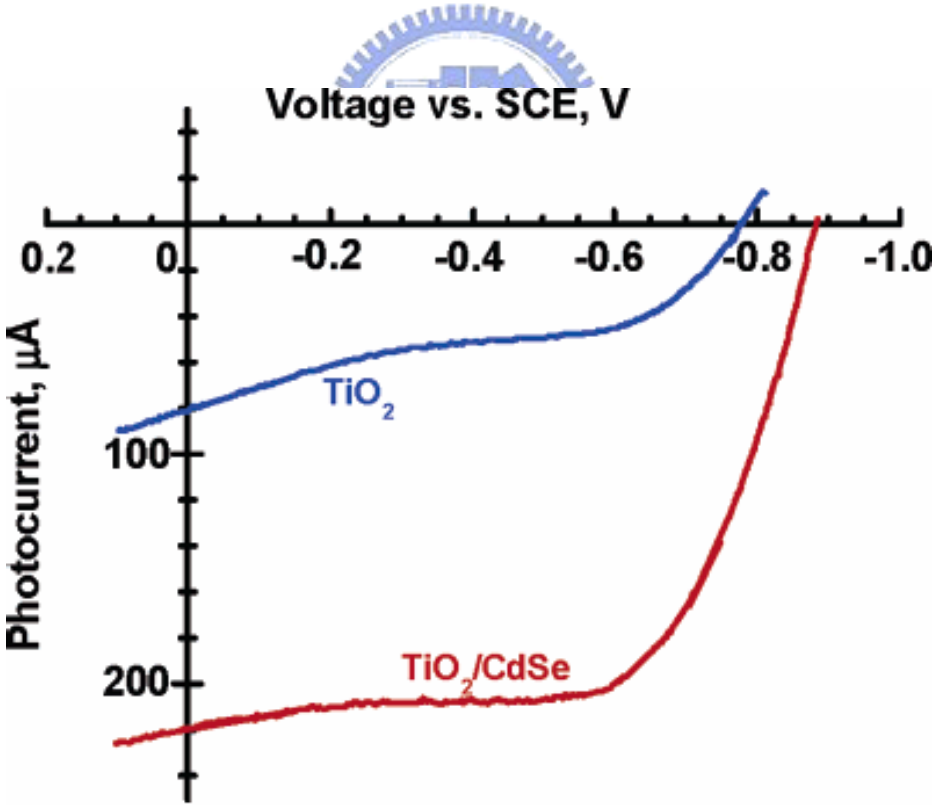


Figure 1.11 I-V characteristics of (a) OTE / TiO_2 and (b) OTE / TiO_2 / MPA /CdSe films. The filtered lights allowed excitation of TiO_2 and CdSe films at wavelengths greater than 300 and 400 nm, respectively [19].

CHAPTER 2
FABRICATION TECHNOLOGIES OF CdSe / Au NANOPARTICLES AND NANODEVICE

In this chapter, the fabrication technology will be discussed, including the process flow and the nanodevice structure design concepts. In section 2.1 and 2.2, the synthesis of Au NPs and CdSe QDs will be introduced. Then, the physical characteristics of the nanodevices will be demonstrated. In section 2.4, some experiments of the environment factors were tested to optimize the reaction conditions. In section 2.5, the electrode process with the lift-off technology will be proposed to solve the unexpected NPs and QDs. In section 2.6, the self-assembly technology of the nanodevice process is announced.

2.1 The Synthesis of Citrate-Capped Au Nanoparticles

Au NPs with ~ 15 nm diameter were prepared by citrate reduction of $HAuCl_4$ as described in literature [4]. The pale yellow $HAuCl_4$ solution (1 mM, 500 mL) was prepared and brought to reflux while stirring for 20 minutes. A solution of citric acid (38.8 mM, 50 mM) was then quickly injected into the flask. The color of the solution changed from pale yellow to deep red indicating the formation of Au NPs. After color changing, the solution was kept in reflux for additional 20 minutes and then standing in room temperature for another 30 minutes. Finally, the solution was

filtered through 0.45 μm Nylon filter. The flow diagram of the Au NPs solution preparation is shown in Figure 2.1. The close photograph of the Au NPs solution is shown in Figure 2.2(a), (left). The TEM image of the approximately 15 nm diameter Au NPs is shown in Figure 2.3(a) and the UV-visible absorbance spectrum of Au NPs solution is shown in Figure 2.3(b).

2.2 The Synthesis of AET-Capped and PDDA-Capped CdSe Quantum Dots

The emission efficiency, spectrum and time evolution of QDs are strongly affected by the surface. A better surface structure of QDs can provide higher stability, higher quantum yield and longer lifetime. Mostly the CdSe QDs lose a large portion of emission efficiency because of electron leakage resulting from the surface defect. Therefore, ZnS layer, a large band gap semiconductor, is used to passivate the surface and improve the quantum yield of CdSe NPs. The band gap diagram and the surface structures of CdSe/ZnS QDs are shown in Figure 2.4(a). It shows the PL intensity spectrum, which confirms the superior quantum yield property of CdSe/ZnS structure over the other two structures, CdSe and CdSe/CdS. The approximately 5 nm diameter fluorescent water-soluble ((PDDA)-coated) and (2-aminoethane thiol (AET)-coated) CdSe/ZnS QDs were obtained from Prof. Teng-Ming Chen's lab, National Chiao Tung University, Taiwan. The surface of the AET-coated CdSe/ZnS NPs had positive-charged amino groups ($-NH3^{+}$). In this section, we will to introduce the synthesis procedure of CdSe/ZnS QDs.

Synthesis of water-soluble AET-capped CdSe/ZnS QDs

In order to prepare positive charge on the NPs surface, the water stabilized amine terminating QDs (NP-NH_2) was fictionalized. Adding methanol washed off the HDA stabilizing layer and rendered a cloudy suspension which was centrifuged and the pellet containing QDs were washed with methanol 4 times to re-dissolve into chloroform. 1.0M 2-aminoethane thiol (AET) was added to the above solution and allowed to react for 2hrs. When ZnS capped CdSe QDs were reacted with AET, the mercapto group in AET bind to the Zn atoms and render the QDs hydrophilic, in addition to facilitating further functionalization possibilities. After the reaction, excess AET was washed off with methanol/chloroform mixed solution and store into the D.I. water.

The close photographs of the AET-CdSe/ZnS QDs solution is shown in Figure 2.2(a), (right). Figure 2.2(b) shows the close photographs of the mixture of 100 μL Au NPs solution and 100 μL AET-modified CdSe/ZnS QDs solution just after mixing (right), the mixture after standing 6 hrs (middle) in room temperature, and the mixture after standing 5 days in room temperature (left). As we can see, the color of mixture just after mixing was like that of Au NPs solution. However, after 6 hrs, it became dark purplish red. After 5 days, there was obvious precipitate at the bottom and the supernatant became pale yellow. The TEM image of the approximately 5 nm diameter CdSe/ZnS QDs is shown in Figure 2.3(a) and the UV-visible/PL spectra of CdSe/ZnS QDs solution is shown in Figure 2.3(c). The detailed modification processes of AET-capped CdSe/ZnS QDs are shown in Figure 3.5.

The PDDA-CdSe QDs are provided by Prof. Teng-Ming Chen's Lab.

2.3 The Physical Characteristics of Au Nanoparticles and CdSe Quantum Dots

Recently, many several of nanostructures or nanoparticles (NPs) have been proposed and improved significantly. They have their unique electrical and optical properties, herein, in order to achieve the Nanodevice that has good performance; we must know their electrical and optical properties as well as the size and the synthesis procedure of the NPs. In nanometer-scaled metal particles, for examples Au or Ag, are certain to be important fundamental building blocks of future nano-scale electronic and optical devices. However, there are numerous challenges that need to be addressed before NPs technologies can be implemented successfully. Metal particles comprise a fundamentally interesting class of matter in part because of an apparent dichotomy that exists between their sizes and many of their physical and chemical properties. For example, Au particles may be synthesized in diameters that span from the macroscopic down to the molecular scale (0.8 μm). Across almost this entire size regime, however, their electrical and optical behaviors are described with relatively simple classical equations, rather than the quantum mechanical concepts required understanding molecular entities. The classical free electron theory combined with optical constants for bulk gold is employed to successfully model the intense visible extinction of Au NPs. Moreover, the electrical and optical properties of metal particles can be tuned considerably simply by adjusting the size, shape, or extent of aggregation of the particles. For example, a typical solution of 13 nm diameter Au NPs is red in color and exhibits a surface plasmon band centered at 518-520 nm. After aggregation, the extended polymeric Au NPs/polynucleotide aggregate shows a red to purplish blue color change in solution, due to a red shift in surface plasmon resonance of Au NPs [4]. The optical property of Au NPs is dominated by collective oscillation

of conduction electrons resulting from the interaction with electromagnetic radiation. The electric field of incoming radiation induces the formation of a dipole in the NP. A restoring force in the NP tries to compensate for this, resulting in a unique resonance wavelength. The oscillation wavelength depends on particle size, particle shape and surrounding medium. [27]

In semiconductor nanocrystals, however, exhibit a wide range of size-dependent properties when the size regime is below 10 nm [9] [11]. Variations in fundamental characteristics ranging from phase transitions to electrical conductivity can be induce by controlling the size of the crystals [11]. There are two major effects to explain these size variation properties in nanocrystals. First, the number of surface atoms is a large fraction of the total atoms of a single nanocrystal. The high surface-to-volume ration will make a contribution to variations in thermodynamic properties of nanocrystals, such as melting point, and solid-solid phase transition. Second, nanocrystals with the same interior bonding geometry as the corresponding bulk material but with only a few hundred to thousand atoms exhibit dramatic size-dependent optical and electrical properties. These variations are because the density of states of electronic energy levels transforms as a function of the size of interior nanocrystal, known as **quantization effects** [11]. Nanocrystals lie in between the atomic and molecular limit of discrete density of electronic states and the extended crystalline limit of continuous bands.

The diagrams of density of states in metal and semiconductor nanocrystals are shown in Figure 3.6. Now in any material, there will be a size below which there is substantial variation of fundamental electrical and optical properties with size, which will be seen when the energy level spacing exceeds the temperature. For a given temperature, this occurs at a very large size in semiconductors, as compared to metal, insulators, and Van der Waals or molecular crystals. This can be understood by

considering that the bands of a solid are centered about atomic levels, with the width of the band related to the strength of nearest-neighbor interactions. As the size of solid increases, the center of a band develops first and the edges develop last. Thus, in metal, the Fermi level lies in the center of a band, so that the relevant energy level spacing is still very small, and at temperature above a few Kelvin, the electrical and optical properties of a metal solid react more closely like those of no energy level spacing, even as small as tens or hundreds of atoms. In semiconductor, however, the Fermi level lies between two bands, so that the edges of bands dominate the low-energy optical and electrical behavior. Optical excitations across the gap depend strongly on the size, even for crystallites as large as 10,000 atoms. Besides, the HOMO-LUMO gap increases as the semiconductor nanocrystals become smaller (bellow 10 nm) [11].

In this work, we used positive-charged 2-aminoethane thiol (AET)-capped CdSe/ZnS (core/shell) NPs of approximately 5 nm in diameter as photoreceptors to detect lamination with above band gap photoexcitation [11]. We proposed two nanodevices composed of semiconductor QDs and/or metal NPs for self-assembly: (1) Au / AET-CdSe/ZnS. (2) Au / PDDA-CdSe/ZnS. However, some properties about CdSe QDs we must know that the **exciton Bohr radius** r_b is the spatial extent of the electron hole pair in material and is defined as $r_b = 4\pi\hbar^2\varepsilon / (m * e^2)$, where $\hbar$ is the Plank's constant, ε is the permittivity in bulk material, and m* is the effective mass. For CdSe semiconductor, the electron's effective mass is 0.13 m_e and hole effective mass is 0.45 m_e. So the exciton Bohr radius of CdSe is calculated to be 4.9 nm [8] [9**]**. If the dimension of CdSe QDs is smaller than 4.9 nm, the **quantum confinement** of electron hole pairs effects significantly. As size is reduced, the electronic excitation shift higher energy, and there is concentration of oscillator strength into a few transitions [9]. The dynamics of the charge carriers in CdSe QDs have been studied in

several reports. These studies revealed that photoexcitation leads to a bleach of the lowest exciton transition within the first few hundred femtoseconds [20]. The bleach recovery has a lifetime between several picoseconds to microseconds, which is similar to the lifetime of the photoluminescence. In literature, it is well known that electron acceptors adsorbed on the surface of CdSe QDs quench the exciton emission by fast electron transition [20]. Monitored the electrons shuttling across the interface of CdSe QDs by femtosecond laser spectroscopy and showed that in CdSe QDs with no electron acceptors adsorbed on the particle surface, the excited electrons get trapped at the surface within 30 ps. Subsequently, electron-hole recombination takes place on a much longer time period of > 10^{-7} s [20]. This is quite a useful knowledge for understanding the dynamics of electrons in CdSe QDs.

The electrical transport properties of nanocrystals also depend strongly on size. On extended crystal, the energy required to add successive charges does not vary. In a nanocrystal, the presence of one charge prevents the addition of another charge. Thus, in metal or semiconductor, the current-voltage curves of individual nanocrystal resemble a staircase, known as **Coulomb blockade effect** [11]. Steps in the staircase are spaced proportional to 1/radious of nanocrystal. A typical Coulomb blockade staircase is shown in Figure 3.7.

2.4 The Self-assembly Process of Au Nanoparticles / CdSe Quantum Dots Nanodevice with Lift-off Technology

In order to measure and utilize the power generated from the Nanodevices, the electrodes are required. Hence, the electrodes are prepared before the NPs and QDs process. The electrode cross-section view is shown as the Figure 2.8. The aluminum is used as the conductor to collect the current. On the other hand, the oxide layer is

utilized as the dielectric to prevent the substrate current flow to the aluminum. This phenomenon will cause the incorrect result to the measurement outcome.

In previous chapter, we have discussed the forces that direct the assembly of NPs is similar to those involving in the interaction between molecules, such as hydrogen bonds, coulombic force, and Van der Waal force. In this work, we utilize the coulombic force system control the assembly of NPs on the silicon substrate. In coulombic force system, we take advantage of the positive or negative charges on the surfaces of NPs to induce repulsion or attraction forces between different NPs or between NPs and the substrate. The repulsion force will prevent NPs from random aggregation before assembled on the substrate. On the other hand, the attraction force will assemble NPs on the substrate. By well controlling the two forces, we are able to construct the structure of photo-sensing nanodevice on the silicon oxide substrate effectively. The overall fabrication process of the photo-sensing nanodevice composed of CdSe QDs and Au NPs on the silicon chip by ionic interaction system is shown in Figure 2.14.

As the structure shown in Figure 2.9, one mask is needed to define the aluminum region (Figure 2.8(a)). The process flow of the electrodes process is demonstrated in Figure 2.10(a)-(g). First, the wafer was cleaned to remove the particles and organics on its surface as the Figure 2.10(a) shown. Secondly, thermal oxidization was carried out to form the oxide film as the dielectric layer as the Figure 2.10(b) demonstrated. The thickness of the oxide layer is 500nm. According to the standard process, the thickness is thick enough to prevent the substrate current from flowing onto the aluminum. Then, the next stage was to coat the aluminum on the oxide by the thermal coater. The thickness of the aluminum is 5 um. The cross-section view and the top-view of the process is shown in Figure 2.10(c). After thermal coating, the photoresist was coated on the surface of the aluminum to define the electrode region

at the next step (Figure 2.10(d)). The samples were exposed by utilizing the mask (Figure 2.8(a)) designed to define the electrode patterns (Figure 2.10(e)). Then, use the acid to etch the aluminum. Meanwhile, the photoresist protected the auminum designed to remain (Figure 2.10(f)). Therefore, the desire pattern was constructed. Finally, remove the photoresist by using the acetone, and the electrode process finished (Figure 2.10(g)).

In previous work, some problems were generated when the self-assembly technology was executed. As the Figure 2.11(a) shown, according to the SEM picture, some unexpected NPs and QDS appears. Therefore, the anticipated patterns of the electrode were disturbed by connecting with other electrode through the thin film composed of NPs and QDs. It is clear that unexpected NPs and QDs have influence on the measurement result. This phenomenon may be caused by the presence of the –OH groups on the surface of the electrodes, which can be modified by TMSPED molecules, making them suitable sites for NP assembly. The presence of NPs on the Al electrodes enhances continuity at the interface between the NP's packed silicon oxide surface and the Al electrodes. Identically, it also enhances continuity at the interface between the NP's packed passivation oxide surface and the Al electrodes. That is the reason why it is necessary to solve this problem.

Turning now to the current flowing path analysis, in figure 3.8(b), the cross-section view of the whole chip shows there are two paths for the current to flow. One is the major path that contains the metal line between the electrodes and the pads. The other is the minor path composed of the NPs and QDs. This path has low conductance because of the CdSe QDs, but it still provides a way for the photocurrent to flow. The unexpected QDs and NPs create the path for the photocurrent. As a result, the measurement of the electrodes (30umX5um, 30umX15um) is affected. To solve the problem issued above, one method to remove the unexpected NPs and QDs is

proposed. Lift-off technology is used in this work to realize the purpose.

First of all, the issue if the lift-off technology damages the nanostructure is concerned. The acetone is used in lift-off process to dissolve the photoresist and bring out the substance attached to the photoresist. Therefore, the acetone should not destroy the nanostructure. The experiment was executed to observe if the acetone destructs the physical characteristics of the nanostructure.

In general, the lift-off process needs the samples immersed in the acetone for a period. Therefore, this condition is simulated. Several 4-layer nanostructure samples were immersed for three kinds of different periods, 0 minute, 15 minutes and 30 minutes. Finally, the samples were observed under PL (Photoilluminace) measurement. Figure 2.12 shows the result of this experiment. The PL emission spectrum of 4-layer nanostructures on quartz glass is shown. The PL of the nanostructure decays as the immersed time increases. There is enough evidence to show that the acetone would damage the nanostructure optical properties.

According to the experimental result, the lift-off process must be executed without CdSe QDs. Therefore, the lift-off is implemented after the first Au-NP-layer is constructed.

Now, the lift-off process will be introduced below. The process flow is shown in the Figure 2.13. In the beginning, the electrode samples were prepared. Then, the samples were coated with photoresist on their surface as the Figure 2.13(a) shown. Next, the samples were exposed by using the definition of the mask 2 (Figure 2.8(b)). In this process, the region we want it to lift off was blocked by the mask (Figure 2.13(b)). In turn, the samples were put into the developer after they were exposed. The photoresist on the region that was exposed was removed (Figure 2.13(c)). In order to modify the electrode surface with positive charges, the electrode surface was modified by N- [3-(trimethoxysilyl) propyl] ethylene diamine (TMSPED) to make the

electrode surface provide amino groups (-$NH3^+$) as the Figure 2.13(d) shown. The sample was immersed in 10% TMSPED/methanol solution for 5 minute [7]. Note that because TMSPED is very moisture sensitive, the methanol used here must be completely dried and all cleaned glasswares must also be dried in oven at 65°C for 30 min prior to use. After immersion, the sample was cleaned by plenty of methanol to remove excess TMSPED staying on the surface, followed by dipping in 30 mM HCl for 3 seconds to protonate the amino groups. Finally, the silicon oxide substrate was cleaned by using plenty of D.I. water for several times and dried in vacuum. Subsequently, Citrate-capped Au NPs (~15 nm) were self-assembled to the TMSPED linkers. In order to construct photo-sensing nanodevice structures, the TMSPED-modified electrode sample was immersed in the Au NPs solution for 24 hours to make negative-charged (-COO^-) Au NPs assembled on the positive-charged (-NH_3^+) substrate by ionic interaction. Au NPs were coated not only on the electrode part but also on the photoresist region. Therefore, Au NPs were coated on the entire wafer (Figure 2.13(e)).

Next, the most important step of the experiment was to lift off the unexpected part where the Au NPs were on the photoresist. Then, the samples were immersed in the acetone for 5 minutes as Figure 2.13(f) shown. The Au NPs on the photoresist were remove with the photoresist. Therefore, the structure of the nanodevice is shown in Figure 2.46(g). After this step, the sample was immersed in the Au NPs solution for 24 hours again to confirm if the Au NPs were coated with high density.

After 24-hour-immersion, the sample was cleaned by D.I. water for several times to remove free Au NPs and then dried in vacuum. Subsequently, the sample was immersed in AET-capped CdSe/ZnS QDs solution for 24 hours to make positive-charged (-NH_3^+) AET-CdSe/ZnS QDs assembled to negative-charged (-COO^-) Au NPs, followed by D.I. water cleaning and vacuum dry as described above.

Theoretically, this process can be repeated for several times to form layers of closely packed CdSe QDs and Au NPs nanostructures. As a result, it can be used as the photovoltaic nanodevice. The measurement result and discussion will be investigated in the following chapter.

2.5 Reaction Environment Investigation

We may now proceed to investigate the environment factor which would have effect on the nanostructure, for example, reaction temperature and reaction time. These effects should be optimized. Accordingly, several experiments to affirm the suitable reaction condition for the nanodevice to fabricate were executed.

As a matter of fact, to construct the nanostructure is like to build the building. The base of the nanostructure should have high density. In this work, the base of the nanostructure is Au NPs which form the thin film. Therefore, if the density of the Au NPs is high, the second layer would also get high. The reason is that CdSe QDs assemble with Au NPs.

Hence, two experiments were executed. One is to observe the reaction time effect on the nanostructure construction. The other is to investigate the reaction temperature effect. Owing to the SEM picture of the nanodevice, we can judge which condition gets high density.

The first experiment is to observe if the different reaction time influence the nanostructure. Therefore, two piece of p-type silicon wafer was prepared. One was to be coated with Au NPs and CdSe QDs as a 2-layer basic nanostructure for 3 hours per layer. The other was to be coated in the same way, but 24 hours per layer reaction period. The result is shown as Figure 2.15. Figure 2.15(a) is the nanostructure that was fabricated with 3 hours reaction time per layer. Figure 2.15(b) is the

nanostructure that was constructed with 24 hours reaction time per layer. As a result, the 24-hour-reaction-time one got high particle density. It benefits the nanodevice construction.

The other experiment is to investigate the temperature effect on the nanostructure construction. Hence, two piece of p-type silicon wafer was prepared. One was to be coated with Au NPs and CdSe QDs as a 2-layer basic nanostructure in the room temperature environment. The other was to be coated in the same way, but in the 4^{o}C reaction environment. Figure 2.16 shows the experiment outcome. As the Figure 2.16(a) shown, the nanostructure which was constructed on condition of the room temperature got lower density.

On the basis of the previous two experiments, lower temperature and longer reaction period would benefit the nanostructure. Thus, these two factors would be adopted in the nanodevice fabrication technology.

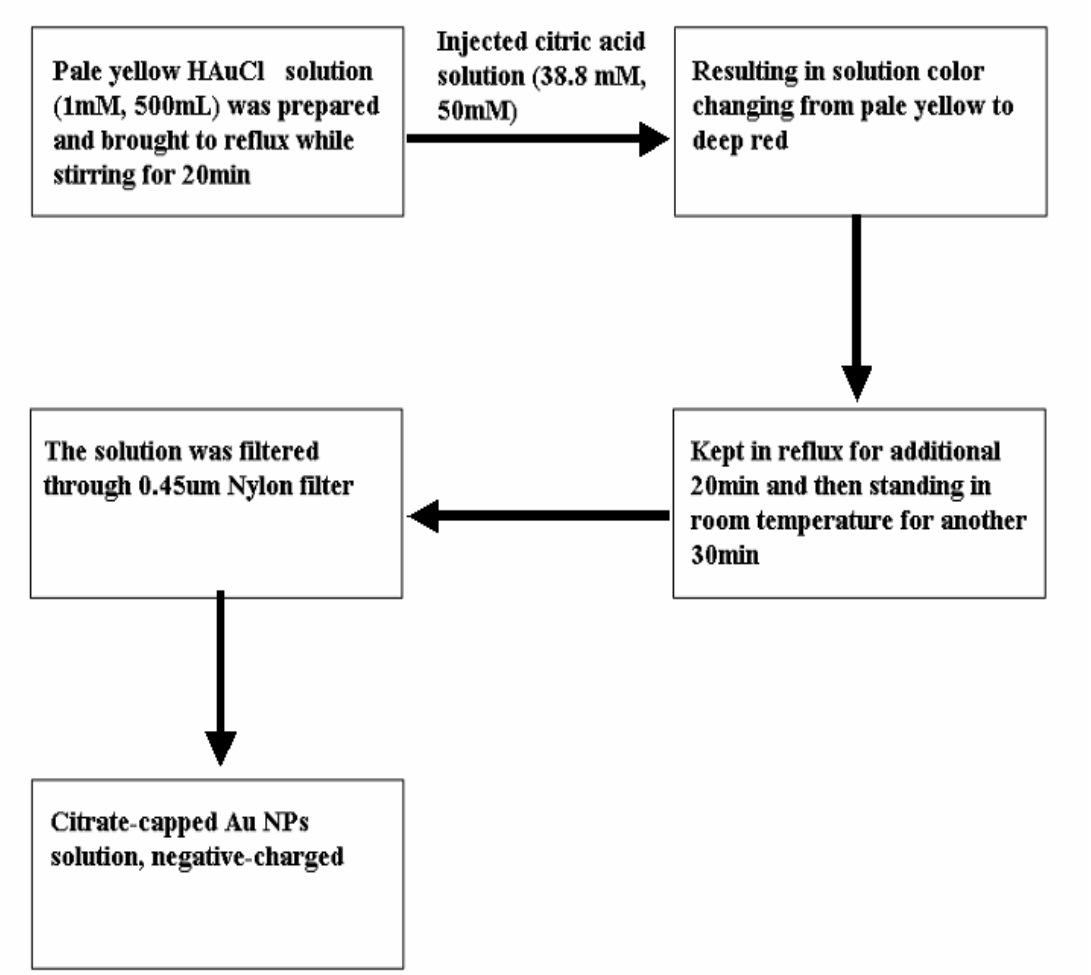


Figure 2.1. The flow diagram for preparing the Citrate-capped Au NPs solution.

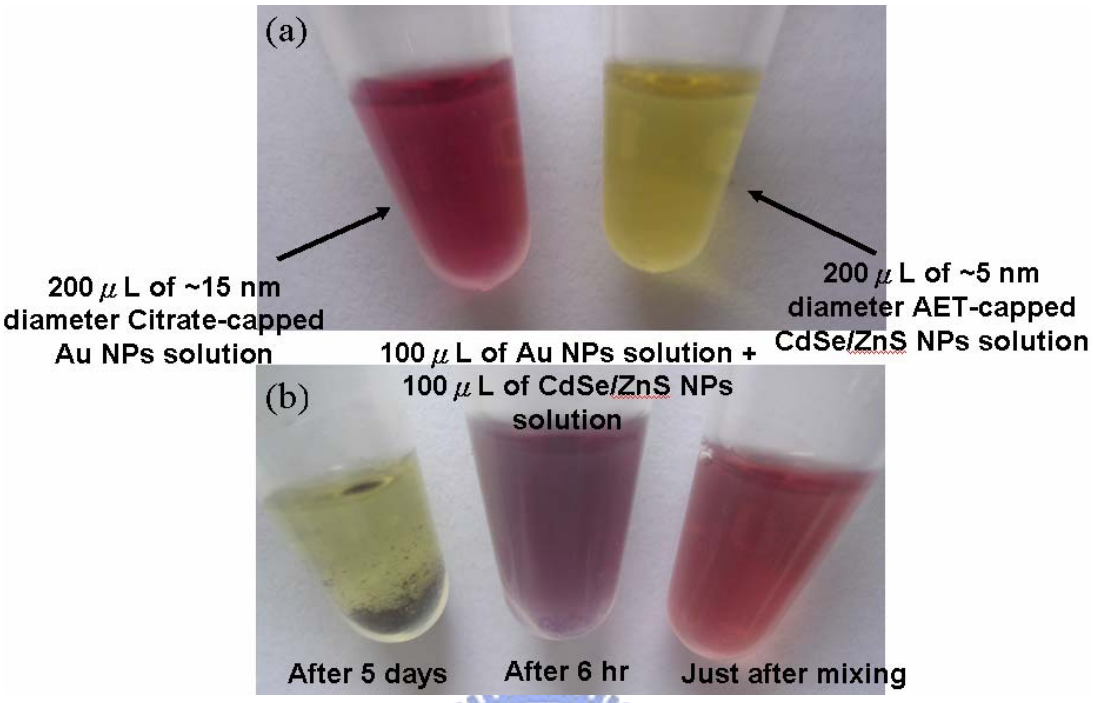
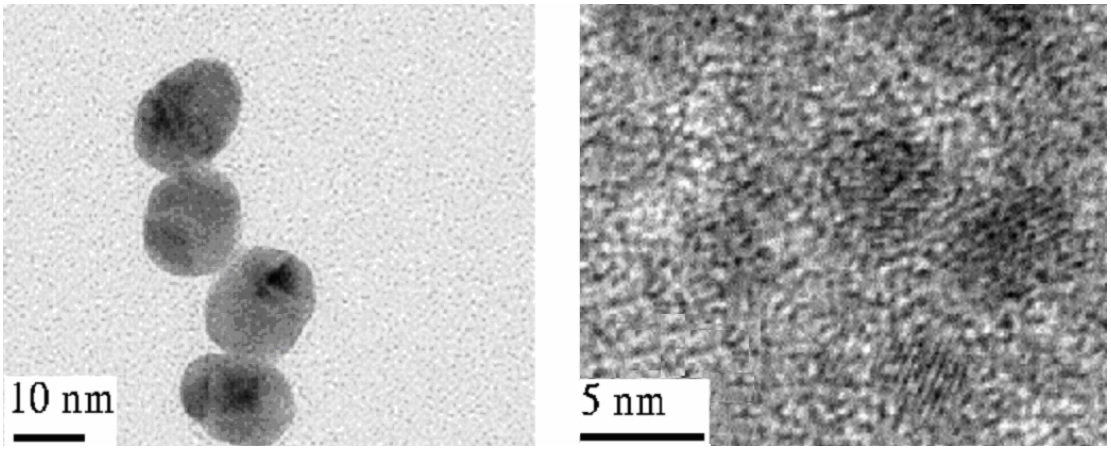
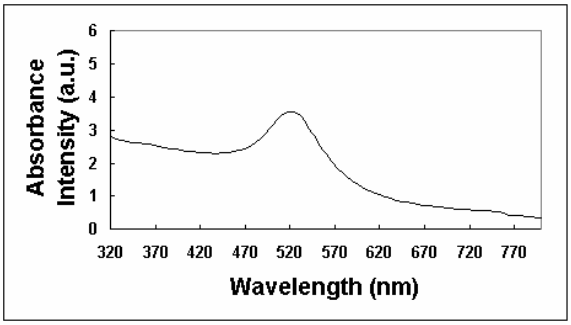


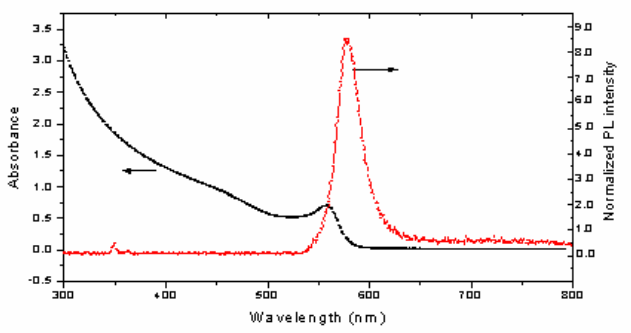
Figure 2.2. (a) The close photographs of 100 μL of approximately 15 nm diameter Au NPs solution + 100 μL DI water (left) and 100 μL of approximately 5 nm diameter AET-CdSe/ZnS NPs solution + 100 μL DI water (right). The Au NPs solution was in deep red while the AET-modified CdSe/ZnS NPs solution was in yellow. (b) The close photographs of the mixture of 100 μL Au NPs solution and 100 μL AET-modified CdSe/ZnS NPs solution just after mixing (right), the mixture after standing 6 hrs (middle) in room temperature, and the mixture after standing 5 days in room temperature (left). As we can see, the color of mixture just after mixing was like that of Au NPs solution. However, after 6 hrs, it became dark purplish red. After 5 days, there was obvious precipitate at the bottom and the supernatant became pale yellow.



(a)

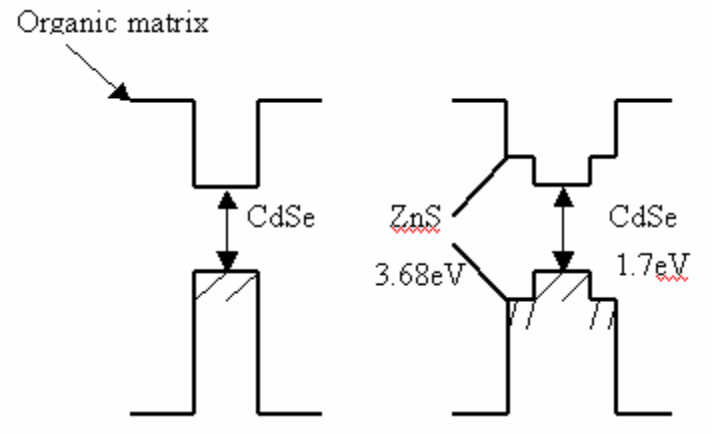


(b)

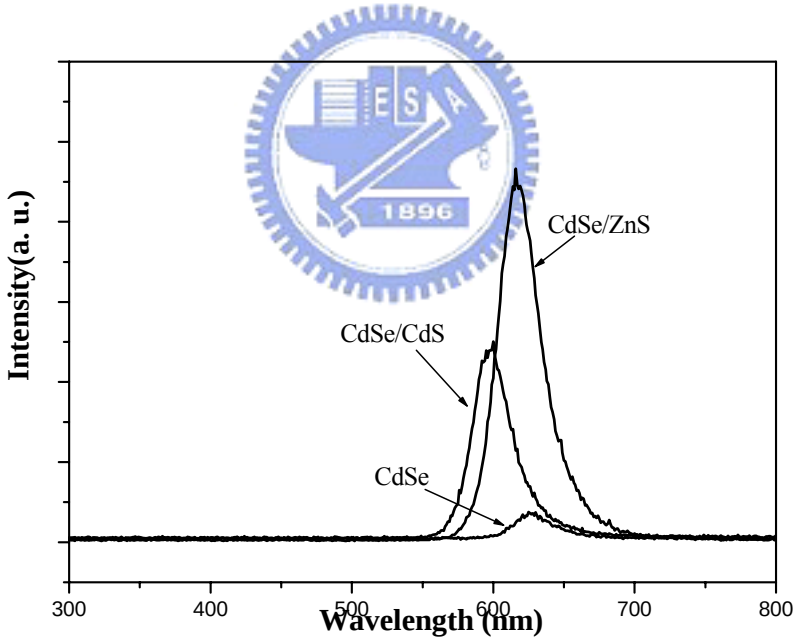


(c)

Figure 2.3. (a) The TEM image of Citrate-capped approximately 15 nm diameter Au NPs and the TEM image of AET-capped approximately 5 nm diameter CdSe/ZnS NPs. (b) The UV-visible spectrum of Au NPs solution. (c) The UV-visible and PL intensity spectrum of MSA-CdSe/ZnS or AET-CdSe/ZnS NPs solution.



(a)



(b)

Figure 2.4 (a) The band gap and surface structure diagram of CdSe/ZnS NP. (b) The PL intensity spectrum of different kind of surface capping method of CdSe NP.

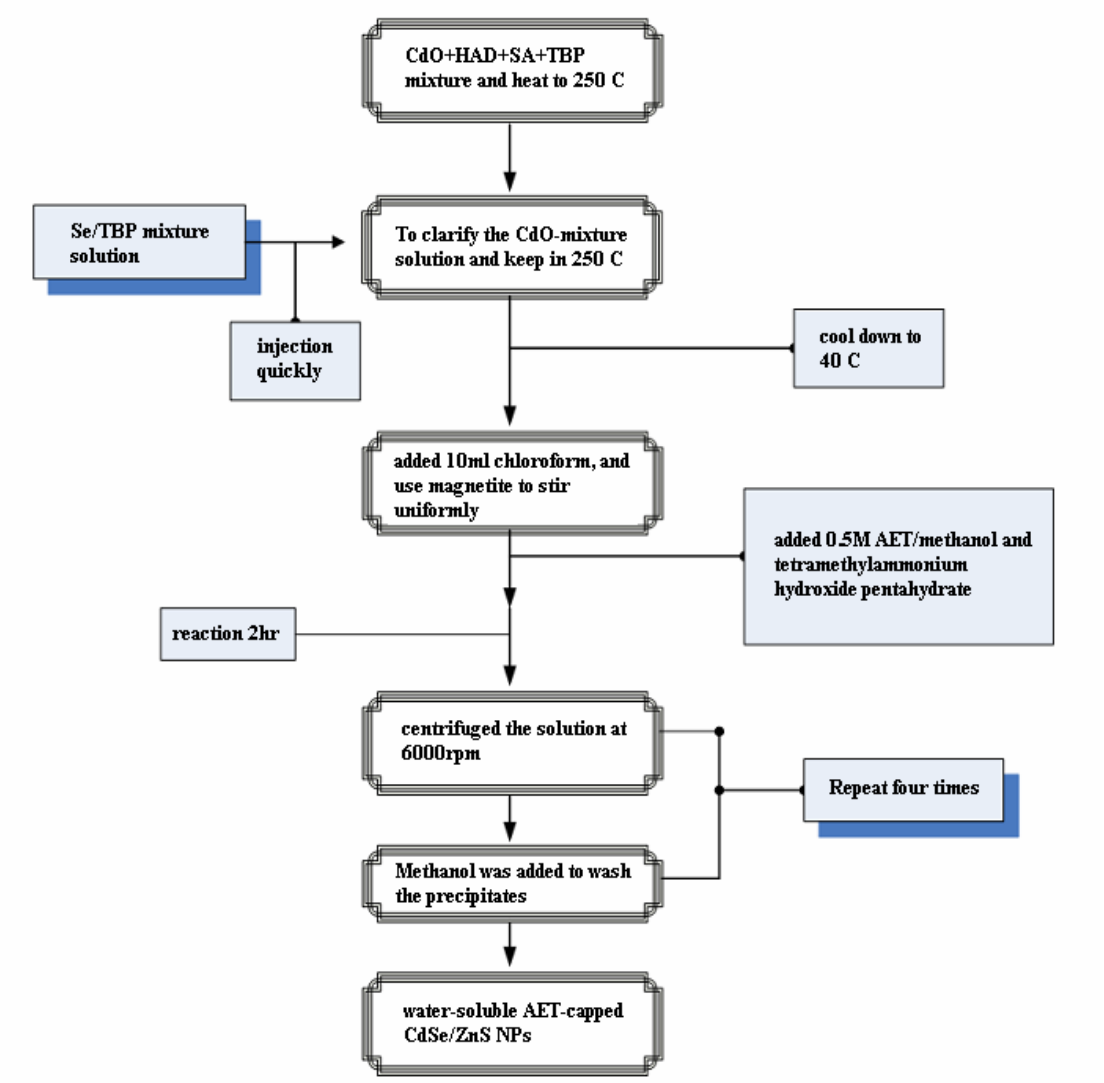
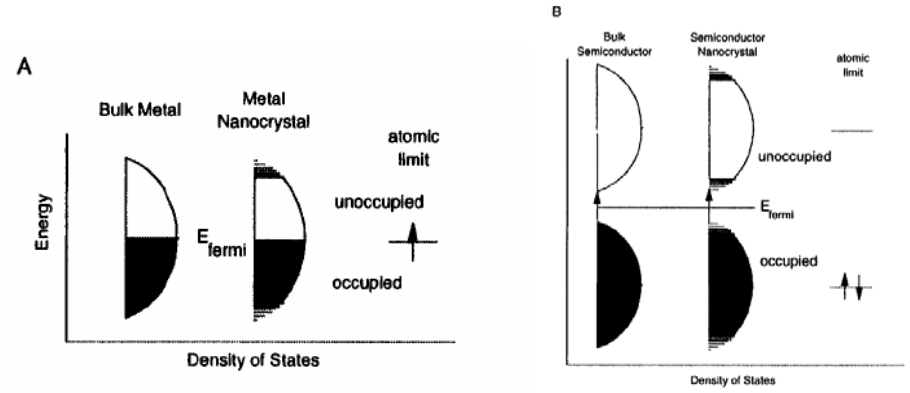
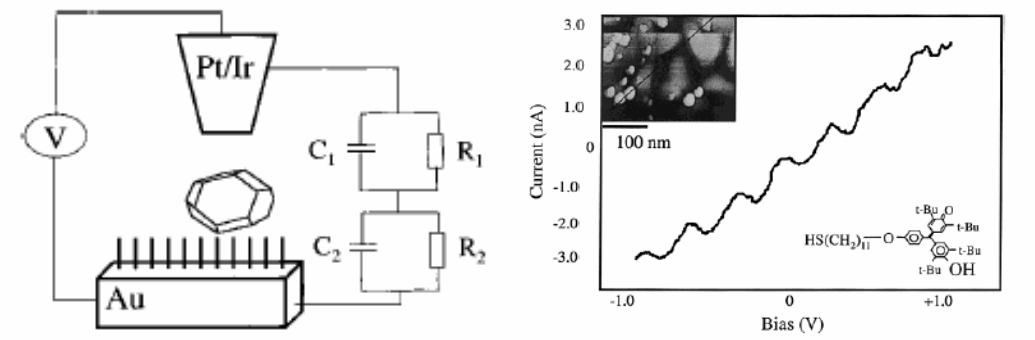


Figure 2.5 The flow diagram for preparing the AET-capped CdSe/ZnS QDs solution.



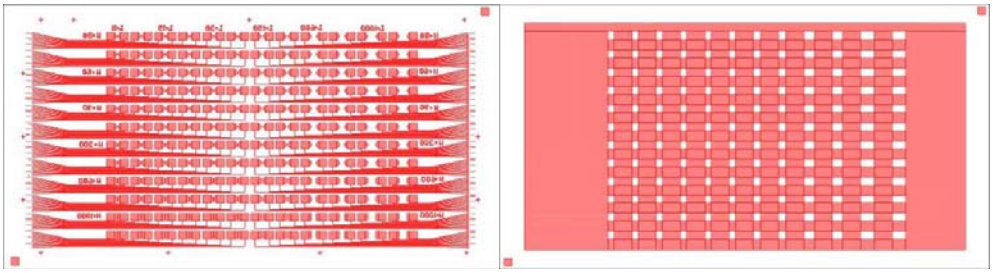
(b)

Figure 2.6 Density of states in metal (A) and semiconductor (B) nanocrystals. In each case, the density of states is discrete at the band edges. The Fermi level is in the center of a band in a metal, and so *kT* will exceed the level spacing even at low temperature and small size. In semiconductor, the Fermi level lies between two bands, so that there is large level spacing even at large size. The HOMO-LUMO gap increases as the semiconductor nanocrystals of smaller size (bellow 10 nm) [11].



(a) (b)

Figure 2.7 (a) Illustration of a STM tip-single metal NP-insulator coated gold substrate double tunnel junction and corresponding equivalent circuit. (b) Current versus voltage for a single galvinol-coated Au NP acquired in aqueous solution at pH 5. Insect shows an STM image of the sample. Tip was coated with Apiezon wax and gold substrate was coated with hexanethiol [8].



(a) (b)

Figure 2.8 (a) The first mask of the nanodevice, and it define the aluminum pattern. (b) The second mask of the nanodevice, and it define the lift-off region.

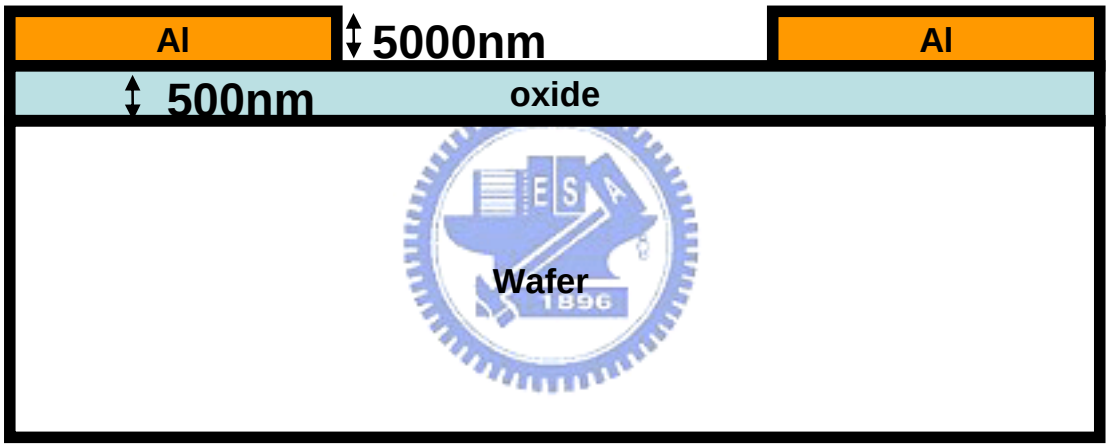
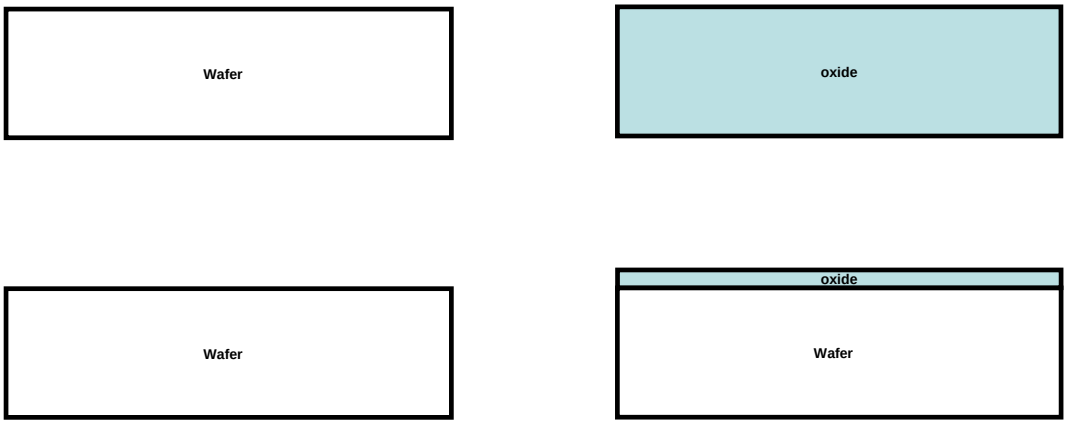


Figure 2.9 The cross-section view of the electrodes



(a) (b)

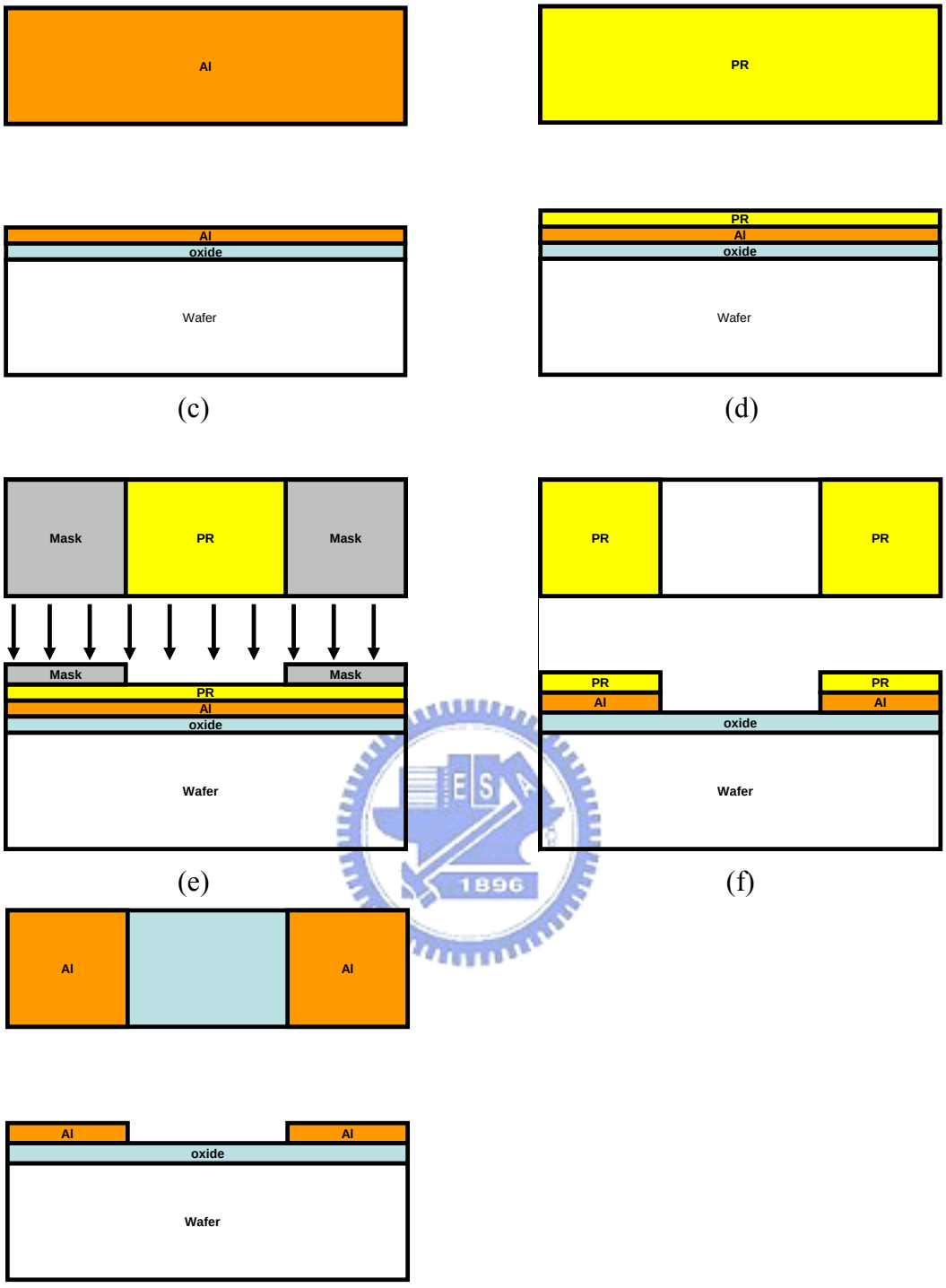
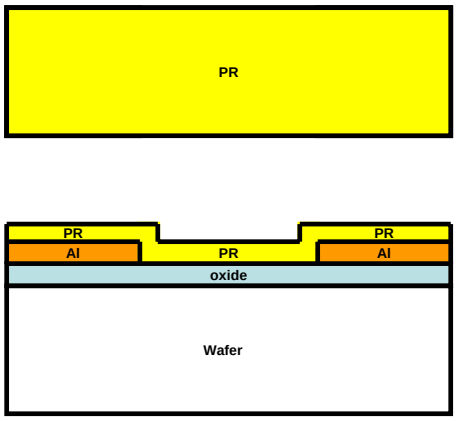
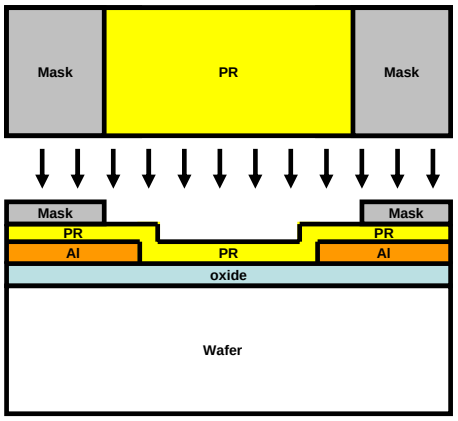


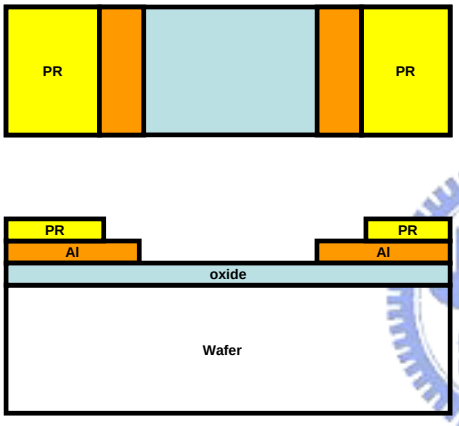
Figure 2.10 The process flow of the nanodevice (top-view and cross-section view) (a) The wafer was cleaned before the electrode process. (b) The oxide layer formed by thermal oxidization process. (c) The aluminum layer was constructed by thermal coating process. (d) The aluminum surface coated with photoresist. (e) The sample is exposed to define the electrode pattern. (f) Etch the extra aluminum and remain the desire region protected by the photoresist. (g) Remove the photoresist, and the electrodes formed.


PR
PR
PR
Al
PR
Al
oxide
Wafer

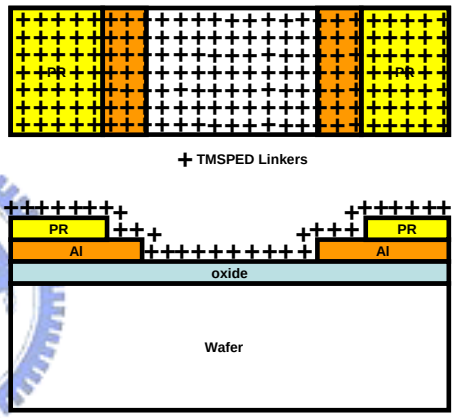
(h)


Mask
PR
Mask
Mask
Mask
PR
PR
PR
Al
PR
Al
oxide
Wafer

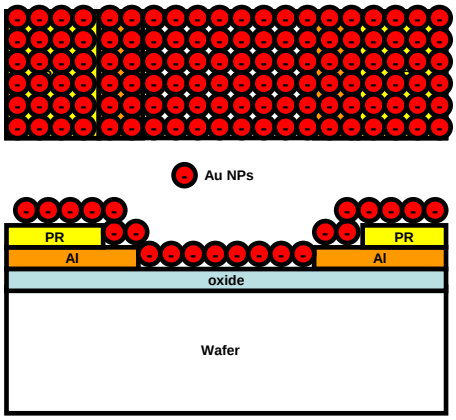
(i)


PR
PR
PR
Al
PR
Al
oxide
Wafer

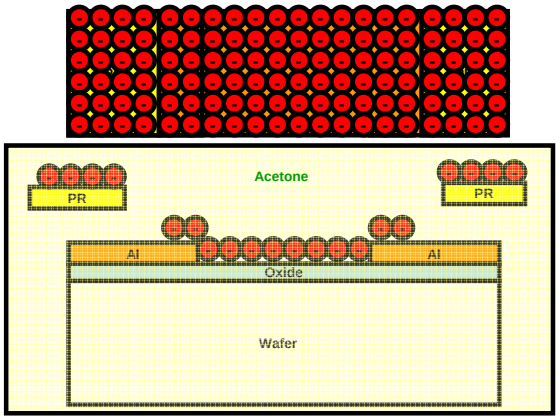
(j)


TMSPED Linkers
PR
Al
PR
Al
oxide
Wafer

(k)


Au NPs
PR
Al
PR
Al
oxide
Wafer

(l)


Acetone
PR
PR
Al
Al
Oxide
Wafer

(m)

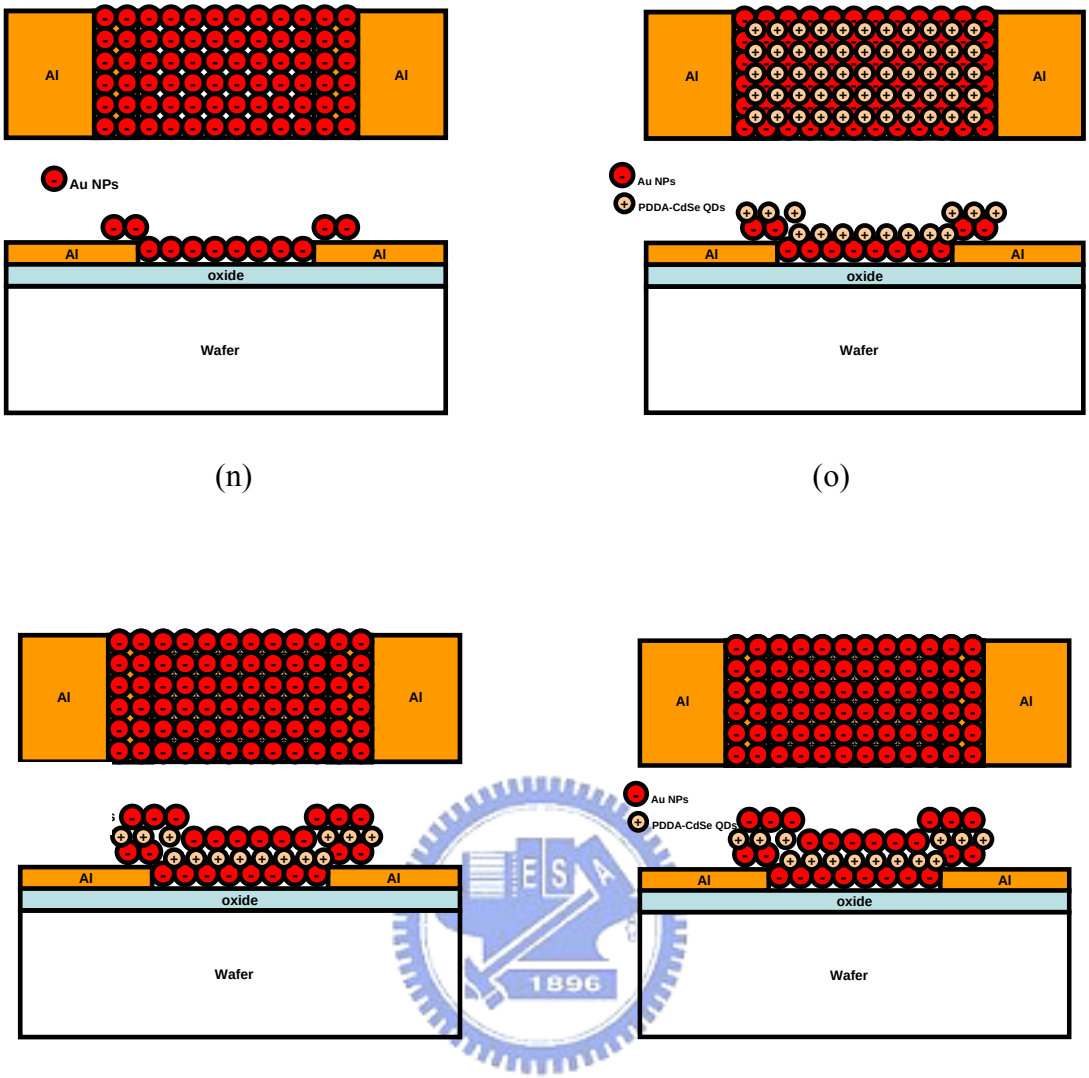
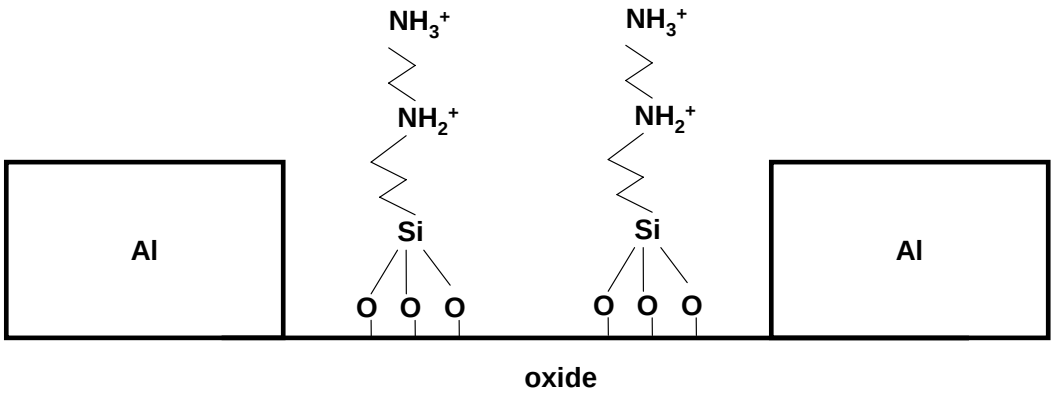
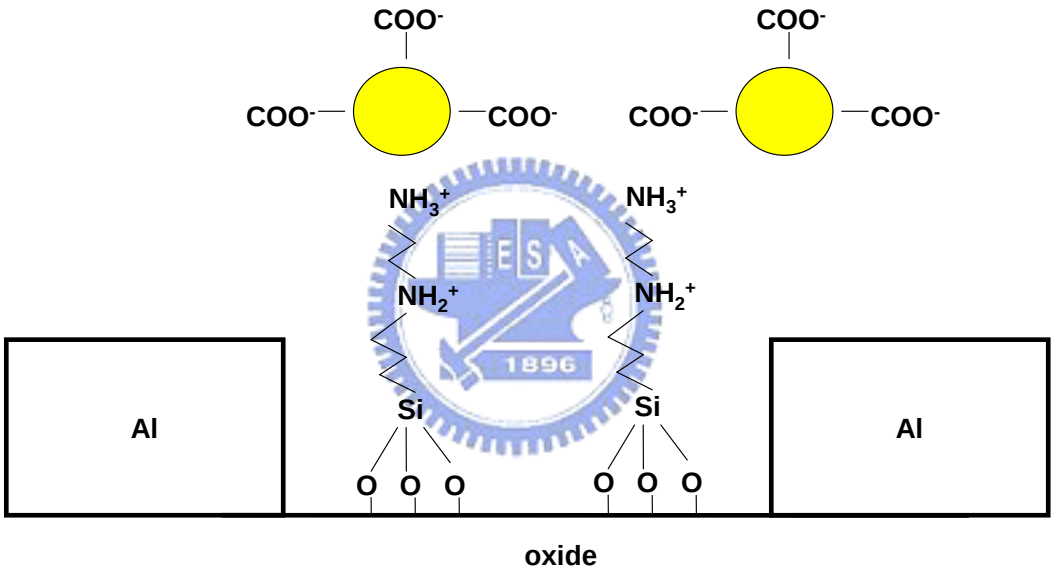


Figure 2.10 The process flow of Nanodevices (top-view and cross-section view) (h) The wafer was coated with the photoresist. (i) The electrode sample was exposed to define the lift-off region. (j) The electrode sample was put into the developer. (k) TMSPED linkers were coated on the electrode surface. (l) The negative-charged Au NPs were coated on the surface. (m) The lift-off process was executed by immersing the sample in the acetone. (n) The unexpected NPs were removed. The desire pattern remained. (o)(p)(q) The layer-by-layer technology was repeated until the desire nanostructure was attained.


NH3+
NH2+
Si
O O O
NH3+
NH2+
Si
O O O
Al
Al
oxide

(a)


COO-
COO-
COO-
COO-
COO-
COO-
NH3+
NH2+
Si
O O O
NH3+
NH2+
Si
O O O
Al
Al
oxide

(b)

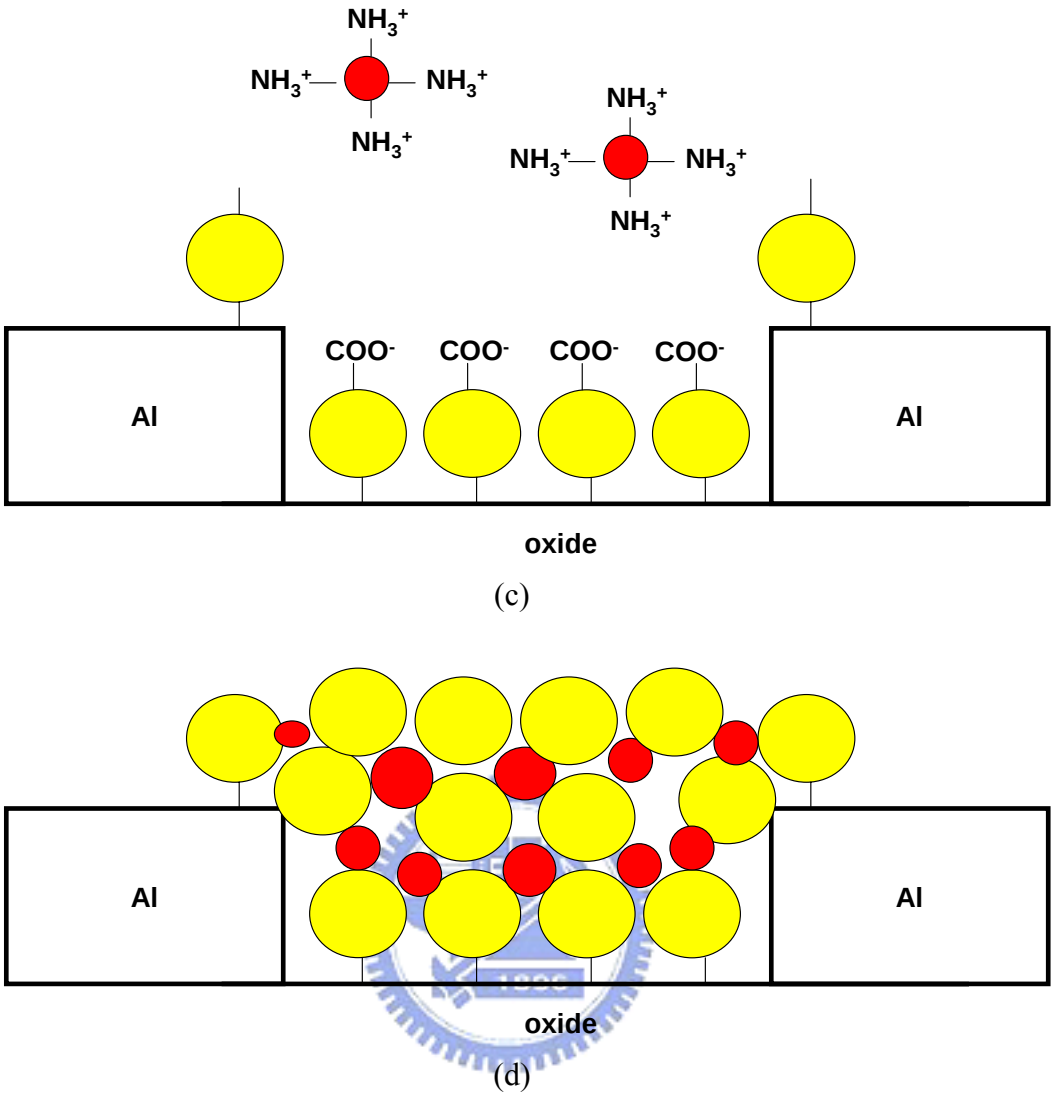
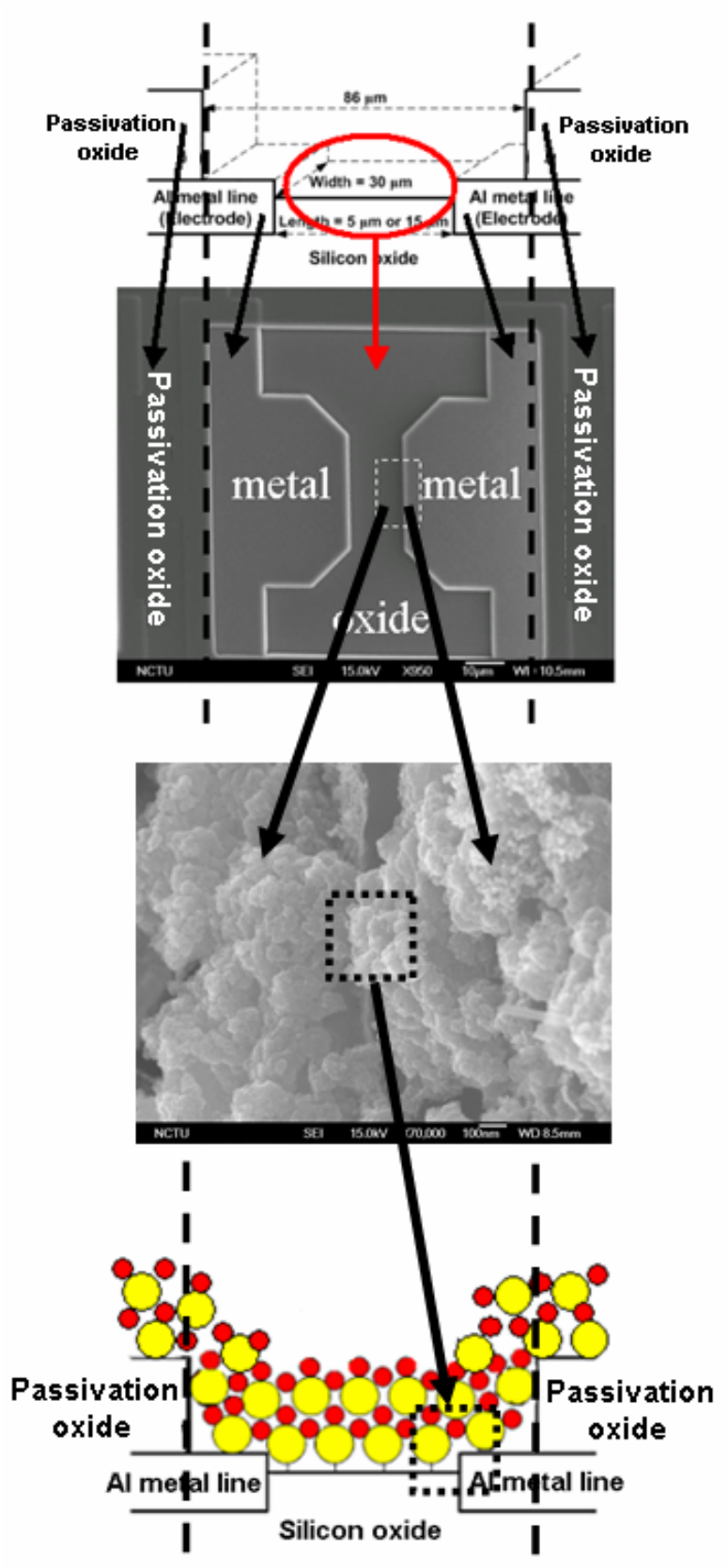


Figure 2.14 The fabrication process of the photo-sensing nanodevice by coulombic force system after lift-off process. (a) The modification of TMSPED on the silicon oxide surface and the protonation of amino ($-NH_3^+$) groups, (b) The assembly of ~ 15 nm diameter Au NPs on silicon oxide substrate by ionic interaction, (d) The assembly of ~ 5 nm diameter AET-CdSe/ZnS NPs on the silicon oxide substrate by ionic interaction, and (e) The formation of the photo-sensing nanodevice structures after repeated assembly process. (Not to scale)


86 μm
Passivation oxide
Passivation oxide
Width = 30 μm
Al metal line (Electrode)
Al metal line (Electrode)
Silicon oxide
Passivation oxide
Passivation oxide
metal
metal
oxide
NCTU
Passivation oxide
Passivation oxide
Al metal line
Al metal line
Silicon oxide

(a)

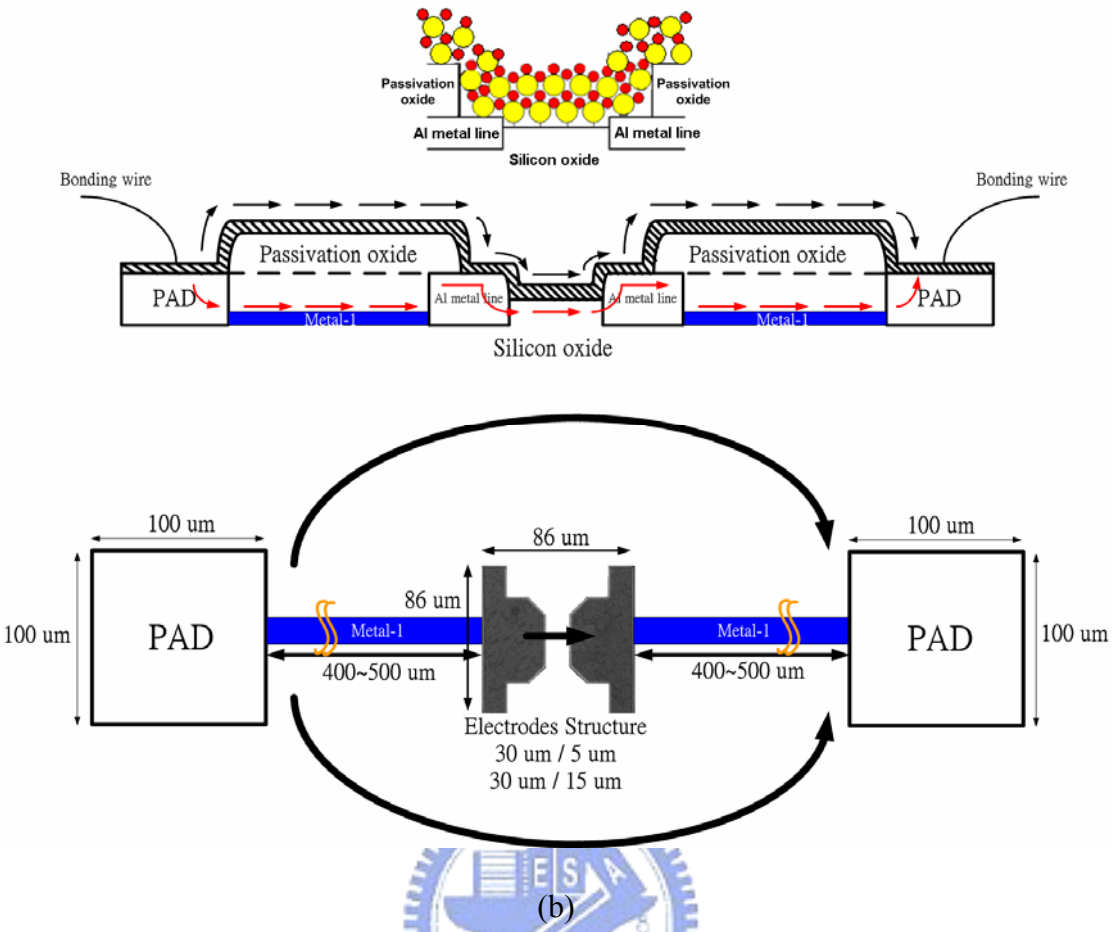


Figure 2.11 (a) The cross section figure of the electrodes structure corresponds to SEM image of the nanodevice-modified silicon chip. (b) The current flow trend of the nanodevice structure, and the electrodes dominated the source of the generated current. In the worse case, the whole chip area is considered, not the area of the electrodes. (The twill line means the thin film structure composed of NPs and QDs.).

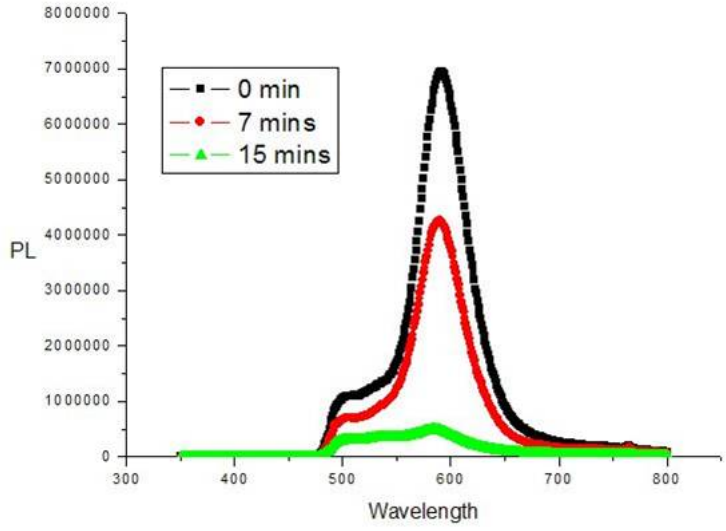
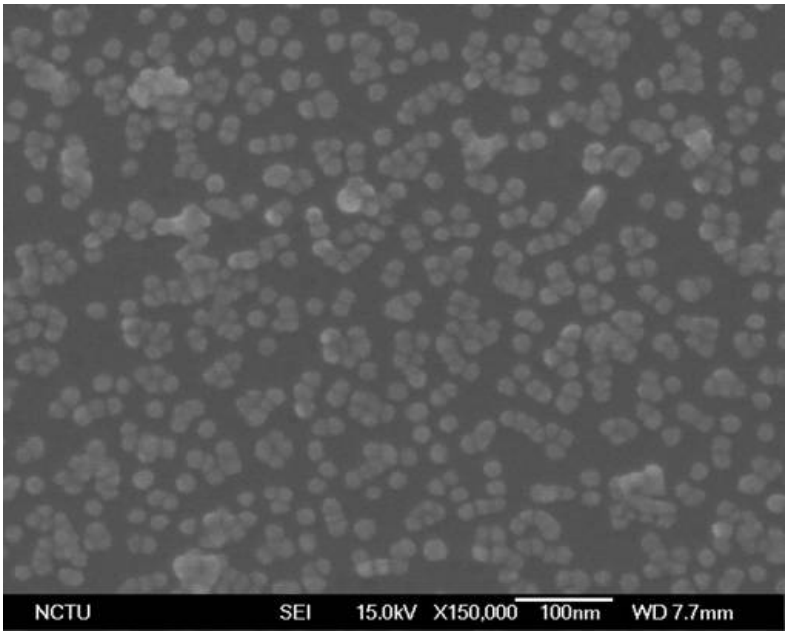
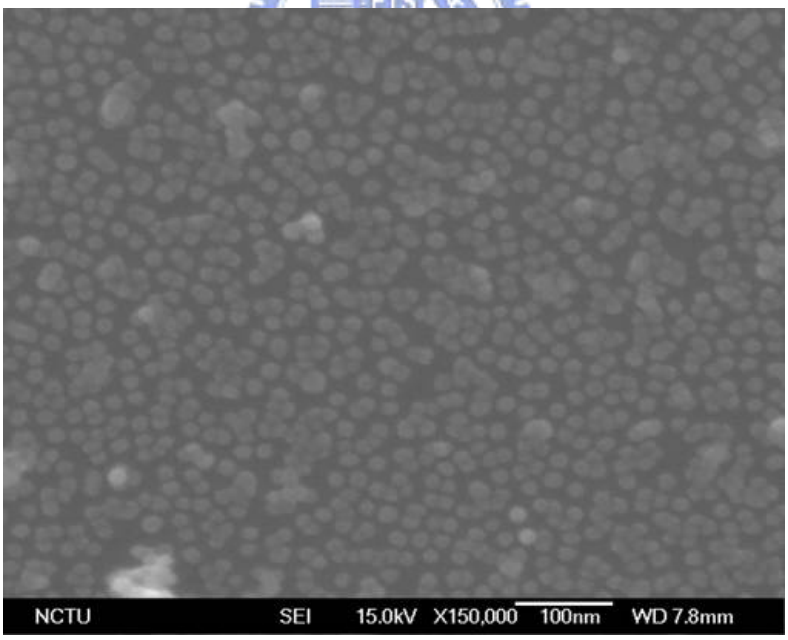


Figure 2.12 The 4-layer nanostructure immersed in acetone during different period.

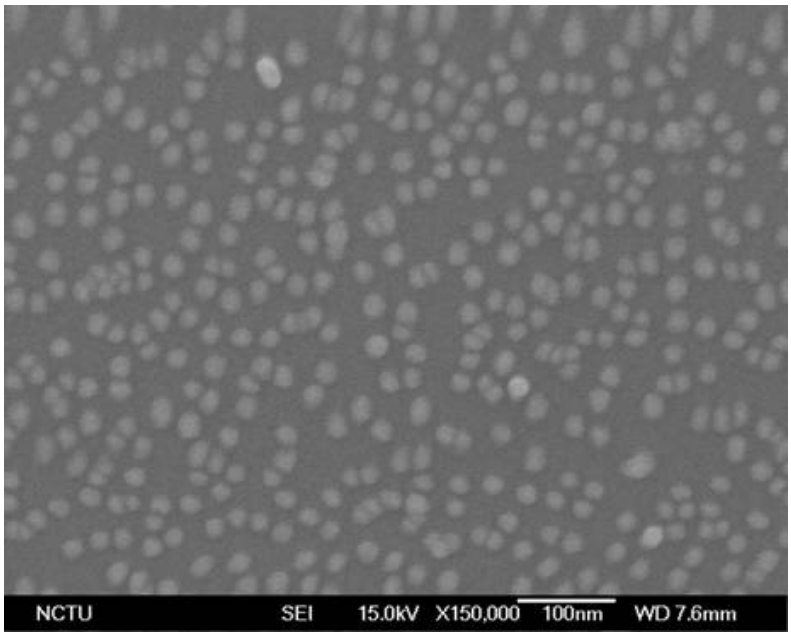


(a)

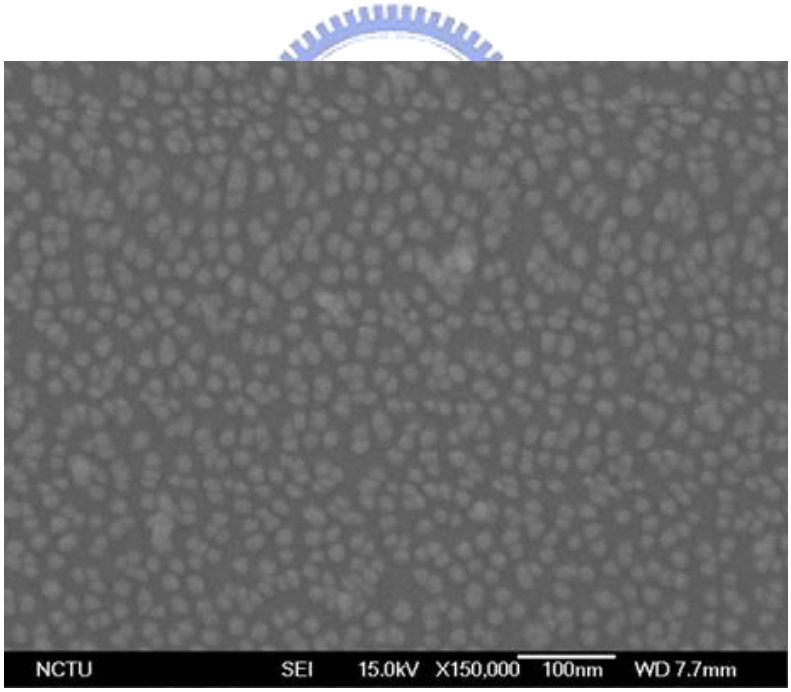


(b)

Figure 2.15 The reaction time effect on the 2-layer nanostructure (SEM view), (a) nanostructure with 3-hour-reaction-time per layer, (b) nanostructure with 24-hour-reaction-time per layer



(a)



(b)

Figure 2.16 The temperature effect on 2-layer nanostructure (SEM view), (a) the nanostructure constructed at room temperature, (b) the nanostructure constructed at 4^{o}C environment.

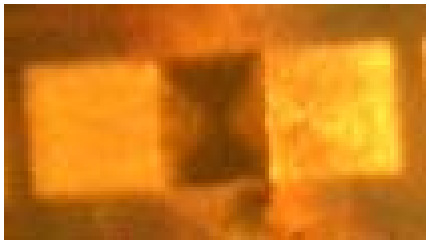


Figure 2.17 The nanodevice with lift-off process, the black part is the place that Au NPs and CdSe deposit on the electrode surface.

CHAPTER 3
EXPERIMENTAL RESULTS AND DISCUSSIONS

In this chapter, experimental results will be showed and discussed. First, the measurement environment is introduced in the section 3.1. Secondly, the nanostructure physical characteristics would be demonstrated, for example, SEM view and absorption / emission Spectra. Thirdly, different layer Au / CdSe (AET-CdSe and PDDA-CdSe) Nanodevice would be measured. Then, the results would be showed and discussed in section 3.3. Next, Nanodevice solar cell efficiency would be estimated in section 3.5. Finally, using HSPICE software to construct the nanodevice model was executed in section 3.6. The simulation result fits the nanodevice measurement results, and it also could explain the electrical characteristics of the different dimension nanodevice.

3.1 The Environment Setup for Measurement

After fabrication, the silicon oxide substrate was observed and evaluated by using scanning electron microscopy (SEM) images at each stage of the procedure. The SEM was performed with JSM-6500F high-resolution scanning microscope. In addition to surface structure observation, the photo-sensing properties of the nanodevice were also verified by using daylight lamp and laser diode as illumination light source. The environment setup for I-V characteristics measurement was shown in Figure 4.1. The laser diode driver is PicoQuant POL 800D and the 375 nm laser

diodes are PicoQuant LDH-P-C375. The I-V measurement instrument is HP 4156.

We also measured the UV-visible and Photoluminescence (PL) spectra to confirm the specific optical characteristics of the nanostructure. The UV-visible absorbance spectrum analysis was performed with Hitachi-U-3010 Spectrophotometer. The detecting wavelength was in the range of 190 nm to 1000 nm, and according the transmitted of sample, its absorption spectra is monitored by Beer's Law. The typical experimental setup is shown in Figure 3.2. A beam of light from a visible and/or UV light source (red colored) is separated into its component wavelengths by a prism or diffraction grating. Each monochromatic (single wavelength) beam in turn is split into two equal intensity beams by a half-mirrored device. One beam, the sample beam (colored magenta), passes through a small transparent container (cuvette) containing a solution of the compound being studied in a transparent solvent. The other beam, the reference (colored blue), passes through an identical cuvette containing only the solvent. The intensities of these light beams are then measured by electronic detectors and compared. The intensity of the reference beam, which should have suffered little or no light absorption, is defined as I_0. The intensity of the sample beam is defined as I. Over a short period of time, the spectrometer automatically scans all the component wavelengths in the manner described. The ultraviolet (UV) region scanned is normally from 200 to 400 nm, and the visible portion is from 400 to 800 nm. If the sample compound does not absorb light of a given wavelength, $I = I_0$. However, if the sample compound absorbs light then I is less than I_0, and this difference may be plotted on a graph versus wavelength. Absorption may be presented as transmittance ($T = I/I_0$) or absorbance ($A = \log I_0/I$). If no absorption has occurred, T = 1.0 and A = 0. Most spectrometers display absorbance on the vertical axis, and the commonly observed range is from 0 (100% transmittance) to 2 (1% transmittance).

The PL spectrometer analysis is performed with Jobin Yvon Instrument S. A. Inc.

Spectrometer. The scanning range is from 200 nm to 1000 nm. The typical experimental setup for PL intensity spectrum measurement is shown in Figure 3.3. When light of sufficient energy is incident on a material, photons are absorbed and excite the electrons from ground state. If radiative relaxation occurs, the emitted light is called photoluminescence (PL). This light can be collected and analyzed to yield a wealth of information about the photo-excitation nanostructure. In this experiment, we used laser source with different wavelengths to photo-activate the nanostructures. Subsequently, the emitted light was passing through a filter lens that can filter out the wavelengths < 500 nm, then analyzed by spectrometer and got into a photo-detector. Eventually, the PL signal data are recorded into computer.

3.2 SEM and Optical Absorption / Emission Spectra

The SEM images of the surface of SiO_2/Si wafer fragments after repeated assembly process are shown in Figure 4.7 (Au / CdSe/ZnS nanostructure). As we can see in the images, the structure becomes more and more compact when increases the number of layers step by step. Besides, for Au / CdSe nanostructure, after the multi-layered structure was formed, typically more than 3 layers, the gold color shining can be easily observed by naked eye. First, the sample (electrode) is modified by N-[3-(trimethoxysilyl)propyl]-ethylene diamine (TMSPED), which provides positive-charged amino ($-NH_3^+$) groups to attract negative ($-COO^-$) charged Au. Second, the modified CdSe QDs that have positive-charged amino groups on the particle surface are assembled on Au NPs. Theoretically, the assembly process can be repeated for several times to form multi-layered nanostructure of CdSe QDs and Au NPs. Thirdly, measurement of nanodevice and then illumination the silicon chip by 0.204mW / cm^2 daylight lamp and 0.5mW / cm^2 laser diodes (375 nm) under

normal room condition.

Furthermore, in order to prove that the closely packed nanostructure has superior optical properties, we used quartz glass to simulate the silicon oxide substrate and observed the variation of UV-visible and Photoluminescence (PL) intensity spectra at different layer nanostructure. From the absorption spectrum, we can see the peak of absorbance rises when the number of layers increases, as shown in Figure 3.5. Besides, the nanostructure retains the optical characteristics of CdSe QDs when they are bound to each other, which can be verified by identifying the characteristic absorbance peaks of Au NPs (~520 nm) and CdSe QDs (~580 nm) in the spectrum. However, in some cases, we observed the peaks of Au NPs (~520 nm) and CdSe QDs (~580 nm) are so close that they merge to form a board band in the spectrum for Au / CdSe nanostructure as shown in Figure 3.5. By comparing the UV-visible spectrum to the sizing curve reported by Peng and co-workers [26], we obtained that the diameter of CdSe QDs is about 4 nm ~ 5 nm, which can also be proved by TEM images.

The PL intensity spectrum of multi-layered nanostructure on quartz glass was shown in Figure 3.6. There are some important characteristics: first, for the Au / CdSe multi-layered structures, the PL intensity will also increase when the number of layers increases when we used 375 nm wavelength for optical excitation, as shown in Figure 3.6. It means that the nanostructure becomes more compact and has fewer defects on the particle surface. During the dip-and-wash procedure, the instable bond between the NPs and QDs will cause the existence of defect. So the probability of defect will be reduced when the number of layers increases. Secondly, as shown in Figure 3.6, there is no absorption for Au NPs under optical excitation; therefore, there is no PL intensity with only a layer of Au NPs on quartz glass (Black Line). The PL intensity in 3-layer (5-layer) nanostructure is smaller than 2-layer (4-layer) nanostructure can also be proved. The Au NPs, which have no absorbance, block the incident light for CdSe

QDs to be photo-activated in the 3-layer (5-layer) structure. Thirdly, we observed the PL intensity in 4-layer nanostructure become larger than 2-layer nanostructure. Specifically, they have the same structure that the CdSe QDs were on the top-layer. This result means that multi-layers constitute a more compact and fewer defects structure. For the same reason, the 8-layer and 12-layer nanostructures show higher PL intensity than the 4-layer nanostructure. Nevertheless, although the ionic assembly using this dip-and-wash process can repeat as many times as we design to, the PL intensity increment will eventually be saturated.

3.3 Au / CdSe Nanodevice

In this section, I-V characteristics of multi-layer nanodevice structure were measured. The measurement environment was introduced in the section 3.1. First, two kinds of the QDs, AET-CdSe QDs and PDDA-CdSe QDs, were compared with the power conservation efficiency. The electrode sets we used, 30um / 5um, 30um / 15um, 30um / 30um, 60um / 5 um, 60um / 15 um, 60um / 30 um, 90um / 5 um, 90um / 15 um and 90um / 30 um (width / length). After the fabrication process described in Section 2.5, the I-V measurement was performed by applying voltage biases to the electrodes and measuring the current flowing through the nanodevice while in dark or under 0.16mW / cm^2 daylight lamp illumination. The result of the nanodevice is shown as Figure 3.7. It is a resistive device in dark. After illumination, the photocurrent is generated. It is also linear but a y-axis direction shift. The shift quantity is the photocurrent.

First, 4-layered AET-CdSe nanodevices were measured. We found that the photocurrent increased as the width increased. Therefore, the PVD (photocurrent volume density) also increased with the width increased. However, the photocurrent

decreased as the length increased. Thus, the PVD also decreased with the length increased. Due to the same number of layer, the photocurrent gets the same trend with the PVD (the same volume).

The most important specification in the nanodevice is the efficiency. This remarks interesting because we care about how much power the nanodevice can generate, not the photocurrent. As the Figure 3.9 shown, the maximum efficiency of the 4-layered AET-CdSe nanodevice is 0.237%, and its device size is 60um / 5um (width /length). In conclusion, the efficiency is a constant value at the same width . Thus, we will explain the reason in the next section.

Then, the 4-layered PDDA-CdSe nanodevices were fabricated. The measurement result is divided to several parts (Figure 3.10(a)(b)(c) and Figure 3.11), the photocurrent, open-circuit voltage, PVD (Photocurrent Volume Density), power volume density, efficiency comparison. We obtain the same result from the PDDA-CdSe nanodevice. The photocurrent increases as the width increase. The same phenomenon also happens in PVD and power volume density. However, they decrease as the length increase. Meanwhile, the efficiency drops when the device length increases. However, the efficiency is still a constant value when the device width varies. Then, as the Figure 3.11 shown, we found the efficiency of the 4-layered PDDA-CdSe nanodevices is better than the 4-layered AET-CdSe nanodevices. Therefore, 8-layered, 12-layered and 24-layered nanodevices are all fabricated by the PDDA-CdSe quantum dots.

As the Figure 3.13(a) and Figure 3.14 shown, the nanodevice performance was obtained. Increasing the number of layer, it benefits the efficiency performance. However, it start to saturate when the number of layer was eight. In other hand, the efficiency was still a constant as the device width varied. This phenomenon can be simulated by HSPICE. We will discuss it in the next section. Figure 3.13(b) shows the

PVD result. We found that 8-layered nanodevices perform best in this work. The same phenomenon can also observed in the power volume density.

In order to compare with previous work, the nanodevices were illuminated by 2.5mW/cm^2 375 nm laser diode and the 0.16mw/cm^2 daylight lamp. The measurement result is shown in the Figure 3.15. Under the 375 nm laser illumination, the efficiency is better than former case. It is because the PDDA-CdSe QDs absorb UV light better.

By altering the width of the device, which is the same as paralleled connected the batteries, the stronger photocurrent can be obtained. In addition, the open-loop voltage does not suffer from significant variation. Since the efficiency of the device is the same under the constraint that the width is fixed, the device with larger area can get more power.

On the other hand, by altering the length of the device, the internal impedance of the device increases as the length increases; consequently, the generated photocurrent is hard to flow out, which is the reason why the photocurrent decreases as the length of the device increases.

At last, by altering the number of layers of the device, the photocurrent flowing on top of the upper layer gets harder to flow to the bottom layer as the number of layers increases, which leads to the fact that as the number of layers increases, the photocurrent will decrease correspondingly. Moreover, the impact of blocking effect , which cause the light that is obtained by the nanoparticle on the bottom layer being blocked by the upper layer, must be taken into consideration. As a result, the photocurrent generated by each nanoparticle is not the same and cannot be observed in device model simulation. This is why the error exists between the device model and the device.

3.4 Au / CdSe Nanodevice Solar Cell Efficiency Estimation and Model Construction

The nanodevice solar cell efficiency on the base of the traditional p-n junction solar cell as the Figure 3.16(a) shown was estimated. Figure 3.16(b) shows the solar cell I-V curve. According to the I-V curve characteristics, assume a resistive device is connected to the solar cell. A operation point is obtained. The parameter, fill factor, is defined.

$$Fill\_Factor = \frac{V_m \times I_m}{V_{OC} \times I_{SC}}$$

Voc is the open circuit voltage of the solar cell. Isc is the short current of the solar cell. Vm and Im is the voltage and the current when the product of the voltage and current (power) is maximum. Then, the efficiency can be defined as

$$Efficiency = \frac{V_{oc} \times I_{sc}}{P_{in}} \times (Fill\_Factor)$$

where Pin is the power of the incident light source.

In this work, the I-V curve of the nanodevice is shown as the Figure 3.17. We can define the formula of the I-V curve and estimate its maximum power.

$$I = \frac{I_{SC}}{V_{OC}} V + I_{SC}$$

$$Power = V \times I = V \times \left(\frac{I_{SC}}{V_{OC}} V + I_{SC} \right)$$

$$\frac{\partial Power}{\partial V} = \frac{2I_{SC}}{V_{OC}} V + I_{SC} = 0$$

Therefore, When $V=V_{oc}/2$, $I=I_{sc}/2$, we have the maximum power of the solar cell , $0.25V_{oc}I_{sc.}$ Thus,

$$Fill\_Factor = \frac{V_m \times I_m}{V_{OC} \times I_{SC}} = \frac{\frac{V_{OC}}{2} \times \frac{I_{SC}}{2}}{V_{OC} \times I_{SC}} = \frac{1}{4}$$

,and the efficiency of the nanodevice solar cell can be defined.

In turns, due to the p-n junction solar cell equivalent circuit, the Au / CdSe nanodevice model can be constructed. An Au NP and a CdSe QD can be considered as a micro p-n junction solar cell or nano-schottky diode as the Figure 3.17 shown. The conventional solar cell equivalent model is illustrated in Figure 3.16(c) where R_s is a small seris resistor and R_p is a very large parallel resistor. Owing to the equivalent circuit shown in Figure 3.16(c), the unit cell of the nanodevice can be constructed as the Figure 3.17(a) shown. It is a symteric structure. R_{s1} and R_{s2} are small seris resistors and R_{p1} and R_{p2} are very large parallel resistors. I_1 and I_2 are the photocurrent after illumination.

The 1-dimension nanodevice model is shown in the Figure 3.18. For HSPICE simulation, Metal-Insulator-Semiconductor diode model was employed. Next, the 2-dimension nanodevice model is constructed. Figure 3.19(a) illustrates the ideal 2-dimension structure of the nanodevice. On the basis of this structure, the 2-D nanodevice model can be built as the Figure 3.19(b) shown.

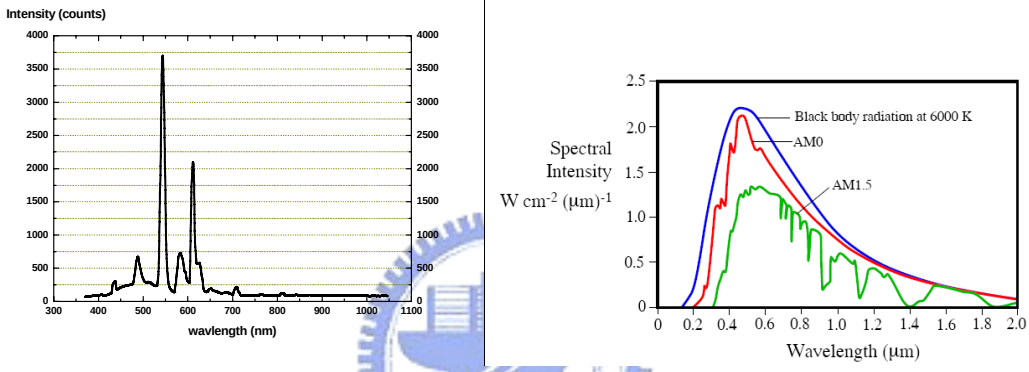
Finally, 3-dimension nanodevice model is concerned. It is more complicated than 1-D and 2-D model. Figure 3.20 shows the ideal 3-dimension nanodevice structure. The unit cells connect two of the 2-D nanodevice model to form a 3-D nanodevice model. The simulation condition illustrate in the Figure 3.21. The photocurrent

increases as the width increases. It also fits the nanodevice measurement results. First, for HSPICE simulation, Metal-Insulator-Semiconductor diode model was employed. X-dimension unit cell : Rs=0.153MΩ, Rp=48.178MΩ, I=2.1nA; Y-dimension unit cell : Rs=0.918MΩ, Rp=289MΩ, I=2.1nA,.Z-dimension unit cell: Rs=6120Ω, Rp=1.95M, I=2.1nA. A 30um / 5um (width / length) 4-layered nanodevice is utilized as a unit cell. Figure 3.22 shows the width effect. The photocurrent increases linearly as the width increases. (fixed length=5um, fixed the number of layer=4). The open circuit voltage is a constant value as the Figure 3.23 shown. The efficiency is a constant value when the device width varies.as the Figure 3.24 shown. Then, length effect is discussed. The photocurrent decreases as the length increases. (fixed width=30um, fixed number of layer=4) as the Figure 3.25 shown. The open circuit voltage saturates as the length increases (Figure 3.26). The efficiency decreases as the length increases. Last, let us consider the layer effect. As the Figure 3.27 show, the photocurrent saturates when the number of the layer larger than eight. (fixed width=30um, fixed length=5um). The open circuit voltage decreases linearly, and then settles to a constant value. The efficiency starts to saturate when the number of the layer eight. According to the simulation result, the efficiency does not increase obviously if the number of the layer is more than 26.

In summary, increasing the width will benefit the performance of the nanodevice. Therefore, the linear fit of the nanodevice efficiency is executed. According to the simulation and measurement results, the photocurrent increases linearly as the width increases. Thus, the best case of the nanodevice, 26-layered nanodevice, is chosed to do the linear approximation. As a result, the 38.1% efficiency solar cell can be fabricated. The 26-layered nanodevice with 65nm in length can reach this purpose. Moreover, when the length is sacled down to the 20nm, the solar cell efficiency is 82.1%.

As the Figure 3.31-3.33 shown, the vertical structure of the nanodevice can reach 4.6% solar cell efficiency based on the simulation result. Because of the symmetric structure, the photocurrent is substracted by each unit cell. Finally, we found that horizontal structure is suitable for the solar cell application.

(a) (b)



(c) (d)

Figure 3.1 The environment setup for I-V characteristics measurement,
(a) probe station (b) HP4156 (c) the spectrum of the daylight lamp (d) Solar Spectrum

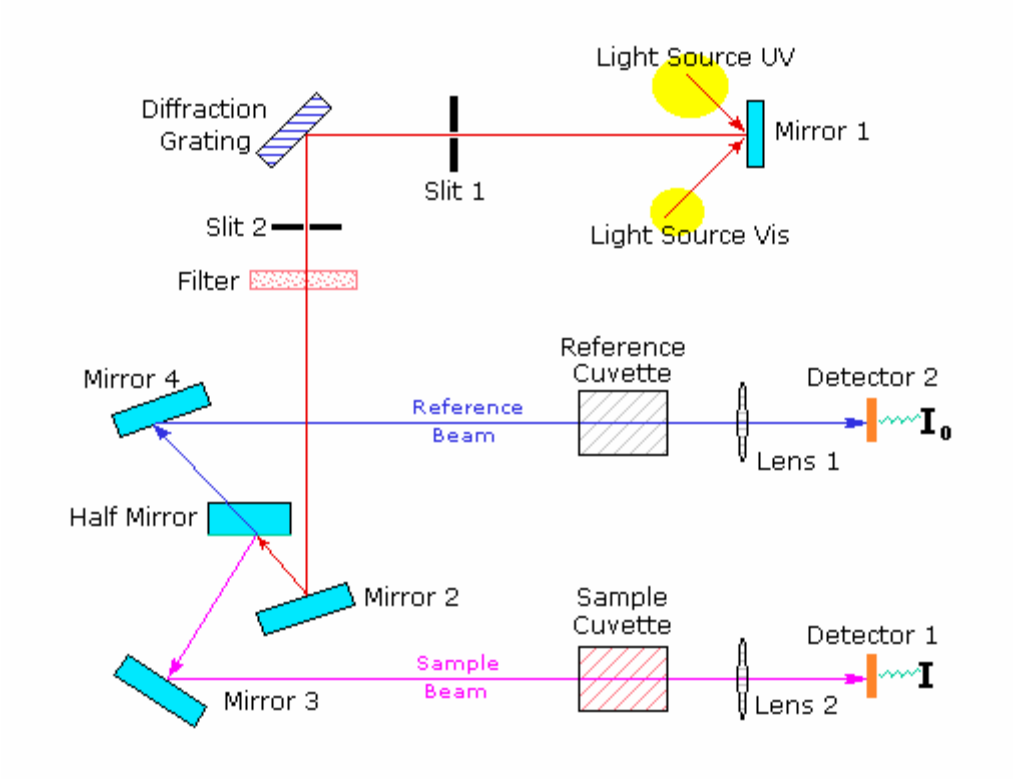
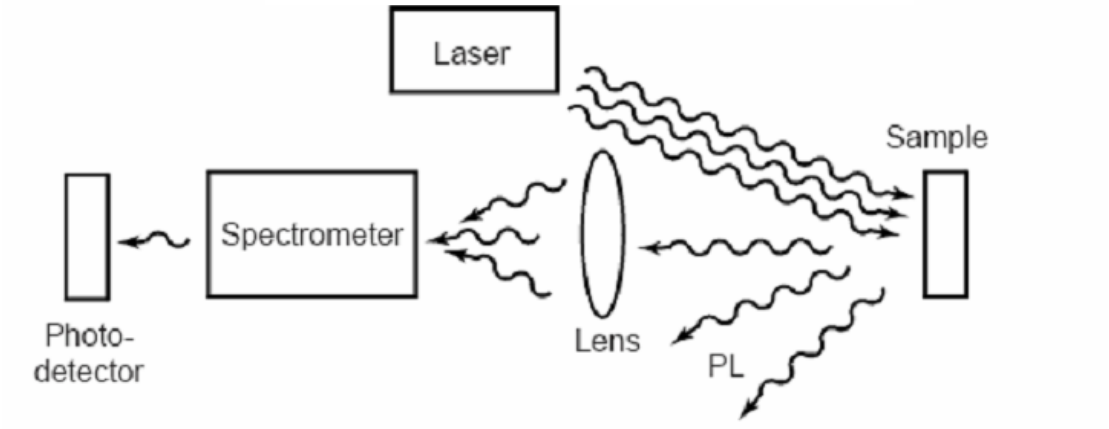


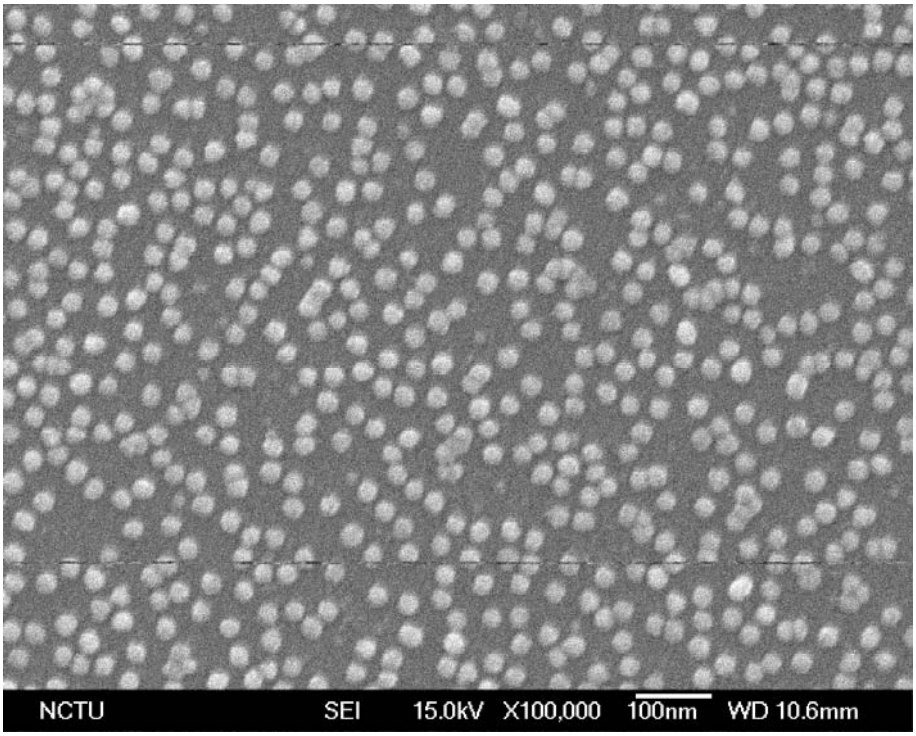
Figure 3.2 The environment setup for UV-visible absorbance spectrum measurement.

375 nm, 400 nm, 435 nm photo-excitation

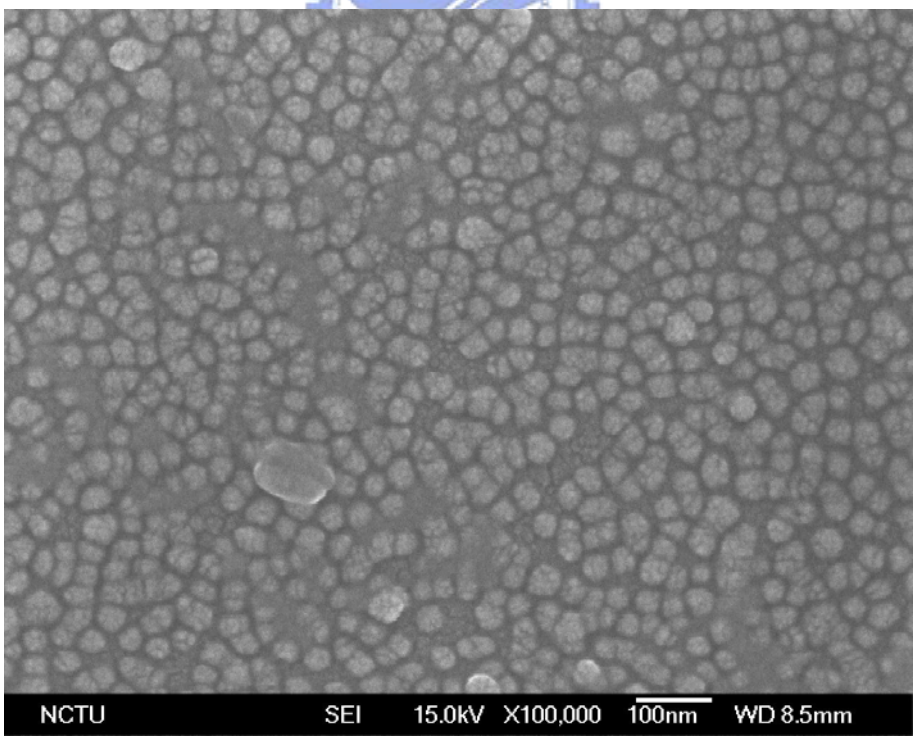


Filter out < 500 nm

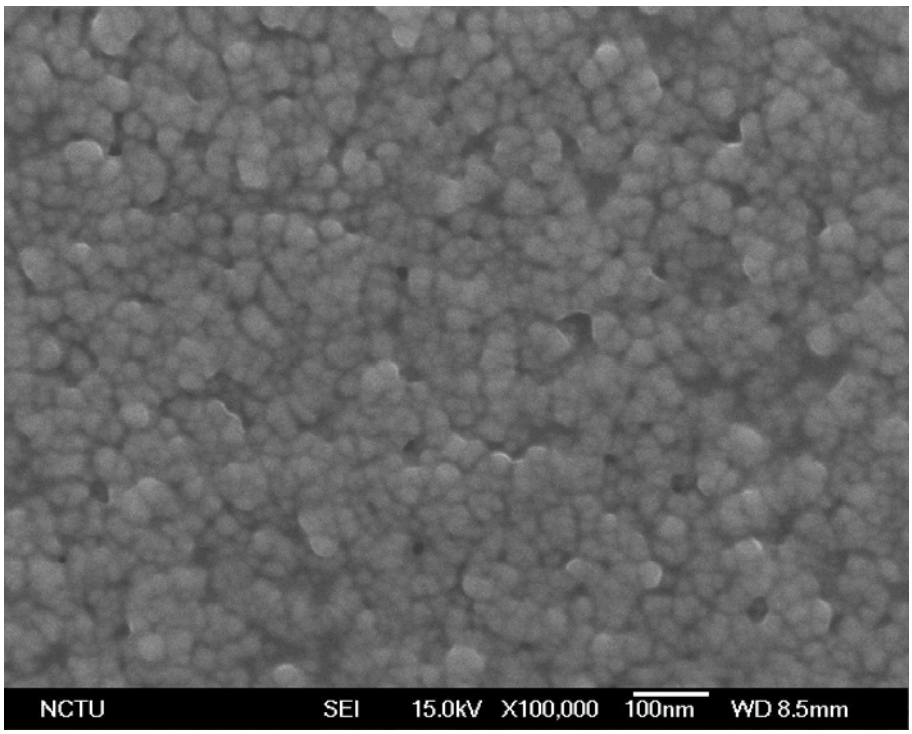
Figure 3.3 The environment setup for PL intensity spectrum measurement.



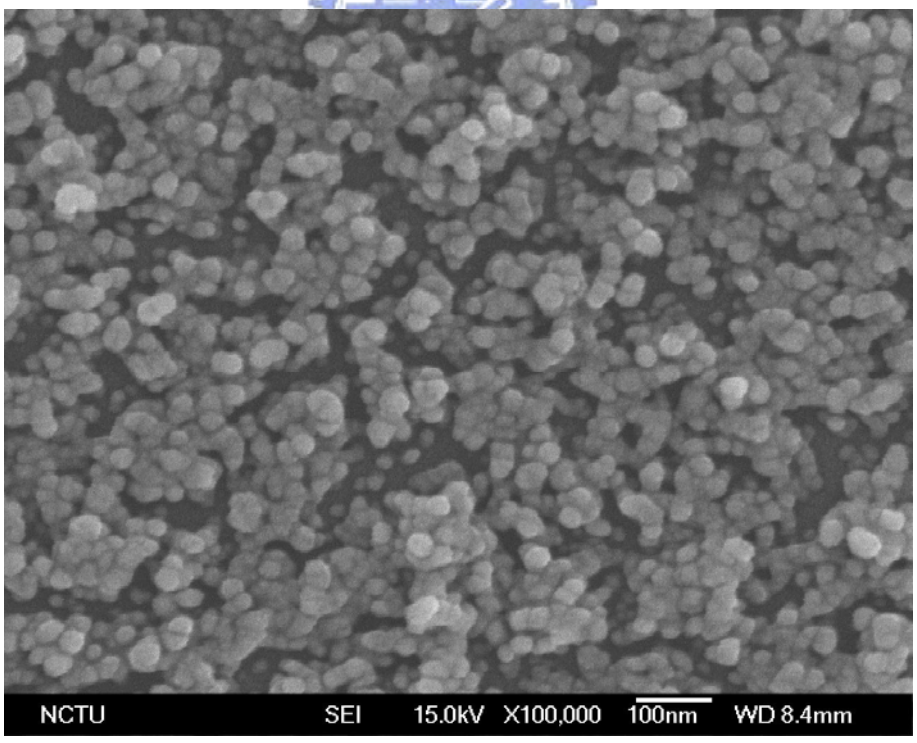
(a) Au NPs on SiO_2/Si wafer fragment



(b) CdSe QDs + Au NPs on SiO_2/Si wafer fragment



(c) Au NPs + CdSe QDs + Au NPs on SiO_2/Si wafer fragment



(d) CdSe QDs + Au NPs + CdSe QDs + Au NPs on SiO_2/Si wafer fragment

Figure 3.4 The SEM images (100k magnification) of Au / CdSe nanostructure of different level construction are shown above (a)~(e).

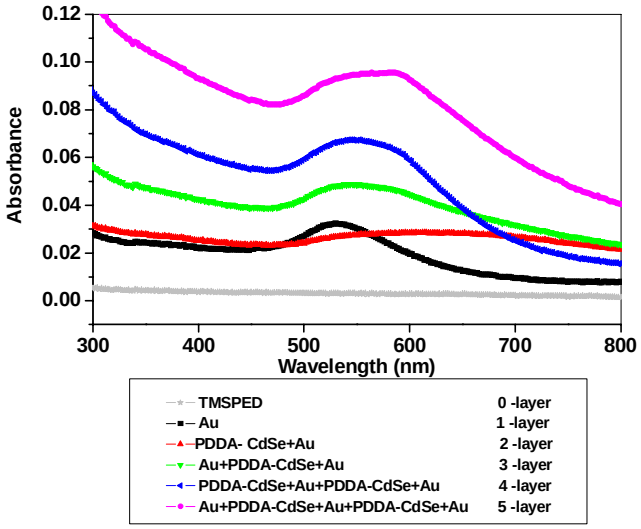


Figure 3.5 The UV-visible absorption spectrum of multi-layered nanostructure on quartz glass**.** The Light Gray Line: 10% TMSPED/methanol ->quartz glass. The Black Line: 1-layered nanostructure. The Red Line: 2-layered nanostructure. The Green Line: 3-layered nanostructure. The Blue Line: 4-layered nanostructure. The Magenta Line: 5-layered nanostructure.

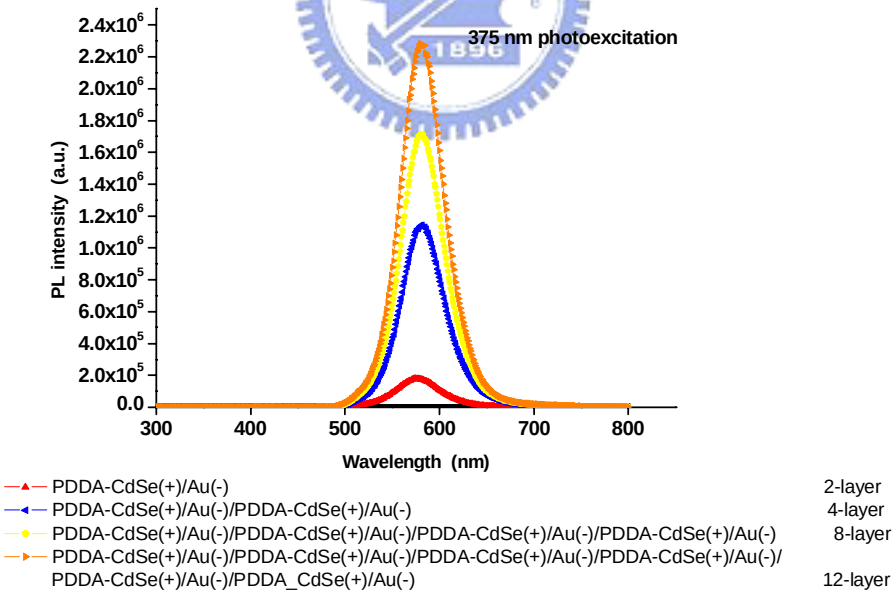


Figure 3.6 The PL emission spectrum of multi-layered nanostructures on quartz glass. The PL intensity of Au / PDDA-CdSe multi-layer nanostructure under 375nm photo-excitation is shown above. The Red Line: 2-layered nanostructure; The Blue Line: 4-layered nanostructure; The Yellow Line: 8-layered nanostructure; The Orange Line: 12-layered nanostructure.

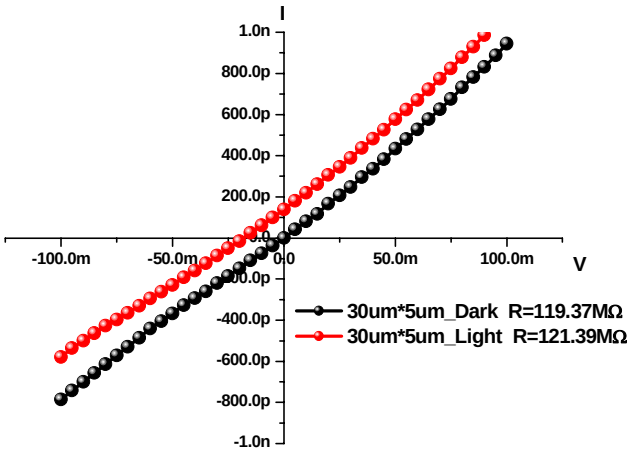


Figure 3.7 The I-V curve of the 30um / 5um (width / length) 4-layered PDDA-CdSe nanodevice

	[Au / CdSe] Nanodevice Electrodes under illumination (4-layered PDDA-CdSe Nanodevice)		
	30um X 5um	30um X 15um	30um X 30um
Volume (nm^3)	$3.2 * 10^{13}$		
Vbias	-100mV~100mV		
Isc (pA)	139	45.5	19
Voc (mV)	-18.1	-17.8	-15.624
Isc * Voc	2.5159pW	0.8099pW	0.0103pW
Req (Dark)	119.37M	390.46M	753.76M
Req (Light)	121.39M	373.38M	833.16M
PVD (A/nm^3)	$4.344 * 10^{-24}$	$1.422 * 10^{-24}$	$1.222 * 10^{-25}$
Power VD (W/nm^3)	$1.966 * 10^{-26}$	$6.327 * 10^{-27}$	$8.048 * 10^{-29}$
Efficiency (%)	0.214	0.025	0.006

Table 3.1 The measurement results of the 4-layered PDDA-CdSe nanodevice (PVD: photocurrent volume density, Power VD: power volume density)

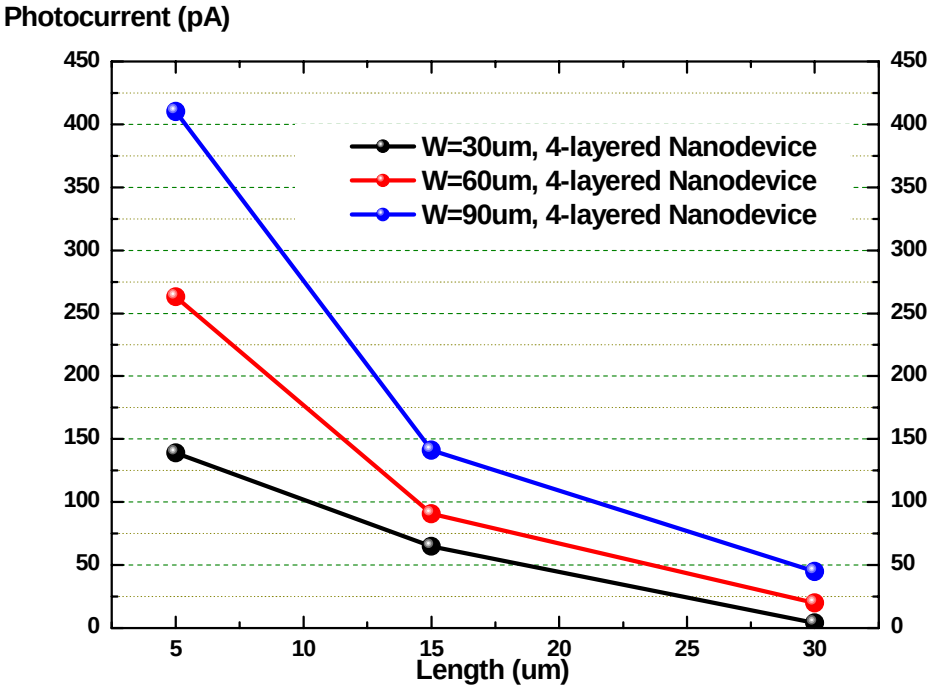


Figure 3.8 The photocurrent comparison of the 4-layered AET-CdSe nanodevice

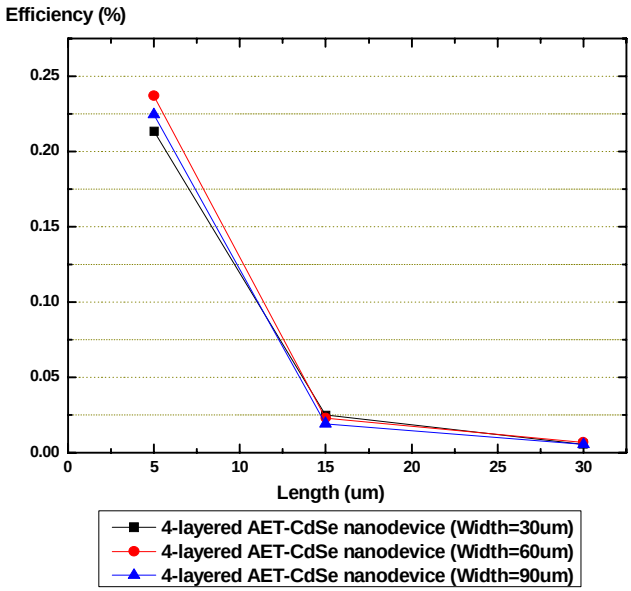
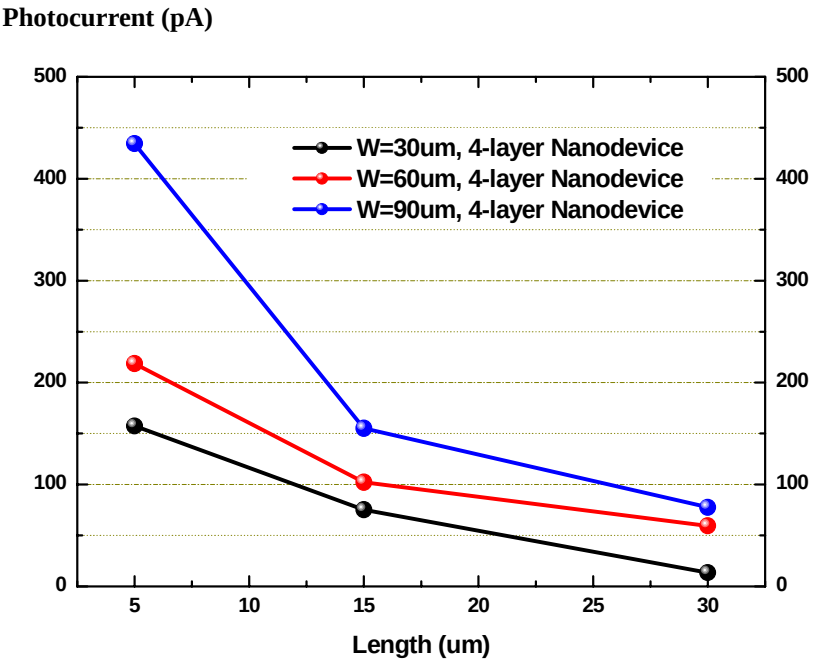
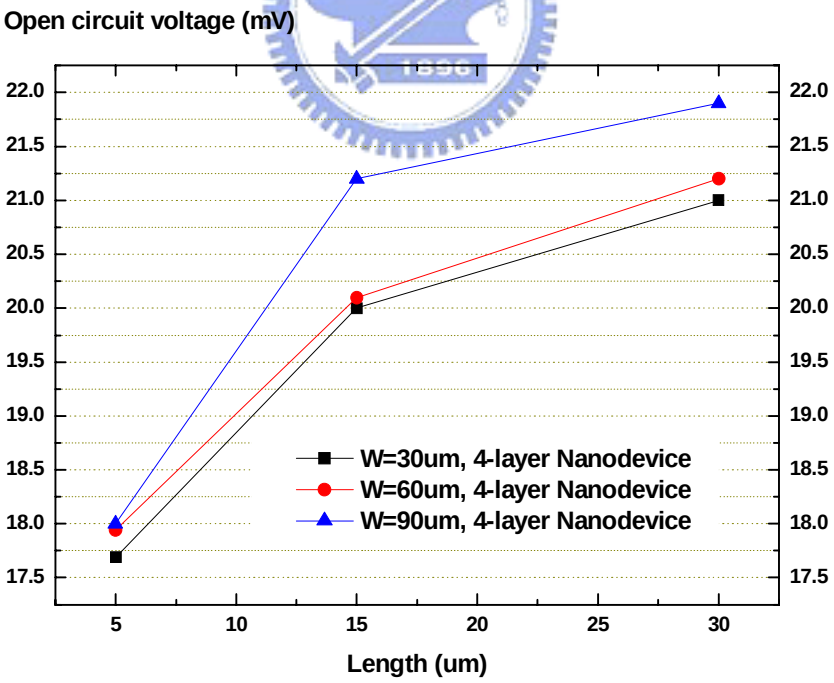


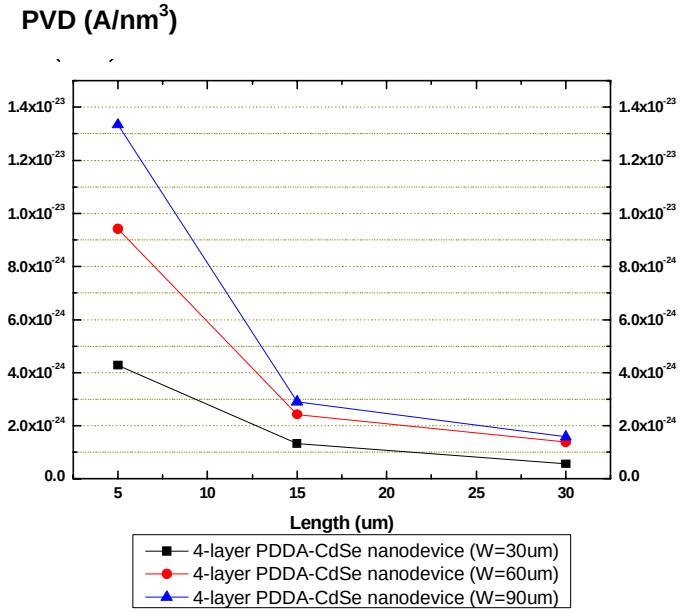
Figure 3.9 The Efficiency comparison of the 4-layered AET-CdSe nanodevice


Photocurrent (pA)
W=30um, 4-layer Nanodevice
W=60um, 4-layer Nanodevice
W=90um, 4-layer Nanodevice
Length (um)

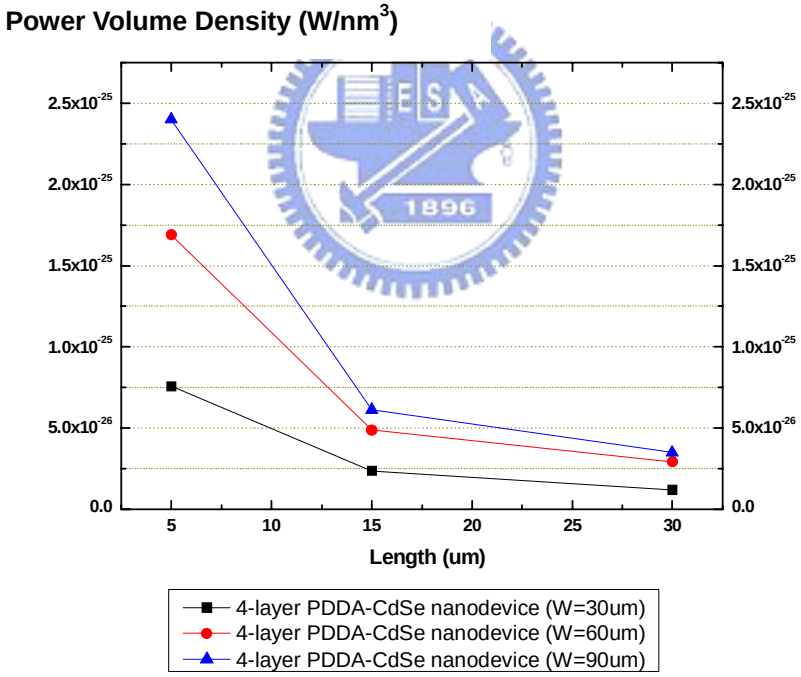
(a)


Open circuit voltage (mV)
W=30um, 4-layer Nanodevice
W=60um, 4-layer Nanodevice
W=90um, 4-layer Nanodevice
Length (um)

(b)



(c)



(d)

Figure 3.10 (a) The photocurrent comparison of the 4-layered PDDA-CdSe nanodevice (b) The open circuit voltage comparison of the 4-layered PDDA -CdSe nanodevice (c) The PVD comparison of the 4-layered PDDA -CdSe nanodevice (d) The power volume density comparison of the 4-layered PDDA -CdSe nanodevice

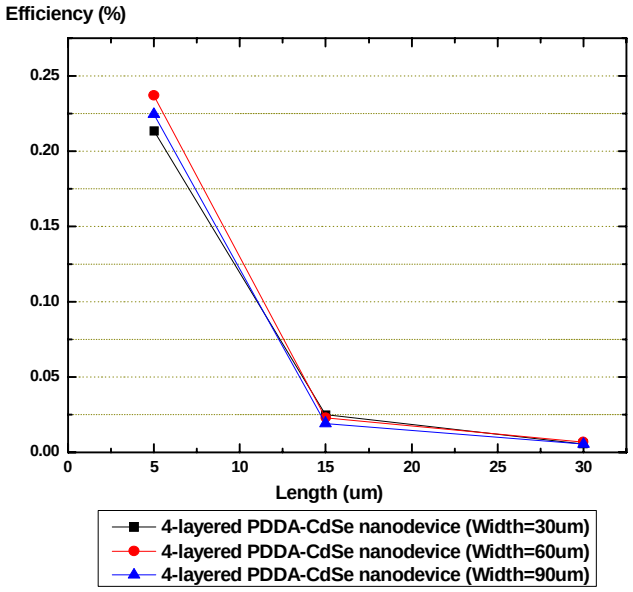


Figure 3.11 The efficiency comparison of the 4-layered PDDA-CdSe nanodevice

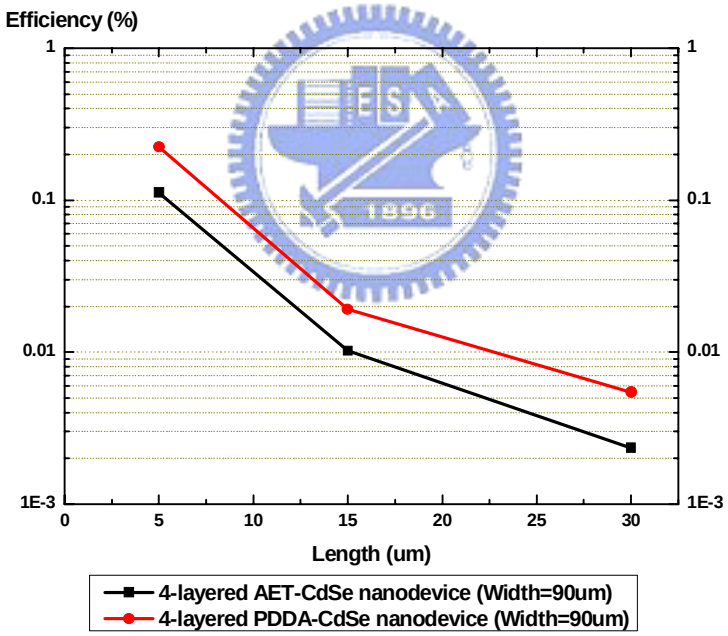
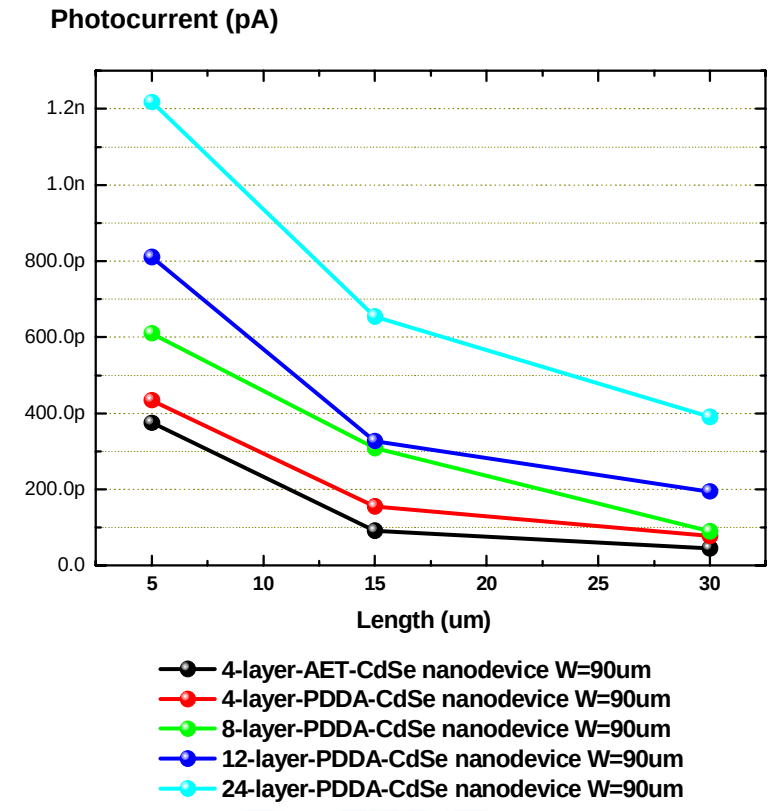
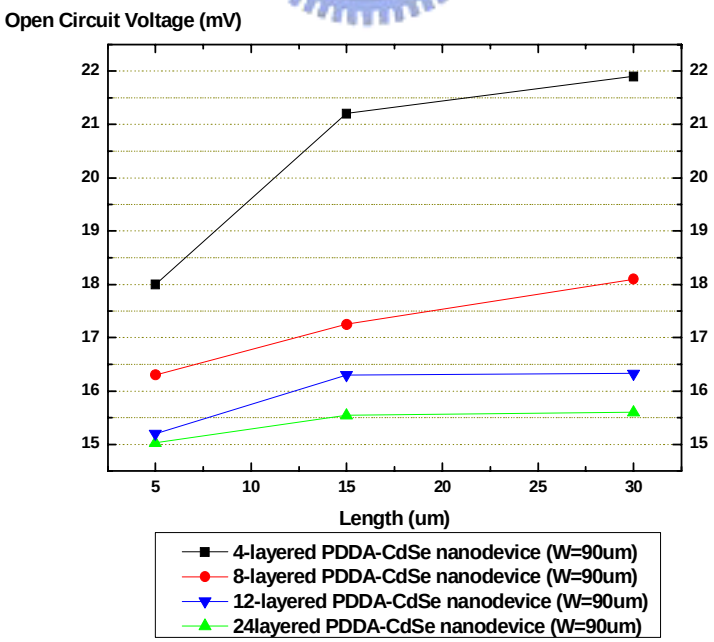


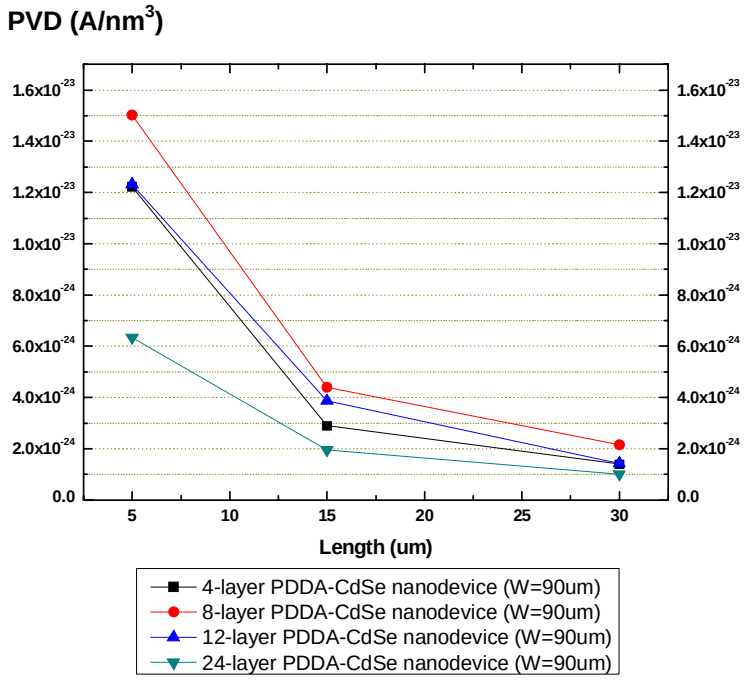
Figure 3.12 The efficiency comparison of the 4-layered nanodevices with different types of CdSe QDs.


Photocurrent (pA)
1.2n
1.0n
800.0p
600.0p
400.0p
200.0p
0.0
5
10
15
20
25
30
Length (um)
4-layer-AET-CdSe nanodevice W=90um
4-layer-PDDA-CdSe nanodevice W=90um
8-layer-PDDA-CdSe nanodevice W=90um
12-layer-PDDA-CdSe nanodevice W=90um
24-layer-PDDA-CdSe nanodevice W=90um

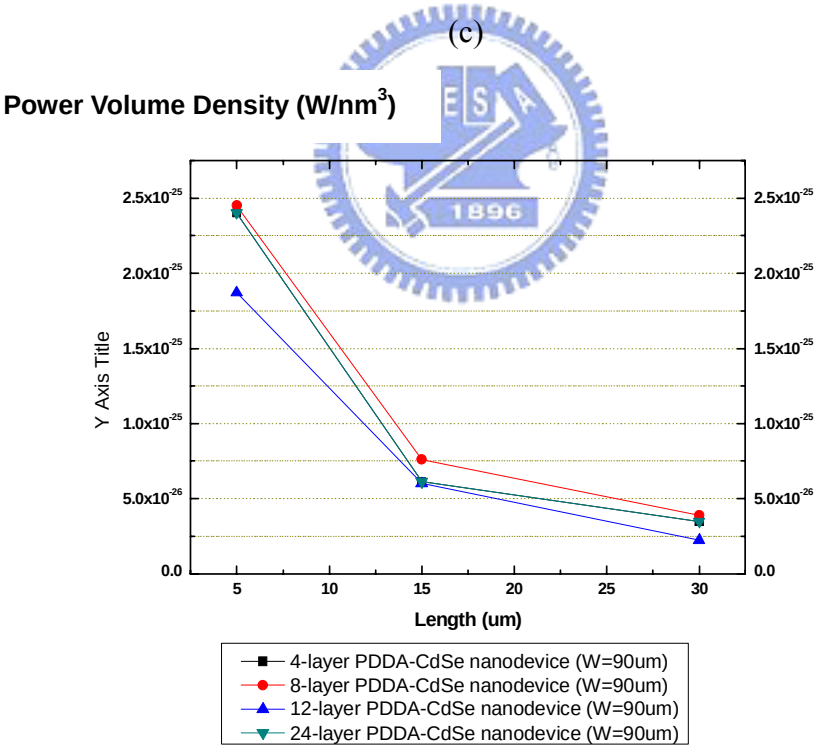
(a)


Open Circuit Voltage (mV)
22
21
20
19
18
17
16
15
5
10
15
20
25
30
Length (um)
4-layered PDDA-CdSe nanodevice (W=90um)
8-layered PDDA-CdSe nanodevice (W=90um)
12-layered PDDA-CdSe nanodevice (W=90um)
24layered PDDA-CdSe nanodevice (W=90um)

(b)



(c)



(d)

Figure 3.13 (a) The photocurrent comparison of the nanodevices (width = 90um) (b) The open circuit voltage comparison of the nanodevices (width = 90um) (c) The photocurrent volume density comparison of the nanodevices (width = 90um) (d) The power volume density comparison of the nanodevices (width = 90um)

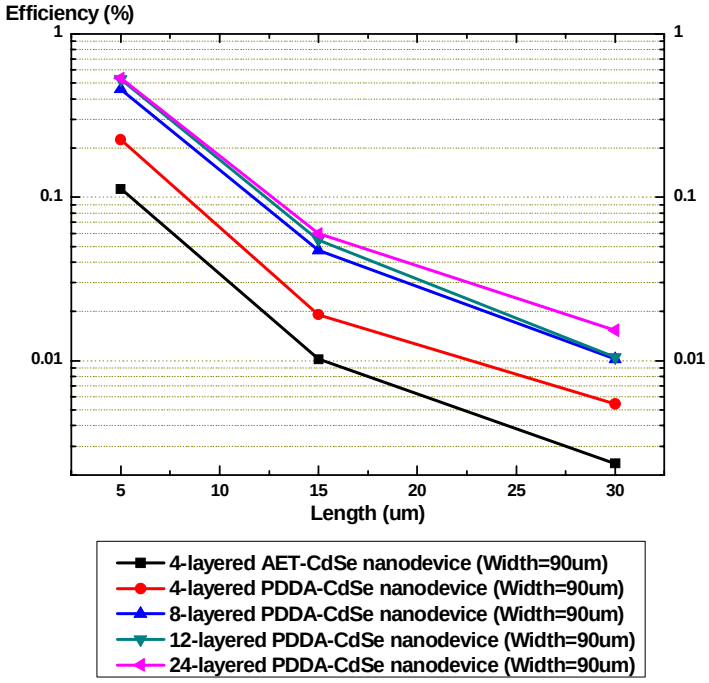


Figure 3.14 The efficiency comparison of the nanodevices (width = 90um)

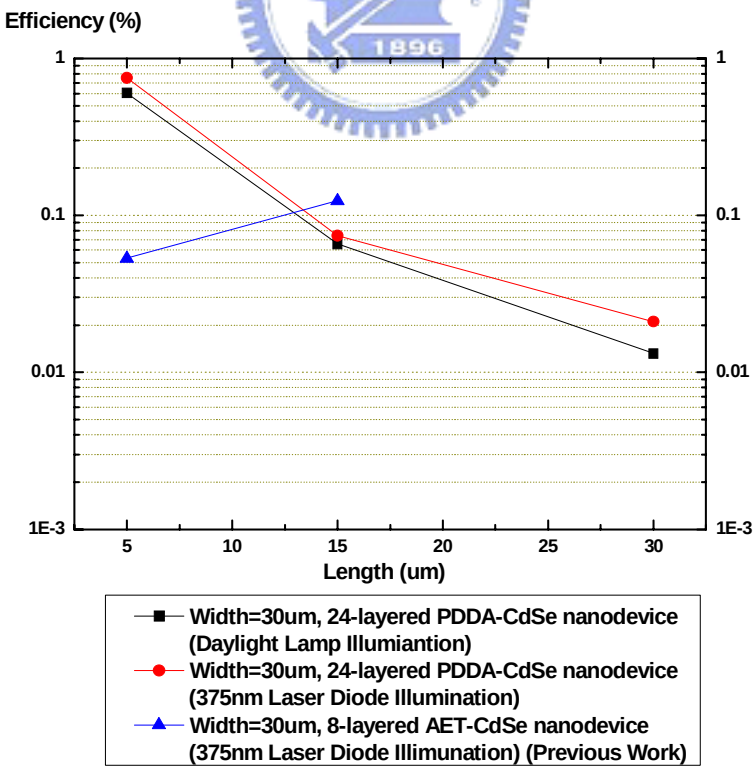
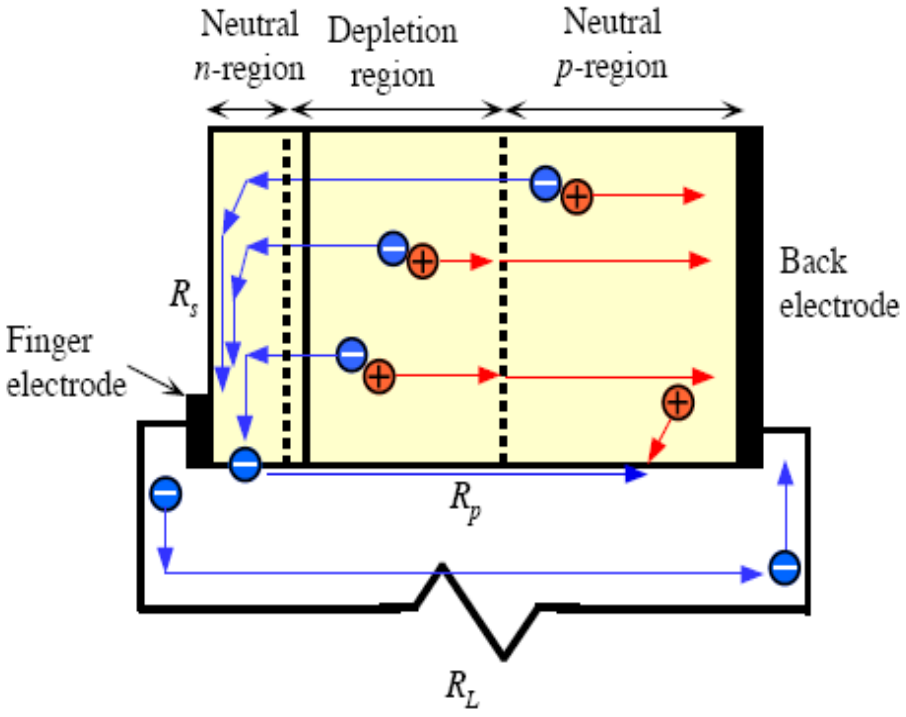
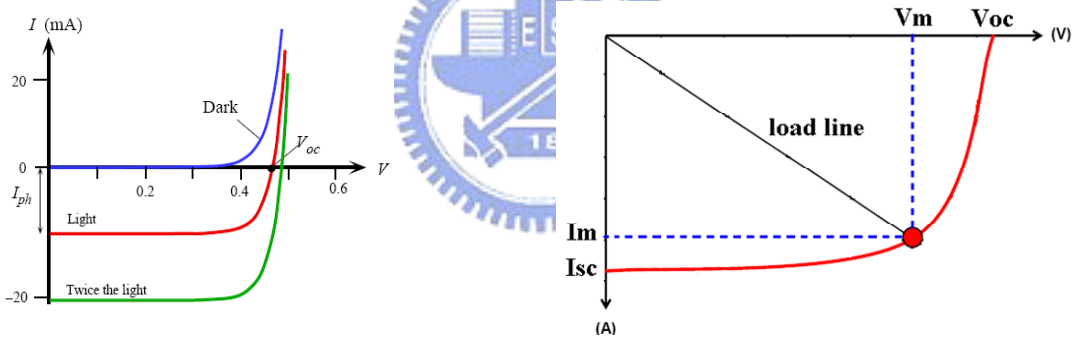


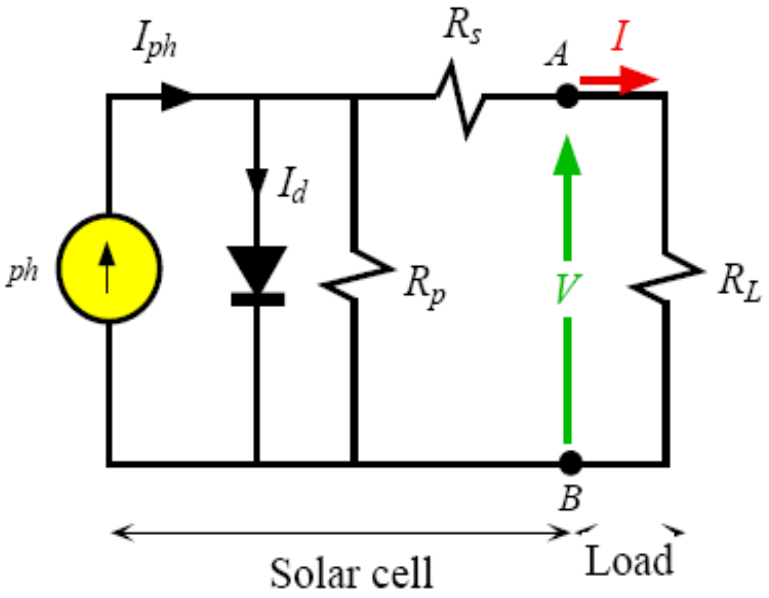
Figure 3.15 The efficiency comparison of the nanodevices with previous work


Neutral
n-region
Depletion
region
Neutral
p-region
Back
electrode
Finger
electrode
R_s
R_p
R_L

(a)


I (mA)
20
0
−20
Dark
V_{oc}
V
0.2
0.4
0.6
I_{ph}
Light
Twice the light
Vm
Voc
(V)
load line
Im
Isc
(A)

(b)



(c)

Figure 3.16 (a) The p-n junction solar cell structure, (b) the I-V cureve of the p-n junction solar cell, (c) the equivalent circuit of the p-n junction solar cell.

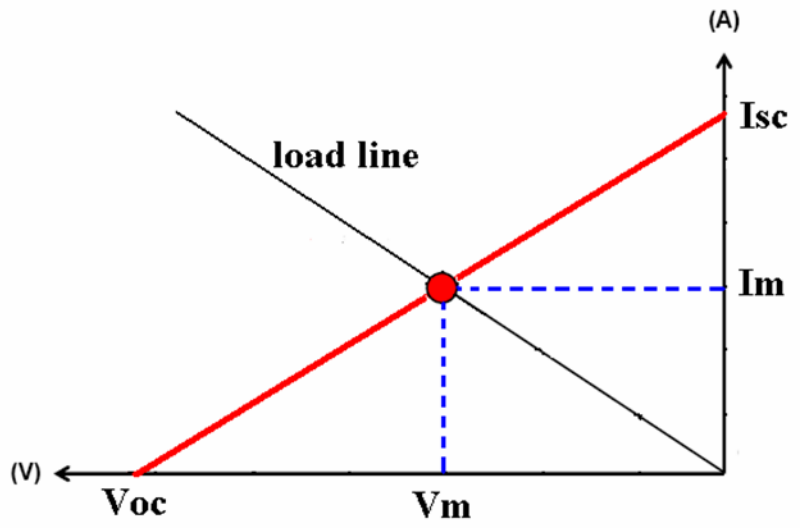
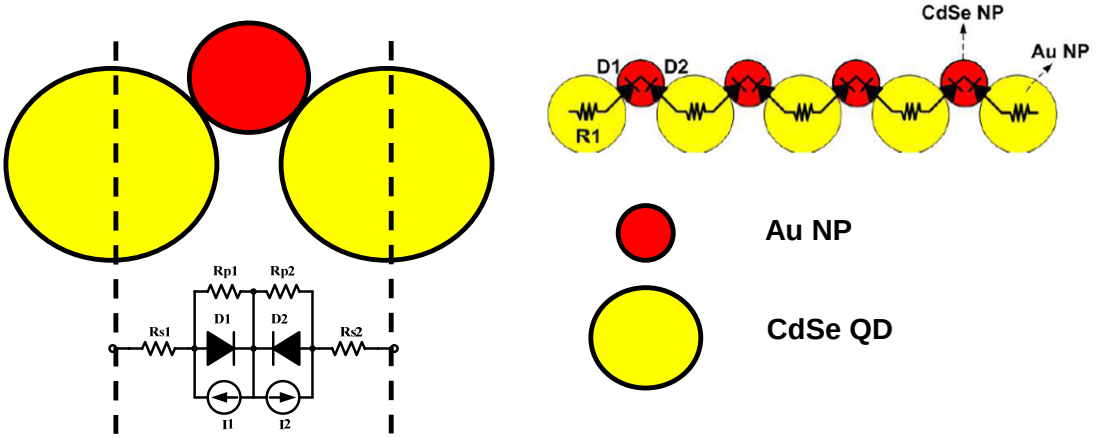


Figure 3.17 The I-V curve of the Au / CdSe nanodevice



(a) (b)

Figure 3.17 (a) The unit cell of the nanodevice model, (b)The 1-D Au / CdSe nanodevice Model

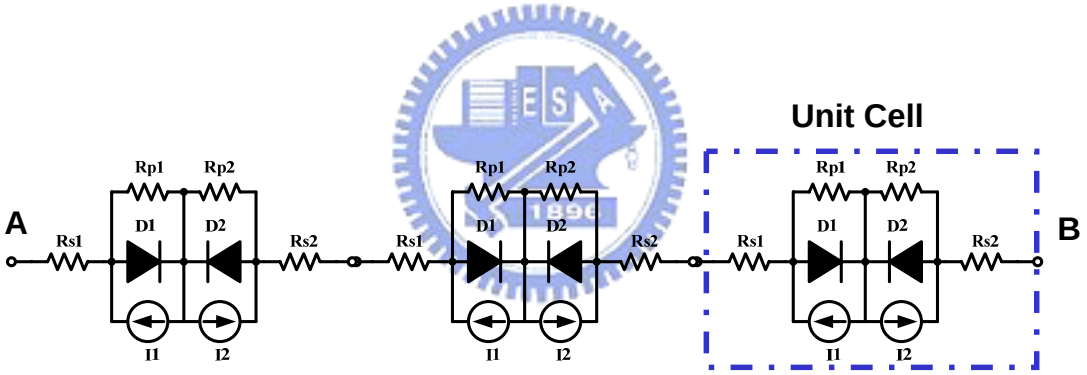
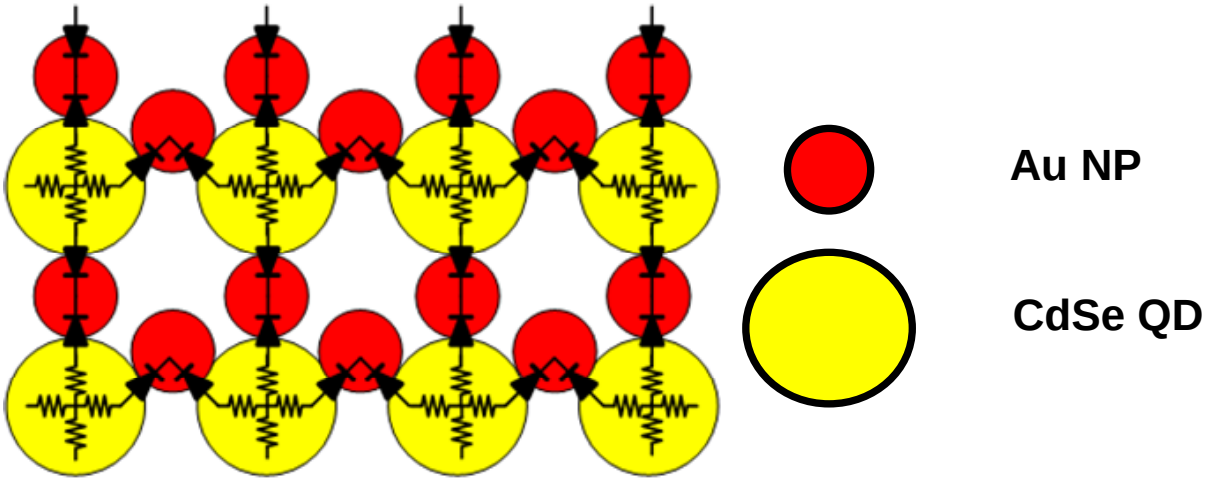
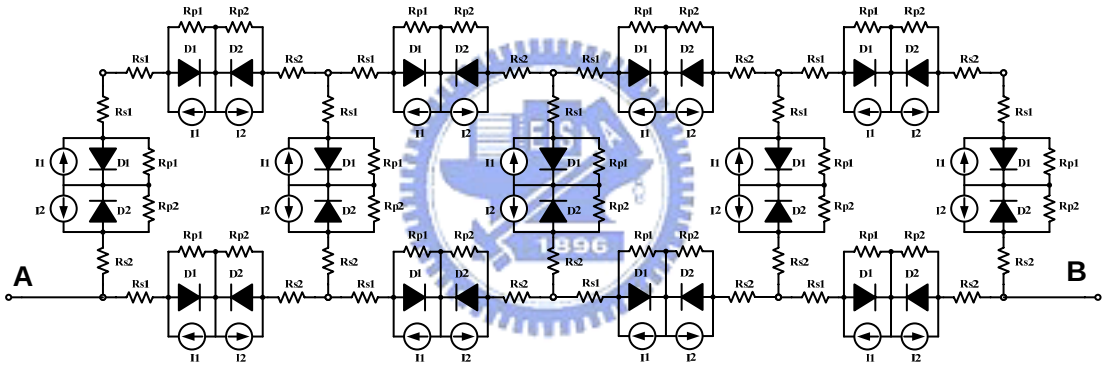


Figure 3.18 The 1-D nanodevice model. For HSPICE simulation, Metal-Insulator-Semiconductor diode model was employed.



(a)



(b)

Figure 3.19 The 2-D nanodevice model (HSPICE). (a) The structure view of the 2-D nanodevice, (b) the 2-D nanodevice model equivalent circuit (4-layer nanodevice). For HSPICE simulation, Metal-Insulator-Semiconductor diode model was employed.

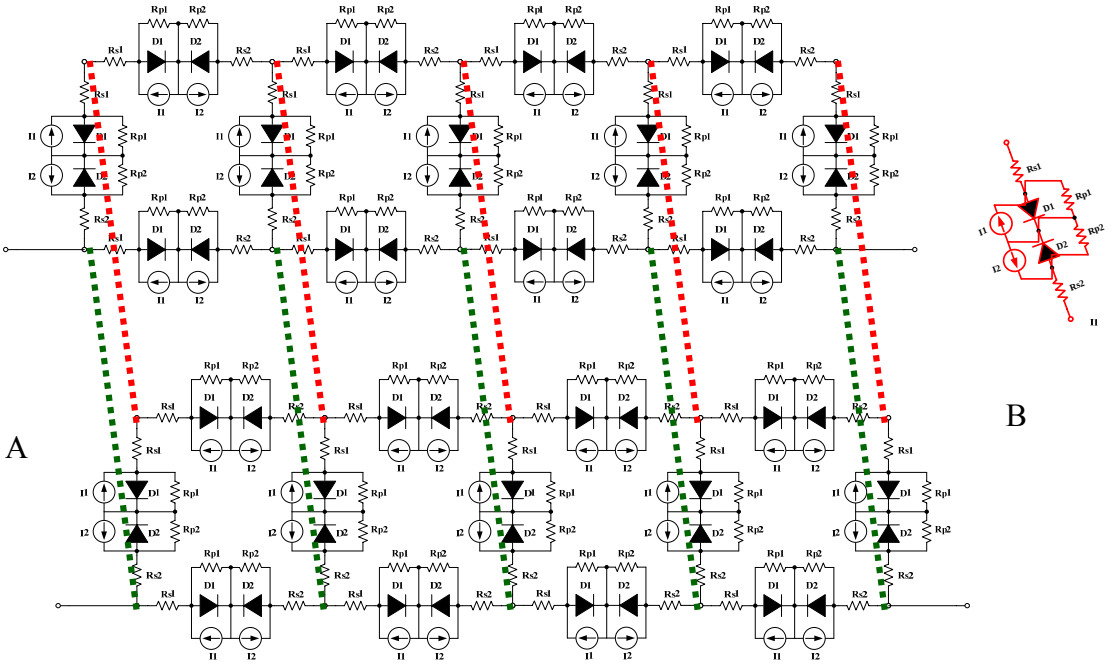


Figure 3.20 The 3-D nanodevice model (HSPICE). The dash line parts are substituted for the unit cells. For HSPICE simulation, Metal-Insulator-Semiconductor diode model was employed.

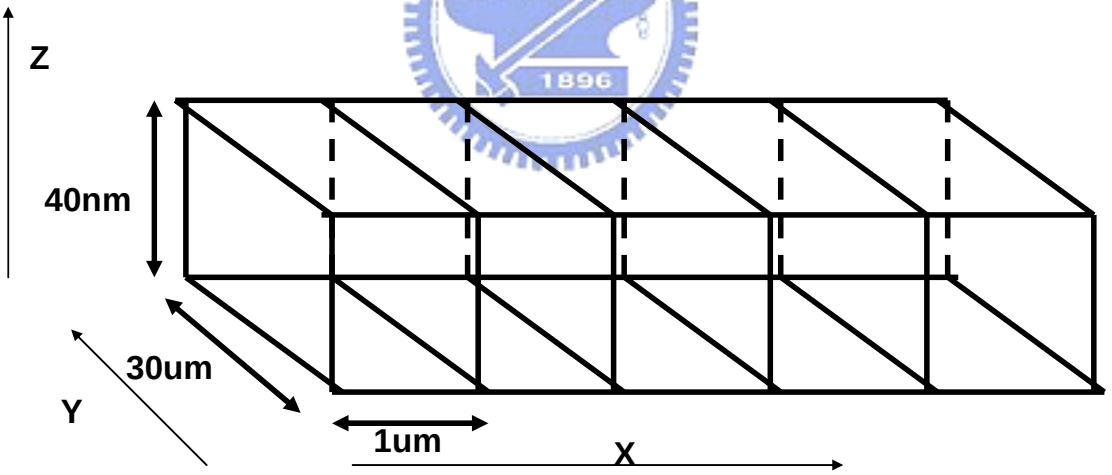


Figure 3.21 The 3-D nanodevice model (HSPICE). The line parts are substituted for the unit cells. For HSPICE simulation, Metal-Insulator-Semiconductor diode model was employed. X-dimension unit cell : Rs=0.153MΩ, Rp=48.178MΩ, I=2.1nA

Y-dimension unit cell : Rs=0.918MΩ, Rp=289MΩ, I=2.1nA,.Z-dimension unit cell : Rs=6120Ω, Rp=1.95M, I=2.1nA

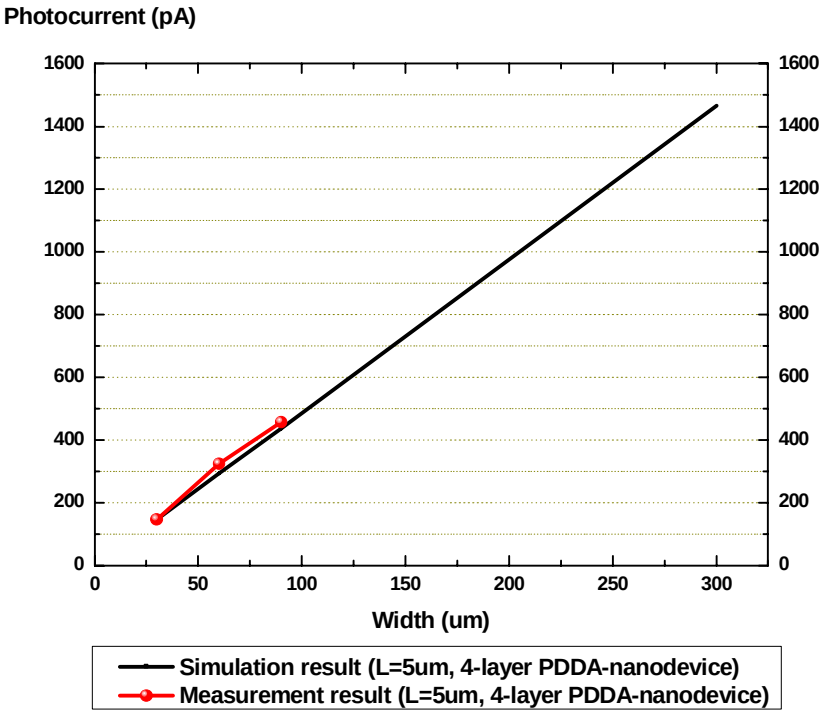


Figure 3.22 (Width Effect) The 3-D nanodevice model (HSPICE) simulation result. The photocurrent increases linearly as the width increases. (fixed length=5um, fixed number of layer=4)

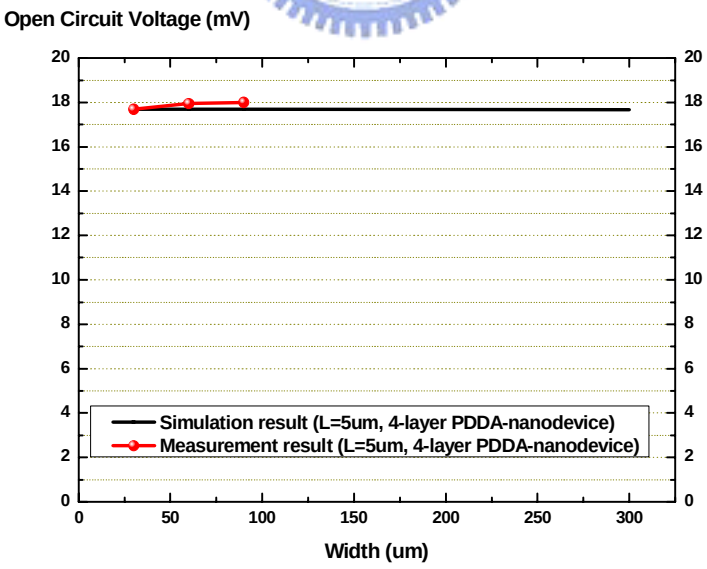


Figure 3.23 (Width Effect) The 3-D nanodevice model (HSPICE) simulation result. The open circuit voltage is a constant value. (fixed length=5um, fixed number of layer=4)

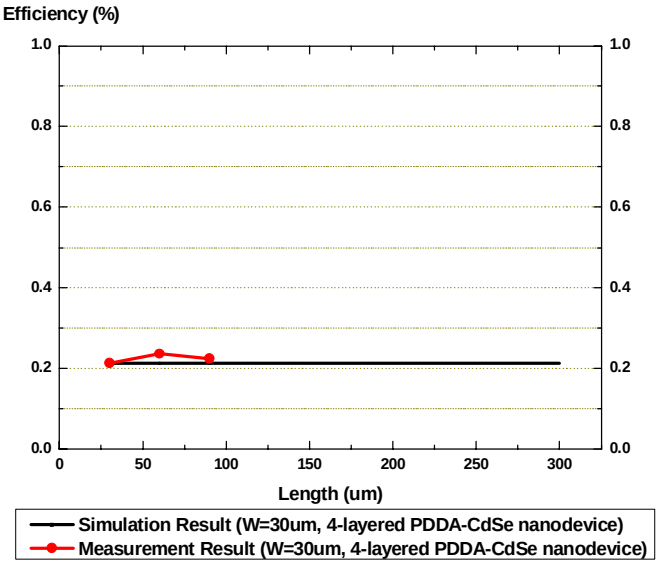


Figure 3.24 (Width Effect) The 3-D nanodevice model (HSPICE) simulation result. The efficiency is a constant value when the nanodevice width varies. (fixed length=5um, fixed number of layer=4)

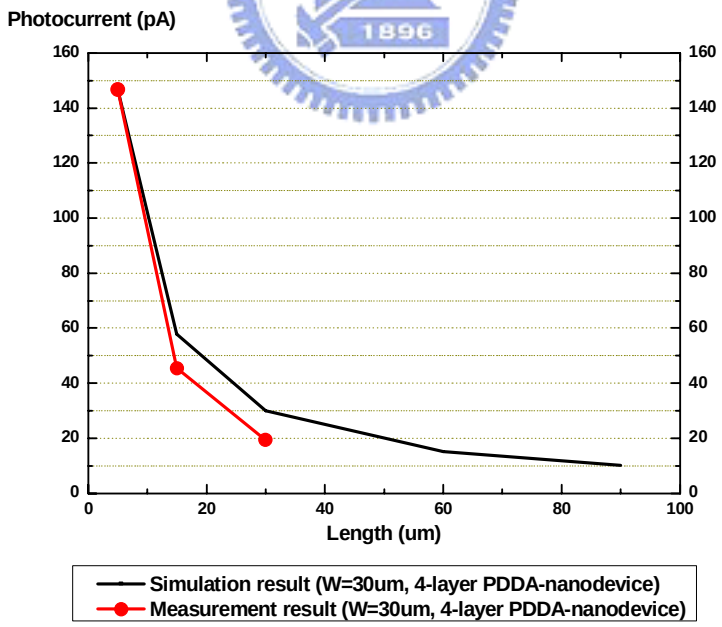


Figure 3.25 (Length Effect) The 3-D nanodevice model (HSPICE) simulation result. The photocurrent decreases as the length increases. (fixed width=30um, fixed number of layer=4)

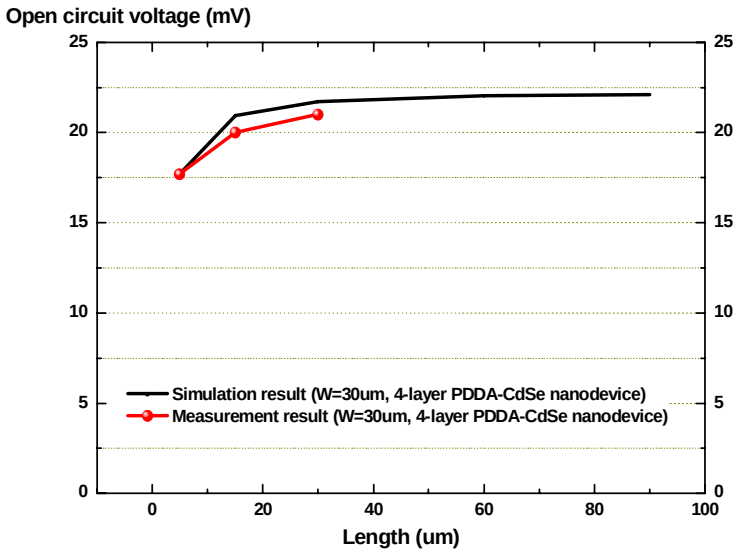


Figure 3.26 (Length Effect) The 3-D nanodevice model (HSPICE) simulation result. The open circuit voltage saturates as the length increases. (fixed width=30um, fixed number of layer=4)

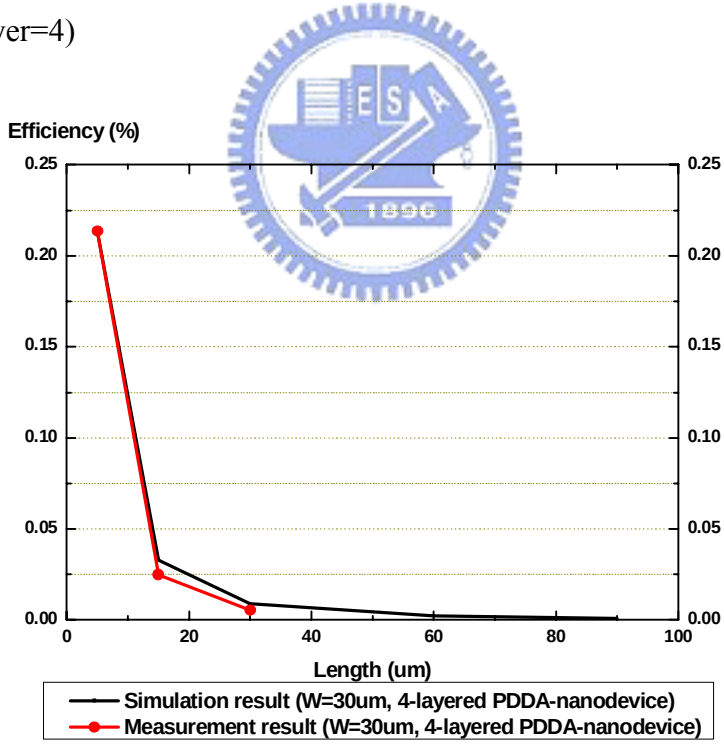


Figure 3.27 (Length Effect) The 3-D nanodevice model (HSPICE) simulation result. The efficiency decreases as the length increases. (fixed width=30um, fixed number of layer = 4)

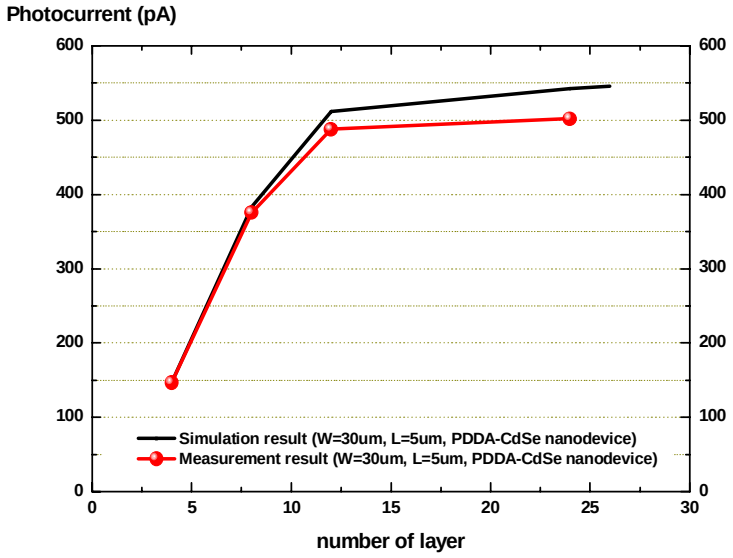


Figure 3.28 (Layer Effect) The 3-D nanodevice model (HSPICE) simulation result. The photocurrent saturates when the number of the layer larger than eight. (fixed width=30um, fixed length=5um)

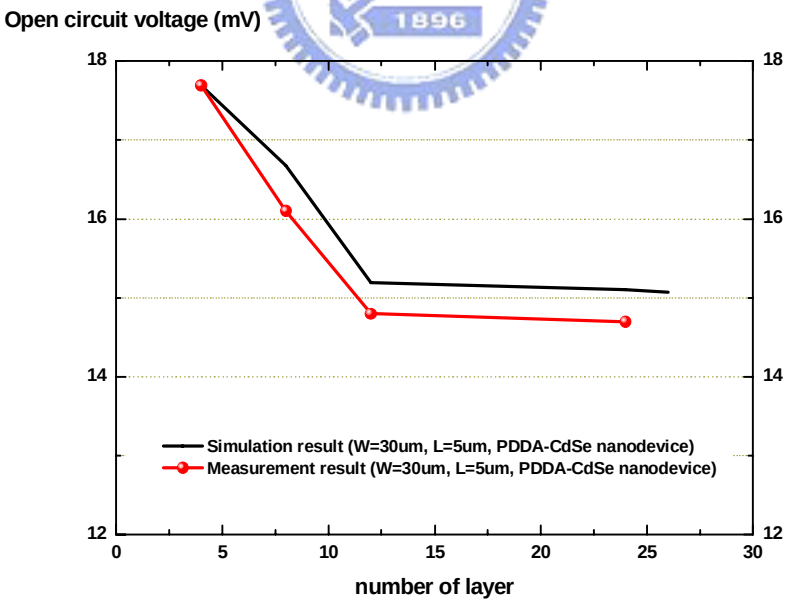


Figure 3.29 (Layer Effect) The 3-D nanodevice model (HSPICE) simulation result. The open circuit voltage decreases linearly, and then settles to a constant value. (fixed width=30um, fixed length=5um)

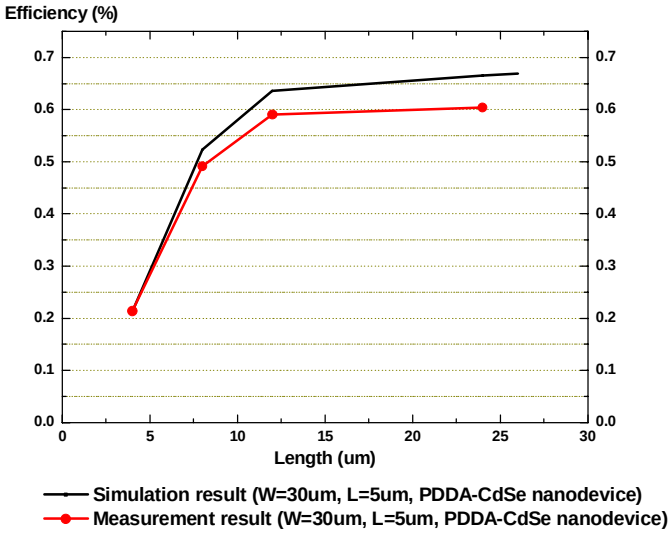
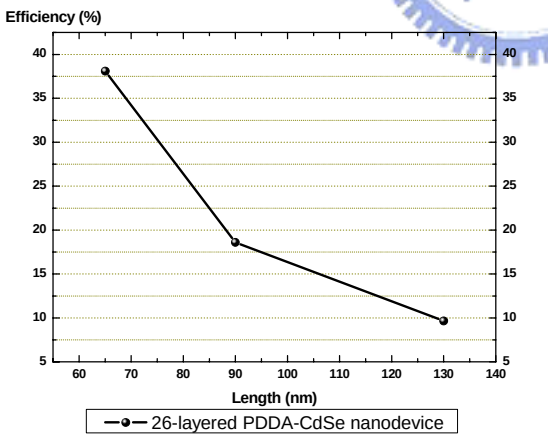


Figure 3.30 (Layer Effect) The 3-D nanodevice model (HSPICE) simulation result. The efficiency saturates when the number of the layer is larger than 12. According to the simulation result, the efficiency does not increase obviously if the number of the layer exceeds 26. (fixed width=30um, fixed length=5um)



Efficiency	Length
38.1%	65nm
18.6%	90nm
9.6%	130nm

Table 3.2 According to the simulation results, the better device dimension to reach the high efficiency solar cell can be decided. 26-layered nanodevices with 30um in width are adopted to predict the high efficiency. On the basis of the ideal inference, the 9.2% PDDA-CdSe nanodevice can be fabricated if the length of the device is 65nm.

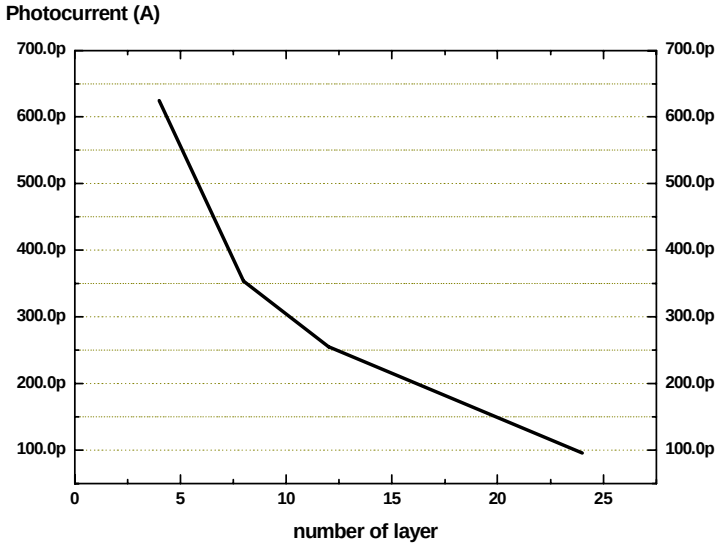


Figure 3.31 (Vertical Structure) The 3-D nanodevice model (HSPICE) simulation result. The photocurrent decreases when the number of the layer increases. (fixed width=30um, fixed length=5um)

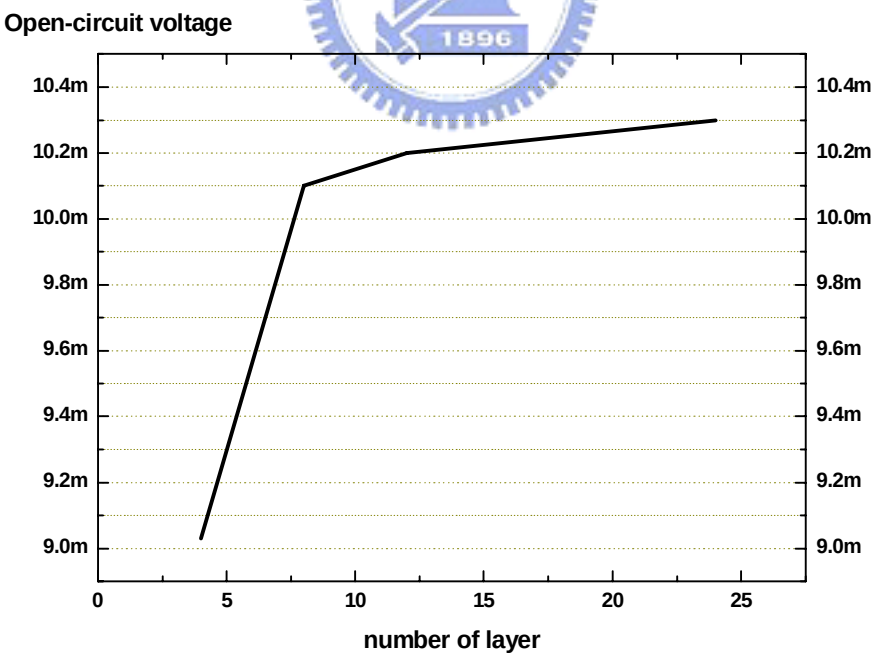


Figure 3.32 (Vertical Structure) The 3-D nanodevice model (HSPICE) simulation result. (fixed width=30um, fixed length=5um)

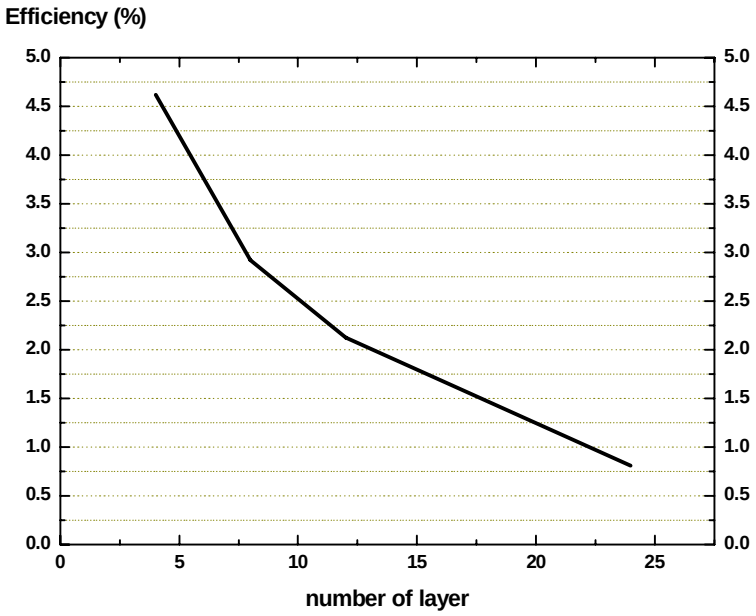


Figure 3.33 (Vertical Structure) The 3-D nanodevice model (HSPICE) simulation result. The efficiency increases as the number of the layer decreases. (fixed width=30um, fixed length=5um)

CHAPTER 4

APPLICAION OF LINEAR REGULATOR ON CdSe / Au NANOPARTICLE SOLAR CELL

Using solar cell to provide the power of portable devices has been considered as one of the potential architecture in the future. The market for regulators has been driven by the portable electronics as well as industrial and automotive applications. Recently, the increasing demand for portable and solar-cell-based devices has caused a revolution in low operating voltage.

Generally, Linear Regulators and Switching Regulators are widely used in the commercial electronic applications. Linear Regulators are purely analog circuits. The utilization of the feedback network is adopted in them. Based on the output of the feedback network, the output can be adjusted to the desired voltage immediately. According to the configuration of the liner regulator, it can only step down the voltage from the power devices. On the other hand, Switching regulators are essentially mixed-mode circuits that feedback an error signal and digitally gate it to provide bursts of current to the output. Furthermore, switching regulators can provide a wide range of output voltages including values that are lower or greater than the input voltage depending on the circuit configuration, buck or boost.

In this work, the linear regulator architecture is adopted. The reason for this is because, first of all, the linear regulator does not suffer the switching noise generated by the clock. Secondly, the regulator can be implemented without the use of inductor. The circuit is inherently less complex and costly than the switching regulator realization.

In this chapter, a linear regulator is designed to target the low voltage conditions and integrated with the CdSe / Au nanoparticle solar cell. The relevant analysis is introduced to design the system, and the TSMC 2P4M CMOS 0.35um technology is used to implement the linear regulator. Finally, the measurement result of the linear regulator chip is showed and discussed.

4.1 System Design Considerations

4.1.1 System Architecture

Proper design of a linear regulator involves intricate knowledge of the system and its load. The tasks if maximizing load regulation, maintaining stability, and minimizing transient output voltage variations prove to be challenging and often conflicting. As the figure 4.1 shown, this architecture was utilized in this work. The system is composed of an error amplifier, a pass element, feedback resistors, and off-chip compensating capacitor. The feedback loop force the output voltage to be regulated at the voltage Vref. However, the stability issue of the feedback loop should be concerned. In this section, the AC analysis and Transient analysis of the linear regulator will be discussed.

4.1.2 AC Analysis

Figure 4.2 illustrates the intrinsic factors that determine the stability of the linear regulator, namely, an error amplifier, a pass element, feedback resistors, an

output loading and associated output impedance, an output capacitor and associated electrical series resistance (ESR), and bypass capacitors.

Then, the each element of the system is introduced. The ESR of the bypass capacitors can typically be neglected because they are usually high frequency capacitors; in other words, the ESR value is low. The pass device is modeled as a circuit element exhibiting a transconductance of gmp and an output impedance of Ro-pass. In this work, a large size PMOS is used. The value of R2 is dependent on the desired value if the output voltage and it means that R2 is zero if Vout is desired to be equal to Vref. The ratio of the Vref and the Vout is related to the ratio of the R2 and R1. The value of R1, on the other hand, is designed to define the quiescent current flowing through R1 and R2 (R1 = Vref / IR1), which is typically high to minimize quiescent overhead.

Frequency Response

Next, the frequency response analysis will be discussed. For the purpose of analysis, the feedback loop can be broken in figure 4.2. It is readily apparent that the system must be unity gain stable, considering Vref and Va to be the input and the output voltage respectively. The open-loop gain can be described as

$$\frac{Vfb}{Vref} = \frac{g_{ma} R_{oa} g_{mp} Z}{1 + sR_{oa} C_{par}} \cdot \frac{R_1}{R_1 + R_2} \quad (4.1)$$

where g_{ma} and g_{mp} refer to the transconductance of the amplifier and the pass element respectively, R_{oa} is the output resistance of the amplifier, Cpar refers to the parasitic capacitance introduced by the pass element, and Z is the impedance seen

at V_{out},

$$Z = Rx // \frac{1 + sR_{esr}C_o}{sC_o} // \frac{1}{sC_b} = \frac{R_x[1 + sR_{esr}C_o]}{s^2 R_x R_{esr} C C_b + s[R_x + R_{esr}]C + sR_x C_b + 1} \quad (4.2)$$

where Co and Resr are the capacitance and the ESR of the output capacitor, Cb represents the off-chip bypass capacitors, and Rx is the resistance seen from Vout into the regulator defined as

$$R_x = R_{o-pass} //(R_1 + R_2) \quad (4.3)$$

where $R_{o\text{-}pass}$ is the output resistance of the pass element. The output resistance of the load (R_L) is commonly neglected because its value is considerably lager than Rx. If Co is assumed to be reasonably larger than C_b, then Z approximates to

$$Z \cong \frac{R_x[1 + sR_{esr}C]}{[1 + s(R_x + R_{esr})C] \cdot [1 + s(R_x // R_{esr})C_b]} \quad (4.4)$$

It can be observed from the equation (4.1)-(4.4) that the overall transfer function of the system consists of three poles and one zero. For the typical load-current range, Rx can be simplified to Ro-pass because (R_1+R_2) is greater in magnitude. The poles and the zero can be approximated as

$$P_1 \cong \frac{1}{2\pi R_{o-pass} C}$$
$$P_2 \cong \frac{1}{2\pi R_{ear} C_b}$$
$$P_3 \cong \frac{1}{2\pi R_{oa} C_{par}}$$
$$Z_1 \cong \frac{1}{2\pi R_{esr} C} \quad (4.5)$$

and Figure 4.3 shows the typical frequency response if the system assuming that the output capacitor (C_o) is larger than the off-chip bypass capacitors (C_b).

As the system architecture is decided, the following stage is to analyze the stability issue induced from the several low frequency poles. The worst case stability condition, arises when the phase margin is at its lowest point, which occurs when the unit gain frequency is pushed to higher frequencies where parasitic poles reside. This happens when the load current is at its peak value. This is because the dominant pole (P_1) usually increases at a faster rate than the gain of the system decreases. "$R_{o\text{-}pass}$" decreases linearly with increasing current, $1/\lambda I_o$ where λ is the channel length modulation parameter of MOS devices. "$g_m R_{o\text{-}pass}$" decreases with the square root of the increasing current for an MOS device or stays constant for a bipolar transistor. The type and value of the output capacitor determine the location of P_1, P_2, P_3 and Z_1. Therefore, the permissible range of the value of ESR for a stable circuit is a function of load current and circuit characteristics.

Parasitic Pole Requirement

The parasitic pole of the system can be identified as P_3 and the internal poles of the error amplifier. These poles are required to be at high frequency, at least

greater than the unit gain frequency. The phase margin for the case where only one parasitic pole was at the vicinity of the unit gain frequency is at approximately 45°. Ensuring that P_3 is at high frequencies is an especially difficult task to undertake in a low current environment. The pole is defined by the large parasitic capacitance (C_{par}). By the way, the large size MOS device is usually utilized as the pass element to attain the high current condition. Therefore, C_{par} is usually very large. On the other hand, this node is the output of the error amplifier. To reach the high gain, this is a high impedance node (R_{oa}). The amplifier output impedance is always the function of the circuit topology, for example, single stage amplifier, folded cascode amplifier or two stage amplifier, etc. As a result, low quiescent current and frequency design issue have conflicting requirements that necessitate compromises.

Load Regulation Discussion

Load regulation performance (output resistance of the regulator, R_o) is a function of the open-loop gain (A_{ol}) if the system can be expressed as

$$R_O = \frac{\Delta V_{LDR}}{\Delta I_O} = \frac{R_{o-pass}}{1 + A_{ol}\beta} \quad (4.6)$$

where ΔV_{LDR} is the output voltage variation arising from a load current variation of ΔI_O, $R_{o\text{-}pass}$ is the output resistance of the pass device, and β is the feedback factor. Consequently, the regulator yields better load regulation performance as the open-loop gain increase. However, the gain is limited by the close-loop bandwidth of the system, equivalent to the open-loop unit gain frequency. The minimum unit

gain frequency is limited by the response time required by the system during transient load current variation. Furthermore, the unit gain frequency is also bounded at the high frequency range by the parasitic poles of the system, the internal poles of the amplifier and pole P_3. In particular, the worst case condition occurs when Z_1 is at low frequencies and P_2 is at high frequencies, which corresponds to the maximum value of ESR and the lowest bypass capacitance (C_b). Moreover, the pass element associated input capacitance is significantly large. This places a ceiling on the value of the amplifier output resistance (R_{oa}). The pass element usually needs to be a large size device to yield low drop-out voltages and high output current characteristics with limited voltage drive in a low voltage and low power environment. In short, load regulation is limited by the constrained open-loop gain of the system.

4.1.3 Transient Analysis

An important specification is the maximum allowable output voltage change for a full range transient load current step. The application determines how low this value should be. For instance, a relatively relaxed specification for the peak output voltage variation can be tolerated if the regulator is used to provide power to digital circuits, which inherently have high noise margin. However, this is not the case for many analog applications. Figure 4.4 shows the characteristic nature of the stimulus and the typical respective response for the typical linear regulator system.

The worst case time required for the loop to respond is specified by the maximum permissible output voltage variation (ΔV_{tr}), which is a function of the output capacitor (C_o), the electrical series resistance (ESR) of the output capacitor, the bypass capacitors (C_b), and the maximum load current ($I_{Load\text{-}max}$),

$$\Delta V_{tr-\max} \cong \frac{I_{Load-\max}}{C_o + C_b}\Delta t_1 + \Delta V_{esr} \quad (4.7)$$

$$\Delta t_1 \cong \frac{C_o + C_b}{I_{Load-\max}}[\Delta V_{tr-\max} - \Delta V_{esr}] \quad (4.8)$$

where ΔV_{esr} is the voltage variation resulting from the presence of the ESR of the output capacitor. The bypass capacitors (C_b) reduce the ESR effect. The duration Δt_1 is a function of the bandwidth, and furthermore it is also limited by the slew rate of the error amplifier associated with the parasitic capacitance C_{par} induced by the pass element. Therefore, Δt_1 can be approximated to be

$$\Delta t_1 \cong \frac{1}{BW_{close-loop}} + t_{slew} = \frac{1}{BW_{close-loop}} + C_{par}\frac{\Delta V}{I_{slew}} \quad (4.9)$$

where the $BW_{close\text{-}loop}$ is the close-loop bandwidth of the system, t_{slew} is the slew rate time associated with C_{par}, ΔV is the voltage variation at C_{par}, and I_{slew} is the slew rate limited current. If the I_{slew} is large enough, the bandwidth of the close-loop will dominate Δt_1.

Once the slew rate condition is terminated, the output voltage will settle to its final value.

$$\Delta V_2 \cong R_{o-reg} I_{Load-\max} \quad (4.10)$$

where $R_{o\text{-}reg}$ is the close loop output resistance of the regulator. According to the above, load regulation effect can be observed. The settling time (Δt_2) is dependent on the duration that the pass element charges the output loading capacitor and the phase margin of the open-loop frequency response.

In real word, the slew rate condition should be concerned. It typically occurs when load current step from zero to full scale. The behavior is dependent on the configuration of the output stage of the error amplifier and the output pass element.

Then, the output voltage variation (ΔV_3), whose magnitude is defined by the voltage charged on the capacitors and the voltage generated across the ESR of the output capacitor, is discussed. The momentary current supplied by the power device flows to the output capacitor (C_o) and the off-chip bypass capacitors. Therefore, the capacitors are charged and a temporary voltage drop is generated between R_{esr}. The transient voltage variation can be approximately expressed as

$$\Delta V_3 \cong \frac{I_{Load-\max}}{C_o + C_b}\Delta t_3 + \Delta V_{esr} \cong \frac{I_{Load-\max}}{C_o + C_b} \cdot \frac{1}{BW_{close-loop}} + \Delta V_{esr} \quad (4.11)$$

Finally, the output transistor is shut off, and then the output voltage will settle. During the period, the voltage variation (ΔV_4) can be approximated as

$$\Delta t_4 \cong \frac{C_o + C_b}{V_{ref} \big/ R_1}\Delta V_4 \quad (4.12)$$

, and therefore the pull-down current plays an important role. As a result, the additional off-chip bypass capacitors (low ESR capacitors) reduce the peak value

of $\Delta V_{tr\text{-}max}$ and ΔV_3. The reason why the they can decrease the transient peak value is the current supplied by the output capacitor (C_o) during transient condition is decreased as C_b is increased thereby exhibiting a lower voltage drop across R_{esr}. The remaining current is supplied by the bypass capacitors, which have negligible ESR voltage drops.

4.2 Circuit Blocks

In this section, each part of the linear regulator will be discussed. As the figure 4.1 shown, the system is composed of an error amplifier, a pass element, ratio resistors, and off-chip compensating capacitors. First, the design flow and the design consideration will be declared. According to the design goal, some topologies of the circuit are proposed. Finally, from the system view, some analog design technique will be brought up to enhance the performance of the linear regulator.

In this work, the nanodevice array supplies low power. Therefore, the design goal of the linear regulator is that the circuit could not consume too much power. The static power consumption should be as low as it can be. Besides, the nanodevice array supplies low voltage. Then, the supply voltage of the linear regulator must be low. In summary, the nanodevice array supplies low current and low voltage. The deign purpose is to attain the requirement.

Error Amplifier Design Issue

The specification of the error amplifier that are relevant to the regulator as

inferred from the previous discussion are: output resistance, gain, bandwidth, output slew rate current, output voltage swing and quiescent current. According to the low voltage application and the low current application, we should concern many aspects.

Many kinds of operational amplifiers can be used as the error amplifier, for example, the folded cascade operational amplifier (Figure 4.5), the telescopic amplifier (Figure 4.6), the single stage amplifier (Figure 4.7) and the two-stage amplifier (Figure 4.8). Due to the low voltage application, the stacked transistors should be minimized. Therefore, the telescopic operational amplifier is not suitable for this work. According to the low current limitation, the two stage operational amplifier can not reach the goal. Finally, the performance of the linear regulator is dominated by the loop gain. The gain of the error amplifier plays an important role, and the gain of the error amplifier should not too low. The single stage amplifier possesses the lowest gain among the above operational amplifier topologies. Thus, the folded cascade amplifier is adopted.

The Pass Device

Designing in a low voltage and low current environment provides difficult challenges that contradict performance and stability [23]. The pass device should provide large amounts of current while displaying low drop-out characteristics. The size of the transistor as the pass device must be large under low voltage condition. A large device is further demanded because voltage drive is reduced as a result of decreased input voltages. The phenomenon causes the parasitic pole P_3 to move to lower frequencies effectively deteriorating phase margin and compromising the stability of the system. In summary, the size of the pass device

must be large for increased current capabilities but restrained by stability and slew rate requirements in a low quiescent current and low voltage environment. In this work, the PMOS is used because the drop-out voltage between the input voltage and the output voltage should be minimized.

4.3 Simulation Results and Layout

The linear regulator was implemented by TSMC 2P4M 0.35um process. The simulation result of the error amplifier is shown as the table 4.1. At the lowest supply voltage case, the gain of the error amplifier is still about 62dB. The phase margin of the error amplifier is 78.8 in the worst case. The average current is about 30uA when the supply voltage is lowest. The size of the each MOS is shown in Figure 4.9. Figure 4.10 illustrates the bias circuit which provides the bias for the error amplifier.

Next, the simulation of the loop gain and phase margin was executed. The method to simulate the loop gain is shown as the Figure 4.12. The value of the inductor L is very large to confirm DC-signal short circuit and AC-signal open circuit. On the other hand, the value of the capacitor C is also very large to confirm DC-signal open circuit and AC-signal short circuit. Table 4.2 shows the simulation result of the loop gain and its phase margin. The loop gain is larger than 60dB within the desired current range (1mA~50mA). Meanwhile, the phase margin of the loop is about 80. The linear regulator would stable within the desired current range.

In turns, the transient response is considered. Figure 4.13 demonstrates the transient response of the linear regulator system. If the loading current varies

extremely from 0 mA to 50mA, the output voltage is still regulated at the voltage we want (1.3V). The peak of the transient voltage variation can be controlled under 50mV. The settling time of the linear regulator can be governed in 10us. The simulation result also proves the stability of the system.

Figure 4.14 shows the layout view of the linear regulator. The poly-2 is used as the resistor because of the lowest process variation quantity. The metal width of the power MOS should be notified. If it is too narrow, it would be melted because of the high current density.

4.4 Measurement Results

The overall measurement result is shown as Table 4.3. First, the situations of the output voltage with different power supply voltages were measured. In heavy load condition (loading current = 50 mA), the output voltage can be regulated between 1.291V and 1.217V as the Figure 4.15 shown. Figure 4.16 illustrates the measurement result of the output voltage with the lowest power supply voltages of this work 1.5V (@ loading current = 50mA). Figure 4.17 shows the measurement result of the output voltage with the highest power supply voltage of this work 3.3V (@ loading current = 50mA).

Then, we measure the different power supply voltages and the different loading current conditions. The outcome is shown as Figure 4.18. Under all of the cases, the output voltage can be regulated about 1.3V.

In summary, the overall specification of the linear regulator is illustrated as the table 4.3.However, the nanodevice array was measured as the Figure 4.18 shown, it just can supply 0.63nW. It is insufficient for the linear regulator to operate.

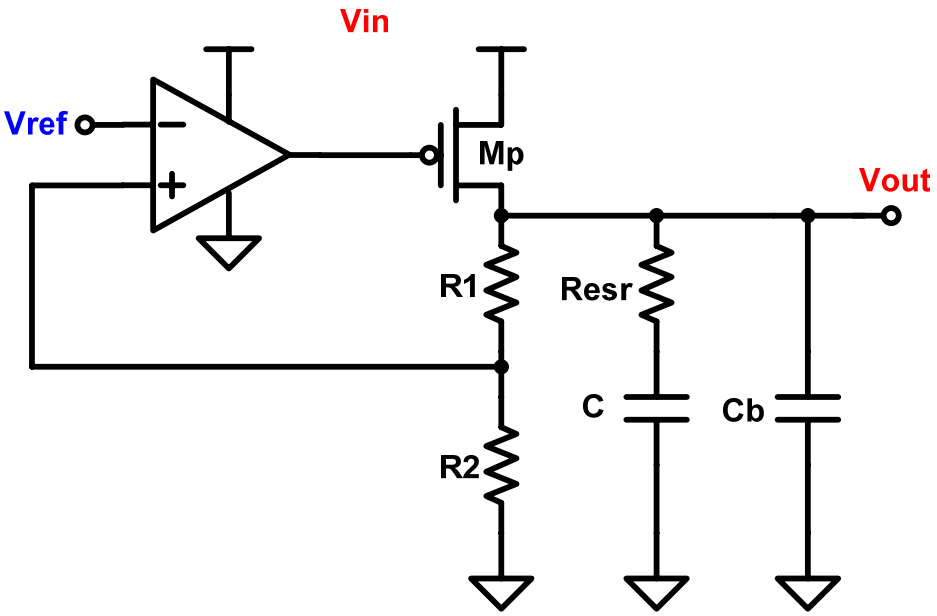


Figure 4.1 The linear regulator architecture

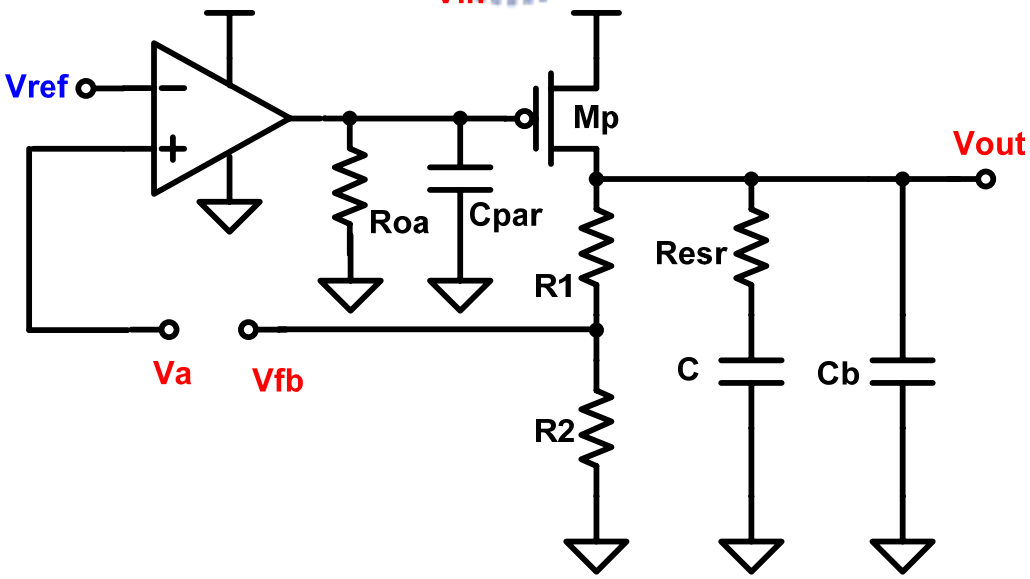


Figure 4.2 The System Model of the linear regulator

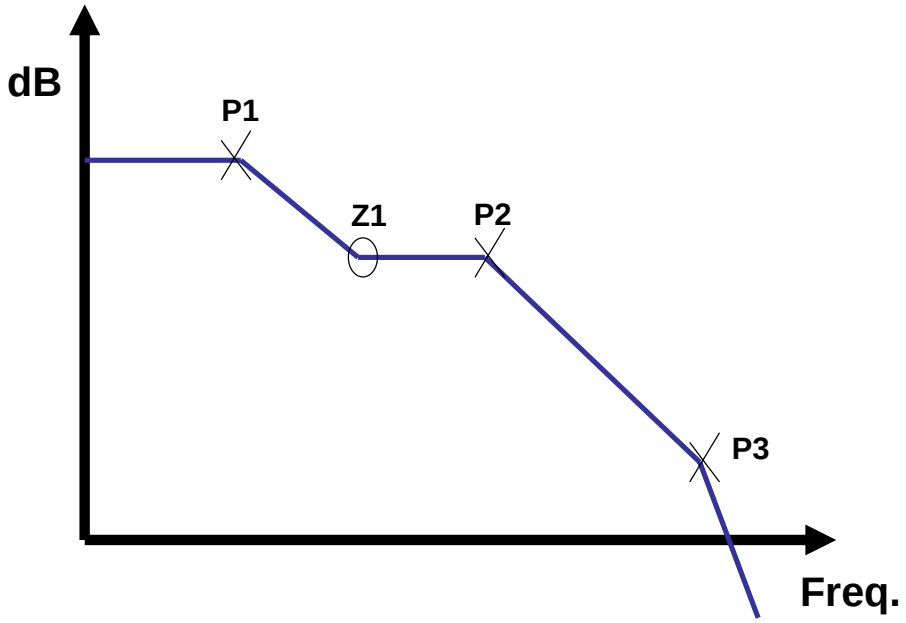


Figure 4.3 The frequency Response of the linear regulator

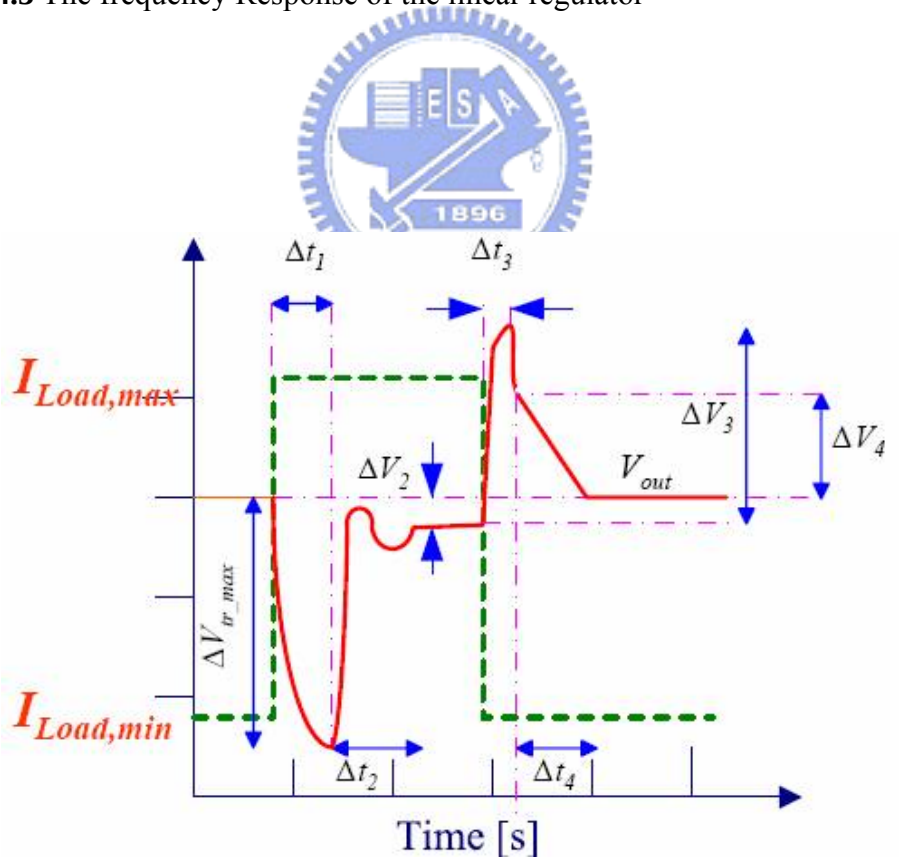


Figure 4.4 Typical linear regulator response

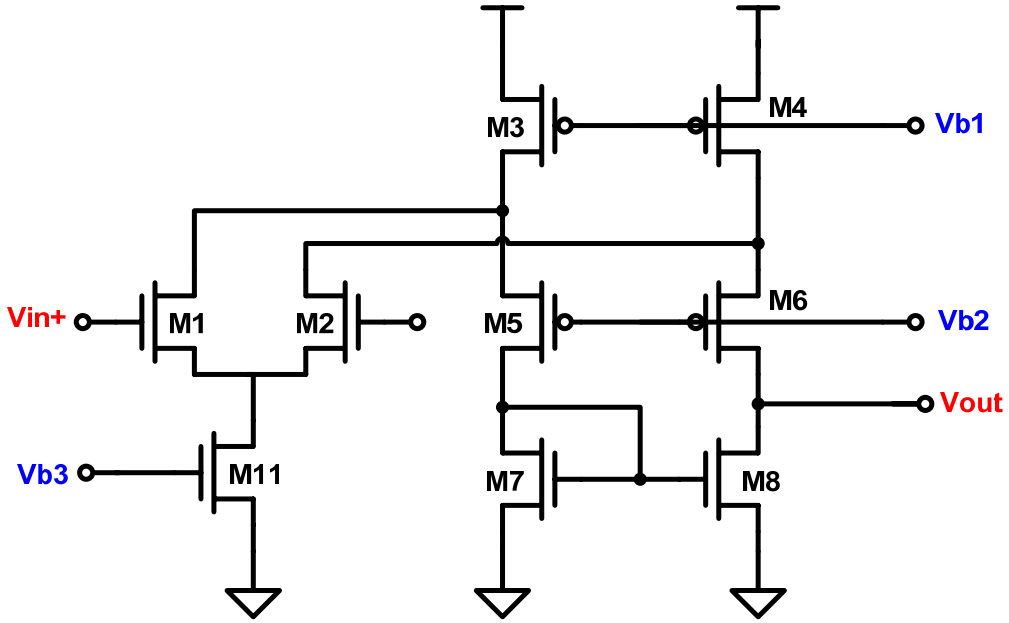


Figure 4.5 The folded cascode amplifier

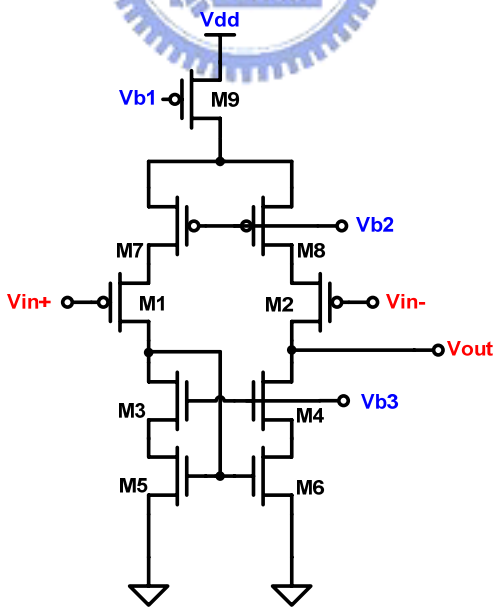


Figure 4.6 The telescopic amplifier

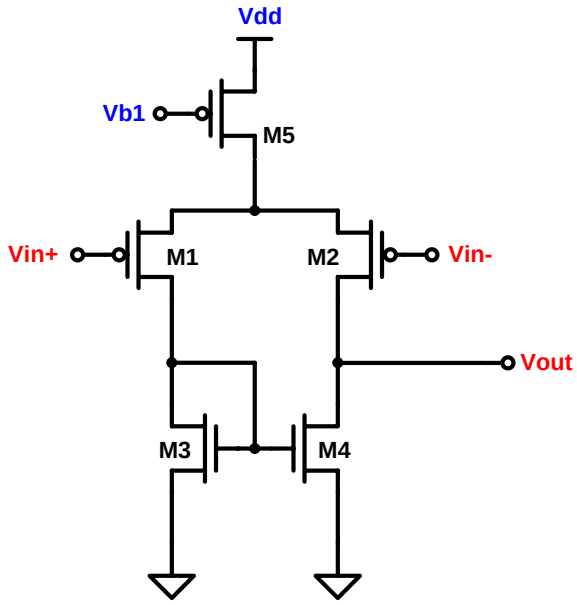


Figure 4.7 The single stage amplifier

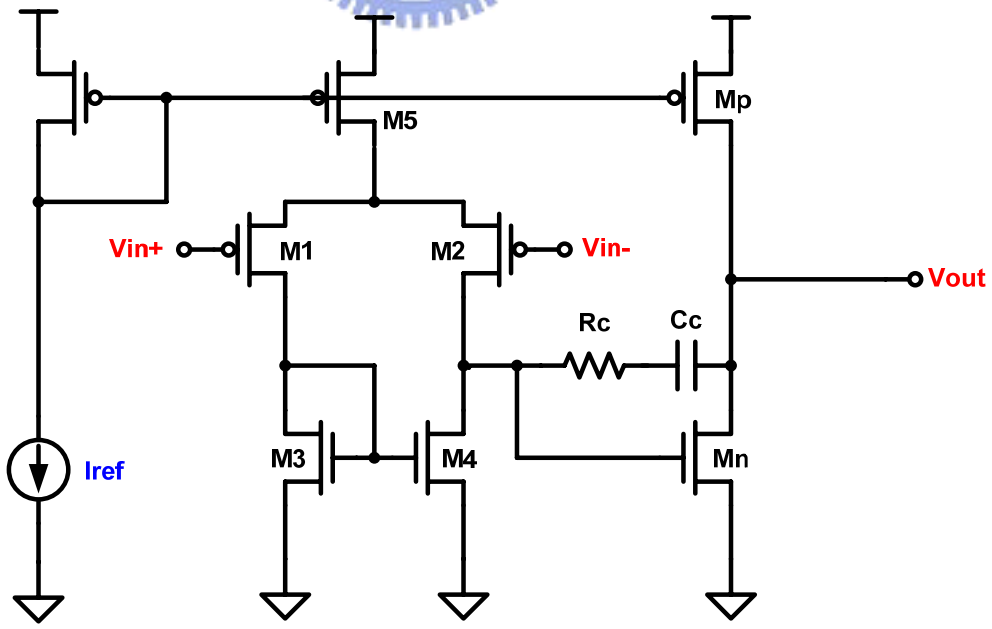
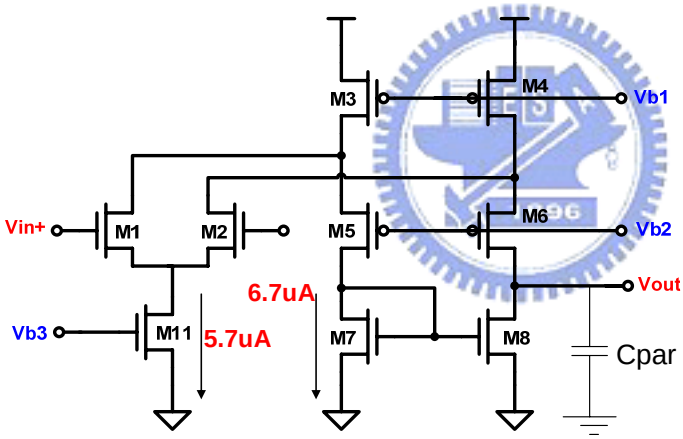


Figure 4.8 The two-stage amplifier

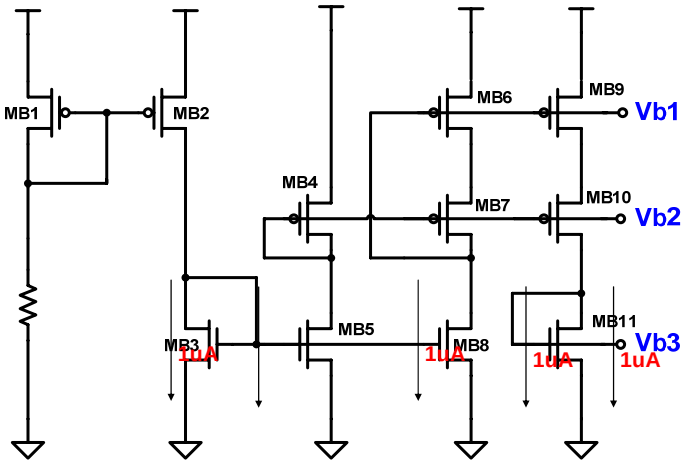
Power Supply	1.5V	2V	2.5V	3V	3.3V
Average Current	29.9 uA	55.19 uA	82.1 uA	110.3 uA	127.7 uA
Phase Margin	83.4	81.3	80	79.2	78.8
Gain	62.5 dB	64.6 dB	66.1 dB	67.1 dB	78.8 dB
Unit-Gain Frequency	3.94 Mhz	6.83 Mhz	9.53 Mhz	12 Mhz	13.5 Mhz

Table 4.1 The specification of the error amplifier



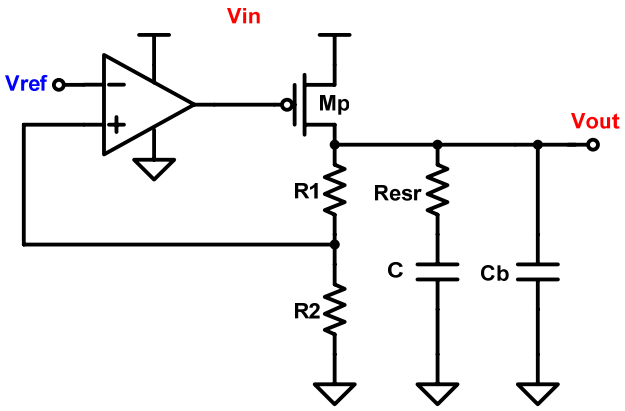
	W/L (um/um)
M1 M2	1/0.35 M=12
M3 M4	1/1 M=25
M5 M6	1/1 M=36
M7 M8	1/4 M=6
M11	1/3 M=12

Figure 4.9 The error amplifier



	W/L (um/um)
MB1	1/2 M=1
MB2	1/2 M=1
MB3	1/2 M=1
MB4	1/2 M=1
MB5	1/2 M=1
MB6	1/1 M=2
MB7	1/1 M=3
MB8	1/2 M=1
MB9	1/1 M=2
MB10	1/1 M=3
MB11	1/3 M=1
R	500k ohm

Figure 4.10 The bias circuit



	W/L (um/um)
Mp	10/0.35 M=1200
R1	3k
R2	36k
C	10uF
Resr	1 (0~5)
Cb	0.1uF

Figure 4.11 The linear regulator

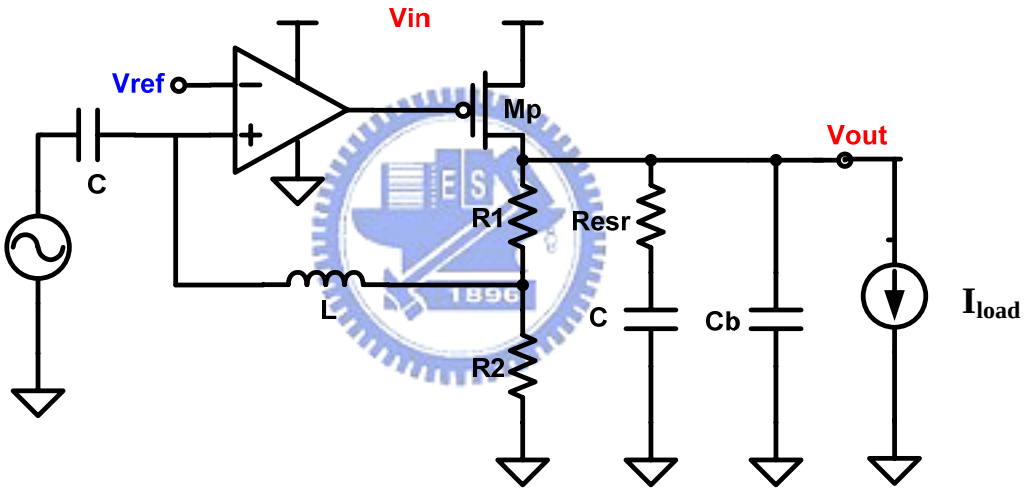


Figure 4.12 The simulation method of the loop gain

Load Current	1mA	10mA	20mA	30mA	40mA	50mA
Loop Gain	83.12dB	80.18 dB	75 dB	69.4 dB	64.6 dB	60 dB
Phase Margin	74.6	79.12	78.5	78.2	78.6	79.5

Table 4.2 The specification of the feedback loop

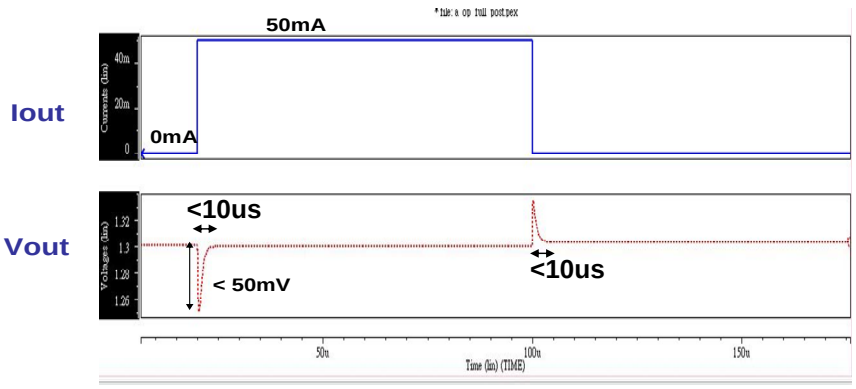


Figure 4.13 The transient response of the linear regulator

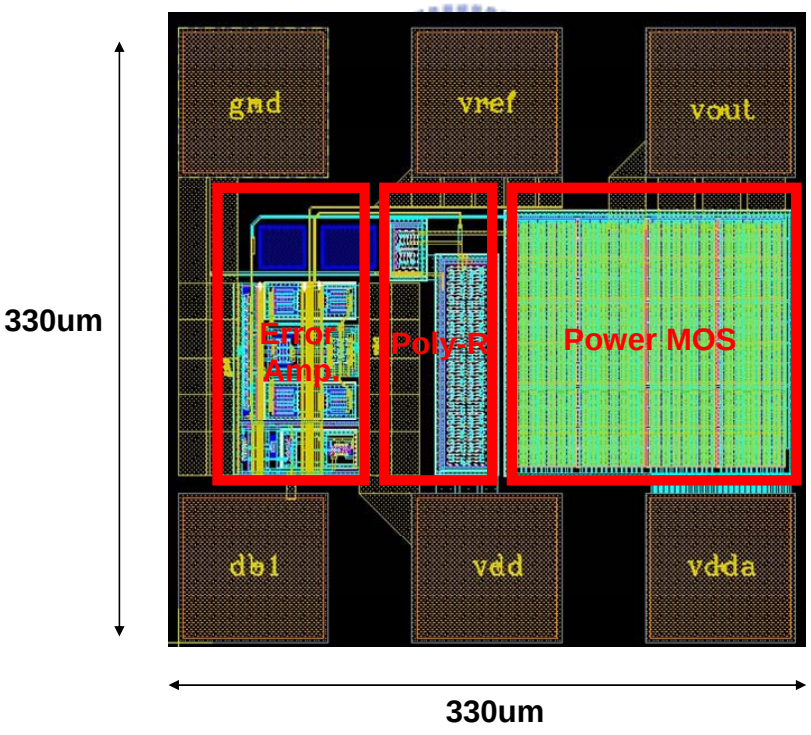


Figure 4.14 The chip layout view

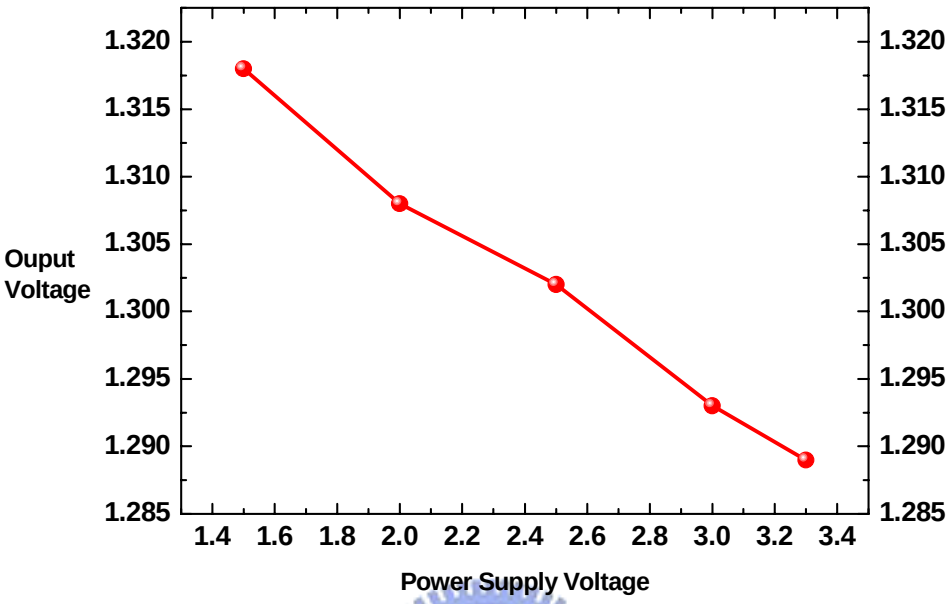


Figure 4.15 The measurement result of the output voltage with different power supply voltages (@ loading current = 50mA)

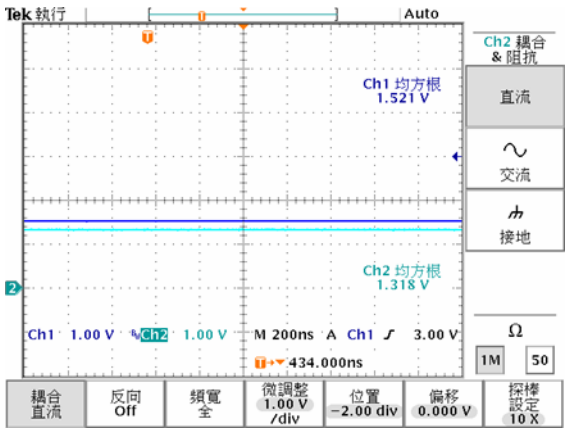


Figure 4.16 The measurement result of the output voltage with the lowest power supply voltages of this work 1.5V (@ loading current = 50mA)

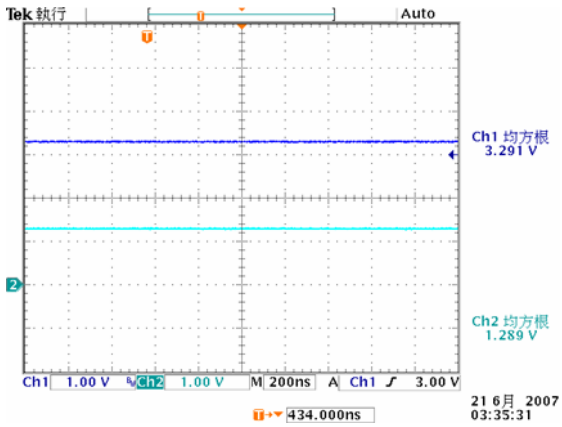


Figure 4.17 The measurement result of the output voltage with the highest power supply voltage of this work 3.3V (@ loading current = 50mA)

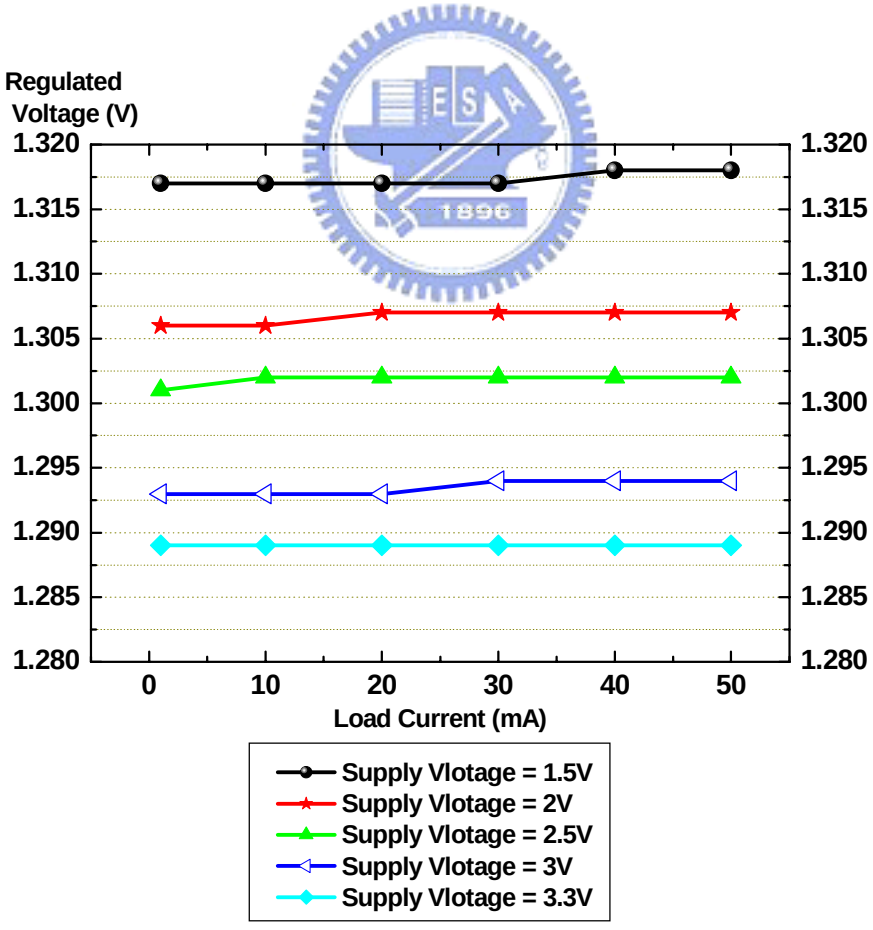


Figure 4.18 The measurement result of the output voltages with different power

supply voltages and loading current

	Simulation	Measurement
Supply Input Voltage	**1.5v~3.3v**	**1.5V~3.3V**
Output Voltage	**1.3v**	**1.291V~1.307V**
Chip Area	**330um * 330um**	
Line Regulation	**< 5.1 mV/V**	**< 8.33mV/V**
Load Regulation	**< 0.16 mV/mA**	**< 0.21mV/mA**
Output Current	**< 50mA**	**< 50mA**
Accuracy	**< 0.73%**	**< 1.2%**

Table 4.3 The specification comparison of the simulation and measurement result

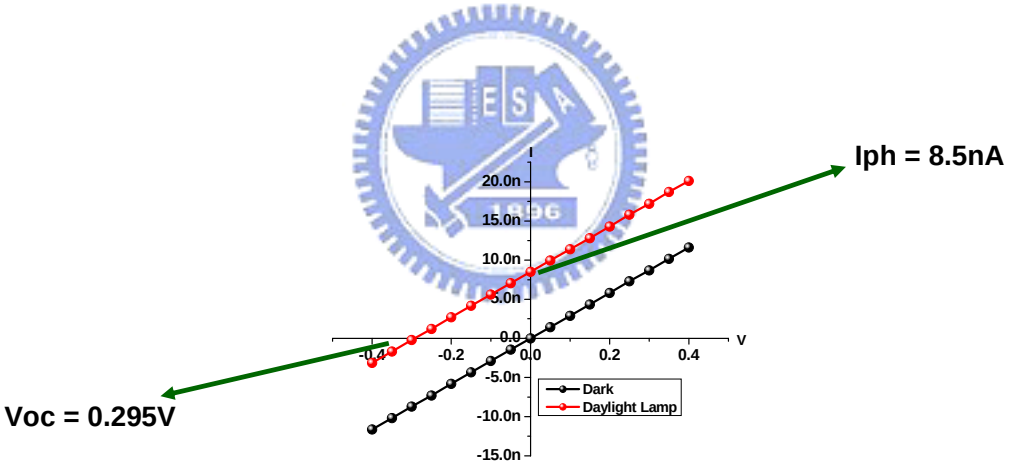


Figure 4.18 The measurement result of the nanodevice array

CHAPTER 5
CONCLUSIONS AND FITURE WORK

5.1 CONCLUTIONS

In this work, the function of PDDA layer was to improve the quantum yield of CdSe QDs. The proposed multi-layere photo-sensing nanodevices were fabricated by integrating CdSe QDs and Au NPs on the silicon substrate. The fabrication of the nanodevices were designed using the "dip-and-wash" procedure and the dip time was increased to 24 hours per layer which is sufficient to deposit the high density structure for the nanodevices. To control and assemble CdSe QDs and Au NPs into well-defined nanostructure, we utilized the ionic interaction between CdSe QDs / Au NPs and silicon oxide substrate. First, the silicon chip was modified by N-[3-(trimethoxysilyl) propyl] ethylene diamine (TMSPED) to make the silicon oxide substrate provide amino groups ($-NH3^{+}$). Subsequently, Citrate-capped Au NPs (~15 nm)、PDDA-capped and AET-capped CdSe/ZnS NPs (~5 nm) was self-assembled layer-by-layer, alternately, between the electrodes. The nanodevice structure after each layer was formed on the silicon oxide substrate was observed by SEM images. UV-visible and PL intensity spectra were used to verify the construction of each layer on quartz glass substrate. Finally, the electrical properties of the photo-sensing nanodevices were observed. The electrodes sets, 30 μm / 5 μm, 30 μm / 15 μm, 30 μm / 30 μm, 60 μm / 5 μm, 60 μm / 15 μm, 60 μm / 30 μm, 90 μm / 5 μm, 90 μm / 15 μm and 90 μm / 30 μm (width / length) were employed for I-V measurement. The laser diodes of 375 nm and the daylight lamp were used as light sources for

nanodevice photo-excitation. For the nanodevice composed of Au NPs and CdSe QDs, there was a constant increment of photocurrent after illumination throughout the applied voltage biases, which resembles the characteristics of a photodiode. Furthermore, the three-dimensional "nano-Schottky-diode" arrays model was proposed and used to explain the photo-sensing mechanisms, and the high solar cell efficiency can be obtained based on our ideal inference.

In this work, under the 0.16mW/cm^3 illumination, the best solar cell efficiency is 0.67% (24-layered PDDA-CdSe nanodevice with 60um in width and 5um in length). The maximum photocurrent is 1.2nA (24-layered PDDA-CdSe nanodevice, with 90um in width and 5um in length). Then, the maximum PVD ($1.503*10^{-23}$A/nm^3) and Power Volume Density ($2.45*10^{-25}$W/nm^3) happen when the device dimension is 90um in width, 5um in length and 8-layered nanostructure. The power conversion efficiency can achieve 38.1% based in our ideal interference (26-layered PDDA-CdSe nanodevice with 65nm in length).

Au / CdSe nano-Schottky diodes and resistors array performance trend

（1）For the same length / number of layer and excitation source

In dark: Width ↑ -> Conductivity ↑

Under illumination: Width ↑ -> Photocurrent ↑, PVD ↑, Efficiency (constant)

Power Volume Density ↑

（2）For the same width / number of layer and excitation source

In dark: Length ↑ -> Conductivity ↓

Under illumination: Length ↑ -> Photocurrent ↓ , PVD ↓, Efficiency ↓

Power Volume Density ↓

（3）For the same width / length and excitation source

In dark: number of layer ↑ -> Conductivity ↑

Under illumination: number of layer ↑ -> Photocurrent ↑ , Efficiency ↑

However, 8-layered nanodevice has best PVD and Power Volume Density.

（4）Solar cell efficiency = 38.1% (ideal inference, not measurement data)

in 26-layered nanodevice with 65nm in length.

5.2 FUTURE WORK

The future works of this project can be divided into five parts:

（1）In this project, we used approximately 5 nm CdSe QDs to construct the nanodevices. As we know that CdSe NPs have the size dependent optical and electrical properties, the band gap increases as the particle size decreases, shifting the absorption and luminescence spectra to the blue. The further research on CdSe QDs is to synthesize the QDs of various sizes and then mix to each other. This goal is to achieve a board band absorption spectrum.

（2）Dye sensitization of mesoscopic TiO_2 has been widely used in solar cells—in which the sunlight creates bound electrons and holes—excitons—that travel as a unit and separate only after reaching some material boundary, resulting a board band absorption spectrum, and then raise the photo-to-charge carrier generation efficiency. In our future work, maybe we can employ charged- laser dyes (Cy2, Cy3, Cy5, FTIC, ...etc) to fill the gap between the assembled-NPs and reduce the probability of defect between the electrodes, consequently, construct more compact structure and achieve a board band absorption spectrum to obtain higher power conversion

efficiency.

（3）Utilize the diversity of optical and electrical properties of different QDs to construct other functional photo-sensing nanodevices based on the developed process (ionic interaction system). Therefore, it is important to cooperate with Professor Teng-Ming Chen's inorganic synthesis laboratory to develop more metal NPs (such as Cu NPs and Ag NPs) and semiconductor QDs (such as CdTe NPs and TiO_2 NPs). And then we can construct and measure different nanostructures composed of various NPs. In the nanodevice structure, the metal NPs are an important role to enhance the conductivity on the nanodevice and connect the CdSe QDs. To improve the efficiency of large area, the size and sharp of metal NPs can be turned to enhance the density and conductivity of the metal. In the CdSe/ZnS NPs, we can use the photo-activated CdSe/ZnS NPs to enhance the quantum yield and photoluminescence.

（4）During the fabrication process, the defect between the electrodes is an very important problem. In order to reduce the probability of defect between the electrodes, the construction procedure must conduct carefully. However, the key point is the bonding between NPs and silicon oxide substrate. In this work, the chip was immersed in a 10% TMSPED/methanol solution that has two amino groups on one alkyl chain. The two amino groups caused the alkyl chain to repulse with each other, and consequently the distance between TMSPED molecules was relatively large. In order to increase the surface density of amino groups on the substrate, instead of modification by TMSPED, we used the APTES solution to modify the silicon oxide substrate with positive charges that has one amino group on one alkyl chain. Therefore, the repulsive force between the alkyl chains can be reduced significantly. To improve the compact structure, we can turn the fabrication conditions, such as low concentration QDs and low temperature, to build the layer-by-layer on the silicon

oxide substrate.

（5）In this work, we have demonstrated the photo-sensing property of the nanodevices. The further works are to incorporate these inorganic nanodevices into nano-electronics system, like utilizing the current photo-sensing nanodevice based on NPs to construct two-dimensional photo-sensing system, a sensitive and multicolored photo-sensing system based on NPs on the silicon chip. Further applications and improvement on the proposed nanodevices are ongoing.

(6) Standard solar simulator measurement is integrated in the research to ensure the correct solar cell efficiency.

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論　　文：

先進奈米元件結構於光感測與太陽能電池之研究

The Research of Advanced Nanodevice Structures for Photo-Sensing and Solar Cell Application