

# 高介電常數介電質於金屬-絕緣層-金屬電容 之電性研究

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隨著元件尺寸的減縮，閘極厚度必須降低以維持電容值和驅動電流。由國際半導體技術藍圖，我們知道在 1.5 奈米製程以下，降低介電質厚度將使得漏電流呈指數級增加。然而，高介電常數介電質的應用將是一種有效防止漏電流呈指數級增加的可能解決方法。

在本篇論文中，我們研究使用高介電常數介電質的金屬-絕緣體-金屬電容。高電容密度、低電容電壓係數、低漏電流和簡單單一介電質製作都是使用此高介電常數介電質 (TiTaO) 之優點。

藉由使用高介電常數介電質 (TiTaO) 和高功函數的鎵電極，我們達成滿足國際半導體技術藍圖所需求性能的高性能金屬-絕緣體-金屬電容。

# **Study on Electrical Characteristics of High- $\kappa$ Metal-Insulator-Metal Capacitors**

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## **Abstract**

With the scale-down of device size, the gate thickness has to decrease to maintain the capacitance value and drive current levels. By ITRS, we know that decreasing dielectric thickness will increase the leakage current exponentially below 1.5 nm. However, high- $\kappa$  materials are much preferred as a possible solution that prevent the exponential increase of the gate leakage current.

In this thesis, we study the metal-insulator-metal capacitors using high- $\kappa$  dielectrics. The high capacitance density, low voltage coefficients of capacitance, low leakage current and simple single dielectric process are the merits using the novel high- $\kappa$  TiTaO dielectric.

By using the high- $\kappa$  TiTaO dielectric and the high work-function Ir electrode, we have exhibited a high performance MIM capacitor that meets the ITRS roadmap requirements for analog capacitors.

## 誌 謝

感謝我的指導教授-荊鳳德教授，給予我專業的知識與正確的研究方法，也熱心的指導與協助，培養我積極的研究精神，讓我建立非常深厚的研究基礎與觀念；在為人處事方面，教導學生努力不懈的態度，要能不斷的充實自己，增長智慧。相信這短短兩年所得，在未來也可以充分應用和實踐。

亦感謝實驗室的學長-國誠學長、淳護學長，感謝你們教導儀器的使用、實驗的方法，遭遇問題時，也給予我適切的指導與意見。感謝軍宏學長、彬舫學長、建宏學長、存甫學長、學人學長、靖謙學長，感謝你們的照顧關心與指導，你們讓實驗室更加茁壯、發展。也感謝諸多同學及學弟妹們-冠麟、懿範、偉倫、哲緯……等，感謝你們在生活上的支持與勉勵，與你們相處的非常愉快，實驗室生活有了你們，更加多采多姿。

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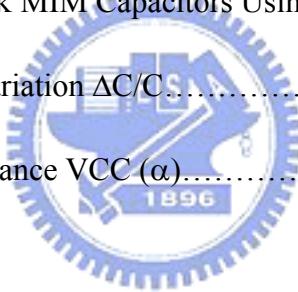
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# Table Caption

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## Chapter 2

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# Figure Caption

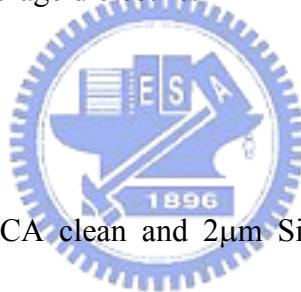
## Chapter 1

Fig. 1-1 ITRS 2005 Trench DRAM Roadmap (Known solutions exist through 57 nm generation.)

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