

高介電常數介電質於金屬-絕緣層-金屬電容 之電性研究

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隨著元件尺寸的減縮，閘極厚度必須降低以維持電容值和驅動電流。由國際半導體技術藍圖，我們知道在 1.5 奈米製程以下，降低介電質厚度將使得漏電流呈指數級增加。然而，高介電常數介電質的應用將是一種有效防止漏電流呈指數級增加的可能解決方法。

在本篇論文中，我們研究使用高介電常數介電質的金屬-絕緣體-金屬電容。高電容密度、低電容電壓係數、低漏電流和簡單單一介電質製作都是使用此高介電常數介電質 (TiTaO) 之優點。

藉由使用高介電常數介電質 (TiTaO) 和高功函數的銦電極，我們達成滿足國際半導體技術藍圖所需求性能的高性能金屬-絕緣體-金屬電容。


Study on Electrical Characteristics of High- κ Metal-Insulator-Metal Capacitors

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Abstract



With the scale-down of device size, the gate thickness has to decrease to maintain the capacitance value and drive current levels. By ITRS, we know that decreasing dielectric thickness will increase the leakage current exponentially below 1.5 nm. However, high- κ materials are much preferred as a possible solution that prevent the exponential increase of the gate leakage current.

In this thesis, we study the metal-insulator-metal capacitors using high- κ dielectrics. The high capacitance density, low voltage coefficients of capacitance, low leakage current and simple single dielectric process are the merits using the novel high- κ TiTaO dielectric.

By using the high- κ TiTaO dielectric and the high work-function Ir electrode, we have exhibited a high performance MIM capacitor that meets the ITRS roadmap requirements for analog capacitors.

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Chapter 2 The Research and Applications of High- κ Dielectrics

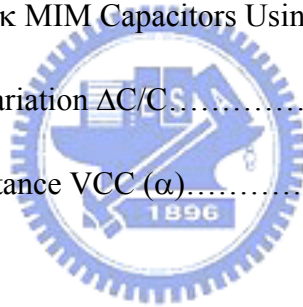
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Chapter 1

Table 2-1 Materials properties of high- κ dielectrics.

Chapter 2

Table 5-1 Comparison of various high- κ capacitors.



Figure Caption

Chapter 1

Fig. 1-1 ITRS 2005 Trench DRAM Roadmap (Known solutions exist through 57 nm generation.)

Fig. 1-2 ITRS 2005 Trench DRAM Roadmap (Red brick wall moved to 28 nm, MIM option for ≤ 50 nm, only option for ≤ 35 nm.)

Fig. 1-3 Several variations of dielectric structures have been attempted in MIM capacitors, such as laminate, sandwich and stack structures.

Fig. 1-4 Scaling of DRAM storage dielectric.



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Fig. 3-5 Ir or Al was deposited on the dielectrics and patterned to form the top capacitor electrode (step 2).

Fig. 3-6 Ir or Al was deposited on the dielectrics and patterned to form the top capacitor electrode (step 3).

Chapter 4

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(B) TiO₂ after annealing at 400°C in O₂ for 10min and N₂ ambient for 30 min.

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(D) TiTaO after annealing at 400°C in O₂ for 10 min and N₂ ambient for 30min.

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Fig. 4-5 The C-V characteristics. High capacitance density of 14.3 fF/μm² is measured.

Fig. 4-6 The C-V characteristics. High capacitance density of 23 fF/μm² is measured.

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