Chapter 1
Introduction

1.1 Background

To meet the requirements for present and future electrical products, technologies and devices of IC industry develop extremely, especially the small-size and high-speed chips. The transistor scaling [1] is driven by industry pressures to increase the chip performance and density at a reduced cost per function [2]. The scaling of the conventional metal-oxide-semiconductor field effect transistor (MOSFET) beyond the 45-nm technology node will be extremely challenging [3].Very high channel doping concentration and very thin gate oxides are needed to control the short channel effect in the nanometer conventional MOSFET. However, very high channel doping concentration reduces carrier mobility, hampering the device performance and leading to a high band-to-band drain leakage current. It is accompanied by an unacceptably high gate leakage current through a very thin gate oxide [4]. Consequently, one is no longer able to improve the performance of the conventional MOSFET by simply increasing the gate capacitance in order to improve the gate overdrive. Industry is actively pursuing solutions to these problems which are seen in the introduction of high-κ gate dielectrics to reduce the gate leakage and novel strained channel materials to boost the device

performance. Such measures may be able to extend the useful life of the conventional MOSFET for one or two generations but more radical solutions are needed beyond the 45-nm technology node. There is a consensus that the bulk MOSFET will be replaced by an ultra-thin body (UTB) silicon on insulator (SOI) and/or a double-gate (DG) MOSFET architecture, such devices tolerate thicker gate oxides and lower channel doping. They allow scaling to sub-10 nm without substantial loss of performance and have better electrostatic integrities. At these scales, their performance could be further increased by the introduction of new channel, gate dielectric and gate materials. However, the transition with new device architectures and the introduction of new materials is a challenging task for industry, further emphasizing the role of modeling and simulation in the areas of technology and device design. Modeling is tasked with screening the endless combinations of new device architectures and new materials to optimize performance thus cutting the cost of technology development to industry. The prediction of the behavior of the next generation of CMOS devices will also be extremely beneficial to the design community which has to cope with an increasing number of changes to device topology and behavior. Unfortunately, the present generation of models and simulation tools, which have been developed over the years to support the design of the conventional Si/SiO_2 transistor, cannot cope with the new device architectures and materials.

From now on the introduction of at least one technology booster will be needed at each ITRS technology node in order to maintain the required performance of the scaled MOSFET [5]. These boosters include the introduction of strain and novel channel materials [6], the introduction of high- κ gate stacks [3], the introduction of metal gates [3] and the introduction of novel transistor architectures [7]-[8].

For the forthcoming technology nodes, strain alone may not be sufficient to sustain the required performance and to compensate for the potential drive current loss associated with the introduction of high-κ gate dielectrics [9].

The use of high-κ materials allows the achievement of a similar or even lesser equivalent SiO_2 thickness (EOT) at a larger physical thickness of the gate dielectric, substantially reducing the gate tunneling current. However, a serious drawback of the high-κ MOSFET is the degradation of carrier mobility in the channel. This is partially related to the significant number of trapped and fixed interface charges, a consequence of the immaturity of the current high-κ growth technology.

These high-κ materials, so-called because of their high dielectric constant (k), can be made much thicker than SiO_2 while achieving the same gate capacitance - the ability to turn a gate on and off, allowing it to process data. As the thickness scales below 2nm, leakage currents due to tunneling increase drastically, leading to unwieldy power consumption and reduce device reliability. Replacing the silicon dioxide gate dielectric

with a high-κ material allows increased gate capacitance without the concomitant leakage effects.

In order to implement metal/high-κ technology at the 45-nm node, slated by the ITRS for initial volume production in 2010, metal/high-κ devices must perform well in many areas like mobility, reliability and threshold voltage (V_{th}) controllability.

Fig. 1-2 show ITRS 2005 Trench DRAM Roadmap.

1.2 Motivation

Dynamic random access memory (DRAM) is the most common kind of random access memory (RAM) for personal computers and workstations. The network of electrically-charged points in which a computer stores quickly accessible data in the form of 0s and 1s is called memory. Random access means that the PC processor can access any part of the memory directly rather than having to proceed sequentially from some starting place. DRAM is dynamic in that, unlike static RAM (SRAM), it needs to have its storage cells refreshed or given a new electronic charge at few milliseconds. Static RAM does not need refreshing because it operates on the principle of moving current that is switched in one of two directions rather than a storage cell that holds a charge in place. Static RAM is generally used for cache memory, which can be accessed more quickly than DRAM.

DRAM stores each bit in a storage cell consisting of a capacitor and a transistor. Capacitors tend to lose their charge rather quickly; thus, the need for recharging.

The architecture, materials choice and process technology for stacked-capacitors in embedded-DRAM applications are a crucial concern for each new technology node.

Capacitor technology is transitioning from the early days of planar PIS (poly/insulator/silicon) capacitors to the MIM (metal/insulator/metal) capacitors used for 65-nm technology node.

Thus, in this work we combine technologies of high-κ dielectrics and MIM capacitor structures in the DRAM process.

1.3 The Structures and Characteristics of MIM Capacitors

A typical process flow for MIM capacitor fabrication includes capacitor opening patterning, bottom electrode deposition, bottom electrode chemical mechanical planarization (CMP), dielectric layer deposition, and top electrode deposition and patterning. Normally, high dielectric constant (k) dielectric materials are used as the insulating dielectric layer between the electrodes.

The electrodes of a MIM capacitor are fabricated using metals such as TiN, TaN, WN, etc., which are deposited using CVD (chemical vapor deposition), ALD (atomic

layer deposition) or MOCVD (metal organic chemical vapor deposition) methods. MIM capacitors used for logic-friendly embedded DRAM features require a low-temperature electrode deposition process (typically less than about 450 degrees C).

To satisfy the requirements of leakage current and voltage linearity, several variations of dielectric structures with two dielectrics have been attempted in MIM capacitors, such as laminate [10], sandwich [11] and stack structures [12], as shown in Fig. 1-3.

The advantages of MIM Capacitors are listed as follows:

(1) Lower parasitic resistance in storage nodes.

(2) Lower temperature process.

(3) Higher stored charge per unit area with high-κ dielectrics.

(4) Enables lower aspect ratio structures.

Therefore, MIM capacitors are especially suitable for mass production in semiconductor fabrication processes.

1.4 The Applications of MIM Capacitors Technology

Integration of passive components such as capacitors into semiconductor devices is an enabling technology that drives higher degree of system-level integration for portable communication devices. The miniaturization and reduction in the number of components in wireless systems allows lower cost, greater functionality, higher performance and increased reliability.

In the conventional MIS structure, metal-insulator-Si-substrate has been used over a long period of time. There are many studies about high-κ on Si-substrate. Comparing with SiO_2, the most benefit for high-κ gate dielectrics is leakage current density reduction by several orders of magnitude at the same EOT. However, in the point of view of device performance, a suitable gate dielectric candidate should also meet the other requirements, such as high thermal stability, high carrier mobility, small oxide charges, and good stress immunity and CMOS compatible. Different from semiconductor (Si-substrate), metal has more carriers and is more conductive.

Therefore, MIM structure (metal-insulator-metal) can reduce contact resistance and raise storage charge comparing to MIS structure. MIM capacitors are integrated in the back end part of process flow. The maximum temperature of deposition is restricted by the thermal budget of back end processes.

In recent years, capacitors are fabricated by using metal-insulator-metal (MIM)

structure and using silicon oxide and silicon nitride, deposited using plasma-enhanced chemical vapor deposition (PECVD), as the dielectrics of MIM capacitors. However, the capacitance density is limited by low dielectric constant values. Hence, MIM capacitor processes need to be developed that can provide higher capacitance density and are compatible with IC processing. Therefore, adoption of high-κ material is a very efficient way to increase the capacitance density [13].

An MIM capacitor has metal plates which are usually formed on the metal conductors of the interconnect layers. Because metal fabrication is required for the conductors of the interconnect layers, the simultaneous or near-simultaneous formation of the metal capacitor plates is readily accomplished without significant additional process steps and manufacturing costs.

MIM capacitors are very valuable in many applications of semiconductor technology. For example, MIM technology can be used in RF circuits, analog ICs, high power microprocessor units (MPUs), and DRAM cells.

High-κ metal-insulator-metal (MIM) capacitors are receiving great attention in RF/analog circuit applications due to high capacitance density [14]–[20]. Besides, MIM capacitors are used for impedance matching and DC filtering and occupied a large portion of the circuit area.

MIM structures are also used in embedded DRAM (eDRAM) technology for

multi-functional SOC application. DRAM technology with its 1-transistor/1-capacitor concept has long been at the leading edge of integrated circuit miniaturization. DRAM capacitor scaling has played a central role in this effort, as shown in fig. 1-4. In order to assure sufficient data retention time, a charge storage capacitance of 25-35 fF/cell and cell leakage currents <1 fA/cell are required and have to be maintained over the coming technology generations.

As DRAM density increasing, devices shrinkage and higher charge storage is inevitable. It is hard for conventional MIS structure to meet the requirements, so MIM structure is expected to apply in trench DRAM process. Therefore, we are wondering if high-κ material interacts with a metal electrode. If high-κ material interacts with a metal electrode, there will be an interfacial layer between high-κ material and metal electrode. That will change the property of the whole film, such as interface roughness, interface stress, electron barrier height, thermal stability, etc..

For DRAM stacked capacitors, metal-insulator-metal (MIM) structures with high-κ dielectrics are now required to meet capacitance requirements. Beyond 50nm (2009), a new dielectric material with a dielectric constant >60 will be required. Embedded DRAM in SOC applications will drive several integration challenges. One of those challenges is matching the ground rules required for the deep contacts around the stacked capacitor with the contact ground rules for the logic device.

The need for advanced capacitor materials in the DRAM trench capacitor is delayed relative to the stacked capacitor by only a few years. Some high-κ materials are currently being used in a silicon-insulator-silicon (SIS) structure for DRAM trench capacitors, but a metal-top electrode will be needed in 2007 and a full MIM structure with high-κ dielectric may be needed in 2009.

EDRAM technology has the significant advantages in terms of performance, area, and power consumption by combining a high bandwidth DRAM macro with logic/analog circuits on the same chip[21]-[22]. However, the process gap between commodity DRAM and logic make it difficult to manufacture highly reliable eDRAM with low cost and high yield.

High density, high speed and low power memory continues to be required for integration into logic chips for applications such as networking, multimedia handhelds, gaming consoles and high definition television. Embedded DRAM today continues to be made in optimized trench capacitor technologies, and in simplified cells designed to reduce the process adders to the CMOS logic processes.

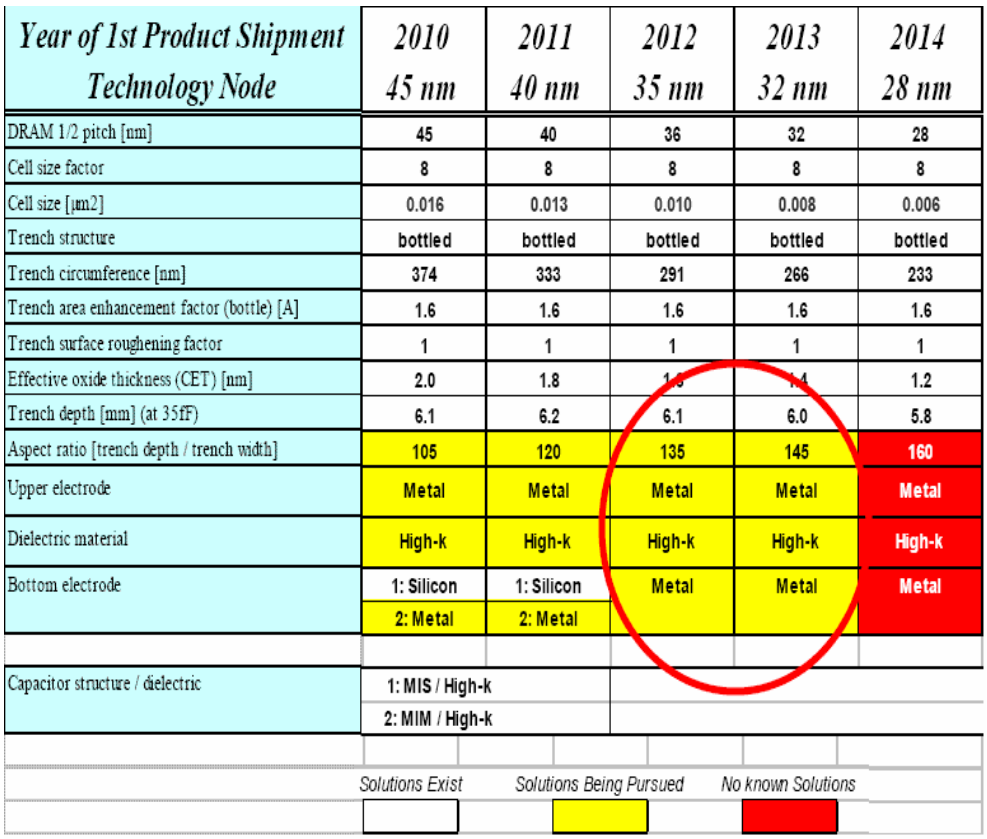
Therefore, the technology challenge is the required higher capacitance density, lower leakage current and simplified integration process for multi-functional SOC application.

To reduce the cell area and cost, the capacitor density should be higher. Because

the capacitor density in MIM device is equal to $\varepsilon_0\kappa/t_d$, increasing dielectric constant (κ) of metal-oxide and reducing the dielectric thickness (t_d) are the methods to increase the capacitor density. However, the using high-κ dielectric is preferred because the reducing t_d will increase leakage current density of the capacitor and the loss tangent exponentially due to electron tunneling.

Year of 1st Product Shipment / *Technology Node*	*2004* / *90 nm*	*2005* / *80 nm*	*2006* / *70 nm*	*2007* / *65 nm*	*2008* / *57 nm*
DRAM 1/2 pitch [nm]	90	80	70	65	57
Cell size factor	8	8	8	8	8
Cell size [µm2]	0.065	0.051	0.039	0.034	0.026
Trench structure	bottled	bottled	bottled	bottled	bottled
Trench circumference [nm]	748	665	582	540	474
Trench area enhancement factor (bottle) [A]	1.6	1.6	1.6	1.6	1.6
Trench surface roughening factor	1.3	1.25	1.25	1.2	1
Effective oxide thickness (CET) [nm]	5.2	4.4	4.3	3.9	2.8
Trench depth [mm] (at 35fF)	6.4	6.2	6.8	6.8	6.7
Aspect ratio [trench depth / trench width]	55	60	75	80	90
Upper electrode	Poly-Silicon	Poly-Silicon	Poly-Silicon	Metal	Metal
Dielectric material	NO	High-k	High-k	High-k	High-k
Bottom electrode	Silicon	Silicon	Silicon	Silicon	Silicon
Capacitor structure / dielectric	SIS / NO	SIS / High-k		MIS / High-k	

Fig. 1-1 ITRS 2005 Trench DRAM Roadmap (Known solutions exist through 57 nm generation.)



Year of 1st Product Shipment / Technology Node	2010 / 45 nm	2011 / 40 nm	2012 / 35 nm	2013 / 32 nm	2014 / 28 nm
DRAM 1/2 pitch [nm]	45	40	36	32	28
Cell size factor	8	8	8	8	8
Cell size [μm2]	0.016	0.013	0.010	0.008	0.006
Trench structure	bottled	bottled	bottled	bottled	bottled
Trench circumference [nm]	374	333	291	266	233
Trench area enhancement factor (bottle) [A]	1.6	1.6	1.6	1.6	1.6
Trench surface roughening factor	1	1	1	1	1
Effective oxide thickness (CET) [nm]	2.0	1.8	1.6	1.4	1.2
Trench depth [nm] (at 35fF)	6.1	6.2	6.1	6.0	5.8
Aspect ratio [trench depth / trench width]	105	120	135	145	160
Upper electrode	Metal	Metal	Metal	Metal	Metal
Dielectric material	High-k	High-k	High-k	High-k	High-k
Bottom electrode	1: Silicon 2: Metal	1: Silicon 2: Metal	Metal	Metal	Metal
Capacitor structure / dielectric	1: MIS / High-k 2: MIM / High-k				

Solutions Exist Solutions Being Pursued No known Solutions

Fig. 1-2 ITRS 2005 Trench DRAM Roadmap (Red brick wall moved to 28 nm, MIM option for ≦50 nm, only option for ≦35nm.)

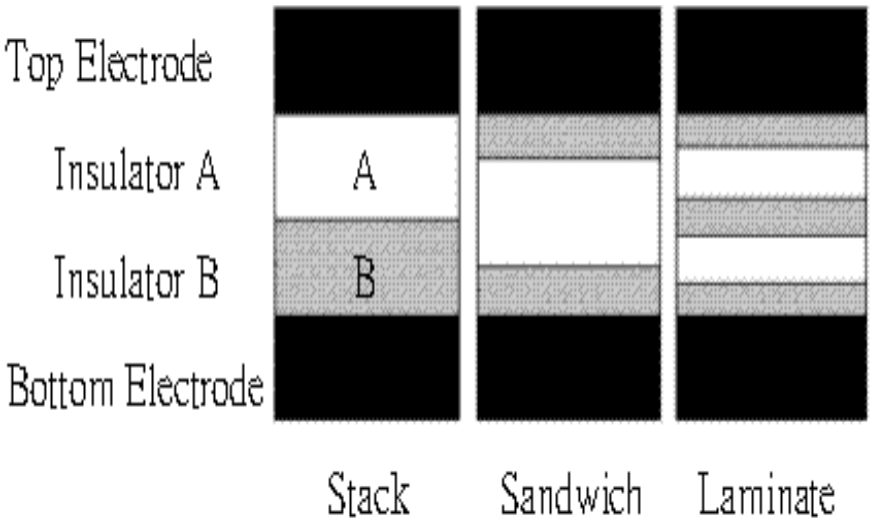


Fig. 1-3 Several variations of dielectric structures with two dielectrics have been attempted in MIM capacitors, such as laminate, sandwich and stack structures.

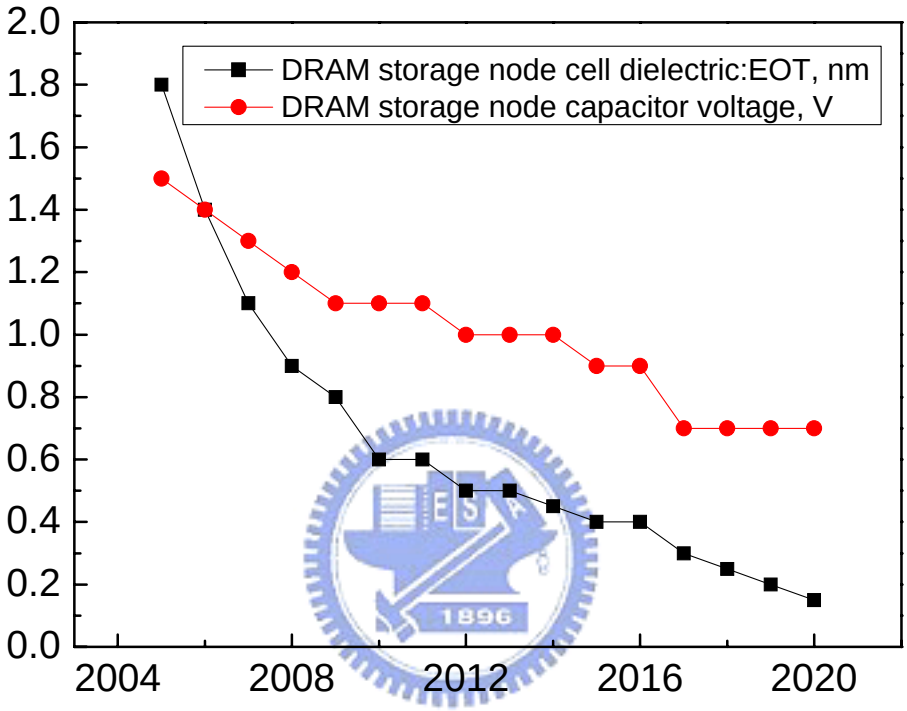


Fig. 1-4 Scaling of DRAM storage dielectric.

Chapter 2
The Research and Applications of High-κ Dielectrics

2.1 Introduction

The gate leakage current increases as the device size decreases. The larger leakage current will not only cause the higher power consumption but also degrade the reliability of the devices. We should avoid it happening.

With using the material with high dielectric constant (high-κ), the physical thickness of the dielectric in the devices can be increased without the reduction of capacitance density. The leakage current is related to the physical thickness as the increasing thickness of high-κ dielectric can reduce the leakage current of the devices. Although high-κ dielectrics often exhibits smaller band gap, weaker bond, and higher defect density than SiO_2, the high-κ dielectrics with the same effective oxide thickness(EOT) still shows lower leakage current than SiO_2 by several orders.

Dielectrics with higher dielectric constant than SiO_2 exhibit the potential to replace the conventional thermal oxide for sub-100nm technology node. Not only the gate leakage current can be reduced without the reduction of drain current drive and mutual conductance, but also the reliability of gate dielectrics can be improved effectively.

Recently, some high-κ dielectrics have been widely studied. The characteristics and issues of those materials have also been reported. The high-κ dielectrics show that good performances are always accompanied by other drawbacks.

According to the ITRS roadmap, the continuously increasing capacitance density of MIM capacitors [1]-[2] is required to achieve smaller chip area and lower cost of IC. Thus, searching for proper high-κ dielectrics [3]–[11] is the primary challenge because decreasing dielectric thickness will increase the unwanted leakage current exponentially.

2.2 The Research of High-κ Dielectrics

The dramatic increase in wired and wireless communications have triggered the demand for metal–insulator–metal (MIM) capacitors, which can offer low parasitic capacitance, low voltage coefficients, and high quality factor for RF applications [12]. With an increase in levels of integration and the scale-down of chip size, future technology generations will require integrated RF MIM capacitors with higher capacitance density in view of lower system cost. High capacitance density can be achieved by utilizing either high dielectric constant (high-κ) materials or very thin insulator layers. However, leakage current and reliability issues limit the aggressive thickness scaling [13]. Therefore, high-κ materials are much preferred as a possible

solution.

In recent years, various high-κ dielectrics, such as HfO_2 [14]–[16], $AlTaO_x$ [17], Tb-doped HfO_2[14], $(HfO_2)_{1-x}$ $(Al_2O_3)_x$ [18], Al_2O_3 [19], [20], $AlTiO_x$ [20], and Ta_2O_5 [19], [21], have been explored to replace conventional silicon dioxide and silicon nitride for MIM capacitors. However, the challenge still remains to achieve high capacitance density especially in RF regime, while maintaining minimal leakage current, acceptable voltage coefficients of capacitance (VCCs), and so on under the thermal budget of a back-end process.

2.3 The Applications of High-κ Dielectrics

The most significant application for high-κ dielectrics will be to extend the scaling of silicon transistors and to reduce the short channel effect and the power consumption. Without high-κ dielectric, it is impossible to prevent the exponential increase of the gate leakage current as the device scaling progresses continuously. Once the scaling is stopped due to the unacceptable power consumption and bad device reliability, the operation frequency of the device cannot have chances to be raised to a higher value. Not only the bandwidth of communication cannot be broadened, but also the limits of operation speed of microprocessors appear. No doubt the gate dielectrics are the core of CMOS devices while CMOS transistors are the fundamentals of integrated circuits.

Therefore, the way to replace conventional oxide by high-κ dielectrics is an inevitable and significant application in the next generation of VLSI technology.

The continuous shrink of scaling of design rules for DRAM leaves us some difficulties to overcome. In the G-bit DRAM generation, the memory cell density is so high that the cell space can only allow dielectrics thicker than 20nm. This requirement of thickness for dielectrics makes it impossible to use complex metal oxide such as BST as the dielectric layers. Because of the difficulty of conformal CVD for complex metal oxide, the high aspect ratio of the trench for DRAM seems to be another challenge to integrate the complex metal oxide into G-bit DRAM generation. Owing to the high dielectric constant, good step coverage and minimum thickness limit, simple metal oxide such as Ta_2O_5, Al_2O_3 and TiO_2 are thought the promising materials in the application of DRAM. Among the simple metal oxide, Ta_2O_5 exhibits better step coverage than others. But it has higher leakage current and degradation after high temperature process. The former can be reduced by using oxygen annealing and the latter can be solved by utilizing a new electrode material reported in the literature. Recently, there has been much attention on TiO_2 due to its high dielectric constant (40~180) and well thermal stability. High temperature crystallization can cause not only the increase of leakage current but also reduce the breakdown voltage as well as non-uniform leakage current. Therefore, the thermal stability is a critical issue in the

choice of high-κ dielectrics for capacitor DRAM cell. In addition to TiO_2 and Al_2O_3 also attract much attention due to their thin effective oxide thickness even in the trench with the aspect ratio of 60 and top critical dimension of 80 nm. These results indicate that simple metal oxide is suitable to enhance the performance and density of DRAM.

For example, the high-κ dielectrics used in MIM capacitors have evolved from SiON (κ~4-7) [1]-[3], Al_2O_3 (κ=10) [4], HfO_2 (κ~22) [5]-[9], Ta_2O_5 (κ~25) [10], [11] to Nb_2O_5 (κ~40) [12] and TaTiO (κ~45) [13]-[15]. Table 2-1 shows materials properties of high-κ dielectrics.

2.4 The Development and Trend of High-κ Dielectrics

By altering the sources of deposition, various dielectrics can be deposited on the substrates. Moreover, this simple process technique will integrate with front-end or back-end process.

Owing to this figure of merits, this process technique makes the development of high-κ dielectric more practicable. As the dielectrics of passive components, our process technique increases the dielectric constant and reduces the thickness of dielectrics without the degradation of electrical characteristics at the same time. Once interface oxide forms during a high temperature process, the effective oxide thickness increases obviously, whereas high-κ dielectrics without doping tend to crystallize during high temperature and cause high leakage current.

Material	Dielectric constant(κ)	Band gap E_g (eV)	ΔE_c (eV) to Si
SiO_2	3.9	8.9	3.2
Si_3N_4	7	5.1	2
Al_2O_3	9	8.7	2.8
La_2O_3	30	4.3	2.3
Ta_2O_5	26	4.5	1-1.5
TiO_2	80	3.5	1.2
HfO_2	25	5.7	1.5
TiTaO	**45**	—	—

Table 2-1 Materials properties of high-κ dielectrics.

Chapter 3

The Experimental Procedure of High-κ MIM Capacitors Using the TiTaO Dielectric

3.1 The Experimental Procedure

The TiTaO MIM capacitors were fabricated using 4 inch p-type or n-type Si wafers. After depositing 2 μm SiO_2 on a Si wafer, the lower capacitor electrode was formed using PVD-deposited TaN/Ta bi-layers. Ta was used to reduce the series resistance and the TaN served as a barrier layer between the high-κ TiTaO and the Ta electrode. Then $Ti_xTa_{1-x}O$ (x~0.6) dielectric was deposited by PVD, followed by a 400°C oxidation and the devices were also annealed at 400°C for 30 min in N_2 for stability test reduce the leakage current. Finally, Ir or Al was deposited and patterned to form the top capacitor electrode [1]-[2].

Different TiTaO thicknesses of 41, 28, 17 and 14nm were used to study the voltage linearity in the devices. The MIM capacitor area is 30 μm × 30 μm.

The fabrication process flow is listed as follows:

1. 4 inch p-type or n-type Si wafer (100).

2. RCA clean.

3. 2 μm SiO_2 deposited on Si wafers in a furnace.

4. Depositing TaN/Ta bi-layers by PVD.

5. Patterning and depositing $Ti_xTa_{1-x}O$ (x~0.6) dielectric by PVD.

6. Followed by oxidation at 400°C and Furnace annealing at 400°C for 30 min in N_2 ambient.

7. Finally, Ir or Al was deposited on the dielectrics and patterned to form the top capacitor electrode.

3.2 The Measurement of High-κ MIM Capacitors Using the TiTaO Dielectric

The fabricated capacitors were characterized by C-V and J-V measurements using an HP4155B semiconductor parameter analyzer and an HP4284A precision LCR meter.

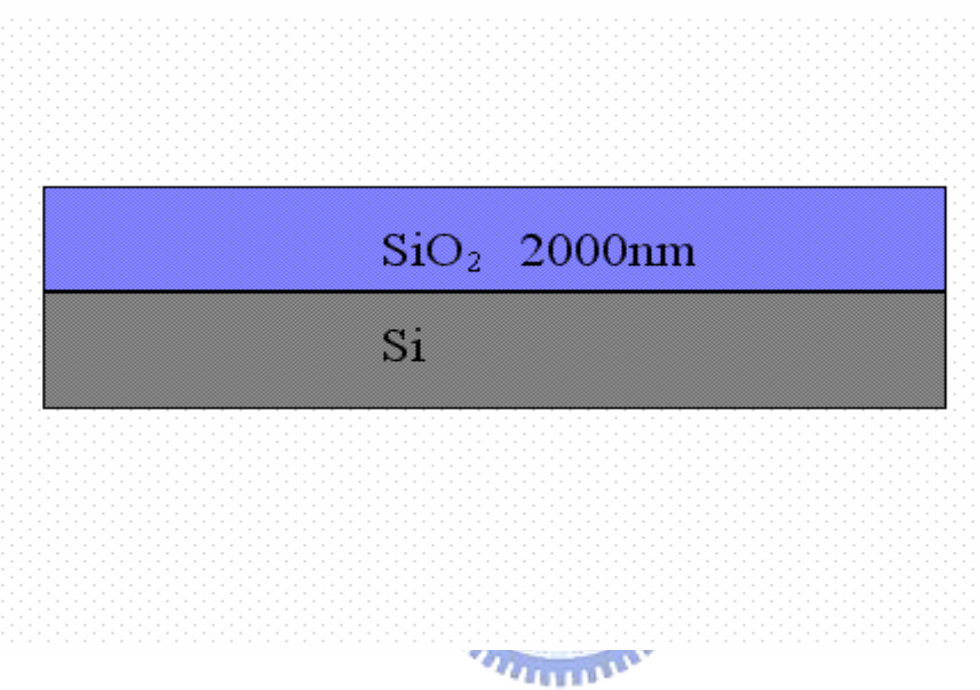


Fig. 3-1 Silicon substrate, RCA clean and 2 μm SiO_2 deposited on Si wafers in a furnace.

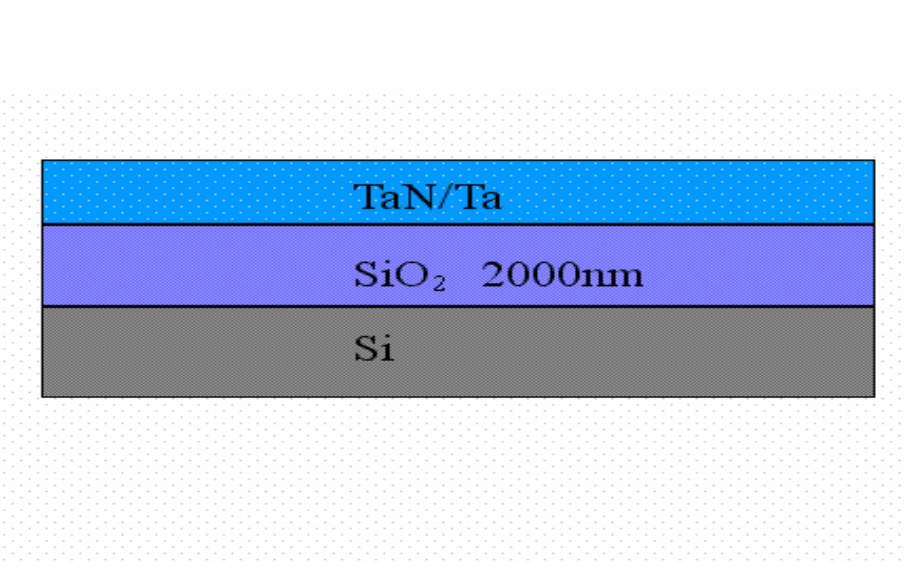


Fig. 3-2 Depositing TaN/Ta bi-layers by PVD

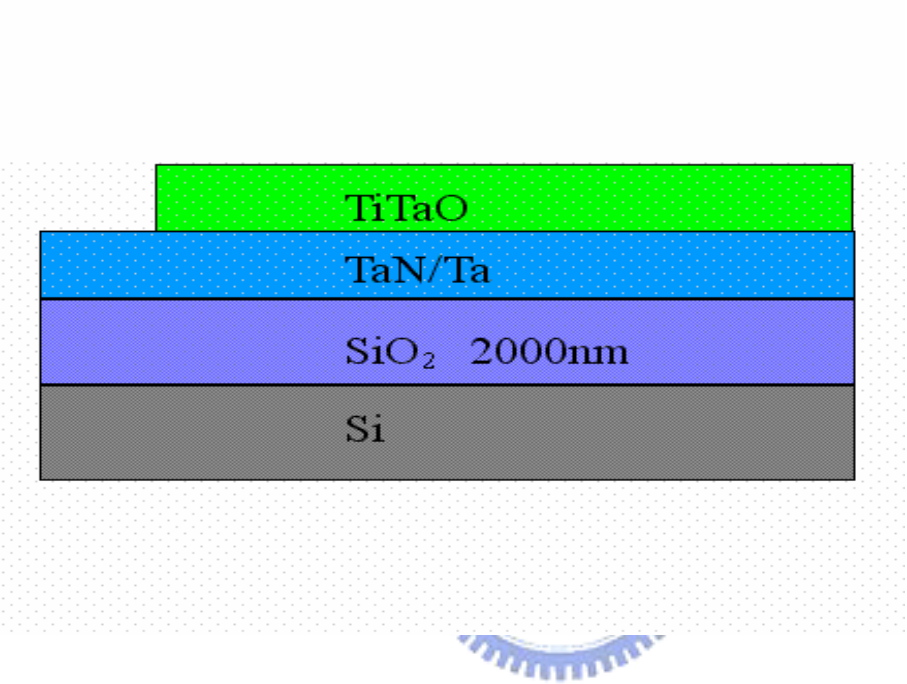


Fig. 3-3 Patterning and depositing $Ti_xTa_{1-x}O$ (x~0.6) dielectric by PVD, followed by oxidation at 400°C and furnace annealing at 400°C for 30 min in N_2 ambient.

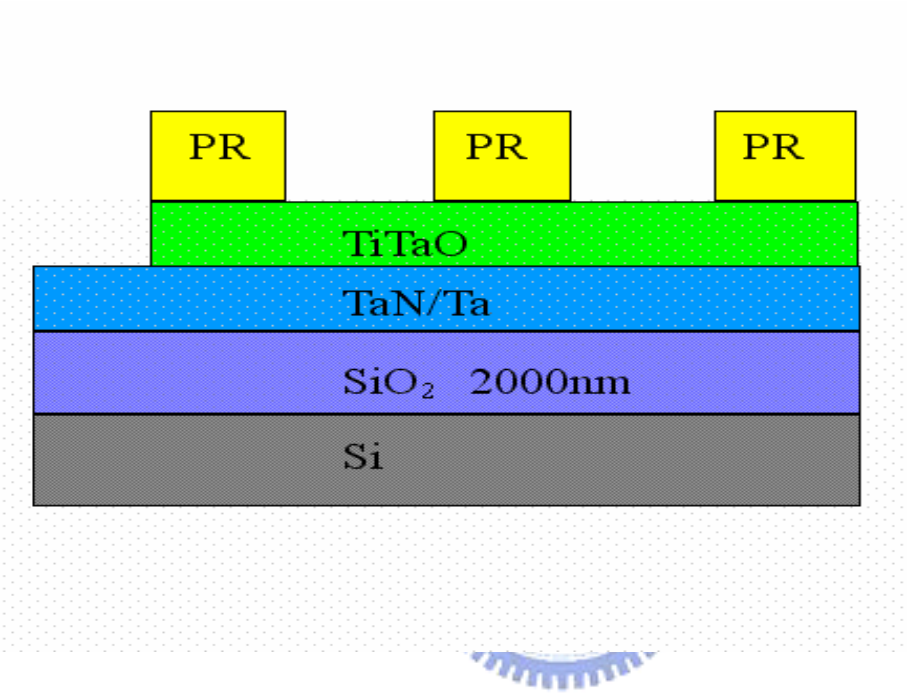


Fig. 3-4 Ir or Al was deposited on the dielectrics and patterned to form the top capacitor electrode (step 1).

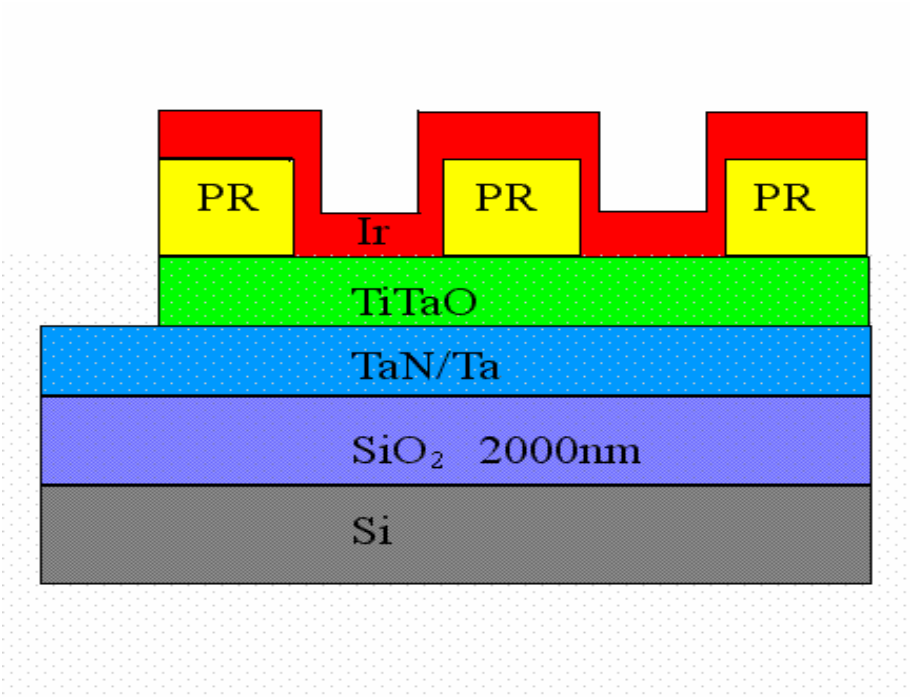


Fig. 3-5 Ir or Al was deposited on the dielectrics and patterned to form the top capacitor electrode (step 2).

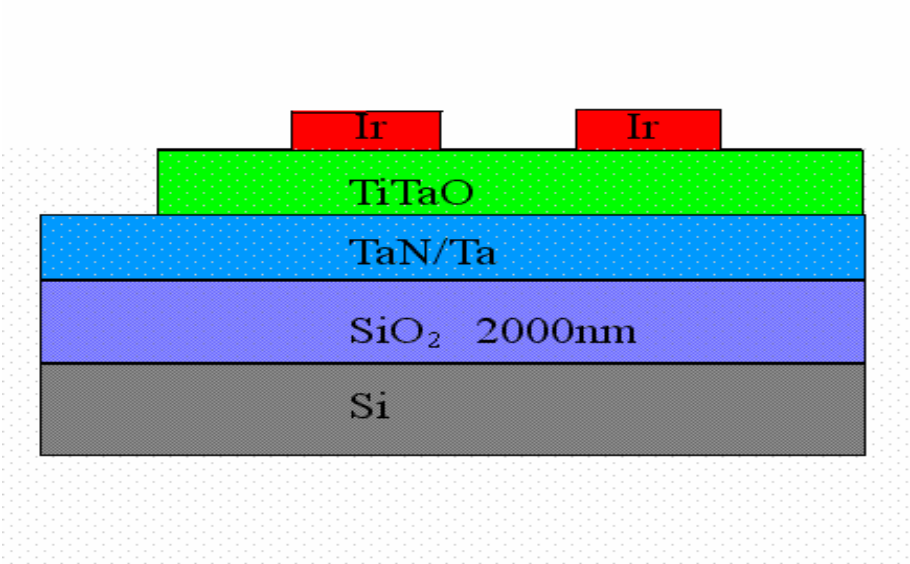


Fig. 3-6 Ir or Al was deposited on the dielectrics and patterned to form the top capacitor electrode (step 3).

Chapter 4

The Characteristics and Analysis of High-κ MIM Capacitors Using the TiTaO Dielectrics

4.1 Introduction

To achieve continuing improvements in mixed signal and RF integrated circuit performance, the sizes of both the active MOSFETs and the passive MIM capacitors [1]-[16] need to be scaled down. The technology challenge for the MIM capacitor is to achieve high capacitance density, low leakage current and small voltage linearity of the capacitance simultaneously [17]. To meet these device requirements, the use of high-κ dielectrics for the MIM capacitors is the only viable choice. This is because decreasing the dielectric thickness (t_d) needed for high capacitance density ($\varepsilon_0\kappa/t_d$) increases the leakage current and degrades the capacitor's voltage linearity.

The novel Ir/TiTaO/TaN capacitors show high capacitance density [18], small leakage current and low voltage linearity, simultaneously. The TiTaO dielectric capacitors also show good thermal stability, such as low leakage current after a 400^{o}C thermal cycle associated with its backend process. This contrasts with TiO_2 dielectric capacitors which give high leakage current after 400^{o}C processing [16]. The excellent

device performance arises from using the very high-κ TiTaO dielectric (κ=45) and high work-function Ir (5.2 eV). These are the first results that meet all the ITRS roadmap requirements for analog capacitors in the year 2018 - such as 10 fF/μm^2 capacitance density, leakage current <5.8 fA/[pF•V], and capacitance voltage linearity <100 ppm/V^2 [17].

4.2 C-V characteristics of High-κ MIM Capacitors Using the TiTaO Dielectric

Fig. 1 shows the cross-sectional TEM image of 28 fF/mm^2 TiTaO with 1.2 nm capacitance-equivalent thickness (CET). A dielectric constant of 45 and CET of 1.2 nm are obtained.

Fig. 2-3 show the XRD for TiO_2 and TiTaO. Significant crystallization of TiO_2 is observed after 400^{o}C O_2 treatment and is worse after following N_2 annealing. In sharp contrast, the TiTaO dielectric stays amorphous even after 400^{o}C annealing for 30 min.

Fig. 4-7 show the C-V characteristics of high-κ Ir/TiTaO/TaN MIM capacitors. The capacitance densities of 10.3, 14.3, 23 and 28 fF/μm^2 were measured for the 41, 28, 17 and 14 nm TiTaO dielectric devices, which give capacitance-equivalent thicknesses (CET) of 3.4, 2.4, 1.5 and 1.2 nm respectively. A high-κ value of about 45 was obtained from the measured capacitance density in the TiTaO dielectric.

4.3 J-V characteristics of High-κ MIM Capacitors Using the TiTaO Dielectric

Figure 8-11 show the J-V characteristics of Al/TiTaO/TaN and Ir/TiTaO/TaN MIM capacitors with 3.4, 2.4, 1.5 and 1.2 nm CET. High breakdown voltages of 14 and 20 V were measured for the 10.3 and 14.3 fF/μm^2 density devices, well above values required for most analog function applications.

The ITRS requirement for analog capacitors by 2018 is the density of 10fF/μm^2 and low leakage current and capacitance voltage linearity. The low leakage current of 1.2×10^{-8} A/cm^2 at 2V or 5.8 fA/[pF•V] obtained for the 10.3 fF/μm^2 density device meets the ITRS-required low leakage current of <7 fA/[pF•V] [17]. Such a low leakage current is due to the amorphous structure of the TiTaO preserved, even after the backend processing involving 400^{o}C oxidation and N_2 annealing. This was confirmed by X-Ray diffraction measurements.

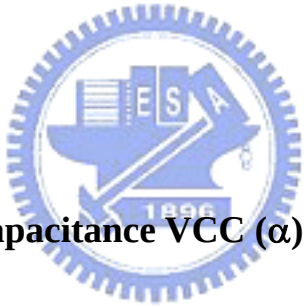
The leakage current of TiTaO is ~4-7 orders of magnitude lower than TiO_2 for the same 23 fF/μm^2 density and consistent with XRD and TEM. The leakage current from top Al or Ir injection is lower than bottom TaN due to the better interface and consistent with capacitance dispersion in C-V, which further reduces by using Ir electrode by ~1 order of magnitude lower than Al due to larger ϕ_B.

The exponential relation of leakage current with capacitance density is plotted in

Fig. 12.

4.4 Normalized Capacitance Variation ΔC/C

For analog capacitors, the low capacitance voltage linearity is important. Figure 13-14 show the plots of ΔC/C versus V for Al/TiTaO/TaN and Ir/TiTaO/TaN MIM capacitors of 10.3 and 14.3 fF/μm^2. The ΔC/C is much lower by using Ir electrode than Al. The ΔC/C decreases rapidly with decreasing capacitance density from 14.3 to 10.3 fF/μm^2, which is consistent with the decreasing trend of the leakage current, as shown in Fig. 10-11.



4.5 Voltage Coefficient Capacitance VCC (α)

Low quadratic VCC (α) of 89 ppm/V^2 and linear VCC (β) of 178 ppm/V are obtained in 10.3 fF/μm^2 devices with low leakage current of 1.2×10^{-8} A/cm^2 or 5.8 fA/[pF•V] at 2V. This is the lowest α[1]–[16] to meet the ITRS roadmap requirement at year 2018: α<100 ppm/V^2 and leakage <7 fA/[pF•V] at 10 fF/μm^2 capacitance density.

Fig. 15 shows the variation of α as a function of CET or 1/C. We note that the effect of β can be cancelled by the circuit design [17]. An exponential decrease of α with increasing CET or 1/C is observed for all the Ta_2O_5, HfO_2, Tb-doped HfO_2 and Ir/TiTaO/TaN capacitors [2], [7]-[8]. This may be due to the trap-related leakage current

that has the exponential dependence with CET [6].

The TiTaO has the lowest α than HfO_2 and Ta_2O_5 devices [19]-[21] at the same 1/C. This is due to the high-κ value of 45 which exceeds the κ~22-25 values for HfO_2 and Ta_2O_5. We note that the exponential decrease with increasing 1/C is important when designing capacitors to meet different requirements.

Fig. 16 shows the energy band diagram of MIM device. Very high κ TiTaO and high ϕ_B of Ir compared with TaN are used to achieve low leakage current and high capacitance density.

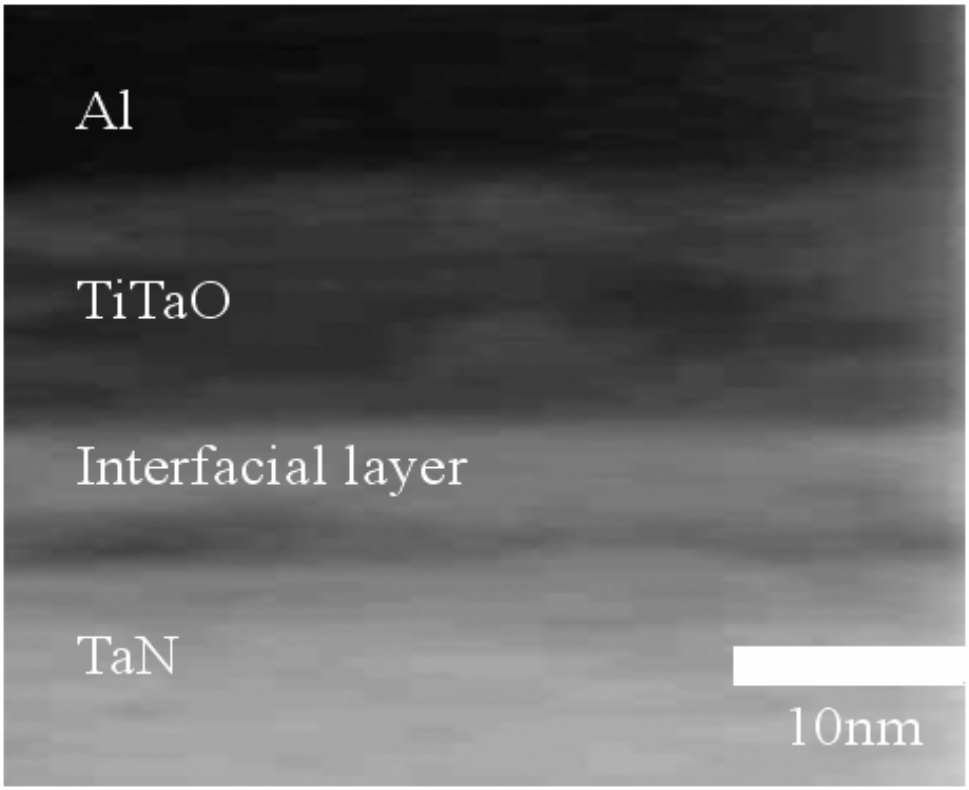


Fig. 4-1 The cross-sectional TEM image of 28 fF/mm^2 TiTaO with 1.2nm capacitance-equivalent thickness (CET).

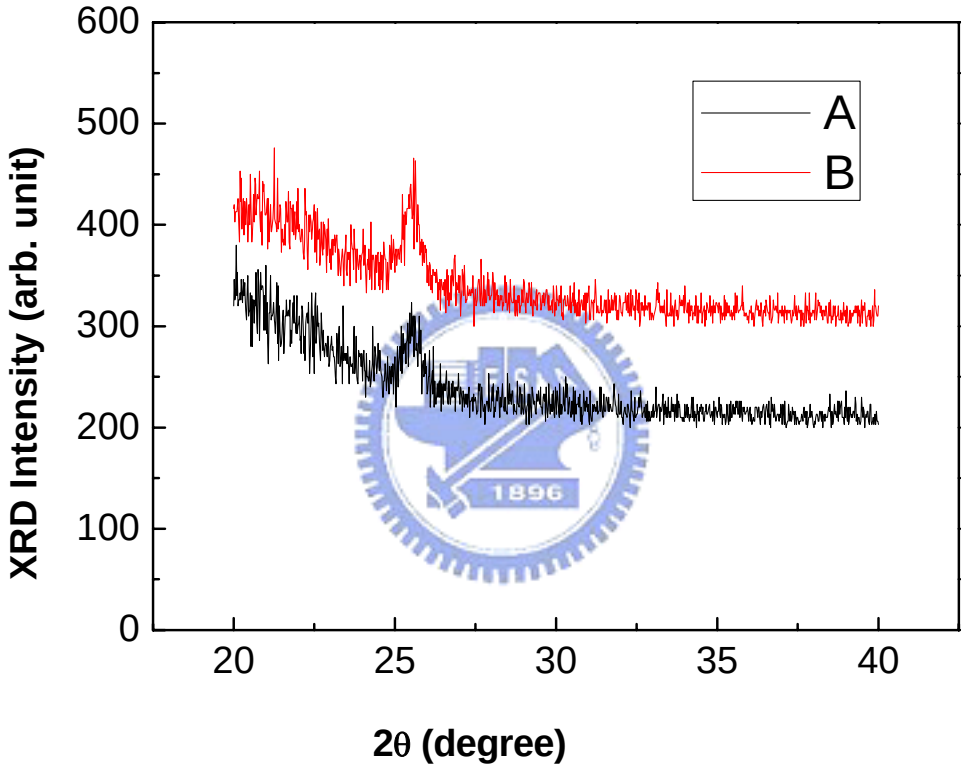


Fig. 4-2 (A) TiO_2 after annealing at 400℃ in O_2 for 10 min.

(B) TiO_2 after annealing at 400℃ in O_2 for 10 min and N_2 ambient for 30min.

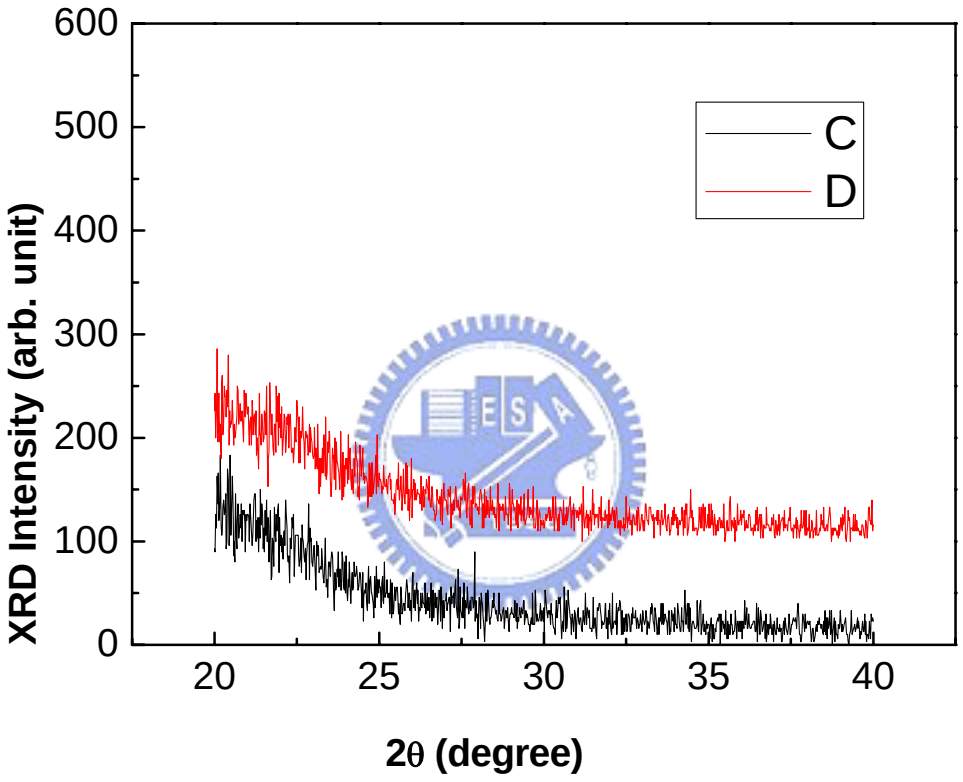


Fig. 4-3 (C) TiTaO after annealing at 400℃ in O_2 for 10 min.

(D) TiTaO after annealing at 400℃ in O_2 for 10 min and N_2 ambient for 30 min.

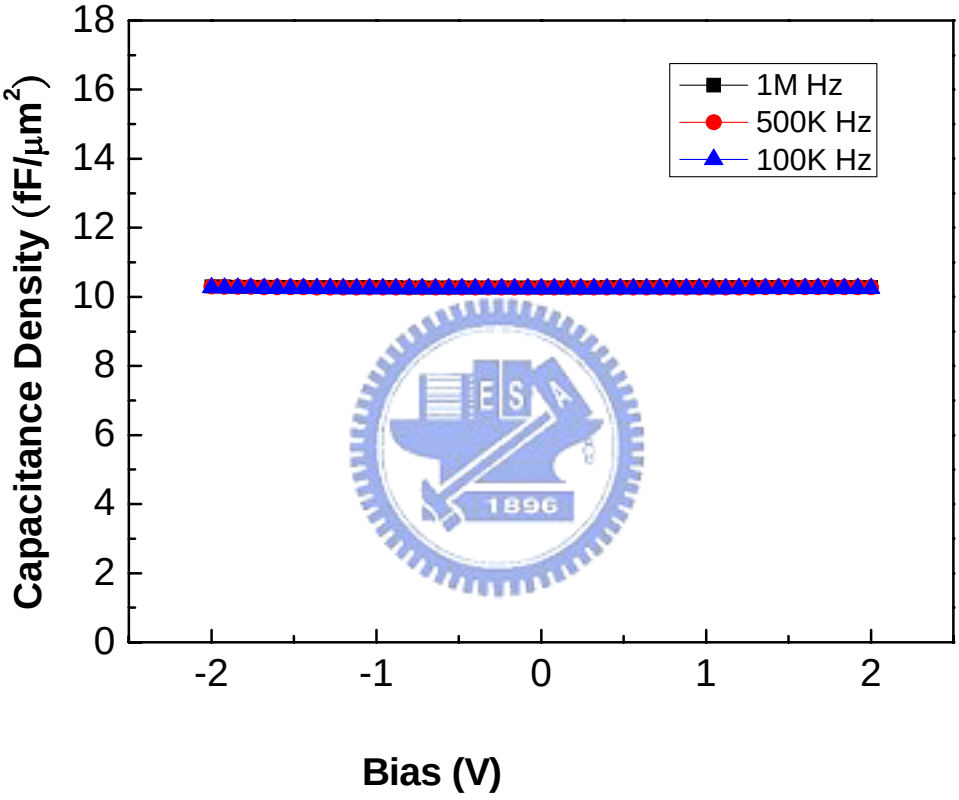


Fig. 4-4 The C-V characteristics. High capacitance density of 10.3 fF/μm^2 is measured.

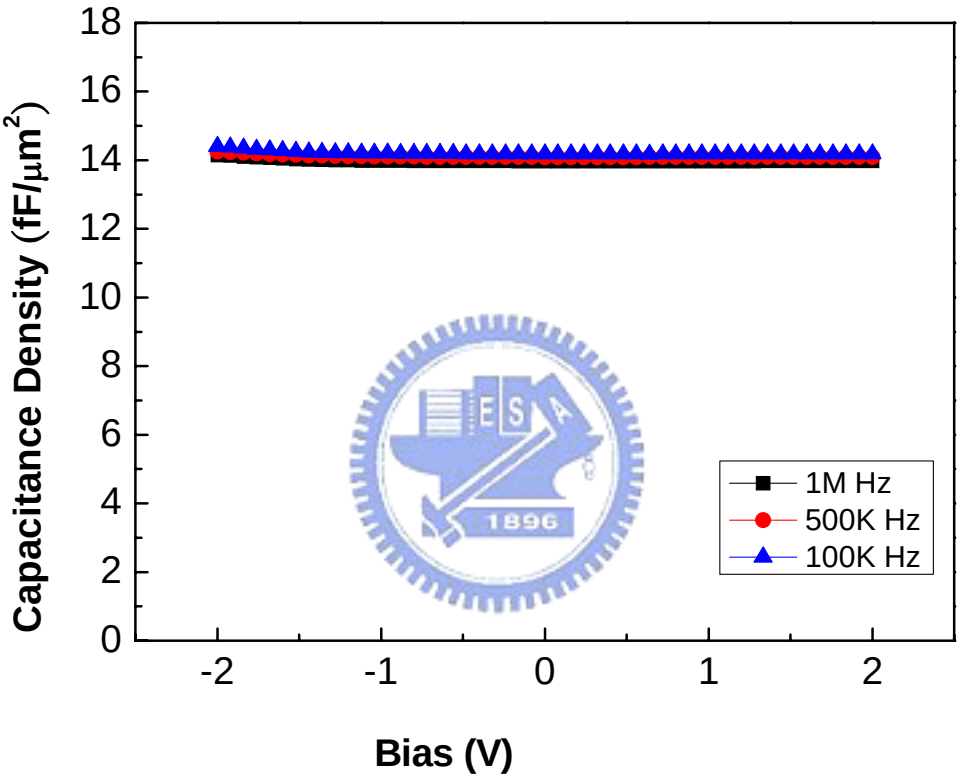


Fig. 4-5 The C-V characteristics. High capacitance density of 14.3 fF/μm^2 is measured.

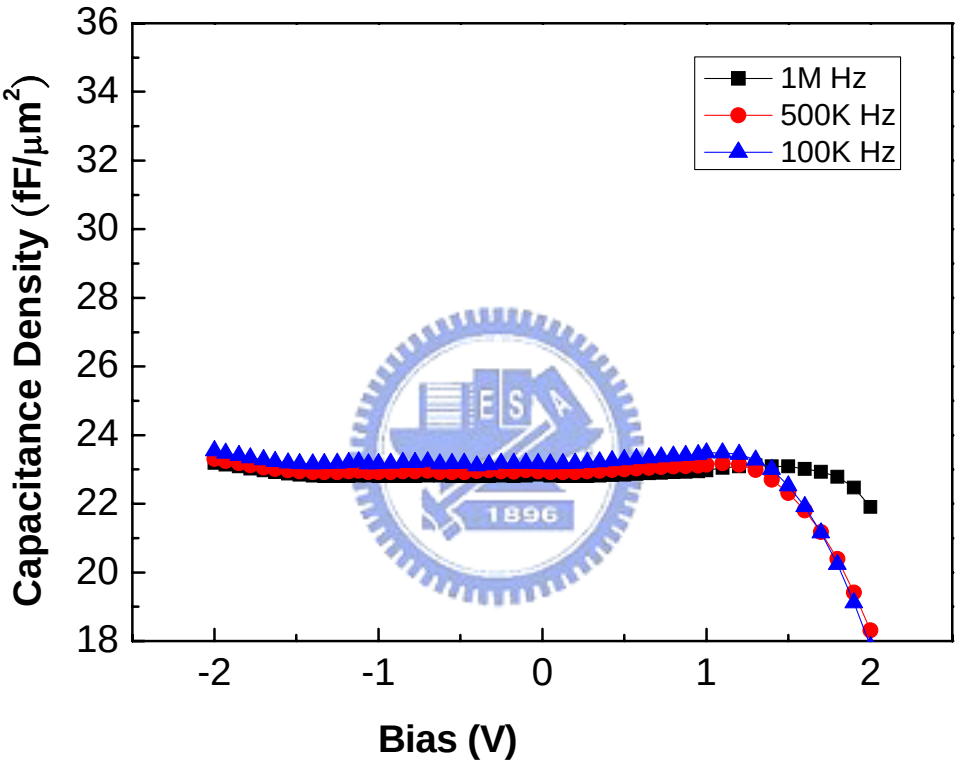


Fig. 4-6 The C-V characteristics. High capacitance density of 23 fF/μm^2 is measured.

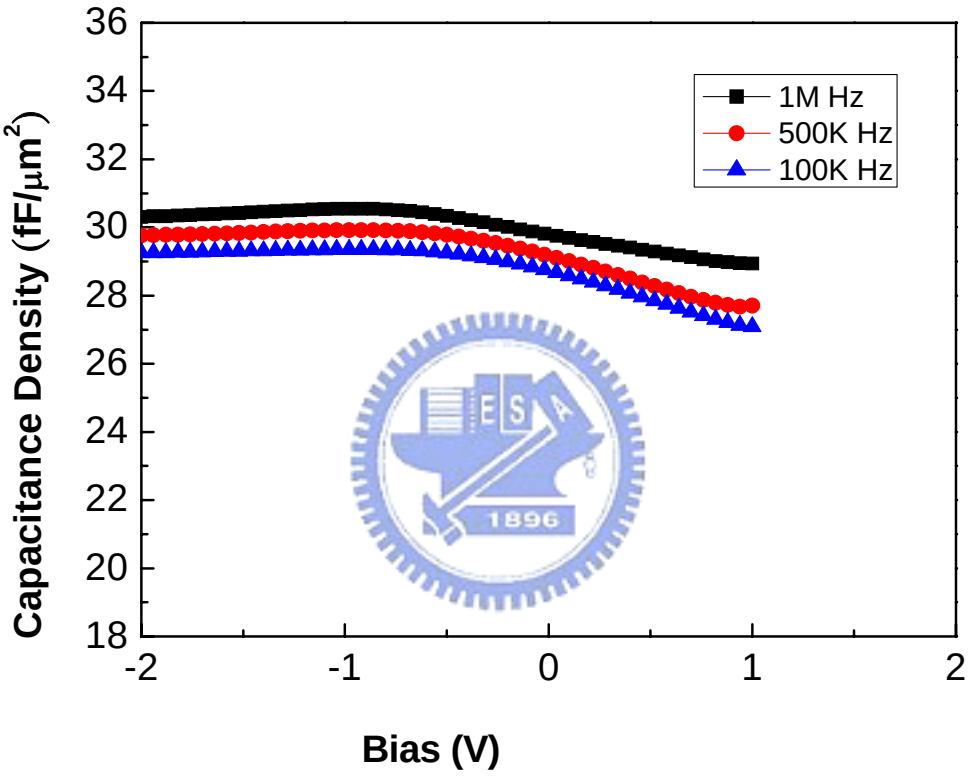


Fig. 4-7 The C-V characteristics. High capacitance density of 28 fF/μm^2 is measured.

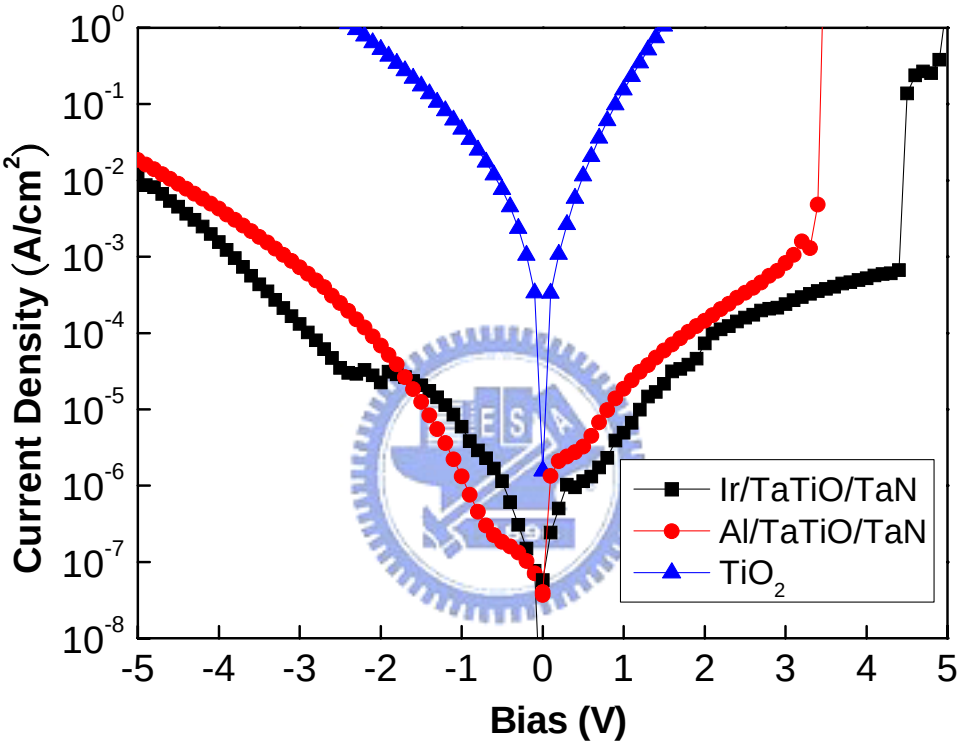


Fig. 4-8 The J-V characteristics of Al/TiTaO/TaN and Ir/TiTaO/TaN MIM capacitors with 23 fF/μm^2 and 1.5 nm CET.

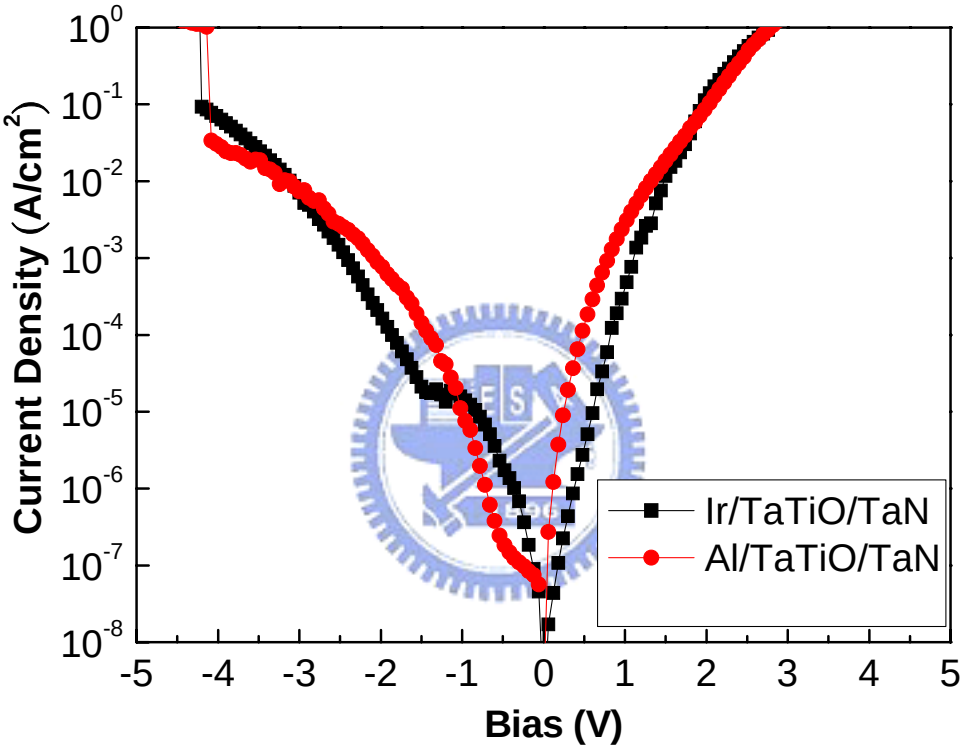


Fig. 4-9 The J-V characteristics of Al/TiTaO/TaN and Ir/TiTaO/TaN MIM capacitors with 28 fF/μm^2 and 1.2 nm CET.

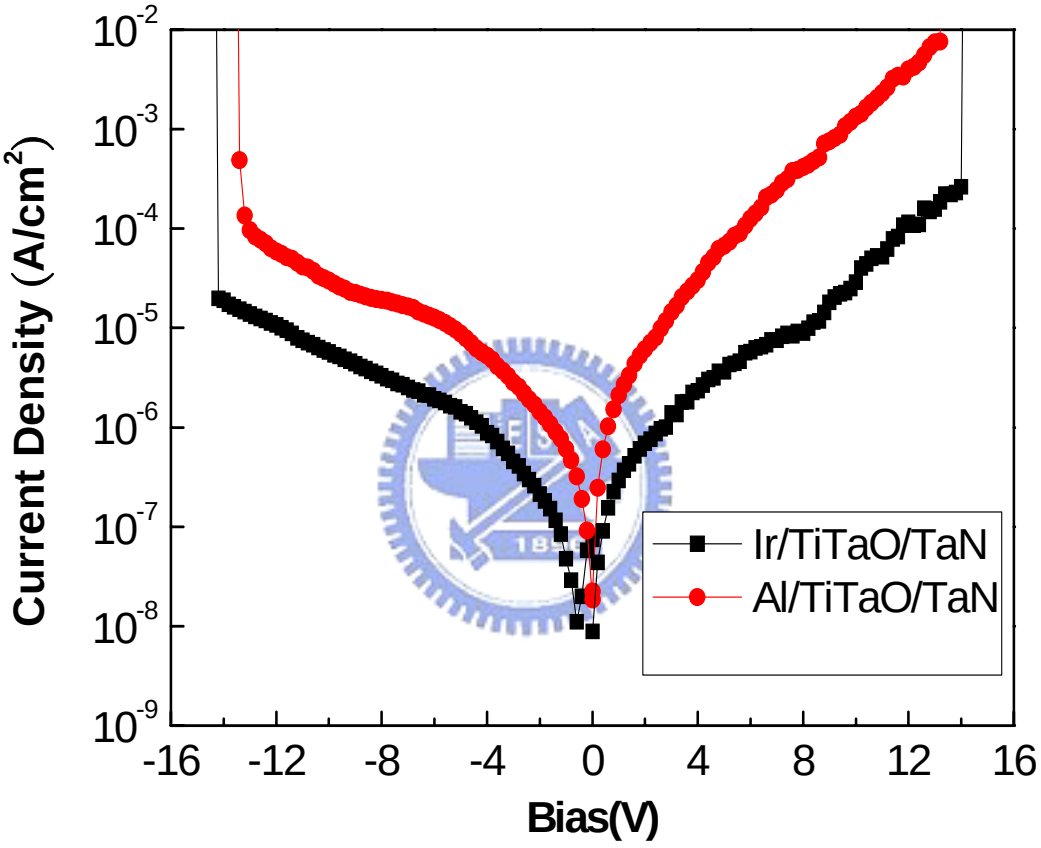


Fig. 4-10 The J-V characteristics of Al/TiTaO/TaN and Ir/TiTaO/TaN MIM capacitors with 10.3 fF/μm^2 and 3.4 nm CET.

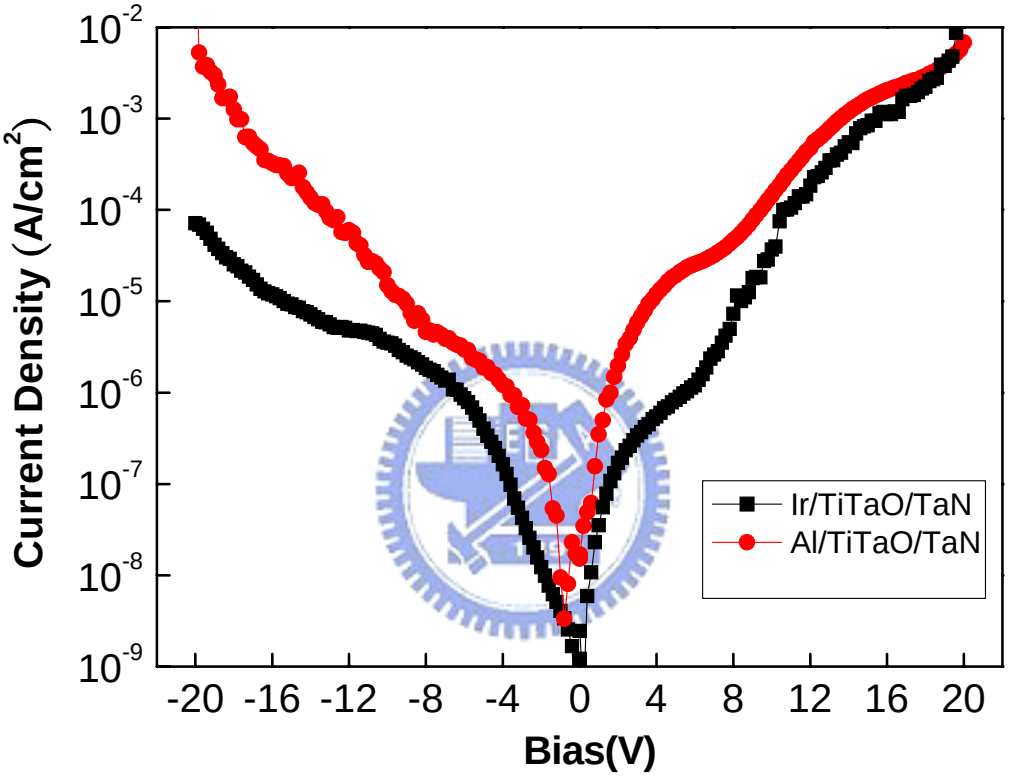


Fig. 4-11 The J-V characteristics of Al/TiTaO/TaN and Ir/TiTaO/TaN MIM capacitors with 14.3 fF/μm^2 and 2.4 nm CET.

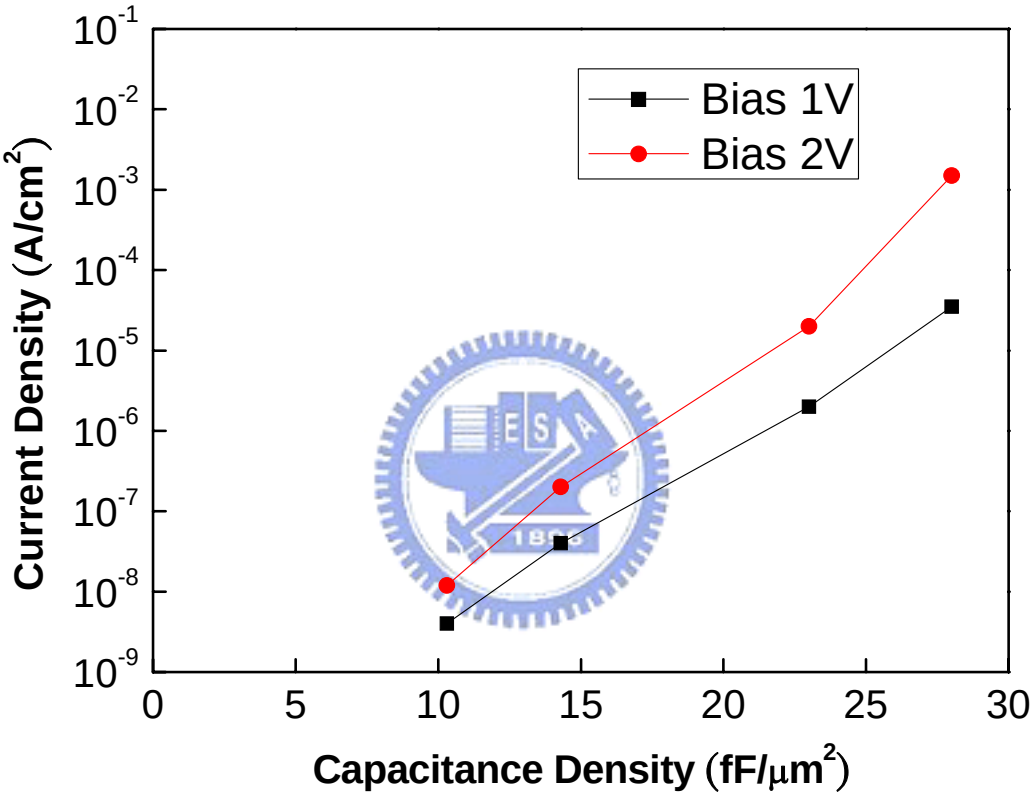


Fig. 4-12 The exponential relation of leakage current with capacitance density.

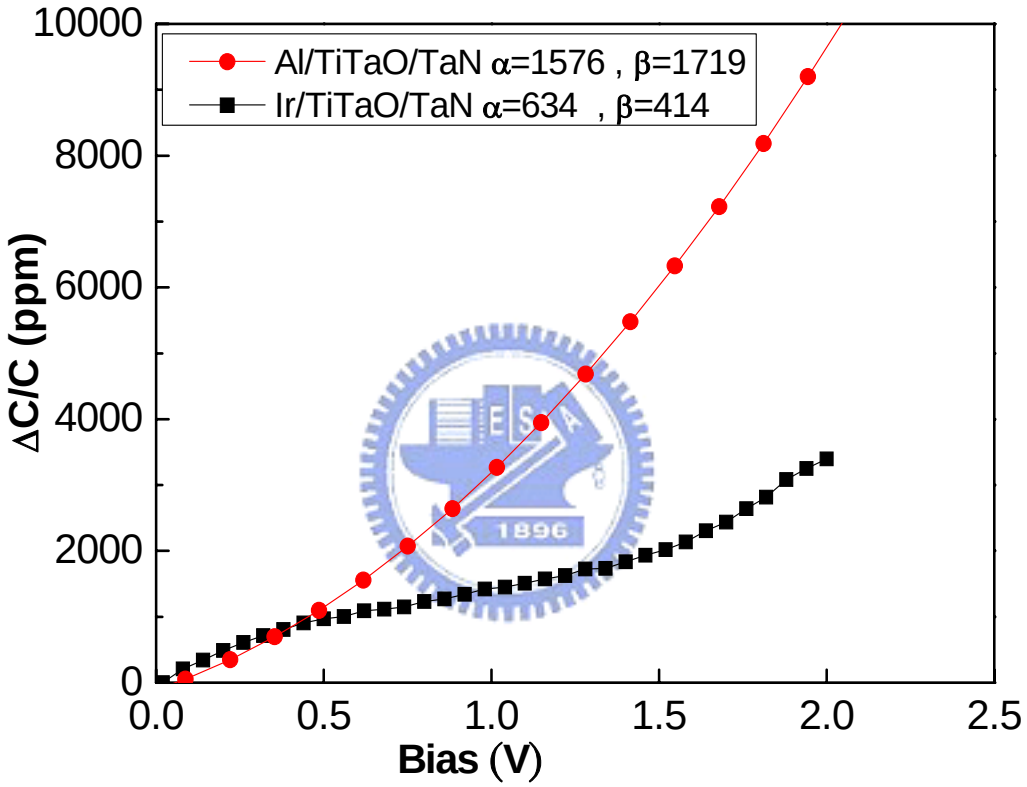


Fig. 4-13 The plots of ΔC/C versus V for Al/TiTaO/TaN and Ir/TiTaO/TaN MIM capacitors of 14.3 fF/μm^2.

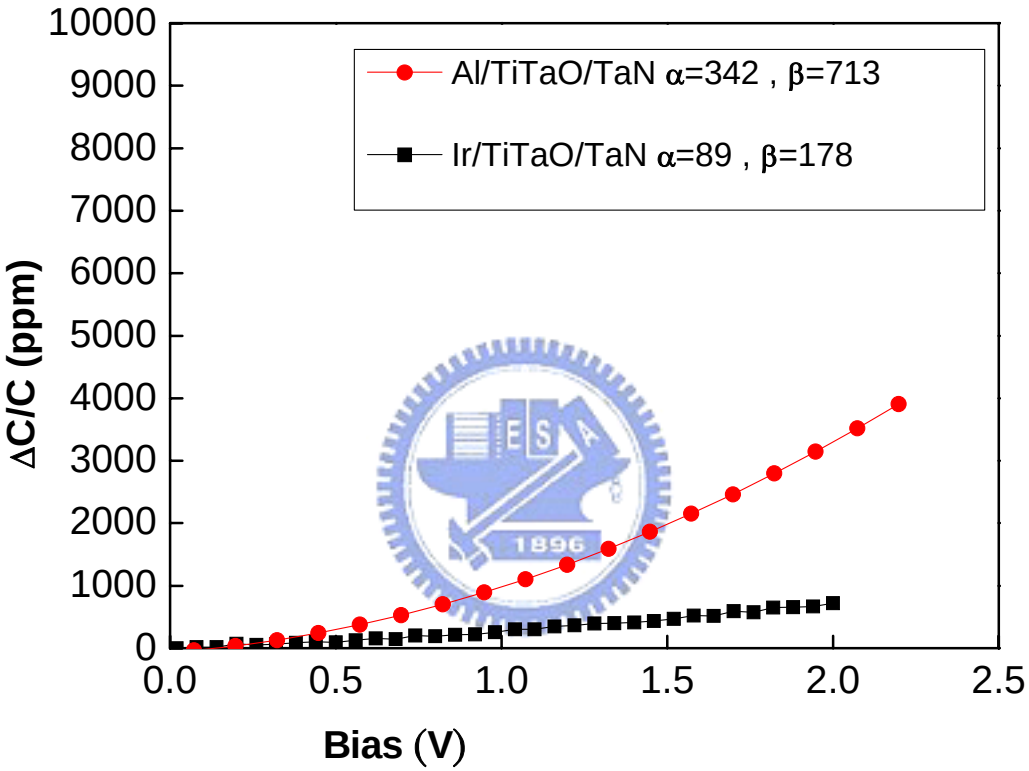


Fig. 4-14 The plots of ΔC/C versus V for Al/TiTaO/TaN and Ir/TiTaO/TaN MIM capacitors of 10.3 fF/μm^2.

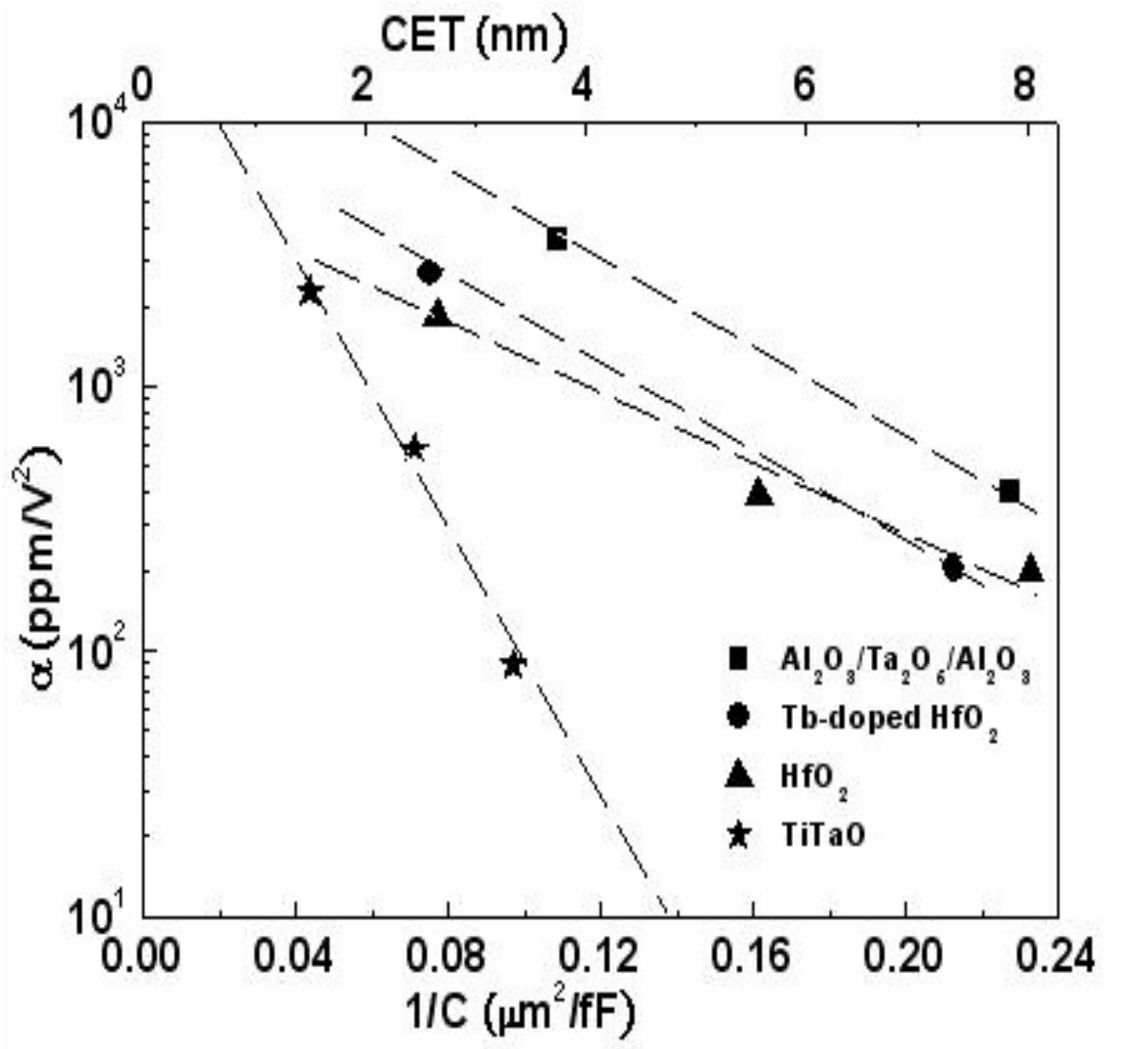


Fig. 4-15 The variation of α as a function of CET or 1/C.

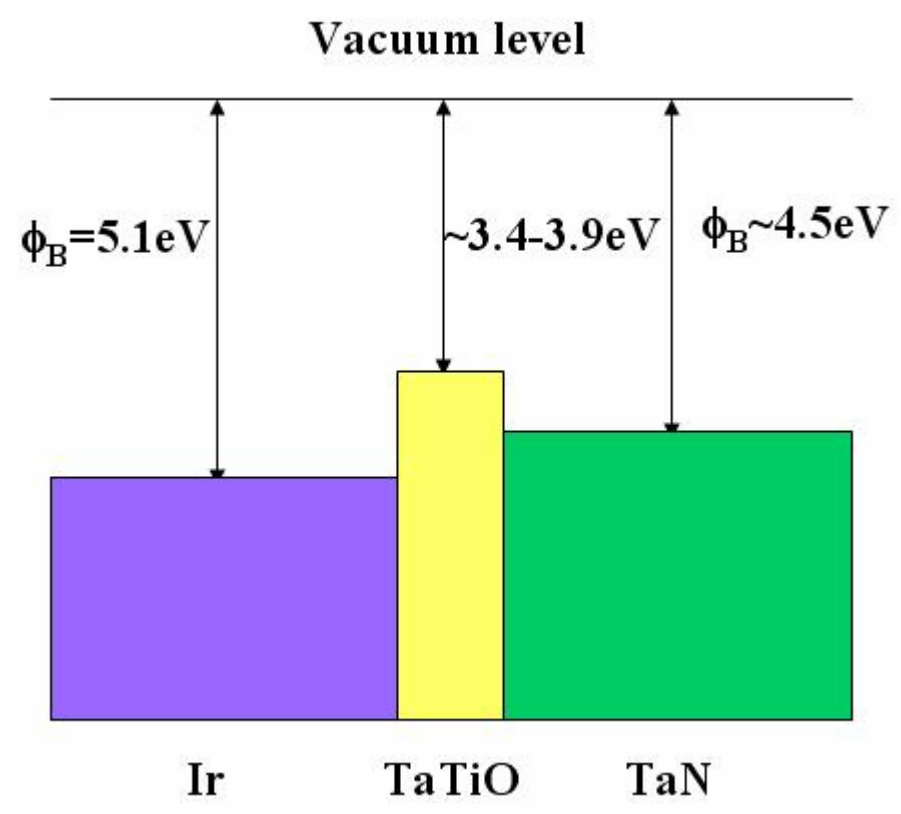


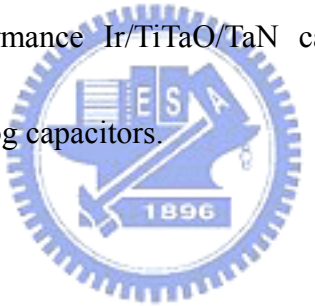
Fig. 4-16 The energy band diagram of MIM device.

Chapter 5
Conclusions

5.1 Conclusions

Table 1 summarizes the comparison of TiTaO with other high-κ dielectric capacitors. The high capacitance density, low VCC, low leakage current and simple single dielectric process are the merits using the novel high-κ TiTaO dielectric.

By using the high-κ TiTaO dielectric and a high work-function Ir electrode, we have exhibited a high performance Ir/TiTaO/TaN capacitor that meets the ITRS roadmap requirements for analog capacitors.



	ITRS @ 2018	Ta_2O_5 [1]	Tb-HfO_2 [2]	HfO_2 [3]	Ir/TiTaO/TaN	
Capacitance Density ($fF/\mu m^2$)	10	9.2	13.3	12.8	10.3	14.3
J (A/cm^2)	—	2×10^{-8} (1.5V)	1×10^{-7} (2V)	8×10^{-9} (2V)	1.2×10^{-8} (2V)	2×10^{-7} (2V)
J/(C•V) (fA/[pF•V])	<7	14.5 @1.5V	38 @2V	2.9 @2V	5.8 @2V	—
α (ppm/V^2) β (ppm/V)	α<100	3580 2060	2667 332	1990 211	89 178	634 414

Table 5-1 Comparison of various high-κ capacitors. All the requirements of the ITRS roadmap at 2018 are satisfied by the Ir/TiTaO/TaN capacitor.

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Chapter 5

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Vita

姓名：簡俊全

性別：男

出生年月日：民國 71 年 4 月 7 日

籍貫：臺灣省桃園縣

學歷：桃園市立桃園高級中學

（86 年 9 月~89 年 7 月）

國立中山大學電機工程學系

（89 年 9 月~94 年 7 月）

國立交通大學電子工程研究所碩士班

（94 年 9 月~96 年 7 月）

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