國立交通大學

電子工程學系 電子研究所

碩士論文

高介電常數金屬-絕緣層-金屬電容電性及其可靠度之研究

The Research of Electric Characteristics and Reliability of High-κ MIM Capacitors

研究生：陳冠麟

指導教授：荊鳳德 教授

中華民國九十六年六月

高介電常數金屬-絕緣層-金屬電容電性及其可靠度之研究

The Research of Electric Characteristics and Reliability of High-κ MIM Capacitors

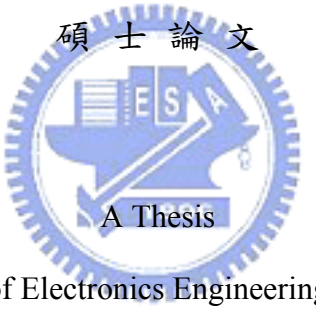
研 究 生：陳冠麟　　Student：Guan Lin Chen

指導教授：荊鳳德　　Advisor：Dr. Albert Chin

國 立 交 通 大 學

電子工程學系電子研究所

碩 士 論 文



A Thesis

Submitted to Department of Electronics Engineering & Institute of Electronics

College of Electrical and Computer Engineering

National Chiao Tung University

in Partial Fulfillment of the Requirements

for the Degree of Master

In

Electronics Engineering

June 2007

Hsinchu, Taiwan, Republic of China

中華民國九十六年六月

高介電常數金屬-絕緣層-金屬電容電性及其可靠度之研究

研究生：陳冠麟　　指導教授：荊鳳德教授

國立交通大學

電子工程學系電子研究所碩士班

摘要

在射頻積體電路中，其阻抗匹配電路、濾波器和類比頻率調節電路都會用到金氧金電容。而對於動態隨機存取記憶體來說，金氧金電容是為了用於儲存電荷，並且會影響到記憶體的一些參數，像是工作電壓、元件速度和資料保留的時間。然而不管是射頻積體電路還是動態隨機存取記憶體的電容，都會占掉大量的晶片面積。所以為了減少晶片面積和成本，我們必須縮小金氧金電容的尺寸。

在這次研究中，我們作出以高介電常數鈦鉭氧化物為介質層的金氧金電容。從元件的量測結果中，我們得到非常高的電容密度值為 23 fF/um^2、從十萬赫茲（100K Hz）到一百億赫茲（10G Hz）只 1.8 %的電容損耗。同時在十億赫茲頻率下（1G Hz），從量測的散射參數計算出低於 550ppm 的電壓相關電容值。由上述數據可知，此金氧金電容可適用於工作在射頻頻率的高精密積體電路上。同時，我們也研究了此電容在固定偏壓一段時間後的電容值、漏電流以及電壓相關的電容值。

The Research of Electric Characteristics and Reliability of High-κ MIM Capacitors

Student: Guan Lin Chen **Advisor: Dr. Albert Chin**

Department of Electronics Engineering

& Institute of Electronics

National Chiao Tung University

Abstract

In RF integrated circuits, MIM capacitors are used for impedance matching, filter and analog frequency tuning circuits. For DRAM, MIM capacitors are used to storage charges; they will influence some parameters of the memory, such as work voltage, device speed, and the data retention time. However, the capacitor area of above all usually consumes a large portion of the whole chip size. In order to reduce chip size and cost, we must continue scaling down the size of MIM capacitors.

In this study, we have fabricated MIM capacitors using high-κ TiTaO dielectrics. From the measurement of devices, a very high capacitance density of 23 fF/μm^2 is obtained, with small capacitance reduction of 1.8 % from 100 KHz to 10G Hz. And Small voltage dependence of capacitance < 550 ppm, mathematical derived from S-parameters, is obtained at 1G Hz, which ensures this MIM capacitor useful for high precision circuits operated at RF regime. We also have investigated the characteristic of capacitance, leakage, and $\Delta C/C_0$ before and after constant-voltage stress.

誌　　謝

首先，要感謝的是我的指導老師荊鳳德教授，在這兩年的碩士研究生涯裡所給予熱心的指導和教誨，使得我不論在研究上或是待人處事上都有很大的收穫，在此衷心的表達感謝之意。

再來，我要感謝鄭淳護學長以及江國誠學長，謝謝你們對我在實驗儀器上的訓練以及研究上所提供的意見和幫助，讓我得以順利的完成碩士學業。此外，軍宏學長、彬舫學長、建宏學長、存甫學長以及實驗室的學長姊們，感謝你們對我的教導和鼓勵。

接下來我還要感謝的是實驗室的同學，俊全、懿範、偉倫、哲偉、俊賢、建弦。有了你們，才讓我的研究生活充滿了歡樂與色彩，使我有動力繼續研究下去，感謝大家的支持與鼓勵，謝謝你們。

最後，我要對我的父母以及家人獻上最深的謝意與祝福，有了你們的栽培、支持與鼓勵，才讓我有今日的表現。

Contents

Figure Captions

Chapter 1 Introduction

Chapter 2 The Experimental Steps and Measurements

Chapter 3 Result & Discussion

Chapter 1

Introduction

1-1 Motivation to study high-κ materials

Silicon oxide is the conventional dielectric material in semiconductor and is used broadly, because it can be manufactured easily and has a great isolated performance. Since 1994, International Technology Roadmap for Semiconductors (ITRS) has made a roadmap for steady reduction in silicon device size, with an accompanying improvement in device performance, measured predominantly by circuit speed. However, in the scaling of CMOS devices, reducing the thickness of gate stack will cause two problems. One is that the tunneling effect will be occurred when the thickness of silicon dioxide is below a certain thickness. Therefore, the leakage current density of device will increase exponentially with the continuing scaling thickness of the gate dielectric film. The other is that the larger leakage current will cause that electrons can not be accumulated in the channel, and let the driving current of the device degrade. This problem will cause the circuit speed down.

For maintaining high driving current of the CMOS devices without large leakage current, it can be achieved by applying the dielectric with high dielectric constant (high-κ). It can increase the physical thickness of the high-κ dielectric film of the device without the reduction of capacitance density. Since the leakage current is related greatly to the physical thickness, the increasing thickness of high-κ dielectric film can reduce the leakage current of the devices. Although there are several drawbacks about the high-κ dielectrics, such as smaller band gap, weaker bond, and higher defect density than SiO_2, the high-κ dielectrics with the same effective oxide thickness (EOT) with SiO_2 still shows lower leakage current than SiO_2 by several orders [1-1][1-2]. That's why high-κ dielectrics have drawn much attention for future technology.

According to the ITRS of SIA (Semiconductor Industry Association) as shown in Fig. 1-1[11-3], it shows that the thickness of gate oxide has to be below 10 Å after 2008. Besides, the bias voltage and gate length reduces by 11 % every year while the drive current has to be maintained. Therefore, it is necessary to continue to scale down the size of the gate dielectric in proceeding CMOS technology. However, at the generation of sub-100nm, the operation frequency of the device will be over GHz, and the performance of high-κ dielectrics over GHz is a key point for the use of high-speed devices. Even some high-κ dielectrics show good electrical characteristics at low frequency, the performance of those at RF regime could possibly degrade. Therefore, it is important to find out the high-κ materials that exhibit superior characteristics at both high and low frequency.

Many material systems are currently under consideration as potential replacements for SiO_2 as the gate dielectric for sub-100 nm COMS technology. A systematic consideration of the required properties of the high-κ gate dielectric indicates that the key guidelines are (a) permittivity, band-gap and band alignment to silicon, (b) thermodynamic stability, (c) film morphology, (d) interface quality, (e) compatibility with the current or expected materials to be used in processing for CMOS devices, (f) process compatibility, and (g) reliability. Especially, it becomes more and more important about the aspect of device reliability. Many dielectrics appear favorable in some of these fields, but very few materials are promising with respect to all of these guidelines.

Recently, some high-κ dielectrics have been researched widely. The characteristics and issues of those materials have also been reported. The high-κ dielectrics which show good performances are always with some defaults. Finding out the most suitable high-κ dielectrics as the gate dielectrics of devices and altering the structures of devices or process to meet the requirements of the high-speed devices are significant tasks to the next VLSI generation.

1-2 High-κ materials for MIM

1-2.1 High-κ MIM for RF analog application and DRAM

To extend the scaling of the device size with less power consumption is the most significant application for high-κ materials. Once the scaling is stopped due to the unacceptable power consumption and bad device reliability, the operation frequency of the devices cannot have chances to be raised to higher value. Not only the bandwidth of communication cannot be broadened, but also the limits of operation speed of microprocessors appear. The gate dielectrics, no doubt, are the core of CMOS devices, which are the main devices of any integrated circuits. Therefore, to replace conventional oxide with high-κ dielectric is an inevitable and significant application in the next generation of VLSI technology.

At the moment, the high-κ MIM (metal-insulator-metal) capacitors have attracted great attention in silicon IC applications because of their high conductive electrode and low parasitic capacitance. The RF MIM capacitors are extensively used for filter, coupler, network matching and mixed-signal IC. But the total capacitor area usually consumes a large portion of the whole chip size.

The requirements for RF MIM capacitors include high capacitance density, less leakage current, low VCC and TCC, low parasitic effect, precision control of value at high frequency and good reliability [1-4]. However, in order to increase the capacitance density for reducing the area occupied by capacitors, utilizing thin dielectrics with high dielectric constant is a best method of all. Recently, some kinds of dielectrics and deposited approaches have been proposed to achieve the goal of high capacitance and the other good performance. For example, instead of SiO_2 dielectric with Si_3N_4 deposited by plasma enhanced chemical vapor deposition (PECVD) has been studied in the past years [1-5] [1-6]. Although Si_3N_4 shows good linearity and reliability, the capacitance density still needs to be increased. However,

Si_3N_4 fabricated by PECVD has the minimum thickness limit and the defect density of nitride is high. Therefore, finding high-κ dielectrics with good linearity and quality is a front-burner issue to develop the innovative and useful RF capacitors [1-7].

There are also the same problems in DRAM. The basis of DRAM is one transistor and one MIM. A MIM capacitor of a memory cell is used to storage charges to analyze the signal which is 0 or 1 and it will influence some parameters of the memory, such as work voltage, device speed, and the data retention time. It is difficult to determine the data exactly when the scaling of the device is going on. Because the smaller area of a memory cell causes the smaller signal. If we want to maintain the charge in the capacitor, it is must to raise the value of capacitance density. For this issue, the best way is also to use high-κ materials as the dielectrics of MIM. The merits and demerits of various high-κ materials will be discussed in the next section.

1-2.2 Background of high-κ dielectrics

There are two methods to achieve higher capacitance density ($\varepsilon_0\kappa/t_\kappa$) for scaling down device size. One is to decrease the dielectric thickness (t_κ) and the other is to use high-κ materials. The former way will rapidly increase the undesired leakage current, loss tangent, voltage dependence of capacitor ($\Delta C/C_0$) and reliability. So, the latter one is the only method to make it without increasing leakage current. To achieve this goal, the high-κ dielectric in RF MIM capacitor is continuously changed from SiON (κ~4-7), Al_2O_3 (κ~10) to Ta_2O_5 (κ~25), TiO_2 (κ~80) or HfO_2 (κ~25), ZrO_2 (κ~25) [1-8] [1-9].

Recently, HfO_2 and ZrO_2 have attracted much attention due to their thermal stability with poly silicon, TiN and TaN [1-10] [1-11]. In addition, they not only exhibit suitable dielectric constant (25~30) and high energy band gap (see Fig. 1-2) as the dielectrics of the devices, but also can be deposited on silicon without the use of the barrier layers [1-12].

However, oxygen tends to diffuse though HfO_2 and form oxide interlayer after high temperature process and it becomes difficult to achieve the effective oxide thickness below 10 Å. Furthermore, the boron penetration effect is occurred when a single HfO_2 layer serves as gate dielectric of transistors, while ZrO_2 reacts with poly silicon to form Zr silicide after post implant annealing. The above problems will cause low capacitor value and high leakage current. In addition, HfO_2 and ZrO_2 will crystallize at the temperature higher than 500^oC. After source/drain activation, this property increases the leakage current and power dissipation of the CMOS devices. The methods to improve these characteristics of HfO_2 and ZrO_2 can be divided into three parts. First of all, dense and thin capping layer was formed on the top of HfO_2 or ZrO_2 by sputtering thin metal film (Hf, Zr) on the top of these dielectrics followed by rapid thermal annealing (RTA) at 600^oC in N_2 to oxidize the nitride layer. Not only boron penetration can be reduced effectively, but also the oxygen diffusion can be suppressed [1-10]. Secondly, to overcome the thermal unstable properties and to remain the amorphous phase for HfO_2 and ZrO_2 after high temperature process, doping some thermal stable material into high-κ dielectrics has been proposed and shows the promising results [1-13] [1-14]. Finally, the NH_3-based interfacial layer can be effective in suppressing the diffusion of O_2 and subsequent growth of interfacial oxide [1-15].

Among the high-κ dielectrics using simple metal oxide, Ta_2O_5 and TiO_2 have the higher dielectric constants 25 and 80 respectively [1-16] [1-17]. In addition, Ta_2O_5 still exhibits other merits including the better capacitance linearity than that of SiO_2, the lower process temperature. However, some other issues about Ta_2O_5 should be noticed. First of all, crystallization and interface state will cause from post implant rapid thermal annealing. Moreover, interface oxide layer between Ta_2O_5 and Si occurs after crystallization. Thus, effective oxide thickness increases while interface oxide layer occurs and capacitance density also decreases [1-18].

It has been reported that TiO_2 has some better properties than other dielectrics in

addition to the higher dielectric constant value (~80). One of those is the good thermal stability when it was integrated with TiN electrode. It allows TiO_2 to show good dielectric characteristics after high temperature process for silicide formation [1-17]. Besides, the heat conduction rate of TiO_2 is higher than that of SiO_2. The issue of heat dissipation should also be considered with the scaling of integrated circuits. Although TiO_2 exhibits the above merits, there are still some other issues that should be considered and overcome such as the higher leakage current than that of other dielectrics with the same effective oxide thickness, lower breakdown voltage and interface oxide layer formation after RTA oxidation. According to the report, the thickness of the interfacial oxide layer can be reduced by using NH_3 plasma treatment, but the flat-band voltage shift and the degradation of channel mobility still occurred [1-19]. Therefore, the main problem of the TiO_2 is that its leakage current is too high to be used for dielectric. From detailed characterization, such large leakage current causes from the poly-crystallization of TiO_2 from amorphous state after annealing, which generates a high current conduction pass through the poly-grain boundaries.

However, the high annealing temperature (>500^{o}C), which is required to crystallize these high-κ materials, not only increases the roughness of the film but also results in lower breakdown voltage, and higher leakage current. It is also incompatible with the existing VLSI backend process integration. So, the difficult technology challenge for high capacitance density of MIM is to search suitable high-κ dielectric with good dielectric integrity when fabricated at a low process temperature (<400^{o}C) for VLSI backend process integration.

Another difficult challenge for RF MIM capacitor is to achieve small voltage dependence of capacitance used for precision circuit application. In addition, it is highly important to measure the voltage dependence of capacitance at RF frequency (>0.8 GHz). This is because the operation frequency of precision circuits is increasing into GHz range as continuous technology evolution.

The most important requirement of the MIM capacitors is that the oxide's κ value

should be high. There is a trade off with the band offset condition, which requires a reasonably large band gap. Figure 1-2 shows that the κ of candidate oxides tends to vary inversely with the band gap, so we must accept a relatively low κ value to keep out the leakage current.

To achieve the high capacitance density (>10 fF/μm^2), the dielectric TiO_2 is a potential candidate, since it can display very high κ value (~80). But, the large leakage current from crystallization of the TiO_2 is a major limitation for device applications. In order to improve the leakage current problem, we dope the high-κ material which has higher band gap and higher κ value to suppress the leakage current [1-20]. Here we report the use of TiTaO as the dielectric, and show capacitors with lower leakage current after backend processing. We report devices with a record high density of 23 fF/μm^2 at 0 V, a κ value of 45, and low leakage current of 1.89×10^{-6} A/cm^2 at -1 V. This performance of the TiTaO MIM capacitors is accompanied by a small voltage-dependence of capacitance ($\Delta C/C_0$) of only 550 ppm at 1GHz.

1-3 The deposition technologies of high-κ dielectrics

Recently, several methods to deposit ultra thin high-κ dielectrics on substrates have been reported and each of them exhibits the merits as well as some other issues that have to be solved.

Among the methods of the deposition of ultra thin high-κ film, metal organic chemical vapor deposition (MOCVD) is the method extensively used in VLSI fabrication. The deposition of high-κ film has been achieved by using metal organic precursor vapor. The precursors are introduced into low-pressure chamber and the substrate is heated to the suitable process temperature. The uniform and conformal deposition of dielectrics can be obtained. That is the reason why MOCVD process is integrated into fabrication process flow extensively [1-21]. Although MOCVD has so many merits, it still exist some issues such as the carbon contamination and the impact of precursors to the environment, health and safety.

Atomic layer chemical vapor deposition (ALCVD) is the another way used extensively in fabrication to deposit high-κ film and has attracted much attention due to its self-limit and mono-layer deposition properties [1-22]. ALCVD is the method using MCl_4 (M: Hf, Ti, Zr…) and H_2O as sources to deposit high-κ film (ie. HfO_2, TiO_2, ZrO_2…). The precursors are introduced into the heated chamber and substrates. The reaction only happens on the substrate surface instead of the deposited layer and one layer is deposited at a time. Thus, the thickness of dielectrics can be controlled precisely and is dependent on the process cycles linearly. The excellent uniformity of deposition can be achieved on SiO_2 and Si_3N_4 films, but the deposition on H-terminated Si substrate can lead to rough surface. However, H-terminated Si substrate is inevitable after HF dipping. Therefore, the improvement of process precursor is the key point to overcome the issues of ALCVD.

Depositing the metal or metal oxide directly on the substrate using physical vapor deposition (PVD) method followed by thermal oxidation and annealing is the another

approach to deposit high quality dielectrics [1-12]. In the recent years, there have been many reports about this technology. The process flow is described as follows. The pre-processed wafer is loaded into high vacuum chamber. Then, the metal layer is deposited using reactive dc magnetron sputtering with oxygen modulation technique or the metal oxide is sputtered directly followed by annealing. Although this method is compatible with the modern VLSI process, the formation of interlayer oxide and crystallization are still the issues that should be solved. By combining the nitridation and dielectric doping techniques, both of the problems mentioned above can be minimized. Therefore, this method is still promising due to the merits.

In this study, we used the PVD method to fabricate the high-κ dielectrics. Instead of nitridation, we utilized NH_3 plasma treatment to prevent from the formation of interface oxide. The pre-processed wafer was loaded into E-beam evaporator under high vacuum condition to deposit dielectric and then annealed at 400^{o}C in O_2 ambient for complete oxidation. The devices using TiTaO are fabricated and measured at low and high frequencies. More detailed fabrication process of high-κ TiTaO as the dielectric can be found elsewhere.

1-4 Thesis

In this thesis, we use the process of PVD technique for the deposition of high-κ dielectrics. By altering the sources of deposition, various dielectrics can be deposited on the substrates. Moreover, this simple process technique is able to integrate with front-end or back-end process. So, we take the above way to fabricate the Metal-Insulator-Metal capacitor using TiTaO material as the dielectric. At low frequency, the results shows that TiTaO as the thin film of the dielectric can make the capacitance density up to 23 $fF/\mu m^2$ at 0 V and the leakage current is 1.89×10^{-6} A/cm^2 low at -1 V.

Beside the measurement of leakage current density and capacitance at low frequency, we measured the S-parameters to investigate the characteristics of the MIM capacitors at RF regime. We also use an equivalent circuit model to derive the voltage-dependent capacitance coefficient (VCC) at RF frequency regime. TiTaO dielectric provides the special advantage, such as a higher permittivity (~45); low normalized capacitance change ($\Delta C/C_0$) with a small value ~550 ppm at 1 GHz; and low temperature-dependent capacitance coefficient (TCC). The good MIM capacitor integrity is suitable for precision circuit application at RF measurements.

In addition, few studies of the stress reliability of the analog characteristics of MIM devices have been reported [1-23] [1-24], beyond considerations of the simple time-dependent dielectric breakdown, despite its importance for circuit applications. This stress degradation is a concern in low-breakdown field and small-band-gap materials, which will lead to high leakage currents because of the small conduction band discontinuity (ΔE_C) with respect to Si [1-25]. Here we also described the stress reliability of the analog characteristics of TiTaO MIM capacitors in this thesis.

	Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
	DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	90	78	68	59	52	45	40	36	32
	MPU Physical Gate Length (nm)	32	28	25	22	20	18	16	14	13
	L_g: Physical L_{gate} for High Performance logic (nm) [1]	32	28	25	22	20	18	16	14	13
	EOT: Equivalent Oxide Thickness [2]									
IS	Extended planar bulk (Å)	12	11	11	10	9	6.5	5	5	
Delete	UTB FD (Å)				~~9~~	~~8~~	7	6	5	5
	DG (Å)							8	7	6
	Gate Poly Depletion and Inversion-Layer Thickness [3]									
IS	Extended Planar Bulk (Å)	7.3	7.4	7.4	7.0	7.0	2.7	2.5	2.5	
Delete	UTB FD (Å)				~~4~~	~~4~~	4	4	4	4
	DG (Å)							4	4	4
	EOT_{elec}: Electrical Equivalent Oxide Thickness in inversion [4]									
IS	Extended Planar Bulk (Å)	19.3	18.4	18.4	17.0	16.0	9.2	7.5	7.5	
Delete	UTB FD (Å)				~~13~~	~~12~~	11	10	9	9
	DG (Å)							12	11	10
	$J_{g,limit}$: Maximum gate leakage current density [5]									
IS	Extended Planar Bulk (A/cm^2)	1.88E+02	5.36E+02	8.00E+02	1.18E+03	1.10E+03	1.56E+03	2.00E+03	2.43E+03	
Delete	UTB FD (A/cm^2)				~~7.73E+02~~	~~9.50E+02~~	1.22E+03	1.38E+03	2.07E+03	2.23E+03
	DG (A/cm^2)							6.25E+02	7.86E+02	8.46E+02
	V_{dd}: Power Supply Voltage (V) [6]	1.1	1.1	1.1	1	1	1	1	0.9	0.9

Fig.1-1 The International Technology Roadmap of SIA for semiconductor 2006.

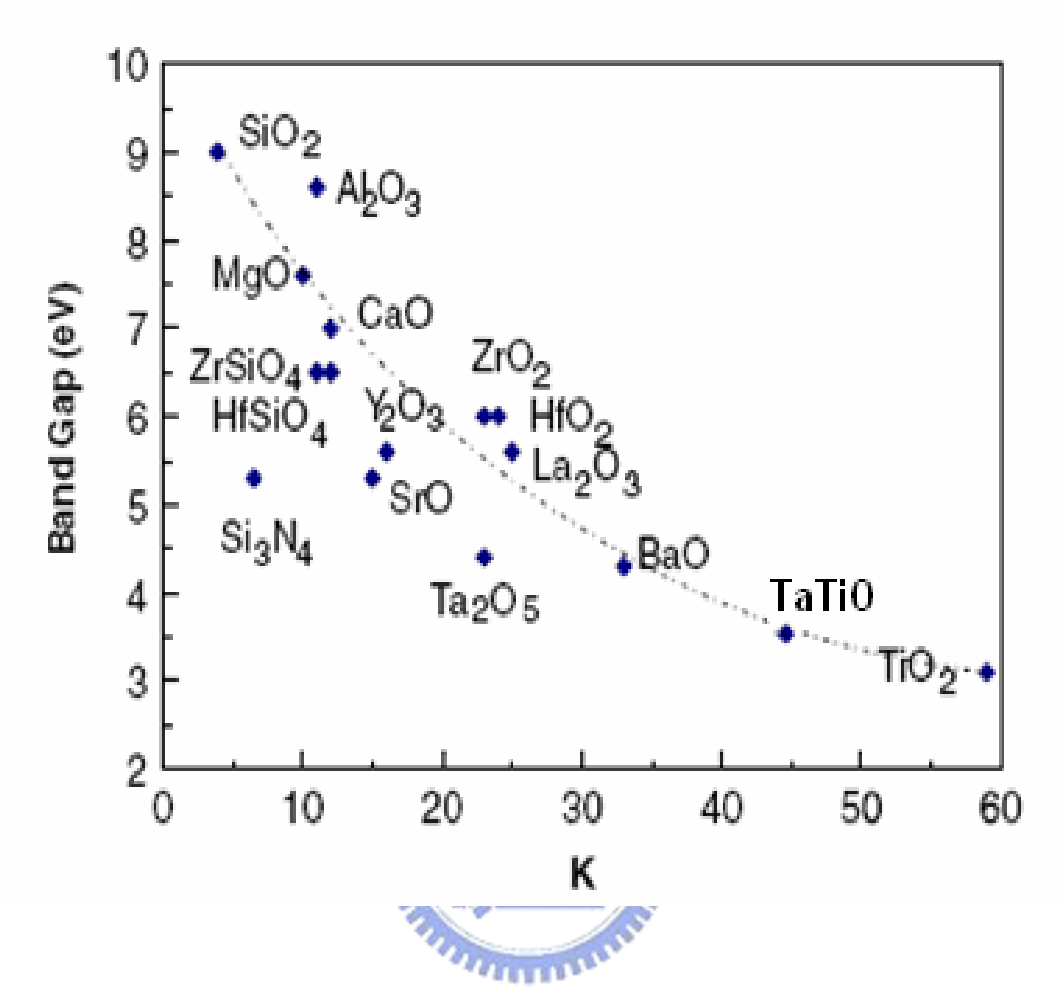


Fig.1-2 Static dielectric constants versus energy band-gap for candidate gate oxides.

Chapter 2

The Experimental Steps and Measurements

2-1 MIM capacitors fabrication

The MIM capacitor in this work, we used a standard 4-in p-type silicon wafer (100) as the substrate and pre-processed with RCA clean. Additional 5000 Å thermal oxide was first deposited on the substrate for VLSI back-end process integration. Then coplanar transmission lines with GSG probe were fabricated on oxide-isolated silicon substrates using deposited TaN/Ta bi-layer followed by subsequent patterning [2-1] [2-2]. The bottom TaN/Ta metal electrode and transmission line are formed. And then we use NH_3 plasma treatment on the bottom electrode to suppress the diffusion of O_2 and the generation of the interfacial layer. Next, a plasma-enhanced chemical vapor deposition (PECVD) passive oxide was deposited for isolation and followed by patterning the major capacitors and the transmission lines region. Then $Ti_xTa_{1-x}O$ (x~0.6) was deposited on bottom TaN/Ta metal electrode and transmission line in a high vacuum chamber by Dual E-Gun Evaporation System, fallowed by subsequent oxidation and annealing at 400^oC in a furnace. The oxidation was performed only using dry O_2. This low temperature of 400^oC is due to the VLSI back-end process integration limitation. Two TiTaO thicknesses of 17nm and 29nm are formed, respectively. For comparison, the TiO_2 dielectric was also deposited.

The motivation of using TiTaO is to use higher κ (~80) property of TiO_2 and reduced low DC leakage using mixed dielectric similar to previous AlTaO study. So, we chose Ta_2O_5 as the dopant, which has better VCC and TCC in the present materials, in order to meet the ITRS roadmap requirement (VCC-α < 100ppm/V^2). Finally, Al metal was deposited and patterned to form both top capacitor electrode and RF transmission line.

The process of MIM will show in Fig. 2-1~ Fig. 2-10. The structure of the RF MIM

capacitor and the layout of this device are showed in Fig. 2-10 and Fig.2-11.

2-2 The measurements of MIM capacitors

To analyze the electrical characteristics of these devices, we have measured the leakage current and stress-induced leakage current using HP 4156A semiconductor parameter analyzer. Besides, HP4284A precision LCR meter was used to evaluate the capacitance before and after constant voltage stress over a frequency range from 100 kHz to 1 MHz. Furthermore, to investigate the characteristics of our devices at the frequency above 1 MHz, we measured the scattering parameter using HP8510C network analyzer from 50MHz to 10GHz and de-embedded from a dummy device [2-1]-[2-4]. Network analyzer generates a calibrated RF signal and has three input measuring channels, which are commonly called the R, the A, and the B channels, respectively. The R channel is used to measure the incident voltage, and the A and B channels measure reflected and transmitted voltages. Then, we obtain S_{11} and S_{21} by calculating A/R and B/R in polar form, respectively. The S_{12} and S_{22} also are obtained using the same way except changing the input voltage channel. Next, the high frequency capacitance was extracted by using a physically based equivalent circuit model reported previously [2-3]. The $\Delta C/C_0$ and quadratic voltage coefficient at RF frequency are derived mathematically from measured S-parameters and circuit theory.

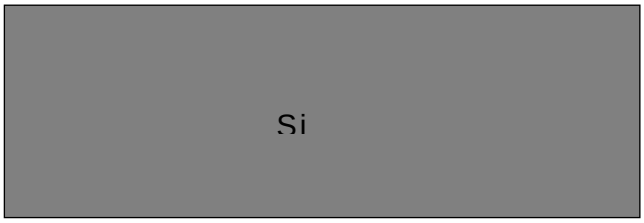


Fig.2-1 Silicon substrate.

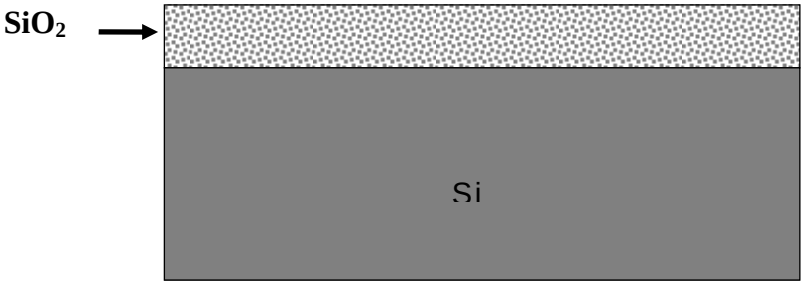
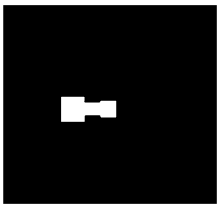


Fig.2-2 Silicon dioxide growth.

MASK#1



PR lithography patterning

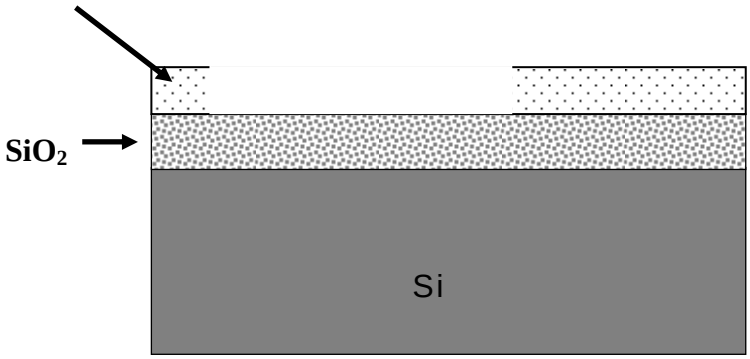


Fig.2-3 Photoresist deposition and lithography patterned.

Bottom electrode + TL

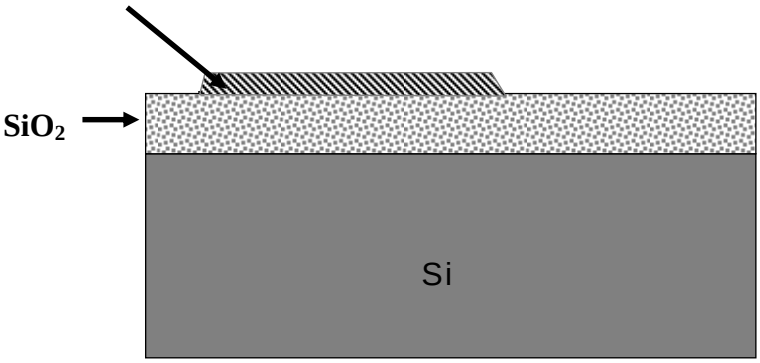


Fig.2-4 Deposited TaN/Ta bottom electrode and lifted out the photoresist.

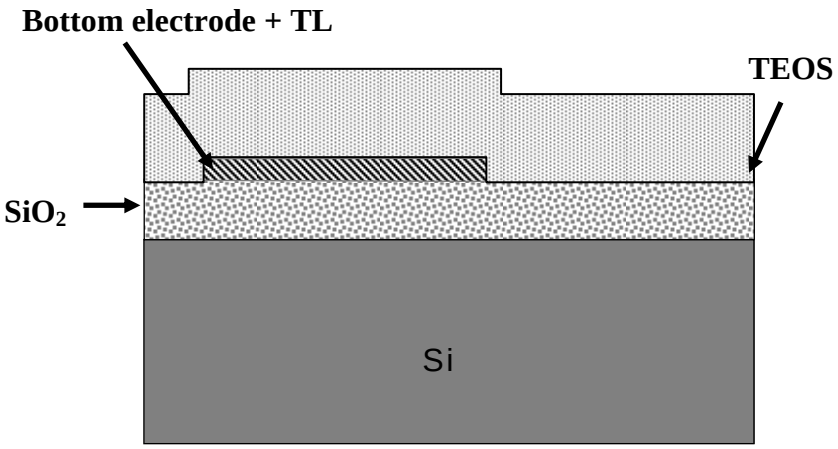
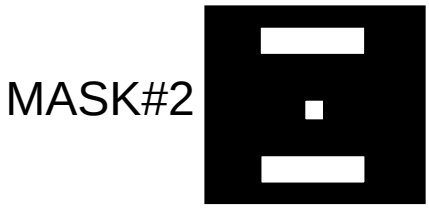


Fig.2-5 Deposited TEOS.



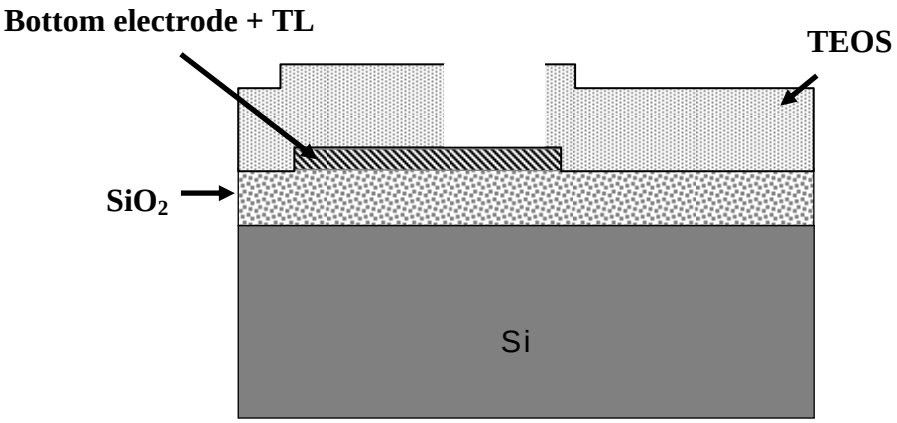


Fig.2-6 Lithography patterned and etched.

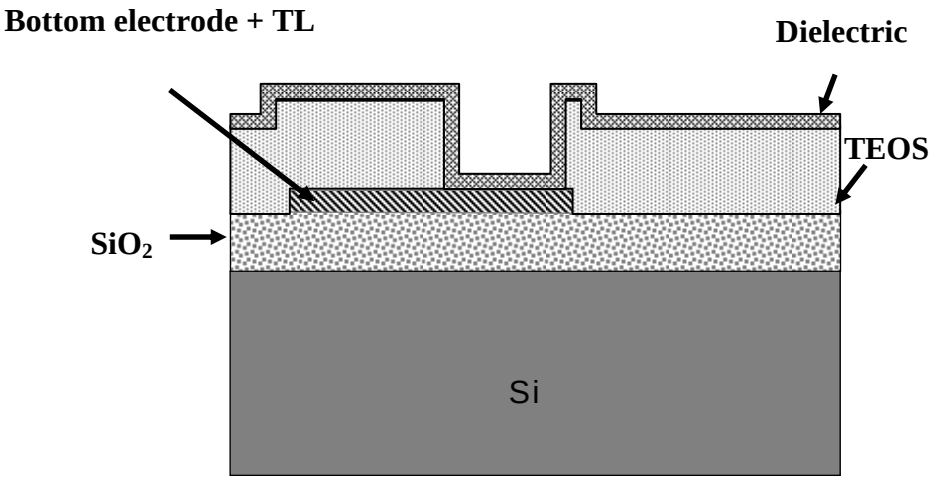
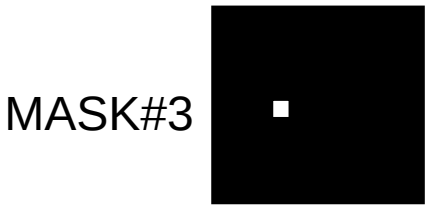


Fig.2-7 Deposited TiTaO followed with oxidation and annealing at 400°C and O_2.



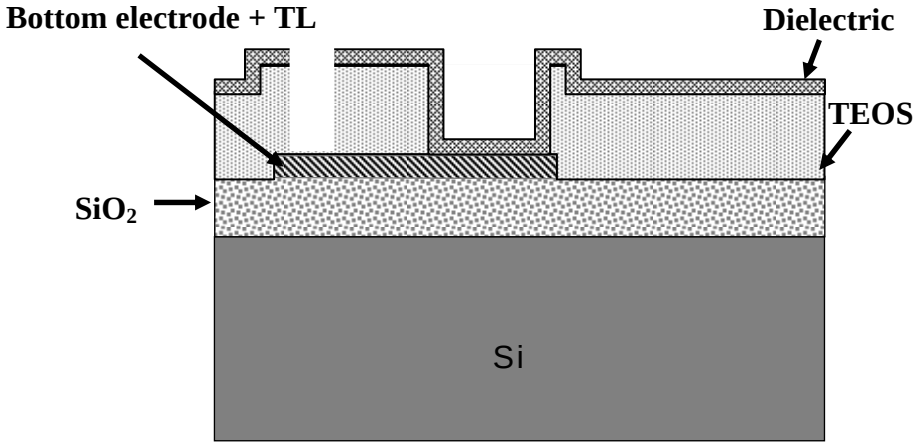


Fig.2-8 Lithography patterned, and etched.

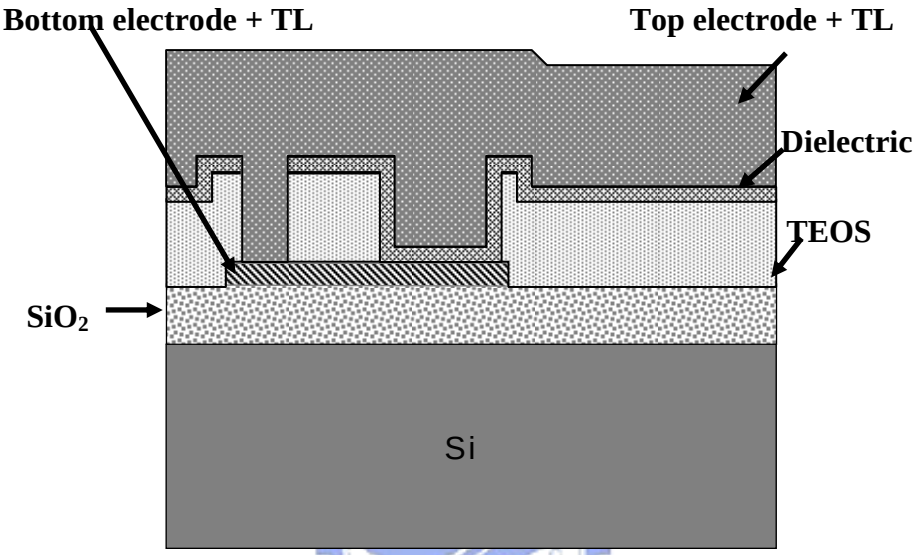


Fig.2-9 Deposited Al top electrode.

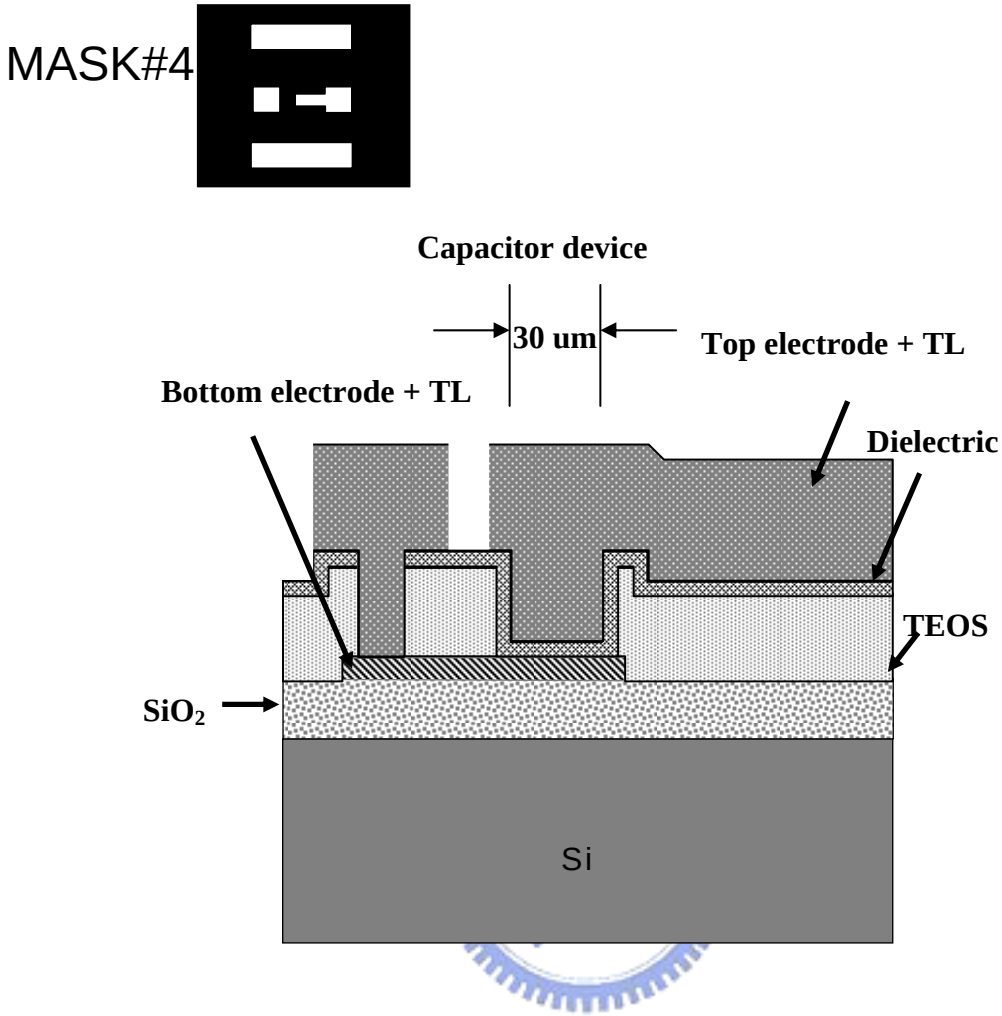


Fig.2-10 Lithography patterned, etched and the complete device cross-section.

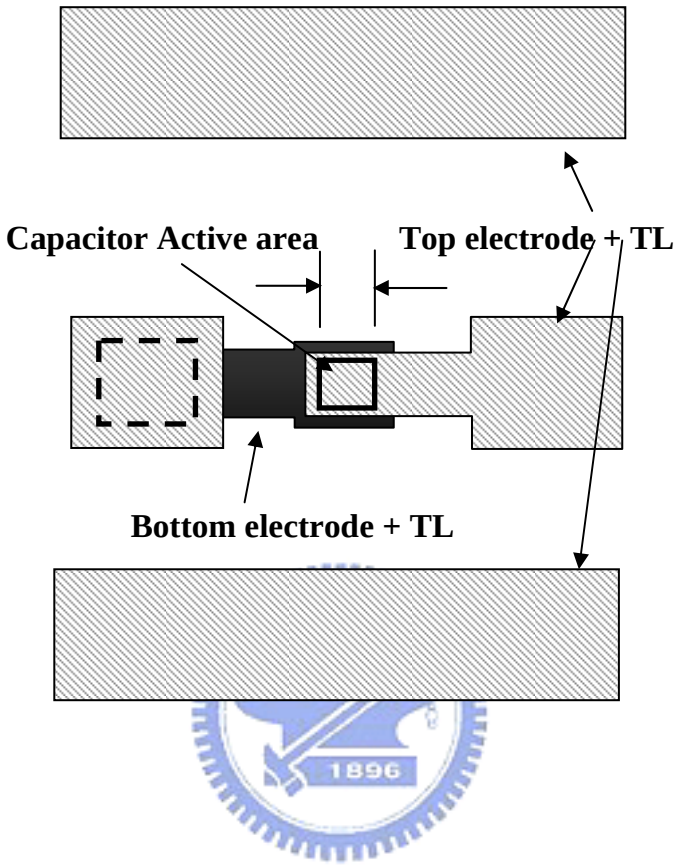


Fig.2-11 Top cell view of a RF MIM capacitor.

Chapter 3

Result & Discussion

3-1 Low frequency characteristics

We first measured the low-frequency capacitance ranging from 10 KHz to 1 MHz. Figure 3-1 shows the C-V and the J-V characteristics of TiTaO MIM capacitors with two different high-κ dielectric thicknesses. In Fig 3-1, capacitance densities of ~23 and ~14 fF/μm^2 were measured at 0 V for respective 17 nm (EOT~1.5nm) and 29 nm (EOT~2.45nm) thickness of physics. The dielectric constant (κ) can be obtained by physical thickness and capacitance value. Therefore, we get a κ value of 45 in TiTaO dielectric. Figure 3-2 shows the C-V characteristics of TiTaO and TiO_2 MIM capacitors. However, the TiO_2 MIM capacitor showed an abnormal capacitance variation at voltages above ±0.75 V. In contrast, constant capacitance values at -1 V~1 V region, with little voltage and frequency dependence, were found for the TiTaO MIM capacitor.

In Fig 3-1, the leakage current increases with decreasing the thickness of the TiTaO film, by trading off the increasing capacitance density. Leakage currents of 1.89×10^{-6} and 6.06×10^{-7} A/cm^2 were measured at -1V for respective 17nm and 29 nm thickness of physics. To investigate the abnormal large capacitance variation in TiO_2 capacitors at applied voltage > 0.75 V (or < -0.75 V), we have also plotted the characteristics of DC Current-Density versus Voltage (J-V) of the TiO_2 capacitors. The poor C-V for the TiO_2 MIM capacitor is related to its large leakage current, as shown in Figure 3-3. It may be due to the current conduction through grain boundaries of the poly-crystalline of TiO_2 [3-1]. The TiTaO MIM capacitors have ~5-7 orders of magnitude lower leakage current than that for the TiO_2 devices. We also can find out the J-V curves shown in Fig. 3-1 and Fig. 3-3 of the TiTaO MIM capacitors are asymmetrical. Although the work function of top Al electrode (4.1eV) is lower than that of

bottom TaN electrode (4.5eV), the leakage current, injecting electrons from the Al contact, is lower than that from the TaN bottom electrode. This is due to the better interface for the Al, which also gives better voltage and frequency dispersion in the C-V curves. Because after oxidation and annealing at 400°C in a furnace, there will have a generant interfacial layer (TiTaON) and more defects between the bottom electrode and the dielectric film.

The TCC and quadratic VCC (VCC-α) are important figures of merit for the MIM capacitors. The voltage non-linearity is classically described by the polynomial law:

$$C(V) = C_0 (\alpha V^2 + \beta V + 1) \quad (1)$$

$$\Delta C/C_0 = \alpha V^2 + \beta V \quad (2)$$

where $\Delta C = C(V) - C(0)$, C_0 is the capacitance at 0V, and α and β are the quadratic and linear coefficients of capacitance[3-2]. Figure 3-4 shows the characteristics of the normalized capacitance density ($\Delta C/C_0$) versus V of the TiTaO MIM capacitors with physical thickness of 17nm and 29nm. But according to Fig. 3-5, $\Delta C/C_0$ is almost related with quadratic electric field inversely [3-3]. Therefore, we can find that the $\Delta C/C_0$ becomes better (smaller) for thinner TiTaO thickness at the constant voltage. It is the key point to choose the thickness to obtain the lower leakage current and better $\Delta C/C_0$. There are several mechanisms to discuss the varying $\Delta C/C_0$ and capacitance value with increasing frequency, such as the presence of traps near the metal-insulator interface, the occurrence of free carrier space charge relaxation, or nonlinearities of the metal-oxygen bond polarizability [3-4] ~ [3-6].

Fig. 3-6 shows the $\Delta C/C_0$ of the 17-nm dielectric thickness of the TiTaO MIM capacitors as a function of temperature.

$$C(V) = C_0 (TCC \times V + 1) \quad (3)$$

The measured temperature coefficient of capacitance (TCC) is 429, 354 and 329 ppm/°C for respective 10 kHz, 100 kHz and 1 MHz. It is noticed that both TCC and $\Delta C/C_0$ decrease monotonically with ln(1/C), and comparable values are obtained with previous HfO_2 data at the same 1/C by extrapolation[3-7].

3-2 High frequency characteristics

We have measured the S-parameters to further investigate the RF frequency characteristics, beyond the 1 MHz upper limit of precision LCR meter. Fig. 3-7 shows the measured S-parameters for TiTaO MIM capacitors. The RF frequency capacitors can be extracted from S-parameters by using the equivalent circuit model shown in Fig. 3-8 [3-8]. The C, R_P, L_S, and R_S in this model are the capacitor, parallel resistance, parasitic series inductance, and parasitic series resistance respectively. The shunt R_P and C are the basic equivalent models for high-κ capacitor and small series R_S and L_S are formed the model of the connected transmission lines. The capacitance value were measured directly using the LCR meter from 10 KHz to 1 MHz and calculated up to 10 GHz from the measured S-parameters by using the following equation (4) and equation (5) [3-9].

$$S_{21} = \frac{2}{2 + Z(\varpi)/Z_0} \tag{4}$$

$$Z(\varpi) = R_s + j\varpi(L_{S1} + L_{S2}) + \frac{R_P / j\varpi C}{R_P + 1/j\varpi C} \tag{5}$$

where Z_0 is the characteristic impedance of transmission line and Z(ω) is the total impedance between two ports shown in the equivalent circuit model of Fig. 3-8, which is frequency-dependent. From known S_{21}, equation (4) and equation (5), the capacitance of TiTaO MIM capacitors at high frequency were obtained, as shown in Fig.3-9. The small capacitance reduction of 1.8% from 100 kHz to 10 GHz indicates good device performance over the IF to RF range.

The $\Delta C/C_0$ below 1 MHz can be calculated from C values measured by precision LCR meter, as shown in Fig. 3-1. However, the accuracy for $\Delta C/C_0$ obtained from the C-V data is not enough for RF frequency region. To achieve high precision $\Delta C/C_0$ at RF frequency, we have used equation (6) for this purpose [3-9]:

$$\frac{\Delta C}{C} = \frac{Z_0\left(2 + Z(\omega)/Z_0\right)}{2R_P^2} j\omega C^2 \left(R_P + 1/j\omega C\right)^2 \Delta(S_{21}) \qquad (6)$$

Based on the circuit theory derived equation (6), the high precision of $\Delta C/C_0$ shown in Fig. 3-10, can be obtained by differentiating the measured S_{21}, i.e., ΔS_{21} to enhance the small variation from S-parameters. The $\Delta C/C_0$ data, below 1 MHz and obtained from the precision LCR meter, is also plotted for comparison. Fast decreasing $\Delta C/C_0$ is observed with increasing from 1 MHz to 0.05 GHz (50 MHz).

To further study the frequency dependence, we also have plotted $\Delta C/C_0$, first order voltage linearity β and quadratic voltage linearity α from 100 kHz to 10 GHz, as shown in Fig3-9. A rapid decreasing $\Delta C/C_0$ (or α or β) with increasing frequency from 1 MHz to 100 MHz is observed as compared with other frequency range of either 100 KHz to 1 MHz or 100 MHz to 10 GHz. Because the typical carrier lifetime from trapped-related Shockley-Read-Hall (SHR) recombination is in a range from ms to μs, the fast reduction $\Delta C/C_0$ within the 1MHz to 100 MHz range may be due to the trapped carriers unable to follow the high frequency signals. The small $\Delta C/C_0$ of 550 ppm, low α of 81 ppm/V^2 and β of 98 ppm/V at 1 GHz are sufficient to meet the requirements of analog/RF IC applications.

3-3 Reliability

The effects of constant-voltage stress on capacitance, leakage current and $\Delta C/C_0$ of Al/TiTaO/TaN capacitor were investigated. After constant-voltage stress, the leakage current of a TiTaO MIM capacitor was lower than fresh one, as shown in Fig. 3-11. It was supposed that there is generation of the electron traps in the high-κ TiTaO dielectric and in the TaTiO/metal interface. And then, the trapped charges decrease the carrier mobility of electrons in the dielectric and lower the charge injection from the top electrode by electrostatic scattering, which in turn produces a smaller leakage current, according to a free-carrier-injection model [3-10]. Fig.3-11 also shows the thermal equilibrium-band diagram of Al/TiTaO/TaN structure after the constant-voltage stress.

Fig. 3-12 shows the C-V characteristics of the TiTaO MIM capacitors before and after constant-voltage stress. It can be seen that the capacitance density decreases with increasing stress time for the TiTaO MIM capacitors, and the curves have positive shift along voltage axis. Because the trapped charges in the dielectric will cause the voltage shift. Fig. 3-13 shows the $\Delta C/C_0$ characteristics below 1 MHz obtained from the data shown in Fig. 3-12 before and after constant-voltage stress. We can also find out that the $\Delta C/C_0$ decreases with increasing stress time as the same as the capacitance values. For this phenomenon, we can use electrode polarization mechanism that implies hopping carriers whose mobility is field dependent to clearly explain it [3-11]. The equation of this mechanism will be

$$\frac{\Delta C}{C_0} = \frac{2}{(\varepsilon_0 \varepsilon)^{2n}} \left(\frac{L}{L_D} \right)^{1-2n} \frac{1}{(\rho+2)^{2(1-n)}} \frac{1}{\varpi^{2n}} \sigma_0^{2n} \times \left[\exp\left({}^{nqEs}\!/\!_{\kappa_B T} \right) - 1 \right] \qquad (7)$$

where L is the film thickness and $L_D = (\varepsilon_0 \varepsilon \kappa_B T / Nq^2)^{0.5}$ is the Debye length, where N is the density of the mobile charges. Parameter ρ is the "blocking parameter," that accounts for electrode transparency. For ohmic contacts, ρ is large (no space charge). On the contrary, for blocking contacts, ρ is weak (no charge transfer at the electrodes in ac). σ_0 is the factor of conductivity $\sigma = \sigma_0 \times \exp(nqEs / \kappa_B T)$, where E is the high field (dc bias) in dielectric, s is the

hopping distance of mobile charges and n is about the empirical Jonscher universal law, where 2n = 0~1 [3-11]. These are all verified experimental factors.

This equation (7) predicts that $\Delta C/C_0$ should decrease with frequency (ω^{-2n}) and should increase with the leakage current (σ_0). Fig. 3-14 shows the characteristics of the VCC-α values versus constant-voltage-tress time at different frequencies. We can find out that the VCC-α becomes worse after constant-voltage stress and becomes better at higher frequency.

Altogether, the leakage current of a TiTaO MIM capacitor was lower, its capacitance and $\Delta C/C_0$ became smaller and the VCC-α was worse than before after the constant-voltage stress.

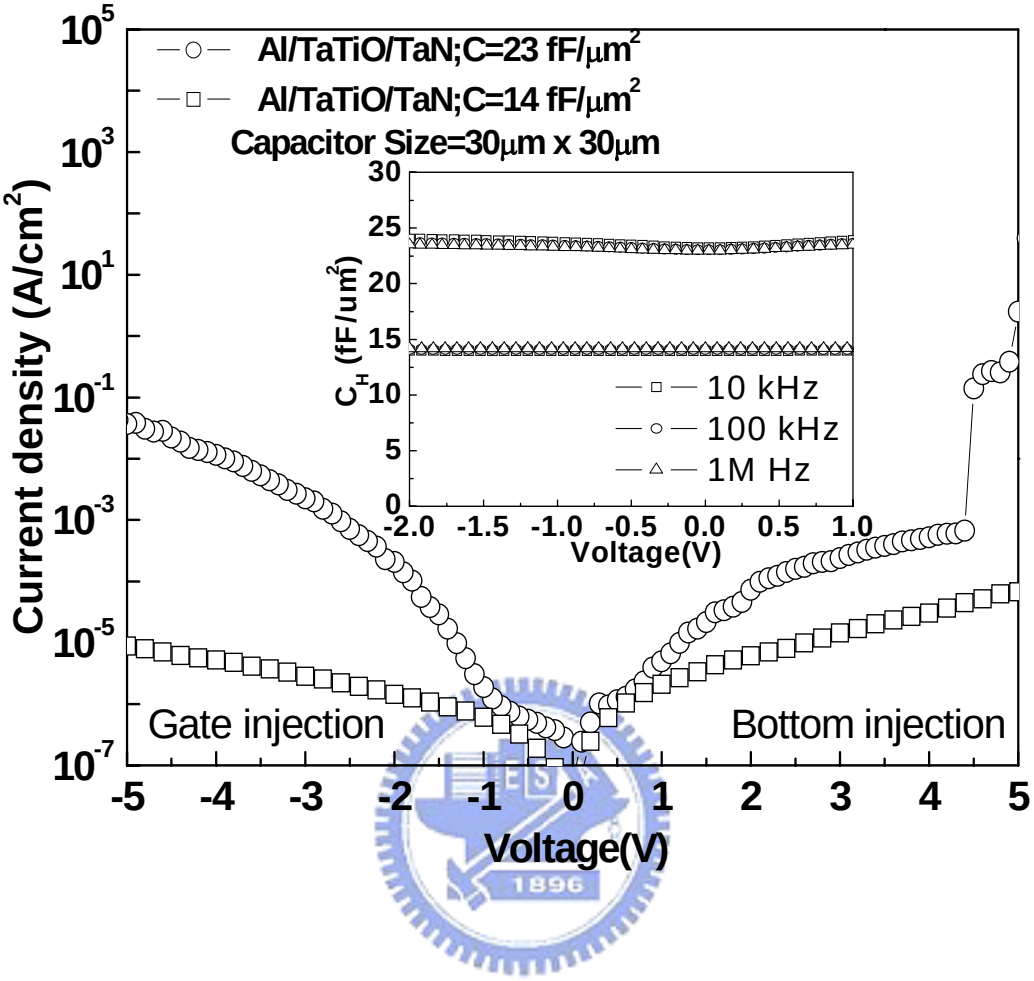


Fig.3-1 C-V and J-V characteristics of the TiTaO MIM capacitors measured from 10 kHz to 1 MHz. The data were measured by HP 4156A and HP4284A precision LCR meter.

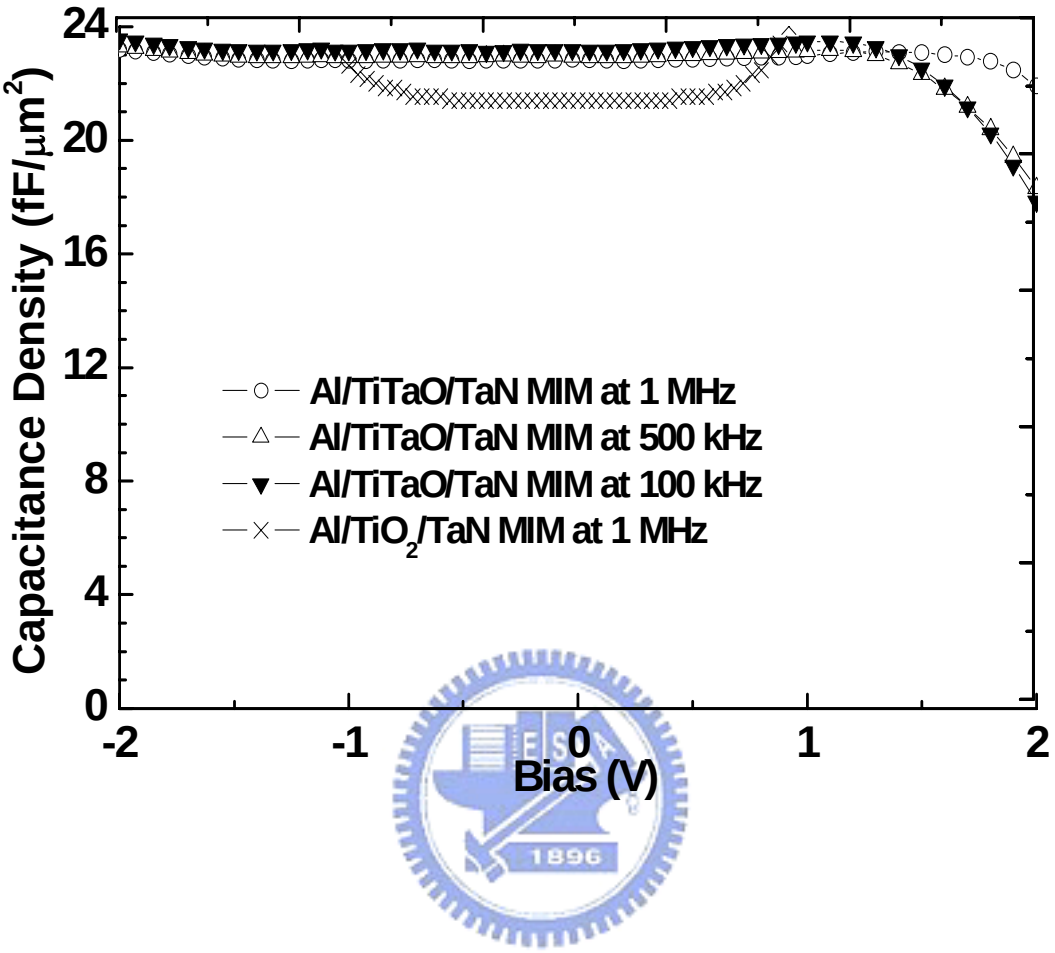


Fig.3-2 The C-V characteristics of TiO_2 and TiTaO MIM capacitors measured at different frequency. High capacitance density of 23 $fF/\mu m^2$ of TiTaO MIM capacitors were measured at 1 MHz with small capacitance variation.

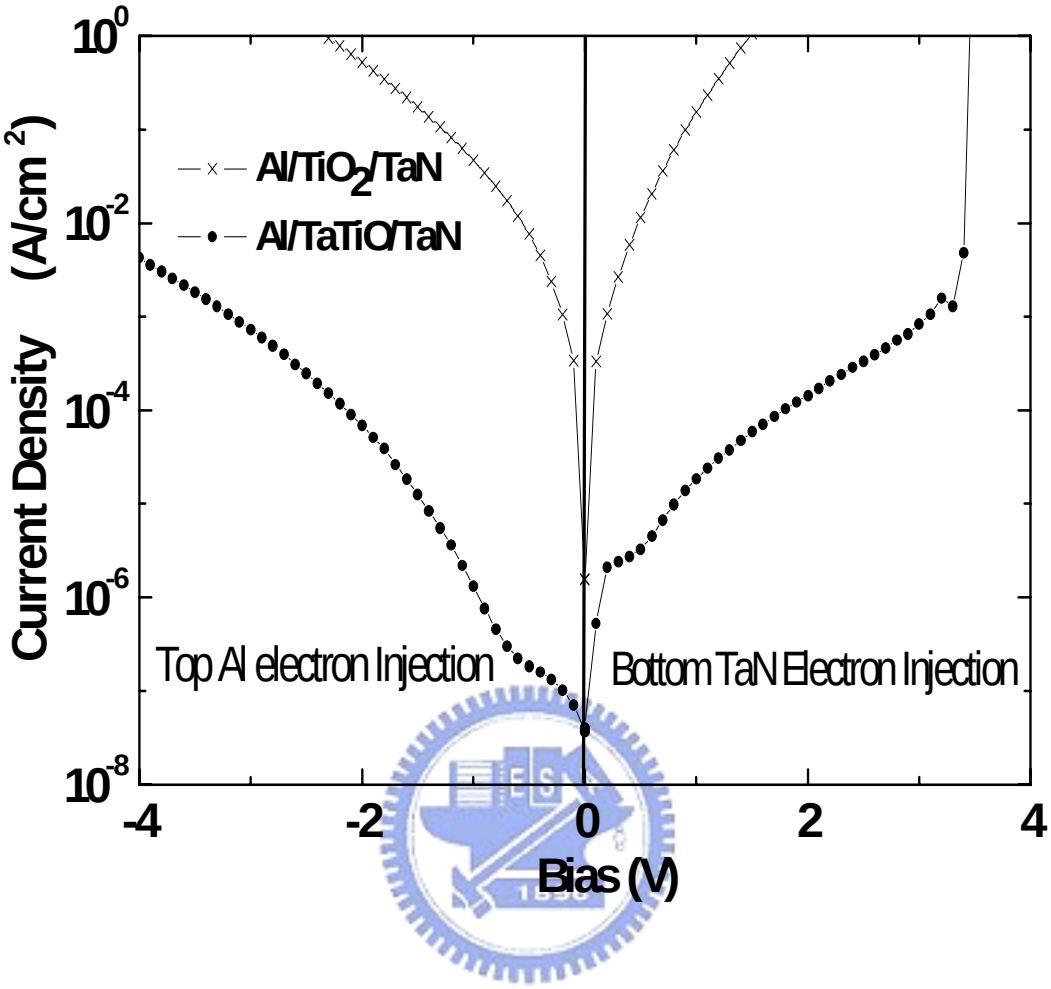


Fig.3-3 The J-V characteristics of TiO_2 and TiTaO MIM capacitors. The leakage current is lower for the TiTaO capacitors.

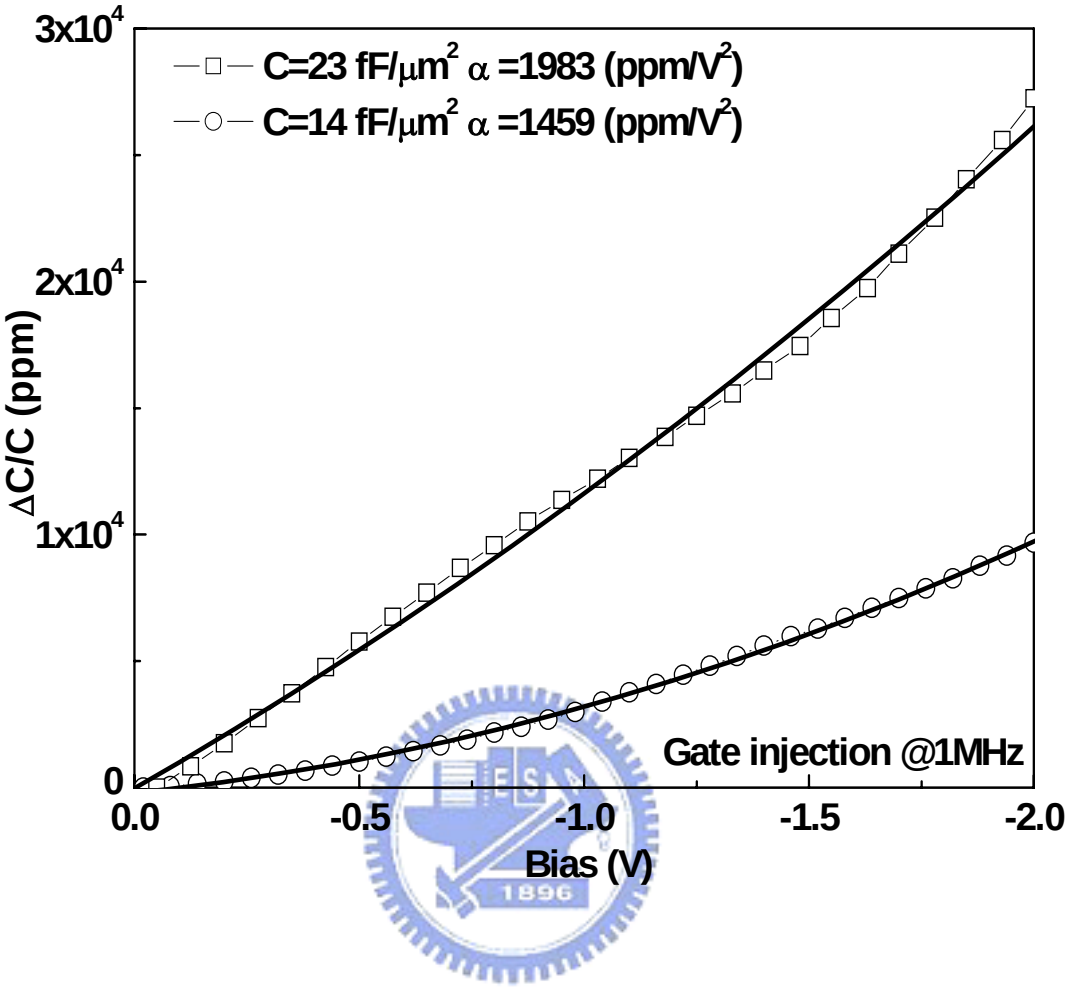


Fig.3-4 The characteristics of $\Delta C/C_0$ for the TiTaO MIM capacitors with dielectric thicknesses of 17nm and 29nm. The data were measured at 1 MHz.

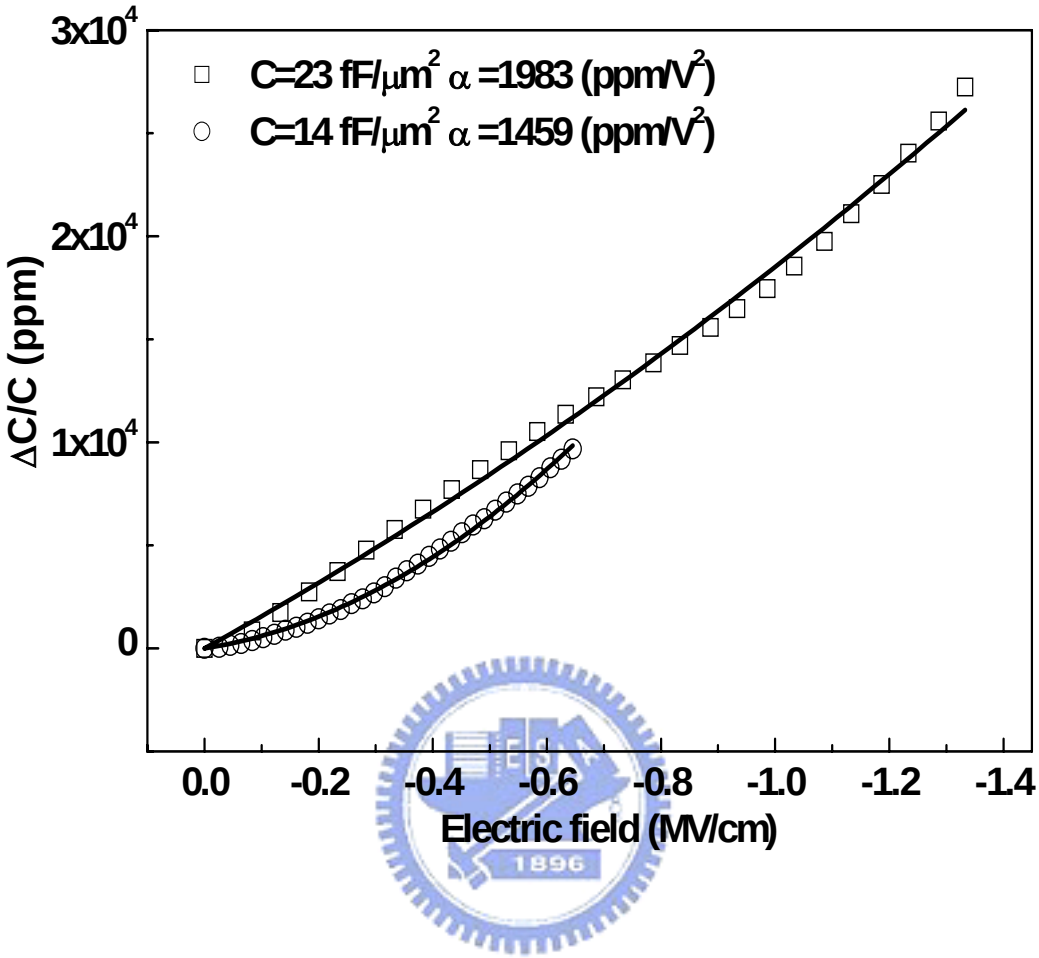


Fig.3-5 The polts of $\Delta C/C_0$ versus electric field (E) with different dielectric thickness. The reason for no matching together is that there are different gauge of trapped charges in the interface of the different thicknesses.

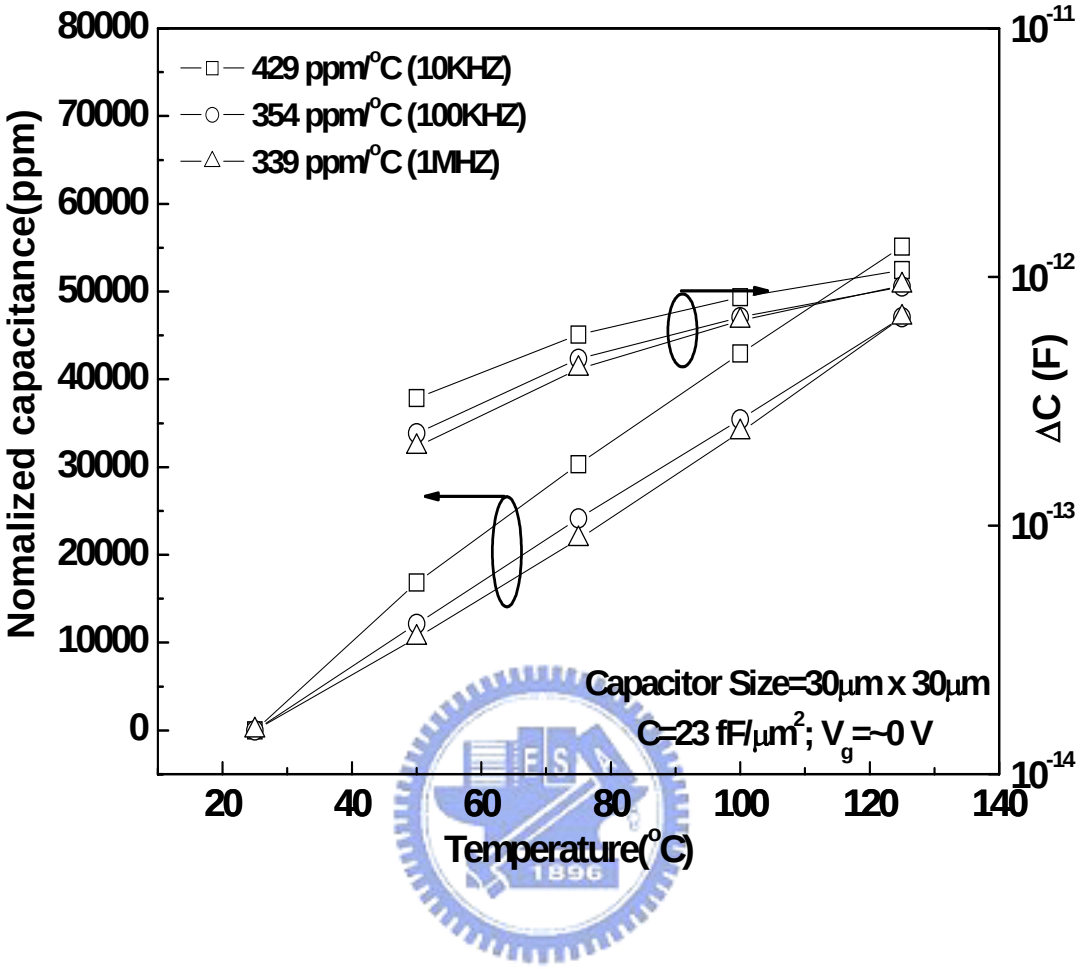


Fig.3-6 The characteristics of the Normalized capacitance of the TiTaO MIM capacitors as an approximate linear function of temperature.

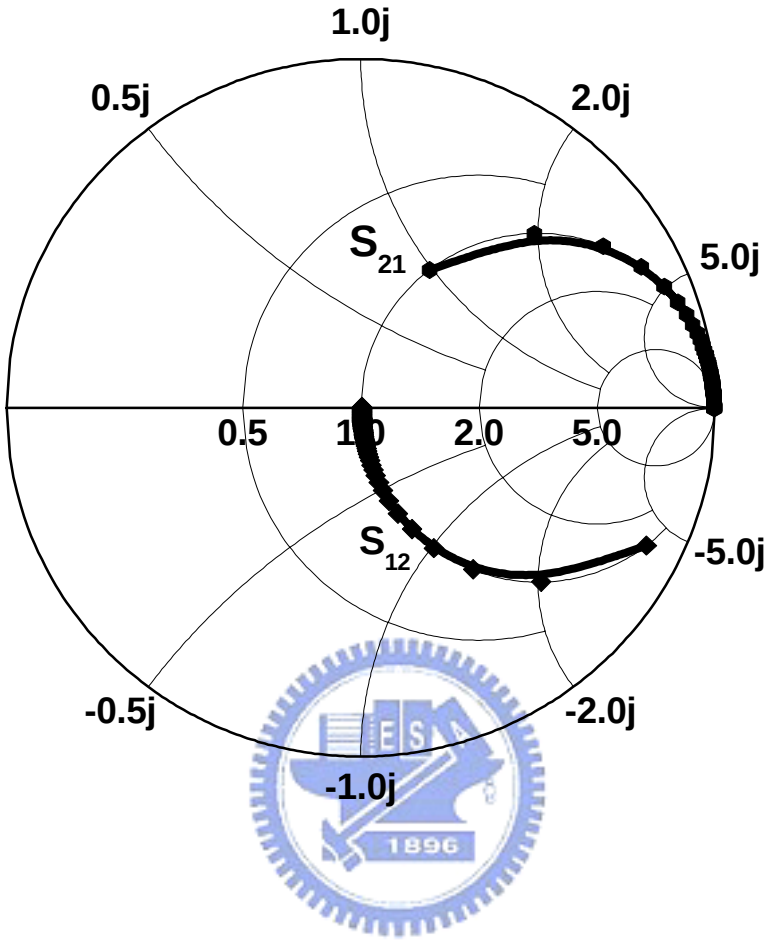


Fig.3-7 The measured scattering parameters of TiTaO MIM capacitors from 50 MHZ to 10 GHz.

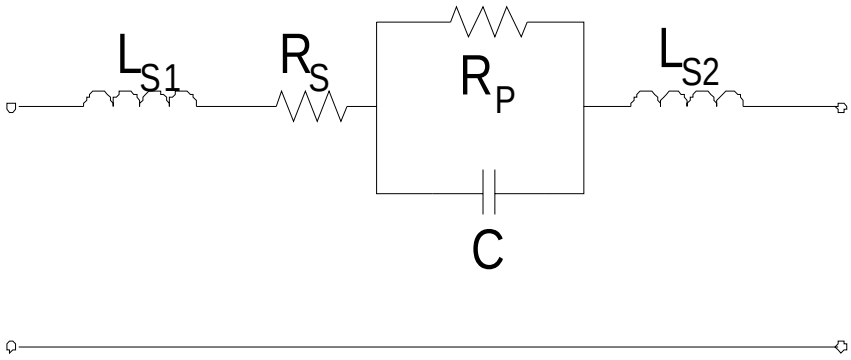


Fig.3-8 The equivalent circuit model for capacitor extraction. The C and R_P are the capacitance and its parallel resistance, and the L_S and R_S are the parasitic inductance and resistance from transmission lines connected between capacitor body and probing pads.

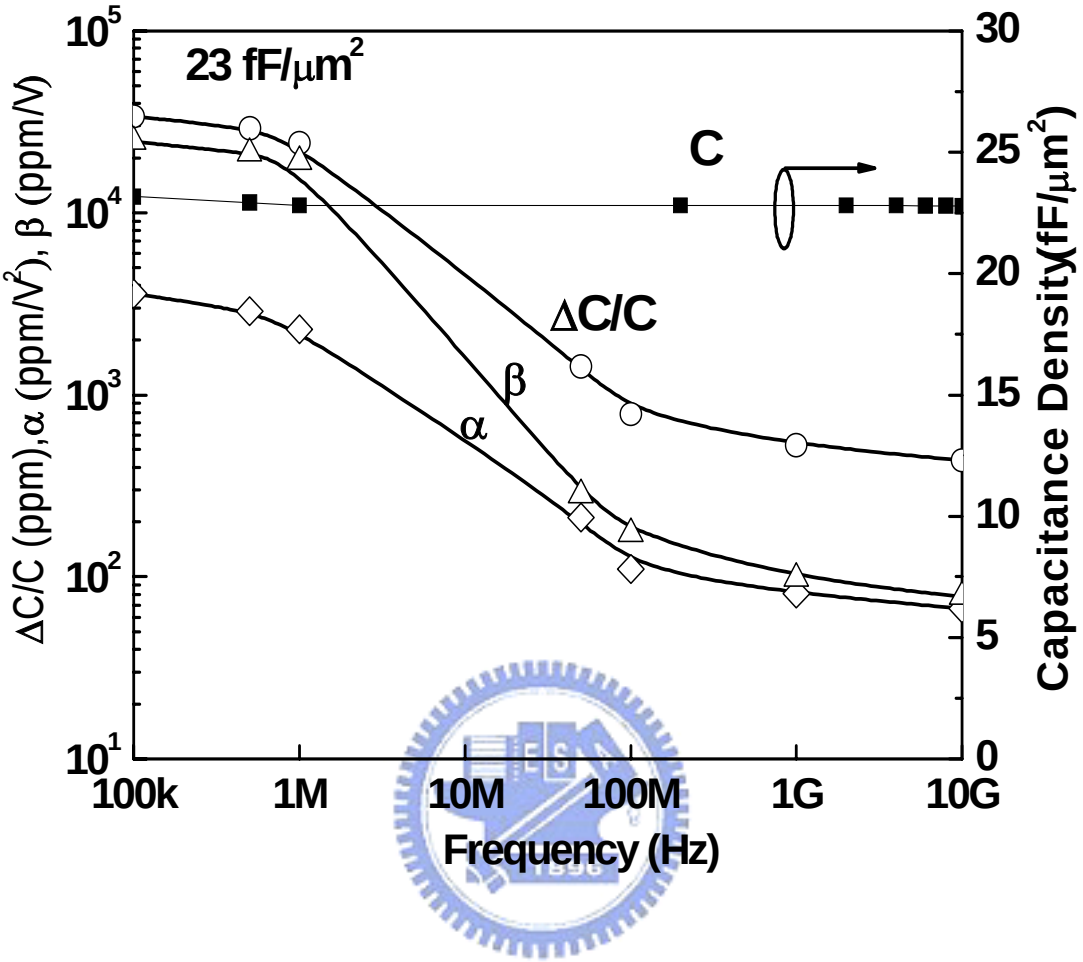


Fig.3-9 Frequency dependent capacitance density, $\Delta C/C_0$, α and β for a TiTaO MIM capacitor.

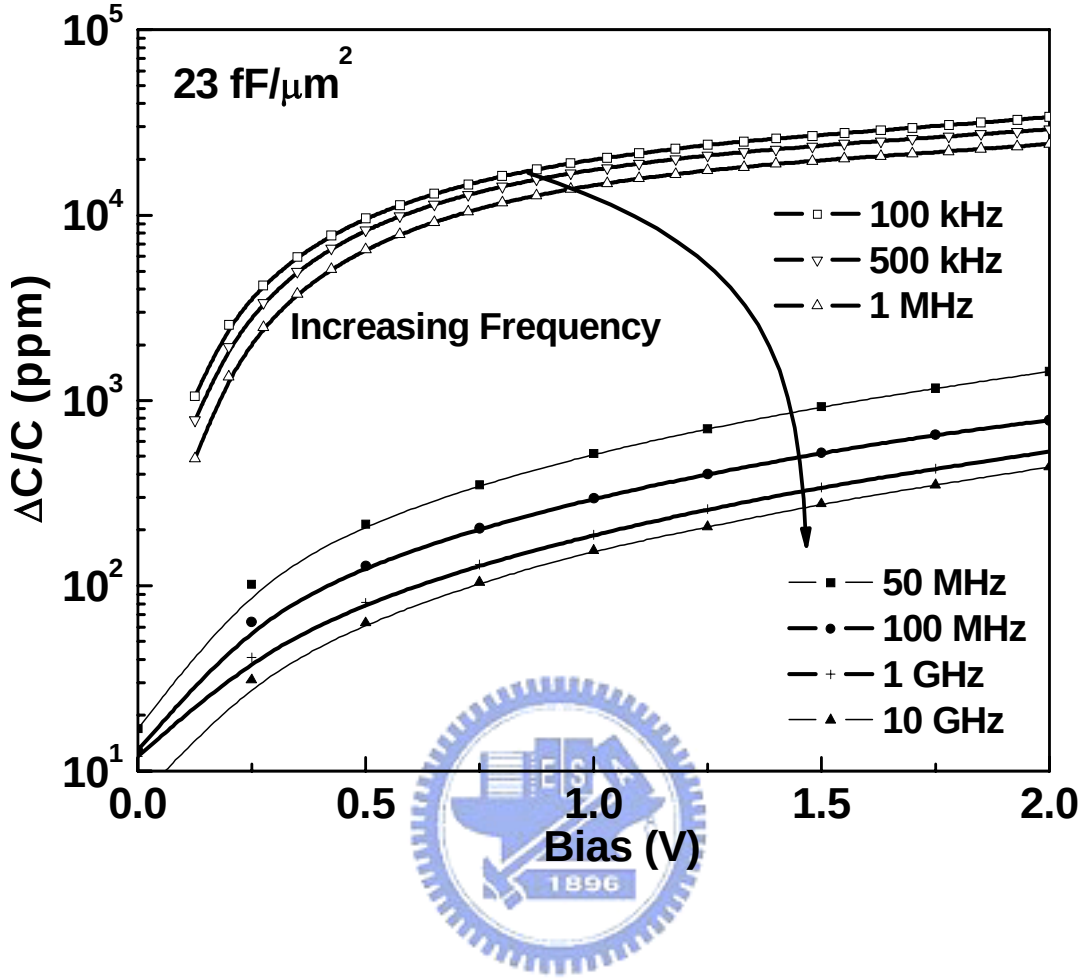


Fig.3-10 The $\Delta C/C_0$-V characteristics of a TiTaO MIM capacitor. The data for frequencies >1 MHz were obtained from the S-parameters.

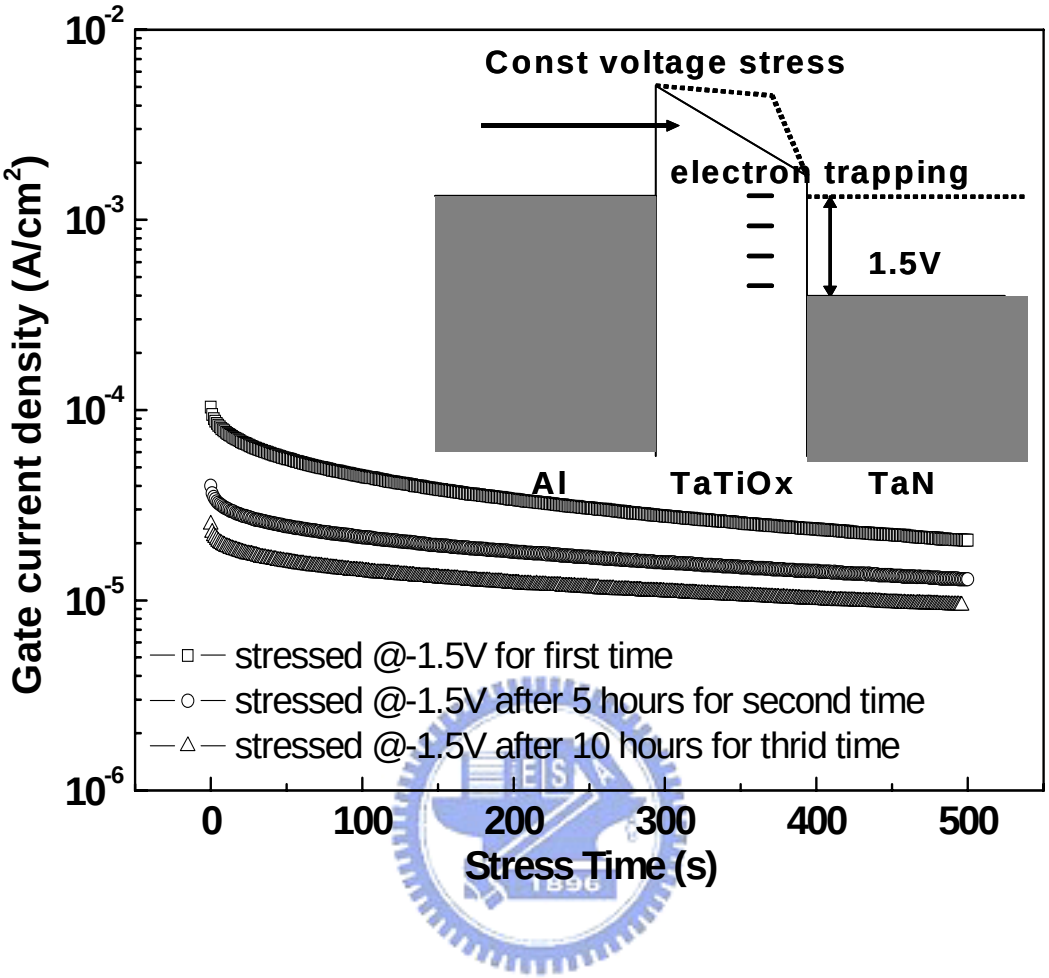


Fig.3-11 The J-V characteristics of Al/TiTaO/TaN capacitors, measured at 1 MHz. The inserted figure is the band diagram of Al/TiTaO/TaN structure.

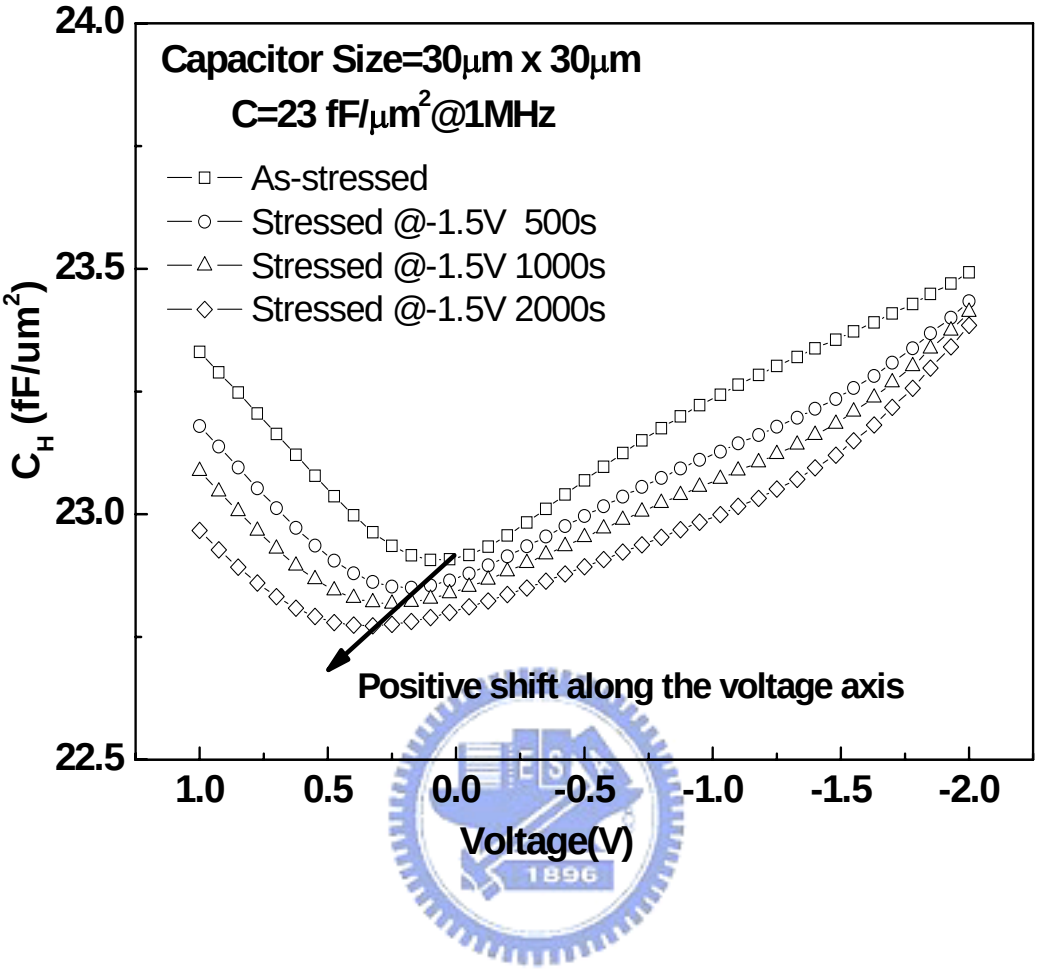


Fig.3-12 The C-V characteristics of a TiTaO MIM capacitor were measured at 1 MHz before and after constant-voltage stress.

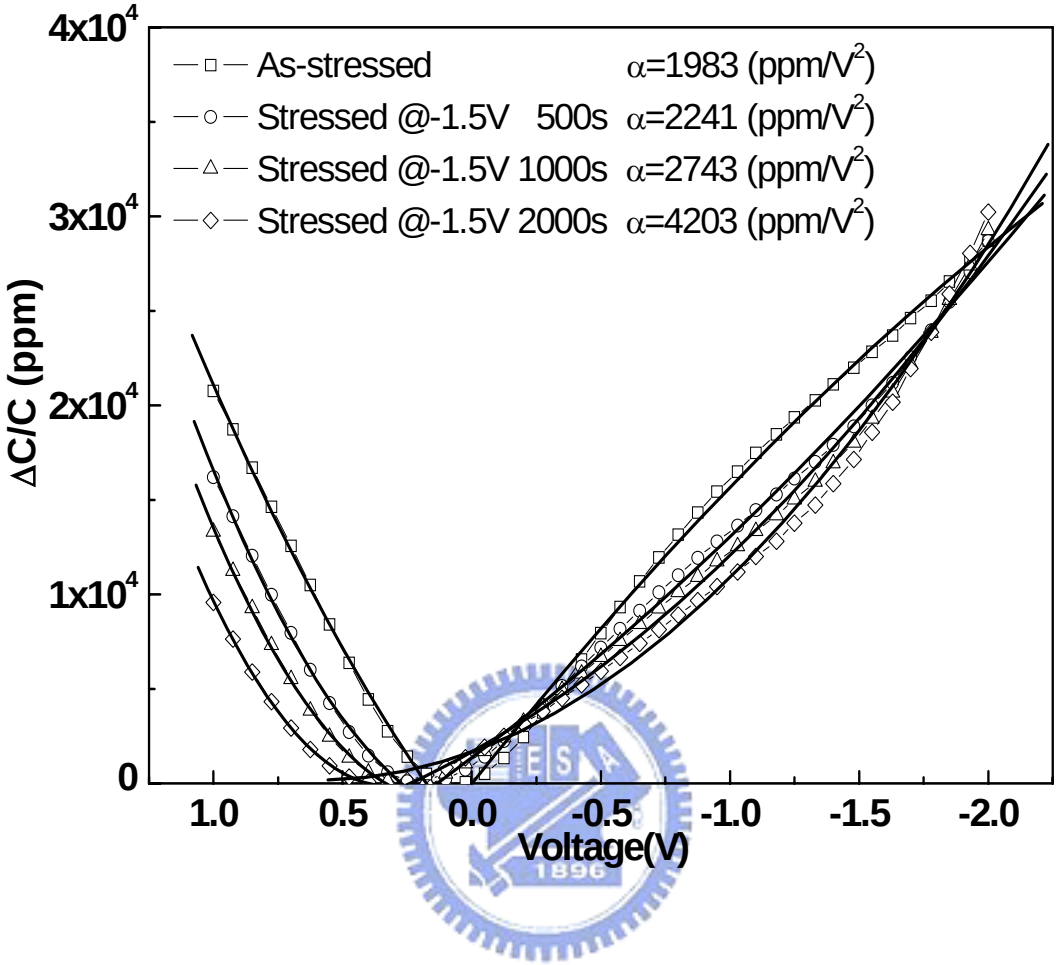


Fig.3-13 The $\Delta C/C_0$-V characteristics of a TiTaO MIM capacitor were obtained from the formula (6).

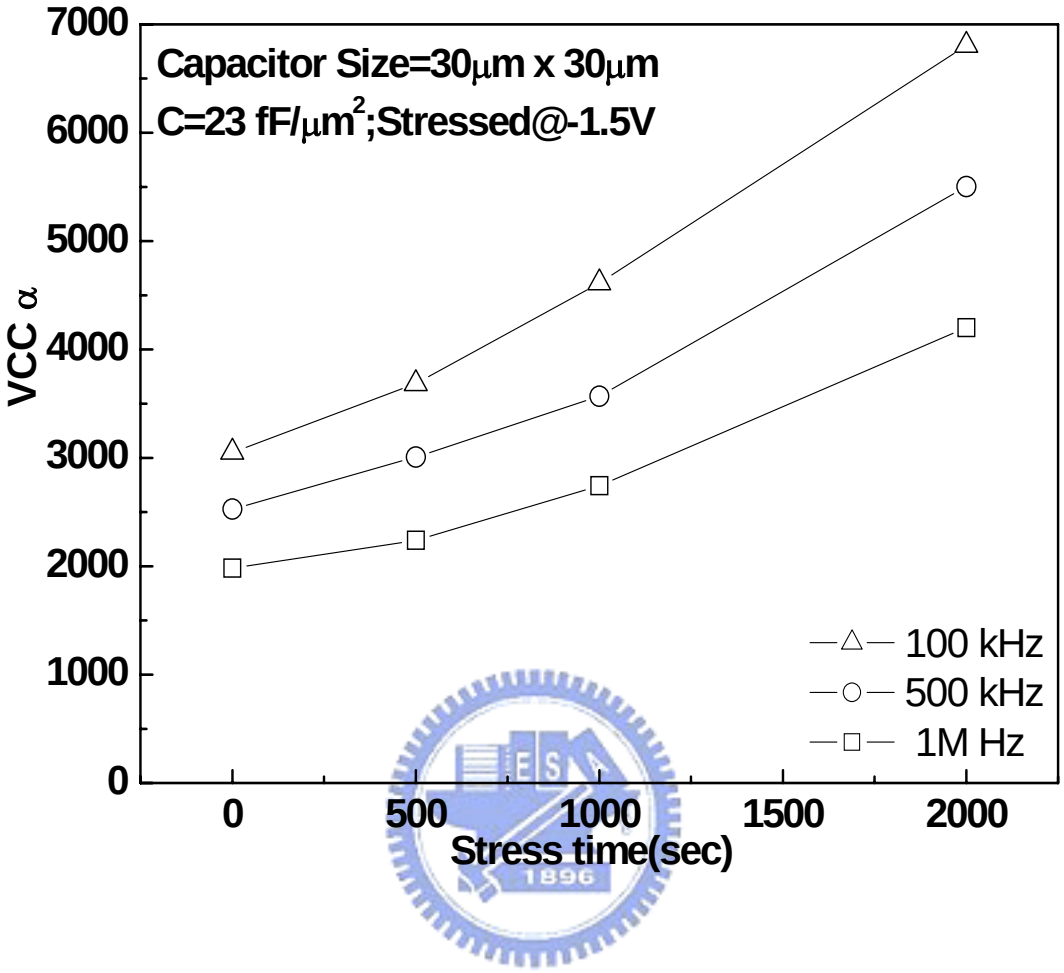


Fig.3-14 The characteristics of VCC-α versus stress time of a TiTaO MIM capacitor at different frequency.

Chapter 4

Conclusion

According to ITRS roadmap (2006), the typical requirements for year 2010 of RF (0.8G ~ 10G) capacitor are capacitance density of 5 fF/μm^2, voltage linearity of less than 100 ppm/V^2 , and leakage current of less than 10^{-8} A/cm^2, respectively. We have achieved high 23 fF/μm^2 capacitance density, < 1.8% capacitance reduction to RF frequency range from 100 kHz to 10 GHz, and $\Delta C/C_0 \leqq 550$ ppm, low α of 81 ppm/V^2 and β of 98 ppm/V at 1 GHz by using high-κ TiTaO MIM capacitors and processed at 400^oC. It can also provide a low leakage current of 1.89×10^{-6} A/cm^2 at -1V. All this indicate that it is very suitable for use in silicon IC applications, although the leakage current of the Al/TiTaO/TaN MIM capacitor structure is higher than 10^{-8} A/cm^2. However, we can solve this problem by replacing top metal electrode which have higher work function than Al, or increase thickness to improve the leakage current at the cost of the degraded capacitance density.

The effects of constant voltage stress on capacitance, leakage current and VCC-α of Al/TaTiO/TaN capacitor were also investigated. We can find out that the decreasing leakage current, decreasing capacitance at low voltage, and increasing VCC-α during the stress time.

Reference

Chapter 1:

[1-1] Wang Bin, J. S. Suehle, E. M. Vogel and J. B. Bernstein, "Time-dependent breakdown of ultra-thin SiO2 gate dielectrics under pulsed biased stress," IEEE Electron Device Lett. 22, pp. 224-226, 2001.

[1-2] J. H. Stathis, A. Vayshenker, P. R. Varekamp, E. Y. Wu, C. Montrose, J. McKenna, D. J. DiMaria, L. -K. Han, E. Cartier, R. A. Wachnik and B. P. Linder, "Breakdown measurements of ultra-thin SiO2 at low voltage," in IEDM Tech. Dig., pp. 94-95, 2000.

[1-3] The International Technology Roadmap for Semiconductors: Semicond. Ind. Assoc., 2006, www.itrs.net.

[1-4] C. P. Yue and S. S. Wong, "A study on substrate effects of silicon-based RF passive components," in IEEE MTT-S Intl. Microwave Symp., pp. 1625-1628, 1999.

[1-5] Jae-Hak Lee, Dae-Hyun Kim, Yong-Soon Park, Myoung-Kyu Sohn and Kwang-Seok Seo, "DC and RF characteristics of a advanced MIM capacitors for MMIC's using ultra-thin remote-PECVD Si_3N_4 dielectric layers," IEEE Microwave and Guided Wave Letters, 9, pp. 345-347, 1999.

[1-6] A. Kar-Roy, Chun Hu, M. Racanelli, C. A. Compton, P. Kempf, G. Jolly, P. N. Sherman, Jie Zheng, Zhe Zhang and Aiguo Yin, "High density metal insulator metal cpapcitors using PECVD nitride for mixed signal and RF circuits," in IEEE International Conference, pp. 245-247, 1999.

[1-7] T. Yoshitomi, Y. Ebuchi, H. Kimijama, T. Ohguro, E. Morifuji, H. S. Momose, K. Kasai, K. Ishimaru, F. Matsuoka, Y. Katsumata, M. Kinugawa and H. Iwai, "High performance MIM capacitor for RF BiCMOS/CMOS LSIs," in Bipolar/BiCMOS Circuits and Technology Meeting, pp. 133-136, 1999.

[1-8] R. B. Van Dover, “Advanced dielectrics for gate oxide, DRAM and RF capacitors,” in IEDM Tech. Dig., pp. 823-826, 1998.

[1-9] G. B. Alers, “Advanced amorphous dielectrics for embedded capacitor,” in IEDM Tech. Dig., pp. 797-800, 1999.

[1-10] H. –J. Cho, C. S. Kang, K. Onishi, S. Gopalan, R. Nieh, R. Choi, E. Dharmarajan and J. C. Lee, “Novel nitrogen profile engineering for improved TaN/HfO_2 Si MOSFET performance,” in IEDM Tech. Dig., pp. 30.2.1-30.2.4, 2001.

[1-11] Y. Abe, T. Oishi, K. Shiozawa, Y. Tokuda and S. Satoh, “Simulation study on comparison between metal gate and polysilicon gate for sub-quarter-micron MOSFETs,” IEEE Electron Device Lett., 20, pp. 632-634, 1999.

[1-12] K. Onishi, Chang Seok Kang, Rino Choi, Hag-Ju Cho, S. Gopalan, R. Nieh, E. Dharmarajan and J. C. Lee, “Reliability characteristics, including NBTI, of polysilicon gate HfO_2 MOSFETs,” in IEDM Tech. Dig., pp. 30.3.1-30.3.4, 2001.

[1-13] L. Manchanda, B. Busch, M. L. Green, M. Morris, R. B. van Dover, R. Kwo and S. Aravamudhan, “High K gate dielectrics for the silicon industry,” in Gate Insulator, pp. 56-60, 2001.

[1-14] G. Wilk, R. M. Wallace and J. M. Anthony, “Hafnium and Zirconium Silicates for advanced gate dielectrics,” J. Applied Physics, 87, pp. 484-492, 2000.

[1-15] J. S. Suehle, E. M. Vogel, M. D. Edelstein, C. A. Richter, N. V. Nguyen, I. Levin, D. L. Kaiser, H. Wu and J. B. Bernstein, “Challenges of high-k gate dielectrics for future MOS devices,” Plasma- and Process-Induced Damage, 2001 6th International Symposium on Page(s): 90 -93, 2001.

[1-16] S. A. Campbell, D. C. Gilmer, Wang Xiao-Chuan, Hsieh Ming-Ta, Hyeon-Seag Kim, W. L. Gladfelter and Jinhua Yan, “MOSFET transistors fabricated with high permittivity TiO_2 dielectrics,” IEEE Electron Device Lett., 22, pp. 104-109, 1997.

[1-17] C. Hobbs, R. Hegde, B. Maiti, H. Tseng, D. Gilmer, P. Tobin, O. Adetutu, F. Huang,

D. Weddington, R. Nagabushnam, D. O'Meara, K. Reid, L. La, L. Grove and M. Rossow, "Sub-quarter micron CMOS process for TiN-gate MOSFETs with TiO2 gate dielectric formed by titanium oxidation," in Symp. on VLSI Technology, pp. 133-134, 1999.

[1-18] Kee-Won Kwon, Chang-Seok Kang, Soon Oh Park, Ho-Kyu Kang and Sung Tae Ahn, "Thermally robust Ta2O5 capacitor for the 256-Mbit DRAM," IEEE Electron Device Lett., 43, pp. 919-923, 1996.

[1-19] Ma Tiezhong, S. A. Campbell, R. Smith, N. Hoilien, He Boyong, W. L. Gladfelter, C. Hobbs, D. Buchanan, C. Taylor, M. Gribelyuk, M. Tiner, M. Coppel and Lee Jung, "Group IVB metal nitrates," IEEE Electron Device Lett., 48, pp. 2348-2356, 2001.

[1-20] S. B. Chen, J. H. Chou, A. Chin, J. C. Hsieh, and J. Liu, "RF MIM capacitors using high-κ Al_2O_3 and $AlTiO_x$ dielectrics," in IEEE MTT-S International Microwave Symp. Dig., vol. 1, pp. 201-204, 2002.

[1-21] T. Shimizu, H. Yamada, A. Kurokawa, K. Ishi and E. Suzuki, "Metalorganic chemical vapor deposited thin film of high-k La-oxides," in International Workshop on Gate Insulator, pp. 196-198, 2001.

[1-22] G. D. Wilk, R. M. Wallace and J. M. Anthony, "High-k gate dielectrics: Current status and materials properties considerations," J. Appl. Phys. 89, pp. 5243-5275, 2001.

[1-23] S.-J. Ding, H. Hu, C. Zhu, S. J. Kim, X. Yu, M.-F. Li, B. J. Cho, D. S. H. Chan, M. B. Yu, S. C. Rustagi, A. Chin, and D.-L. Kwong, "RF, DC, and reliability characteristics of ALD HfO_2-Al_2O_3 laminate MIM capacitors for Si RF IC applications," IEEE Trans. Electron Devices, vol. 51, pp. 886-894, June 2004.

[1-24] K. Takeda, R. Yamada, T. Imai, T. Fujiwara, T. Hashimoto, and T. Ando, "DC-stress-induced degradation of analog characteristics in $Hf_xAl_{(1-x)}O$ MIM capacitors," in IEDM Tech. Dig., pp. 359-362, 2006.

[1-25] J Robertson, **"**Band offsets of wide-band-gap oxides and implications for future

electron devices," J Vac Sci Technol B, vol. 18, pp. 1785-1791, May 2000.

Chapter 2:

[2-1] K. T. Chan, A. Chin, C. M. Kwei, D. T. Shien, and W. J. Lin, "Transmission line noise from standard and proton implanted Si," in IEEE MTT-S Int. Microwave Symp. Dig., pp. 763-766, June 2001.

[2-2] Y. H. Wu, A. Chin, K. H. Shih, C. C. Wu, C. P. Liao, S. C. Pai, and C. C. Chi, "RF loss and crosstalk on extremely high resistivity (10k-1MΩ-cm) Si fabricated by ion implantation, " in IEEE MTT-S Int. Microwave Symp. Dig., pp. 221-224, June 2000.

[2-3] S. B. Chen, C. H. Lai, A. Chin, J. C. Hsieh, and J. Liu, "RFMIM Capacitors Using High-K Al_2O_3 and AlTiOx Dielectrics," IEEE MTT-S Int. Microwave Symp Dig., vol. 1, pp. 201-204, June 2002.

[2-4] Y. H. Wu, A. Chin, C. S. Liang, and C. C. Wu, "The performance limiting factors as RF MOSFETs scale down, " IEEE RF IC Int. Microwave Symp. Dig., pp. 151-155, 2000.

Chapter 3:

[3-1] K. Eufinger, E.N. Janssen, H. Poelman, D. Poelman, R. De Gryse and G.B. Marin, "The effect of argon pressure on the structural and photo-catalytic characteristics of TiO_2 thin films deposited by d.c. magnetron sputtering," Science Direct Thin Solid Films, Volume 515, Issue 2, Pages 425-429, 25 October 2006.

[3-2] C. Zhu, H. Hu, X. Yu, A. Chin, M. F. Li, and D. L. Kwong, "Dependences of VCC (voltage coefficient of capacitance) of high-k HfO_2 MIM capacitors: an unified understanding and prediction," in IEDM Tech. Dig., pp. 379-382, Dec. 2003.

[3-3] S. Bécu, S. Crémer and J. L. Autran, "Capacitance non-linearity study in Al_2O_3 MIM

capacitors using an ionic polarization model," Science Direct Microelectronic Engineering, Volume 83, Issues 11-12, Page 2422-2426, November-December 2006.

[3-4] J. A. Babcock, S. G. Balster, A. Pinto, C. Dirnecker, P. Steinmann, R. Jumpertz, and B. El-Kareh, "Analog characteristics of metal-insulator-metal capacitors using PECVD nitride dielectrics," IEEE Electron Device Lett. 22, pp. 230-232, 2001.

[3-5] S. Blonkowski, M. Regache, and A. Halimaoui, "Investigation and modeling of the electrical properties of metal–oxide–metal structures formed from chemical vapor deposited Ta_2O_5 films," J. Appl. Phys., 90, pp.1501, 2001.

[3-6] S. Becu, S. Cremer, and J.-L. Autran, "Microscopic model for dielectric constant in metal-insulator-metal capacitors with high-permittivity metallic oxides," Appl. Phys. Lett., 88, pp.052902, 2006.

[3-7] H. Hu, C. Zhu, Y. F. Lu, M. F. Li, B. J. Cho, and W. K. Choi, "A higher performance MIM Capacitors Using HfO2 dielectrics," IEEE Electron Device Lett. 23, no. 9, pp. 514-516, 2002.

[3-8] S. B. Chen, C. H. Lai, A. Chin, J. C. Hsieh, and J. Liu, "RF MIM Capacitors Using High-K Al2O3 and AlTiOx Dielectrics," IEEE MTT-S Int. Microwave Symp Dig., vol. 1, pp. 201-204, June 2002.

[3-9] D. M. Pozar, "Microwave Engineering," John Wiley & Sons, pp. 208-209, 1998.

[3-10] C. Zhu, H. Hu, X. Yu, S. J. Kim, A. Chin, M. F. Li, B. J. Cho, and D. L. Kwong, "Voltage and temperature dependence of capacitance of high-k HfO_2 MIM capacitors: a unified understanding and prediction," in IEDM Tech. Dig., pp. 879-882, 2003.

[3-11] P. Gonon and C. Vallee, "Modeling of nonlinearities in the capacitance-voltage characteristics of high-κ metal-insulator-metal capacitors," Applied Physics Letters, Volume 90, Issue 14, id. 142906, 2007.

Vita

姓名：陳冠麟

性別：男

出生年月日：民國 70 年 10 月 22 日

籍貫：台灣省彰化市

住址：彰化縣彰化市台化街 86 巷 14 號

學歷：國立中山大學電機系

（民國 89 年 9 月~民國 94 年 6 月）

國立交通大學電子研究所固態電子組

（民國 94 年九月~民國 96 年 6 月）

論文題目：

高介電常數金屬-絕緣層-金屬電容電性及其可靠度之研究

The Research of Electric Characteristics and Reliability of High-κ MIM Capacitors