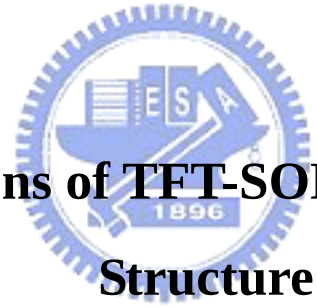
國 立 交 通 大 學

電子工程學系　電子研究所碩士班

碩 士 論 文

具奈米線通道的薄膜電晶體之氮化矽記憶體元件特性分析



Characterizations of TFT-SONOS with Nanowire Structure

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中 華 民 國 九 十 六 年 六 月

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A Thesis

Submitted to Department of Electronics Engineering & Institute of Electronics

College of Electrical Engineering and Computer Science

National Chiao-Tung University

in Partial Fulfillment of the Requirements

for the Degree of

Master of Science

in

Electronic Engineering

June 2007

Hsinchu, Taiwan, Republic of China

中 華 民 國 九 十 六 年 六 月

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摘要

在本篇論文中，我們使用邊襯(sidewall spacer)過度蝕刻的方法製作具有奈米線通道之薄膜電晶體的氮化矽記憶體，另外還進一步結合了雙閘極的概念，並且對基本電特性、寫入/抹除速度、可靠度做詳細的分析討論。

我們利用奈米線結構來提高對通道的控制能力，而且有效的降低臨界電壓(threshold voltage)、漏電流以及次臨界擺幅(subthreshold swing)，其基本電特性較一般標準結構的薄膜電晶體為好。

因為元件通道由多晶矽組成，通道中有很多由晶粒邊界(grain boundary)造成的能障，阻礙電子從源極加速到汲極，所以我們捨棄通道熱電子注入(CHEI)，改用FN穿隧來寫入/抹除資料。由於奈米線高敏感的特性，使元件擁有不錯的寫入/抹除速度。在可靠度方面，我們發現利用雙閘極的結構可以改變電子儲存的位置，因此調整上閘極的偏壓使電子儲存在距離穿隧氧化層較遠的位置，進而增加資料的保存能力。不過在重複寫入/抹除耐久性的表現上，並沒有因為雙閘極的結構而改善。耐久性差的主要原因，是因為使用TEOS當作穿隧氧化層，而TEOS的品質較乾氧化層差，容易產生缺陷；再加上因為通道尖角造成的局部大電場會對穿隧氧化層造成極大的傷害，所以特性並不理想。不過，我們相信

只要能製作出品質較好的穿隧氧化層，並且平緩通道的尖角，耐久性是可以獲得改善的。

Characterizations of TFT-SONOS with Nanowire Structure

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Abstract

In this thesis, TFT-SONOS with nanowire structure was fabricated by sidewall spacer over-etching technique. In addition, the double-gated configuration was also studied. The electrical characteristics, programming and erasing characteristics, and reliability of NW-SONOS were studied and discussed in detail.

The nanowire structure was employed in this thesis to enhance the channel control by taking advantage of its high surface-to-volume ratio. We confirmed that it indeed improves the threshold voltage, leakage current, and subthreshold swing of the resultant devices. In short, the electrical characteristics of NW-TFT are better than those of the conventional TFT.

Since the channel in our device is composed of poly-Si material, there exist many barriers arising from the grain boundaries in the channel. These barriers tend to block the electrons in the source from accelerating toward the drain. To avoid this disadvantage, the CHEI mechanism is replaced with FN tunneling for programming and erasing operations in our device. Due to the high sensitivity of nanowire structure,

the proposed NW-SONOS indeed depicts good programming and erasing characteristics. In order to improve the reliability characteristics, the double-gated structure was employed to shift the location of the trapping charges. Specifically, the electrons can be trapped further away from the tunneling oxide by adjusting the top-gate bias, improving the data retention characteristics. It should be noted, however, that the double-gated structure does not seem to improve the endurance characteristics of the device. The poor endurance is ascribed to the poor quality of TEOS used for the tunneling oxide as well as the horn-shaped channel. The traps are easily generated because of poor quality of TEOS. Besides, high electric field due to the horn of the channel could seriously damage the tunneling oxide. We believe, however, that the endurance could be improved by optimizing the quality of the tunneling oxide, and/or smoothing the shape of the channel in the future.

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Chapter 1

Introduction

1-1 Overview of Nanowire Technology

Accompanying the shrinkage of device dimensions to nano-scale in the fabrication of metal-oxide semiconductor field-effect transistor (MOSFET) is the severe short-channel effects which persistently hinder the technology development. Owing to their inherent high surface-to-volume ratio, nanowires (NWs) hold great potential for solving this issue. In addition, a high surface sensitivity makes NWs extremely suitable for applications to sensing devices. For these reasons, many possible applications of NWs have already been exploited, including nano CMOS [1], memory devices [2], NW TFTs [3], and biosensors [4].

The preparation of NWs can be categorized into two approaches: “top-down” and “bottom-up.” The top-down approach usually involves advanced techniques to generate NWs, such as lithography and etching. Though such techniques are already well developed and widely used in VLSI industry, related equipments are costly and their accuracy is limited. Therefore, research efforts have been put into a range of specific methods, such as chemical shrinking [5], thermal evaporation [6], and spacer patterning [7], to help generate NWs while replying only on the use of conventional lithography and etching tools.

The bottom-up approach differs from the top-down approach in the sense that it

usually employs deposition techniques for preparing the NWs and synthesizing them on a substrate. To complete the NW device structure, the NWs are harvested from the original substrate and aligned on another insulating substrate, after which the electrical contacts are attached. Due to the complexity of the synthesis and alignment processes, a considerable amount of research works have been conducted in this area. Methods for synthesizing NWs include laser ablation catalyst growth [8], chemical deposition catalyst growth [9], and oxide-assisted catalyst-free [10]. Methods used to assemble and align NWs include electric-field-directed assembly [11], microfluidic channels [12], and the Langmuir-Blodgett (LB) technique [13].

Although the bottom-up approach is significantly cheaper than the top-down approach, its fabrication is relatively complex and time-consuming, and high-density integration is difficult to achieve.

1-2 Overview of SONOS

In 1967, D. Kahng and S.M. Sze invented the floating-gate nonvolatile memory [14], leading to a flurry of research in the related technology. One of the most important subsequent inventions is that of flash memory, which possesses a byte-selectable write operation combined with a sector “flash” erase. This leads to significant improvements in the speed and practicality of the floating-gate memory, which has subsequently been applied to a variety of portable electronic systems, such as cellular phones, digital cameras, PDAs, MP3s, and memory sticks. As transistors become smaller, the thickness of tunneling oxide used also approaches certain limits. Since the charge trapping layer of the floating-gate memory is made from poly-silicon, a single defect in the tunneling oxide will cause all stored charges to be lost, thus

degrading the retention characteristics of the memory. It is therefore essential that the tunneling oxide used is at least 8nm thick [15]. Consequently, not only is it not possible to further reduce the size of transistors, it is also difficult to speed up writing and erasing functions.

Si-oxide-nitride-oxide-Si (SONOS) devices [16-18] are currently one of the most promising solutions for overcoming difficulties presenting for flash technology. Such devices replace the poly-silicon storage layer in conventional flash devices with a nitride. Since nitride is an insulator, a single defect in it will not cause all stored charges to be lost. This property can therefore be used to improve retention and reduce writing and erasing times.

A significant amount of research has been conducted for developing advanced SONOS. These can be broadly categorized into the following three major areas:

1. Replacing one of the dielectric layers with a high-k dielectric:
    A. Replace the block oxide with high-k dielectric. The thicker high-k layer tends to prevent the flow of stored charges into the control gate. For this purpose, a higher barrier height for electrons relative to other high-k alternative is preferred, such as Al_2O_3 [19].
    B. Replace the nitride with a high-k material, such as HfAlO [19]. The improvement in the programming speed and the over-erase characteristics of HfAlO is attributed to suitable valence and conduction band offsets with respect to silicon.
    C. Replace the tunneling oxide with a high-k material [20-24]: For example, replacing the oxide with a multilayer, like oxide-nitride-oxide (O-N-O) or O-Nanocrystal-O. The multilayer suppresses direct tunneling in a low electric

field during retention, while allowing an efficient hole tunneling erase in a high electric field due to the suitable band offset. It is therefore able to offer fast hole tunneling erase, while relieving the retention issue suffered by conventional SONOS.

2. Multiple-gate structure [25-28]: The advantage of the double gate transistor, which was first demonstrated in the1980s, lies in its better controllability. As the transistor is surrounded by gate electrodes on multiple channel sides, it tends to reduce the bulk leakage. This leads to an improvement in the subthreshold swing and reduces the short channel effects. Additionally, by adjusting the voltage on separate gates to a suitable level, writing and erasing times are also reduced. Applying the multiple-gate structure to SONOS may not only improve its basic electrical characteristics, but also increase writing and erasing speeds.
3. Thin-film transistor (TFT) SONOS [29-31]: Poly-Si TFTs are widely used in active-matrix liquid-crystal displays (AMLCDs) [32]. Currently, the possibility of integrating a whole system on top of the panel (SOP) is also being actively pursued [33]. Such integration can feasibly be achieved by employing TFT-SONOS. TFT-SONOS arrays could also be built by using the stacking method, allowing for an increase in the device density without decreasing the device dimensions.

1-3 Motivation

Although TFT-SONOS is appealing, there still exist a number of challenges lying ahead that must be overcome. For example, the subthreshold swing and leakage current of TFTs are inferior to that of MOS, limiting both the operation speed and

power dissipation. These concerns could be addressed with the use of nanowire channels in the device structure which tend to reduce the subthreshold swing with a better gate controllability and reduce the leakage by minimizing the cross-sectional area of leakage paths. In addition, since the double gate structure is able to enhance writing and erasing functions, we are also anxious to equip TFT-SONOS with the double-gate configuration and exploit its potential in practical applications.

1-4 Thesis Organization

In this thesis, we employ a structure previously developed by the Advanced Device Technology Laboratory, National Chiao Tong University, to fabricate and characterize a novel NW-SONOS. The thesis will be divided into five chapters. In Chapter 2, we will briefly describe the device structure and process flow and introduce the programming and erasing mechanism about SONOS. Then, the basic electrical characteristics, writing and erasing characteristics, and reliability of NW-SONOS will be presented and discussed in Chapter 3 and Chapter 4. Finally, Chapter 5 will summarize our major findings and achievements. Directions for future work are also suggested in this chapter.

Chapter 2
Device Fabrication and Operation Principles

2-1 Device Structure and Process Flow

Devices used in this study were fabricated on 6-inch silicon wafers. First, silicon wafers were capped with a 1000Å silicon dioxide layer serving as the starting substrate. Then, a 1000Å n^+-doped poly-Si layers was deposited on the starting substrate to serve as the gate electrode (side-gate electrode). The poly-Si layer was subsequently etched to form the gate stack. Afterwards, a total 210Å ONO multilayer gate dielectric, consisting of a 100Å-thick layer of tetra-ethyl-ortho-silicon (TEOS) blocking oxide at 700℃, a 55Å-thick layer of silicon nitride trapping layer at 780℃, and a 55Å-thick layer of TEOS tunneling oxide, all deposited by an Low Pressure Chemical Vapor Deposition (LPCVD) system. A 1000Å-thick amorphous-Si layer was then also deposited by LPCVD. Next, an annealing step was performed at 600℃ in N_2 ambient for 24 hours to transform the amorphous-Si into poly-Si. Subsequently, source/drain (S/D) implant was performed by P^+ implantation at an energy of 15keV and a dose of $1x10^{-15}$ cm^{-2}. Note that the implant energy was kept low so that most of the implanted dopants were located near the top surface of the poly-Si layer. S/D photoresist patterns were then formed on the substrate by a standard lithography step. A reactive plasma etch step was subsequently employed to remove the poly-Si layer except at the S/D regions, and the sidewall poly-Si nanowire channels were simultaneously formed in a self-aligned manner. After this step and subsequent

activation treatment, the S/D regions were formed with a heavy-dose implant. Note that, due to the low implantation energy, the nanowire channels remain undoped. Afterwards, the devices were divided into two splits, with one split fabricated is the double-gated configuration. In this split, 180Å-thick or 360Å-thick TEOS used as top gate oxide was deposited by LPCVD at 700℃. Subsequently, 1000Å n^+-doped poly-Si layers was deposited to serve as the gate electrode (top-gate). The other split with single-gated configuration skipped those steps until passivation deposition. All wafers then received the deposition of a 2000Å-thick passivation TEOS oxide layer by LPCVD at 700℃. Finally, the fabrication was completed after the formation of test pads using standard metallization steps. Top views of the single- and double-gated NW-SONOS are shown in Fig. 2-1(a) and Fig. 2-1(b), respectively. Fig. 2-2(a) and Fig. 2-2(b) respectively display the cross-sectional views along A-B in Fig. 2-1(a) and Fig. 2-1(b). The three-dimensional (3D) structures of the single- and double-gated NW-SONOS are illustrated in Fig. 2-3(a) and Fig. 2-3(b), respectively. The cross-sectional Transmission electron microscopy (TEM) picture of a double-gated NW-SONOS with 180Å-thick top gate oxide is shown in Fig. 2-4(a). The views shown in Fig. 2-4 indicate that the thickness and width of nanowire channel are around 65 nm and 45 nm, respectively.

2-2 The Program/Erase Mechanisms

In general, the program/erase mechanisms employed in SONOS include channel hot electron injection (CHEI), Fowler-Nordheim tunneling (FN tunneling) and band to band tunneling (BTBT). The three mechanisms will be illustrated and described in the following sub-sections.

2-2-1 Channel Hot Electron Injection

The channel hot electron injection can be well understood by “lucky-electron model” [34]. The injection of channel hot electrons into the gate oxide region occurs at large drain-to-source voltage, as illustrated schematically in Fig. 2-5. Electrons flowing from source to drain gain energy from the high-field region near the drain junction.

The electrons are emitted into the gate dielectric by first gaining enough energy without suffering an energy stripping collision in the channel and then being redirected by acoustic phonon scattering toward the Si/oxide interface. On the other hand, the effective mass of hole is heavier than the electron. In addition, barrier height of valence band is also higher than conduction band. It is thus much more difficult for holes to obtain enough energy to surmount the oxide barrier. Therefore, hot-hole injection is rarely employed in nonvolatile memory operation.

Another merit of CHEI mechanism is to achieve NROM [35], SONOS with 2Bit/Cell. Employing CHEI, the charge can be programmed into drain or source terminals, then the data can be sensed by “reverse read”.

2-2-2 Fowler-Nordheim Tunneling

The tunneling mechanism is a kind of quantum-mechanical process during which the carriers may tunnel through the forbidden region of the insulator into the allowed states of the insulator or the opposite electrode material. Due to different electric field strength across the insulator, the tunneling mechanism can be classified into direct

tunneling and FN tunneling. If the electric field strength across the tunneling oxide (E_{ox}) is smaller than $\frac{q\phi_1}{t_{ox}}$, where $q\phi_1$ is the barrier height between Si channel and tunneling oxide, the carriers may tunnel into nitride trapping layer by direct tunneling. The current density is expressed as:

$$J = AE^2_{ox}\left(\frac{\phi_1}{V_{ox}}\right)\left(\frac{2\phi_1}{V_{ox}}-1\right)e^{\frac{-B\left[1-\left(1-\frac{V_{ox}}{\phi_1}\right)^{3/2}\right]}{E_{ox}}} \quad \text{(eq. 2-1)}$$

where $A=\frac{q^3E^2}{8\pi h\phi_1}$, $B=\frac{8\pi\sqrt{2m_{ox}}\phi_b^{3/2}}{3hq}$, and the electron effective mass, m_{ox}, is $0.5\,m_o$.Direct tunneling is illustrated in Fig. 2-6 (b).

If $E_{ox}>\frac{q\phi_1}{t_{ox}}$, the carriers may tunnel into nitride trapping layer by FN tunneling. The current density is expressed as:

$$J = AE^2_{ox}e^{-\frac{B}{E_{ox}}} \quad \text{(eq. 2-2)}$$

FN tunneling is illustrated in Fig. 2-6 (c). [36]

2-2-3 Band to Band Tunneling

The phenomenon of band to band tunneling occurs in the n^+ drain region overlapping the gate. For this event to happen, the strength of electric field in the region must be sufficiently high to cause deep-depletion situation. Typically a negative gate voltage is applied, and the voltage difference between the gate and drain must be large. During the operation, electrons tunnel directly or are assisted by traps in the gap from valence band to conduction band at the drain. At the same time, holes are generated in the deep-depletion region, and are then accelerated by the strong field and may be attracted by the negative gate bias into the nitride trapping layer. The

processes are illustrated in Fig. 2-7.

Chapter 3
Basic Electrical Characteristics and Program/Erase Characteristics

3-1 Basic Electrical Characteristics

3-1-1 Determination of The Threshold Voltage

For MOSFET, the threshold voltage (V_{th}) is usually determined from the extrapolated gate voltage V_{Gi} by $V_T = V_{Gi} - V_D/2$, where V_{Gi} is determined by Gm_{max}. However, this method is not suitable for TFTs. For TFTs, defects in grain boundary of the channel will trap the electrons, resulting in a rough Gm-V_G curve under large V_G region. In this thesis, the method we adopted to determine V_{th} is the constant drain current method in TFTs, i.e.,

$$V_{th} = V_G \mid_{I_D = 1nA, V_D = 1V} \quad \text{(eq. 3-1)}$$

3-1-2 Comparisons of Transfer Characteristics

Fig. 3-1 shows transfer characteristics of conventional TFT and NW-SONOS. The subthreshold swing (SS) of NW-SONOS is significantly improved over that of the conventional TFT which can be ascribed to the high surface-to-volume ratio. In addition, the leakage current of NW-SONOS is much lower than that of the conventional TFT. The better SS and less leakage current will result in a larger programming window for the NW-SONOS. The merit demonstrates that NW-TFT is

more suitable than conventional TFT.

The fresh state, programming state, and erasing state of SG-NW-SONOS and DG-NW-SONOS are shown in Fig. 3-2 and Fig. 3-3. Fig. 3-2 (a) and Fig. 3-3 (a) show I_D-V_G curve in logarithmic scale, while Fig. 3-2 (b) and Fig. 3-3 (b) show I_D-V_G curve in liner scale. From Fig. 3-2 and Fig. 3-3, it can be seen that V_{th} of erasing state and fresh state is not equal. One plausible reason is that there are many deep-level traps existing in the channel and interface between the channel and dielectric layer. As device is programmed by applying a large bias, a considerable amount of electrons is gathered in the channel, and some electrons will be trapped in deep-level traps. Fig. 3-4 is in accord with the argument about deep-level traps. Because a fraction of electrons will be used to fill the traps at the first programming stage, the V_{th} shift of the first programming stage is smaller than that after the second programming stage. In addition, the leakage current of erased state is smaller than that of fresh state in double-gated SONOS. Fig. 3-5 may explain this phenomenon. Figs. 3-5 (a) and (b) compare the leakage current of side-gate read mode relative to that of top-gate mode, It can be seen that the leakage current of the top-gate read mode is improved over the side-gate read mode. This demonstrates that the deep-level traps exist near not only the side-gate but also the top-gate, so electrons during the first programming stage are also trapped in deep-level traps near the top-gate.

3-2 Program/Erase Characteristics

In the study, the devices are programmed and erased by Fowler-Nordheim (FN) tunneling mechanism. In this structure, the conventional channel hot electron injetion (CHEI) method is not suitable because of the existence of the barrier height from

grain boundaries in the channel. The barrier height will hinder the acceleration of the electrons from the source to drain, hence the electrons will not be hot enough to inject into the trapping layer. For programming, both source and drain are grounded, and the gate is biased at a highly positive voltage to induce a strong electric field. And for erasing, source and drain are still grounded, and the gate is biased at a highly negative voltage to detrap electrons in the nitride. The bias of each electrode in figures is expressed as (side-gate, top-gate, drain, source) for both single-gated and double-gated SONOS (in single-gated SONOS, the bias of top-gate is always "0"). For example, (15, 15, 0, 0) means that the biases of side-gate (V_{SG}) and top-gate (V_{TG}) are 15V, and the biases of drain (V_D) and source (V_S) are 0V. The program and erase condition for single-gated SONOS and double-gated SONOS are listed at Table 3-1 and Table 3-2, respectively.

V_{th} shift versus programming time for side-gate bias of 13V, 14V, and 15V is shown in Fig. 3-6. Fig. 3-6 (a) and Fig. 3-6 (b) show that the FN programming speeds of the single- and double-gated SONOS, respectively. It can be seen that memory window of around 2V can be achieved within 0.5 msec of programming time. The programming speed is shown to increase when applying a higher side-gate voltage. Fig. 3-7 shows the erasing characteristics of the single-gated SONOS and double-gated SONOS for side-gate bias of -10V, -12V, and -14V. The erasing speed is also found to increase with side-gate voltage. However, erase saturation may occur because gate injection is stronger at higher side-gate voltage. As decreasing the trapped charges in the nitride layer, the electric field across the tunneling oxide will also be reduced, and the electric field across the blocking oxide will be enhanced. Therefore, the electrons may be injected from the gate into the nitride, and the speed is larger than the erasing speed. In other words, when the erasing time is longer, the V_{th} may increase.

Fig. 3-8 and Fig. 3-9 show the programming speed and erasing speed versus channel length for single-gated SONOS and double-gated SONOS, respectively. The bias for programming is (15, 0, 0, 0) for each structure. Both the programming speed and the erasing speed change less with decreasing channel length. Furthermore, the short channel effect is improved due to high surface-to-volume ratio of nanowire.

Next, the influence of the V_{TG} on the programming and erasing speed is discussed in the following section. Programming speed and erasing speed for different V_{TG} are shown in Figs. 3-10 (a) and (b), respectively.

In programming, the programming speed is enhanced by the top-gate bias, with the maximum enhancement occurs at a top-gate bias of 3V. The V_{th} shift versus V_{TG} is shown in Fig. 3-11, where the programming time is 0.5msec and V_{SG} is 15V. During programming operation, there are a lot of electrons in the channel due to the side-gate bias, and both V_S and V_D are 0V, therefore, the voltage of the channel should be 0V. If the top-gate is applied with positive voltage in programming situation, more electrons will be generated in the channel and the programming speed will be enhanced. However, with increasing V_{TG}, the amount of electrons in the channel will reach saturation, and the enhancement in the programming speed will stop. In addition, the electric field from large V_{TG} may interfere with the electric field from V_{SG}, thus decreases the programming speed.

In erasing, the erasing speed is reduced by V_{TG}. V_{th} shift versus V_{TG} is shown in Fig. 3-12. Since there may be no electrons due to the highly negative V_{SG}, the channel should be floating. And the influence of excess holes from V_{TG} will be much less than that due to the electric field from V_{TG}.

Figs. 3-13 (a) and (b) show the effect of top-gate bias on V_{th} shift, i.e., V_{SG} and V_S is 0V, V_D is 1V, under programming and erasing operations, respectively. Only slight V_{th} shift is observed in the figure, suggesting that there are no significant

charges trapping occurring in the top-gate oxide.

Figs. 3-14 (a) and (b) compare the programming speed and erasing speed of single-gated SONOS with those of double-gated SONOS, respectively. In our structure, the programming speed and erasing speed are not improved. Because the most important parameters that determine the programming speed and erasing speed are the thickness of tunneling oxide and the programming efficiency. But with the same thickness of tunneling oxide, the programming efficiency can not be enhanced obviously by double-gated structure with FN tunneling.

Chapter 4
Reliability Characteristics of TFT-SONOS

In addition to program/erase speed, nonvolatile memory cells have some important functional characteristics, which are used to evaluate the suitability and practicality of the cells under test. These characteristics are divided into two main classes, namely retention and endurance. They are discussed in the following sections.

4-1 Retention

Retention is a measure of the time that a nonvolatile memory cell can retain the charge in the trapping layer. Fig. 4-1 shows the band diagram for illustrating the charge loss paths in SONOS cells. There are two major leakage current components in relating to charge loss, one is the thermionic emission following Frenkel-Poole mechanism, another one is tunneling through either blocking oxide or tunneling oxide. The Frenkel-Poole emission is due to field-enhanced thermal excitation of trapped electrons into the conduction band of silicon. The trapped charge can be expressed as:

$$n_t(\phi_t,t) = n_t(\phi_t,0) \bullet e^{-t/\tau} \qquad \text{(eq. 4-1)}$$

where $n_t(\phi_t,0)$ is the initial trapped charges, and τ is the time constant. The time constant of Frenkel-Poole emission can be expressed as:

$$\tau_{FP} = \tau_0 \exp\{[\phi_N - q(qE/\pi\varepsilon)^{1/2}]/kT\} \qquad \text{(eq. 4-2)}$$

where ϕ_N is the corresponding nitride trap energy, E is the electric field and ε is the high-frequency permittivity.

The tunneling mechanisms include trap-to-band (T-B) tunneling, trap-to-trap

(T-T) tunneling, and band-to-trap (B-T) tunneling. The trapped electrons in nitride can tunnel back to the conduction band of the silicon substrate (trap-to-band tunneling), or to the interface traps between tunneling oxide and channel (trap-to-trap tunneling). In addition, holes from the silicon valence band may tunnel into the nitride traps under the influence of the internal electric field (band-to-trap tunneling). The time constant of tunneling mechanism can be expressed as:

$$\tau_T = \tau_0 \cdot \exp(\alpha_{ox} \cdot t_{ox}) \cdot \exp(\alpha_N \cdot t_N) \qquad \text{(eq. 4-3)}$$

where t_{ox} is the thickness of tunneling oxide, t_N is the distance from trap in nitride to tunneling oxide. And τ_0, α_{ox}, and α_N are different in trap-to-band tunneling, trap-to-trap tunneling, and band-to-trap tunneling.[37]

Fig. 4-2 shows the data retention of single-gated NW-SONOS, and it is far worse than the required ten years retention. In general case, i.e., with single-crystal silicon for th channel and dry oxide for tunneling oxide, trap-to-trap tunneling is normally neglected for a fresh SONOS cell measurement. However, in our case with TFT-SONOS, since there are many interface traps existing between tunneling oxide fabricated by TEOS and poly-Si channel, trap-to-trap tunneling must be considered. Hence the worse retention capability for TFT-SONOS over conventional SONOS is expected. Nevertheless, as shown in Fig. 4-3, the data retention at programming state is improved by double-gated structure. Data retention with a continued electric field on the trapping layer is also tested. At the programming state, the side-gate is biased at -2V and the source and drain are grounded to accelerate the trapped charges loss. On the other hand, at the erasing state, the side-gate is biased at +2V and the source and drain are grounded to accelerate the charges tunneling into nitride. The result is shown in Fig. 4-4. The retention capability at programming state of double-gated structure is better than that of single-gated structure, and the erasing state of single gated structure is more easily influenced by electric field than that of double gated

one.

Possible cause of the phenomenon is the location of trapped charges. In equation 4-3, τ_T is seriously influenced by t_N. If the distance from the location of trapped charges to tunneling oxide is larger, nitride will retain the trapped charges longer. In addition, since the nitride layer covers the whole side-gate and no oxide layer stops the charges from diffusing toward the vertical dimension in our structure, the distance from the location of trapped charges to channel edge is important for retention. Based on the assumption, the cause of improved retention ability is due to the top-gate, which can change the direction of electric field toward trapping layer, and cause charges to be trapped deep.

If top-gate can change the direction of electric field toward trapping layer, different V_{TG} will cause charges to be trapped on different locations. Therefore, the retention will also be different. Retention under different V_{TG}, i.e., V_{TG} of 15V, 0V, and floating, is compared in Fig. 4-5, and the result supports the assumption.

In addition, the V_{th} of single-gated structure ($V_{th,\,SG}$) is the smallest, while the V_{th} of double-gated structure ($V_{th,\,DG}$) with 180Å-thick top gate oxide is the largest, as shown in Fig. 4-4. The explanation of this situation is referred from [38]. Fig. 4-6 is extracted from [37], and State C in Fig. 4-6 (c) shows that when V_{g2} is less than V_{thDG}, $V_{th(G1)}$ will be larger than V_{thDG}. Therefore, since V_{TG} is grounded in read state, i.e., V_{TG} is smaller than V_{thDG}, $V_{th,\,SG}$ is smaller than $V_{th,\,DG}$. Besides, when T_{ox2} is thinner, $\frac{AB}{DE}$ will be larger with the same ΔV_{g2}. Hence, $V_{th,\,DG}$ with 180Å-thick top gate oxide is larger than that with 360Å-thick top gate oxide. In physics, V_{TG} is lower than $V_{th,\,DG}$, and the higher V_{SG} is needed to generate sufficient electrons in the channel near the side-gate to turn on the device, so $V_{th,\,SG}$ will be higher. In addition, the thicker top-gate oxide will cause the channel control near the top-gate to be lower, so ΔV_{th}

will be smaller.

4-2 Endurance

Endurance is the ability of a nonvolatile memory to endure the damage of numerous cycles of programming and erasing, i.e., the number of erase/write cycles that the memory will retain the required memory window and continue to operate as specified in the data sheet. Since the carriers for programming and erasing have energy, they will cause the degradation of tunneling oxide and trapping layer in every operation. In addition, high electric field stress across tunneling oxide will increase the current density at low electric field. The excess current at low electric field is called stress-induced leakage current (SILC) [39]. SILC is attributed to stress-induced oxide defects, which lead to a trap assisted tunneling. The main parameters controlling SILC are the stress field, the amount of charge injected during the stress, and the oxide thickness.

In general, flash products are specified for 10^6 erase/program cycles. However, the endurance requirement can be loosened with the increase of memory density for the other applications. Fig. 4-7 shows the endurance requirement of NAND Flash memories [40]. We can see that the endurance requirement is 100k cycles for NAND Flash with 256 MB density. Since for a memory array with higher density, a certain cell in a block has less possibility of being written and erased. This is because the memory operation of an individual cell in the array is repeated only after the entire memory blocks are addressed. This is why the endurance requirement of digital still camera (DSC), the biggest NAND Flash application, has decreased from 10.3K cycles for 128MB to 2.6K cycles for 1GB. The endurance requirement is sufficient for the

user to take 700 photos with 1MB size every day for 10 years.

Figs. 4-8 (a) and (b) show the I_D-V_G curve of single-gated and double-gated structures with increasing erase/program cycles. It can be seen that the subthreshold swing and memory window of both structures worsen with increasing erase/program cycles. The subthreshold swing worsening is due to the degradation of tunneling oxide, and the memory window closure is due to the degradation of nitride. Figs. 4-9 (a) and (b) show the memory window versus erase/program cycles of single-gated structure and double-gated structure, respectively. The poor endurance is due to the poor quality of TEOS for tunneling oxide and the horn of the channel. The traps are easily generated because of poor quality of TEOS. Besides, high electric field due to the horn of the channel will seriously damage the tunneling oxide.

Chapter 5
Conclusion and Future Work

5-1 Conclusion

In this thesis, we have successfully fabricated and characterized TFT-SONOS with nanowire structure. The nanowire channels were formed by sidewall spacer etching technique. The proposed fabrication method is simple, fast, and low cost. Moreover, we have also fabricated TFT-SONOSs with double-gated configuration and comparisons were made with their single-gated counterparts.

Regarding the programming speed and erasing speed, the characteristics of TFT-SONOS with nanowire structure are comparable to those of conventional SONOS. The double-gated configuration in the proposed device does not seem to contribute nor enhance the programming speed or erasing speed. On the other hand, the reliability of TFT-SONOS is still worse than that of the conventional SONOS, due to poor quality of tunneling oxide and the horn-shaped structure of the nanowire channels. However, the double-gated configuration is found to improve the retention of TFT-SONOS with nanowire structure. Although there are many disadvantages lying ahead and need to be improved, we demonstrate the feasibility of nonvolatile memory with nanowire-TFTs fabricated by the simple and production-worthy sidewall spacer technique.

5-2 Future Work

To improve the reliability of the proposed device is the most urgent work in the

future. Since the poor reliability is due to the mediocre quality of tunneling oxide and the horn-shaped structure of the nanowire channels, some effective methods to alleviate these issues can be used for reliability improvement. One is to deposit high quality TEOS or replace the TEOS with another dielectric material with better quality. Another approach is to improve the nanowire structure by eliminating the horn or at least suppress its negative impact on the devices. In addition, further improvement in device characteristics is possible by introducing some advanced process techniques to improve the film crystallinity, such as laser annealing, metal induced lateral crystallization, and plasma treatment. We believe that dramatic progress in making such NW-SONOS device toward practical application will be made in the future with additional efforts to improve and optimize the device structure and process steps.

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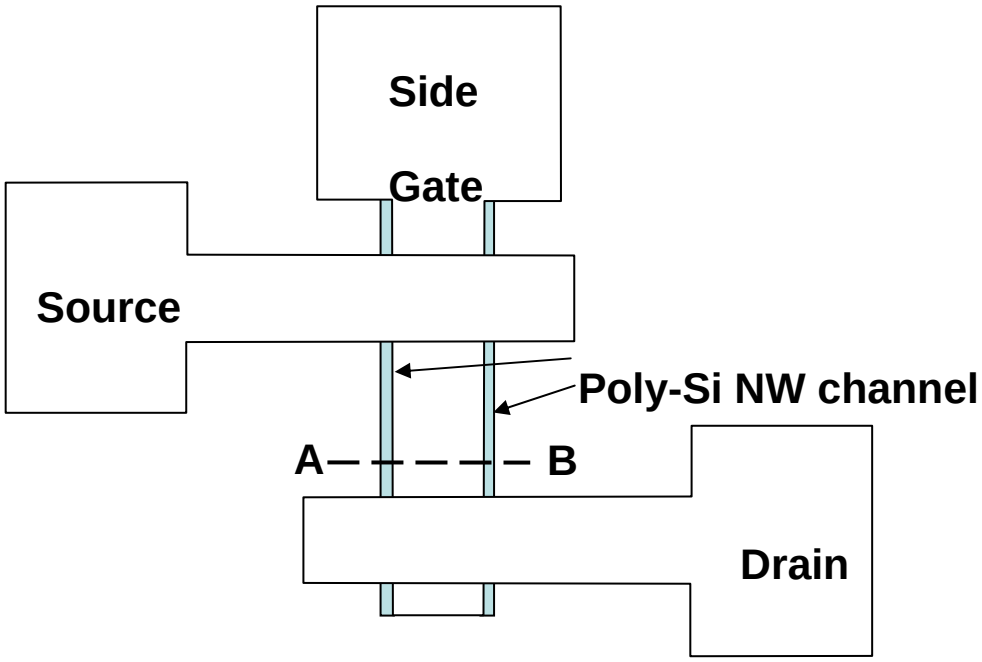
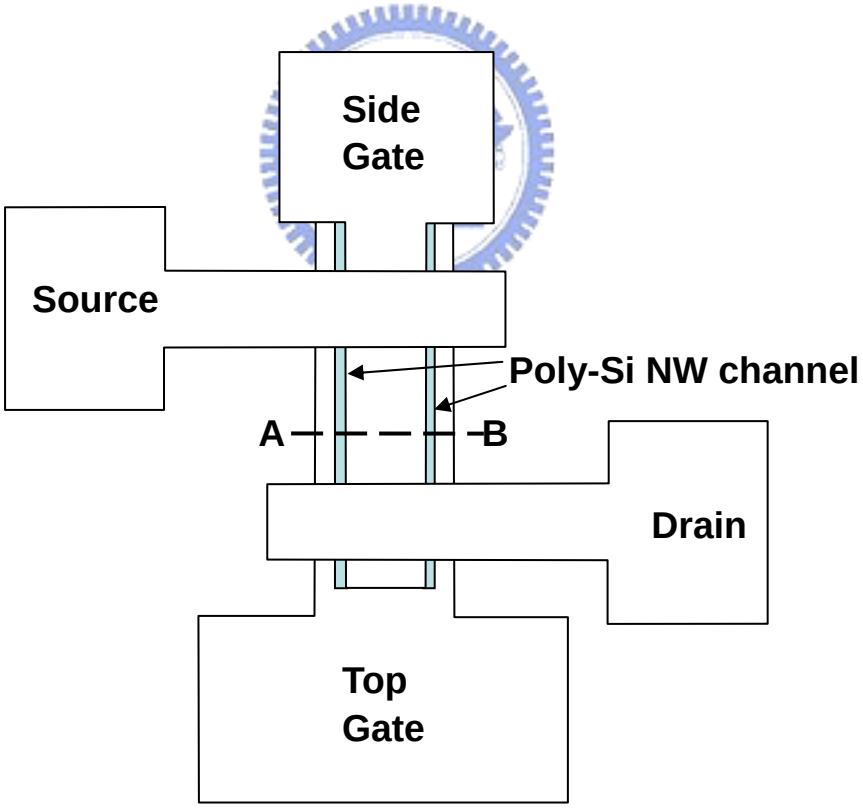
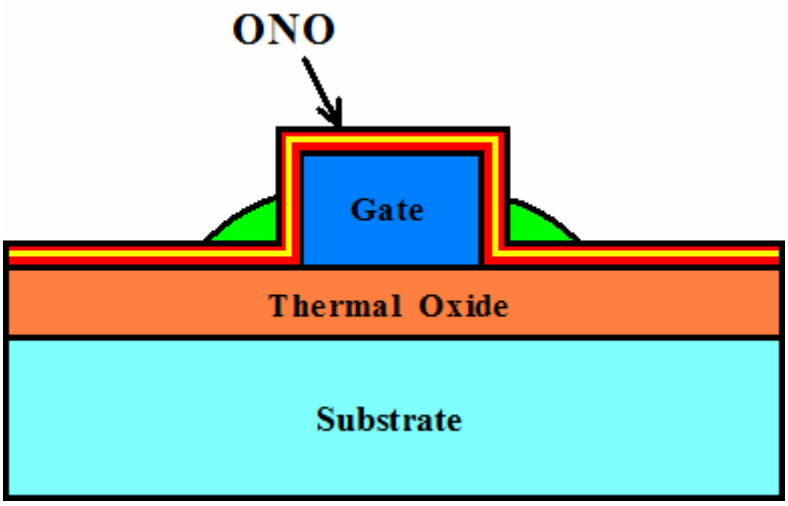


(a)

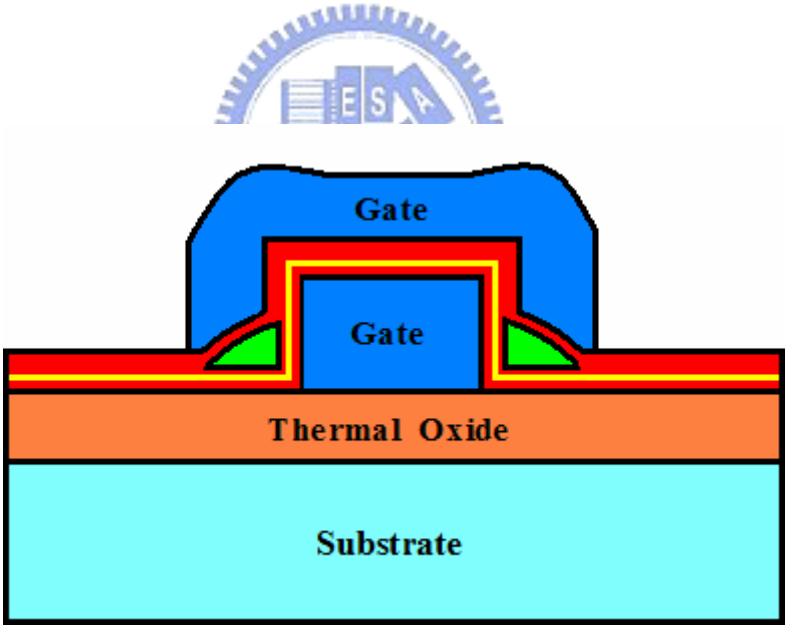


(b)

Fig. 2-1 Top view of (a) single gate (b) double gate NW-SONOS.

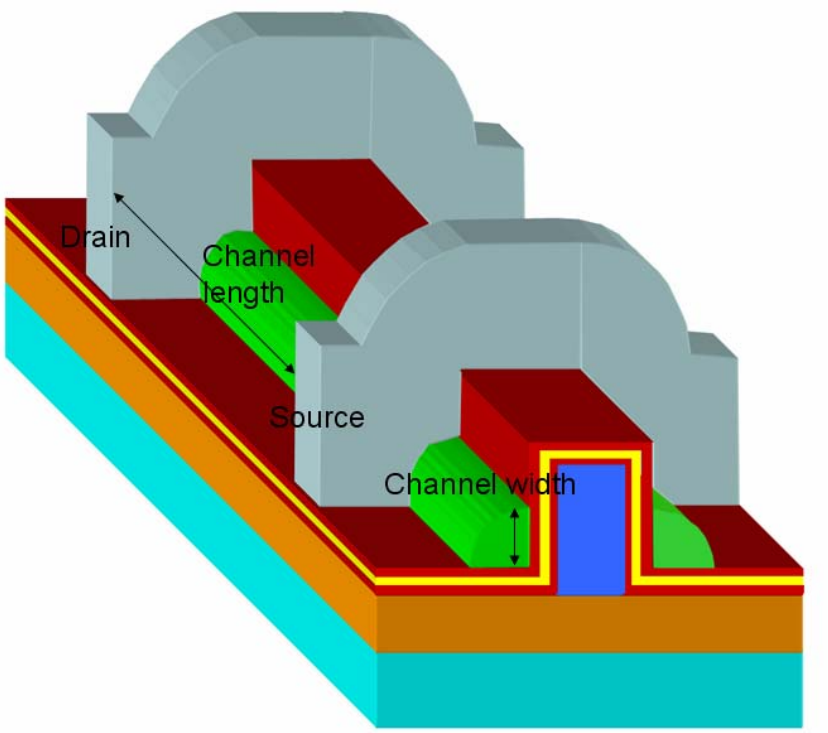


(a)

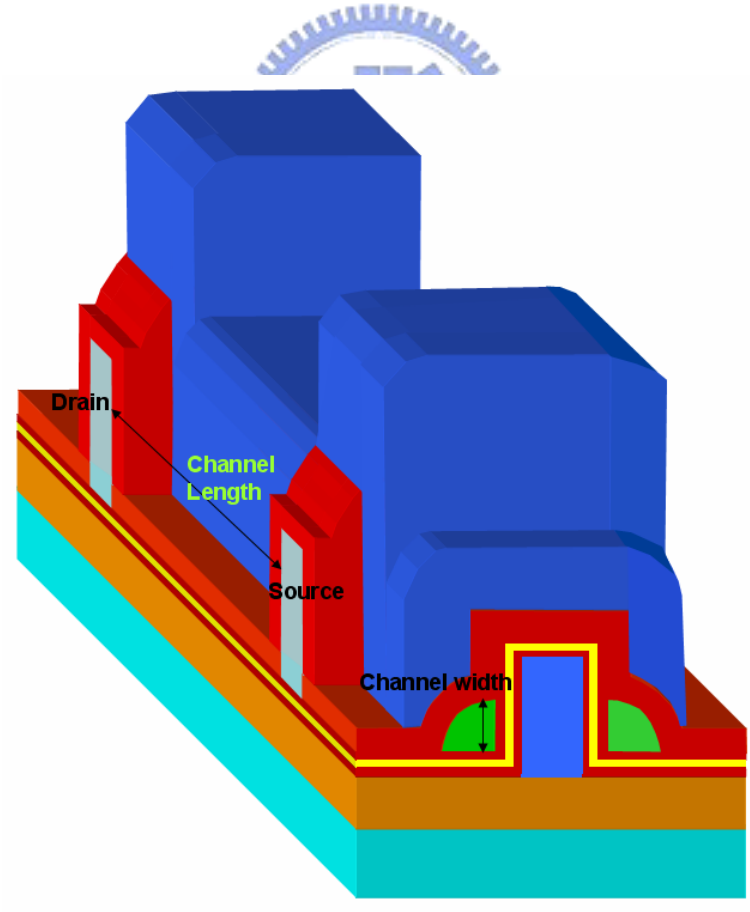


(b)

Fig. 2-2 The cross-sectional views of (a) single- gate (b) double-gated NW-SONOS.



(a)



(b)

Fig. 2-3 The 3D structures of (a) single- and (b) double-gated NW-SONOS devices.

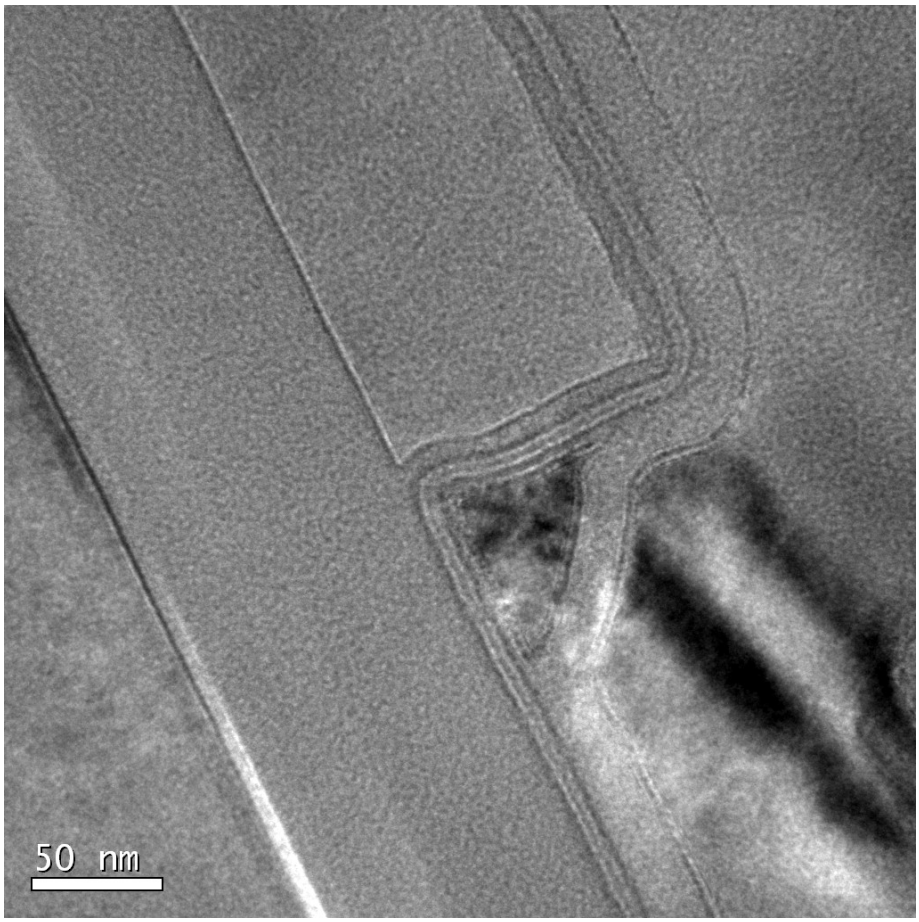


Fig. 2-4 TEM pictures of double-gated SONOS with 180Å-thick top gate oxide.

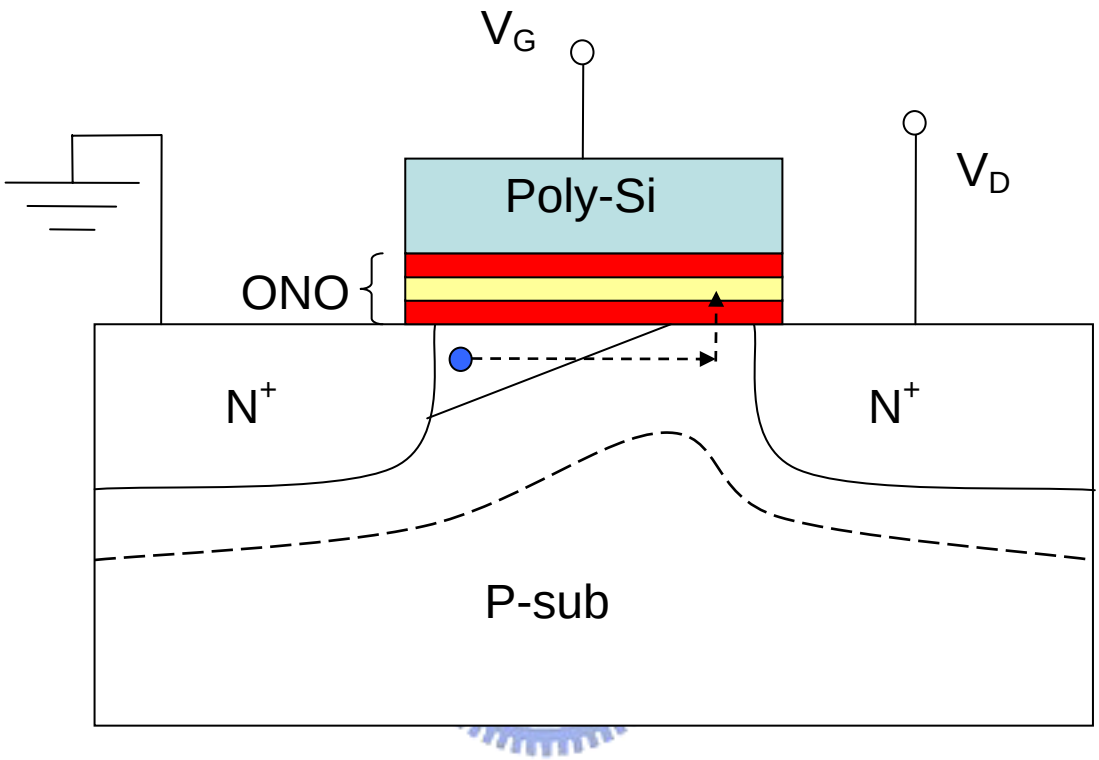


Fig. 2-5 Proposed trajectory of an emitted channel electron. An energetic electron is redirected toward the interface by an acoustic phonon scattering.

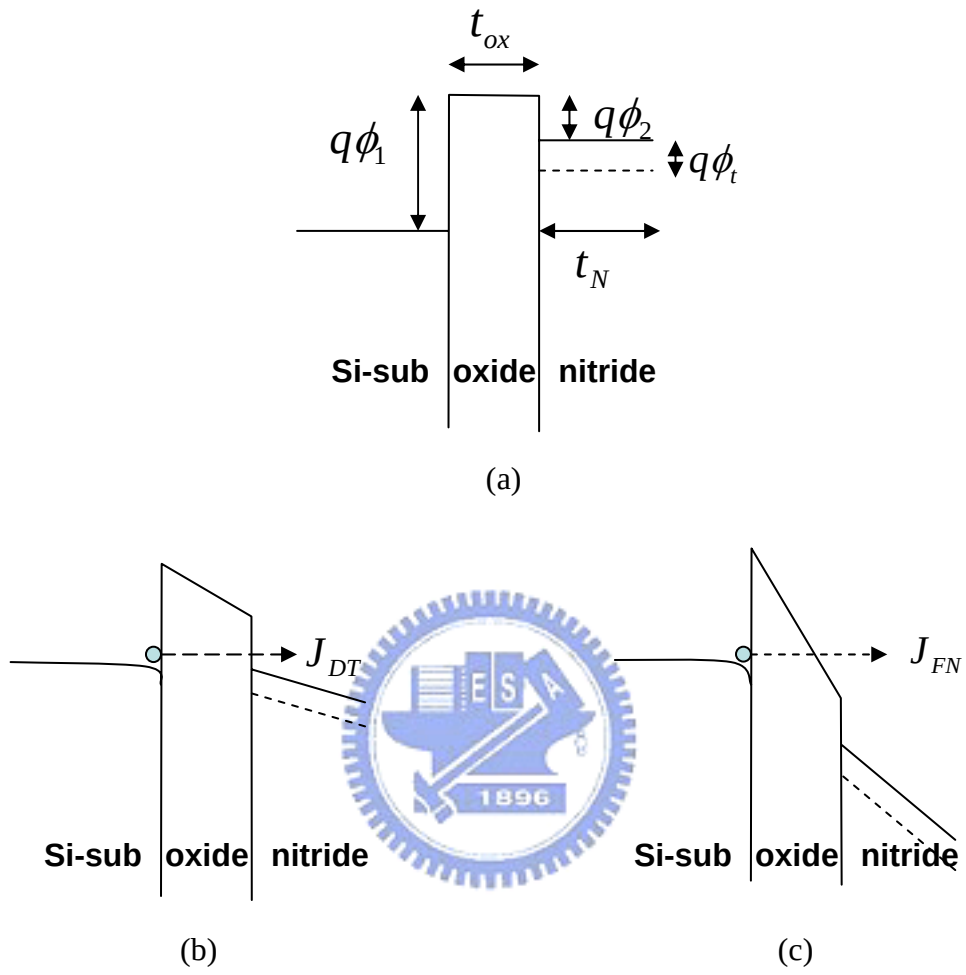
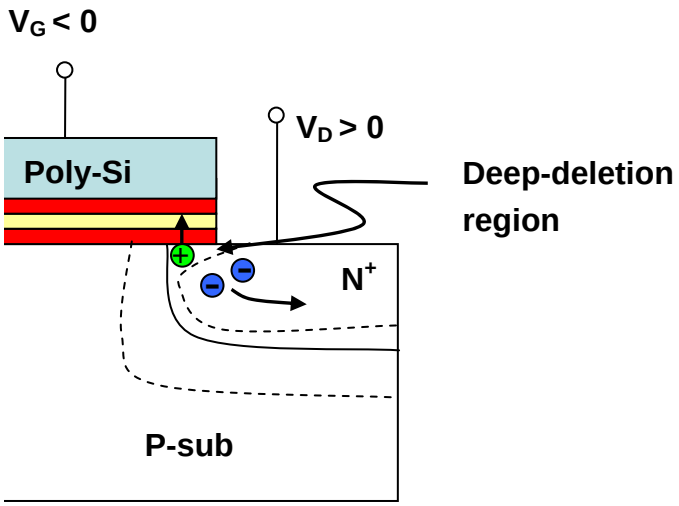
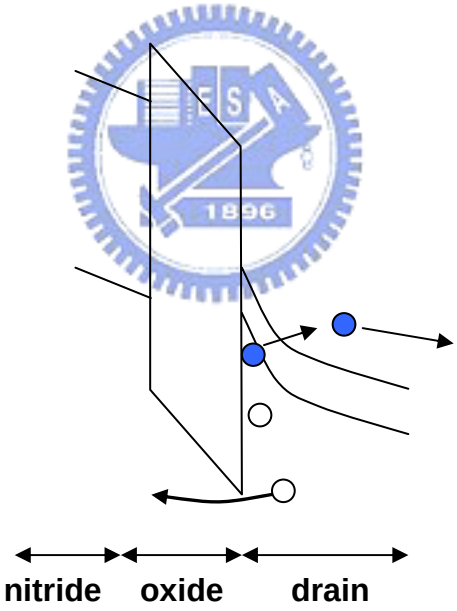


Fig. 2-6 Energy band diagram of ONO structure and illustrations of the physical difference between Fowler-Nordheim and direct tunneling. (a) Energy band diagram of ONO at V=0, where $q\phi_1$ is barrier height between Si-channel and tunneling oxide, $q\phi_2$ is barrier height between tunneling oxide and nitride, $q\phi_t$ is energy difference between the conduction band and trap state of nitride, t_{ox} and t_N are thickness of tunneling oxide and nitride respectively. (b) Direct tunneling is associated with transversal of a trapezoidal barrier. (c) Fowler-Nordheim Tunneling is associated with transversal of a triangular barrier.



(a)



(b)

Fig. 2-7 Illustration of Band to band tunneling. (a) Breakdown occurs in the deep-depletion layer in the n^+ drain. (b) The path of electron-hole pair in energy band diagram.

(SG , X , D , S)					
	V_{SG}(V)	V_{TG}(V)	V_D(V)	V_S(V)	Time(s)
Program Speed Test	**13 ~ 15**	**X**	**0**	**0**	**1μs ~ 10ms**
Erase Speed Test	**-12 ~ -14**	**X**	**0**	**0**	**1μs ~ 1s**
Program for Reliability Test	**15**	**X**	**0**	**0**	**0.5ms**
Erase for Reliability Test	**-12**	**X**	**0**	**0**	**50ms**

Table 3-1. The program / erase condition for single-gated SONOS

(SG , TG , D , S)					
	V_{SG}(V)	V_{TG}(V)	V_D(V)	V_S(V)	Time(s)
Program Speed Test	**13 ~ 15**	**0 ~ 15**	**0**	**0**	**1μs ~ 10ms**
Erase Speed Test	**-12 ~ -14**	**0 ~ -5**	**0**	**0**	**1μs ~ 1s**
Program for Reliability Test	**15**	**0 ~ 15**	**0**	**0**	**0.5ms**
Erase for Reliability Test	**-12**	**0**	**0**	**0**	**50ms**

Table 3-2. The program / erase condition for double-gated SONOS

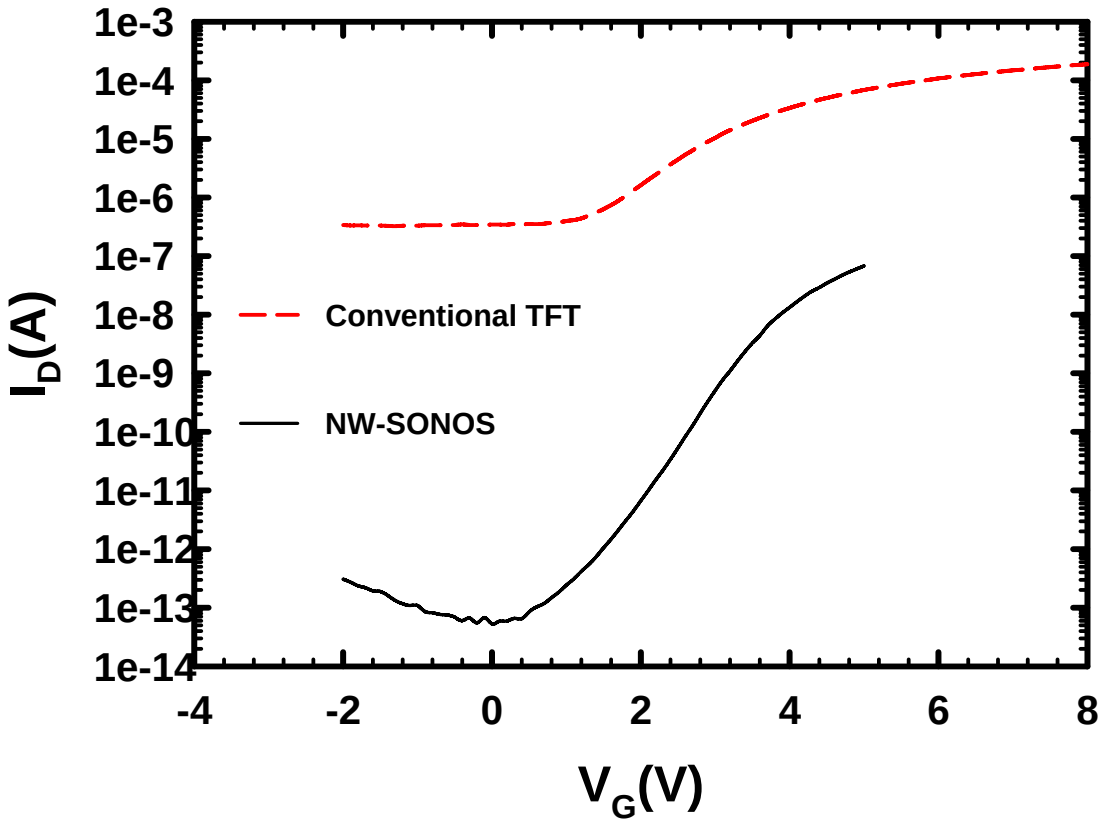
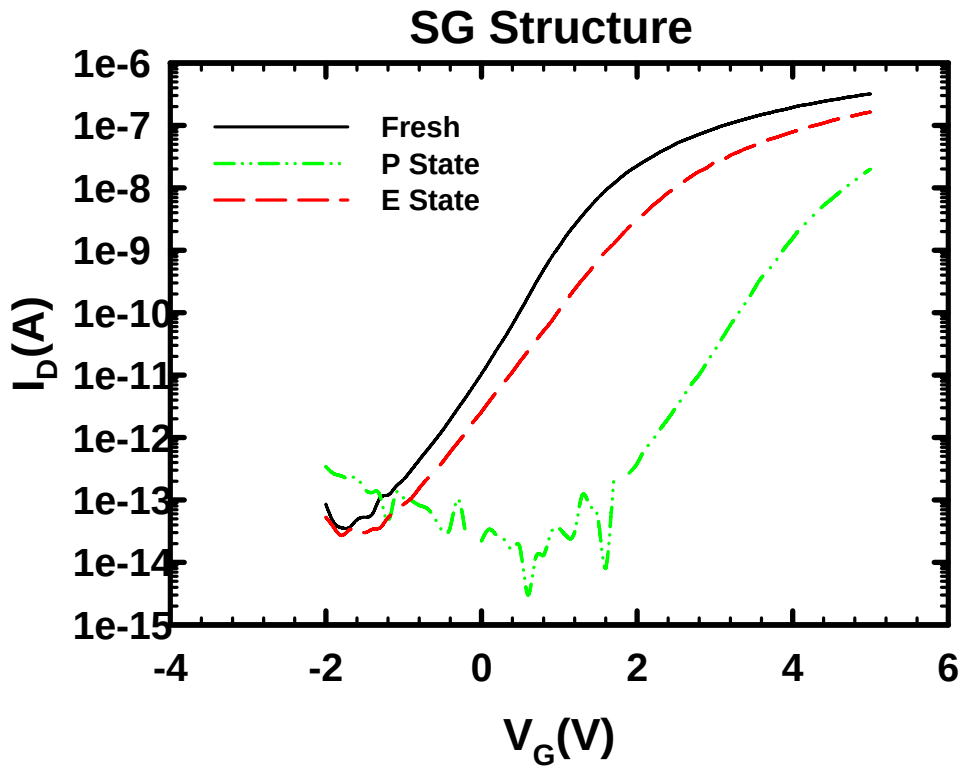
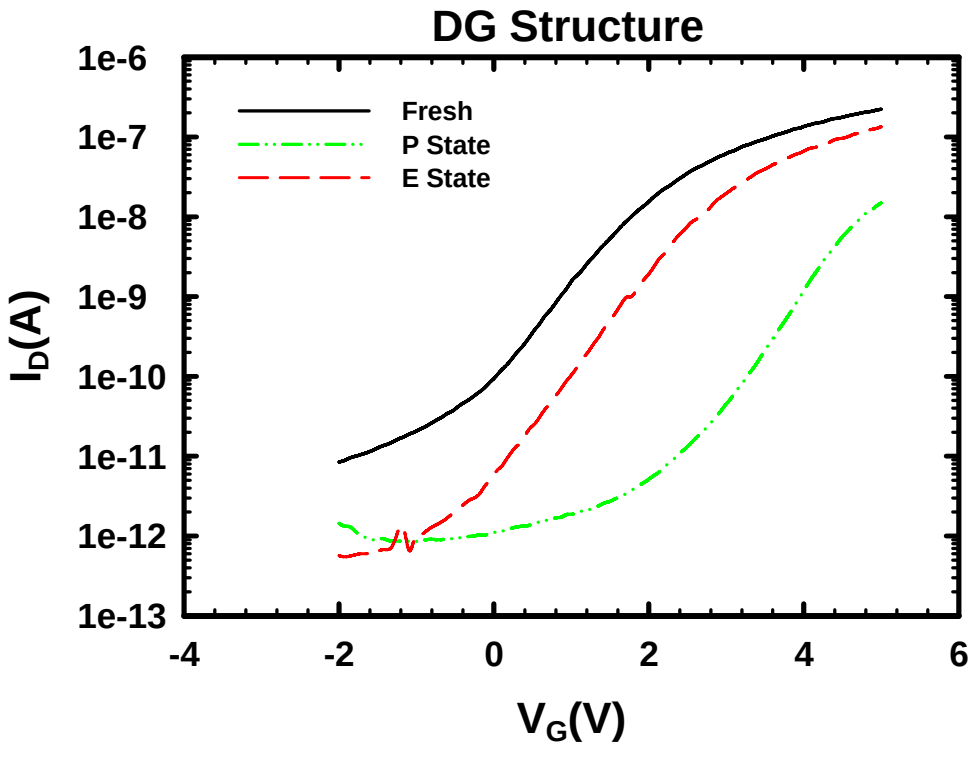


Fig. 3-1 Transfer characteristics of conventional TFT and NW-SONOS.

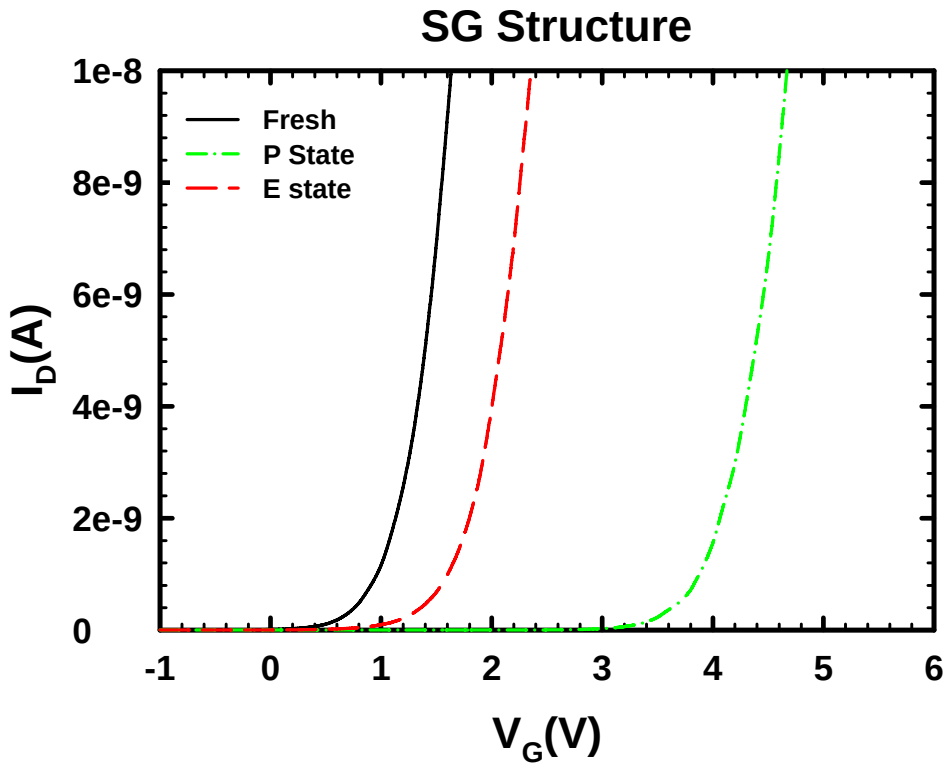


(a)

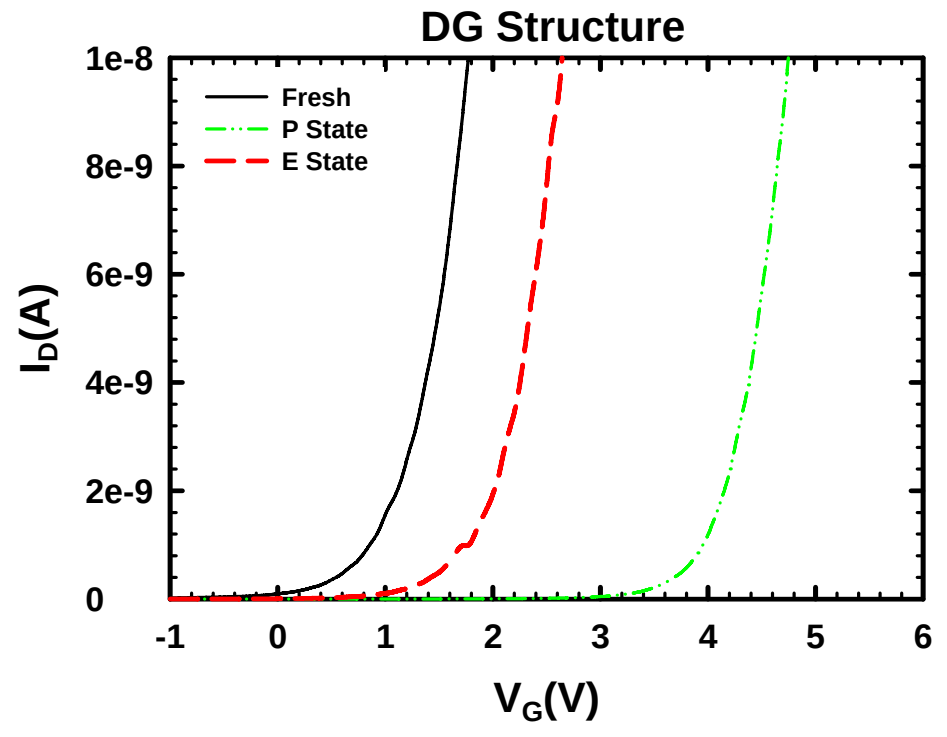


(b)

Fig. 3-2 Fresh, programming state, and erasing state I_D-V_G curves under logarithmic scale for (a) single-gated and (b) double-gated SONOS.



(a)



(b)

Fig. 3-3 Fresh, programming state, and erasing state I_D-V_G curves under linear scale for (a) single-gated and (b) double-gated SONOS.

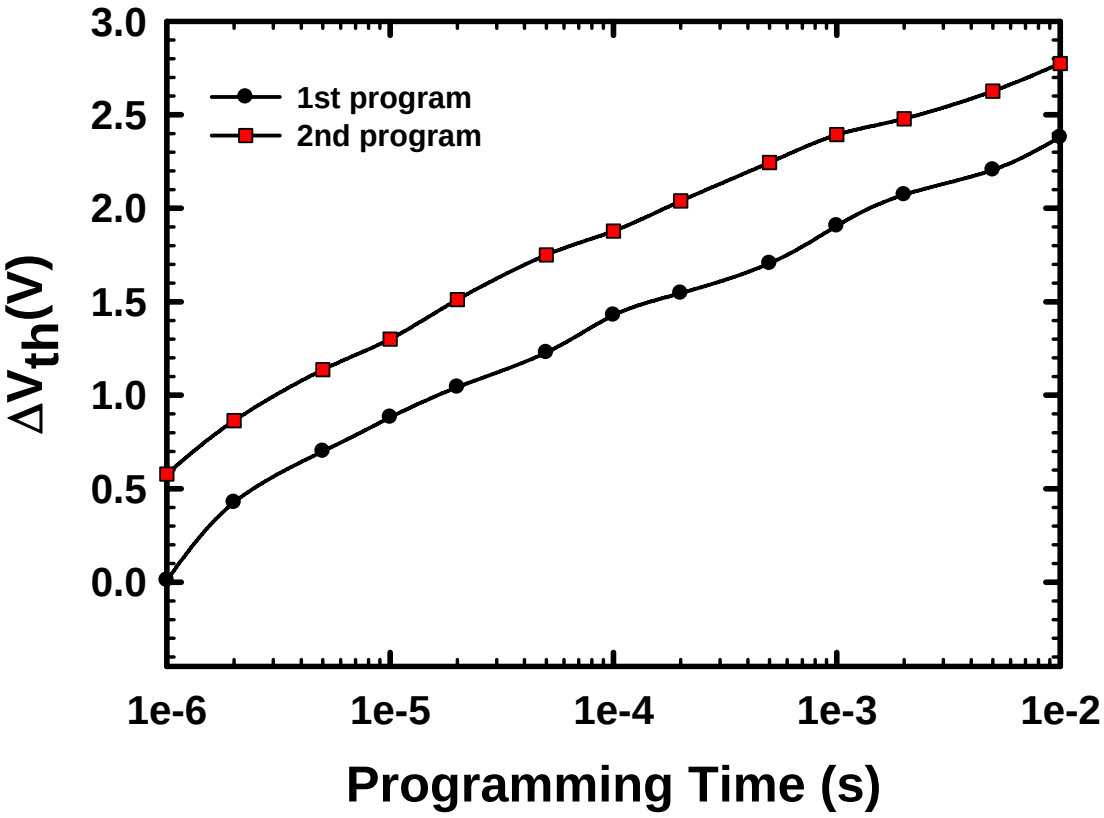


Fig. 3-4 Programming characteristics of NW-SONOS after first and second programming.

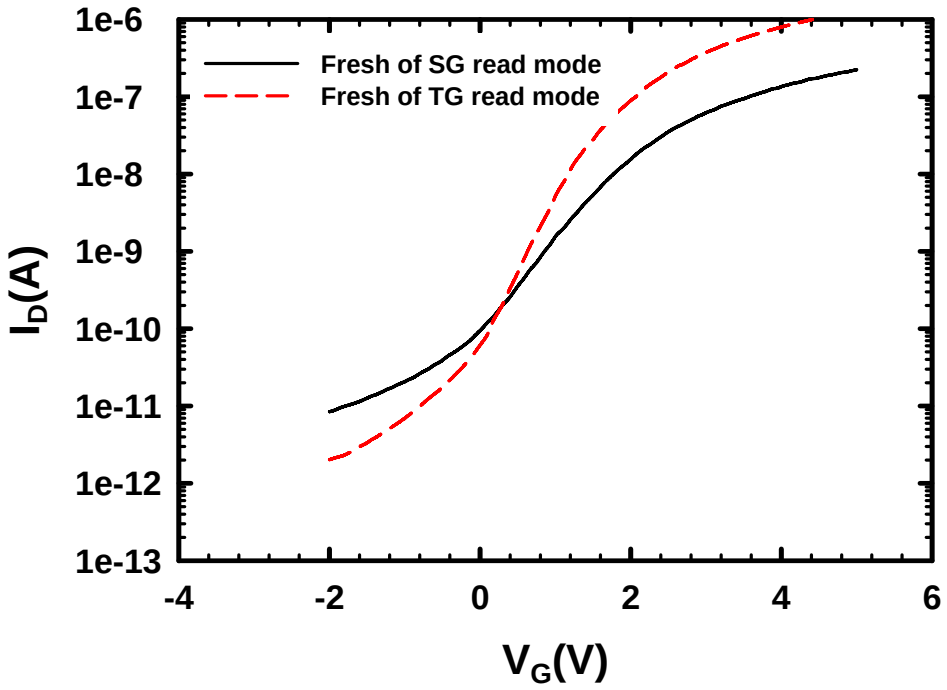


Fig. 3-5 (a) Fresh I_D-V_G curve of side-gate read and top-gate read modes.

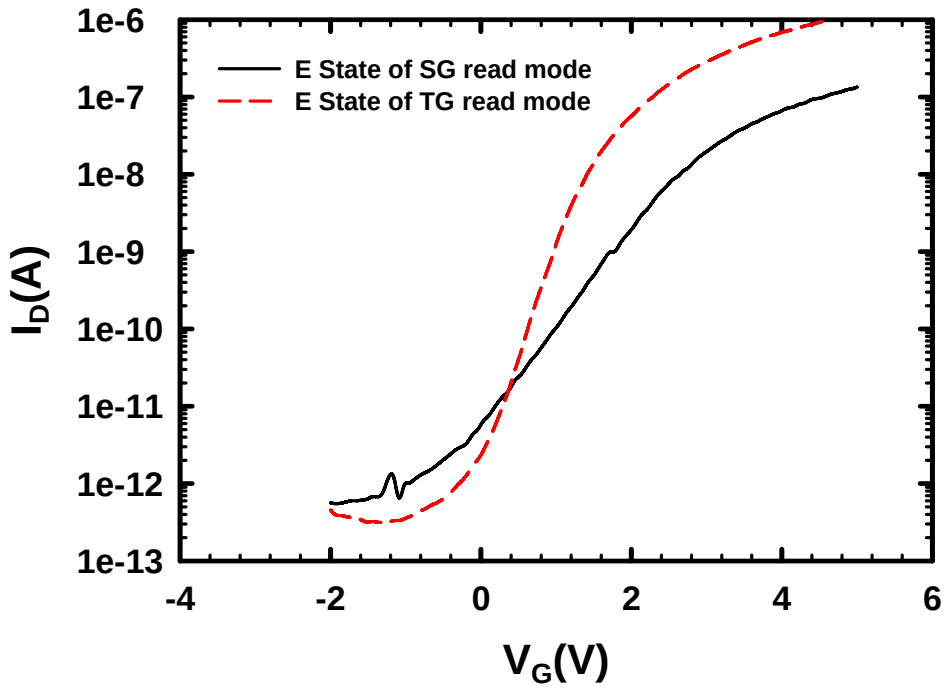
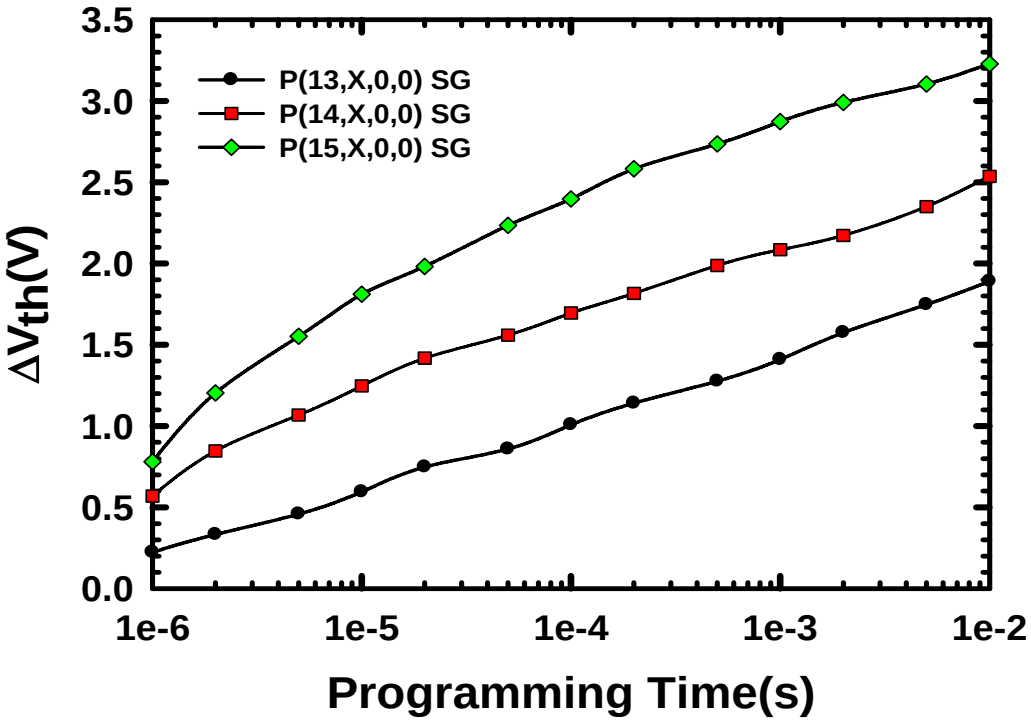
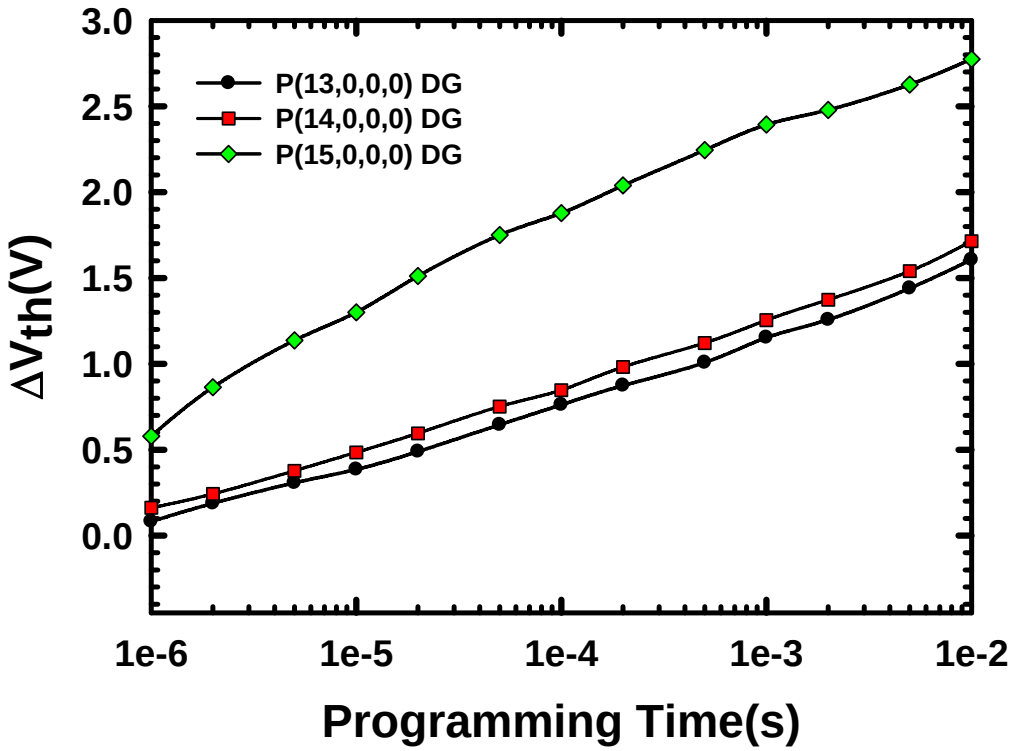


Fig. 3-5 (b) I_D-V_G curve at erasing state for side-gate read and top-gate read modes.

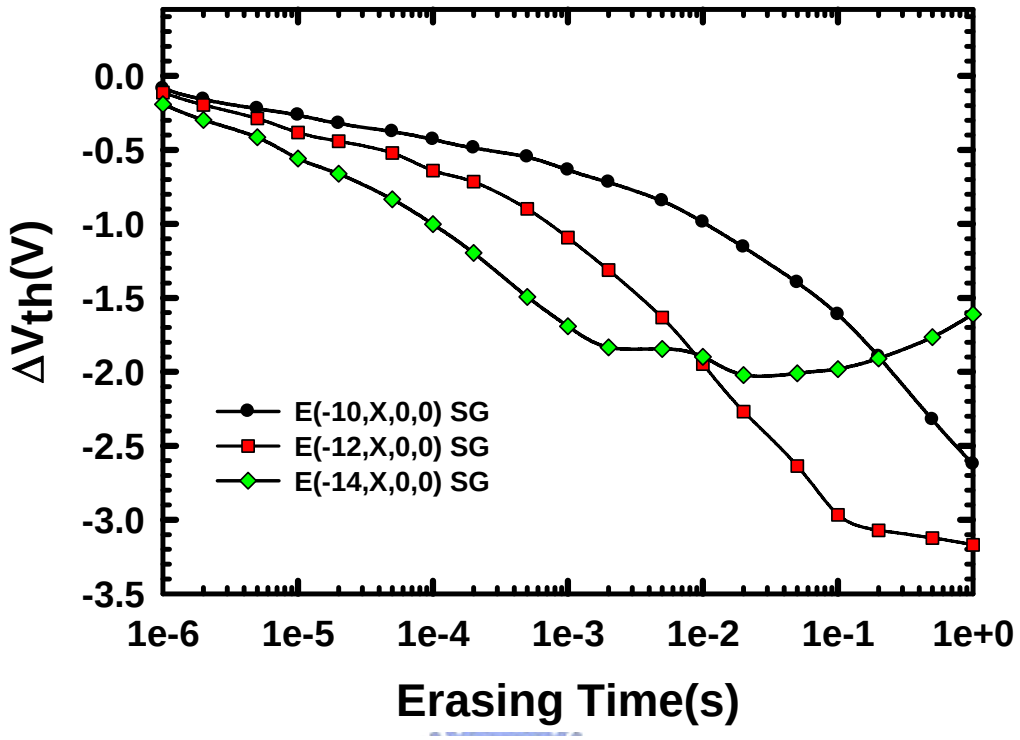


(a)

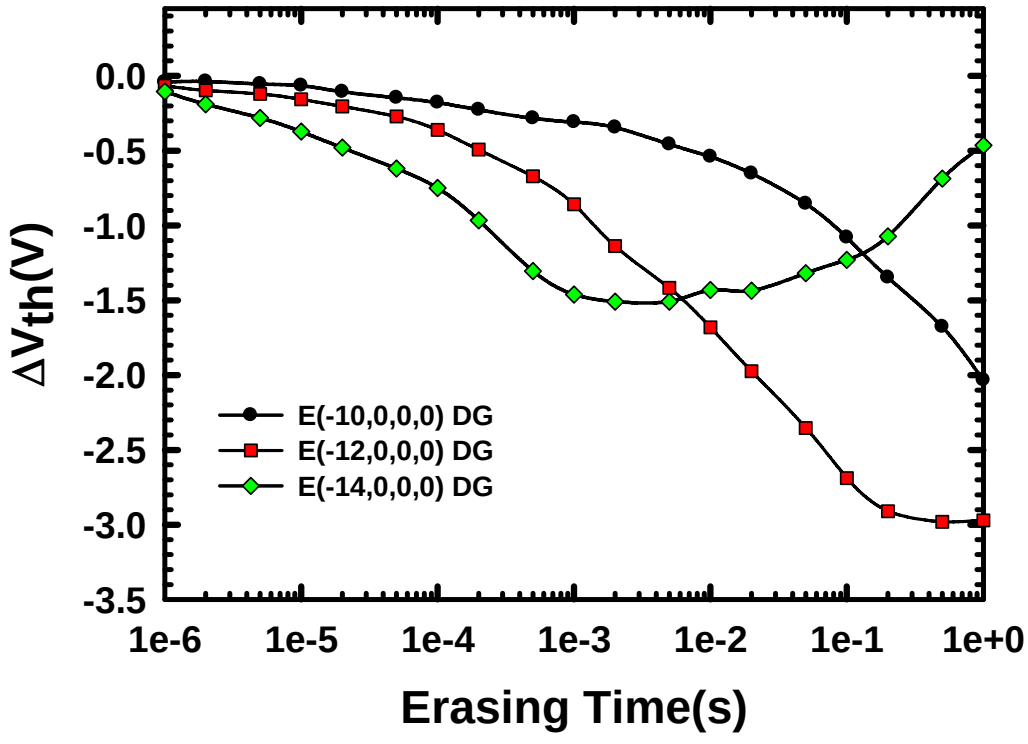


(b)

Fig. 3-6 Programming characteristics of (a) single-gated (b) double-gated SONOS with different side-gate biases.

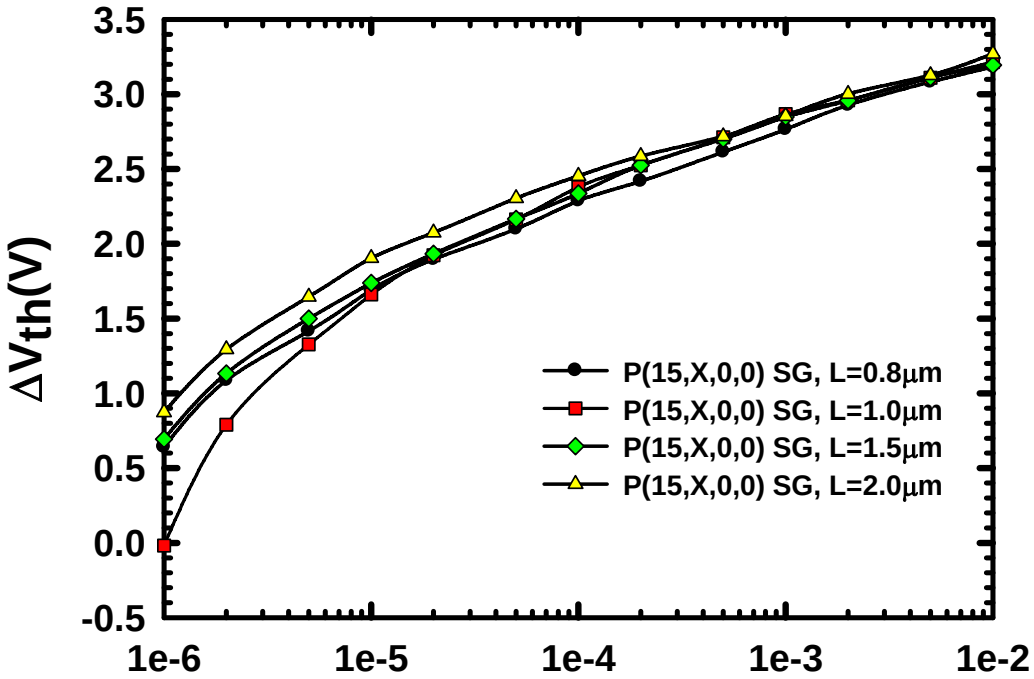


(a)

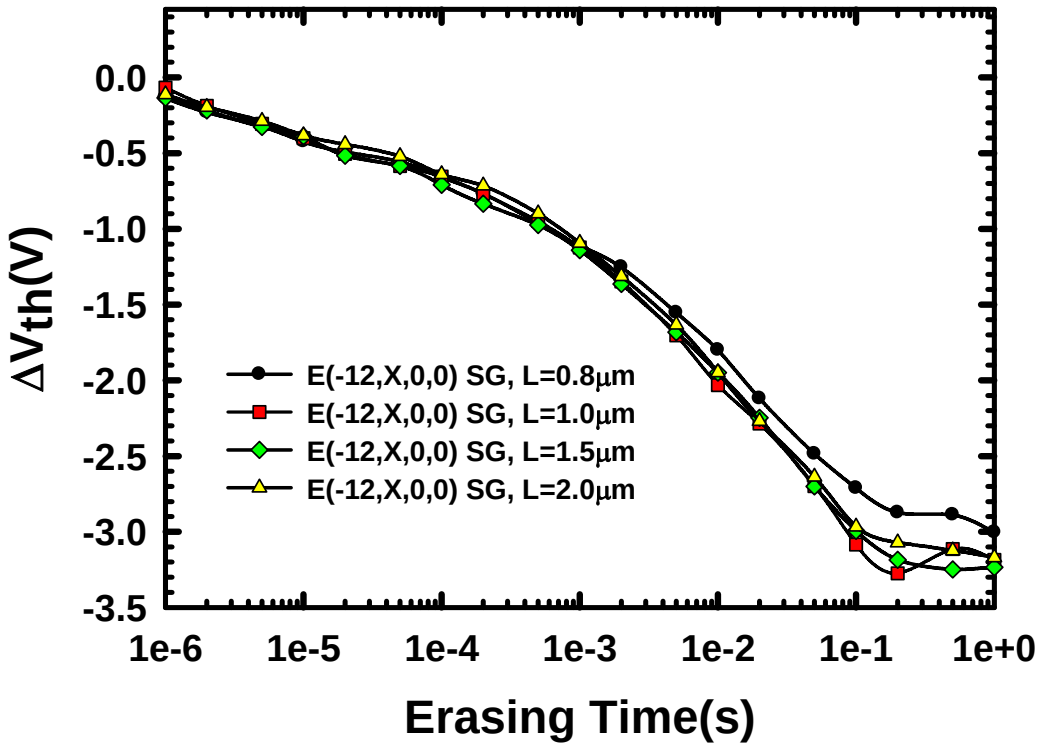


(b)

Fig. 3-7 Erasing characteristics of (a) single-gated (b) double-gated SONOS with different side-gate biases.

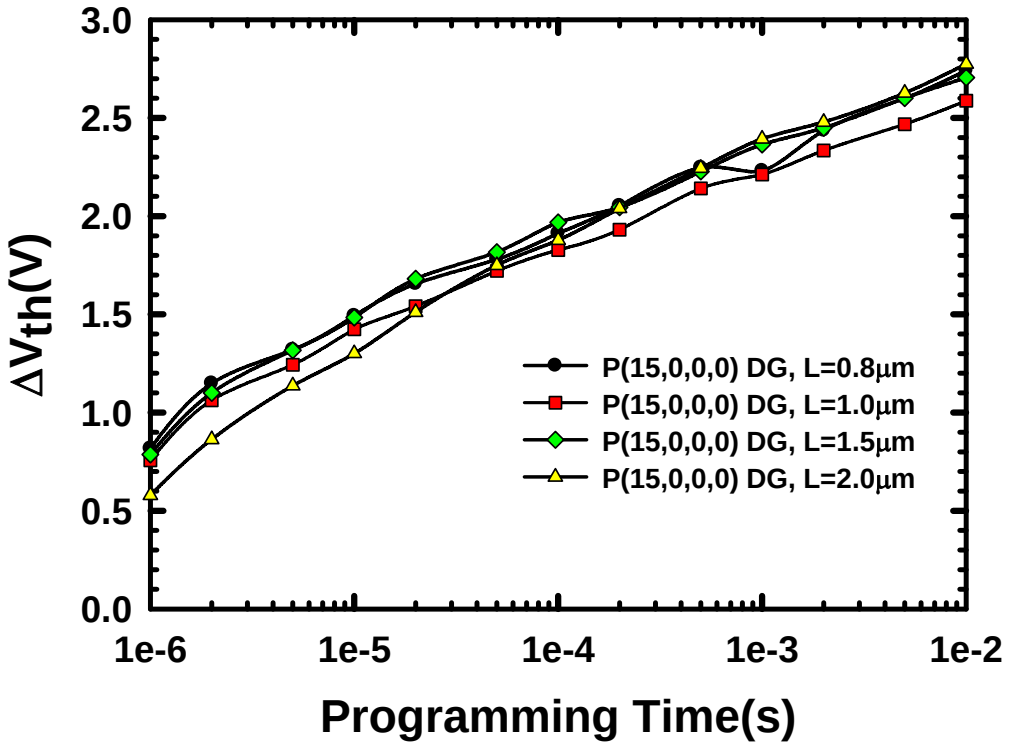


(a)

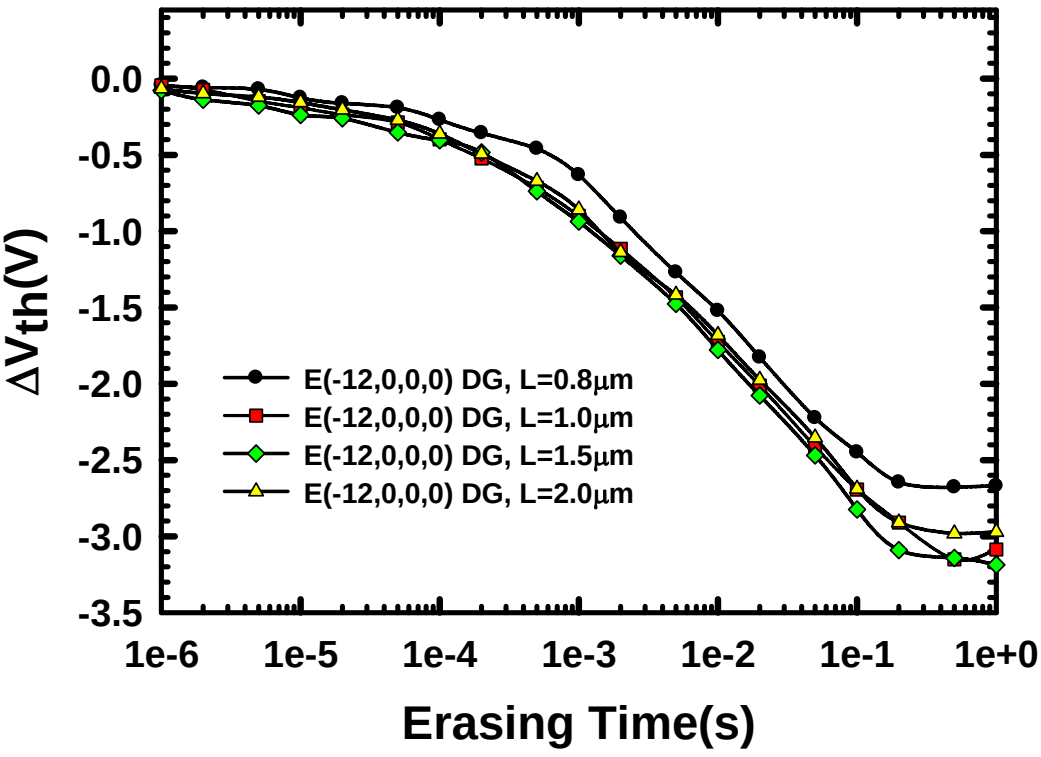


(b)

Fig. 3-8 (a) Programming and (b) erasing characteristics of single-gated SONOS with different channel lengths.

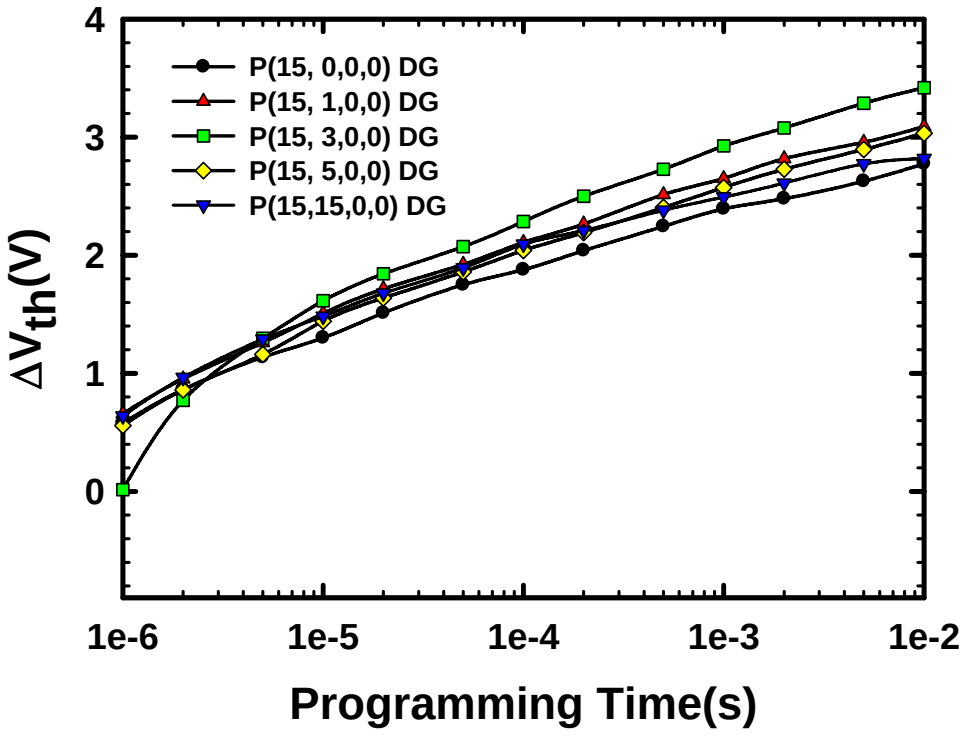


(a)

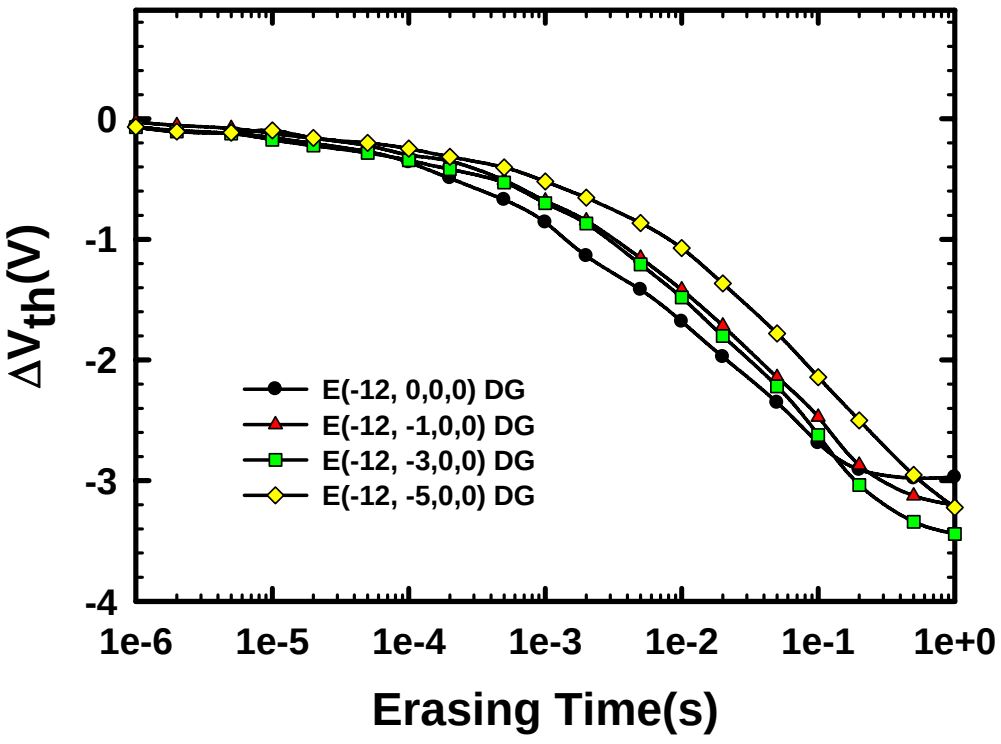


(b)

Fig. 3-9 (a) Programming and (b) erasing characteristics of double-gated SONOS with different channel lengths.



(a)



(b)

Fig. 3-10 (a) Programming and (b) erasing characteristics of double-gated SONOS with different top-gate biases.

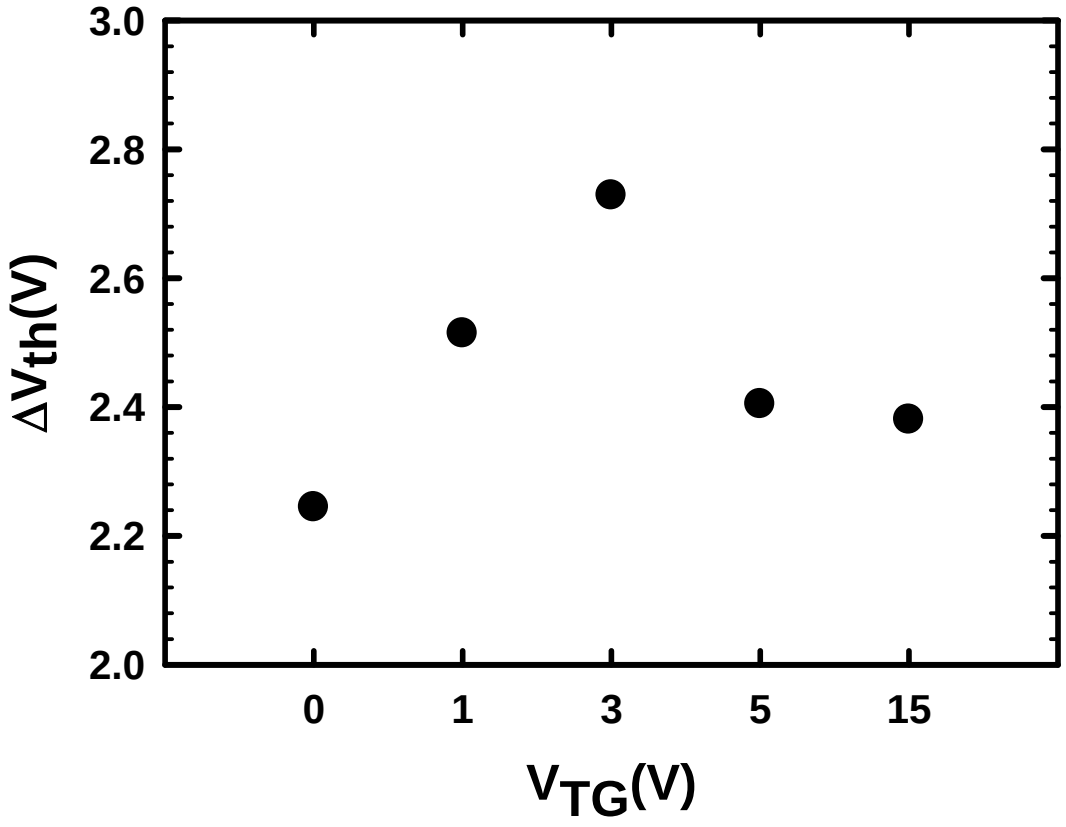


Fig. 3-11 V_{th} shift of double-gated SONOS at programming time = 0.5msec, side-gate voltage = 15V under different top-gate biases.

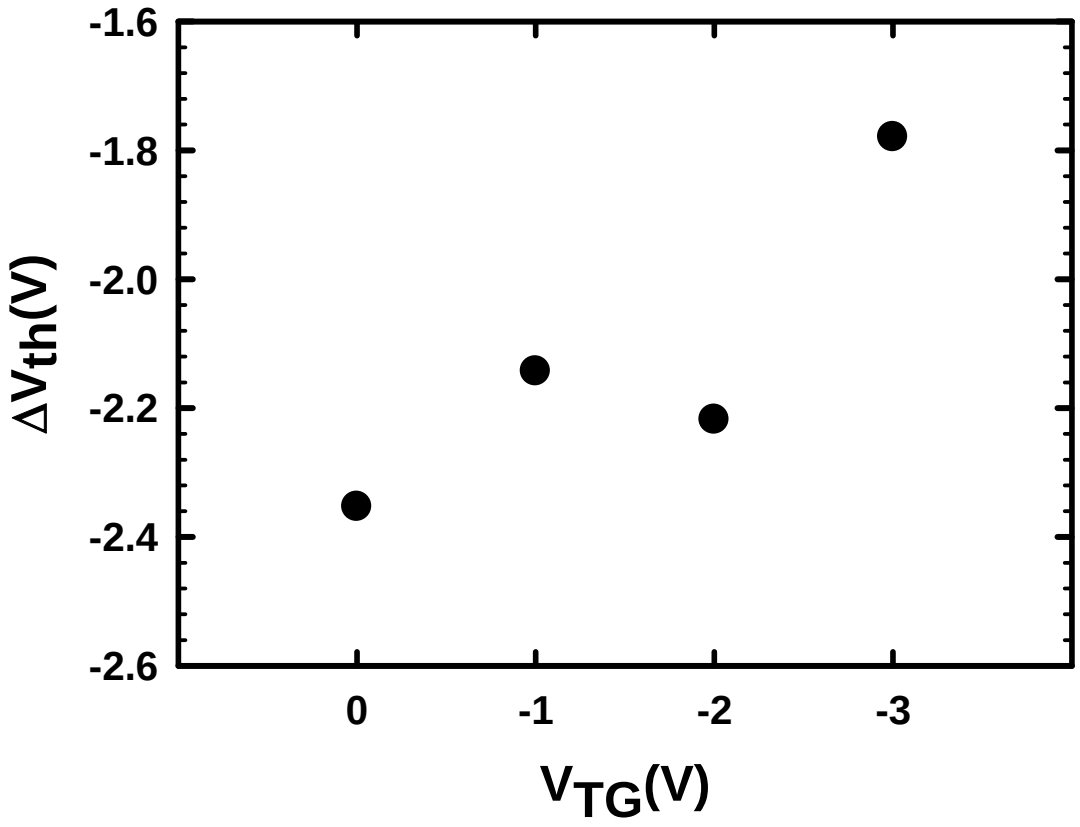
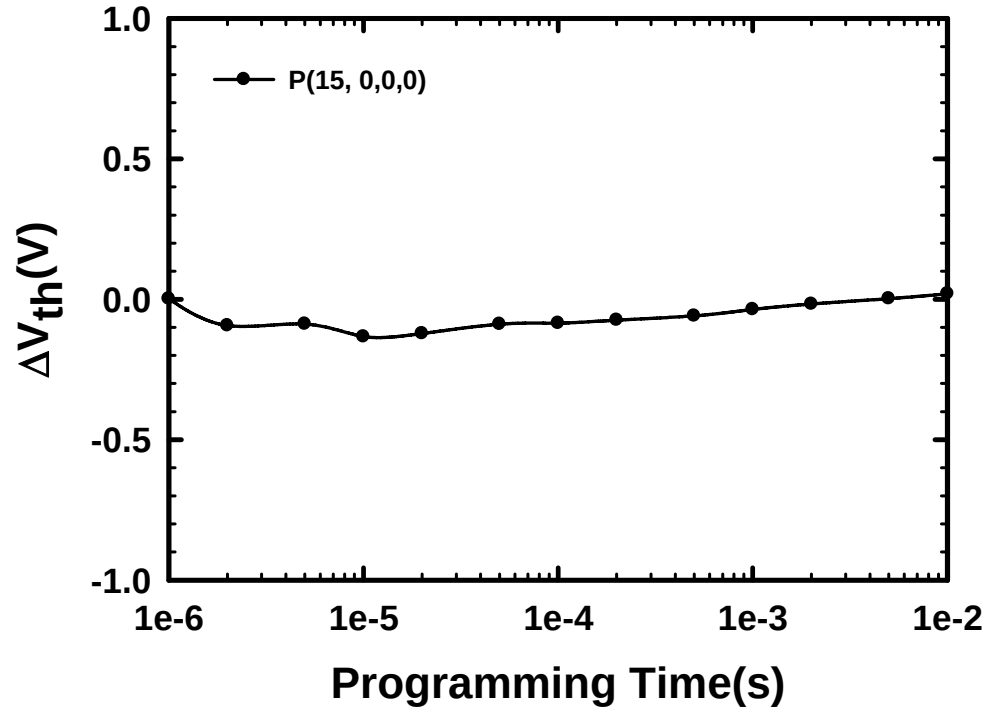
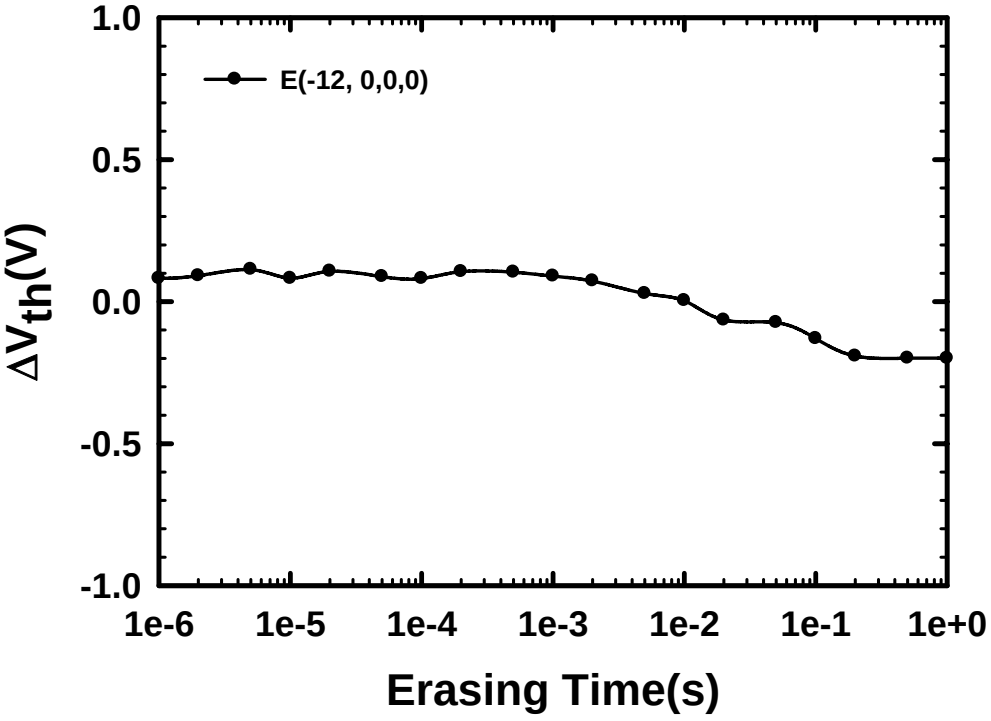


Fig. 3-12 V_{th} shift of double-gated SONOS at erasing time = 0.5msec, side-gate voltage = -12V under different top-gate biases.

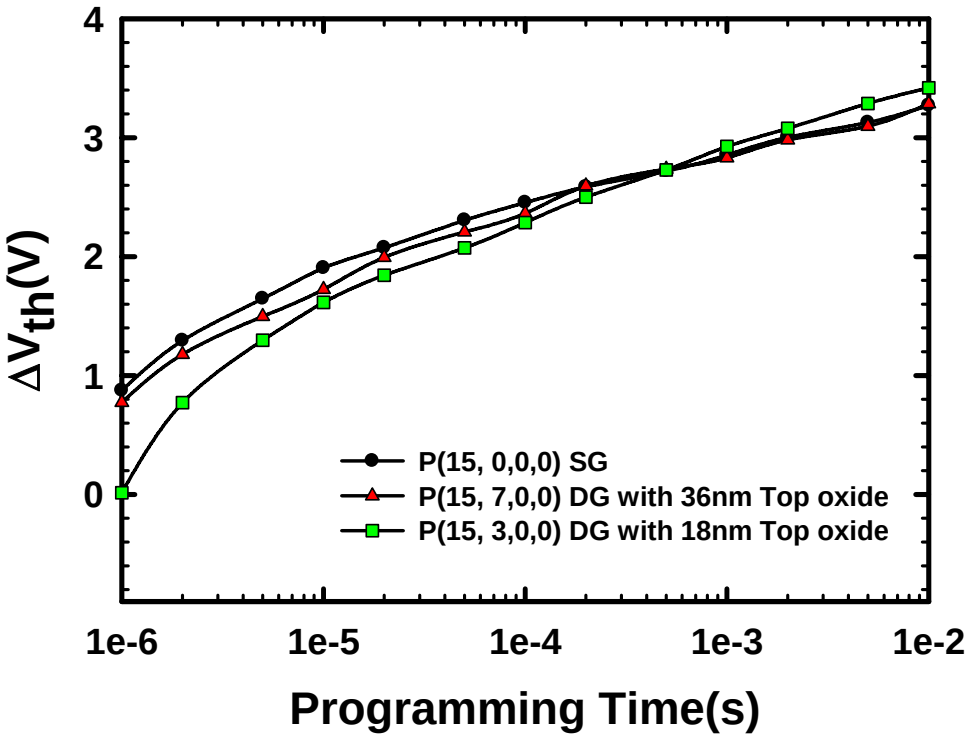


(a)

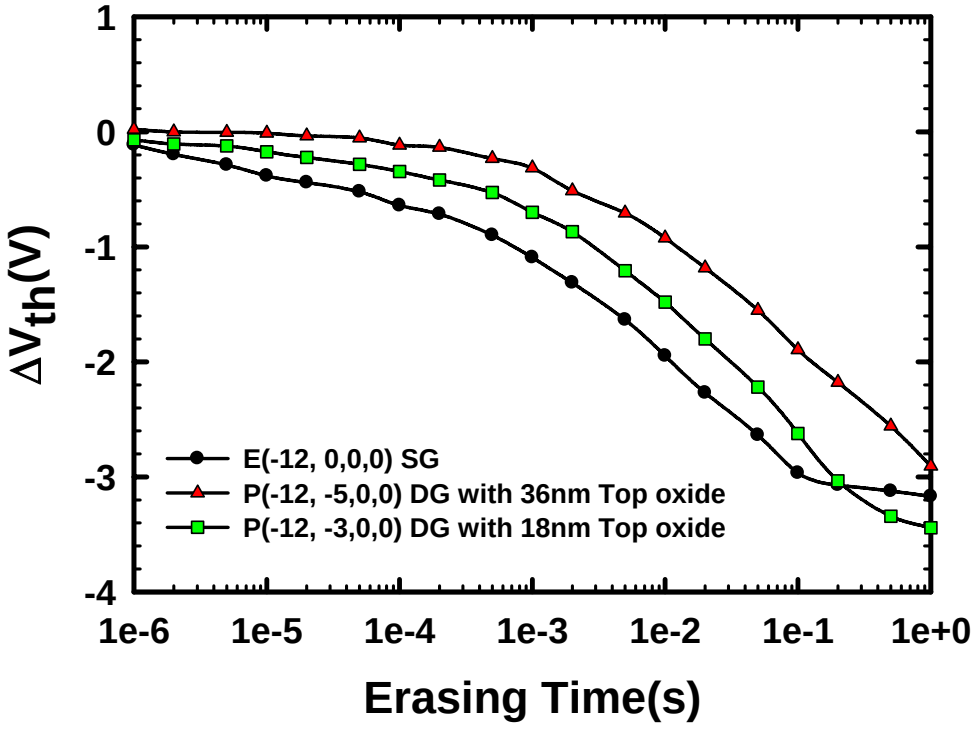


(b)

Fig. 3-13 (a) programming and (b) erasing characteristics of double-gated SONOS under top-gate read mode, i.e., ΔV_{th} is the V_{th} shift of top-gate.



(a)



(b)

Fig. 3-14 Comparisons of (a) programming and (b) erasing characteristics between single-gated SONOS and double-gated SONOS.

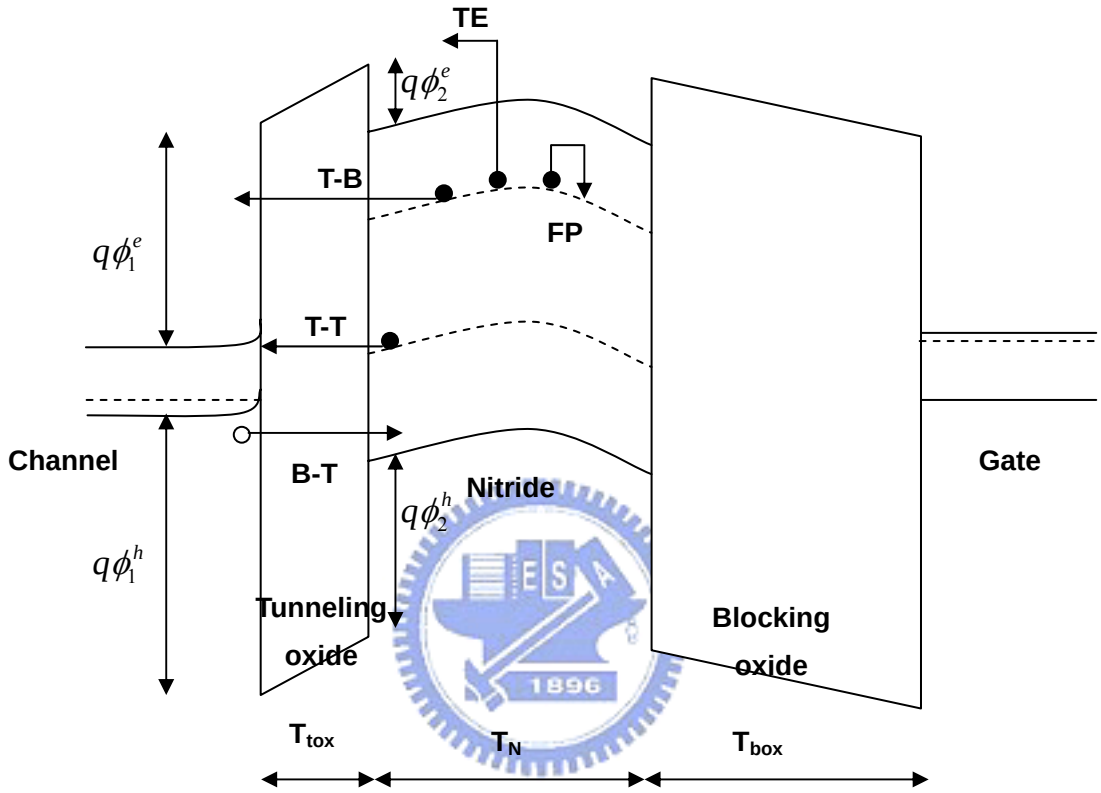


Fig. 4-1 Band diagram of trapped charge loss path in SONOS: trap-to-band tunneling (TB), trap-to-trap tunneling (T-T), band-to-trap tunneling (B-T), thermal excitation (TE) and Frenkel-Poole emission (PF).

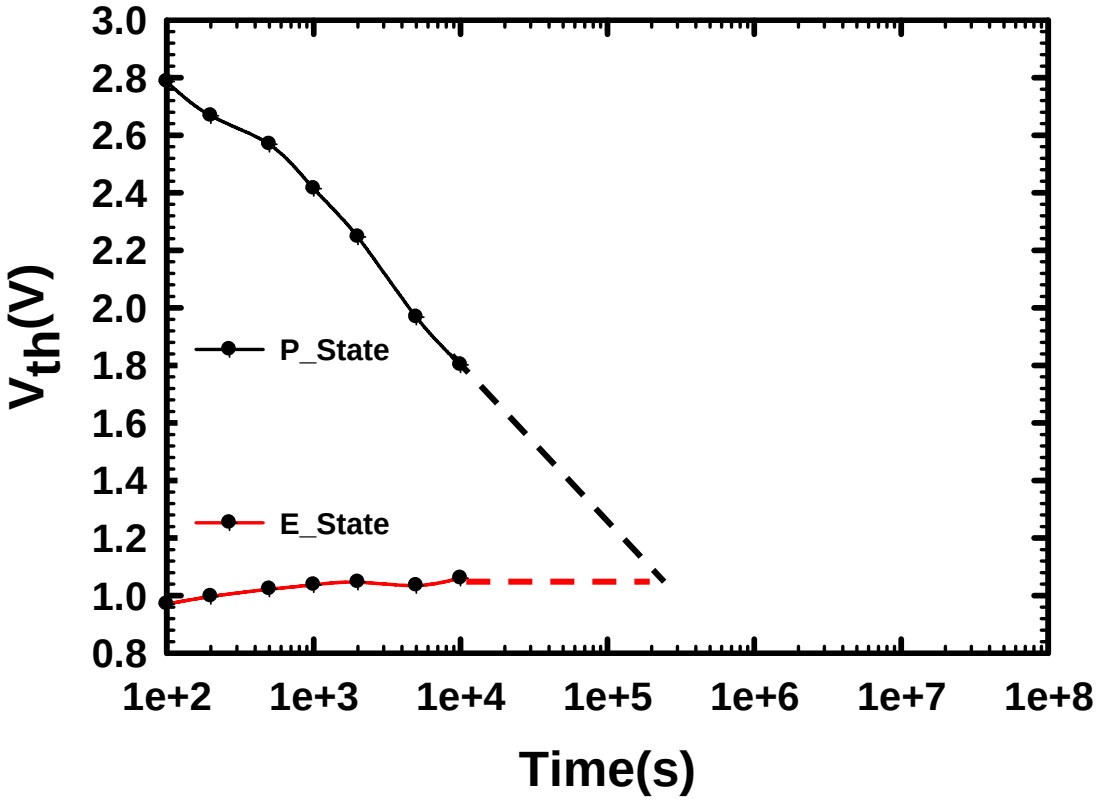


Fig. 4-2 Retention characteristics of single-gated SONOS.

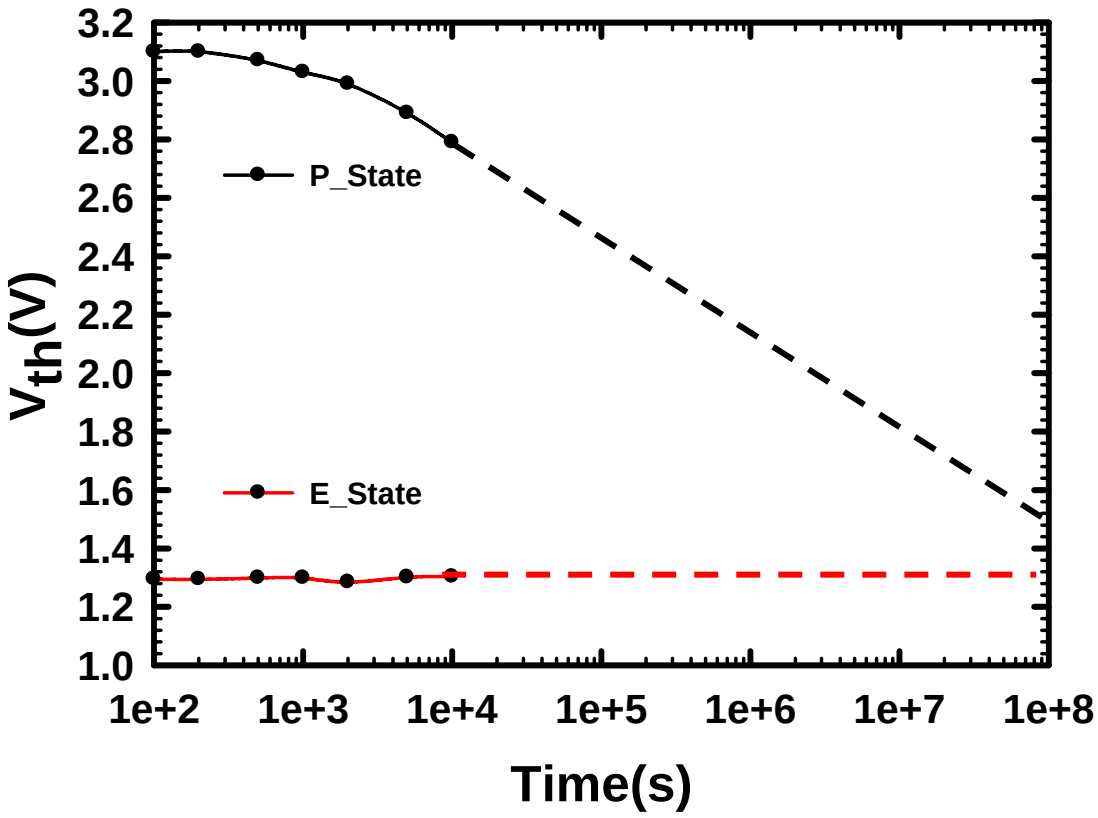


Fig. 4-3 Retention characteristics of double-gated SONOS.

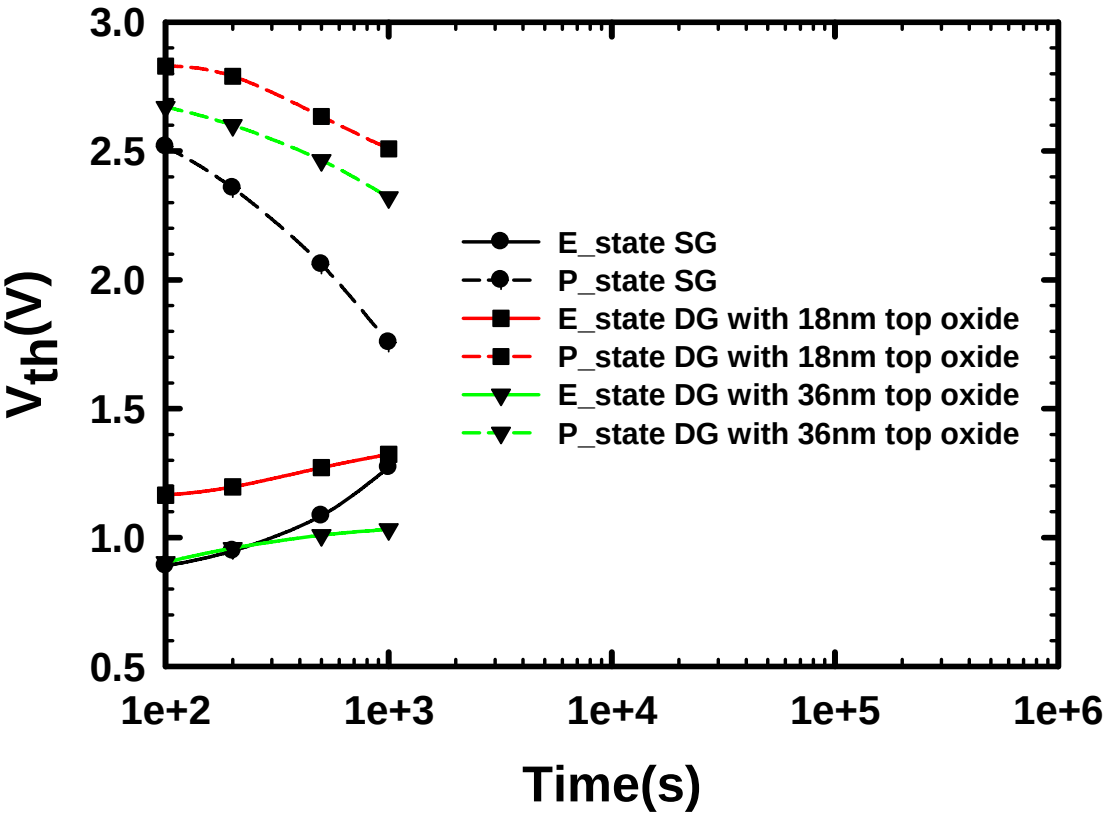


Fig. 4-4 Retention characteristics under the influence of an additional electric field. For programming, -2V is applied to the side-gate; for erasing, 2V is applied to the side-gate.

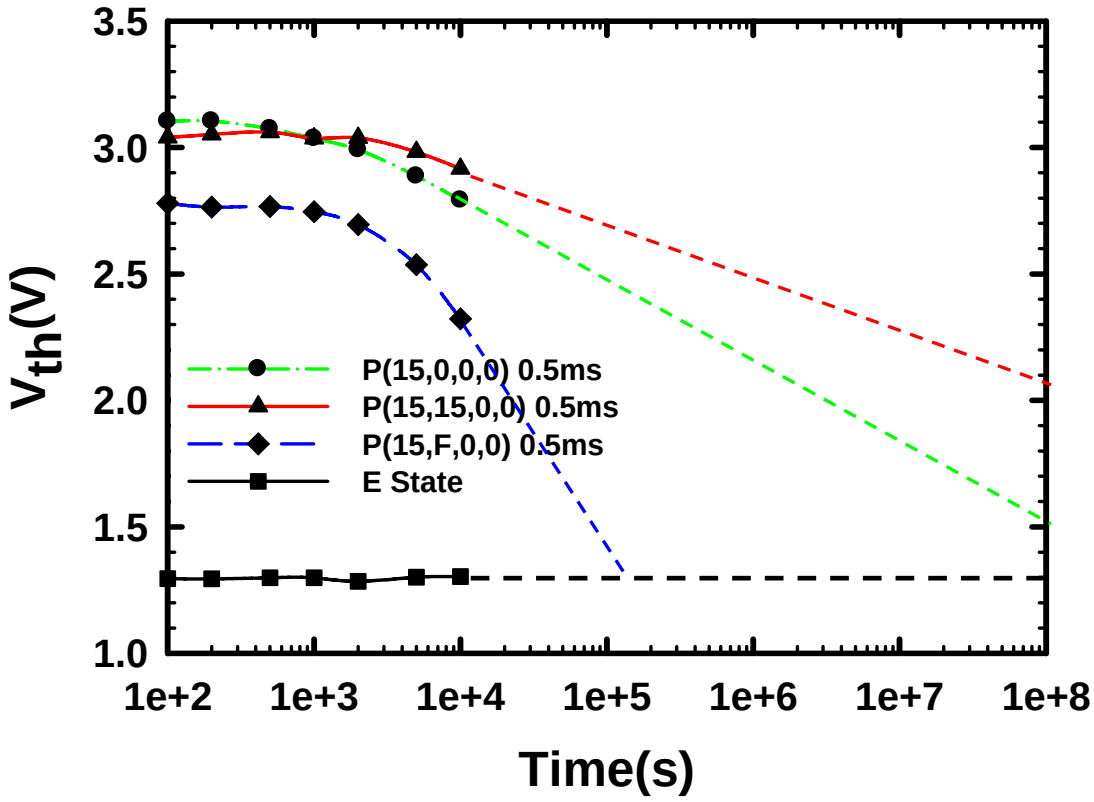


Fig. 4-5 Retention characteristics of double-gated SONOS under different programming conditions.

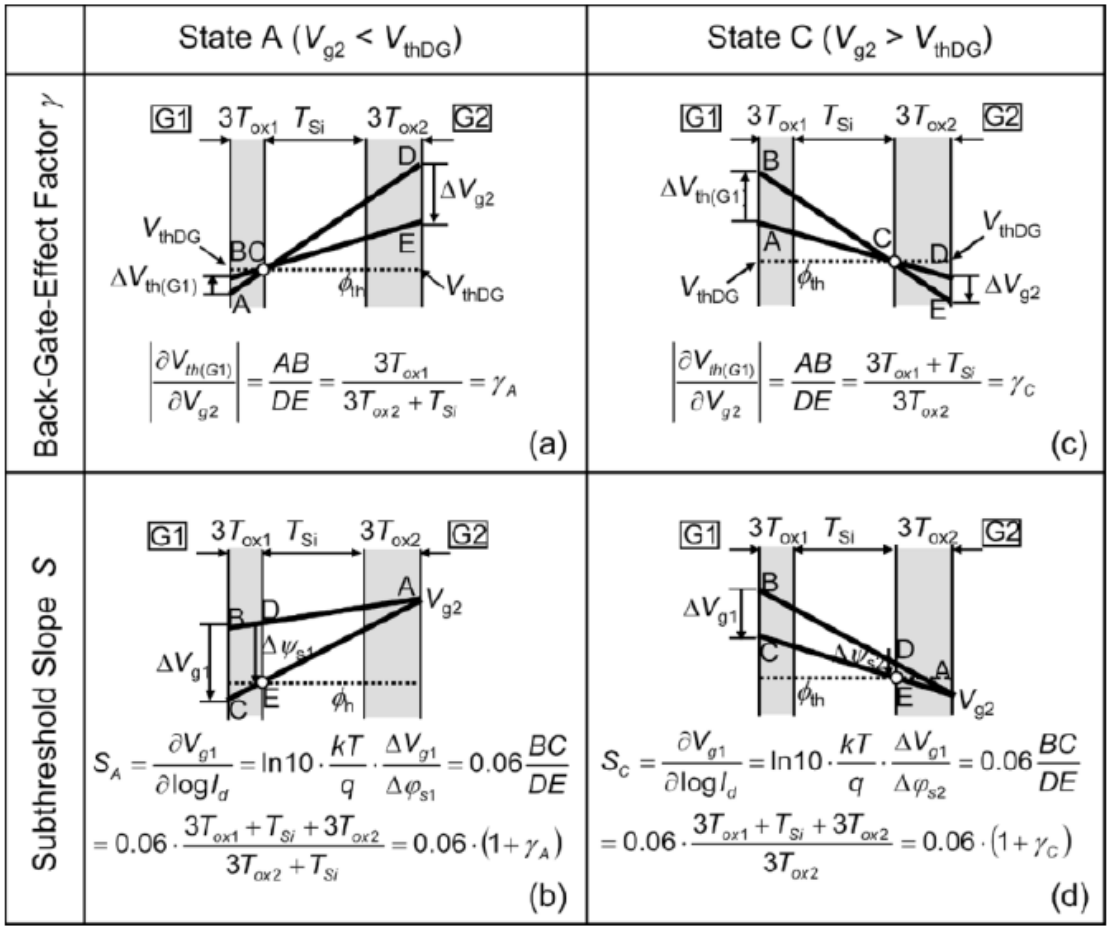


Fig. 4-6 [Ref. 37] Schematic potential distributions of NMOS 4T-XMOSFET across the channel, explaining (a)$dV_{th(G1)}/dV_{g2}$ and (b) S in State A; (c) $dV_{th(G1)}/dV_{g2}$ and (d) S in State C. Thick lines indicate the intrinsic Fermi level E_i. T_{ox1} and T_{ox2} increase according to $\varepsilon_{Si}/\varepsilon_{ox}$=3. Note that S_A and S_C become lower with increasing T_{ox2} , and $dV_{th(G1)}/dV_{g2}$, and S in State C are always larger than those in State A.

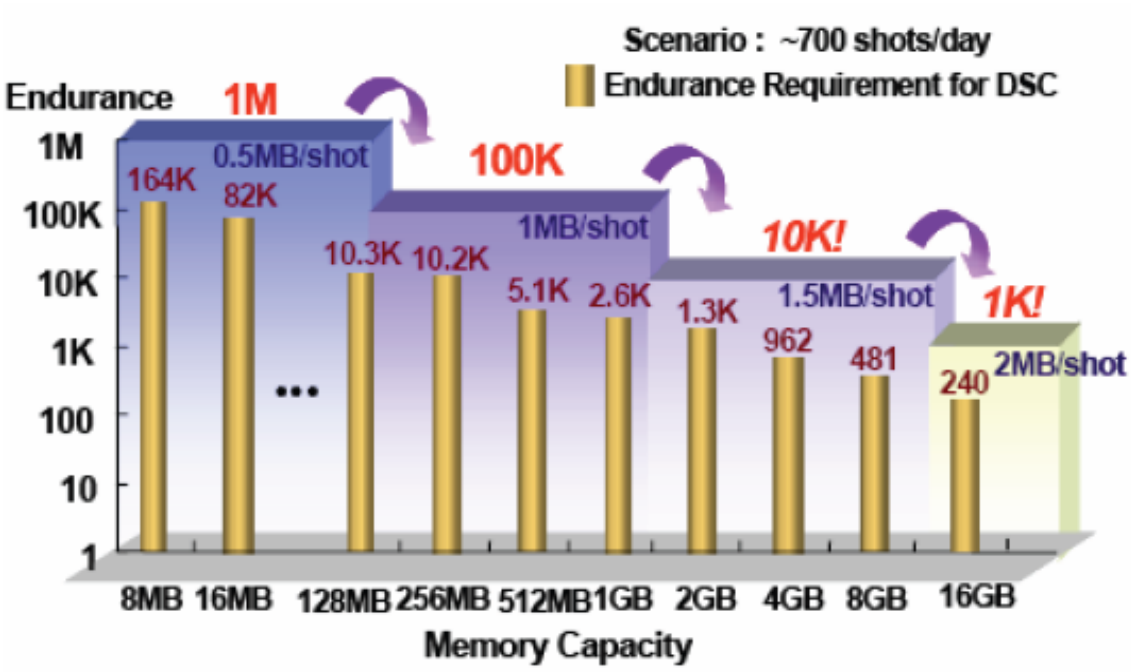
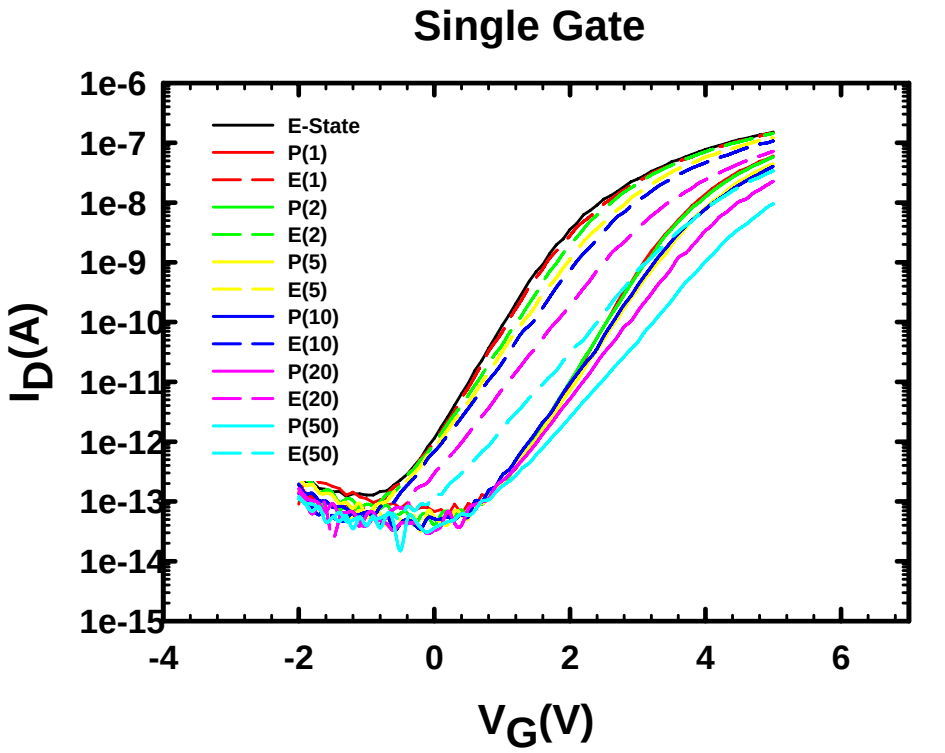
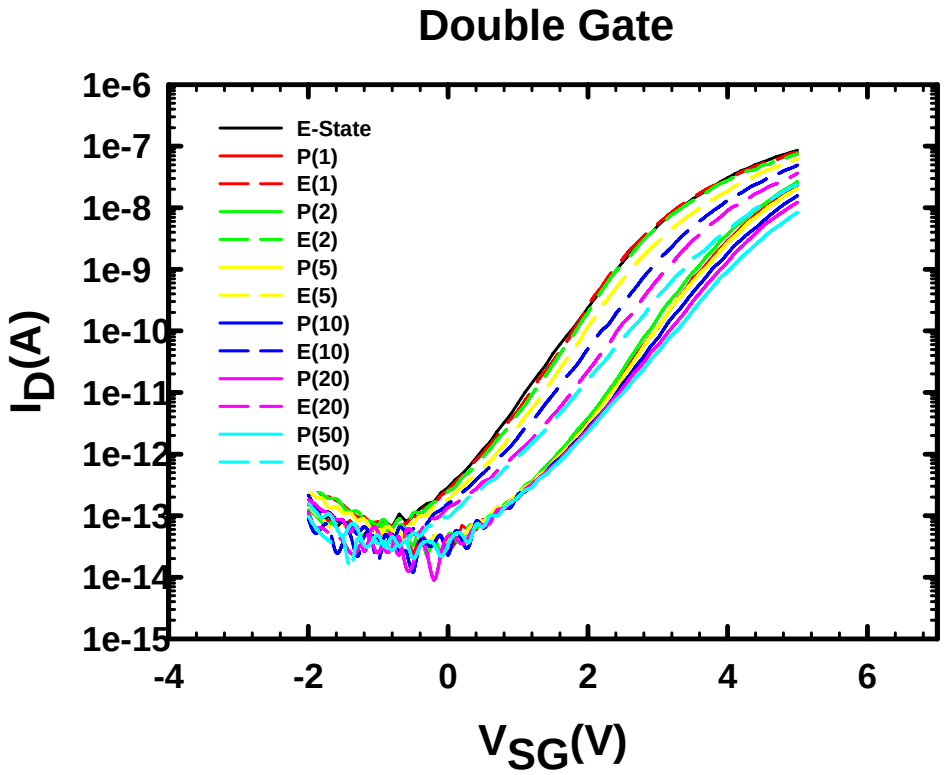


Fig. 4-7 [Ref. 40]Endurance requirement as a function of memory capacity.

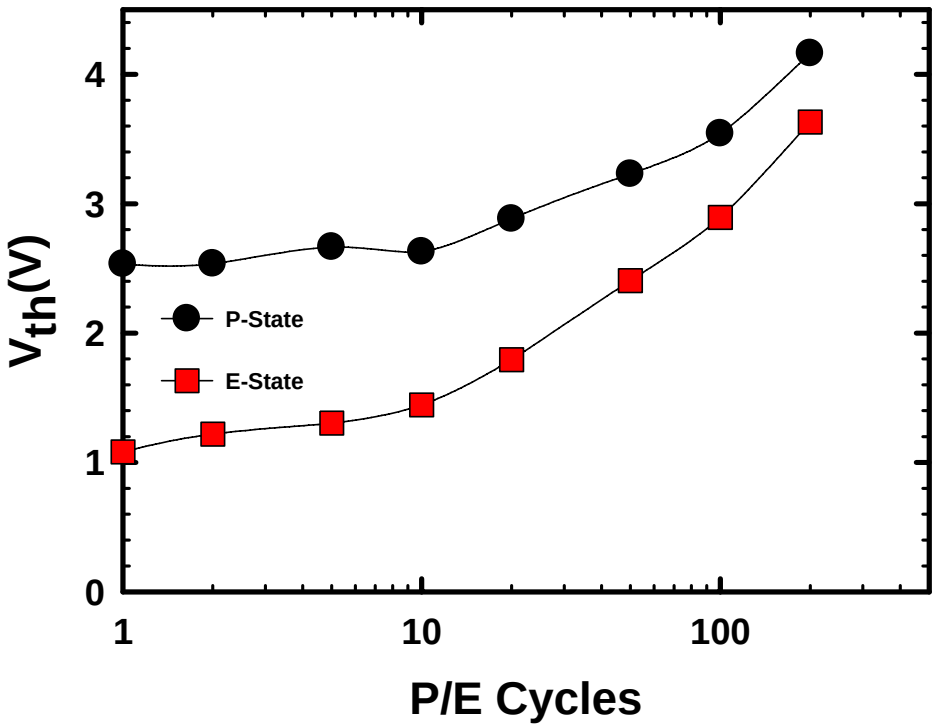


(a)

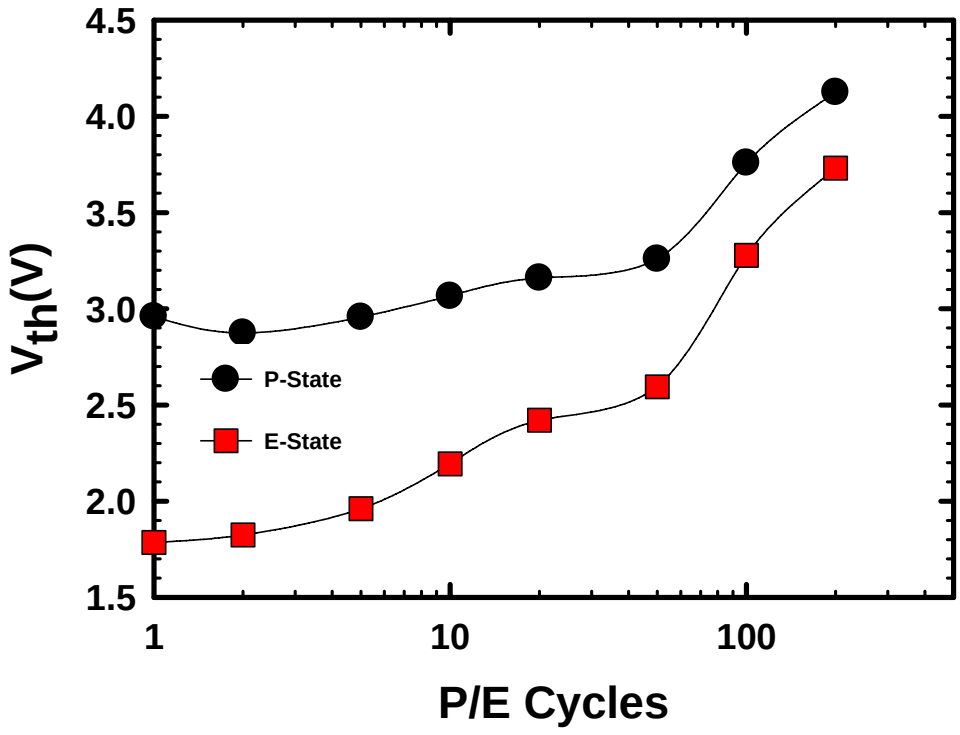


(b)

Fig. 4-8 I_D-V_G curve of (a) single-gated and (b) double-gated structures with increasing erase/program cycles



(a)



(b)

Fig. 4-9 V_{th} evolution of (a) single-gated and (b) double-gated SONOS with increasing program/erase cycles.

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論文題目：

具奈米線通道的薄膜電晶體之氮化矽記憶體元件特性分析

Characterizations of TFT-SONOS with Nanowire Structure