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電子工程學系 電子研究所碩士班

碩 士 論 文

損耗基板模型建立與高頻雜訊模擬
射頻場效電晶體與探針墊架構之研究

The Lossy Substrate Model for RF MOSFET High Frequency Noise Simulation under Various Pad Structures

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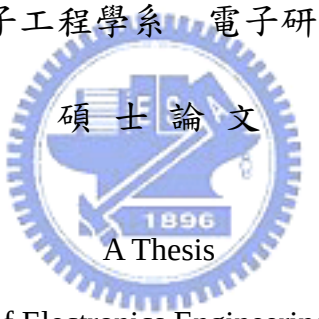

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摘要

在本論文中，首先對金氧半場效電晶體的雜訊理論與原理、各種不同雜訊模型的介紹與雜訊量測的原理及架構做基本的介紹其中包括熱雜訊(高頻)與閃爍雜訊(低頻)。接下來進入本論文的核心部分，利用 130nm 製程研製之射頻互補式金氧半場效電晶體來建立並驗證一個寬頻且可調性的矽基板損耗模型。在第三章，利用開路探針墊的量測結果建立一個可以適用於包括：損耗(lossy)、標準(normal)、小型(small)等三種不同探針墊架構的改良型損耗矽基板模型。在第四章，藉由量測電晶體的電流-電壓特性、轉導與導納參數來校正電晶體的本質特性模型，其中包跨電流-電壓、電容-電壓模型。在第五章，探討不同的探針墊架構其矽基板損耗效應所貢獻的額外雜訊的影響。藉由將探針墊的等效電路搭配經過準確校正的本質元件模型構成的完整電路來進一步驗證改良型矽基板損耗模型。已完成的可調性矽基板模型可以準確的預測損耗型探針墊（lossy pad)在雜訊參數上所表現的異常閘極指叉數(gate finger number)相關性與對頻率的非線性關係。更進一步的，可以有效分析探針墊架構，如金屬堆疊層次與形狀大小，以及連線佈局之影響，得以準確模擬矽基板損耗經由傳輸線與探針墊所貢獻的額外雜訊。最後，改良型損耗矽基板模型提供了一個適當且能有效降低由傳輸線與探針墊所貢獻的額外雜訊的佈局方法。本論文中，小型(small) 探針墊可以很明顯的降低由探針墊所貢獻的外在雜訊，使直接量測到的雜訊特性幾乎接近元件的本質雜訊特性。

A Lossy Substrate Model for RF MOSFET High Frequency Noise Simulation under Various Pad Structures

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ABSTRACT

In this thesis, the basic noise theory, noise models, noise measurement principles and the equipment configuration will be introduced at the first place. Both thermal noises at high frequency and flicker noise dominant at low frequency will be covered. Then a broadband and scalable lossy substrate model is developed and validated for nanoscale RF MOSFET, which were fabricated by 130nm 1.2V CMOS technology. In chapter 3, an enhanced lossy substrate model adopting various pad structures, such as lossy, normal, and small pads was developed based on open pad S-parameters at high frequency up to 40 GHz. In chapter 4, the intrinsic MOSFET model through extensive calibration on I-V and C-V models will be presented. The model calibration was done based on the measured I-V, transconductance, and admittance from Y-parameters. In chapter 5, a detailed discussion on the pad structures effect on RF noise will be provided. The enhanced lossy substrate model is verified by integration with the intrinsic devices model for full circuit model. The scalable lossy substrate model can consistently predict the abnormally strong finger number dependence and nonlinear frequency dependence of noise figure (NF_{min}) revealed by the devices with lossy pads. Furthermore, the scalable model can precisely distribute the substrate loss between the transmission line (TML) and pad with various metal topologies and the resulted excess noises. Finally, the enhanced model provides useful guideline for appropriate layout of pads and TML to effectively reduce the excess noises. The remarkably suppressed noise figure to ideally intrinsic performance can be approached by the small pad in this thesis.

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時間過的很快，兩年的碩士班生涯過去了，雖然我加入高頻奈米元件實驗室的時間不過一年多，不過這一年來，不管是研究上或是做人處世上所學到的都很多，也進步很多，首先我要感謝我的指導老師 郭治群教授，在研究方法與態度上的指導與鞭策，以及不斷的替實驗室尋求研究資源與實驗設備，讓我們能有最好的研究環境，並且時常給予學生專業知識上的傳授與建議，是我的研究能有成果最重要的關鍵之一；也感謝老師不斷的鼓勵我繼續深造，並提供良好之進修機會，讓我可以無後顧之憂的繼續攻讀博士學位。此外特別要感謝林益民學長在我剛進來實驗室的時候，不遺餘力的悉心指導，讓我能再最短的時間內踏入這個陌生的領域。另外要感謝 NDL 的研究員 黃國威博士 在研究設備上的支持，讓我能夠學習到高頻量測，也感謝 RFTC 的工程師們，邱佳松、王生圳等學長在量測過程上的建議與指導，讓我在量測的過程中受益匪淺。也感謝在高頻奈米實驗室的成員們，仁嘉、冠旭、國良，因為你們的陪伴，在做研究的過程中，不至於太苦悶。當然還要感謝陪伴我兩年的室友，書維、政鴻、祥倫、承德，謝謝你們這兩年來的照顧以及陪伴我度過無數次的狂歡與低潮。最後要感謝默默在背後支持我的家人，感謝你們的養育之恩與教導我做人處世的道理，使我能有積極上進的求學態度，讓我可以順利的完成碩士學位。

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Chapter 1

Introduction

The aggressive CMOS device scaling to sub-100-nm regime has driven dramatic reduction of gate delay to approach 10 ps ($1p=10^{-12}$) and the remarkable increase of the unit current gain cut-off frequency to well beyond 100 GHz. Compact MOSFET model with broadband accuracy and scalability is recognized as a critical engine to facilitate the success of RF CMOS circuit design. The increasing demand on low power and low noise for wireless communication escalates the importance of noise characterization and modeling. However, the complicated noise coupling through the lossy pads, lossy substrate, and transmission lines (TML) will contribute excess noises and make the high frequency noise measurement and simulation a dramatic challenge.

1.1 Motivation

It is a difficult task to extract RF CMOS noise accurately while its scalability with device scaling is quite important for low noise RF circuit design. The challenges arise from the strong dependence of RF noise on the parasitic and coupling effect associated with the gate, lossy substrate, TML, and lossy pads. Regarding the lossy pad rendered through pad-to-substrate coupling, the impact is increasing for miniaturized devices and particularly worse for sub-100-nm Si RF CMOS. The extrinsic minimum noise figure (NF_{min}) before de-embedding may be dominated by the lossy substrate , TML, and lossy pad effect. However, a reliable noise de-embedding method to assure accurate extraction of intrinsic noise remains a difficult subject and is particularly challenging for nanoscale devices. A noise correlation matrix method [1] was proposed to deembed these effects but the complicated matrices calculation sometimes suffers fluctuation at very low noise level and poor accuracy in frequency dependence [2-3]. In our previous work, a lossy substrate model was developed to

predict the measured noise and a lossy substrate de-embedding method can be easily performed through circuit simulation for precise extraction of intrinsic noise [4-6]. The accuracy has been proven by sub-100 nm NMOS with various finger numbers and operation under varying frequencies and biases.

Furthermore, a scalable lossy substrate model is desirable to enable prediction for on-chip devices. This demand triggers our motivation of this study on the excess noise coupling from lossy substrate, (TML and pads with various metal topologies. The enhanced lossy substrate model and lossy substrate de-embedding method have been extensively verified and justified by nanoscale devices adopting various pad structures.

1.2 Overview

A broadband and scalable lossy substrate model has been developed and validated for nanoscale RF MOSFETs with different finger numbers and adopting various pad structures such as lossy, normal and small pads.

Chapter 2 gives an introduction to the classification and physical mechanism of noises in MOSFETs. The noise measurement theory and measurement system configuration are also covered.

In chapter 3, we purpose an enhanced lossy substrate pad model to precisely distribute the substrate loss between the TML and pads with various metal topologies and the resulted excess noises.

In chapter 4, the intrinsic MOSFET model with relevant calibration on I-V and C-V models will be presented. The key model parameters in BSIM3 I-V and C-V models will be compared before and after calibration.

In chapter 5, we will describe a full equivalent circuit model, which include the pads,

TML, and intrinsic MOSFET. The high frequency simulation using this full circuit can realized good agreement with measured S- and Y-parameters up to 40GHz. Furthermore, the proposed lossy substrate model is scalable to fit various pad structures. The measured noise parameters (NF_{min}, R_n, and Y_{opt} or Γ_{opt}) corresponding to various pad structures can be accurately simulated up to 18 GHz. This scalable lossy substrate model can consistently predict the abnormally strong finger number dependence and nonlinear frequency response of minimum noise figure (NF_{min}) revealed by the devices with lossy pad.

Chapter 6 will wrap up the summary for this thesis and suggestions for future work.

Appendices A and B provide more detailed explanation of certain contents. Appendix A addresses the Y-factor method for noise figure measurement. Appendix B describes the modified open and short de-embedding method.

Chapter 2

Noise Theory and Noise Measurement Technique

Noise can be defined as a kind of undesired signal for a device, circuit, or system. It is generally caused by the small current and voltage fluctuations generated within the devices themselves or from external coupling paths. Noise represents a lower limit to the electrical signal that can be amplified by a circuit without significant deterioration in signal quality. Also, noise sets an upper limit to the useful gain of an amplifier. It is because that the gain at output stage will be self limited by the amplified noise. In this chapter, various sources of electronic noise are considered, and high frequency noise in MOSFET is of major focus that is dominated by the thermal noise. Noise theory for noise behavior analysis of two-port network will be covered. Noise models available for existing simulation tools like BSIM3 will be addressed. To the end of this chapter, noise measurement with system configuration and calibration methods will be described.

2.1 Noise Sources

The most important sources of noise in electronic devices are shot noise, generation-recombination noise, flicker noise and thermal noise. Shot noise is always associated with a direct-current flow, which generated when carriers in device cross barriers independently and randomly. It is an eminent noise source for diodes and bipolar transistors. For MOSFETs, only DC gate leakage current contributes shot noise. However, gate leakage is normally controlled to be very small. Generation and recombination noise occurs in semiconductors in which traps and recombination centers are always involved. Fluctuation of carrier number due to random trapping and de-trapping process contributes this noise.

2.1.1 Flicker Noise

In the low frequency domain (≦100 KHz), the noise in MOSFETs is dominated by Flicker noise. The physical mechanisms responsible for Flicker noise are generally classified as carrier fluctuation model and mobility fluctuation model. In the following, three popular models in existing literature [7] will be reviewed.

1) Carrier number fluctuation model :

For carrier fluctuation model, the channel noise is originated from the random capture and emission of charge carriers through trapping and detrapping in the interface states residing at Si-SiO_2. The carrier number fluctuation theory has been successful in modeling 1/f noise in n-channel devices. The equation proposed for the carrier fluctuation model is described as follow [8] .

$$\frac{S_{ID}}{I_{DS}^{\ 2}} = \frac{g_m^{\ 2}}{I_D^{\ 2}} \frac{q^2 kT \lambda N_t}{WLC_{ox}^{\ 2} f} \left(1 + \alpha \mu_{eff} C_{ox} \frac{I_D}{g_m} \right)^2 \qquad (2\text{-}1)$$

where N_t is the interface trap density, C_{ox} is the gate oxide capacitance, f is the operating frequency, μ_{eff} is the effective carrier mobility, and α is the scattering parameter.

2) Mobility fluctuation model :

As for mobility fluctuation model, the channel noise is generated due to mobility variation induced channel current fluctuation. Hooge's empirical formula was proposed to account for the mobility fluctuation model. This model, as compared with the carrier fluctuation is more appropriate to simulating the 1/f noise in p-channel devices.

3) Unified 1/f noise model :

The unified model has been proposed to cover both n-channel and p-channel devices, in 1/f noise simulation using a single model. The unified model that can be considered as a

combination of the carrier number fluctuation model and the Hooge mobility fluctuation model. It extends the carrier number fluctuation model to include the mobility fluctuation induced by the fluctuating oxide trap charges through coulomb scattering. The carrier number fluctuation and the mobility fluctuation are correlated because not only the charge carriers in the channel, but also their mobility fluctuated. The basic assumption is that trapping and detrapping of charge carriers through the oxide traps constitutes a common origin for both models. The unified model has been adopted in some public-domain compact MOSFET models, such as BSIM3 and BSIM4.

Flicker noise is also named as 1/f noise due to its noise power spectral density given by (2-2) in which a frequency dependence with slope n approaching unity is achieved

$$S_I(f) = K \cdot \frac{I^m}{f^n} \tag{2-2}$$

Flicker noise is important to be considered in RF circuit design such as mixers, oscillators, and frequency dividers that are used to up convert low frequency signals to higher frequency, and may deteriorate the phase noise and signal-to-noise ratio due to simultaneous up conversion of low frequency noise. As for the operation in very high frequencies, Flicker noise generally becomes negligible and thermal noise will emerge as a major concern for RF circuit operation.

2.1.2 Thermal Noise

For MOSFET operating in high frequency domain, thermal noise becomes the dominant noise source. It is due to the random thermal motion of the electrons and the current fluctuation caused by collision of lattice. Thermal motion of carriers is ubiquitous in any electronic components as long as its temperature is not absolutely zero. Because of the thermal nature, thermal noise power turns out to be exactly proportional to the absolute temperature. Starting from the quantum theory of a harmonic oscillator, noise power of

thermal noise is given by [9]

$$P_{av} = [\frac{1}{2}hf + \frac{hf}{e^{(hf/kT)} - 1}] \cdot \Delta f \tag{2-3}$$

where h is Planck constant, k is Boltzmann constant, f is the operating frequency, and Δf is the frequency interval. For *hf/kT* << 1 (holds for general case) and based on the noisy resistor model shown in Fig. 2.1. the mean-square open circuit noise voltage and noise current can be obtained.

$$P_{av} = kT\Delta f = \frac{\overline{v_n^2}}{4R} \tag{2-4}$$

$$\overline{v_n^2} = 4kTR\Delta f \tag{2-5}$$

$$\overline{i_n^2} = \frac{4kT\Delta f}{R} = 4kTG\Delta f \tag{2-6}$$

Herein, every component with electrical resistivity can be considered as a resistor. With known resistance value or equivalent resistance, noise voltage or noise current can be calculated.

2.1.3 Thermal Noise in MOSFETs

In MOSFETs, the thermal noise components include channel noise (or called drain current noise), induced gate noise, and thermal noise due to terminal parasitic resistances (R_g, R_d, and R_s).

For thermal noise, the dominant contribution comes from the channel thermal noise. The most broadly accepted noise model for MOSFETs is the van der Zeil model [10]. For a MOSFET under operation, the conducting channel behaves like a voltage-controlled resistor. This resistor contributes thermal noise at the drain terminal. The power spectral density can be derived from the drain current expression. Refer to Fig. 2.2, taking velocity saturation into

consideration, drain current at a certain position along channel direction is given by [9]

$$I_D(x) = W_{eff} \cdot Q_I(x) \cdot \nu(x) = \left(\mu_{eff} \cdot W_{eff} \cdot Q_I(x) - \frac{I_D(x)}{E_C} \right) \cdot \frac{dV}{dx} \tag{2-7}$$

Integrating this current over the effective channel L_{eff}, drain current can be obtained

$$I_D = \frac{1}{L_{eff}} \int_{V_S}^{V_D} \left(\mu_{eff} \cdot W_{eff} \cdot Q_I(V) - \frac{I_D}{E_C} \right) \cdot dV \tag{2-8}$$

The mean square values of a current fluctuation $\Delta i_d(t)$ caused by $\Delta v(t)$ in a unit length segment is

$$\overline{(\Delta i_d)^2} = \frac{1}{L_{eff}^2} \left(\mu_{eff} \cdot W_{eff} \cdot Q_I(V) - \frac{I_D}{E_C} \right)^2 \cdot \overline{(\Delta v)^2} \tag{2-9}$$

where $\overline{(\Delta \nu)^2}$ is

$$\overline{(\Delta \nu)^2} = \frac{4kT_e(x_i) \cdot \Delta x}{\left(\mu_{eff} \cdot W_{eff} \cdot Q_I(x_i) - \frac{I_D(x_i)}{E_C} \right)} \Delta f \tag{2-10}$$

Finally, power spectral density of the noise current generated by the channel resistance includes velocity saturation effect and hot-electron effects is given

$$S_{Id} = \frac{\overline{(i_d)^2}}{\Delta f} = \frac{4k}{L_{eff}^2 \cdot I_D} \int_{V_S}^{V_D} T_e(x) \left(\mu_{eff} \cdot W_{eff} \cdot Q_I(V) - \frac{I_D}{E_C} \right) \cdot dV \tag{2-11}$$

where T_e is the effective electron temperature in which hot-electron effect is considered. This is a general expression for the thermal noise in a channel. For simplicity it can be written as

$$S_{Id} = \frac{\overline{(i_d)^2}}{\Delta f} = 4kT\gamma g_{d0} \tag{2-12}$$

where g_{d0} is the drain transconductance at V_{DS} equal to zero. For long channel devices, γ is close to unity in its triode region and decreases to about 2/3 when in saturation (i.e. $\frac{2}{3} \le \gamma \le 1$). In long channel case, g_{d0} is equal to the gate transconductance g_m in saturation region, which leads to a familiar result

$$S_{Id}=\frac{\overline{(i_d)^2}}{\Delta f}=\frac{8}{3}kTg_{d0}=\frac{8}{3}kTg_m \tag{2-13}$$

Due to the carrier heating by the large electric fields in short channel devices, γ may become larger than 2 or even larger.

Besides the channel current noise, the induced gate noise has gained increasing attention. As the operation frequency increases, contribution of this noise cannot be neglected. Noise model including this terms, thus, become essential. Induced gate noise is, as implied by the name, the noise induced by capacitive coupling from channel region to gate terminal due to the fluctuating potential. This noise can be expressed as [11]

$$S_{Ig}=\frac{\overline{(i_g)^2}}{\Delta f}=4kT\gamma g_g \tag{2-14}$$

where g_g is given by

$$g_g=\frac{\omega^2 C_{gs}^2}{5g_{d0}} \tag{2-15}$$

Because the channel noise and induced gate noise have a common origin, they do have correlation. The correlation coefficient is usually expressed as

$$c=\frac{\overline{i_g i_d^*}}{\sqrt{i_g^2}\sqrt{i_d^2}} \tag{2-16}$$

As for noise contributed from parasitic resistances, following (2-6), three noise terms corresponding to the gate, drain, and source are given by

$$S_{I,Rg} = \frac{4kT}{R_g} \; ; \; S_{I,Rd} = \frac{4kT}{R_d} \; ; \; S_{I,Rs} = \frac{4kT}{R_s} \tag{2-17}$$

Among them, due to the larger sheet resistance of poly-Si, gate resistance (R_g) is typically much larger than drain and source resistances (R_d and R_s). Therefore, R_g is an important noise contributor, which can greatly affect the noise figure of the device. To consider the gate resistance (R_g) impacts on channel thermal noise separately, an additional drain current noise, which is contributed from gate resistance, was shown as follows

$$\Delta S_{Id} = 4kTR_g g_m^{\,2} \tag{2-18}$$

The gate resistance also gives rise to gate current noise as shown below

$$\Delta S_{IG} = 4kTR_g \omega^2 C_{gg}^{\,2} \tag{2-19}$$

The gate resistance will turn out to be a major contributor to the gate current noise in short channel device. The contributions of the gate resistance to drain current and gate current noise are correlated. The correlation coefficient is purely imaginary, i.e. c=1.0 j.

Multi-finger gate structure is widely used in RF MOSFET design to reduce R_g. In addition to high frequency noise, multiple high frequency performance parameters are related to R_g, and the maximum oscillation frequency (f_{max}) is one relevant example. Multi-finger gate structure can improve mentioned high frequency performance but may suffer the penalty of larger parasitic capacitance.

2.2 Two-Port Noise Theory

2.2.1 Noise Figure

As mentioned above, the overall noise in a device is generally contributed from multiple

sources. An accurate and reliable method to measure noise is indispensable and sometimes challenging. For device characterization and circuit performance evaluation, noise figure or noise factor is the most popular expression. Based on the two-port noisy network model and definition of noise figure (or noise factor), four noise parameters can be derived as follows.

Noise factor is defined as the signal-to-noise power ratio at the input port divided by signal-to-noise power ratio at the output port. It can be given by (2-20)

$$F \equiv \frac{S_i/N_i}{S_o/N_o} \tag{2-20}$$

Where S_i and S_o are input and output signals and N_i and N_o are input and output noise power. From this definition, we can understand that noise factor of a network represents the degradation of signal-to-noise ratio as a signal goes through this network. Considering a network with gain G and noise N_a, the noise factor can be express as

$$F \equiv \frac{S_i/N_i}{S_o/N_o} = \frac{S_i/N_i}{GS_i/(N_a+GN_i)} = \frac{N_a+GN_i}{GN_i} \tag{2-21}$$

where N_a and G are the noise power and gain of the network. From above expression in (2-21), noise factor can be defined as the ratio of total noise power at the output to the output noise power, which is due to the input noise. In short, the larger noise factor means the noisier for the network. In (2-20), it shows the value of a noise factor is affected by the input noise power, which is generally contributed from the thermal noise of the source, kTΔf. This means that the noise factor depends on the source temperature. For IEEE standard regulation, 290K was specified as a standard temperature, because it makes the value of kT close to around 4×10^{-21} Joule. Generally, we use this measure in the unit of dB, defined as noise figure

$$NF = 10 \log F \tag{2-22}$$

2.2.2 Noise Parameters

The noise factor (or noise figure) is primarily affected by two factors — the source impendence at the input port of a two port network and the noise sources within the network itself. The noise factor of a two-port network with various source impedance was derived and given by the expression [12]

$$F = F_{min} + \frac{R_n \left| Y_s - Y_{opt} \right|^2}{G_s} \tag{2-23}$$

where

$$Y_s = G_s + j\, B_s \tag{2-24}$$

$$Y_{opt} = G_{opt} + j\, B_{opt} \tag{2-25}$$

herein, Y_s is the source admittance, G_s is the real part of Y_s, Y_{opt} is the optimum source admittance resulting in the minimum noise figure (NF_{min}), and F_{min} is the minimum noise factor achieved in the network when the source admittance Y_s is equal to Y_{opt}. R_n is defined as the equivalent noise resistance, which determines the sensitivity of the noise factor with respect to the deviation of Y_s from Y_{opt}. Replacing the source admittance with its corresponding reflection coefficient at specific characterization impedance Z_0 (50Ω), another common form of noise factor is obtained

$$F = F_{min} + \frac{4R_n}{Z_0} \frac{\left| \Gamma_s - \Gamma_{opt} \right|^2}{(1 - \left| \Gamma_s \right|^2) \left| 1 + \Gamma_{opt} \right|^2} \tag{2-26}$$

$$Y_{opt} = \frac{1}{Z_0} \frac{1 - \Gamma_{opt}}{1 + \Gamma_{opt}} \tag{2-27}$$

$$Y_s = \frac{1}{Z_0}\frac{1-\Gamma_s}{1+\Gamma_s} \tag{2-28}$$

It is a general practice in high frequency device and circuit design to get a smaller noise factor while keep sufficient gain by varying Y_s. The so-called noise parameters are the four parameters NF_{min}, R_n, $Re(\Gamma_{opt})$, and $Im(\Gamma_{opt})$. These parameters are determined purely by the intrinsic noise source of the network, they are unique under a certain operation frequency and bias.

2.3 Thermal Noise Model

There are two channel thermal noise models supported by BSIM3v3.2.2. One is SPICE2 model and the other is BSIM3v3 model. The model selection is accessed by the flag given the name as *noiMod* in BSIM3v3.2.2 [13].

noimod flag	Flicker noise model	Thermal noise model
1	SPICE2	SPICE2
2	BSIM3v3	BSIM3v3
3	BSIM3v3	SPICE2
4	SPICE2	BSIM3v3

Through noise model selection by specifying *noimod*, flicker noise and thermal noise can be calculated using SPICE2 or BSIM3v3 model. Another noise model supported by many simulators is the HSPICE model. In Agilent-ADS, BSIM3 model selected by *noimod* is valid when *NLEV* < 1 or HSPICE model will be used by setting *NLEV* values (*NLEV*=1, 2 or 3). In the mentioned models, two important physical effects were not considered - the velocity saturation effect and the hot-electron effect, and these effects generally become very significant in sub-100nm modern transistors.

SPICE2 Model

For *noimod* = 1 or 3, thermal noise is calculated according to [14]

$$S_{Id} = \frac{8kT}{3}(g_m + g_{ds} + g_{mbs}) \tag{2-29}$$

This model is the modification of old HPSICE model shown below as with *NLEV* < 3, this equation valid only in the saturation region, and is not suitable in the linear region.

BSIM3v3 Model

If *noimod* = 2 or 4, thermal noise power spectral density is calculated by [15]

$$S_{Id} = \frac{4kT\mu_{eff}}{L_{eff}^2}\left|Q_{inv}\right| \tag{2-30}$$

where Q_{inv} is the channel inversion charge calculated according to the capacitance models (*capMod*=0, 1, 2, or 3). This model is only accuracy in long-channel devices because without taking the velocity saturation effect into consideration. This model is not suitable for the noise modeling of modern transistors.

HSPICE Model

The HSPICE noise model has different equations to calculate the flicker and thermal noises. Equation selection is through a parameter, *NLEV*. For *NLEV* smaller than 3, different flicker noise model was used but the same thermal noise equation was implemented which is given by [16]

$$S_{Id} = \frac{8kT \cdot g_m}{3} \tag{2-31}$$

which is an old model and is lack of accuracy for modern devices.

If *NLEV* is set to 3, the noise equation is then given by [14]

$$S_{Id} = \frac{8kT}{3} \cdot \beta \cdot (V_{GS} - V_T) \cdot \frac{1 + a + a^2}{1 + a} \cdot Gdsnoi \tag{2-32}$$

where

$$\beta = \frac{W_{eff}}{L_{eff}} \cdot \mu_{eff} \cdot C_{ox} \tag{2-33}$$

$$\begin{aligned} a &= 1 - \frac{V_{DS}}{V_{DSAT}}, \quad \text{Linear region} \\ &= 0, \quad \text{Saturation region} \end{aligned} \tag{2-34}$$

and *Gdsnoi* is the thermal noise coefficient with default value equal to 1.

Models mentioned above are integrated into various commercial simulators. Many other models have been proposed to consider velocity saturation effect, hot-electron effect or both [17, 18]. But they are not yet well accepted and verified. Noise simulation result comparison of different models was done in [19]. In this thesis, HSPICE model with *NLEV* set to 3 was used.

BSIM4 Model

There are two channel thermal noise model in BSIM4. One is a charge based model similar to that used in BSIM3v3.2 and the other is called the holistic model. These two model can be selected by setting the parameter *tnoiMod* [13]. The schematic for BSIM4 channel thermal noise model is shown in Fig. 2.3.

If *tnoiMod* =0 (charge based model)

The noise current is given by

$$S_{Id} = \frac{4kT\Delta f}{R_{ds}(V) + \frac{L_{eff}^2}{\mu_{eff}\left|Q_{inv}\right|}} .NTNOI \tag{2-35}$$

Where Rds(V) is the bias-dependent LDD source/drain resistance, and the parameter *NTNOI* is introduced to improve accuracy for fitting to short-channel devices.

If *tnoiMod* =1 (holistic model)

In this thermal noise model, all the short-channel effects and velocity saturation effect incorporated in the I-V model are automatically included and it explain the name given by "holistic" noise model. In this model, the amplification of the channel thermal noise through G_m and G_{mbs} as well as the induced-gate noise with partial correlation to the channel thermal noise are all captured in the new noise partition model (Fig .2.3). The noise voltage source partitioned to the source side is given by

$$\overline{v_d^{\,2}} = 4kT\theta_{tnoi}{}^2 \frac{V_{dseff}\Delta f}{I_{ds}} \tag{2-36}$$

and the noise current source put in the channel region with gate and body amplification is expressed as

$$\overline{i_d^{\,2}} = 4kT\frac{V_{dseff}\Delta f}{I_{ds}}[G_{ds} + \beta_{tnoi}.(G_m + G_{mbs})]^2 - \overline{v_d^{\,2}}.(G_m + G_{ds} + G_{mbs})^2 \tag{2-37}$$

where

$$\theta_{tnoi} = RNOIB[1 + TNOIB.L_{eff}.(\frac{V_{gsteff}}{E_{sat}L_{eff}})^2] \tag{2-38}$$

and

$$\beta_{tnoi} = RNOIA[1 + TNOIA.L_{eff}.(\frac{V_{gsteff}}{E_{sat}L_{eff}})^2] \tag{2-39}$$

where *RNOIB* and *RNOIA* are model parameters with default values 0.37 and 0.577 respectively. In the end of this thesis for future work, 90m RF-CMOS technology with BSIM4 model will be adopted and different noise models can be specified by setting *tnoiMod*. RF-CMOS at 90nm node and beyond will build the technology platform to support our future research work.

2.4 Flicker Noise Model

BSIM-3 Model [13]

There are two flicker noise models available for selection in BSIM-3. One is SPICE2 flicker noise model and the other is BSIM-3 flicker noise model. The flicker noise model parameters were shown in the following table.

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit
Noia	noia	Noise parameter A	(NMOS) 1e20 (PMOS) 9.9e18	none
Noib	noib	Noise parameter B	(NMOS) 5e4 (PMOS) 2.4e3	none
Noic	noic	Noise parameter C	(NMOS) -1.4e-12 (PMOS) 1.4e-12	none
Em	em	Saturation field	4.1e7	V/m
Af	af	Flick noise exponent	1	none
Ef	ef	Flicker noise frequency exponent	1	none
Kf	kf	Flicker noise coefficient	0	none

1) SPICE2 model:

$$S_{Id} = \frac{K_f I_{DS}^{\ af}}{C_{ox} L_{eff}^{\ 2} f^{ef}} \tag{2-40}$$

where f is the frequency, C_{ox} is the gate oxide capacitance. L_{eff} is the effective channel length.

2) BSIM3 model:

If $|V_{gs}| > |V_{th}| + 0.1$ (V_{gs} and V_{th} are positive for nMOS but negative for pMOS)

$$S_{Id} = \frac{q^2 kT \mu_{eff} I_{ds}}{C_{ox} L_{eff}^{\ 2} f^{ef} .10^8} \left[Noia.\log\left[\frac{N_0 + 2x10^{14}}{N_1 + 2x10^{14}}\right] + Noib.(N_o - N_1) + \frac{Noic}{2}(N_o^{\ 2} - N_1^{\ 2}) \right]$$
$$+ \frac{V_{tm} I_{ds} \Delta L_{clm}}{W_{eff} L_{eff}^{\ 2} f^{ef} .10^8} . \frac{Noia + Noib.N_1 + Noic.N_1^{\ 2}}{(N_1 + 2x10^{14})^2} \tag{2-41}$$

where V_{tm} is the thermal voltage, μ_{eff} is the effective mobility at the given bias condition. L_{eff} and W_{eff} are the effective channel length and width, respectively. N_o is the charge density at the source side given by

$$N_0 = \frac{C_{ox}(V_{gs} - V_{th})}{q} \tag{2-42}$$

The parameter N_1 is the charge density at the drain end given by

$$N_1 = \frac{C_{ox}(V_{gs} - V_{th} - \min(V_{ds}, V_{dsat}))}{q} \tag{2-43}$$

ΔLclm is the channel length reduction due to channel length modulation and calculated by

$$\Delta L_{clm} = \begin{cases} L_{itl} \cdot \log\left[\dfrac{V_{ds} - V_{dsat} + E_m}{\dfrac{L_{itl}}{E_{sat}}}\right] (for V_{ds} > V_{dsat}) \\ 0 (otherwise) \end{cases}$$
$$E_{sat} = \frac{2v_{sat}}{\mu_{eff}}, L_{itl} = \sqrt{3X_j T_{ox}} \tag{2-44}$$

Otherwise ($|V_{gs}| \leqq |V_{th}| + 0.1$)

$$S_{Id} = \frac{S_{limit} x S_{wi}}{S_{limit} + S_{wi}} \tag{2-45}$$

where S_{limit} is the flicker noise calculated at $|V_{gs}| = |V_{th}| + 0.1$ and S_{wi} is given by

$$S_{wi} = \frac{Noia.V_{tm}.I_{ds}^{\ 2}}{W_{eff}L_{eff}.f^{ef}.4x10^{36}} \tag{2-46}$$

BSIM-4 Model [13]

There are two flicker noise models in BSIM-4. The parameter *fnoimod* is available to

specify which model to use. When *fnoimod* is set to 0, a simple flicker noise model, i.e. the SPICE2 model is invoked. As *fnoimod* =1 is specified, a unified physical flicker noise model is used. Basically, these two models follow those implemented in BSIM3v3, but there exist significant improvement on the unified model. For instance, the smooth transition over all bias regions is achieved and the bulk charge effect is considered in the improved model.

For fnoiMod=0 (a simple model)

$$S_{Id} = \frac{KF.I_{DS}^{AF}}{C_{oxe}L_{eff}^{2}f^{EF}} \tag{2-47}$$

where f is device operating frequency. This model is the same as SPICE2 flicker noise model in BSIM3. Note that C_{oxe} used in BSIM4 is different from C_{ox} used in BSIM3. This change accounts for the fact that BSIM4 adopts the electrical oxide thickness for most of capacitance calculations, but BSIM3 does not distinguish between the physical and the electrical oxide thicknesses.

For fnoiMod=1 (a unified model)

This model involve both carrier number fluctuation and mobility fluctuation models, and take into account of the bulk charge effect. In the inversion region , the noise density is expressed as

$$S_{Id} = \frac{q^2 kT\mu_{eff}I_{ds}}{C_{oxe}(L_{eff}-2.LINTNOI)^2 A_{bulk}f^{ef}.10^{10}}\left[NOIA.\log\left(\frac{N_0+N^*}{N_1+N^*}\right)+NOIB.(N_o-N_1)+\frac{NOIC}{2}(N_o^{\,2}-N_1^{\,2})\right]$$
$$+\frac{kTV_{tm}I_{ds}^{\,2}\Delta L_{clm}}{W_{eff}(L_{eff}-2.LINTNOI)^2 f^{ef}.10^{8}}\cdot\frac{NOIA+NOIB.N_1+NOIC.N_1^{\,2}}{(N_1+N^*)^2} \tag{2-48}$$

where V_{tm} is the thermal voltage, μ_{eff} is the effective mobility at the given bias condition, and L_{eff} and W_{eff} are the effective channel length and width, respectively. N_o is the charge density at the source side given by

$$N_0 = \frac{C_{ox} V_{gsteff}}{q} \tag{2-49}$$

The parameter N_1 is the charge density at the drain end given by

$$N_1 = \frac{C_{oxe} V_{gsteff} . (1 - \frac{A_{bulk} V_{dseff}}{V_{gsteff} + 2v_t})}{q} \tag{2-50}$$

N* is given by

$$N^* = \frac{kT.(C_{oxe} + C_d + CIT)}{q^2} \tag{2-51}$$

where CIT is a model parameter from DC I-V model and C_d is the depletion capacitance.

In the subthreshold region, the noise power spectral density (PSD) is written as

$$S_{id,subVt} = \frac{NOIA.kT.I_{ds}^{\ 2}}{W_{eff} L_{eff} . f^{EF} . N^* . 10^{10}} \tag{2-52}$$

The total PSD of flicker noise is

$$S_{Id} = \frac{S_{id,inv} x S_{id,subVt}}{S_{id,inv} + S_{id,subVt}} \tag{2-53}$$

2.5 High Frequency Noise Measurement

In this work, high frequency noise measurement was supported by Radio Frequency Technology Center of National Nano Device Laboratory (NDL RFTC). On-wafer noise characterization was conducted using NP5 series noise parameter measurement system. The

measurement system is introduced as follows.

2.5.1 System Configuration [20]

The configuration of a high frequency noise measurement system ATN-NP5B is shown with a simple block diagram in Fig. 2.4. This system basically consists of three sub-systems an ATN NP5B wafer probe test set, a vector network analyzer (VNA) - HP8510C, and a noise figure meter (NFA) - HP8970B. The NP5B system works as a switch for switching between the HP8510C for s-parameters measurement and the HP8970B for noise measurement in a two port network. The NP5B is comprised of a main controller unit, which drives the externally connected mismatch noise source (MNS) and remote receiver module (RRM). The MNS is a solid state electronic tuner with a built-in bias-T and RF switches, which serve to switch the connection between the DUT (device under test) to VNA and the noise source to the DUT. The DUT's output is connected through RRM unit to either a VNA (8510C) or a NFA (HP8970B). Note that the RRM contains a bias-T, a low noise amplifier (LNA), and switches. The LNA adopted in RRM can drive the second stage to a lower noise and lower system noise figure. In this way, he noise measurement accuracy can be improved. Noise source is the noise power supply connected at port 1 defined by ENR (excess noise ratio) value, which contains a diode ~~on~~ under reverse bias. It can be operated at a hot or a cold state. When operating at a cold state, the diode was free from the external bias. At this time the noise is the room temperature noise and defined by a noise temperature T_c. When working at a hot state, the diode is subject to a reverse bias and contributes a higher noise defined by a noise temperature T_h. The ENR of noise source can be calculated as

$$ENR(dB) = 10\log(\frac{T_h - T_c}{T_0}), T_0 = 290K \quad (2\text{-}54)$$

2.5.2 System Calibration and Measurement [21]

As high frequency characterization was conducted on the devices (DUT), the applied signals with short wavelength are comparable to the probe, cables, adapters, bonding wires, and DUT. Thus, losses caused by the mentioned connecting elements will seriously degrade the measurement accuracy and resolution, and the impact becomes particularly critical with increasing frequency.. On the other hand, a measurement system has its own system error. Consequently, a system calibration should be performed to take those losses into consideration. The standard procedure is to calibrate the system errors and then shift the measurement signal reference plane to the DUT plane. The validity and accuracy of the calibration results depend on the calibration method used.

The calibration procedure is conducted through the following six steps. Following the system calibration, the RF probe must be probed on short, open, load, and thru dummy pad; in other calibration steps, the RF probe is probed on the same thru dummy pad.

1. Short, open, and load (SOL) calibration : Connected with a short, open, load in the place of the noise source on MNS to perform S_{22} measurement. This raw data will be combined with the data achieved through full two-port calibration to determine the s-parameters of the MNS.

2. Noise source calibration : First, connect the noise source to the MNS, which have established a reference plane from the SOL calibration. Then, make S-parameters measurement with the noise source at hot/cold to calculated the corresponding reflection coefficients and noise power for the noise source. This noise power measurement is used later to establish the gain and noise figure for the receiver.

3. S-parameters calibration : This step is a standard s-parameters calibration. There are many calibration methods like short-open-load-thru (SOLT), line-reflect-match (LRM), thru-reflect-line (TRL). In this thesis, we used the SOLT calibration method. This calibration

step was conducted in order to shift the reference plane to the DUT plane, and later for the noise figure calculation.

4. Thru-delay calibration : Once the S-parameter calibration is finished, then system will check the thru delay automatically. For our currently measurement, the thru delay approximates 1ps.

5. RRM and MNS calibration : For MNS calibration, S_{22} measurement was carried out by changing the impedance states of the solid state tuner to calibrate the source reflection coefficients. These impedances are then referred to the S-parameters port 1 reference plan. For RRM calibration, S_{11} measurement was performed to determinate the input reflection coefficient of the receiver. This information is referred to the S-parameter port 2 reference plan.

6: System noise parameter calibration : In the last step, the noise power with varied source impedance is measured and the receiver noise parameters are stored at the port 2 reference plan.

After calibration, noise measurement reference plane is then established. Before noise measurement, we can measure the noise figure on the thru pad to verify the calibration result. Theoretically, the thru pad didn't contribute the noise. Therefore, the noise figure we measured must be less than 0.1dB. In the beginning of noise measurement, S-parameters measurement at the DUT reference plane should be done first. These S-parameters are necessary information for calculating noise parameters in next step. In the following, the electronic tuner (MNS) will vary the impedance to change the source reflection coefficient (Γ_s) around the Smith chart. Then the output noise power of DUT via the receiver as a function of Γ_s was measured. As a result, each individual Γ_s and its corresponding noise power construct a set of equations. Basically, Only four input states are needed for noise parameters characterization because the noise parameters calculation equation has only four unknown

parameters. In practice, in order to reduce the random system error, we usually measured more than four states, in our experience, we generally collect data from 24 or 32 states. Then a proper fitting procedure was performed to extract these four parameters. Finally, the four noise parameters: NF_{min}, R_n, Re(Γopt) or Re(Yopt) and Im (Γopt) or Im(Yopt) are obtained.

In the measurement process, the overall noise figure was calculated by Y-factor method technique. The overall noise figure is then under a noise figure correction step to determine the noise figure of the DUT. Details of Y-factor method and noise figure correction are included in Appendix A.

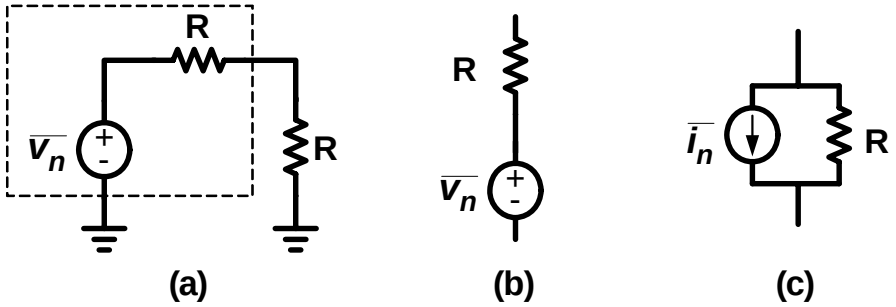


Fig. 2.1 (a) Equivalent network for computing thermal noise of a resistor. (b)(c) Thermal noise model for a resistor.

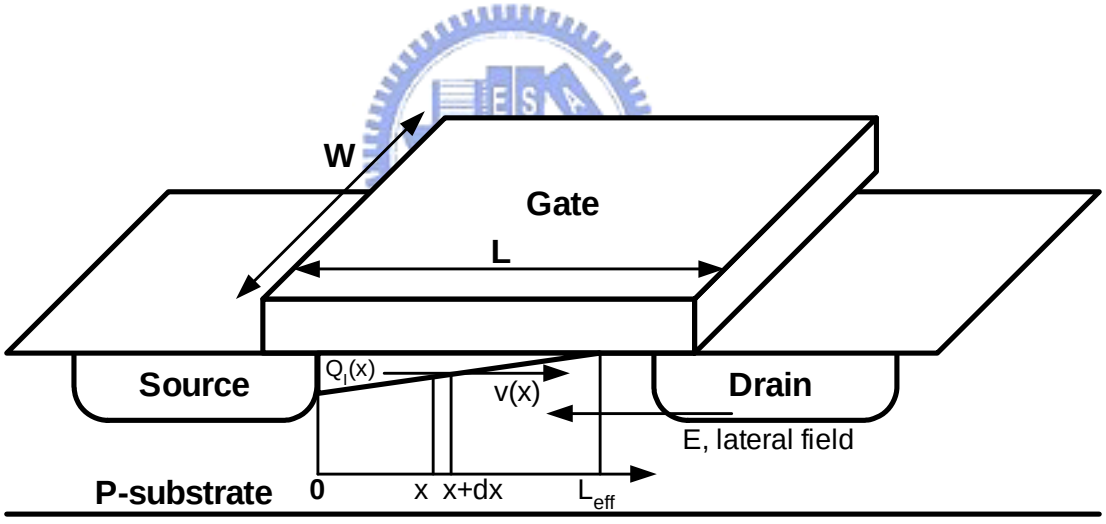
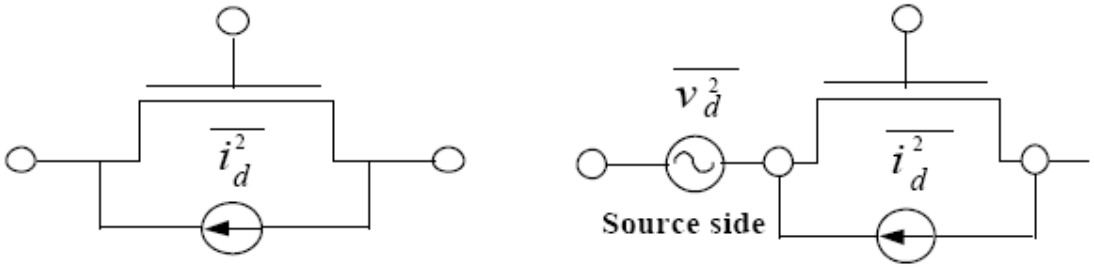
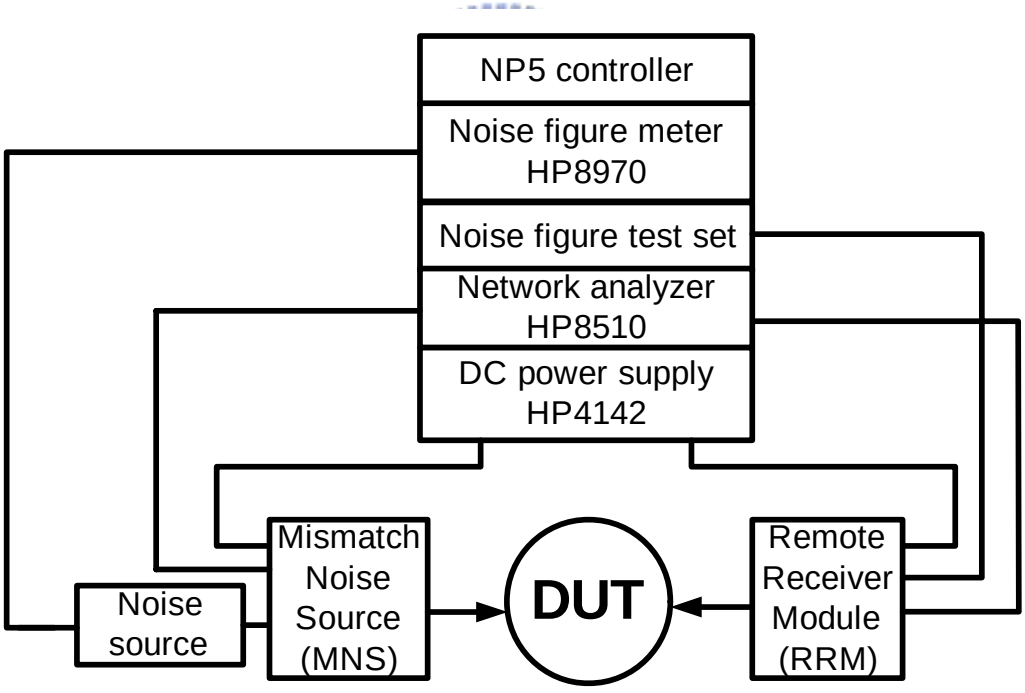


Fig. 2.2 Schematic diagram of a MOSFET operated in saturation condition.



(a) (b)

Fig .2.3 Schematic for BSIM4 channel thermal noise modeling (a) tnoiMod=0 (b) tnoiMod=1



MNS: A solid state electronic tuner with embedded bias-T and switching circuit.
RRM: A low noise amplifier with embedded bias-T and switching circuit.

Fig. 2.4 Block diagram of ATN NP5B noise figure measurement system configuration.

Chapter 3

Scalable Lossy Substrate Model for Various Pad Structures

The original lossy substrate model proved the mechanism of excess noises caused by substrate loss coupled through the lossy pads [4-6]. In this chapter, an enhanced lossy substrate model is developed to accurately simulate RF noise for on-chip devices with freedom in pad and TML (transmission line) layouts. This new lossy substrate model is composed of two parallel and series RLC networks in series with C_{pad} and C_{ox} to model the capacitive coupling through the GSG pads and TML from the low resistivity silicon substrate. The precise distribution of lossy substrate effect between that through the pads and the remaining portion through TML realizes accurate prediction of S-parameters and noise parameters for miniaturized devices over broadband regime.

3.1 GSG Pad Layout Structures

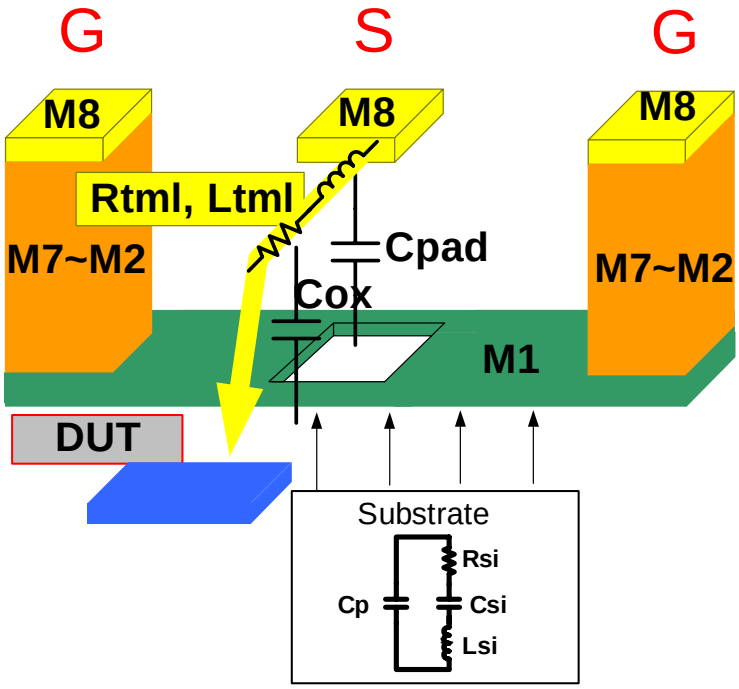
In order to study lossy substrate effect on high frequency noise and the excess noise induced through pad and TML, various GSG pad structures such as lossy, normal, and small pads with different metal topologies or pad sizes were fabricated by 0.13um Cu/FSG BEOL (Back-End-Of-Line) process to investigate the resulted lossy substrate effect. Fig. 3.1.(a) and (b) illustrate the 3D schematics for lossy and normal pads in which the ground pads (G) were constructed with stacked metals from the bottom (M1) to the top (M8) while the signal pads (S) were built with two different schemes. For lossy pad scheme in Fig. 3.1.(a), the S pad are composed of stacked metals from M2 to M8, whereas for normal pad scheme in Fig. 3.1.(b), they are consisted of top metal (M8) only and excluding all lower metals. As for small pad scheme, its signal pads just follow that of normal pad scheme but with smaller size of 50umx35um w.r.t. 50umx50um for normal and lossy ones. All three pad structures adopt exactly the same G pad scheme.

3.2 Lossy Substrate Model Development for Various Pad Structures

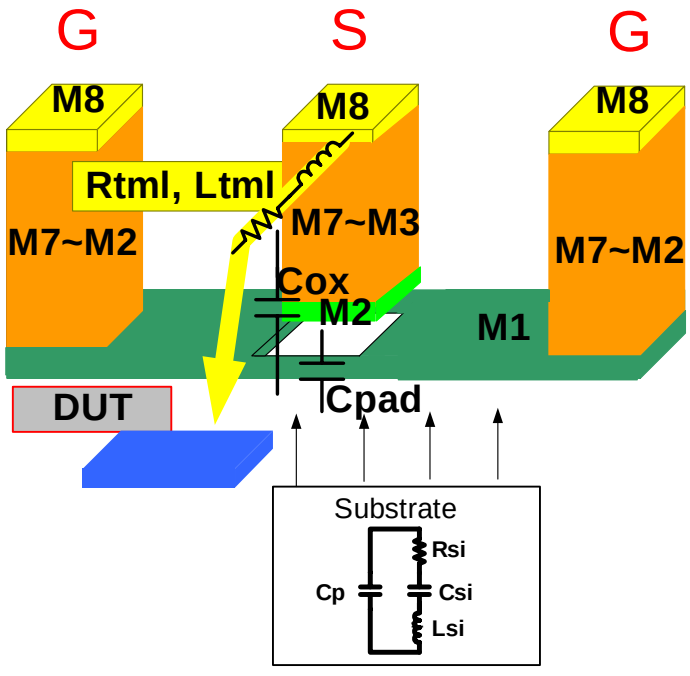
Before we study lossy substrate effect on high frequency noise and the excess noises, which were introduced through pad and TML, the open pad equivalent circuit model should be developed first. Fig. 3.2. depicts the equivalent circuit schematics of the enhanced lossy substrate model to incorporate various pad structures. This new RLC network was created to accurately capture the frequency response with varying pad structures associated with the lossy substrate. The primary enhancement to the original model is a modification on the substrate RLC network in conjunction with TML by adopting a C_{ox} representing the TML to substrate coupling capacitance. The resulted enhanced model is composed of two substrate RLC networks in series with C_{pad} and C_{ox} to simulate substrate loss through the pads and TML from silicon substrate, respectively. These capacitances are mainly governed by the signal pad or TML area and metal stack underneath. In this work, these two capacitances are physical parameters calculated based on layout and BEOL process parameters (metal thickness, IMD thickness and dielectric constants) rather than from extraction. C_{si} and L_{si} in series with R_{si} make this RLC network different from the conventional substrate network by a simple shunt RC. Capacitances C_p and C_{si} account for the capacitive coupling while substrate resistance R_{si} and inductance L_{si} were proposed to model the semi-conducting nature of silicon substrate under high frequency operation. Coupling capacitance C_c connecting the two-ports is required to model S_{12} and S_{21} of the open pads and it should be removed from the pad model when a device is attached through the two-ports to simulate S-parameters and noise parameters of a full structure before de-embedding. Regarding the resistance (R_{tml}) and inductance (L_{tml}) associated with transmission line, they can be extracted from Z-parameters of a short pad after modified open de-embedding. A complete extraction flow assisted by equivalent circuit analysis can be referred to our original work [4-5]. Fig. 3.3. illustrates the schematic block diagram derived by circuit analysis theory to extract the circuit elements (R_{si}, C_{si}, L_{si}, C_p, R_{TML}, and L_{TML}). Note that this model parameters extraction method just serves as the initial

values for further optimization. Parameters optimization was done by Agilent IC-CAP and Agilent Advance Design System (ADS) to get the best fit to S- and Y-parameters. The table 3.1 lists full set of model parameters through optimization for lossy, normal, and small pads respectively. We could observed something interesting from the parameters of lossy substrate model for various pad structures. The category of lossy pad reveals apparently larger capacitances for all three elements(C_{pad}, C_{p1}, C_{si1}) and lower resistance (R_{si1}) and inductance (L_{si1}) in the first RLC network under pad and larger C_{si2} and lower R_{si2}, L_{si2} under the second RLC network under TML. As shown in Fig. 3.4. The large capacitances indicated the much coupled effect from the lossy substrate, and the lower resistances and inductances implied that the low resistivity Si substrate effect. Note that C_{ox} is kept at similar value for all three kinds of pad due to the same metal layout and topology for TML from the pads to intrinsic device. On the other hand, C_{pad} presents significant difference among the three pad structures in which the scaling factors of around 3.9~4 for lossy versus normal and 0.82~0.85 for small versus normal just approach the theoretical values of 4.04 and 0.75 calculated by layout and process parameters. The accuracy of optimized lossy substrate model was verified and justified by good match with measured S_{11} and S_{22} (mag. and phase) for lossy, normal, and small pads together in Fig. 3.5. Good prediction was achieved for Y-parameters simultaneously (real and imagine part of Y_{11} and Y_{22}) as shown in Fig. 3.6. We could observed something interesting that the lossy pad reveals remarkably smaller magnitudes and more negative phase for both S_{11} and S_{22},extraordinary shift in magnitude and phase away from 1.0 and 0° under increasing frequency. We have been known that the purely capacitive plot on Smith chart was trended to along the side of smith chart and kept the constant R circle (kept the same magnitudes), which started form the point of Γ=1 on smith chart. The lossy pad revealed remarkably smaller magnitudes indicated there were not only capacitances but also some parasitic components like resistances and inductances in lossy substrate model to characterize this lossy effect, and the more negative phase indicated the larger capacitances. We could observed these effects

obviously from Y-parameters which larger Im(Y_{11}) indicated larger capacitances in the lossy pad. The difference between normal and small pads is much smaller. As a result, the enhanced lossy substrate model can accurately simulate the pad structure effects in terms of layout and metal topologies with predictable scaling factors.



(a)



(b)

Fig .3.1. 3D schematics of GSG pads (a) lossy pad scheme : S-pads with stacked metals from M2 to M8 (b) normal pad:S pads with top metal (M8) only

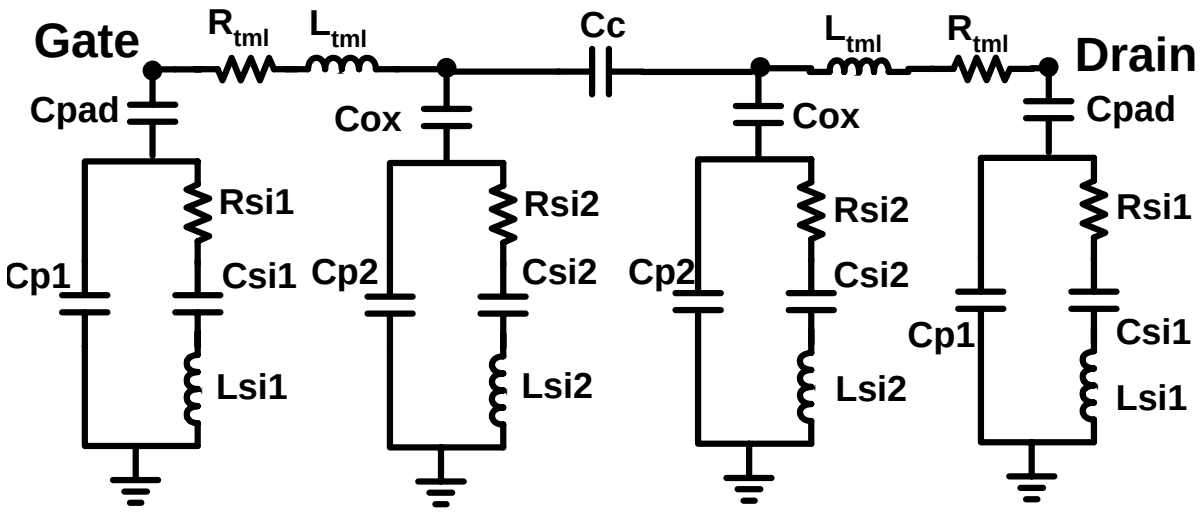


Fig. 3.2. The equivalent circuit schematics of enhanced lossy substrate open pad model

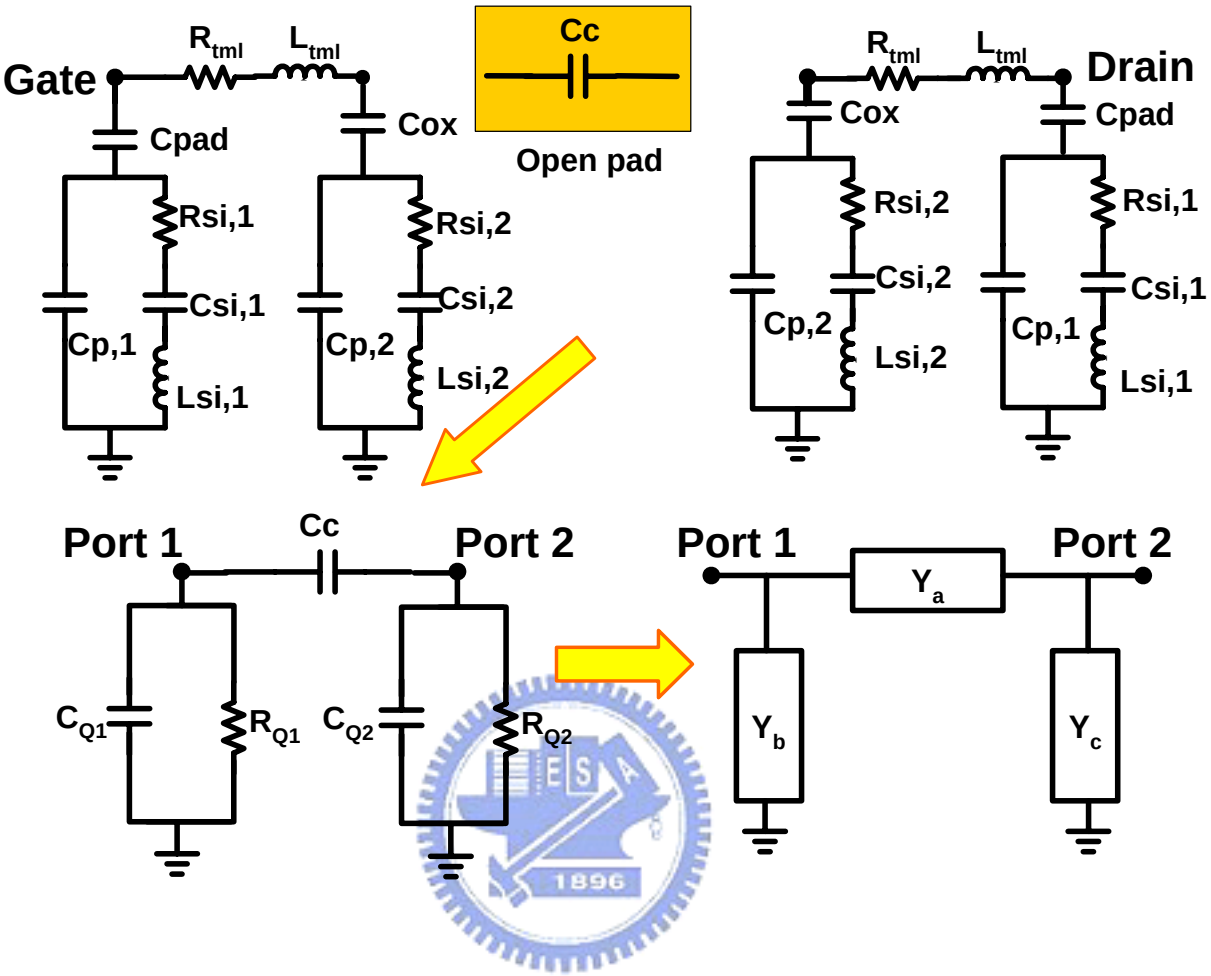


Fig. 3.3 (a) Equivalent circuit model derivation by circuit analysis

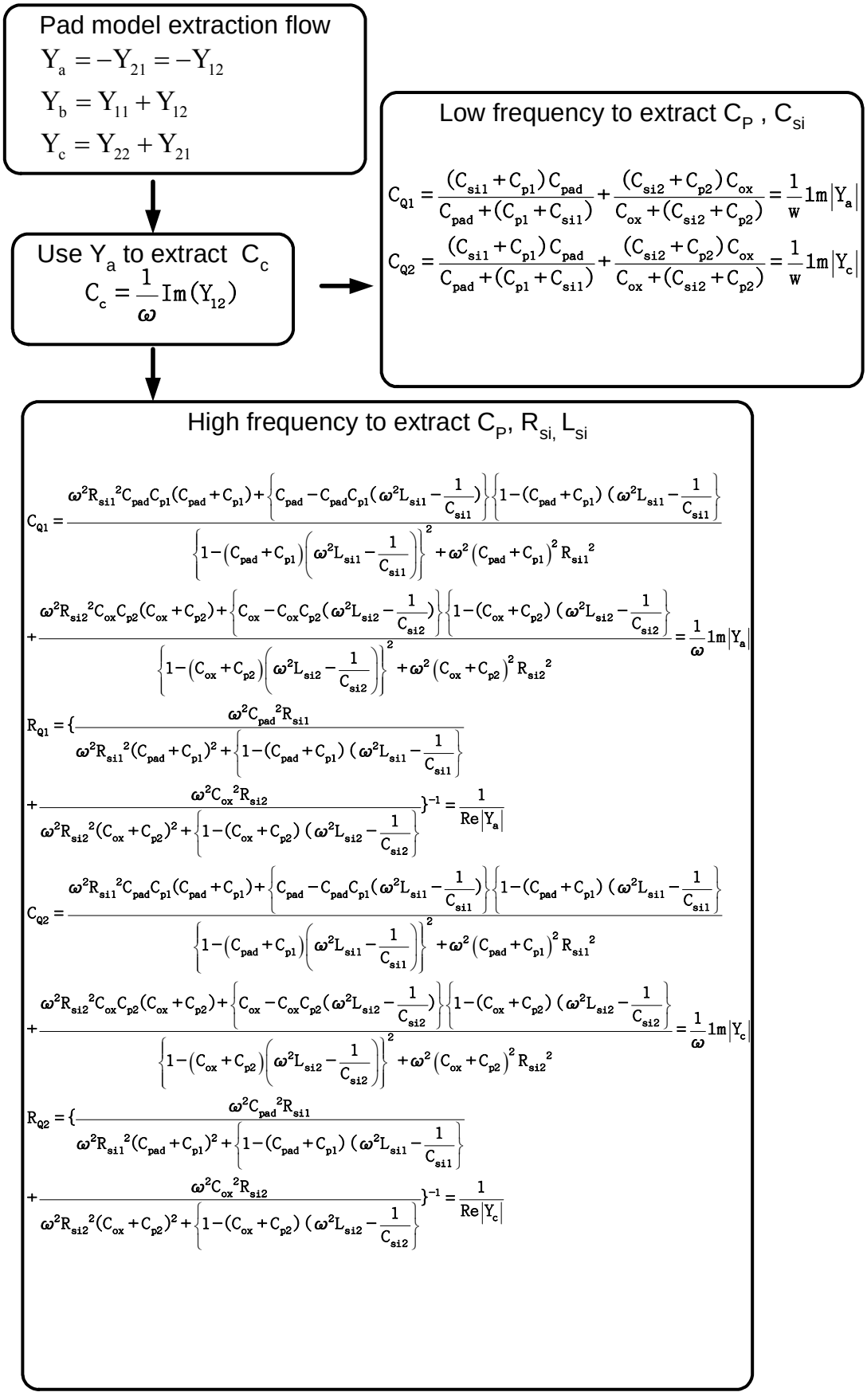


Fig. 3.3 (b) Pad model parameter extraction flow

Table 3.1

Pad model parameters for various pad structures

Gate Pad RLC model parameters							
Pad layout	**C_{pad} (fF)**	**C_{p1} (fF)**	**C_{Si1} (fF)**	**L_{Si1} (pH)**	**R_{Si1} (Ω)**	**L_{tml} (pH)**	**R_{tml} (Ω)**
Lossy	**77.87**	**74.97**	**200**	**170.7**	**159.9**	50	0.2
Normal	20	28.55	32.68	425.3	511.7		
Small	13.89	24.43	33.4	425.3	511.7		
Pad layout	**C_{ox} (fF)**	**C_{p2} (fF)**	**C_{Si2} (fF)**	**L_{Si2} (pH)**	**R_{Si2} (Ω)**	**C_c (fF)**	
Lossy	10.78	1.629	**45.98**	**515.4**	**328.8**	1.103	
Normal	9.932	2.553	9.316	874.3	638.3		
Small	9.913	2.635	8.741	874.3	638.3		

Drain Pad RLC model parameters							
Pad layout	**C_{pad} (fF)**	**C_{p1} (fF)**	**C_{Si1} (fF)**	**L_{Si1} (pH)**	**R_{Si1} (Ω)**	**L_{tml} (pH)**	**R_{tml} (Ω)**
Lossy	**80.99**	**62**	**200**	**83.72**	**164.3**	50	0.2
Normal	20.17	24.05	30	671.3	511.7		
Small	12.84	19.72	30	671.3	511.7		
Pad layout	**C_{ox} (fF)**	**C_{p2} (fF)**	**C_{Si2} (fF)**	**L_{Si2} (pH)**	**R_{Si2} (Ω)**		
Lossy	11.07	2	**54.15**	**590.6**	**270.9**		
Normal	10.21	2.887	11.73	1059	540.3		
Small	9.932	2.635	10.29	1059	540.3		

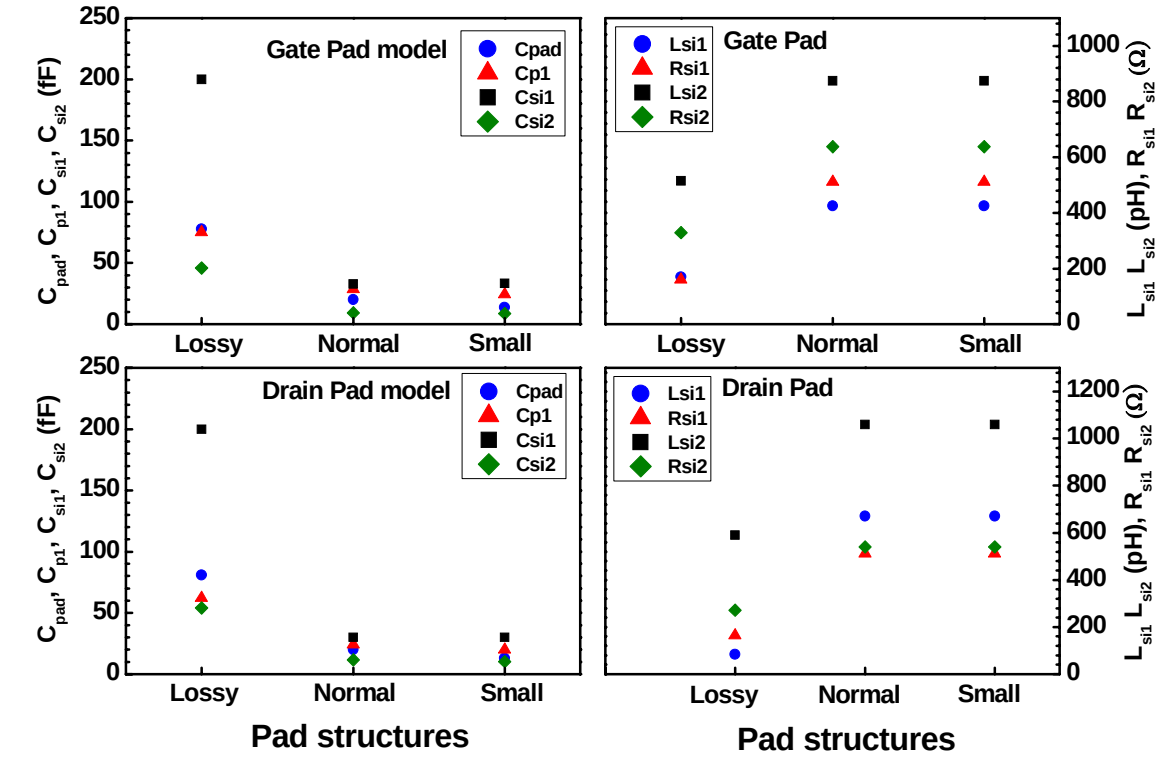


Fig. 3.4. Pad model parameters scalability for various pad structure

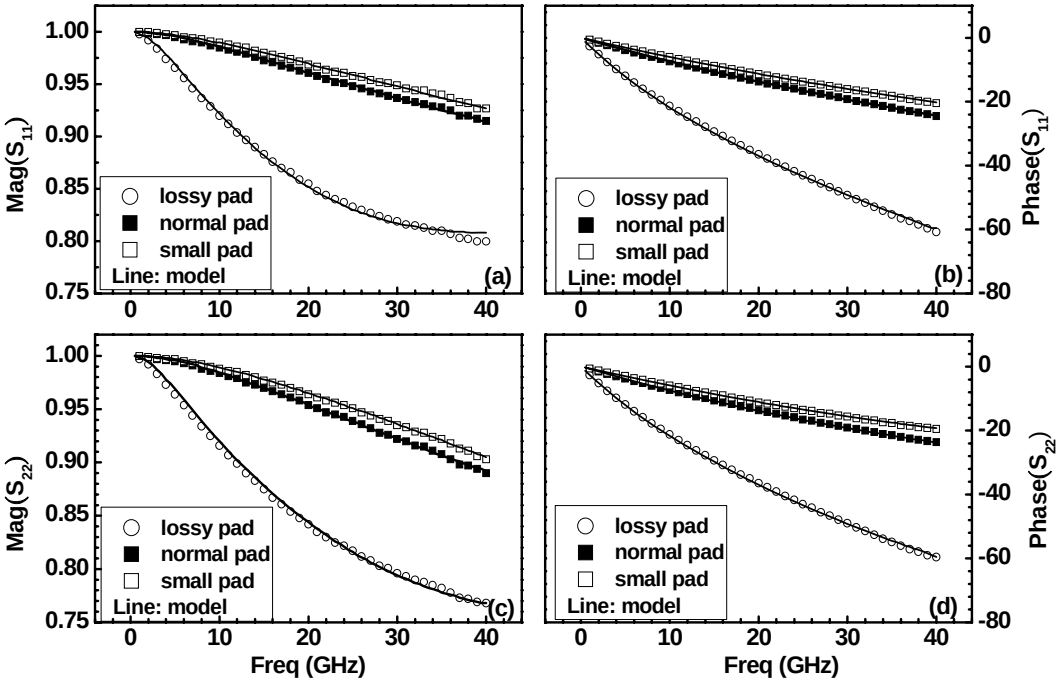


Fig. 3.5. Comparison of open pad S-parameters between measurement and lossy substrate model for three pad schemes, lossy normal, and small (a) mag(S_{11}) (b) phase(S_{11}) (c) mag(S_{22}) (d) phase(S_{22})

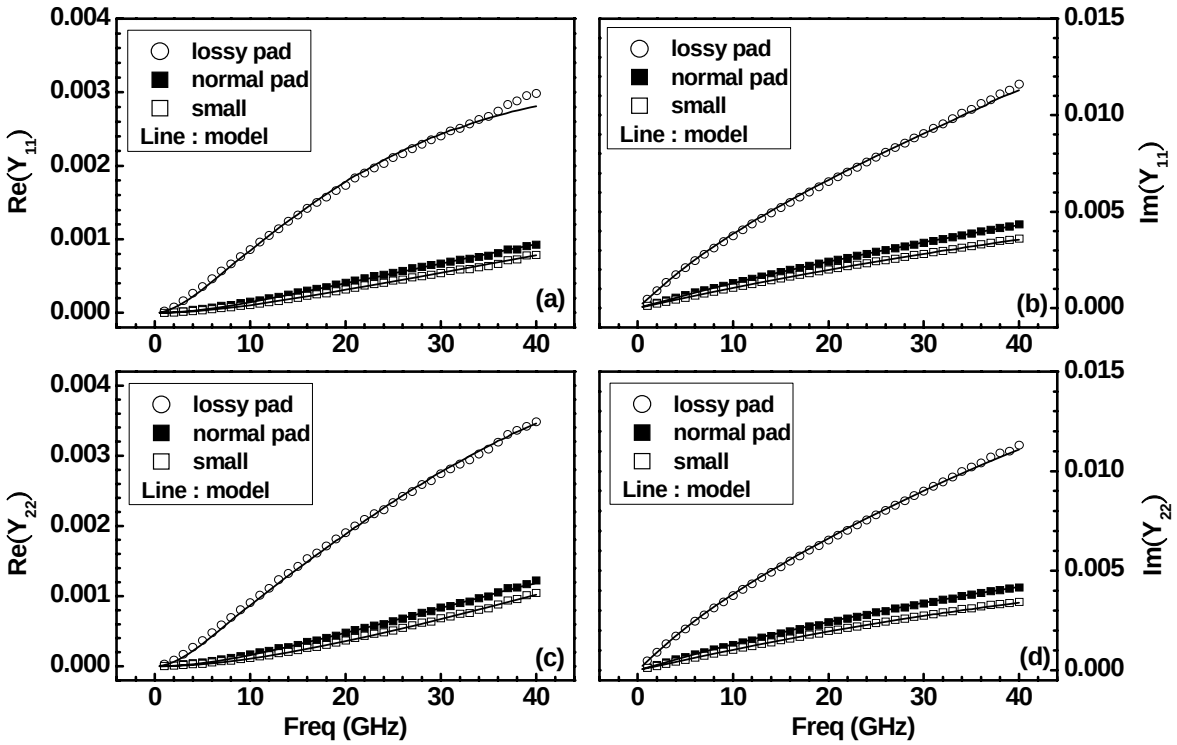


Fig. 3.6. Comparison of open pad Y-parameters for three pad structures (a) re(Y_{11}) (b) imag(Y_{11}) (c) re(Y_{22}) (d) imag(Y_{22})

Chapter 4

RF MOSFET Intrinsic I-V and C-V Model Calibration

4.1 I-V and C-V Modeling Theory Valid for Sub-100nm MOSFETs

It is very important and required pre-works to create an accurate current-voltage (I-V) and capacitance-voltage (C-V) model for RF MOSFET model development. A complete model of I-V characteristic over a wide bias range is important for nowadays circuit design, especially for analog and RF circuit design, where a variety of bias conditions will be used. Also with the rapidly increases demand for ultra-low power circuit design in recent year, an accurate model near subthreshold region is also necessary. An accurate capacitance model is also required to predict the devices or circuit speed and AC performance. In conclusion, correct I-V and C-V models are essentials to provide us trustworthy DC and AC characteristics for further study of high frequency performance.

In our research, Bsim3v3 model [13] is used which releases by foundry, TSMC for 0.13um MS/RF CMOS general purpose 1P8M 1.2V technology. In this thesis, there are three dimension of devices which keep width with 4um and length with 0.13um by various finger numbers of NF=18, 36, 72, were adopted for I-V , C-V and S-parameters model calibration and extended to high frequency noise model development. Multi-finger structure was employed to reduced gate resistance and the induced excess noise, and then further to investigate the impact on high frequency and noise performance as well as model scalability to fit various device geometries. The model calibration work was started by modifying the model parameters in Bsim3v3 model. Before this work, DC I-V and two port S-parameters were measured by Agilent vector network analyzer up to 40GHz. Y- and H- parameters can be derived from S-parameters for extraction of gate capacitances (C_{gg}, C_{gs}, C_{gd}) and current gain

cut-off frequency f_T. The ultimate goal is to build a accurate model by Bsim3v3 model calibration which can be correspond to the measured results on I-V, C-V, S-parameters, and noise performance. Before starting the model parameters calibration and optimization, we must be known some process related model parameters are specified and fixed at their known values, such as some important geometry or process parameters, L_{int} (channel length offset), W_{int} (channel width offset), T_{ox} (oxide thickness), N_{ch} (channel doping concentration), X_j (junction depth) and so forth. For sub-100nm MOSFET, the following important mechanisms are considered in Bsim3v3 model (1) short channel and narrow width effects on threshold voltage, (2) mobility reduction due to vertical field, (3) velocity saturation, (4) drain-induced barrier lowering (DIBL), and (5) Substrate current induced body effect (SCBE). It is assumed that most of the I-V and C-V parameters were fairly modeled in the original model and only minor modification is needed to improve the model accuracy.

4.2 DC I-V Model Development

For RF MOSFET, 3–terminal test structure is usually implemented with common source configuration in which source and body terminals are tied together and grounded. To measure its high frequency characteristic (both S parameter and NF_{min}), two sets of probing pad with G-S-G structures are implemented and connected to the gate and drain terminals. The parasitic resistances associated with MOSFET's terminals such as R_{g_ext}, R_{d_ext}, R_{s_ext}, and R_{b_ext} contributed from the interconnection lines and probing pads will affect I-V characteristic of DUT. In I-V model development, these parasitic resistances can not be moved out. Extraction of these parasitic resistances should be done and added to the original intrinsic MOSFET model (BSIM3). These parasitic resistances such as R_{d_ext} and R_{s_ext} will cause the measured drain current degradation. R_{d_ext} at drain terminal will affect the rising slope between linear and saturation region, and R_{s_ext} at source terminal will affect the drain current at saturation region and also cause the transconductance (gm) degradation. R_{g_ext} at

gate terminal is minor affect on drain current because the current at gate terminal is assumed to very small, and without voltage dropped across the R_{g_ext} at gate terminal. Therefore, modeling these parasitic resistances accurately is very important. The mentioned parasitic resistances can be extracted from the dummy short pads which is designed to de-embed the resistive and inductive parasitics of the interconnect lines and probe pads, etc. In this study, simulation was done by using Agilent IC-CAP for model verification and calibration. Based on the original model card, default simulation results of I_d-V_g and I_d-V_d curves were obtained. Through comparison between simulation and measurement in terms of I_d-V_g and g_m-V_g curves in both linear and saturation regions, significant deviation was identified for the threshold voltage (V_{th}), drain current (I_d), gate subthreshold swing (S), etc. As for comparison of I_d-V_d curves, channel length modulation (CLM) and drain induced barrier lowering (DIBL) effects were revealed. In BSIM3v3 model, there are many parameters associated with the threshold voltage model. Since source and body of the DUT are tied together and connected to ground, body bias effect on threshold voltage is not available. Narrow width effect on V_{th} was neglected for sufficient large width of 4μm. Short channel effect related parameters such as *Dvt0* and *Dvt1* were included to account for charge sharing induced threshold voltage lowering. Mobility model parameter *U0* is the zero-filed mobility for I_d-V_g simulation in linear region under small drain bias (V_d = 0.1 or 0.05V). *Ua, Ub* and *Uc* are fitting parameters used to model the mobility degradation subject to normal field under gate bias. Saturation velocity V_{sat} determines the saturation current level. *Eta0* and *Dsub* control the amount of threshold voltage variation caused by DIBL and I_d-V_g under V_d= V_{dd} is the fitting target. Parameters *A1* and *A2* stands for first and secondary non-saturation effect which occurs in the expression of V_{dsat} also help to improve I_d-V_g and g_m-V_g modeling. Subthreshold current fitting can be improved by V_{off} and *Nfactor* after the previous terms are well modeled. As for I_d-V_d modeling, *Pclm*, *Pdiblc1*, *Pdiblc2* can be used to properly modify the linear and saturation currents as well as output resistance R_{out}. Besides I_d-V_g and I_d-V_d characteristics,

first order derivative and even second order derivative also deserve the effort to be well modeled since g_m or g_{ds} at a certain given bias (application bias point) may affect the device performance such as f_T, f_{max} as well as circuit simulation result.

Fig. 4.1 ~ Fig. 4.4 present the DC I-V modeling results. Good agreement between measured and simulated results under varying biases and various N_F shows the integrity of the intrinsic BSIM model. Due to the same metal routing of the interconnect lines for various pad structures (same parasitic resistances and inductances), and the DC I-V characteristic have no concern with the pad capacitances. So the DC I-V measured results for various pad structures were almost identical when used the same device geometries. Therefore, the DC I-V modeling results which present in Fig. 4.1~4.4 are without the pad definition. Actually, the DC I-V modeling results were not exactly fitting the measured one, because it is difficult to exactly modeling I-V and S-parameters simultaneously especially on S_{22}. So we met a trade off between the exactly fitting on I-V model but poorly accurate on intrinsic S-parameters and doesn't purely exact fitting but looks ok on I-V model and almost exactly fitting on intrinsic S-parameters, and we have chose the latter one.

4.3 Intrinsic C-V Model Development

In this section, intrinsic gate capacitance model of multi-finger RF MOSFET is presented. For submicron MOSFET, the thinner oxide thickness is necessary which can reduce SCE (short channel effect), gate swing, but suffer the penalty of gate leakage and gate capacitances. Since the details are not our focus. The physical oxide thickness of RF013G NMOS technology is 2.8nm. For this thin oxide thickness, the BSIM3 capacitance model flag capMod=3 was set as default model to consider the finite charge thickness determined by quantum effect, which becomes more important for thinner T_{ox} CMOS technologies.

Capacitances in MOSFET is generally divided into three parts, intrinsic, extrinsic, and extrinsic parasitic. In Bsim3v3 model, intrinsic and extrinsic capacitances model were been

included, but extrinsic parasitic capacitance neither. We will explain this later. The intrinsic is associated with the region between the metallurgical source and drain junction. The extrinsic capacitances model considered in BSIM3 are fringing capacitance and overlap capacitance, both consist of bias dependent and bias independent part. In this thesis, only the bias independent outer fringing capacitances are added between the gate and source as well as the gate and drain (parameter *CF*). The overlap capacitances are composed of two parts: (1) bias independent component which models the overlap capacitances between the gate and the heavily doped (non-LDD) source/drain (parameter *Cgso*, *Cgdo*); (2) bias dependent between gate and the gate and the lightly doped (LDD) source/drain (parameter C_{gsl}, C_{gdl}). Finally, the extrinsic parasitic capacitances are due to the metal routing (M1~M3) parasitic capacitances which can not be de-embedding. Because the open dummy pad we used in this thesis was deembedding to M3, and couldn't clearly de-embedding the metal routing capacitances below M3. So these parasitic capacitances (C_{gs_ext}, C_{gd_ext}, C_{ds_ext}) should be added to the original intrinsic MOSFET model. Fig. 4.5. demonstrates a detailed classification of capacitances in MOSFETs.

Capacitances of RF MOSFET with GSG probing structure are conventionally extracted from the intrinsic Y parameter (Y_{int}) at low frequency. Before the extracting process, parasitic capacitances due to probing pad and interconnection metal should be de-embedded from the measured data. Traditionally, the removal of these parasitics is done through open de-embedding mentioned early. In fact, short de-embedding should also be carried out to get rid of the series impedances. This is essential for accurate capacitance extraction. A broadly accepted de-embedding technique is open/short two step de-embedding for two-port three terminal device (source/bulk tied together) [22]. Due to the fact, a conventional open pad leaving only the GSG pad can not de-embedding all the coupling capacitances. Thus remand the metal connecting between DUT and GSG pad. However, the coupling capacitances

between two port is mainly dominated not only GSG pad but also the interconnection line which may influences the accuracy of capacitances extraction on real device. Therefore, a modified open/short de-embedding approach was used to improve these influence. A modified structure is to remove the DUT cell simply, thus leave the connecting metal between DUT cell and signal metal pad. This modification enables us to extract the capacitances of the DUT cell that is sometimes what a circuit designer need in some cases. Appendix B presents this modified de-embedding. The new de-embedding method is especially efficient when an open pad is designed with all the interconnection metal left.

After the open/short de-embedding, intrinsic gate capacitances can be extracted from the formulas given by [23]:

$$C_{gg} = \mathrm{Im}(Y_{int,11})/\omega \tag{4-1}$$

$$C_{gd} = -\mathrm{Im}(Y_{int,12})/\omega \tag{4-2}$$

$$C_{gs} = \mathrm{Im}(Y_{int,11}+Y_{int,12})/\omega \tag{4-3}$$

$$C_{ds} = \mathrm{Im}(Y_{int,22}+Y_{int,12})/\omega \tag{4-4}$$

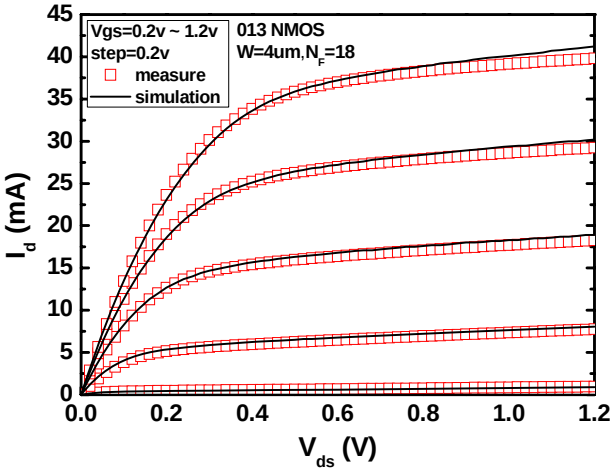
Intrinsic gate-to-back capacitance C_{gb} is negligible due to its small value in triode and saturation regions. This is because the inversion layer in the channel shields between gate and bulk. In the modeling process, extrinsic components C_{gs_ext} and C_{gd_ext} were used to model the remanded parasitic capacitance (M1~M3) and model parameters, C_{gso}, C_{gdo}, C_{gsl}, C_{gdl}, V_{offcv} were used to complete the result. With little modification on these model parameters, C-V characteristics ca be modeled well. First, adjust C_{gso} and C_{gdo} to a value so that simulation result is close to the measured one. Then, use V_{offcv} to better fit measured near subthreshold region. C_{gsl} and C_{gdl} are employed to modulate the gate bias trend of C_{gs} and C_{gd} individually.

Finalized model parameters are shown in Table 4.1. Fig. 4.6. present the modeling result of gate capacitances for multi finger (NF=18, 36, 72) NMOS devices.

Table 4.1

Model parameters for gate capacitances modeling

T13RF-95A		Modified values							
W_F=4um	N_F	C_{gs_ext}(fF)	C_{gd_ext}(fF)	C_{gs0}(F/m)	C_{gd0}(F/m)	C_{gsl}(F/m)	C_{gdl}(F/m)	C_F(F/m)	Voffcv
	18	5.37	1.99	360p	386p	70p	70p	0	-0.053
	36	9.27	3.69	360p	386p	70p	70p	0	-0.053
	72	17.07	7.10	360p	386p	70p	70p	0	-0.053



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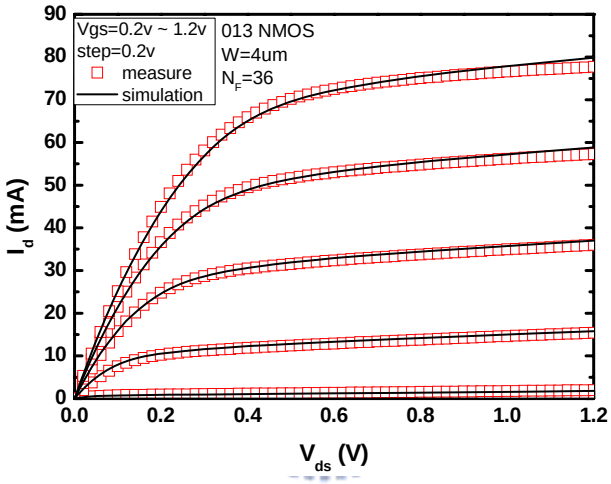

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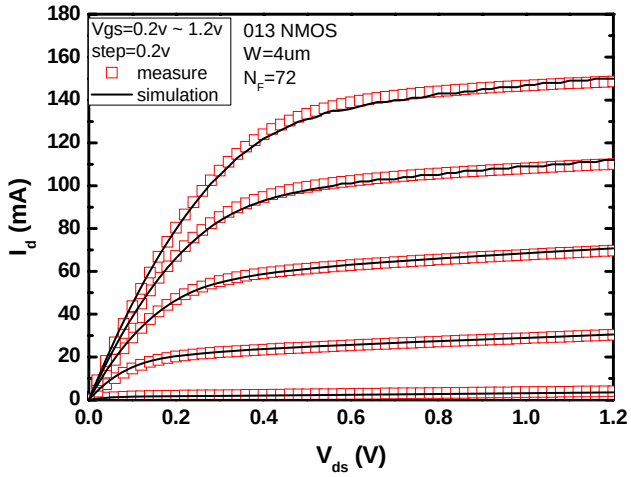
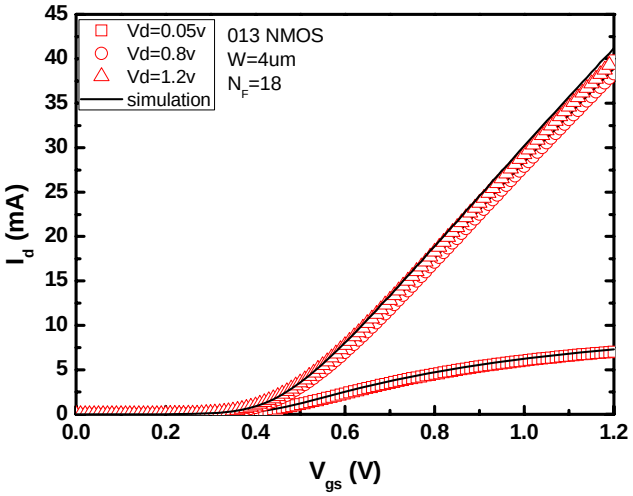
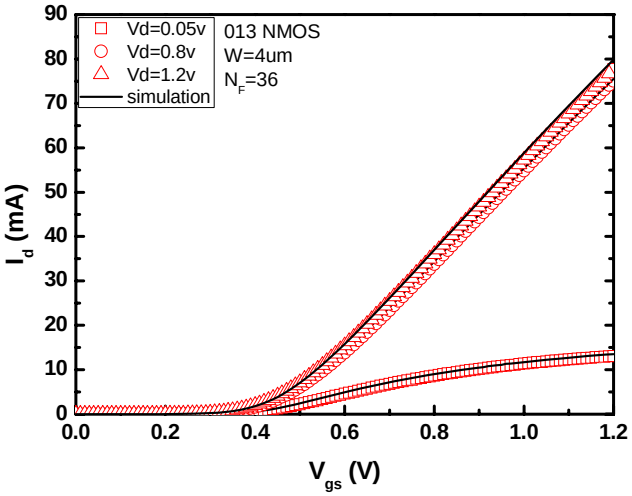


(c)

Fig. 4.1. Modeling results of DC Id-Vd for Vg=0~1.2V with 0.2 Vg step. (a)N_F=18 (b)N_F=36 (c)N_F=72



(a)



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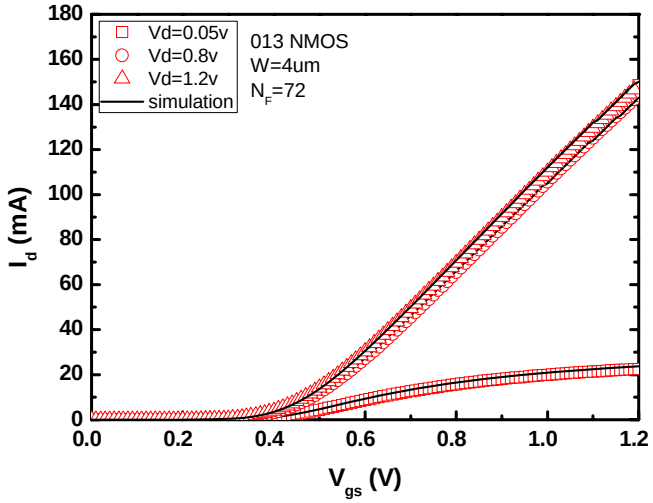
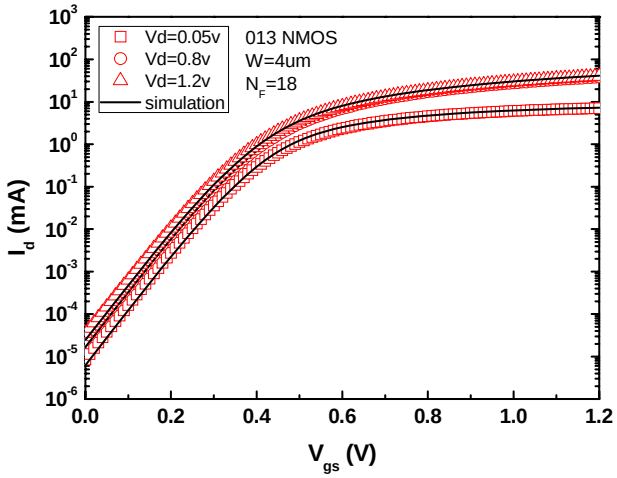


(c)

Fig. 4.2. Modeling results of DC Id-Vg for Vd=0.05, 0.8, 1.2V (a)N_F=18 (b)N_F=36 (c)N_F=72



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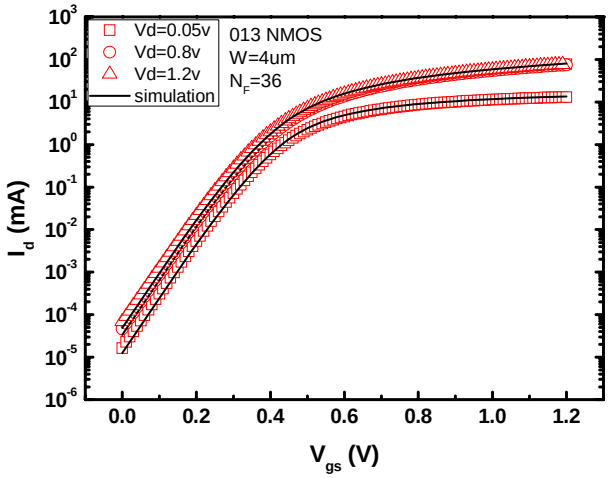

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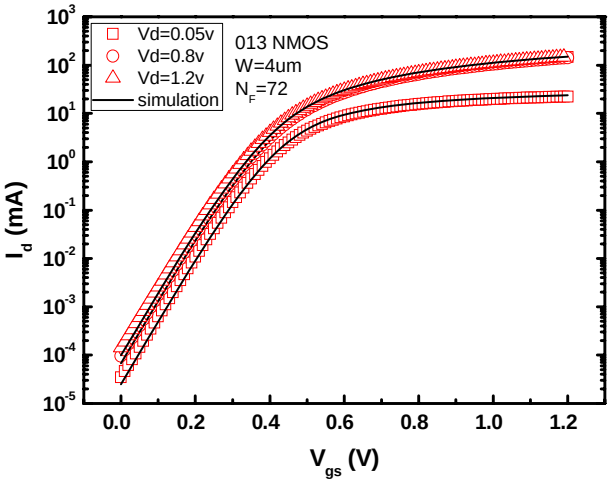
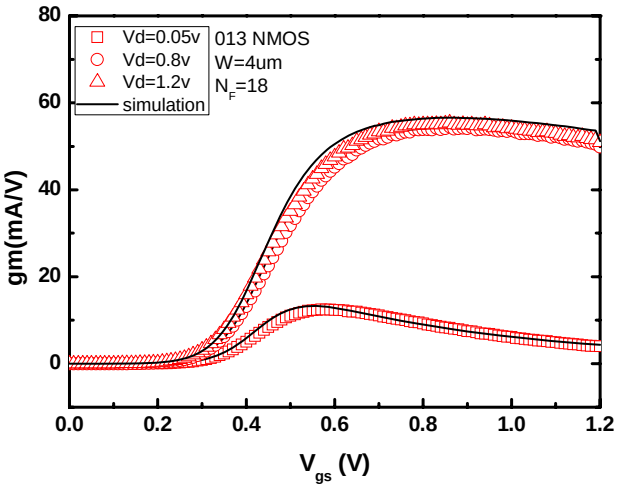
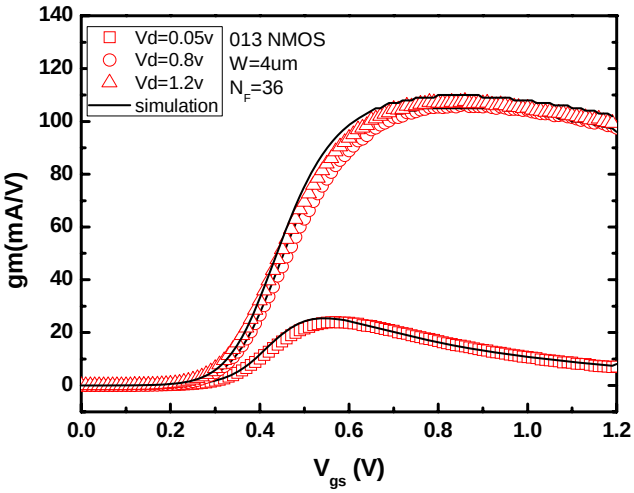


(c)

Fig. 4.3. Modeling results of DC log scale Id-Vg for Vd=0.05, 0.8, 1.2V (a)N_F=18 (b)N_F=36 (c)N_F=72



(a)



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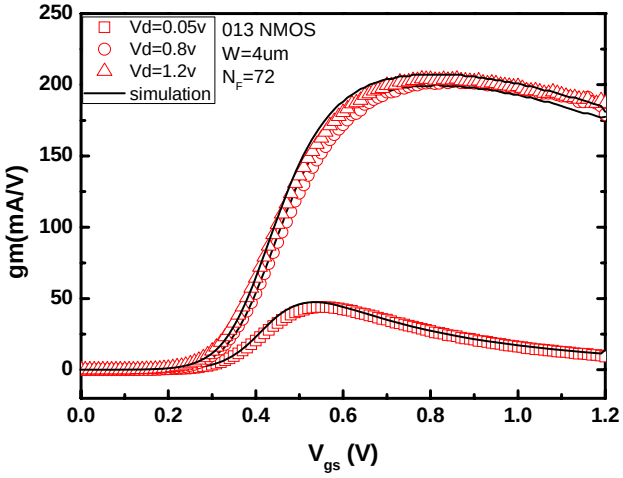

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Fig. 4.4. Modeling results of gm-Vg for Vd=0.05, 0.8, 1.2V (a)N_F=18 (b)N_F=36 (c)N_F=72

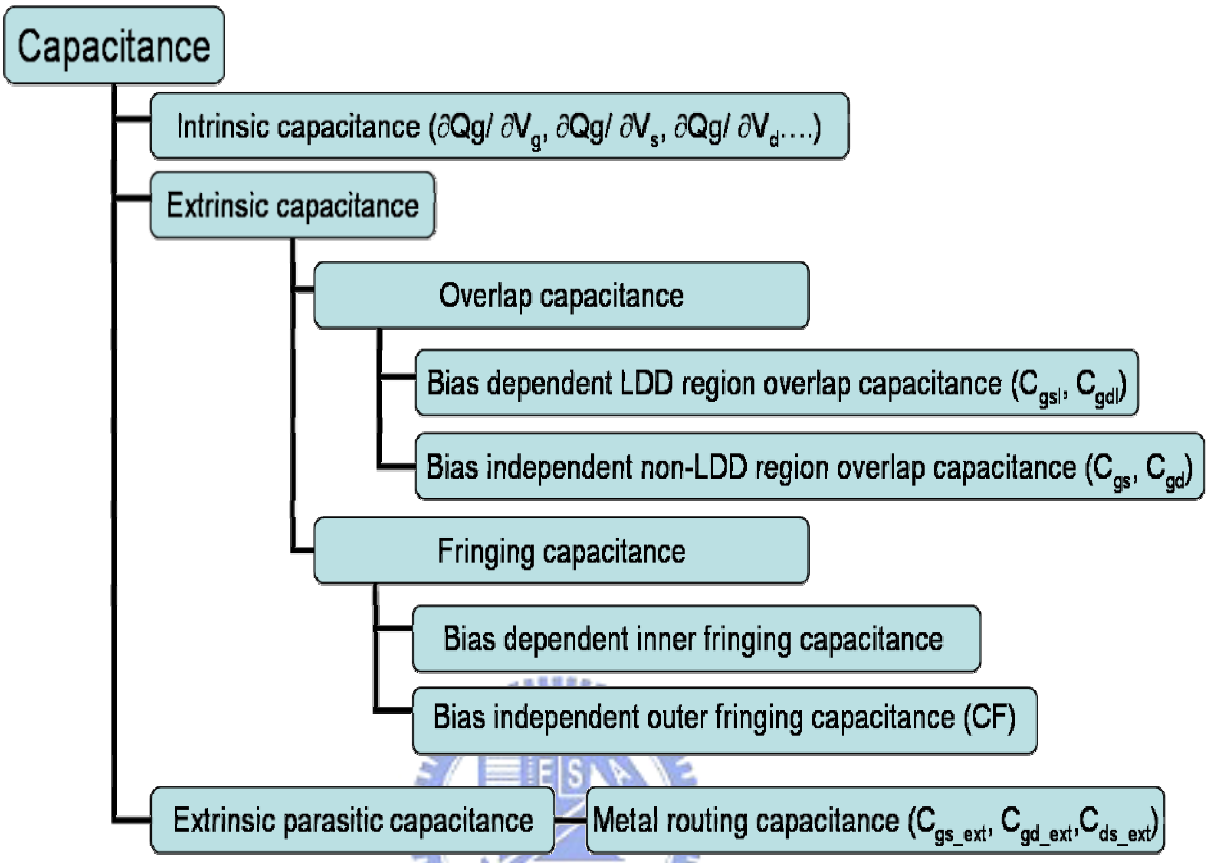
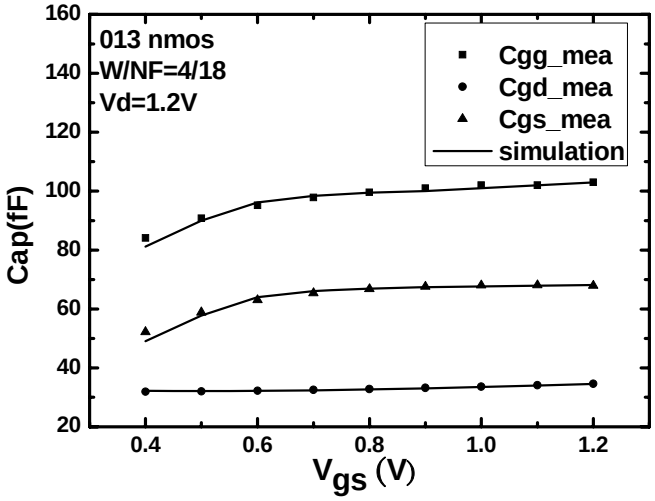
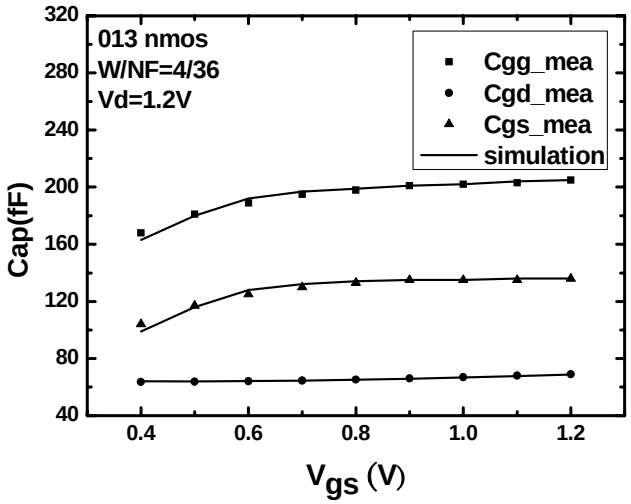


Fig. 4.5.Category diagram of gate capacitances in MOSFETs



(a)



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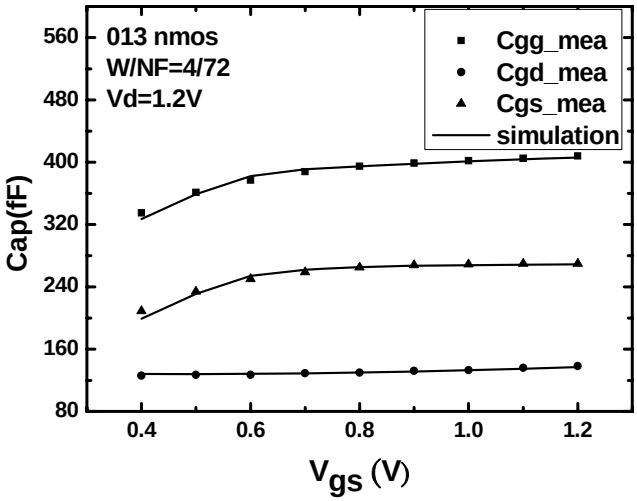

(c)

Fig. 4.6.Gate capacitances modeling results under various Vg (a)N_F=18, (b) N_F=36, (c)N_F=72

Chapter 5

Lossy Substrate Model to Predict Pad Structure Effect on RF Noise-Broadband Accuracy & Scalability

In this chapter, the enhanced lossy substrate model was further verified by integrating with the intrinsic devices for full circuit (pad+intrinsic) simulation to identify the impact on high frequency and noise characteristics. The particularly interesting and useful application is an accurate and simple noise extraction method to ensure noise simulation accuracy for nanoscale devices. Before starting the full circuit model calibration. The lossy substrate model must be developed firstly by open pad measurement (chapter 3). Then the model calibration was done on the intrinsic device's I-V and C-V models(chapter 4). Afterward, 4 terminal parasitic R and L (R_g, R_s, R_d, R_{bulk}, L_g, L_d, L_s) were correctly extracted and deployed in intrinsic MOSFET. Consequently, good match in terms of gm, C_{gg}, C_{gd}, C_{gs} (Y-parameters), and f_T (H-parameters) over wide range of biases or currents was realized for 100nm NMOS of various finger numbers (N_F=18, 36, 72). The full circuit model accuracy can be verified in terms S-parameters up to 40GHz and noise parameters up to 18GHz.

5.1 Equivalent Circuit Model Verification

Fig. 5.1. illustrates the device characterization and modeling flow. An equivalent full circuit include the pad model and intrinsic MOSFET model were shown in Fig. 5.2. The RLC networks represents the lossy pad, lossy substrate ,and transmission line are linked with the intrinsic MOSFET. The dash block in the full circuit schematic was the equivalent circuit of intrinsic MOSFET which given by foundry. A core BSIM3 MOSFET model was calibrated in terms of I-V and C-V characteristics. Due to that BSIM3 MOSFET model didn't include the high frequency characteristic components like gate resistances and substrate network. Therefore, in order to modeling the intrinsic MOSFET accurately up to 40GHz, some

parasitic components must be added to core BSIM3 model. The parasitic components such as gate resistance, substrate network, C_{ds} ,and R_{ds} were the important and necessary elements for high frequency characterization (S-,Y-parameters). In the intrinsic MOSFET model, two junction diodes were implemented to represent the drain-to-body and source-to-body p-n junctions. C_{ds} and R_{ds} were adopted to model the source to drain proximity capacitance and the associate resistance apparent at high frequency, they play an important role in accurate modeling of S_{22}. R_g is the gate resistance extracted from real part of Z-parameters which is mainly dominated by poly gate resistance and distributed channel-coupled resistance [23]. It's greatly affects the noise performance of the MOSFET. R_d is the parasitic drain resistance due to the metal routing below M3 which can not be de-embedding. R_s is a series resistance of metal interconnection to the source and substrate network due to that metal line connecting the source/bulk common to the ground pad. L_g, L_d, and L_s are parasitic inductances which required to model the high frequency effect (transmission line effect) of metal routing. The substrate network which has significant effect on high frequency characterization which are constructed of R_{db}, R_{sb}, R_b, C_{db}, C_{sb}, C_b. This substrate network model was original given by foundry TSMC, and we have only done calibration by adjusting parameters of the RC substrate network but didn't change the construction of this substrate network. This method was commonly be used to model the substrate effect by using three resistances and capacitances which the resistances and capacitances were parallel to each other. But we got important observation that these substrate components in series with a junction diode does not show visible effect in the simulated results at most affect S_{22} at high frequency. Finally, the noise current source ΔS_{id} is used to calibrate the abnormal trends on noise parameters near the subthreshold region in noise measurement of sweep drain current.

How do we develop this full circuit model accurate fitting by circuit simulation to the measured one? First, A accurate pad model which previously established from open pad structures (chapter 3). Then integrated with well calibrated intrinsic MOSFET model which

good agreement with I-V, C-V, S-parameters. It is fortunate that we didn't need to do any further optimization to get better fitting with the measured S-parameters, Y-parameters when integrated the pad model with the intrinsic MOSFET model. Finally, the full circuit model parameters for various N_F and pad structures are given in table 5-1(a) and (b). The pad model parameters verification for various pad structures has been covered in Chapter 3. We will focus on the intrinsic MOSFET model parameters here. It is assumed that parasitic resistance and inductance of metal interconnection can be removed after short de-embedding. Actually, a common shared short and open pad structures for various N_F were been used, and the short de-embedding structures which short to M3 may lead to de-embedding the metal line parasitics (M1~M3) not cleanly. Therefore, the small amounts of remaining parasitic resistances and inductances after short de-embedding was revealed. C_{ds} and R_{ds} played an important role in accurate modeling of S_{22}. As for larger N_F devices the larger C_{ds} and smaller R_{ds} were revealed. It was due to the metal of fingers between source and drain were in parallel. The bulk resistances also revealed this trend due to the parallel effect. Actually, in two port configuration, since the source and body are tied together. The complex signal coupling at port2 which include drain, source and bulk effect make us difficult to observe drain-bulk and source-bulk coupling effect directly. Many approaches have been proposed to established a accurate substrate model and parameters extraction method. However, a standard extraction and modeling method have not been established yet. In this thesis, a complete substrate network model parameters extraction method was not accomplished and not covered in this work. In our work, the parameters of substrate resistances and capacitances was given by foundry with a default value and made a little optimization.

Table 5-1

(a)Intrinsic MOSFET model parameters for various N_F

Intrinsic Model parameters after open/short de-embedded											
	Cds(fF)	Rds(Ω)	Rs(Ω)	Rd(Ω)	Rg(Ω)	Ls(pH)	Ld(pH)	Lg(pH)	Rb(Ω)	Rdb(Ω)	Rsb(Ω)
N_F=18	4.467	161.8	0.17	0.15	4.819	1.99	7.61	3.064	232.3	16.22	16.22
N_F=36	19.54	138.4	0.15	0.12	2.34	2.3	4.225	2.585	168.9	11.14	11.14
N_F=72	47	64.72	0.199	0.199	1.119	3.012	1.052	0.478	95.6	5.586	5.586

(b)Pad model parameters for various pad structures

Gate Pad RLC model parameters							
Pad layout	C_{pad} (fF)	C_{p1} (fF)	C_{Si1} (fF)	L_{Si1} (pH)	R_{Si1} (Ω)	L_{tml} (pH)	R_{tml} (Ω)
Lossy	77.87	74.97	200	170.7	159.9	50	0.2
Normal	20	28.55	32.68	425.3	511.7		
Small	13.89	24.43	33.4	425.3	511.7		
Pad layout	C_{ox} (fF)	C_{p2} (fF)	C_{Si2} (fF)	L_{Si2} (pH)	R_{Si2} (Ω)	C_c (fF)	
Lossy	10.78	1.629	45.98	515.4	328.8	1.103	
Normal	9.932	2.553	9.316	874.3	638.3		
Small	9.913	2.635	8.741	874.3	638.3		

Drain Pad RLC model parameters							
Pad layout	C_{pad} (fF)	C_{p1} (fF)	C_{Si1} (fF)	L_{Si1} (pH)	R_{Si1} (Ω)	L_{tml} (pH)	R_{tml} (Ω)
Lossy	80.99	62	200	83.72	164.3	50	0.2
Normal	20.17	24.05	30	671.3	511.7		
Small	12.84	19.72	30	671.3	511.7		
Pad layout	C_{ox} (fF)	C_{p2} (fF)	C_{Si2} (fF)	L_{Si2} (pH)	R_{Si2} (Ω)		
Lossy	11.07	2	54.15	590.6	270.9		
Normal	10.21	2.887	11.73	1059	540.3		
Small	9.932	2.635	10.29	1059	540.3		

The full circuit as shown in Fig. 5.2. was adopted for high frequency and noise simulation to achieve S-parameter and noise parameters before de-embedding. First, good

match in terms of gm, C_{gg}, C_{gd}, C_{gs} (Y-parameters), and f_T (H-parameters) over wide range of biases or currents was realized for 100nm NMOS of various finger numbers (N_F=18, 36, 72). These intrinsic device parameters (gm, C_{gg}, C_{gd}, C_{gs}, f_T) played an important factor in accurate modeling high frequency noise characterization which shown as Fig. 5.3. Further, good agreement with both intrinsic and full circuit model S-parameters in wide range of biases was achieved. Fig. 5.4.~5.11. exhibit good match in S-parameters (magnitude and phase) and Y-parameters (real and imagine part) between model and measurement under V_{gs}=0.8V at maximum gm for full circuits adopting various pad structures and intrinsic ones after pad de-embedding. It is worth to note that intrinsic S-parameters of the devices after de-embedding are almost the same from different pad structures. It suggested that the de-embedding method could be de-embedding all the parasitic components from GSG pad clearly. In Fig. 5.4.(a)-(c), the phase sign change from negative to positive revealed by full circuits of larger devices (N_F=36, 72) at sufficiently high frequency accounts for the parasitic inductance effect. This effect can be eliminated for intrinsic devices in Fig. 5.4.(d) subject to pad and lossy substrate de-embedding. In practice, we can not observe the pad effect obviously with various pad structures in S-, Y- parameters. Furthermore, we will focus on the pad structures effect on RF noise in next section.

5.2 Pad Structure Effect on RF Noise

In this section, we will focus on the lossy substrate effect on high frequency noise and the excess noise introduced through pad and TML for various pad structures. Before this work, the model calibration must be done on the intrinsic device's I-V, C-V (chapter4), gm, C_{gg}, C_{gd}, C_{gs} (Y-parameters), f_T (H-parameters) over wide range of biases or currents was realized for 100nm NMOS of various finger numbers (N_F=18, 36, 72), and full circuit S-parameters (pad+intrinsic) for various pad structures. Then this full circuit model accuracy can be

verified in terms noise parameters. Noise parameters (NF_{min}, R_n, Γ_{opt} or Y_{opt}) were measured by ATN-NP5B under Vgs=0.8V at maximum gm, and sweeping frequency to 18GHz. Fig. 5.12.(a)-(c) indicate the simulated extrinsic NF_{min} and good agreement with measurement for full circuit adopting various pad structures such as lossy, normal, and the small pads respectively. Very interestingly, the devices adopting lossy pad reveal abnormally large finger number dependence and nonlinear frequency response (Fig. 5.12.(a)) while the finger number dependence is much relieved and frequency dependence was recovered to be linear for normal and small pads (Fig. 5.12.(b), (c)). It is very important to research what factors induce this nonlinear frequency response. According to the analytical expression related NF_{min} to devices parameters as follows:

$$F_{min} = 1 + K_1 \cdot \frac{f}{f_T}\sqrt{g_m(R_g + R_s)} = 1 + K_2 \cdot f \cdot C_{gs} \cdot \sqrt{\frac{(R_g + R_s)}{g_m}} \qquad (5\text{-}1)$$

According to equation (5-1). For intrinsic devices, it must revealed linear frequency dependence for intrinsic NF_{min}. So we suggested that this abnormal nonlinear frequency response is due to a great deal of noise coupling (larger C_{pad} on lossy pad) from lossy substrate which might covered up the real noise characterization on intrinsic devices. The larger NF_{min} revealed by the smaller finger number (N_F) in the category of lossy pads suggested the amplification effect through larger noise resistance R_n for small N_F devices (Fig. 5.13.). The larger noise resistance R_n indicate more sensitive to the source impedance. Another opinion is due to the fact that the pad capacitance may overwhelm the gate capacitance for miniaturized devices. So the small finger number (N_F =18) device revealed great influence by pad effect. The intrinsic NF_{min} simulated by the calibrated model as shown in Fig. 5.12.(d) presents near constant free from finger number dependence over wide range of frequency up to 18GHz. It is due to that the larger gm but smaller R_g for big devices, according to equation (5-1), gm and R_g are complementary to each other which keeping near f_T. The intrinsic NF_{min} at V_{gs}=0.8V corresponding to maximum gm is as low as 0.75dB at

10GHz and can be further suppressed to around 0.55dB under Vgs=0.5V corresponding to minimum NF_{min}. Fig. 5.14.~15. indicate the real(Y_{opt}), imag(Y_{opt}) respectively and good agreement with measurement for full circuit adopting various pad structures (a)~(c) and intrinsic one(d).

Pad structure effect on four noise parameters NF_{min}, R_n, Re(Y_{opt}), and Im(Y_{opt}) are illustrated in Fig. 5.16.~18. for N_F=18, 36, 72, to investigate finger number dependence of excess noise coupled through different pad structures. We can observe that the smallest device (N_F=18) in Fig. 5.16.(a)-(b) reveals the largest sensitivity to pad structures with substantial increase in NF_{min}, Re(Y_{opt}), and Im(Y_{opt}) for lossy pad. The pad sensitivity is obviously suppressed by increasing finger numbers. The pad effects that increase of mentioned excess noise becomes much smaller for N_F=72 in Fig. 5.18.(a)-(b). The noise resistance R_n is the key point for this phenomenon. The smaller devices reveal larger noise resistance R_n indicate more sensitive to the source impedance. We suggest it is due to the smaller gm and gate capacitances (C_{gg}) in small device. The pad capacitances (C_{pad}) in lossy pad and normal pad are around 100fF and 20fF respectively which close to the small device N_F=18 (C_{gg}≈100fF). Therefore, the pad capacitances will affects the source impedance greatly in small device (N_F=18) but not obvious affects on large device (N_F=72 for C_{gg} ≈ 400fF). As a result, the smaller device reveals larger sensitivity to various pad structures. Note that R_n is effectively reduced by increasing N_F attributed to smaller R_g and larger gm but keeps nearly constant for different pad structures. The pad effects were revealed on Re(Y_{opt}) and Im(Y_{opt}) then responded to NF_{min}. The scalability and broadband accuracy of the lossy substrate model is proven by good agreement with measured noise parameters corresponding to various pads as well as finger numbers and over wide range of frequencies to 18GHz. Based on the proven lossy substrate model and calibrated intrinsic MOSFET model, lossy substrate de-embedding can be done by removing the elements of the lossy pad and substrate R-L-C network from the full circuit model in Fig. 5.2. The parasitic resistance like R_g, R_d, R_s, R_b, etc, which can not be

removed through de-embedding were left with intrinsic MOSFET model to account for the excess noise. The intrinsic noise parameters extracted through lossy substrate de-embedding indicates effective reduction and recovery to linear frequency dependence in NF_{min}, $Re(Y_{opt})$, and $Im(Y_{opt})$. The extracted intrinsic $Re(Y_{opt})$ and $Im(Y_{opt})$ were compared with extrinsic Y_{opt} (measured or simulated) to identify the effect through lossy substrate de-embedding. This obvious reduction of $Re(Y_{opt})$ through de-embedding contributes to the significant suppression of NF_{min}. It is worth to note that NF_{min} of small pads are effectively suppressed near the intrinsic values. The physical parameters C_{pad} was play an important role on lossy substrate excess noise coupling. The larger C_{pad} caused the larger excess noise coupling path from the silicon substrate. With careful observe, the most amount of excess noise was contributed from lossy substrate under the signal pad (through C_{pad}), and minor amount of excess was contributed from lossy substrate under inter connection line (through C_{ox}).

As a result, the enhanced lossy substrate model of two R-L-C networks introduced via pad and TML justify themselves scalable through the physical parameters C_{pad} and C_{ox}, which consistently follow the pad and TML layout as well as metal topology parameters. The extreme conditions of fully open or fully short along pad and TML can be simulated by the scalable model to explore the optimized layout to approach the intrinsic noise characteristics. The simulation subject to extreme conditions suggests that elimination of C_{pad}, fully open along pad can minimize substrate loss induced excess noise and attain the intrinsic characteristics. On the other hand, elimination of C_{ox}, full isolation along TML makes minor contribution provided that C_{pad} stays not reduced. The proven scalable model is useful to guide pad and TML layout to minimize noise for miniaturized devices.

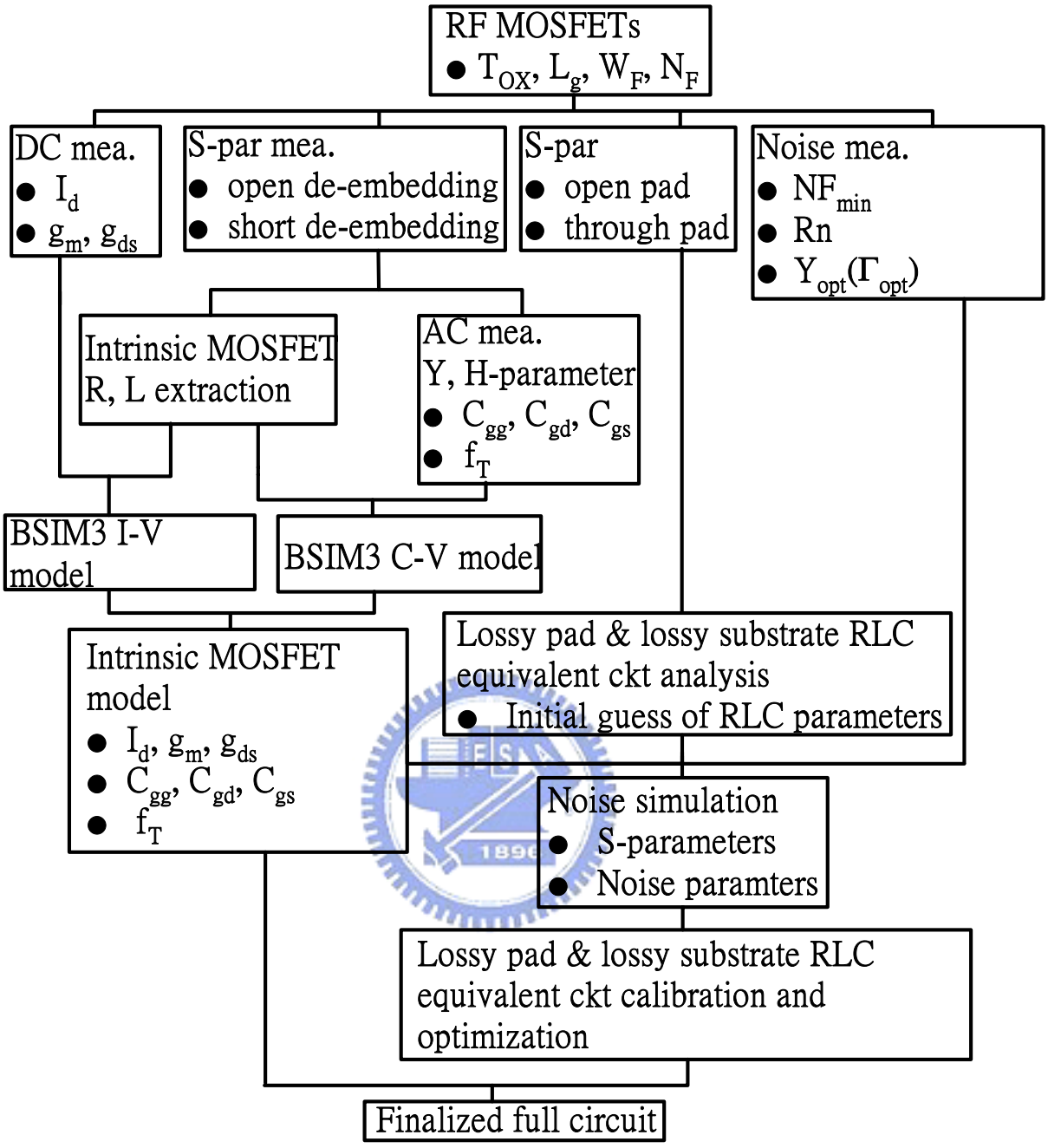

Fig. 5.1.MOSFET device modeling flow

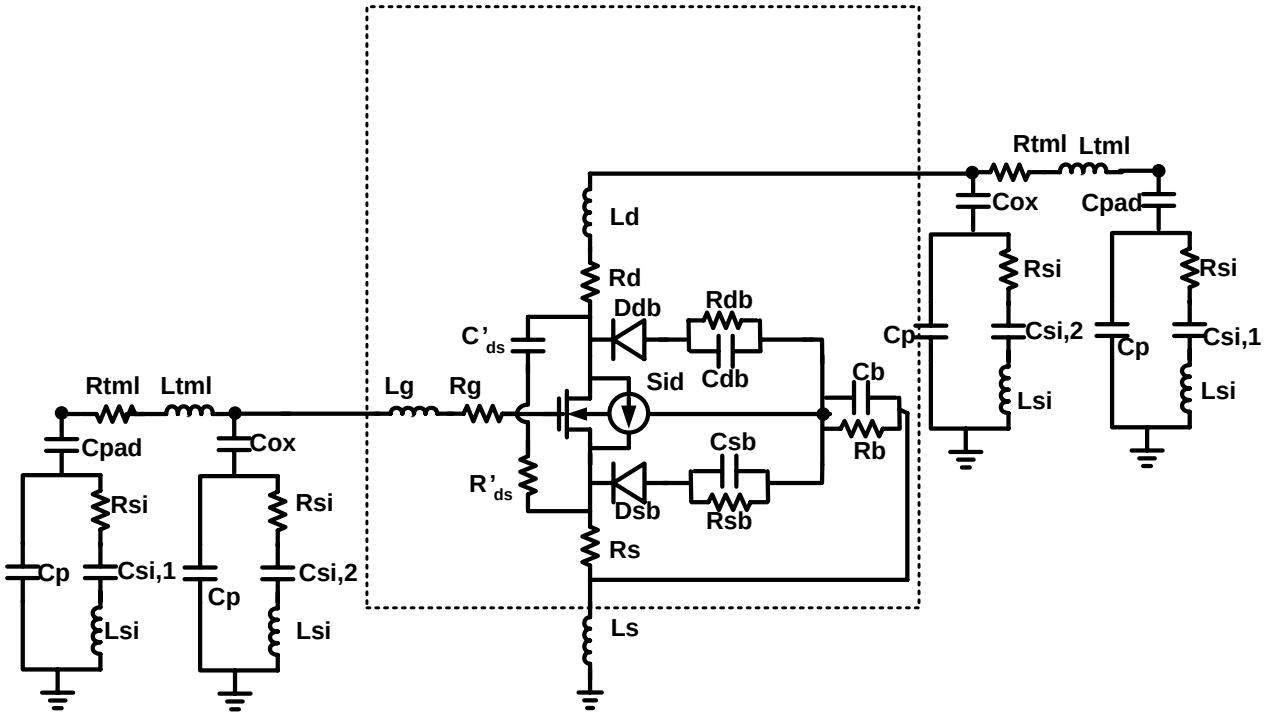

Fig. 5.2.Full circuit model includes intrinsic MOSFET device and pad model

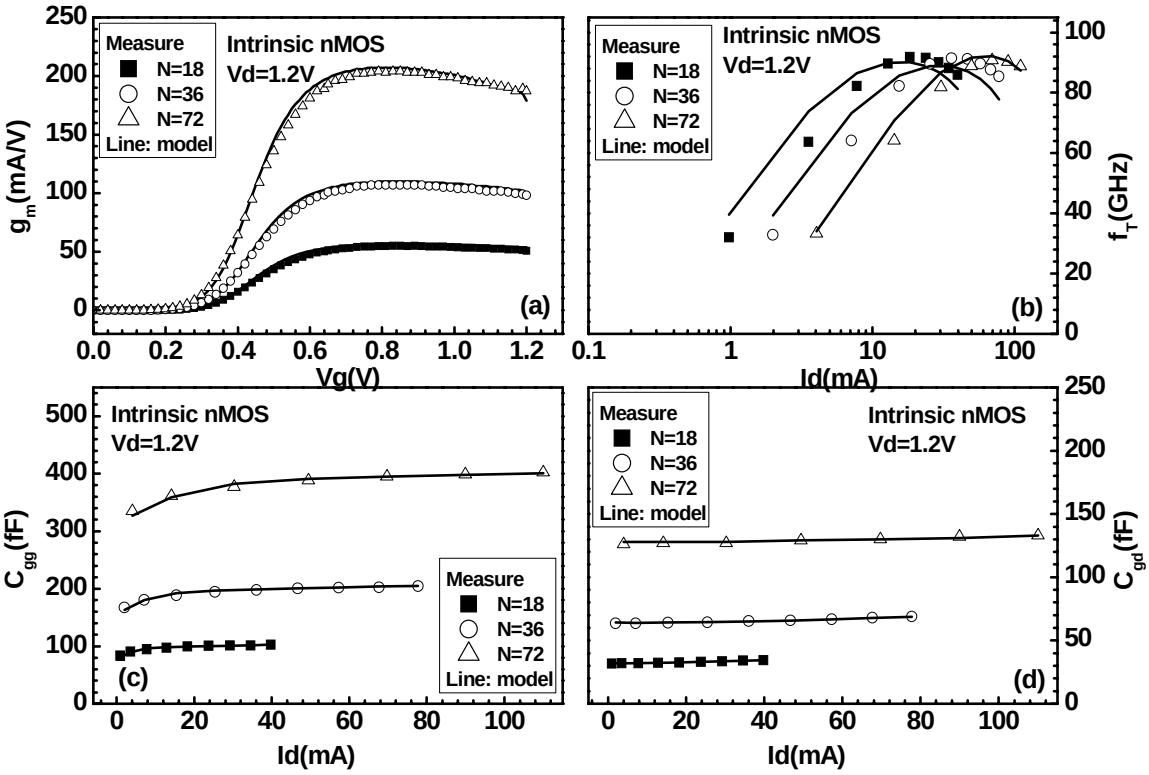

Fig. 5.3. Intrinsic MOSFET modeling results with good match in terms of (a)gm, (b)f_T (c)C_{gg}, (d)C_{gd}, and over wide range of biases or currents

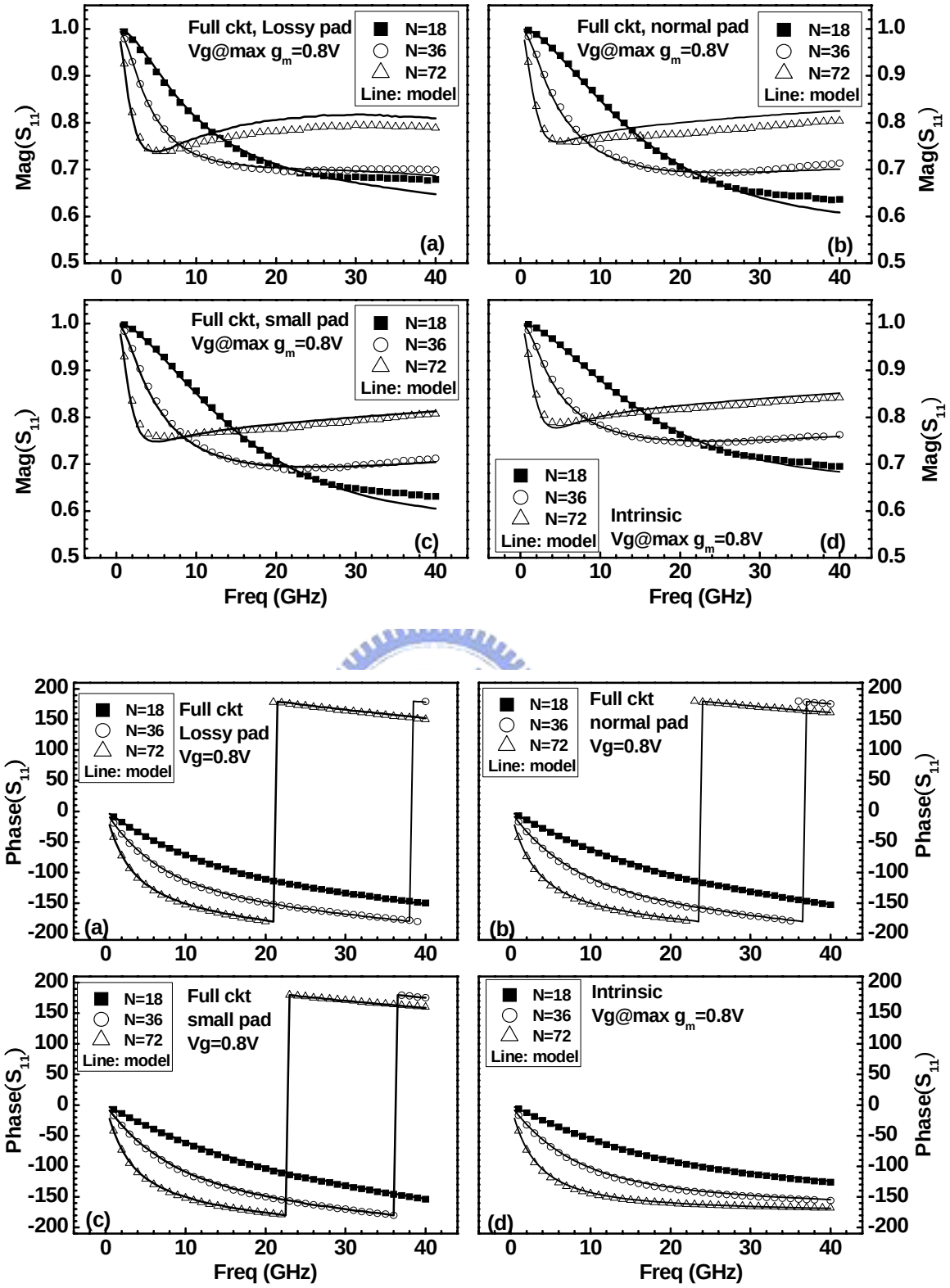

Fig. 5.4.Comparison of measured and simulated S_{11} by full circuit model for 100nm NMOS(N_F=18,36,72) adopting 3 different pads,(a)lossy pad (b)normal pad (c)small pad (d)intrinsic S_{11} by pad de-embedding

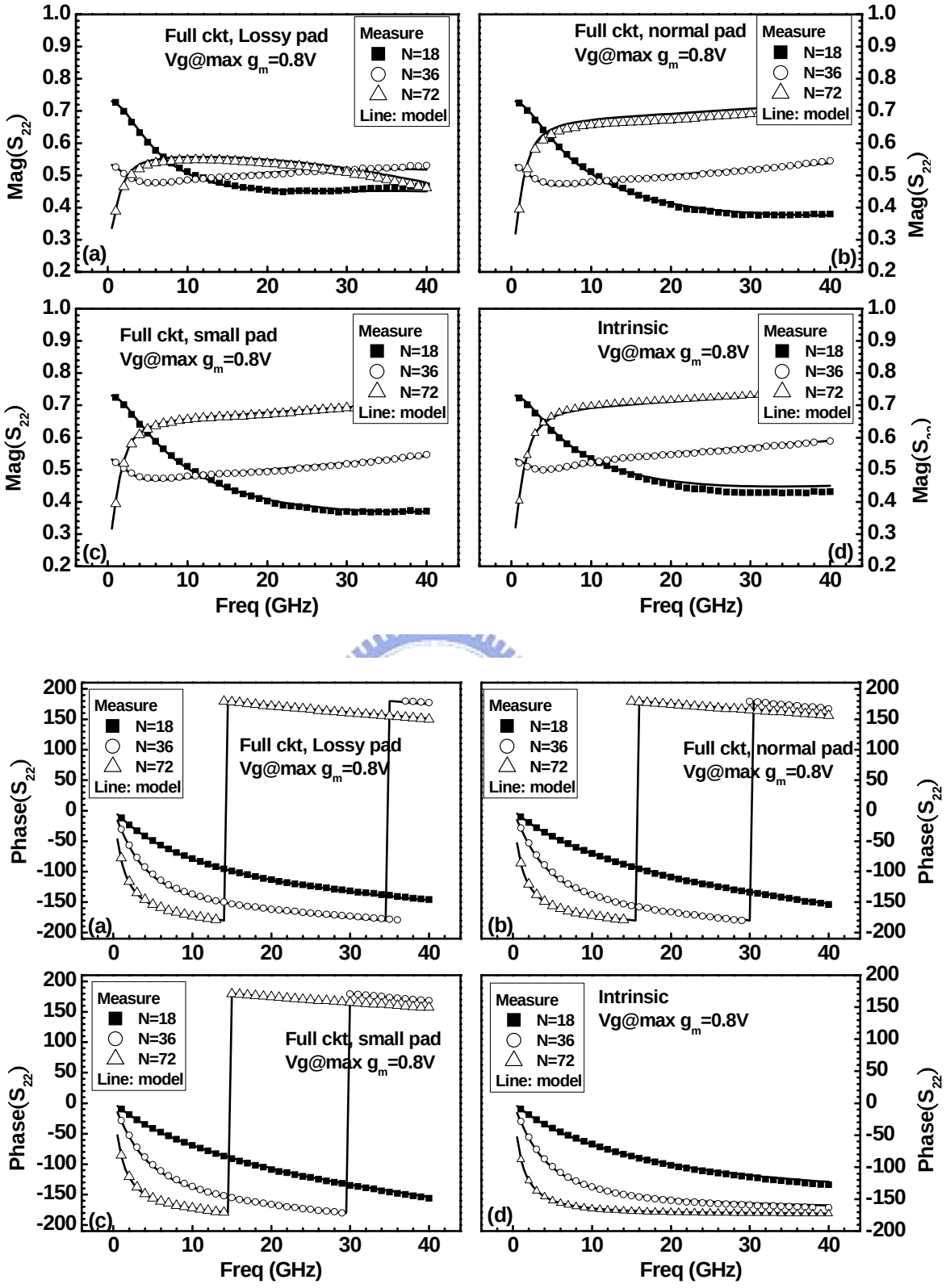

Fig. 5.5.Comparison of measured and simulated S_{22} by full circuit model for 100nm NMOS(N_F=18,36,72) adopting 3 different pads,(a)lossy pad (b)normal pad (c)small pad (d)intrinsic S_{22} by pad de-embedding

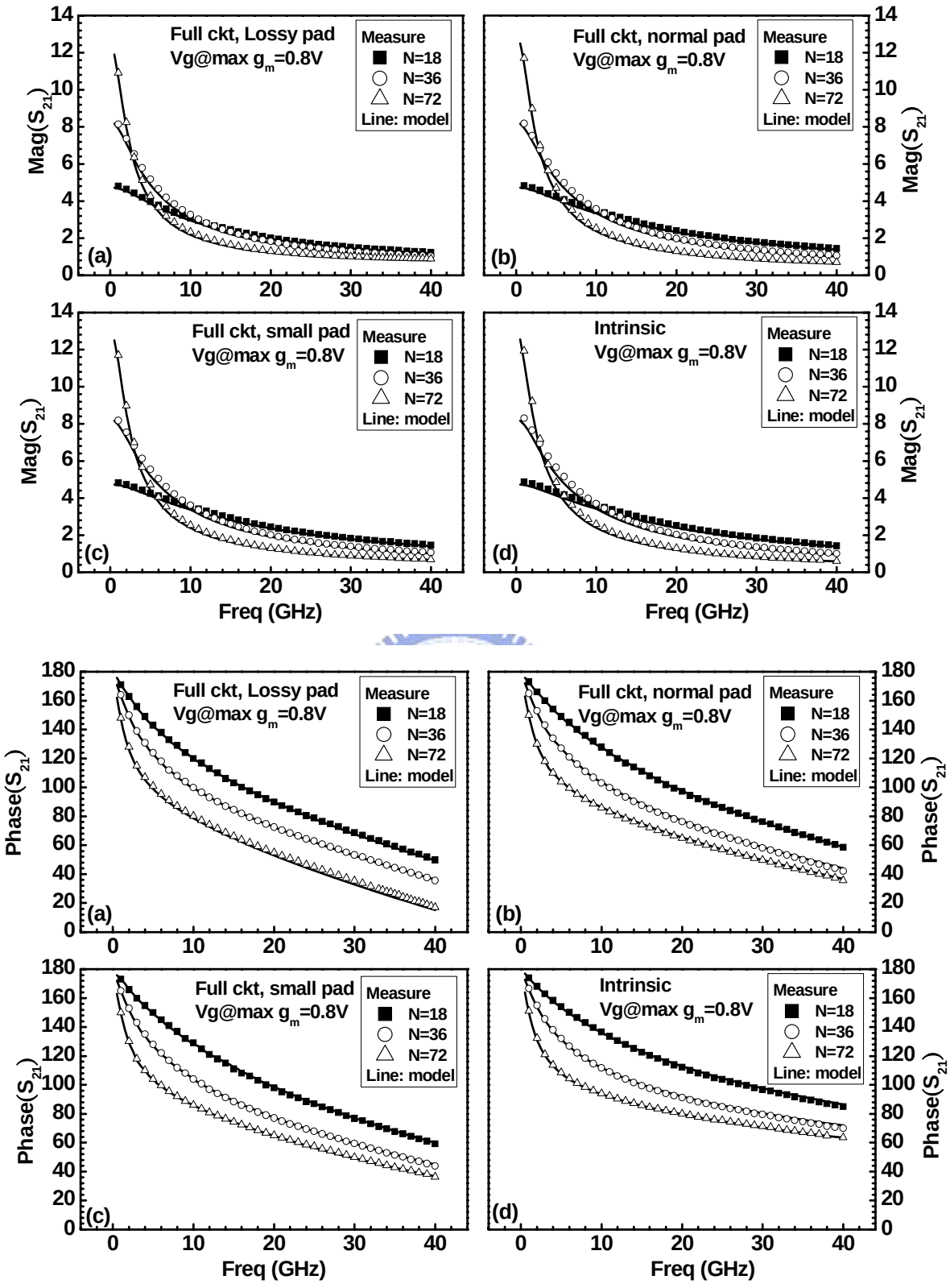

Fig. 5.6.Comparison of measured and simulated S_{21} by full circuit model for 100nm NMOS(N_F=18,36,72) adopting 3 different pads,(a)lossy pad (b)normal pad (c)small pad (d)intrinsic S_{21} by pad de-embedding

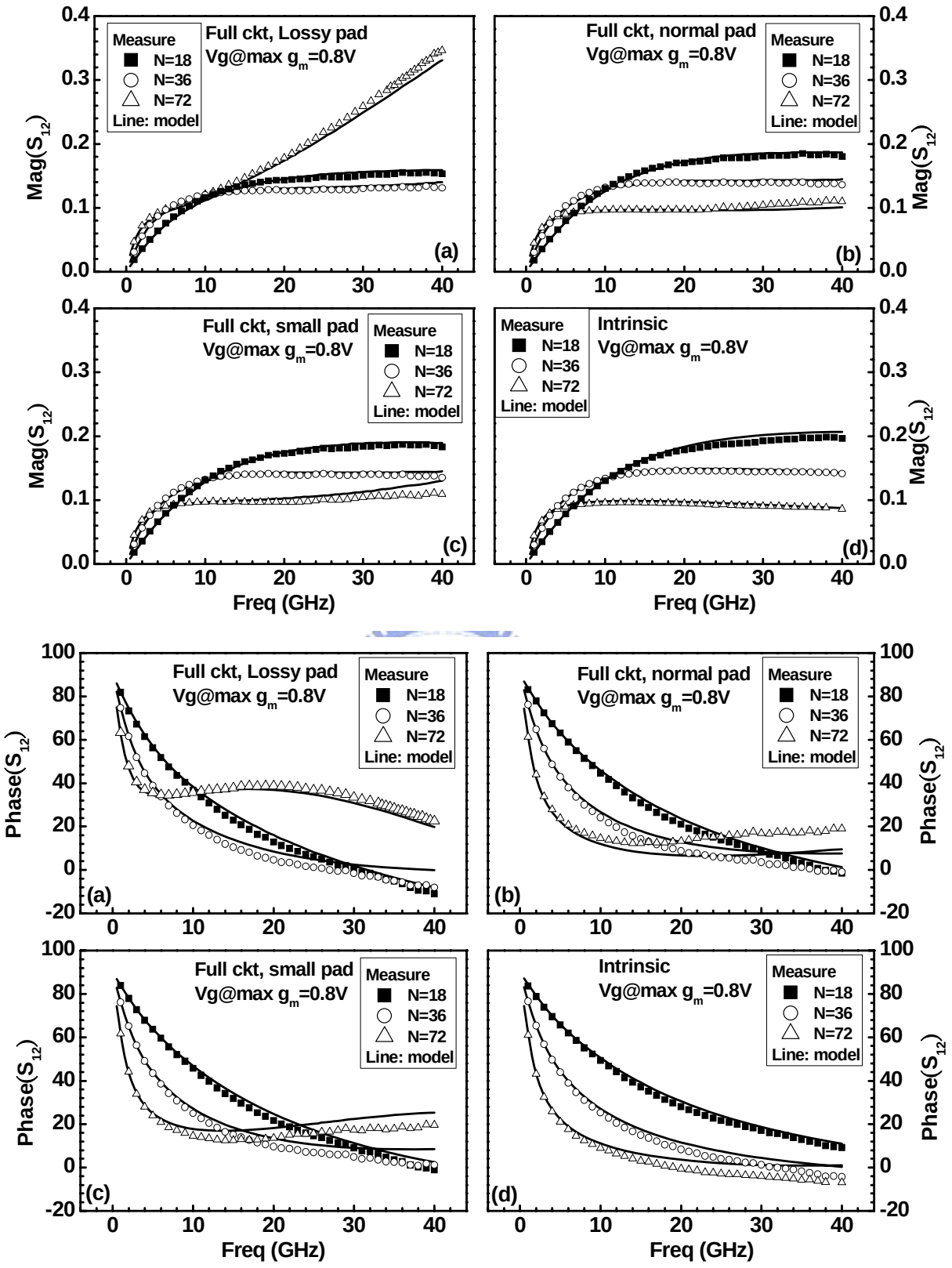

Fig. 5.7.Comparison of measured and simulated S_{12} by full circuit model for 100nm NMOS(N_F=18,36,72) adopting 3 different pads,(a)lossy pad (b)normal pad (c)small pad (d)intrinsic S_{12} by pad de-embedding

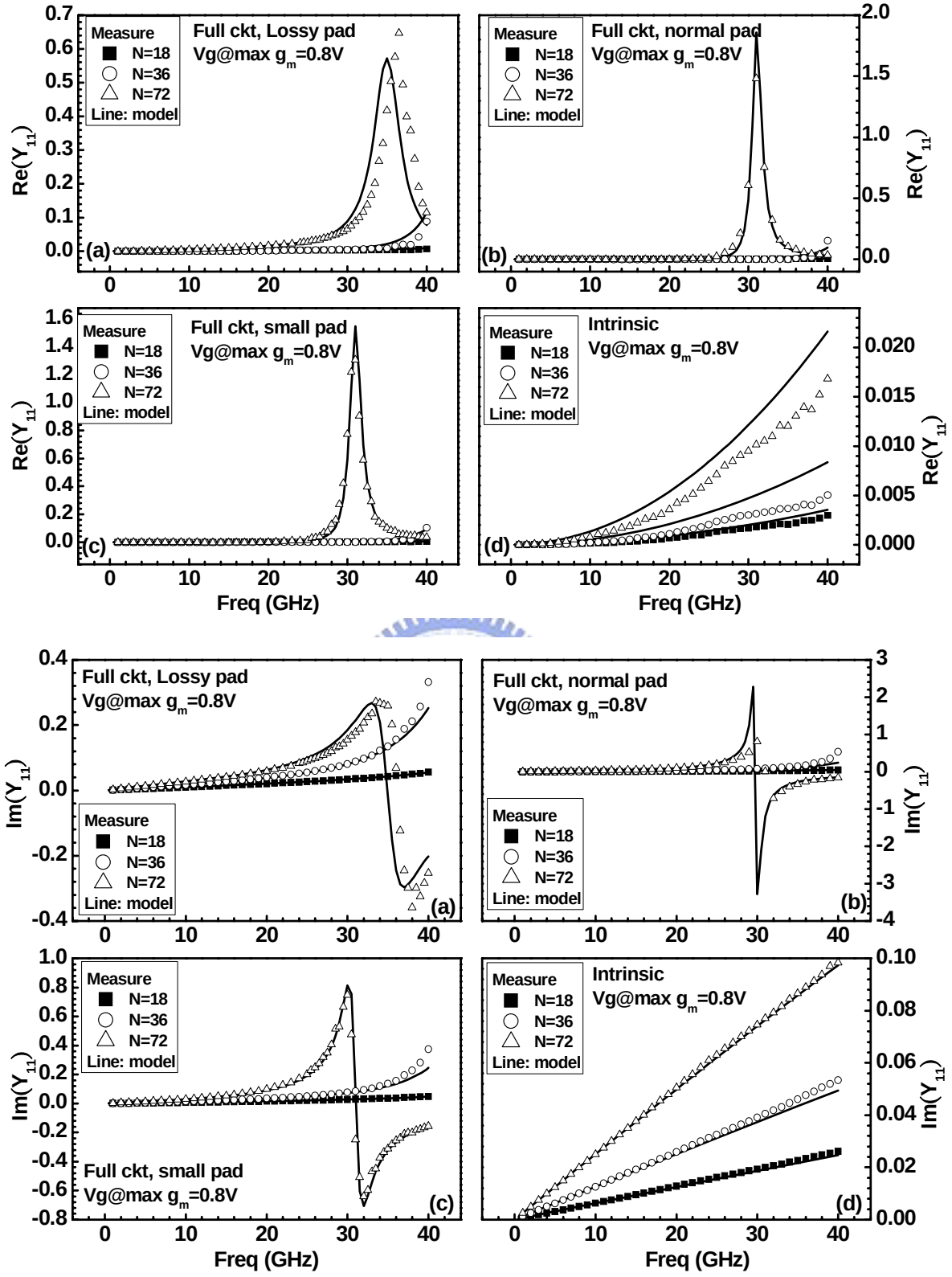

Fig. 5.8.Comparison of measured and simulated Y_{11} by full circuit model for 100nm NMOS(N_F=18,36,72) adopting 3 different pads,(a)lossy pad (b)normal pad (c)small pad (d)intrinsic Y_{11} by pad de-embedding

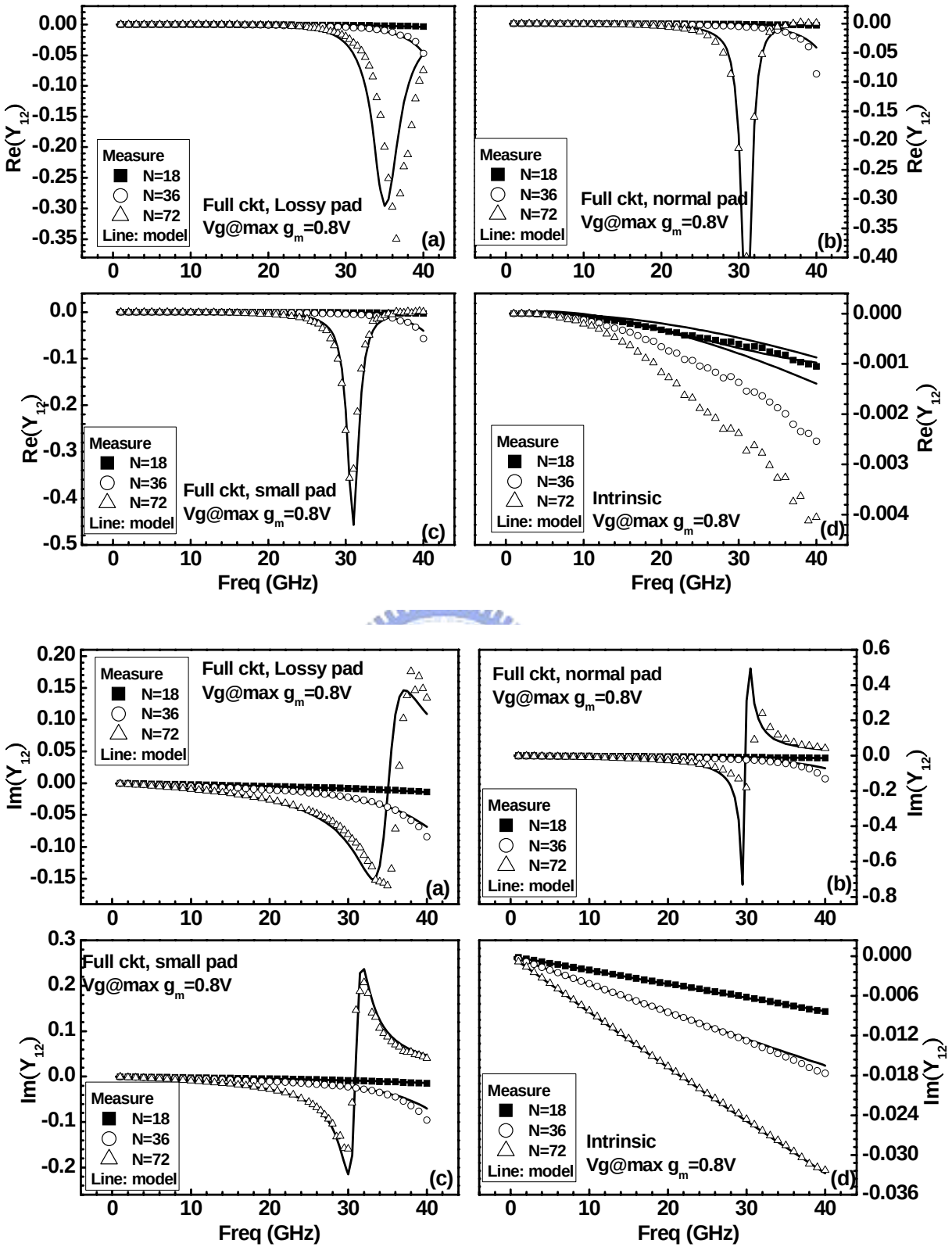

Fig. 5.9.Comparison of measured and simulated Y_{12} by full circuit model for 100nm NMOS(N_F=18,36,72) adopting 3 different pads,(a)lossy pad (b)normal pad (c)small pad (d)intrinsic Y_{12} by pad de-embedding

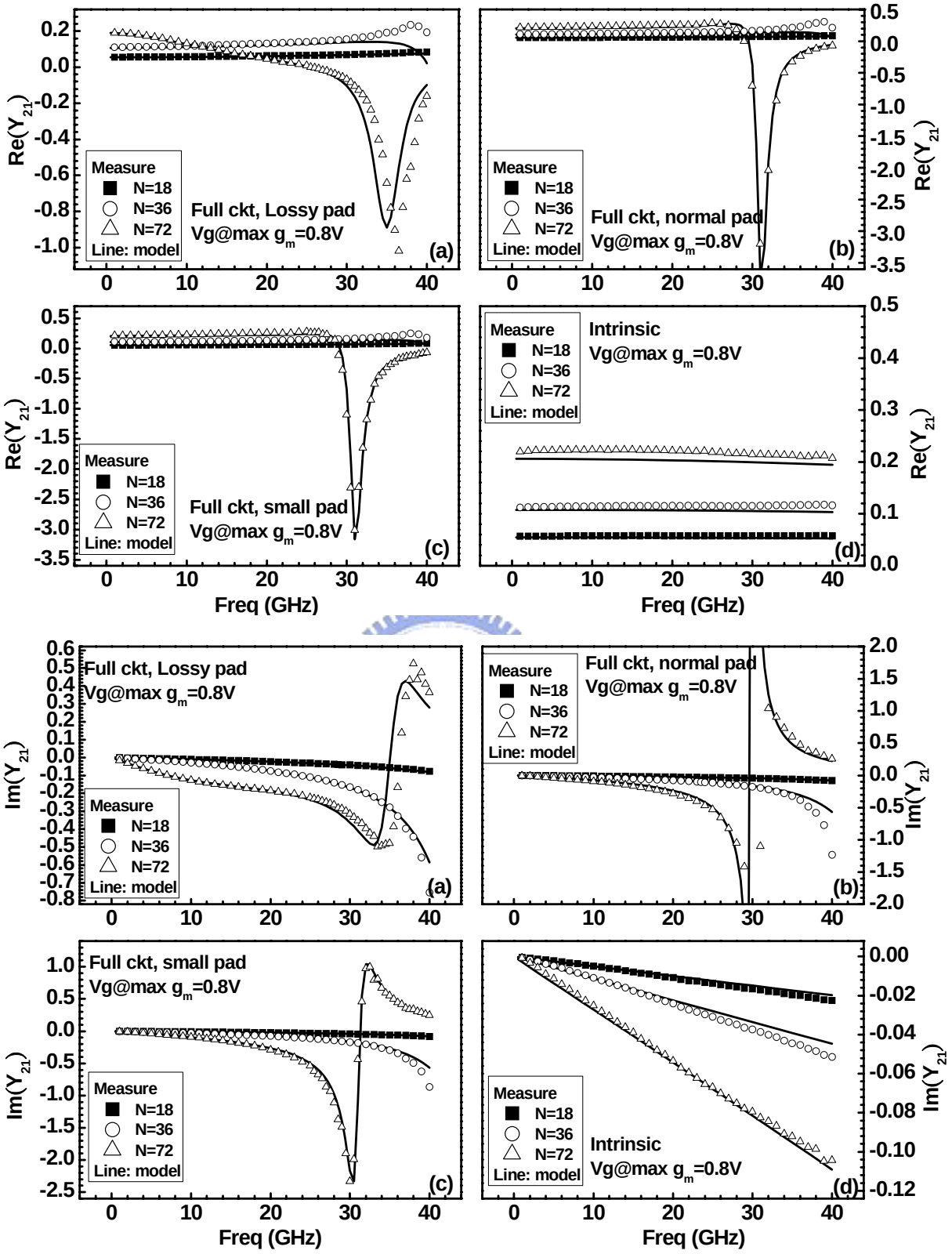

Fig. 5.10.Comparison of measured and simulated Y_{21} by full circuit model for 100nm NMOS(N_F=18,36,72) adopting 3 different pads,(a)lossy pad (b)normal pad (c)small pad (d)intrinsic Y_{21} by pad de-embedding

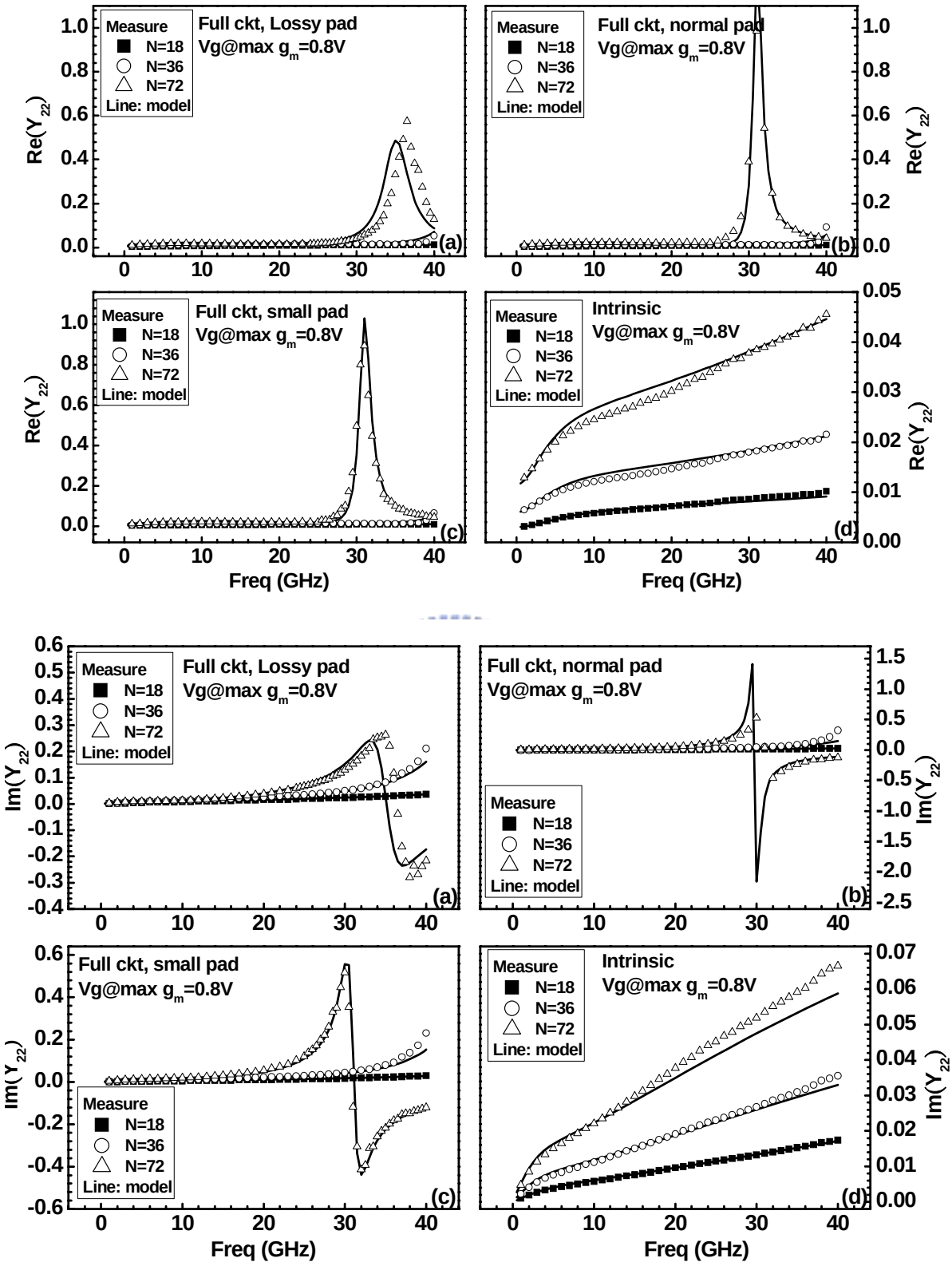

Fig. 5.11.Comparison of measured and simulated Y_{22} by full circuit model for 100nm NMOS(N_F=18,36,72) adopting 3 different pads,(a)lossy pad (b)normal pad (c)small pad (d)intrinsic Y_{22} by pad de-embedding

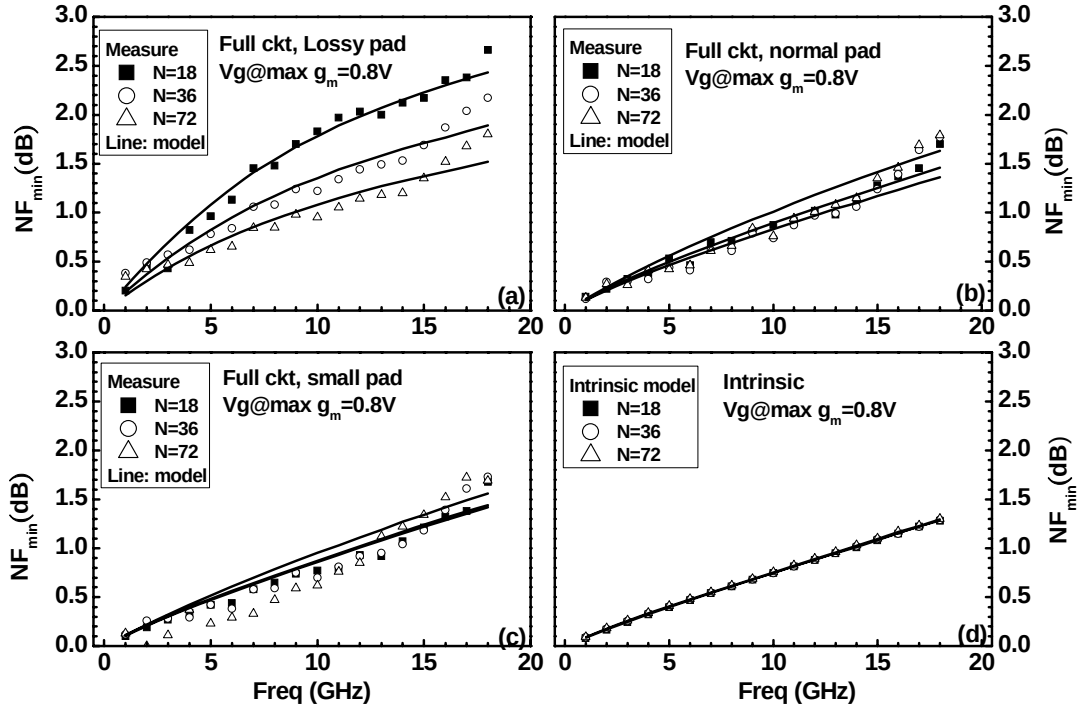

Fig. 5.12. Comparison of measured and simulated NF_{min} by full circuit model for 100nm NMOS(N_F=18,36,72) adopting 3 different pads,(a)lossy pad (b)normal pad (c)small pad (d)intrinsic NF_{min} by lossy substrate de-embedding

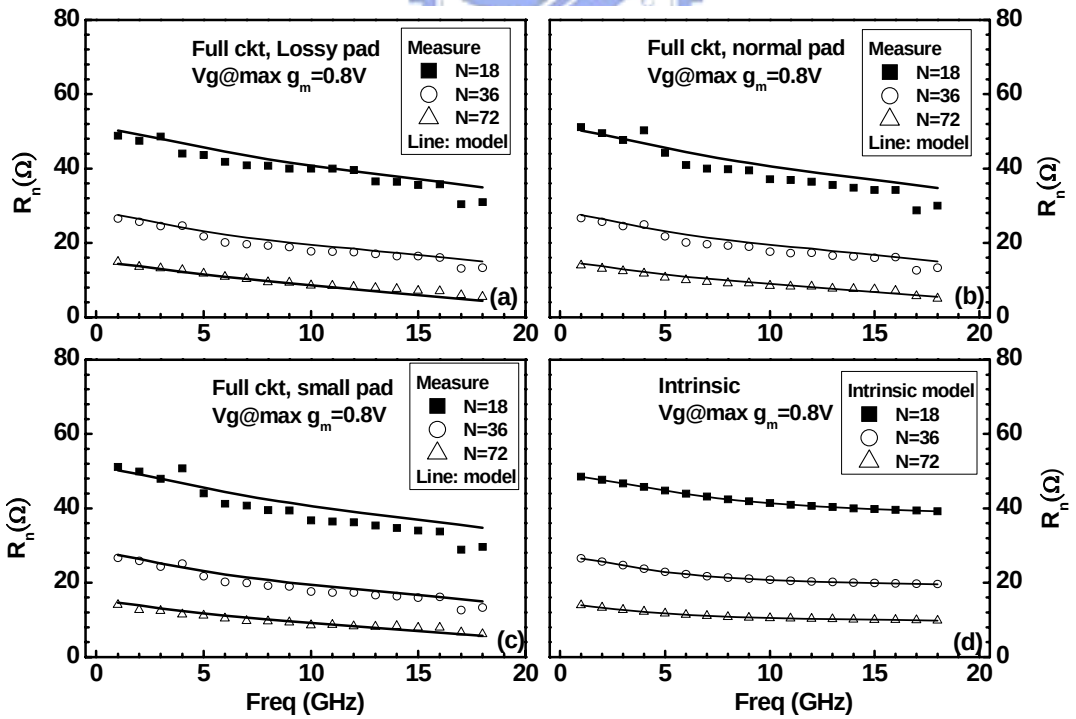

Fig. 5.13. Comparison of measured and simulated R_n by full circuit model for 100nm NMOS(N_F=18,36,72) adopting 3 different pads,(a)lossy pad (b)normal pad (c)small pad (d)intrinsic R_n by lossy substrate de-embedding

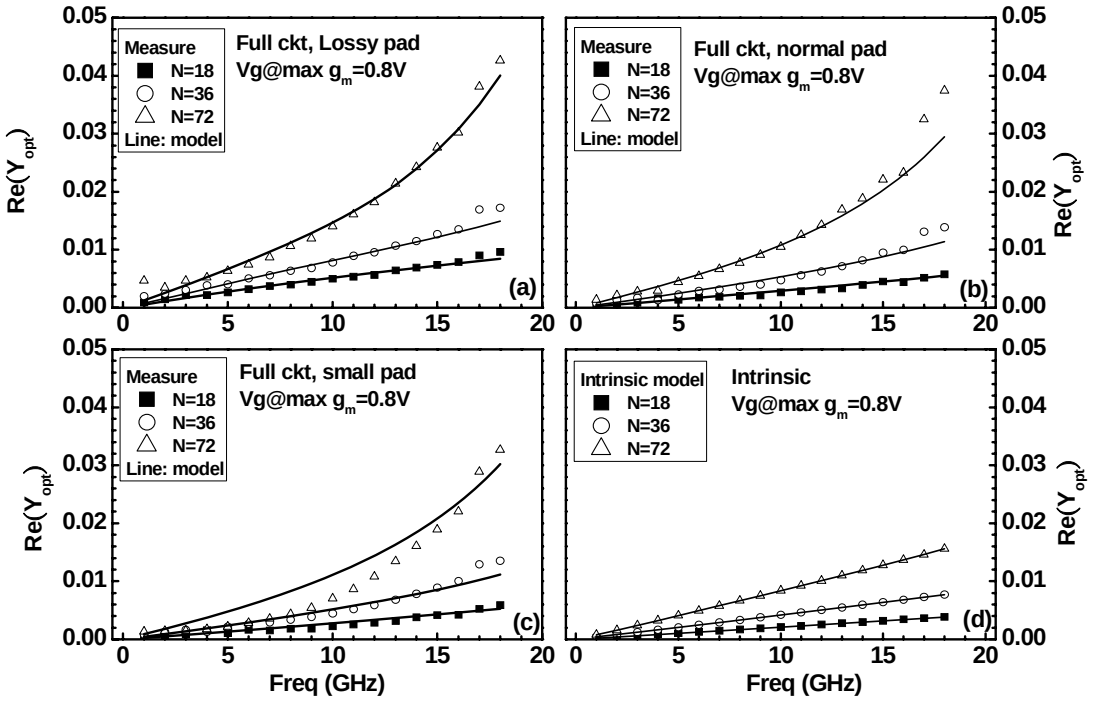

Fig. 5.14. Comparison of measured and simulated $Re(Y_{opt})$ by full circuit model for 100nm NMOS(N_F=18,36,72) adopting 3 different pads,(a)lossy pad (b)normal pad (c)small pad (d)intrinsic $Re(Y_{opt})$ by lossy substrate de-embedding

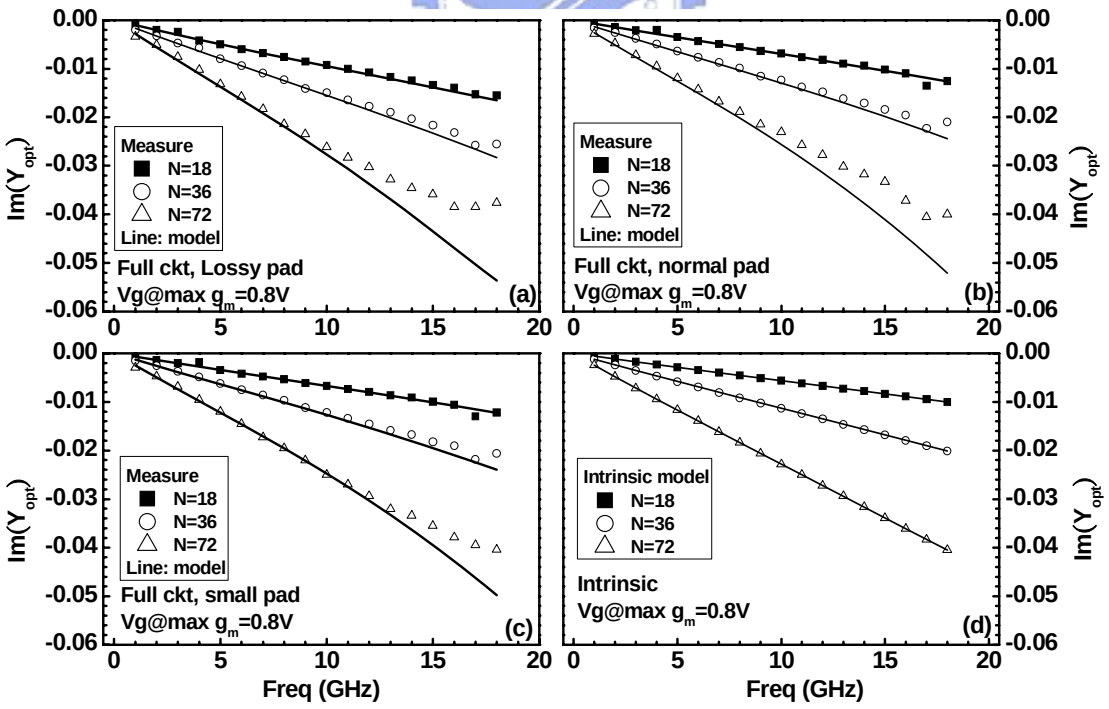

Fig. 5.15. Comparison of measured and simulated $Im(Y_{opt})$ by full circuit model for 100nm NMOS(N_F=18,36,72) adopting 3 different pads,(a)lossy pad (b)normal pad (c)small pad (d)intrinsic $Im(Y_{opt})$ by lossy substrate de-embedding

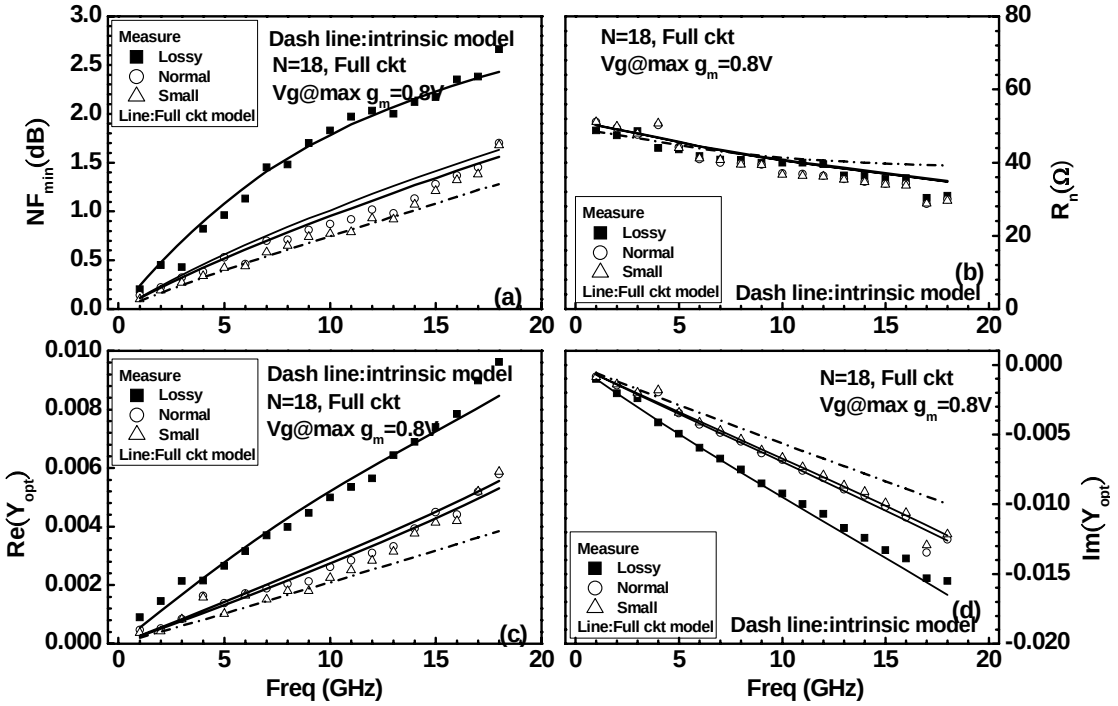

Fig. 5.16.Measured and simulated four noise parameters for 100nm NMOS by full circuit model of lossy,normal,small pads and comparison with intrinsic ones after lossy substrate de-embedding,N_F=18 (a) NF_{min}, (b)R_n, (c)$Re(Y_{opt})$,(d)$Im(Y_{opt})$

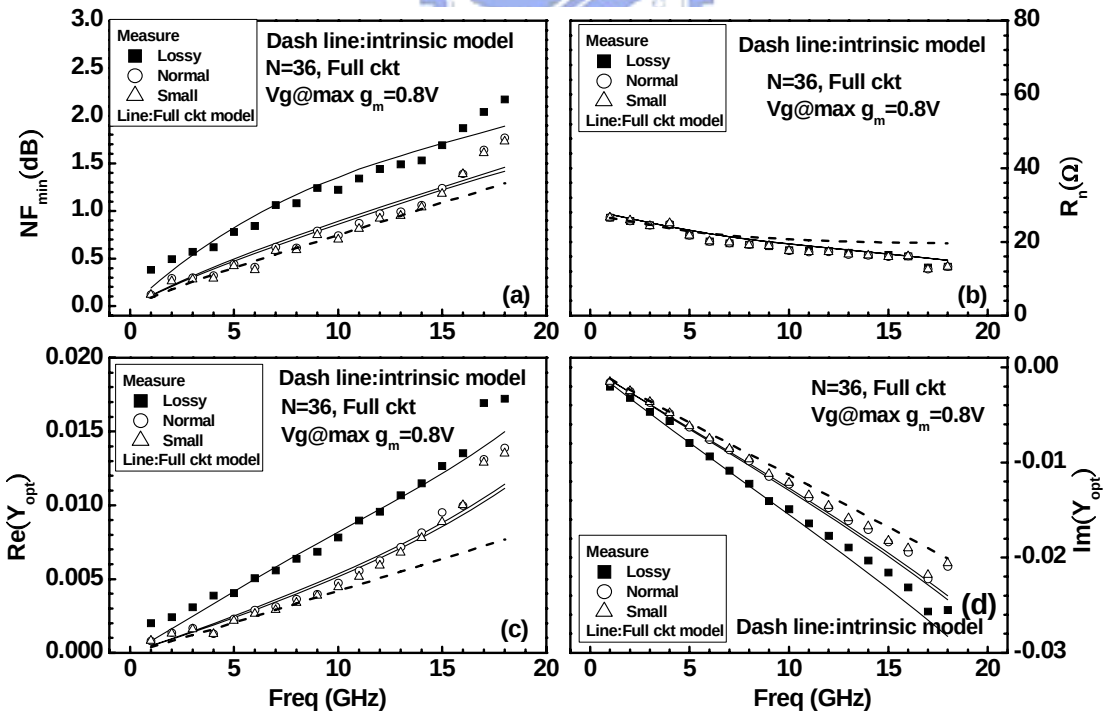

Fig. 5.17.Measured and simulated four noise parameters for 100nm NMOS by full circuit model of lossy,normal,small pads and comparison with intrinsic ones after lossy substrate de-embedding,N_F=36 (a) NF_{min}, (b)R_n, (c)$Re(Y_{opt})$,(d)$Im(Y_{opt})$

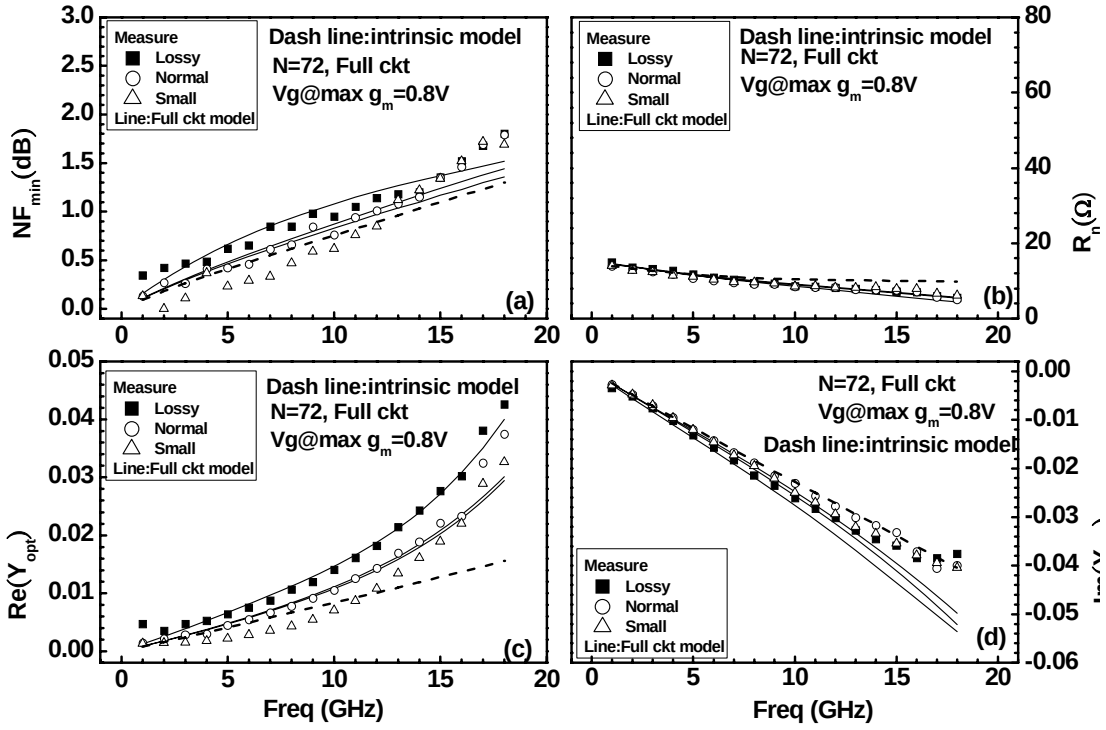

Fig. 5.18.Measured and simulated four noise parameters for 100nm NMOS by full circuit model of lossy,normal,small pads and comparison with intrinsic ones after lossy substrate de-embedding,N_F=72(a) NF_{min}, (b)R_n, (c)$Re(Y_{opt})$,(d)$Im(Y_{opt})$

Chapter 6

Conclusion

6.1 Summary

A broadband and scalable lossy substrate model has been developed and validated by 100nm RF MOSFET with various finger numbers and adopting deferent GSG pads. The broadband accuracy is justified by good match with measured S- and Y- parameters up to 40 GHz as well as noise parameters up to 18 GHz. The scalability is proven by accurate prediction for RF MOSFETs with various fingers numbers in conjunction with lossy, normal and small pads. The enhanced lossy substrate model can be easily deployed in circuit simulator and is useful to improve RF circuit simulation accuracy for low noise design.

6.2 Future Work

The future work following this thesis is the development of a complete compact RF MOSFET model for low power and low noise RF circuit simulation and design. Subthreshold region model with proven accuracy in I-V, C-V, and noise characteristics is indispensable for ultra-low power design. Four port MOSFETs to enable dynamic body bias is a new approach to attain low power and high speed simultaneously.

6.2.1 Low Noise Measurement and Modeling :

The established lossy substrate model and lossy substrate de-embedding method have been extensively verified and justified by nanoscale devices adopting various pad structures. Further research works to be done will cover two major subjects : one is on-chip noise shielding methods to measure truly intrinsic device noise without resort to de-embedding and another one is a broadband and fully scalable lossy substrate model for nanoscale RF MOSFET noise extraction and simulation with broad freedom in pad and interconnect layouts.

We will also extend our effort to several interesting and challenging topics like short channel effect on channel noise, substrate network effect, noise model valid in subthreshold region, and dynamic body biasing effect for low noise, low power and high speed design through 4T and 4-port device implementation. The ultimate goal for us to realize through future-project supported by 90nm low power CMOS process is to assure on-Si-chip noise simulation accuracy and to facilitate low noise, low power and broadband RF circuit design.

6.2.2 Ultra-low power RF CMOS design

The advancement of CMOS technology to nanoscale era can offer miniaturized devices of higher speed at even lower voltage. It is really a very attractive solution for low power and low cost RF integrated circuit (IC) development. However, the tradeoff among various RF performance parameters such as bandwidth, linearity, gain, power, and noise becomes an important reality to be considered. For cable-free body monitoring with μW biomedical acquisition devices, a sub-mW wireless transceiver is required for long-term observation. However the power consumption is a critical issue, and how to reduce the active and standby leakage power in the circuit is a big challenge. Therefore, the demand for ultra-low power circuit design increases rapidly.

To meet the stringent requirements for ultra-low power design, new device and/or circuit techniques become increasingly important to corporate with technology scaling to realize leakage reduction and maintain performance simultaneously. A future work with interest in new device configuration with new bias schemes for ultra-low power design will be one of research topics worthy of continuous effort.

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Appendix A [24]

The Y-Factor Method and Noise Figure Correction

In noise figure measurement, total output noise power measured is

$$N_o = N_a + GN_i = N_a + kTBG \tag{A-1}$$

where N_o and N_i represent the noise levels available at the output and input respectively, G is the gain of the DUT, B is the bandwidth, k is Boltzmann's constant, and T is the absolute temperature.

To determine N_a, output noise power corresponding to two source temperatures are needed. Two output noise power and two source temperatures determine the slope kBG and intercept N_a. A diode based noise source in the on-state (hot) generates noise when it is reverse biased into avalanche breakdown. Thus the equivalent noise temperature will be higher than its "off-state" (cold). Temperature difference is expressed by excess noise ratio (ENR)

$$ENR_{dB} = 10\log\left(\frac{T_h - T_c}{T_0}\right) \quad , \quad ENR = 10^{\frac{ENR_{dB}}{10}} \tag{A-2}$$

Y-factor is defined as the output noise ratio

$$Y = \frac{N_1}{N_2} \tag{A-3}$$

Derivation is shown as follows:

$$N_1 = N_a + kT_cBG \quad , \quad N_2 = N_a + kT_hBG$$
$$ENR = 10^{\frac{ENR_{dB}}{10}} = \frac{T_h - T_c}{T_0} \tag{A-4}$$
$$Y = \frac{N_2}{N_1} = \frac{N_a + kT_hBG}{N_a + kT_cBG}$$

In practice, T_c is assumed to be 290K when it is calibrated. This leads to

$$
\begin{aligned}
(Y\text{-}1)N_a &= kBG(T_h - YT_0) \\
&= kBG(T_0 \cdot ENR + T_0 - Y \cdot T_0) \\
&= kT_0BG(ENR + 1 - Y) \qquad \text{(A-5)}
\end{aligned}
$$

$$\Rightarrow$$

$$N_a = kT_0BG\left(\frac{ENR}{Y\text{-}1} - 1\right)$$

From the derived N_a, the total noise factor measured can be calculated.

$$F_{tot} \equiv \frac{N_a + GN_i}{GN_i} = \frac{kT_0BG\left(\frac{ENR}{Y\text{-}1} - 1\right) + GkT_0B}{GkT_0B} = \frac{ENR}{Y\text{-}1} \qquad \text{(A-6)}$$

Because only the noise factor of the DUT is interested, removal of the noise contributed from the second stage is essential. Based on the noise factor analysis of multi-stage system, total noise factor of a two-stage system is

$$F_{tot} = F_1 + \frac{F_2 - 1}{G_1} \qquad \text{(A-7)}$$

where F_1, F_2 and G_1 are noise factor of 1st stage, 2nd stage and gain of 1st stage respectively.

Noise factor of the instrument (F_2) can be characterized while doing system calibration and gain of the DUT (G) will be obtained while measuring S-parameters before noise measurement. Therefore corrected noise factor is obtained

$$F_1 = F_{tot} - \frac{F_2 - 1}{G_1} \qquad \text{(A-8)}$$

then is used to construct the noise equation.

Appendix B

Modified Open-Short De-embedding

Open and short pads were conventionally used to de-embed parallel parasitic admittance and series parasitic impedance respectively. The de-embedding procedure is shown as follows:

$$Y_{m\_de\_o} = Y_m - Y_o \tag{B-1}$$

$$Y_{s\_de\_o} = Y_s - Y_o \tag{B-2}$$

$$Z_{int} = (Y_{m\_de\_o})^{-1} - (Y_{s\_de\_o})^{-1} = (Y_m - Y_o)^{-1} - (Y_s - Y_o)^{-1} \tag{B-3}$$

$$Y_{int} = (Z_{int})^{-1} \tag{B-4}$$

where

Y_m = measured Y parameter of DUT

Y_o = measured Y parameter of open pad

Y_s = measured Y parameter of short pad

Y_{int} = intrinsic Y parameter after open/short de-embedding

Equivalent circuits of test structure with DUT, open pad and short pad are given in Fig. B.1~Fig. B.3. According to these equivalent circuits, following expression holds

$$Y_o = \begin{pmatrix} Y_{p1}+Y_{p3} & -Y_{p3} \\ -Y_{p3} & Y_{p2}+Y_{p3} \end{pmatrix} \tag{B-5}$$

$$Z_{s\_de\_o} = (Y_{s\_de\_o})^{-1} = Y_s - Y_o = \begin{pmatrix} Z_{s1}+Z_{s3} & Z_{s3} \\ Z_{s3} & Z_{s2}+Z_{s3} \end{pmatrix} \quad \text{(B-6)}$$

In this de-embedding process, based on Fig. B.3, short pad does not see a parasitic admittance Y_{p3} because all the interconnection metals are shorted at the same potential. De-embedding procedure (B-2) may introduce an over-de-embedding error because Y_{p3} was deducted from Y_s in which Y_{p3} does not exist. Therefore step (B-2) was modified as given below and keeps the rest of the steps the same.

$$Y_{s\_de\_o} = Y_s - \begin{pmatrix} Y_{11}+Y_{12} & 0 \\ 0 & Y_{22}+Y_{21} \end{pmatrix} \quad \text{(B-7)}$$

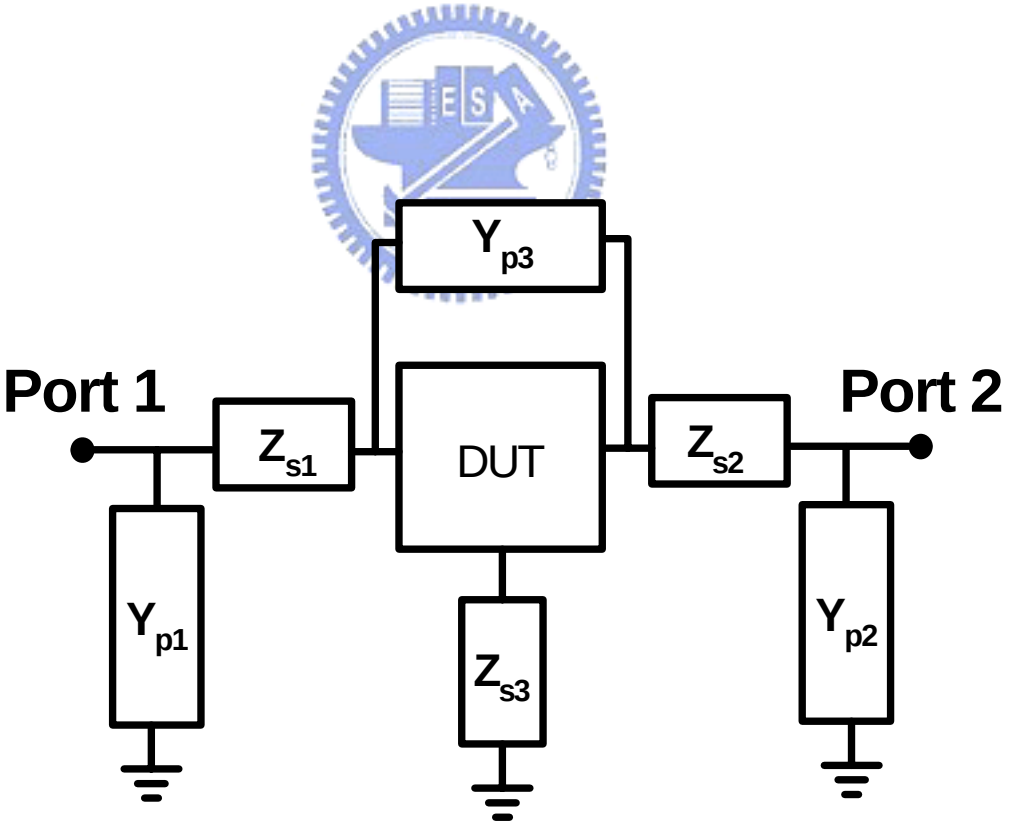

Fig. B.1 Equivalent circuit of test structure with DUT

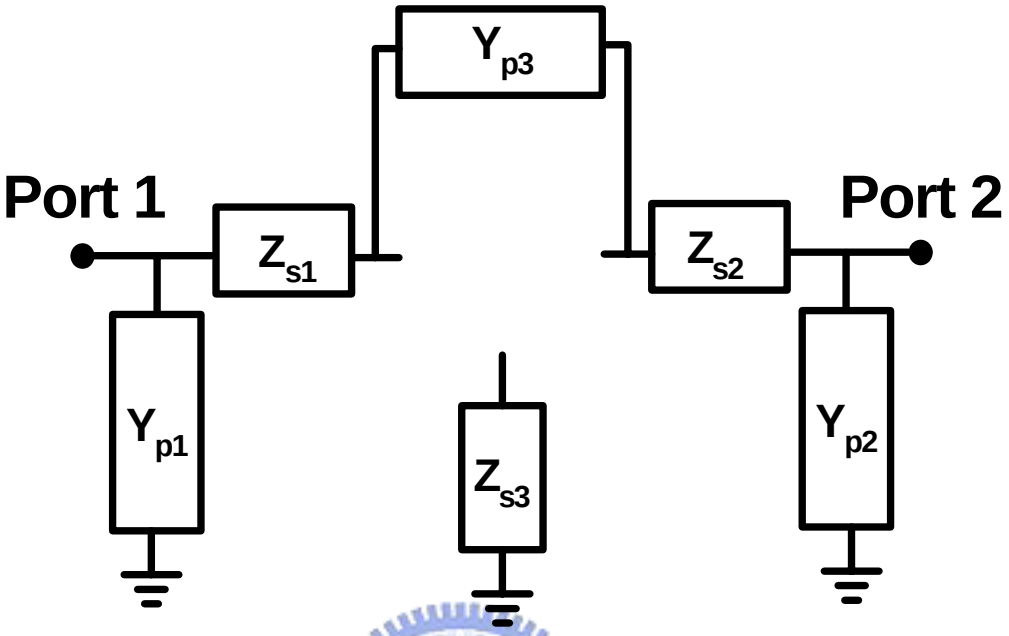

Fig. B.2 Equivalent circuit of open pad

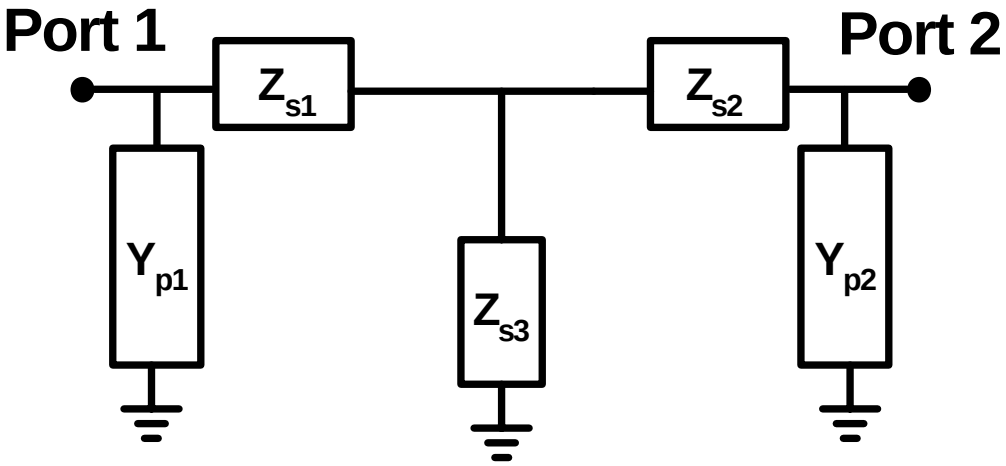

Fig. B.3 Equivalent circuit of short pad

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