國 立 交 通 大 學

電子工程學系　電子研究所碩士班

碩 士 論 文

氟摻雜對二氧化鉿堆疊式閘極P型金氧半場效電晶體其可靠性的影響

Effect of Fluorine Incorporation on the Reliability Issue of pMOSFETs with HfO2/SiON Gate Stack

研 究 生：王信智

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研 究 生：王信智　　Postgraduate：Hsin Chih Wang

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羅正忠　博士　　Dr. Jen-ChungLou

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摘要

根據半導體積體電路的微縮定理,極薄的二氧化矽介電質層(1 至 1.5 奈米)將遭遇量子穿遂效應的問題而導致極大的洩電流,導致元件可靠度上的問題。近年來使用高介電質材料來取代傳統以二氧化矽當介電質層已廣泛被研究。相較於二氧化矽,由於在相同的等效厚度之下高介電質物質有較厚的實際厚度,因此可以抵擋因量子的穿遂效應而導致的大量漏電。然後,以高介電質材料當閘極介電質層卻遭遇到其它的問題。例如:相對於二氧化矽操作在相同電壓下,高介電質材料有較高的界面狀態產生及較多的電荷捕捉,這對於元件操作時臨限電壓的漂移有較嚴重的影響。

在 P 型金氧半場效電晶體中,負偏壓溫度不穩定效應是主要的問題。我們於

閘極介電質沈積前,以離子佈值的方式植入氟摻雜,使氟原子在後續的高溫摻雜活化的過程中,使其擴散至通道和閘極介電質層。利用氟的摻入,我們深入的探討氟對二氧化鉿/氮氧化矽閘極之 P 型金氧半場效電晶體對於負偏壓溫度不穩定效應的影響。我們發現,摻雜氟對於元件的基本特性,沒有顯著的降級。但對於固定電壓應力(CVS)以及負偏壓-溫度應力(NBTS)量測時,含氟摻雜的元件有較低的界面狀態產生,和較少的電荷捕捉,對於元件的可靠度和穩定性有明顯的改善,因此改善了以高介電質材料為閘極介電極層的穩定性和可靠性。

Effect of Fluorine Incorporation on the Reliab ility Issue of pMOSFETs with HfO2/SiON Gate Stack

Student : Hsin Chih Wang **Advisor : Dr. Chin-Fa Yeh**

Dr. Jen-ChungLou

Department of Electronics Engineering & Institute of Electronics

National Chiao Tung University

Abstract

According scaling rule, ultra-thin oxide(about 1~1.5nm) will undergo tunneling effect and then cause gate leakage current , which is the issue of the reliability . Recently , high dielectric constant materials are used to replace SiO_2 has widely studied. Compare with SiO_2 at the same equivalent oxide thickness (EOT) , high dielectric constant materials have thicker physical thickness which can resist tunneling effect , and then avoid leakage current . However , using high dielectric constant materials as gate dielectric experience other problems . For example , high dielectric constant materials have higher interfacial states and charge traps , these will cause more serious threshold voltage shift when working device as the same voltage compare with SiO_2 .

In pMOSFETs , negative bias temperature instability is the main issue . We

incorporate F before gate dielectric deposition via channel implantation technique, which was subsequently diffused into the gate stack during annealing process . By fluorine incorporation , we discuss the effects of negative bias temperature instability (NBTI) of F incorporated in pMOSFETs with HfO_2/SiON stack in depth . We found that F incorporated improves the fundamental electrical properties of the fabricated transistors . In addition , under constant voltage stress (CVS) and negative bias temperature stress (NBTS) , we found that lower generation rate of interface states and charge trapping are observed for device with F incorporation , thus enhances the reliability and the stability of high-k devices.

致謝

在二年的努力下,此篇碩士論文才能順利完成,有相當多的人要感謝。首先,要感謝我的指導教授葉清發博士和羅正忠博士,在二年的指導讓我學習到很多做研究的方法以及為人處世的方法。其次要感謝實驗室的學長們,打從心裡感謝永裕學長在口試前給的建議、伯翰學長教導量測的方法以及做實驗的方法、柏村學長為實驗室爭取資源。再者,感謝帶我玩遍新竹的慧敏、世璋學長、湯尼伯、很堅持己見的德安、愛走天涯的智仁、生氣來很嚇人的正凱、打電動不耐煩的大峰、猶豫不決的小天、疼老婆的建宏,以及學弟幸福、佳樺、土豆、鄭元愷、洪晨修、簡嘉宏。最後要感謝我的爸爸王英富、媽媽程錦碧,這二年來的支持。有很多話要說,千言萬語都帶表不了我的謝意。總之,謝謝各位我認識的人。

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Chapter 1

Introduction

1-1 Backgrounds and Motivation

With the developing of the IC (integrated circuit) technology , the rapid shrinking of the metal oxide field effect transistors (MOSFETs) has confronted the channel length and gate dielectric thickness to also decrease rapidly . The research point out that when conventional SiO_2 gate insulator scales to at least 1.0nm~1.5nm , large gate leakage current tunnels from this ultra-thin oxide and then causes the reliability issues . To suppress above , high dielectric constant (high-k) materials has widely investigated [1]. The main reason of using high dielectric constant materials to replace conventional SiO_2 is : under the same equivalent oxide thickness (EOT) , high dielectric constant materials have thicker physical thickness which can avoid gate leakage current generating .Therefore , we will require high-k gate dielectrics to seek the specification in ITRS (Table 1-1) [2] in terms of sufficiently low gate leakage combined with ultra-thin equivalent oxide thickness (<1nm)

There are several high-k dielectrics have studied in recent . Hafnium oxide (HfO_2) is considered as one of the most promising candidates , since its thermal stability in contact with silicon (47.6Kcal/mole at 727℃) compared to TiO_2 and Ta_2O_5 , high permittivity (k~25~30 for HfO_2) compared to Si3N4 and Al2O3 , a large band gap

5.6eV with band offsets to silicon >1.5eV , appropriate barrier high for both electrons and holes (> 1eV) , and compatible with poly-silicon . However , there are still a number of pending issues when high-k dielectrics are liable applied in future technology nodes , including high density of traps in the bulk dielectric and interfacial layer which will cause mobility degradation and threshold voltage instability . Therefore , how to improve bulk traps and interfacial traps is our goal . Except this , the reliability of high-k dielectrics is need to be understand in order to introduce to CMOS technology .

Abundant literatures have been published about the methods of incorporating nitrogen [3-4] or Si [5-6] into Hf-based films/stack in order to improve the film quality. Recently, some literatures have also incorporated fluorine into different high-k gate dielectrics by different ways [7-8-9]. The results reveal the breakthrough of device reliability and performance are indeed improved . In this thesis, fluorine are incorporated into HfO_2/SiON gate stack via channel implantation before gate dielectric growths, and its impact on the pMOSFETs are studied . It was clearly seen that the degradation is improved in the F-incorporated sample. More importantly , we also found less shift of threshold voltage under CVS (constant voltage stress) and NBTS (negative bias temperature stress) in this sample. We believe it has the potential to be an industrial standard if ALCVD HfO_2 is the final selection of future

dielectric of the ULSI industry .

1-2 Organization of This Thesis

In this chapter, we introduce the reason of the high-k dielectrics on CMOS technology and systematic discuss the effect of fluorine incorporating on pMOSFETs with HfO_2/SiON gate stack.

In chapter 2 , we describe the process flow for fabricating pMOSFETS test devices with HfO_2/SiON gate stack . We will show some basic electrical characteristics with and without fluorine incorporation, split C-V to obtain mobility , charging pumping to verify the amount of interface states and carrier separation to gain leakage current mechanisms .

In chapter 3, we discuss the reliability issues such as constant voltage stress (CVS) , negative bias temperature stress (NBTS) of the devices with and without fluorine incorporation .

In chapter 4 , we conclude the result and important discovery in this research . Some suggestion for future work about fluorine incorporating is given .

Years of Production	2005	2006	2007	2008	2009	2010	2011
EOT (Physical) for High –performance(nm)	1.2	1.1	1.1	1.0	0.9	0.65	0.5
Electrical thickness adjustment for gate depletion and inversion layer effects (nm)	0.73	0.74	0.74	0.7	0.7	0.27	0.25
Nominal gate leakage current density limit (at 25℃) (A/cm^2)	188	536	800	1180	1100	1560	2000

Table 1-1 2005 ITRS roadmap

Manufacturable solutions, and are being opitimized.

Manufacturable solutions are known.

Manufacturable solutions are not known.

Chapter 2

Electrical Characteristics of Fluorine Incorporation on pMOSFETs with HfO_2/SiON Gate Stack

2-1 Introduction

Fluorine incorporation in silicon dioxide gate dielectrics has widely studied in 1980s. The research pointed out that fabrication of transistors with fluorine-enriched oxide will not show degradation as long as the concentration is sufficiently low. The research also found fluorine have caused an improvement in interfacial properties [10].

In high-k dielectrics we faced high defect density in the bulk of high-k gate dielectric and interfacial state in the gate stack structure are major reasons for V_{th} instability and mobility degradation [11]. Recently, the research of fluorine incorporation into CMOS has studied in high-k gate dielectrics with different methods , such as channel implantation [9] , gate implantation [7] and UV-F_2 [8]. They indicated that fluorine piles up in the bulk of dielectric, but excessive amount of fluorine ions are present in the dielectric will increase the leakage current [12].

In this chapter, we compared with electrical characteristics for pMOSFETs with and

without fluorine incorporation, which was implemented by channel implantation. We found the 5E13cm^{-2} sample doesn't cased severe damage while channel implantation compared with the non-fluorine sample. On the contrary, it make the electrical characteristics better like mobility enhancement and driving current increase without serious leakage current.

2-2 Experiment

2-2.1 Experimental Procedure

Standard local oxidation of silicon (LOCOS) process was applied to devices isolation. The pMOSFETs were fabricated on 6-inch p-type (100) Silicon wafer utilizing conventional self-align process. After LOCOS was made and then fluorine (5E13cm^{-2}) was incorporated by ion implantation, the schematic diagram is shown in Fig. 2-1, which to see if fluorine affects device performance and reliability compared with control sample (non-fluorine). After stripping sacrificial oxide by dipping in HF solution for seven minutes, standard RCA clean was used to remove the organics, particles and metal contamination. Immediately, a thin interfacial layer SiON was formed by Horizontal Furnace at 800℃ in NH_3 and O_2 ambient in order to avoid negative oxide growing before depositing high-k dielectric and decrease leakage current. The SiON film was about 0.7nm~0.11nm, which was measured by ellipsometer. And then 3nm HfO_2 film was deposited by ALCVD, following by RTA

at 600℃ for 30s in N_2 ambient to improve the quality of high-k dielectrics. A 200nm poly-silicon was deposited by low pressure chemical vapor deposition (LPCVD) . Subsequently, gate electrode was defined by I-line lithography stepper and etched by ECR etching system. After removing sidewall polymer, S/D extension implantation was implemented by B implantation. Spacer formation was carried out by plasma-enhance chemical vapor deposition (PECVD) and then S/D implantation was executed by Boron implantation. After S/D implantation, rapid thermal anneal (RTA) was performed at 950℃ for 20s in N_2 ambient to activate dopants. Afterward, SiO_2 capping layer was deposited by PECVD and contact hole pattering . And Al-Si-Cu metallization was deposited by PVD system and then pattering. Finally, forming gas annealing at 400℃ for 30 minutes in N_2/H_2 ambient .

2-2.1Measurement Setup

Current-voltage (I-V) and capacitance-voltage (C-V) characteristics were evaluated by a HP4156A precision semiconductor parameter analyzer and an HP4284 LCR meter, respectively. The equivalent oxide thickness (EOT) of the gate dielectrics was obtained from high frequency (100 KHz) capacitance-voltage (C-V) curve at strong inversion without considering quantum effect. The main process flow is summarized in Fig. 2-2 and schematic cross section of pMOSFETs with HfO_2/SiON gate stack in Fig. 2-3.

In this thesis, the interface trap density (N_{it}) was analyzed using the charging pumping method. Square-wave waveforms (f=1MHz) which generated from 8110A were applied to the gate, and the base voltage was varied from inversion to accumulation, while keeping the pulse amplitude at 1.5V. Fig. 2-4 shows the configuration of measurement setup used in our charging pumping experiment. A MOSFET with gate area A_G gives the charging pumping current as:

$$I_{cp} = qA_G f N_{it} \qquad (2\text{-}1)$$

The hole mobility for pMOSFETs was obtained by split C-V method. We know that drain current is a combination drift and diffusion currents as follows:

$$I_D = \frac{W u_{eff} Q_n V_{DS}}{L} - W u_{eff} \frac{kT}{q} \frac{dQ_n}{dx} \qquad (2\text{-}2)$$

The effective mobility for pMOSFETs was measured at low drain voltage (about -50mv or -100mv), because then the channel charge is more uniform from source to drain, allowing the diffusive second term as below

$$u_{eff} = \frac{g_d L}{W Q_n} \qquad (2\text{-}3)$$

where the drain conductance g_d is defined as

$$g_d = \frac{\partial I_D}{\partial V_{DS}}\Big|_{V_{GS}} = const.$$

Q_n was direct measured from capacitance measurements. The capacitance meter is connected between the gate and the source/drain connected together with the substrate grounded. Therefore, Q_n was expressed as follows

$$Q_n = \int_{\infty}^{-V_{GS}} C_{GC} dV_{GS} \qquad (2\text{-}4)$$

and the vertical surface electric field ε_{eff}, was expressed as

$$\varepsilon_{eff} = \frac{Q_b + \eta Q_n}{K_s \varepsilon_0} \qquad (2\text{-}5)$$

$$Q_b = \int_{V_{fb}}^{V_{GS}} C_{GB} dV_{GS}$$

where Q_b and Q_n were charge densities (C/cm^2) in the space-charge region and the inversion layer , respectively. The parameter η=1/3 was for hole mobility. We finally can calculate universal mobility by following equation

$$u_{p,eff} = \frac{180}{1 + (\varepsilon_{eff} / 4.5 \times 10^5)} \qquad (2\text{-}6)$$

We can extract mobility, universal mobility , effective field by above equation. Fig. 2-2 is the configure of split-CV measurement setup.

2-3 Result and Discussion

2.3-1. Electrical characteristics of pMOSFETs with and without fluorine incorporation

The C-V curves in Fig. 2-6 indicate not obvious change of EOT with and without fluorine sample, this means that fluorine atoms doesn't break Hf-F bond and then causes dielectrics degradation [10]. And we can also observe that C-V curve in F-incorporated sample show shift toward positive V_g direction. Similar phenomenon was observed in I_d-V_g characteristics show in Fig. 2-7. This is point out that decrease

of positively charged traps or increase of negatively charged traps [8, 9, 13]. In Fig. 2-7 and Fig. 2-8 we also observe both drain current and transconductance have a apparent improvement in F-incorporated sample. Fig. 2-9 and Fig. 2-10 depict the results of driving current and maximum transconductance versus different channel length. When channel length becomes shorter, the improvement is more apparent.

Fig. 2-11 indicates the sub-threshold swing for devices with and without fluorine incorporation. We find that sub-threshold swing versus channel length. We find that sub-threshold swing in F-incorporated sample is smaller than it in control sample. This implies that this dose of fluorine doesn't cause severe damage in silicon bulk, on the other hand it makes the interface better. Fig. 2-12 shows the threshold voltage versus channel length. Threshold voltage shift toward positive V_g direction was also observed in F-incorporated sample. Fig. 2-13 and Fig2-15 show the maximum transconductance versus various channel width and area .Fig. 2-14 and Fig. 2-16 show the threshold voltage versus diverse channel width and area. We can see that F-incorporated sample has obvious improvement on maximum transconductance no matter in different channel length, width and area. And threshold voltage shift toward positive Vg direction also observe in F-incorporated sample. The driving current and transconductance of F-incorporated are higher than control sample. This is because less interface state existed in F-incorporated sample, and the higher mobility we get.

We can prove that by charge pumping method, in Fig 2-17. express charge pumping current for device with and without fluorine incorporation. We observe that charge pumping current decreases in F-incorporated sample. This implies a lot of dangling bond could be fixed by fluorine ion and therefore reduces interfacial layer. And then we can extract the value of N_{it} by equation (2-1). Then we get N_{it} values of $6.3067x10^{10}cm^{-2}$ and $5.3926x10^{10}$ cm^{-2} with and without fluorine incorporation respectively.

Fig. 2-18 shows that mobility versus effective electric field, we find the higher mobility we get in F-incorporated sample. This is also caused by fluorine ion fixed dangling bond in the interfacial layer. But using split-CV method wouldn't calculate short channel device because we the capacitance is too small and disturbance is too large, then we can't get it by HP4284 LCR meter. Therefore, we only can measure the large dimensional device. Fig 2-19 reveals that leakage current seems not to be increased for device with and without fluorine incorporation.

2.3-2. Conduction mechanism of pMOSFETs with HfO_2/SiON gate stack

The carrier type involved in the leakage current through HfO_2/SiON dielectric layers have also been investigated for unstressed pMOSFETs, using carrier separation

method [14]. The contributing carrier of the gate leakage current can be separated into holes and electrons. Fig. 2-20 shows carrier separation results under the inversion region, and Fig. 2-21 shows carrier separation results under the accumulation region for P^+-gated PMOSFETs with HfO_2/SiON gate stack, both with and without fluorine incorporation. It is found that the source/drain current I_{SD} dominates the leakage current under inversion region, and the substrate current I_B dominates the leakage under accumulation region. This indicates holes from S/D that tunnel through gate dielectric is the dominant component of conduction mechanism under inversion region , while electrons from gate electrode that tunnel through gate dielectric is the dominant component of conduction mechanism under accumulation region.

This could be explained by band-diagrams shown in Fig. 2-22(a) and carrier separation experiment shown in Fig. 2-22(b). The substrate current I_B corresponds to the electron current from the gate , while the source/drain current I_{SD} corresponds to the hole current from Si substrate under inversion region. Electron supply from the gate conduction band in pMOSFETs is limited by the generation rate of minority electrons in p^+ gate. In other words, the probability of carriers from S/D that tunnel through gate dielectric is strongly affected by tunneling distance and barrier height [15]. Because of the asymmetry of the HfO_2/SiON band structure , it is more difficult for electrons to tunnel through gate dielectrics compared with holes. In pMOSFETs ,

hole current from the channel is the predominant injection current under stressing. The leakage component under accumulation region can also be explained by band-diagrams shown in Fig. 2-23(a), and the current component flow in carrier separation experiment is shown in Fig. 2-23(b).

In Fig. 2-24 and Fig. 2-25 , the gate current I_g as a function of V_g for the HfO2/SiON layer is measured from temperature up to 125℃, both under inversion region and accumulation region for two samples. The current is temperature dependent that increases with increasing temperature. This implies that the conduction mechanism of current is trap-related, i.e., trap-assisted tunneling (TAT). Frenkel-poole, etc.

The gate leakage current for devices with HfO_2/SiON gate stack is composed of two types of current, i.e., hole current and electron current. To determine the conduction process in the HfO_2/SiON dielectric, Frenkel-poole (F-P) plots are fitted for hole current and electron current, respectively, for both samples.

The current from Frenkel-poole emission is of the form:

$$I \propto V \exp\left(\frac{2a\sqrt{V}}{n} - \frac{q\Phi_B}{k_B T}\right) \qquad (2\text{-}7)$$

$$J = B * E_{ox} \exp\left(\frac{-q(\Phi_B - \sqrt{qE_{ox}/\pi\varepsilon_{ins}\varepsilon_0})}{k_B T}\right) \qquad (2\text{-}8)$$

$$\ln\left(\frac{J}{E_{ox}}\right) = \frac{q\sqrt{qE_{ox}/\pi\varepsilon_{ins}\varepsilon_0}}{k_B T}\sqrt{E_{ox}} - \frac{q\Phi_B}{k_B T}\Big) \qquad (2\text{-}9)$$

$\Rightarrow$ intercept gives the Barrier height ($-\frac{q\Phi_B}{k_B T}$)

where B is a constant in terms of the trapping density in the HfO_2 film , Φ_B is the barrier height, E_{ox} is the electric field in HfO_2 film. ε_0 is the free space permittivity, ε_{ins} is HfO_2 dielectric constant, k_B is Boltzmann constant , and T is the temperature measured in Kelvin.

As shown in Fig. 2-26 and Fig. 2-27, under inversion region, excellent linearity for each current characteristic has been observed for both samples. This tendency indicates that both samples exhibit the Frenkel-Poole conduction mechanism for the gate leakage current. Both the electron and hole conduction mechanisms are the same, and the result agree well with the F-P conduction mechanism. Barrier height Φ_B and dielectric constant ε_{ins} of HfO_2/SiON can be calculated. The ε_{HfO_2} valre is found to be ~ 14.7 and ~14.4 for the control and F-incorporated samples, respectively.

The Φ_B for the hole traps in the control sample and F-incorporated sample is about 1.47eV and 1.51eV, respectively. On the other hand, for electron traps, the Φ_B of the control sample and F-incorporated sample are about 1.59eV and 1.62eV, respectively. The Φ_B to be discussed in this chapter is the "effective" value that is representative of the HfO_2/SiON gate stack [15]. We consider the case when the injected carriers flow across HfO_2/SiON by hopping via the trap sites with energy barrier Φ_B, whose value depends on the fabrication process [16]. These experimental results indicate that

the energy level for traps in the control sample is similar to that of the F-incorporated sample, and the energy barrier Φ_B for holes is clearly lower than that for electrons about 0.12eV in both samples.

2-4 summary

In this work, the initial electrical properties of the devices are smaller affected by fluorine incorporation, such as absolute threshold voltage is smaller and CV curve shifts toward positive V_g direction. We verify that appropriate fluorine incorporation doesn't degrade the interface and dielectric quality, and it can enhance mobility and drive current of the device. We use carrier separation to verify that devices with and without fluorine incorporation, we found gate leakage current is the same with both devices. And conduction mechanism is Frankel-Poole emission.

Fluorine Channel Implantation

- **Standard LOCOS process**
- **Fluorine implantation(Dose:5E13 Energy:10KeV)**

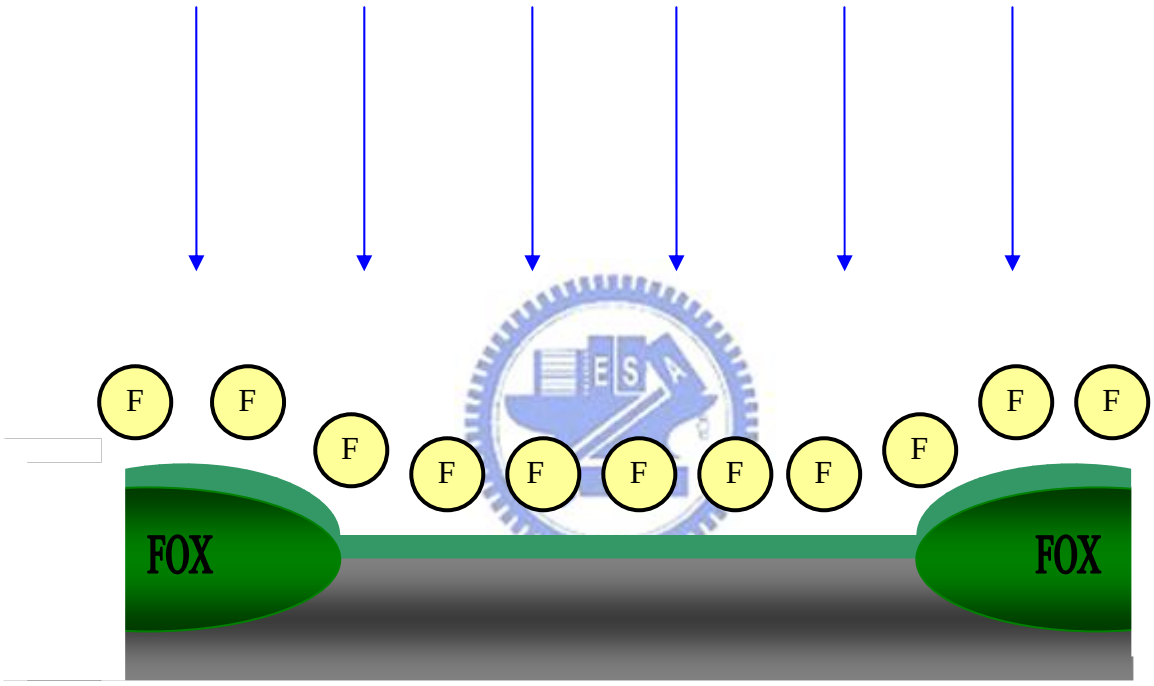


Fig. 2-1 Fluorine incorporation via channel implantation

- **Standard LOCOS process**
- **Fluorine implantation(Dose:5E13 Energy:10KeV)**
- **RCA clean and HF dip**
- **800℃ in NH_3 ambient by furnace ~SiON 0.7nm**
- **ALD of 30 nm HfO_2**
- **PDA 600℃ 20sec in N_2 ambient**
- **poly-Si deposition 200nm and pattering**
- **Spacer , S/D extension , S/D implant**
- **Dopant activation : 950℃ , 30s**
- **Passivation layer : SiO_2 400nm**
- **Metallization : Al-Si-Cu 900nm**
- **Forming gas sintering : 400℃ , 30min**

Fig 2.2 The process flow of pMOSFETs with HfO_2/SiON gate stack

Device Structure

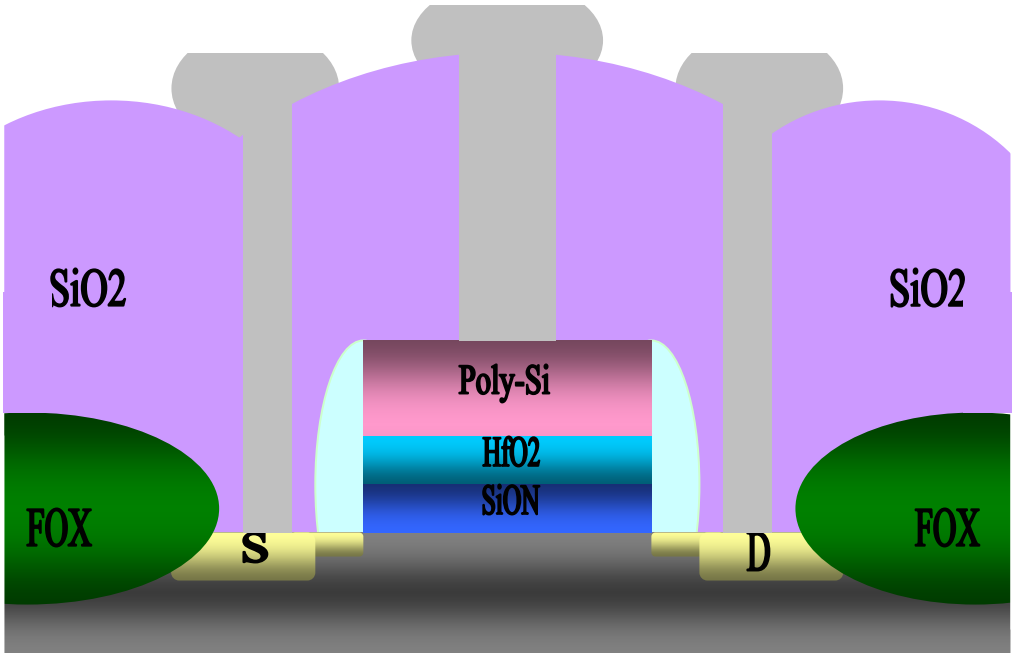


Fig 2-3 Schematic cross section of pMOSFETs with HfO_2/SiON gate stack.

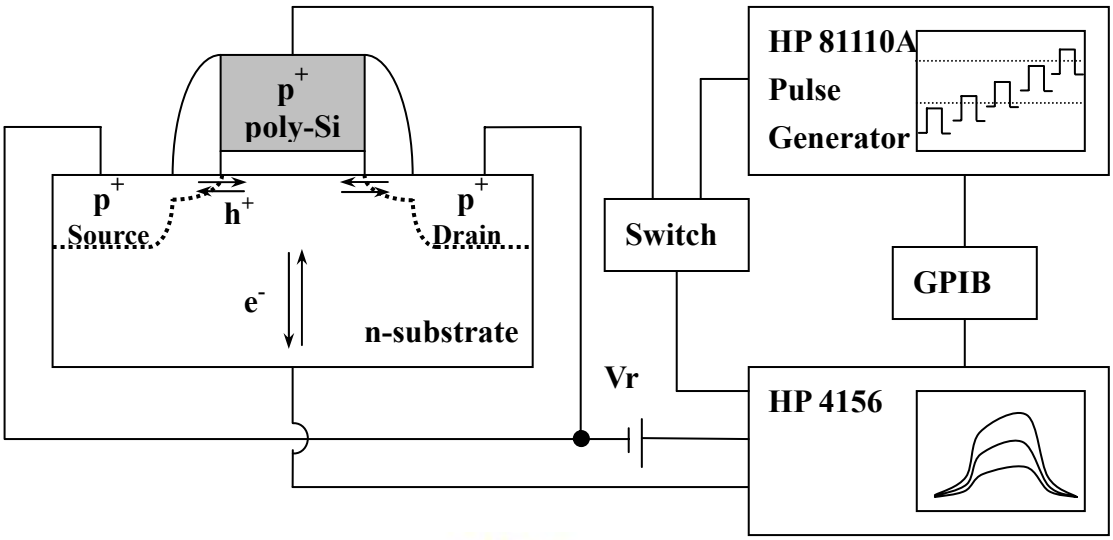
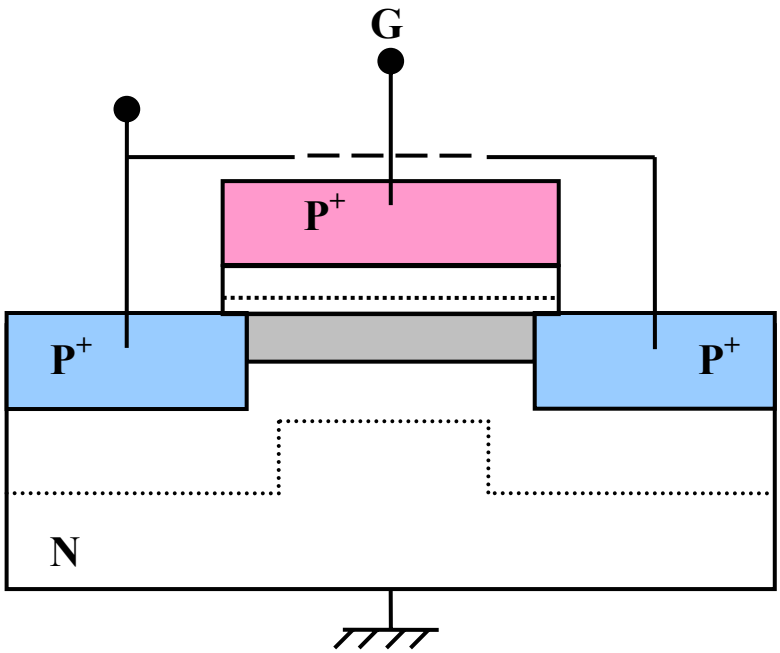
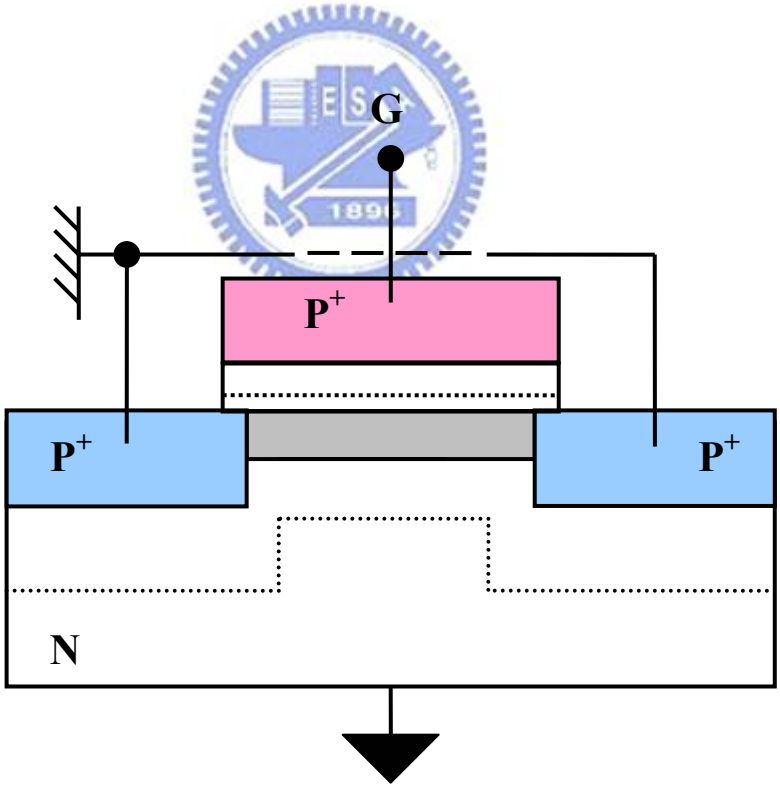


Fig. 2-4 Basic experimental setup of charging pumping measurement.



(a)



(b)

Fig. 2-5 Configuration for (a)gate-to-channel, and (b)gate-to-substrate capacitance measurement.

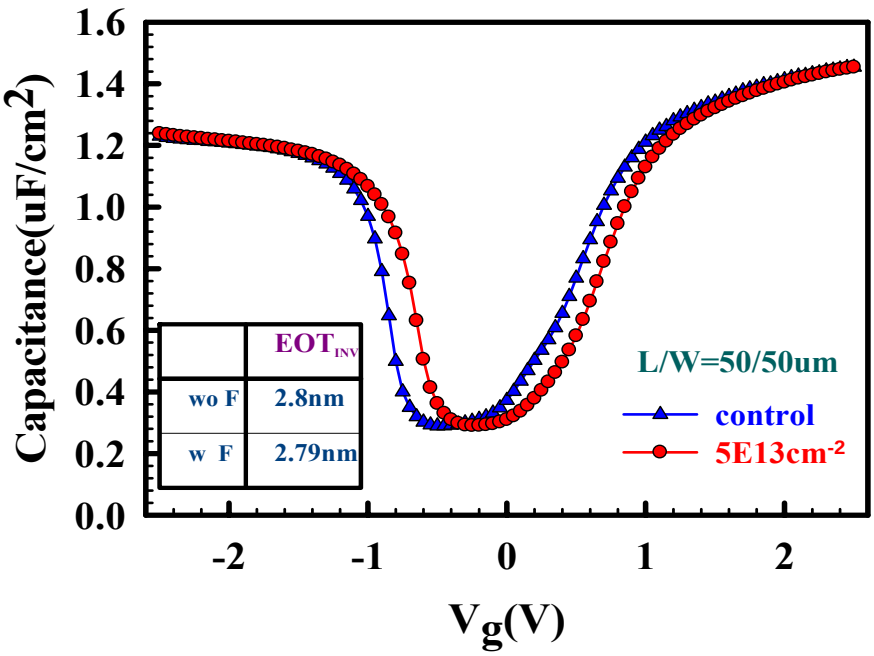


Fig. 2-6 C-V curves for pMOSFETs.

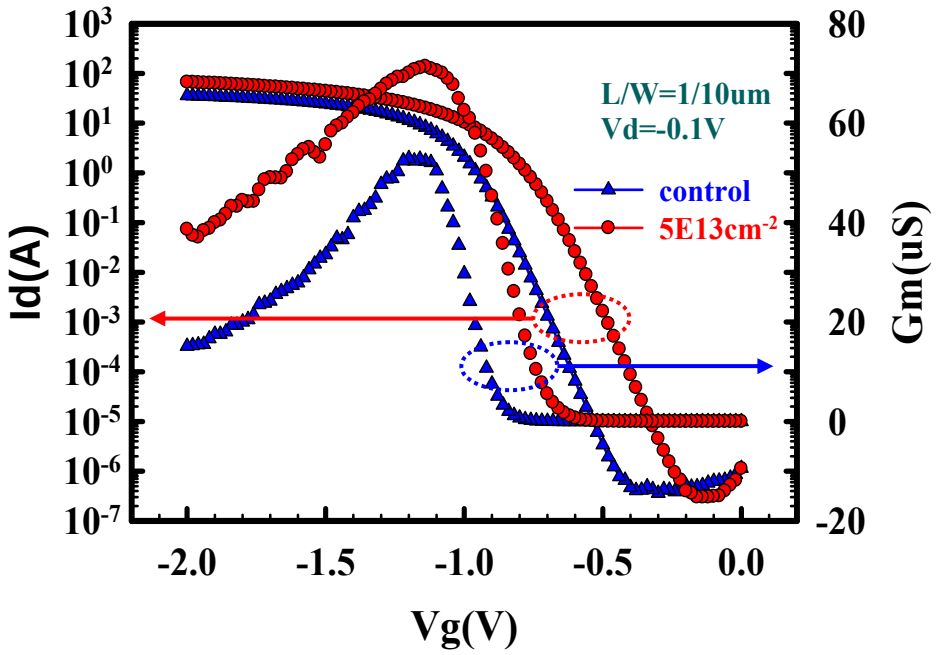


Fig. 2-7 Id-Vg & Gm-Vg characteristics of devices with and without fluorine incorporation at V_D=0.1V.

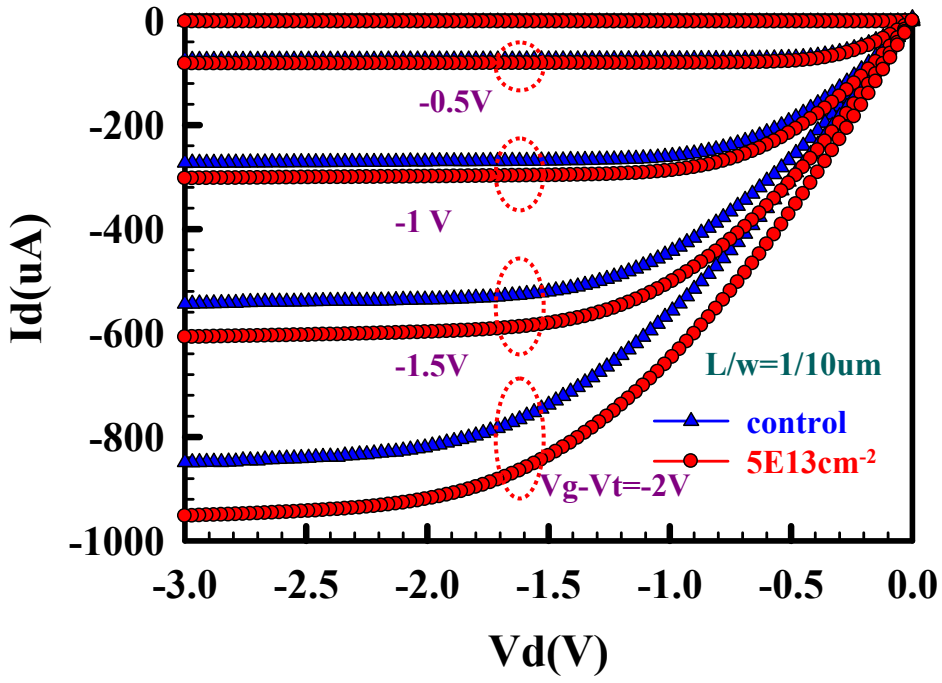


Fig 2-8 I_d-V_d characteristics for devices with and without fluorine incorporation.

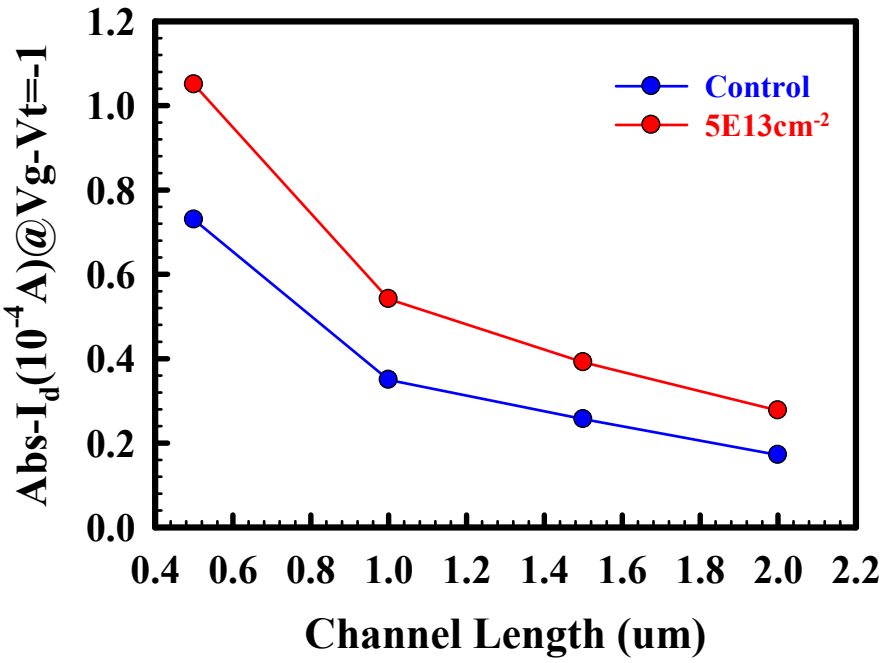


Fig. 2-9 Compared Id_{linear} with channel length for device with and without fluorine.

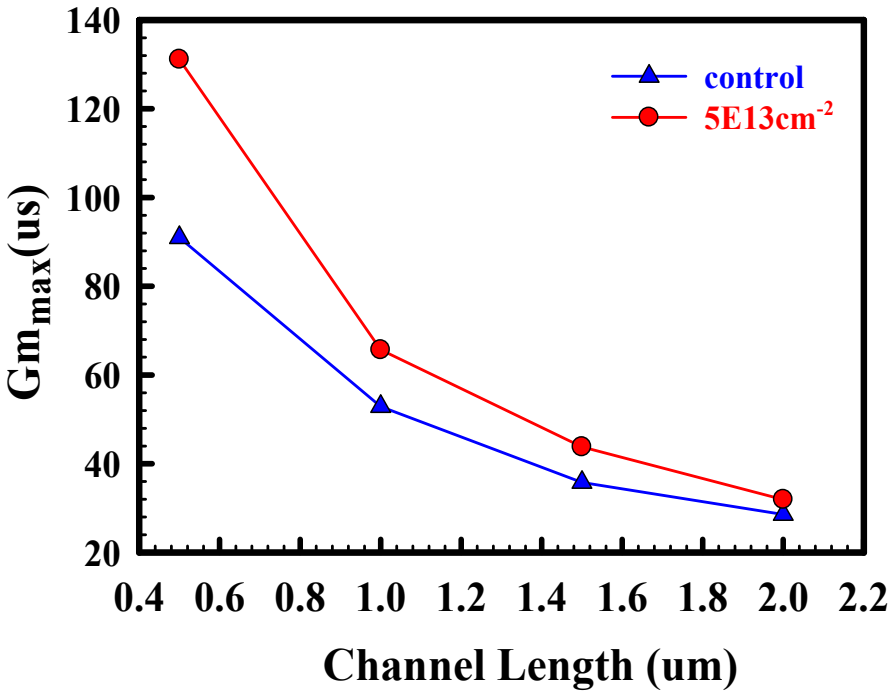


Fig. 2-10 Compared Gm_{max} with different channel length for device with and without fluorine.

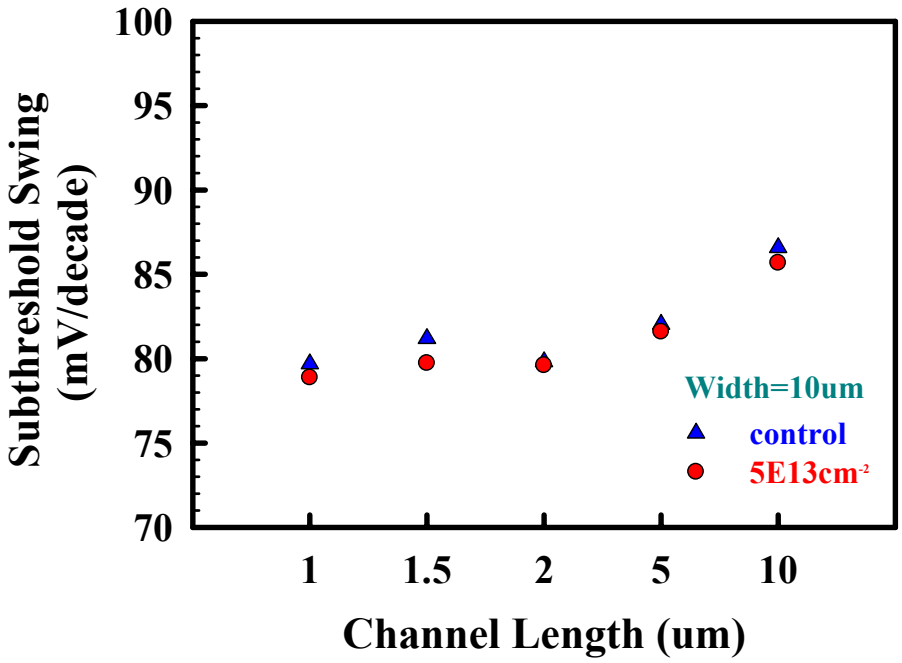


Fig. 2-11 Compared sub-threshold swing with different channel length for device with and without fluorine.

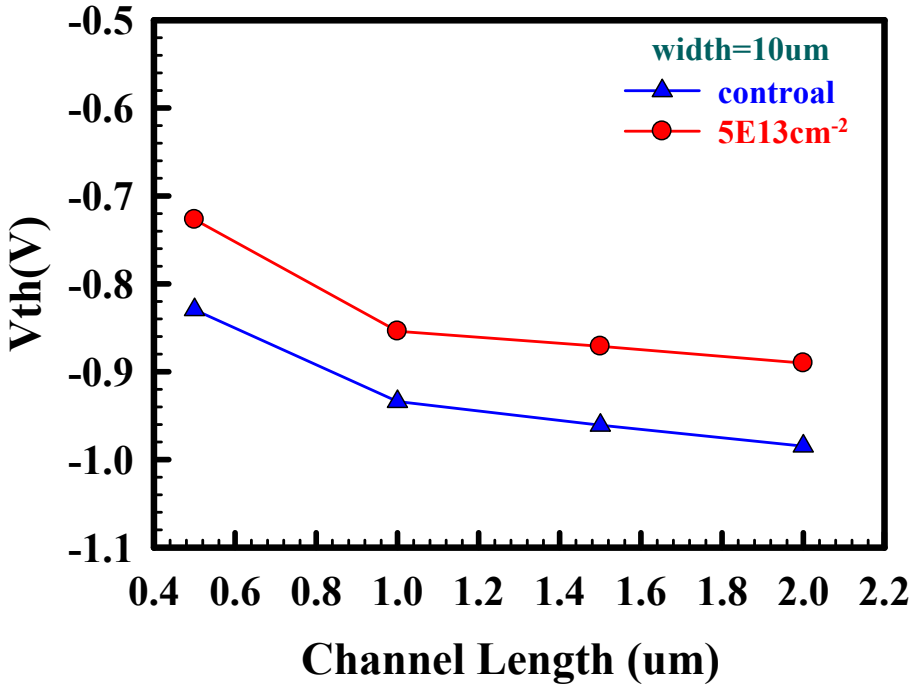


Fig. 2-12 Compared threshold voltage with channel length for device with and without fluorine.

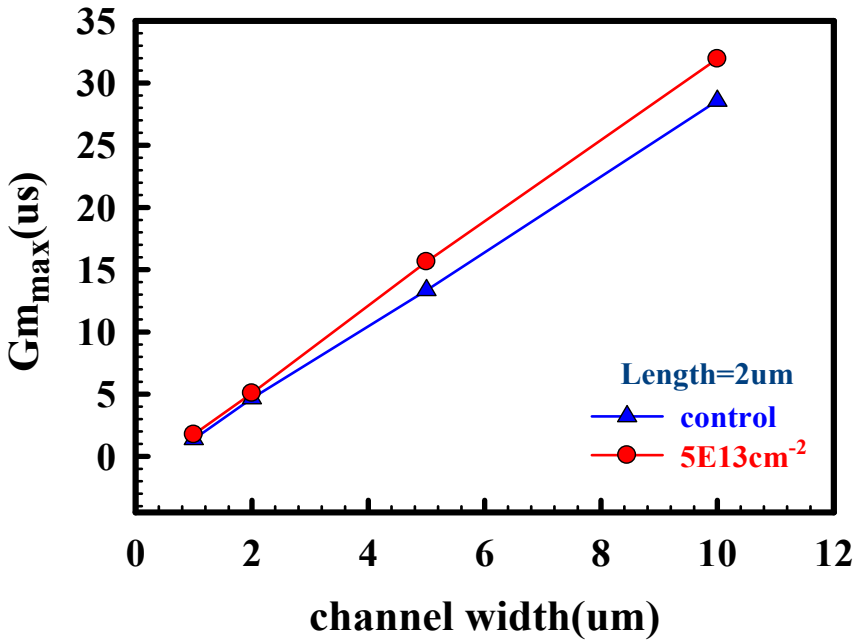


Fig. 2-13 Compared Gm_{max} with channel width for device with and without fluorine.

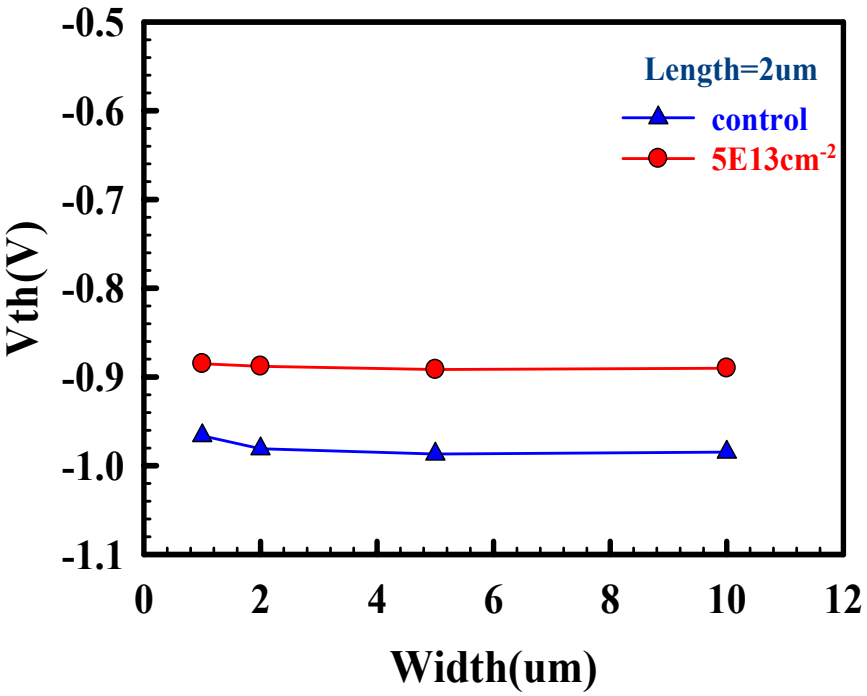


Fig 2-14 Compared threshold voltage with channel width for device with and without fluorine.

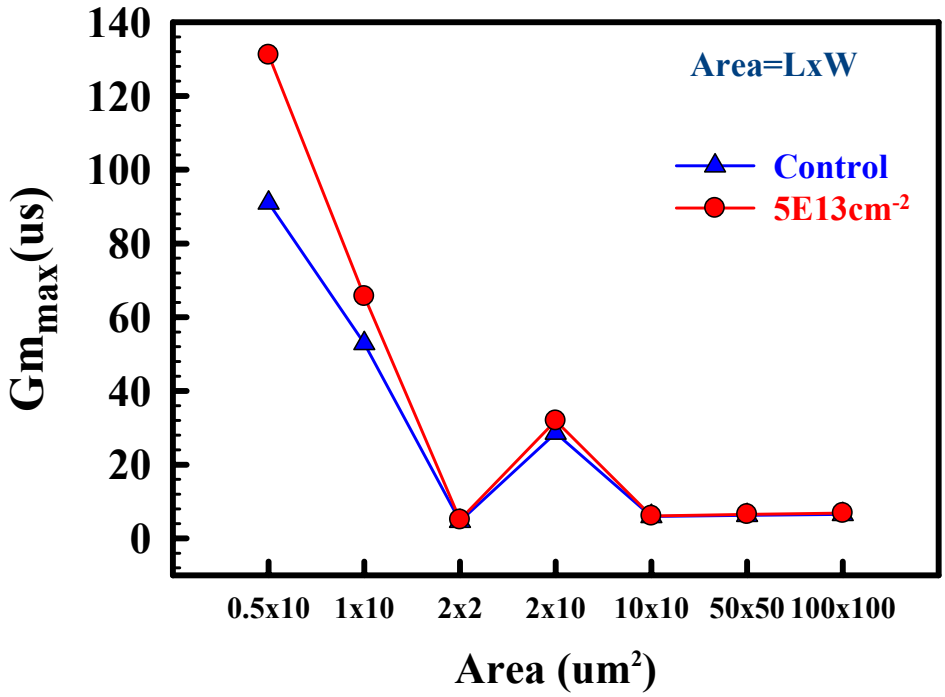


Fig. 2-15 Compared Gm_{max} with area for device with and without fluorine.

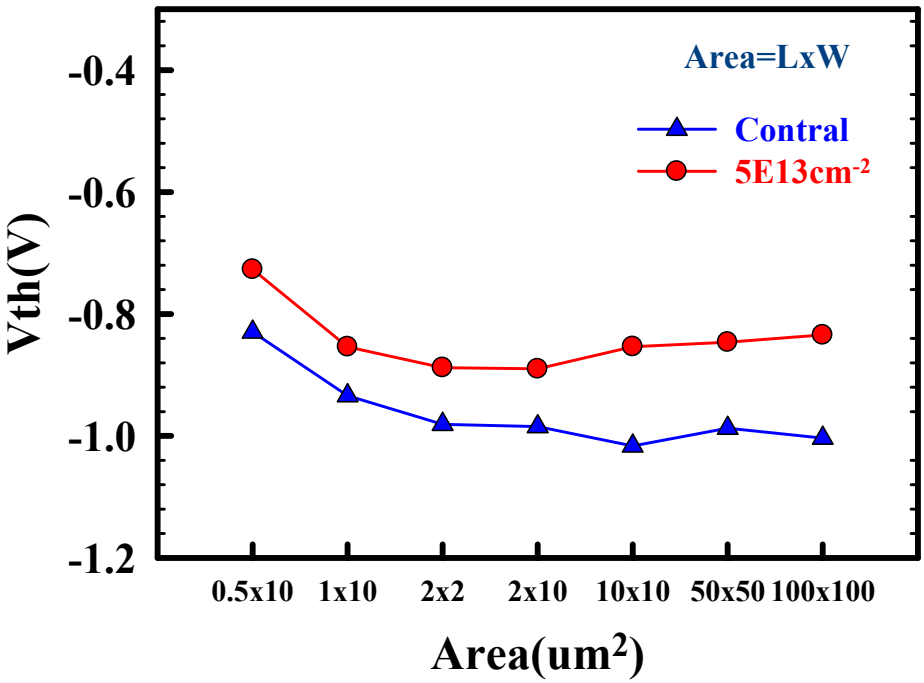


Fig. 2-16 Compared threshold voltage with area for device with and without fluorine.

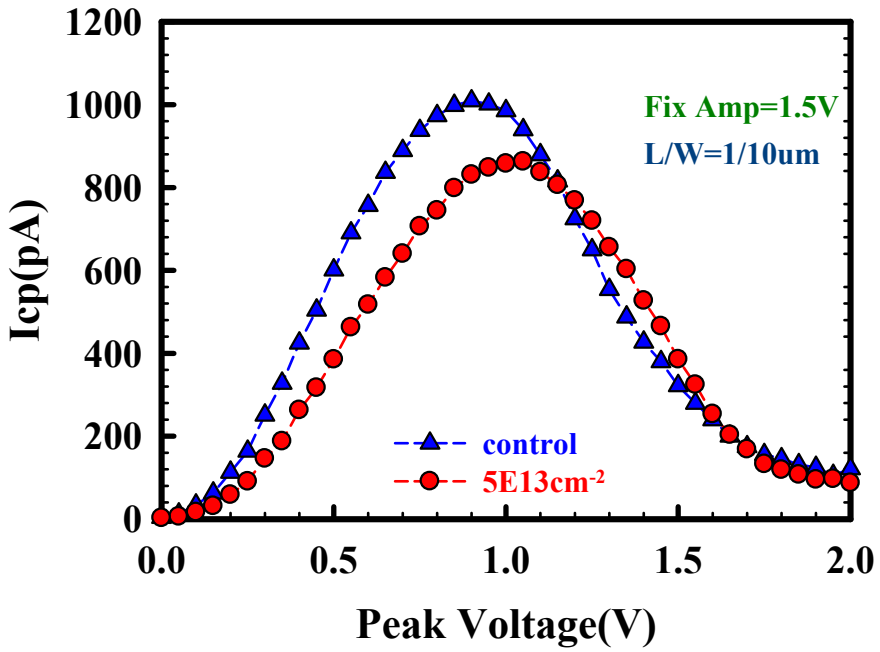


Fig. 2-17 Charge pumping current for device with and without fluorine incorporation.

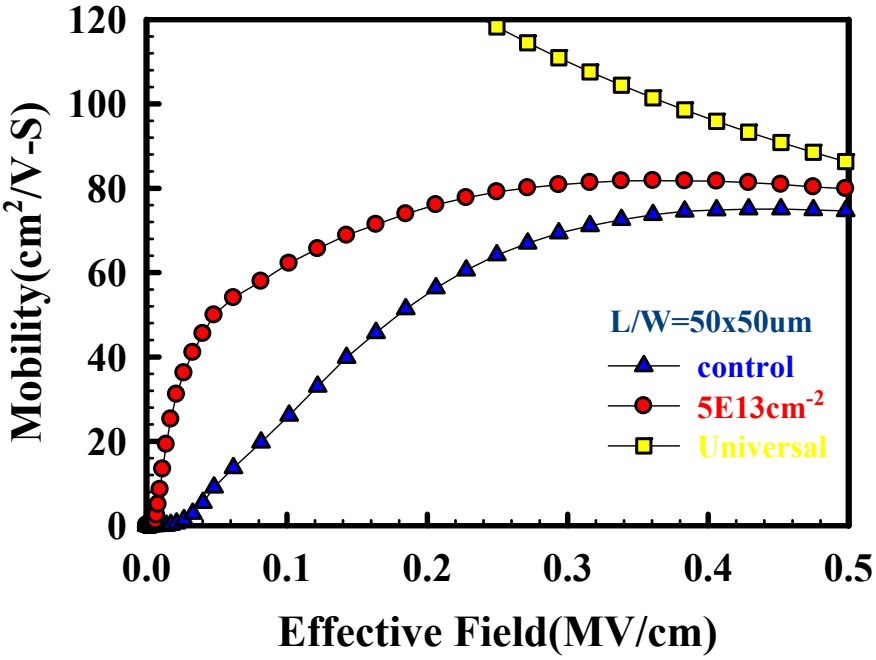


Fig. 2-18 Compared hole mobility with effective field for device with and without fluorine.

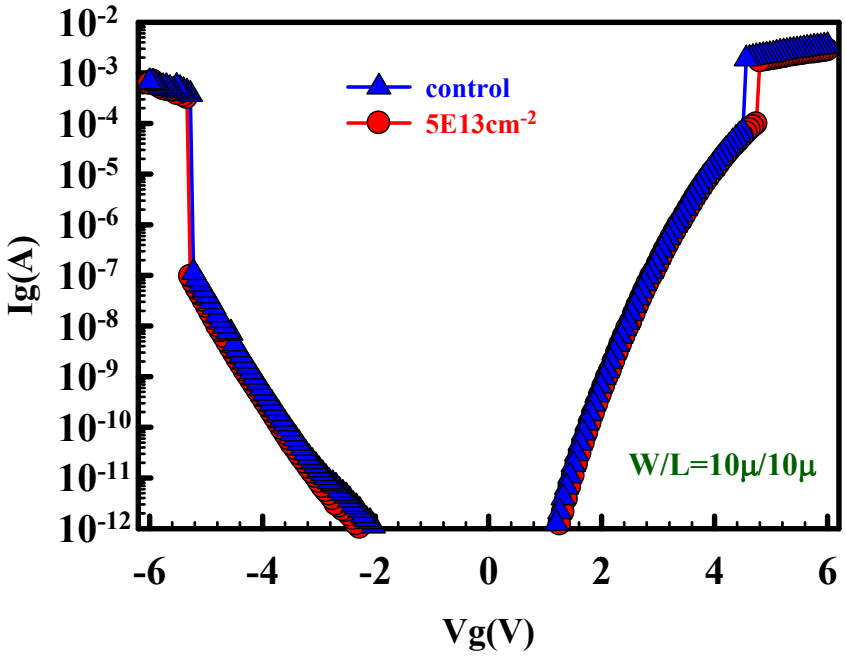
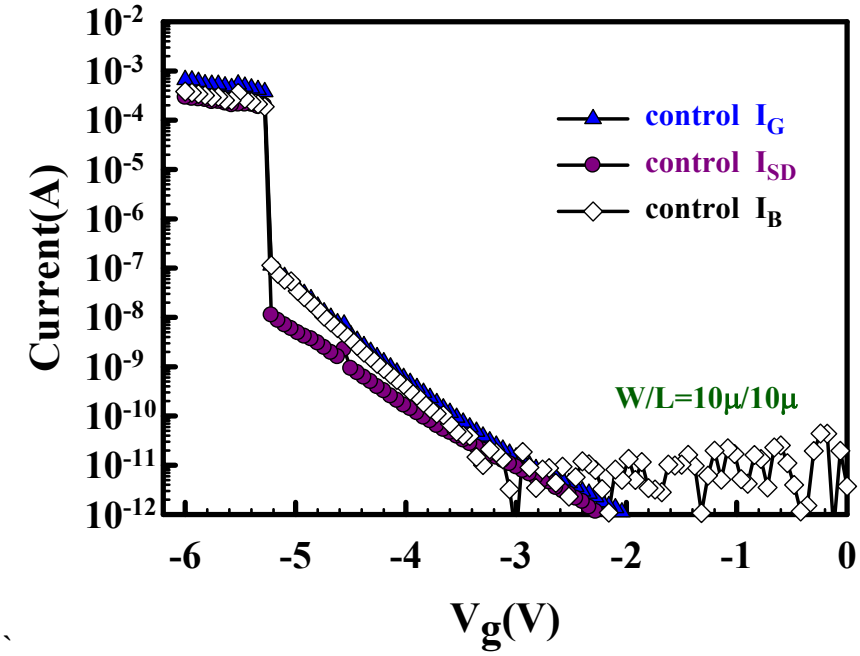
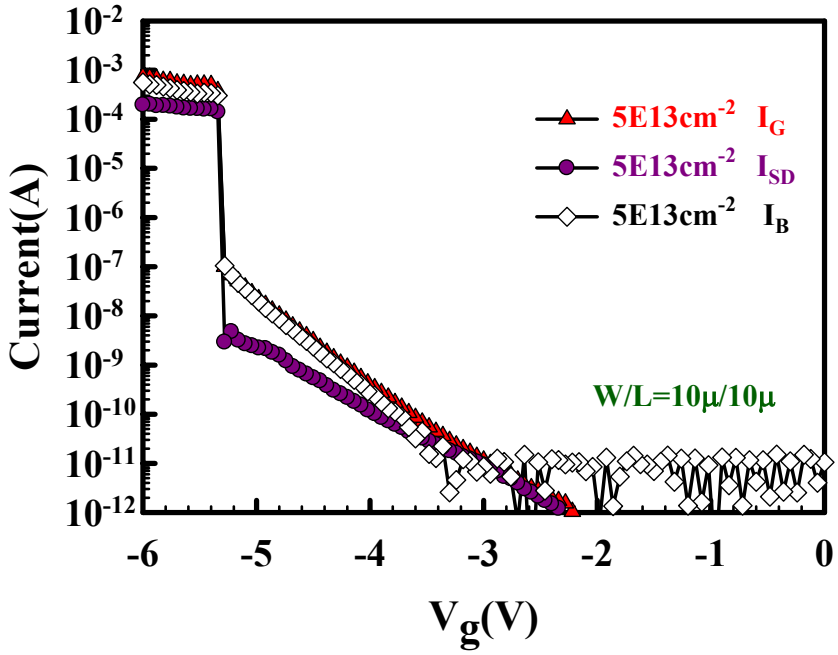


Fig. 2-19 Gate leakage current versus gate bias for fresh p-channel devices at room temperature.

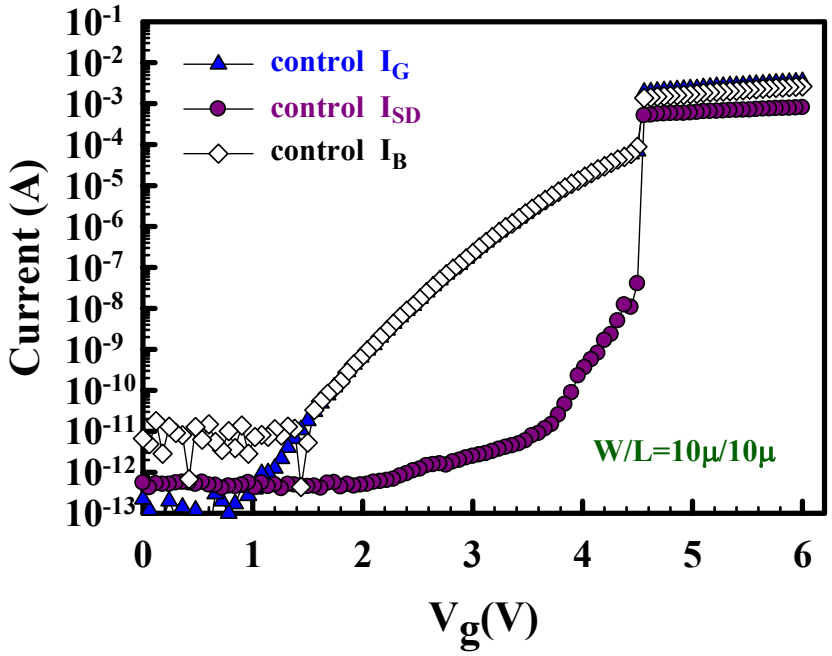


(a)

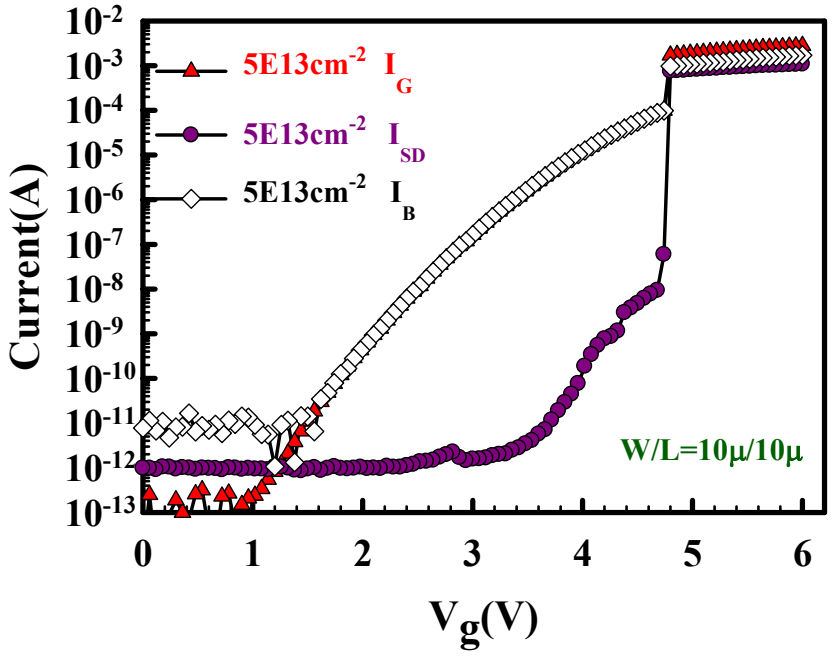


(b)

Fig. 2-20 Carrier separation under inversion region (a) control sample, and (b)with F sample.



(a)



(b)

Fig. 2-21 Carrier separation under accumulation region (a) control sample, and (b)with F sample.

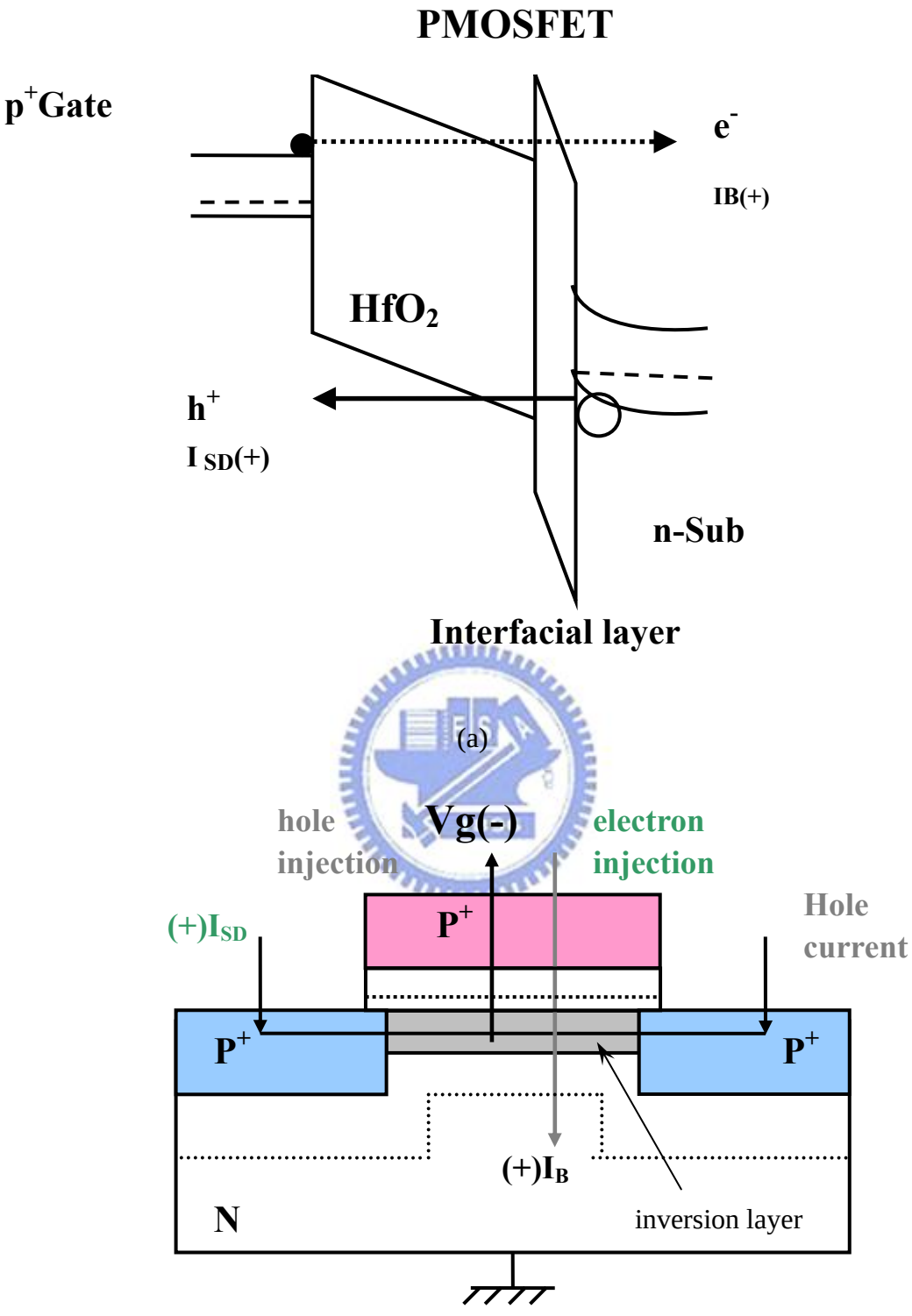


Fig. 2-22 p+-gated pMOSFET with HfO2/SiON gate stack under inversion region (a) band diagrams, and (b) Schematic illustration of carrier separation experiment.

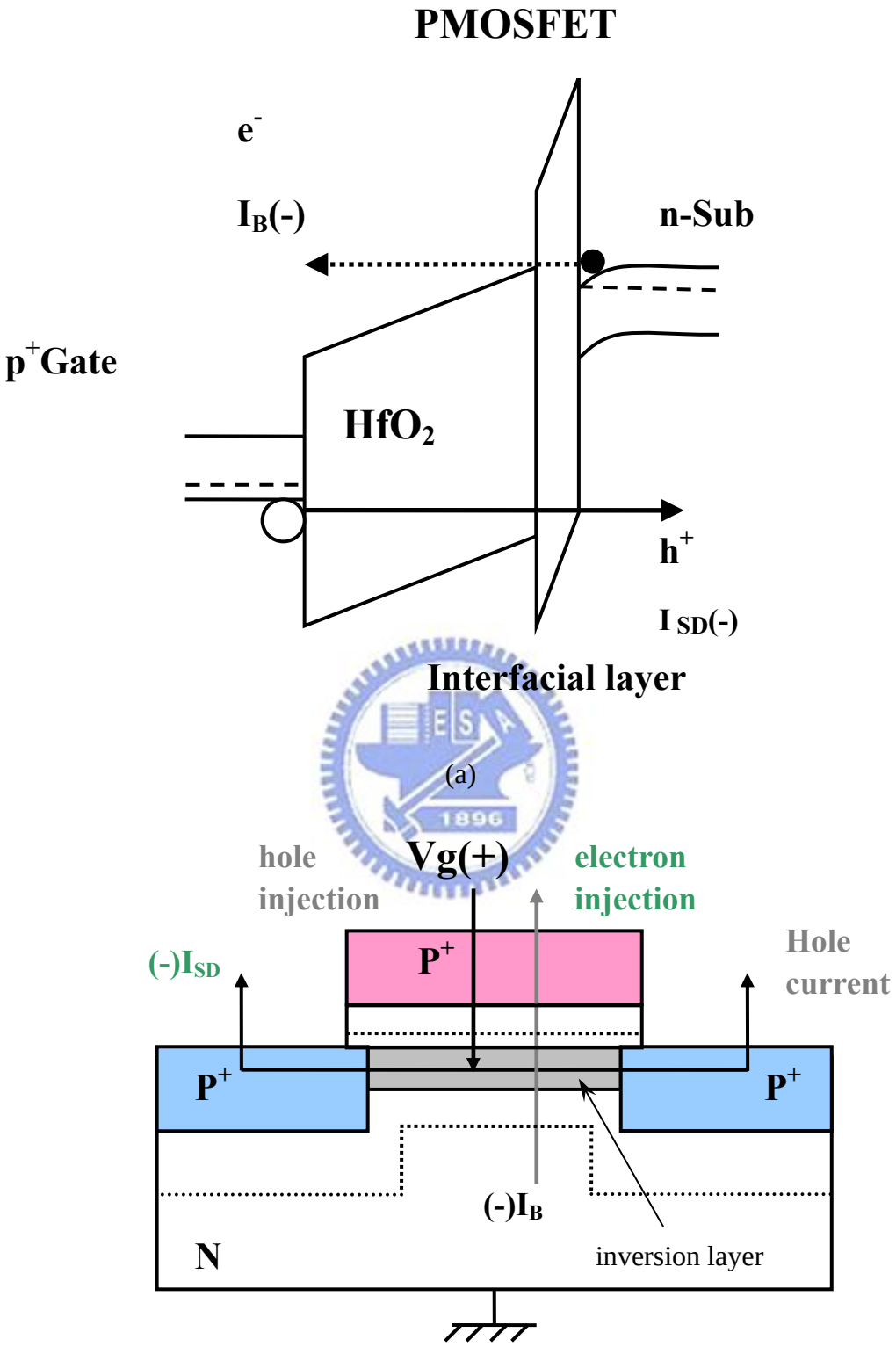


Fig. 2-23 p^+ -gated pMOSFET with HfO_2/SiON gate stack under accumulation region (a)band diagrams , and (b)Schematic illustration of carrier separation experiment.

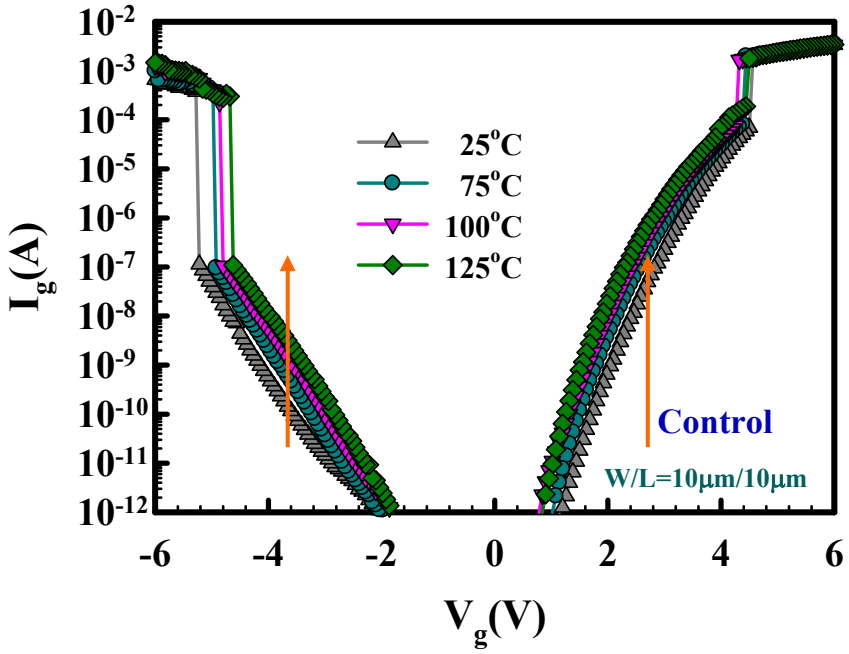


Fig. 2-24 Gate leakage current versus gate bias without fluorine incorporation for fresh p-channel devices at different temperature.

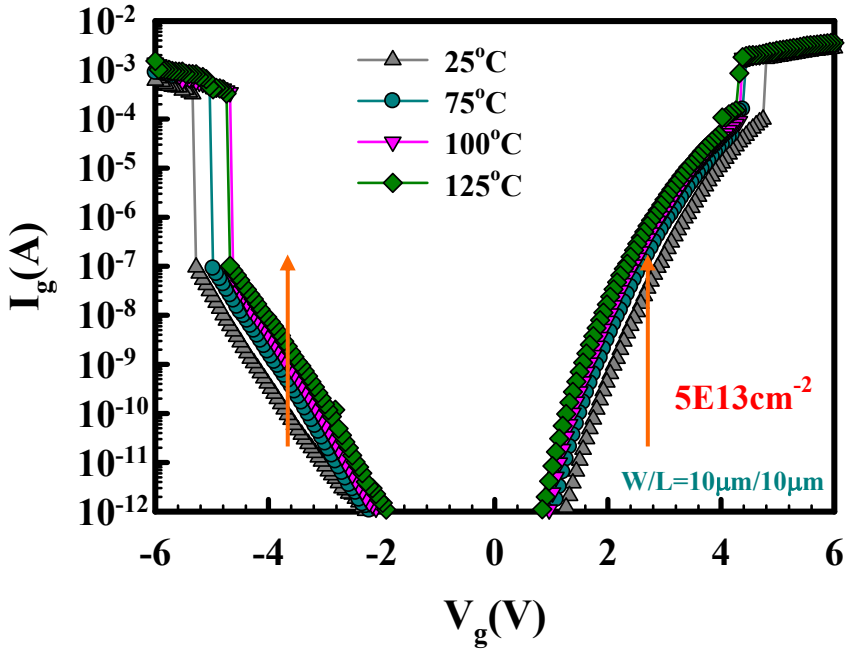
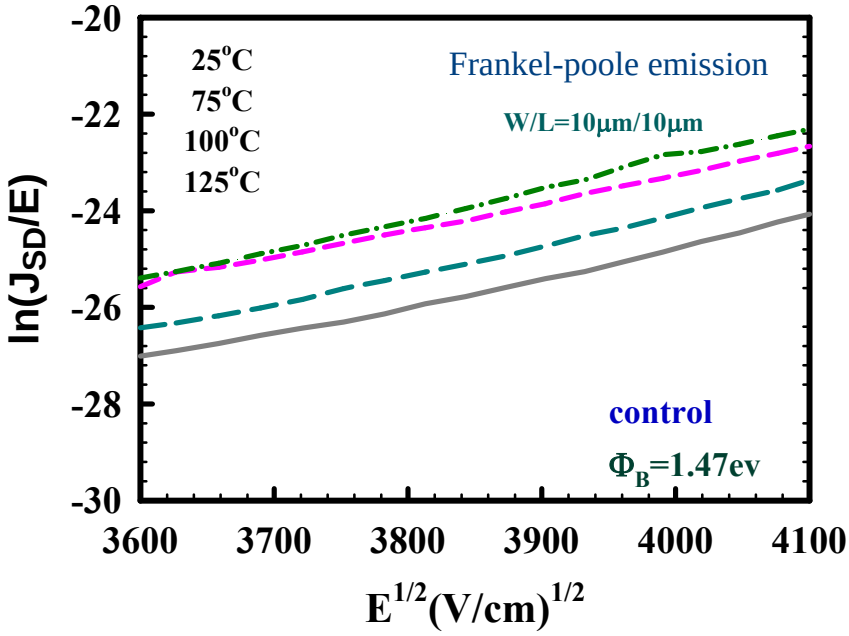
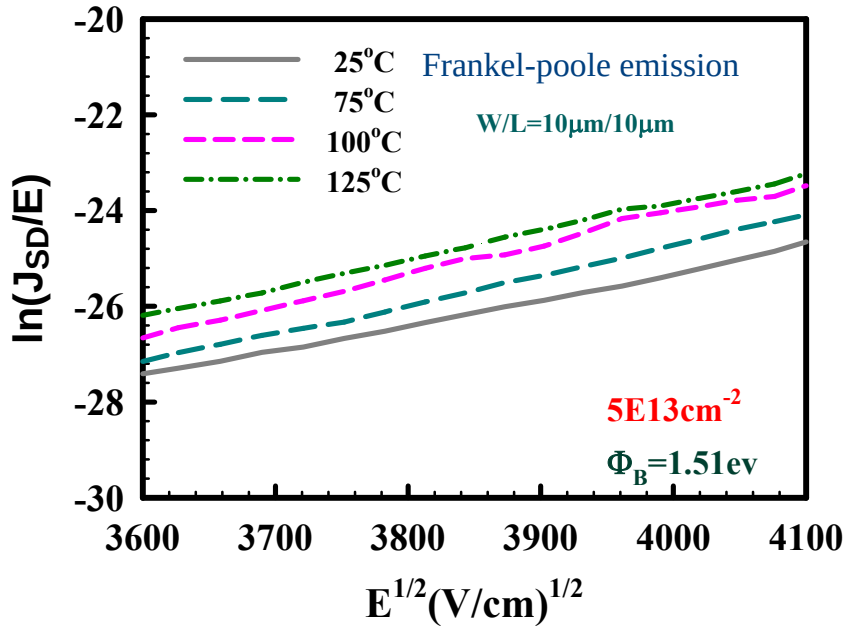


Fig. 2-25 Gate leakage current versus gate bias with fluorine incorporation for fresh p-channel devices at different temperature.

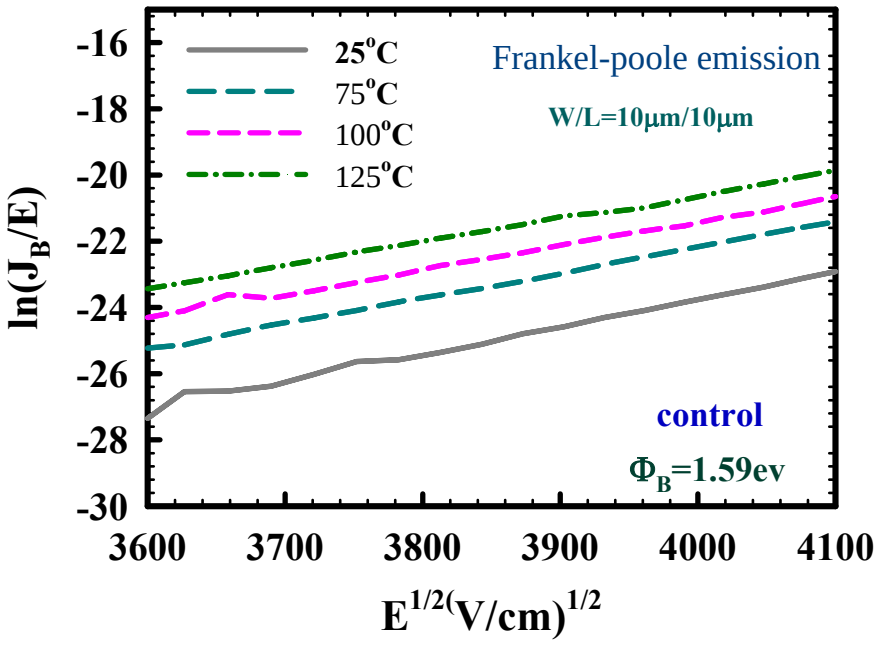


(a)

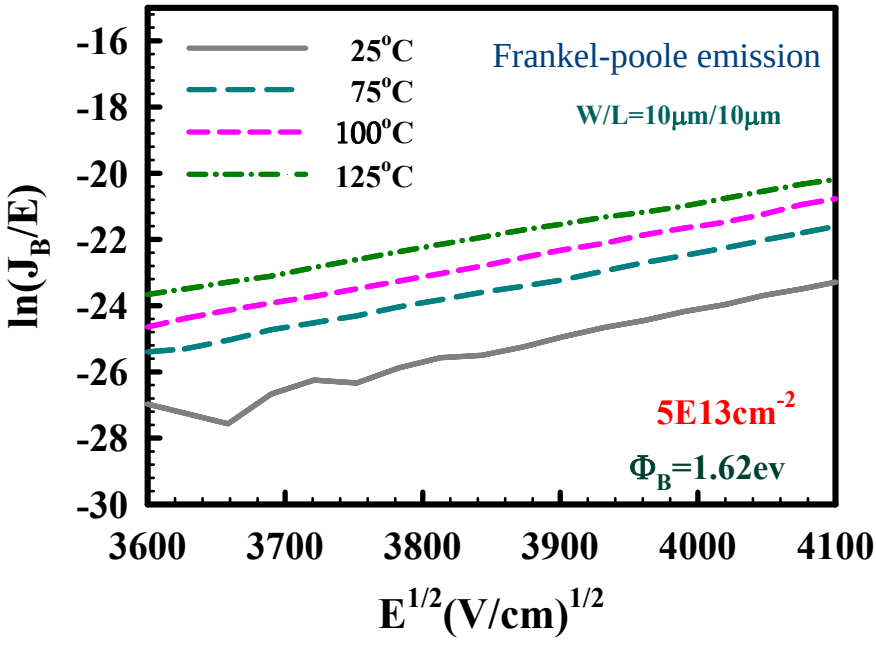


(b)

Fig. 2-26 conduction mechanism for source/drain current fitting under inversion region (a) without fluorine sample (b) with fluorine sample.



(a)



(b)

Fig. 2-27 conduction mechanism for substrate current fitting under inversion region (a)without fluorine sample (b) with fluorine sample.

Chapter 3

Impacts of Fluorine Incorporation on the Reliability of pMOSFETs with HfO_2/SiON Gate Stack

3-1 Introduction

The main issue of reliability in pMOSFETs is NBTI (negative bias temperature instability) [17-18-19]. It manifests itself as a increase in the absolute threshold voltage, and a decrease in the inversion layer mobility under the negative bias at elevated temperatures. This is due to increase in interface states and generation of positive charges during NBTI processes. The device parameter degradations can lead to circuit failures, both for analog and digital application. The mechanism of NBTI is the depassivation of Si-H bonds at Si/SiON interface.

Unlike SiO_2 films, high-k films have another problem, charging trapping . Charge trapping causes the threshold voltage to shift with stressing time, and is therefore an important transistor reliability issue. Two mechanisms: the depassivation of Si-H bonds and trapping effect for pMOSFETs with high-k gate dielectric.

Fluorine is known as to worsen boron penetration in PMOS devices employing p^+ gate. Therefore fluorine incorporation has been generally regarded as undesirable

for PMOS device application. Nevertheless, an appropriate fluorine implant will enhance oxide reliability.

Huard et al. has demonstrated that the use of BF_2 implants , in lieu of B implants , for the S/D and poly gate for the traditional p^+-gated pMOSFETs with nitrided gate oxide layer results in lower device degradation. Fluorine was found to improve the gate oxide reliability as long as the concentration is moderate. This result has been confirm by deliberate fluorine implantation, in addition to BF_2 doping, which also shows alleviated NBTI degradation [20].

In this thesis, effects of fluorine (F) on the reliabilities of pMOSFETs with HfO_2/SiON have been studied. We incorporate fluorine ions via channel implantation , and we found that F-incorporated sample improving NBTI immunity. The reliability of pMOSFETs with and without fluorine incorporation will discuss in this later.

3-2 The Models of NBTI and the Mechanism of Fluorine Incorporation Alleviate NBTI Degradation

3-2.1 The Models of NBTI

The model about negative bias stress (NBS) was first published by Jeppson and Svensson in 1977 [21-22]. This is so call Reaction-Diffusion model, which can be

generalized as

(interface defect) $\longleftrightarrow$

(interface trap) + (fixed oxide charge)$^{+}$ + $X_{\text{interface}}$ +e^{-} (3-1)

$$X_{\text{interface}} \xleftrightarrow{diffusion} X_{bulk} \quad (3\text{-}2)$$

where X represents a mobile species which diffuse away from the interface. It is noted that interface defect in Eq. (3-1) means Si/SiO2 or Si/high-k interface is comprised of hydrogen passivating Si dangling bond and that X is hydrogen (atom or proton) or some water-related species[17,22,23]. The interface trap is then supposed to be a silicon dangling bond denoted as Si $\bullet$ which results when H is removed from Si-H bond. A detailed critical analysis of the proposed reactions has been given in [21,24] Their model forms the basis for models subsequently modified by others.

Other models like hydrogen models are used to explain NBTI. They are:

(a)high electric fields induced SiH dissociation model , as follows

$$Si_3 \equiv SiH \longrightarrow Si_3 \equiv Si\bullet + H^0 \quad (3\text{-}3)$$

where H^0 is a neutral interstitial hydrogen atom or atomic hydrogen .

(b)interstitial atomic hydrogen attack model , as follows

$$Si_3 \equiv SiH + H^+ \longrightarrow Si_3 \equiv Si\bullet + H_2 \quad (3\text{-}4)$$

according to the first-principles calculations show that the positively charged hydrogen or proton H^+ is the only stable charge state of hydrogen at the interface and

that H^+ reacts directly with the SiH to form an interface trap. This model uses the fact that the Si-H complex is polarized such that a more negative charge resides near the hydrogen atom. Mobile positive H^+ migrates toward the negatively charged dipole region or the Si-H molecule. The H^+ atom then reacts with the H^- to form H_2 leaving behind a positively charged Si dangling bond.

(c) holes induce Si-H dissociation model , as follows

$$Si_3 \equiv SiH + h^+ \longrightarrow Si_3 \equiv Si\bullet + H^+ \qquad (3\text{-}5)$$

SiH interact with “hot holes” or holes near the Si/SiO_2 interface during NBTI stress. The fixed charge (Q_f) is a by-product of trivalent Si defect near the SiO_2/Si interface oxide and also contributes to the shift of threshold voltage

$$O_3 \equiv SiH + h^+ \longrightarrow O_3 \equiv Si^+ + H^0 . \qquad (3\text{-}6)$$

The generation of fixed charges is independent of oxide thickness, while the interface trap generation is inversely proportional to oxide thickness [21]. This suggests that NBTI is worse for thinner oxide, but this phenomenon is not always observed and highly dependent on the process conditions.

As proved by Jeppson and Svensson [22], the behavior of the interface trap generation suggests the generation process is diffusion controlled. N_{it} buildup equals the total number of released H species. Hole-assisted reaction breaks interfacial SiH bonds, resulting in N_{it} generation:

$$\Delta N_{it}(t) = R(Dx\ t)^n \qquad (3\text{-}7)$$

Although reaction-diffusion model can predicts the threshold voltage shift to increase with a power law dependence on time. However, the model does not predict the saturation as observed after prolonged stressing nor does it derive the dependence of ΔV_t on stress oxide field from first principles. In 2004 , Sufi Zafar from IBM proposed a physical based model for NBTI induced degradation [25]. This model attributes NBTI to depassivation of Si-H bonds at the SiO_2/Si interface. The two distinguishing features of the proposed model are: (i) statistical mechanics is applied to calculate the decrease in interfacial Si-H density as a function of stressing conditions, and (ii) hydrogen diffusion in the oxide is assumed to be dispersive and the diffusing species is identified with the positively charged hydrogen ion (Hi^+). The model assumes that as Hi^+ diffuses away from the interface into the oxide, interfacial and bulk traps are created. Based on these model assumptions, an equation .for ΔV_t shift is derived as a function of stress time, oxide field, temperature, oxide thickness, and initial Si-H density at the interface. The equation as follows

$$\Delta V_t(t) = \Delta V \max \cdot (1 - e^{-(t/\tau)\beta}) \qquad (3\text{-}8)$$

where, $\Delta V \max$, τ , β are the model parameters. According this model, we can explain NBTI mechanism in conventional dielectrics completely.

Unlike SiO_2, a increase in the absolute threshold voltage of pMOSFETs in high-k

dielectrics is more serious. This is because that high-k film is a big trapping center compared to SiO_2 [1] . Although Si-H dissociation is one of the reason of threshold voltage shift, but the main reason of V_{th} shift is charge injection [26]. This indicate the threshold voltage shift is bulk fixed charges dominative, not interface defects.

3-2.2 The Mechanism of Fluorine Incorporation Alleviate NBTI Degradation

Fluorine incorporation technique was widely studied in 1980s. Wright and Saraswat, their research point out that fluorine incorporation will improve interfacial layer quality [10]. This is because fluorine can passivate the interface defects by forming Si-F bond, and lead to higher reliability. But the research also indicated that large concentrations of fluorine can cause deterioration of bulk gate oxide, although the interfacial region is improved.

In this work, we incorporated fluorine via channel implantation. We found that most of the fluorine atoms implanted in the channel are diffused into HfO_2 layer after annealing [9]. Fluorine is believed to form stronger Si-F bonds (5.73eV) compared to Si-H bonds (3.18eV) in the SiON/Si interface [8], and then improved interface quality and has NBTI immunity. A large number of fluorine exited in the high-k bulk is expected to reduce the defect density and thus reduce charge trapping by bonding to

Hf dangling bond resulting in annihilation of oxygen vacancies. As show in Fig. 3-2 , we schematic describe the binding of Si-F bonds and Hf-F bonds.

3-3 Measurement Setup

Constant voltage stress (CVS) is method to evaluate the reliability of devices as it causes threshold voltage to shift with electrical stressing. A constant voltage stress is applied to device gate from V_g=-2V~-3V, while source/drain and substrate are grounded.We measurement I_d-V_g and charging pumping during stress intervals. I_d-V_g measurements are used to evaluate Gm variation and threshold voltage shift. And charging pumping measurements are used to obtain interface density generation. Moreover, the total trap density which consists of interface trap density and bulk trap density is calculated from threshold voltage shift before and after stress. It expresses as follows

$$\Delta N_{total} = C\Delta V_{th} / qA_G \qquad (3\text{-}9)$$

and bulk trap density also can be calculated as follows

$$\Delta N_{bulk} = \Delta N_{total} - \Delta N_{it} \qquad (3\text{-}10)$$

Negative bias temperature instability (NBTI) is an important reliability issue as it causes the threshold voltage to shift with electrical stressing at elevated temperature. To evaluate device degradations due to the bias temperature stress (BT), the gate

electrode of the device was subjected to stress condition with negative bias (-3V) varying from 25℃ to 125℃, while the drain/source and substrate were all grounded. The detail process is the same as CVS process , except temperature variation. Fig. 3-3 shows the experimental framework of our measurements.

3-4 Reliability of Control and Fluorine-Incorporated Devices

3-4.1 CVS of control and Flourine-Incorporated Devices

Fig. 3-4 (a) and Fig. 3-4 (b) expresses I_d-V_g characteristics before stress and after stress at 25℃. We observe that there is no severe degradation of sub-threshold swing but positive V_{th} shift after stress is observed. This means that interface state generation plays no significant role, rather, charge trapping in the bulk dielectric is the primary mechanism leading to CVS issues in high-k dielectrics. V_{th} shift of the control sample is found to be slightly larger.

The threshold voltage shift (ΔV_{th}) is measured with respect to the I_d-V_g characteristics with and without fluorine incorporation shown in Fig. 3-5 in linear scale, and Fig3-6 in logarithm scale .The threshold shifts toward negative gate voltage ($\Delta V_{th} < 0$), thus implying that net positive charges are trapped in the gate dielectric layer as devices is measured. It is clear that fluorine-incorporated sample always

shows smaller ΔV_{th} than the control sample under different stress voltages as shown in Fig. 3-7. Fig. 3-6 shows that V_{th} degradation obeys the power law [22,27],

$$\Delta V_{th}(t) = At^b \qquad (3\text{-}11)$$

and the exponential values of both samples at vg=-3V(0.076 for control sample, and 0.54 for fluorine sample) are much larger than those of the device at Vg=-2V(0.022 for control sample, and 0.013 for fluorine sample) . This indicates that V_{th} degradation is more severe for the devices under larger constant voltage stressing. The exponential value is voltage dependent relative to bulk trap generation.

To further gain insights into the degradation mechanism during voltage stressing, the interface state generation, ΔN_{it}, and the increase of effective total trap density, ΔN_{tot}, are plotted as a function of the stress time in Fig 3-8(a)control sample ,and (b)fluorine sample ,respectively. Apparently, $\Delta N_{tot}(=\Delta N_{it+}\Delta N_{ot})$ is significantly larger than ΔN_{it}, suggesting that the degradation under CVS is dominated by the charge trapping in the bulk of HfO_2 film, rather than the generation of interface states, irrespectively of whether fluorine is added or not. The instability of HfO_2/SiON gate stack is mainly determined by the bulk charge traps, contrast to that in the SiON gate stacks. In addition, the improvement in charge trapping is larger than that in interface generation as shown in Fig. 3-9.

3-4.2 NBTI of Control and Flourine-Incorporated Devices

Fig. 3-10(a) and (b) expresses I_d-V_g characteristics before stress and after stress at 125℃. Compared Fig. 3-4 (a) and (b), we found that there is observable change in S.S at high temperature, compared to that at room temperature, indicating that ΔN_{it} increases with increasing temperature. This phenomenon is consistent with our results as shown in Fig. 3-11.

Fig. 3-12 and Fig. 3-13 compare the NBT-Stress-time dependence of threshold voltage shift for HfO_2/SiON gate stack with and without fluorine incorporation. A significantly smaller Vth shift is observed for the F-incorporated sample under the BT stress,V_g=-3V at 25℃ and 125℃ as shown in Fig 3-14. Such phenomena can be attributed to fluorine incorporation into gate dielectric. Fig. 3-14 also shows that the exponential values of both samples at 125℃ (0.106 for control sample and 0.093 for fluorine sample) are much larger than those of the devices at 25℃ (both about 0.056). This indicates that the V_{th} degradation could be more severe for the devices under BT stress at high temperature [28]. The exponential value is temperature dependent relative to bulk trap generation.

Fig. 3-15(a) and (b) show ΔN_{tot} as a function of time during NBTI for both devices measured at different temperatures. It is found that for both devices, V_{th} degradation during NBTI stressing. We found V_{th} degradation during NBTI stressing is serious in

control sample than in F-incorporated. Fig. 3-16 shows that F-incorporated sample has less ΔN_{tot} than control sample, this means less degradation in F-incorporated sample. Compared Fig. 3-11 with 3-15(b), we found that interface states is not the main reason of threshold voltage shift. This indicates that charge trapping in bulk is the main reason of threshold voltage shift. The research has pointed out that amount of bulk traps is one to two order higher than amount of interfacial traps [1].

3-5 Summary

In this work, we found F-incorporated sample has less degradation than control sample. From CVS measurements, the value of ΔN_{it} is similar to that of traditional SiO_2 dielectric. And the exponential value of ΔV_{th} is voltage dependent. From NBTI measurements, the exponential value of ΔV_{th} is voltage and temperature dependent. As result, we can confirm that charge traps in the bulk of HfO_2/SiON gate stack are responsible for the instability. We can expect a continuous distribution of charge trapping cross sections, instead of a discrete-value capture cross section, in HfO_2 high-k film [26]. A better interface is expected to help reduce V_{th} instability, therefore bulk traps need to be reduced. Our experimental also results show that hole trapping is dominant in DC stress.

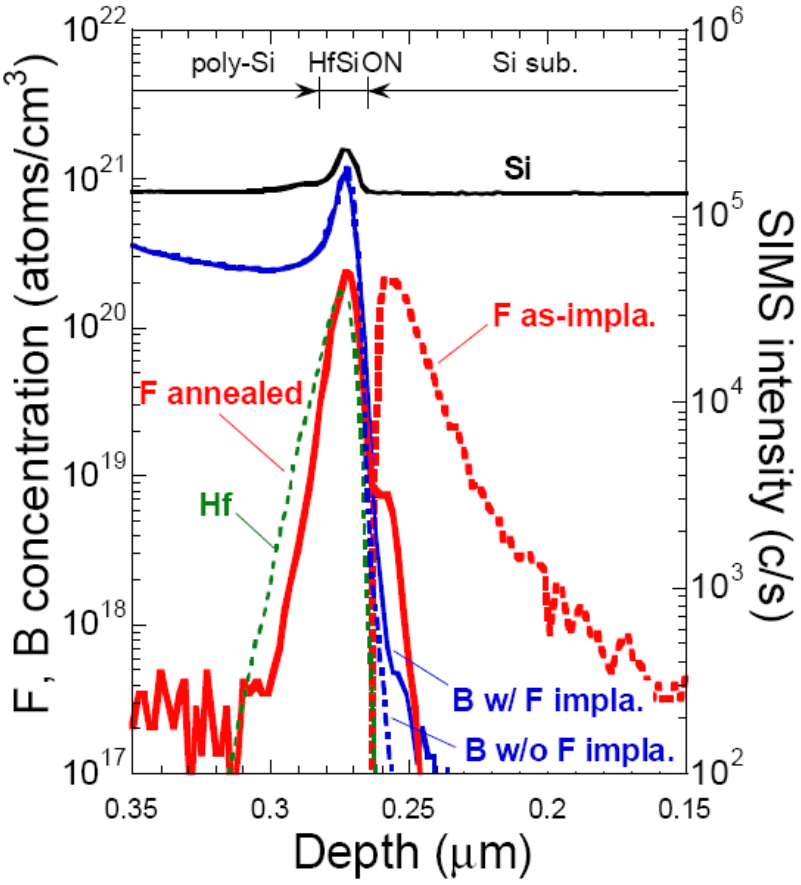


Fig. 3-1 SIMS profile of F and B atoms for as-implanted and after annealing with and without F implantation. (Ref[9])

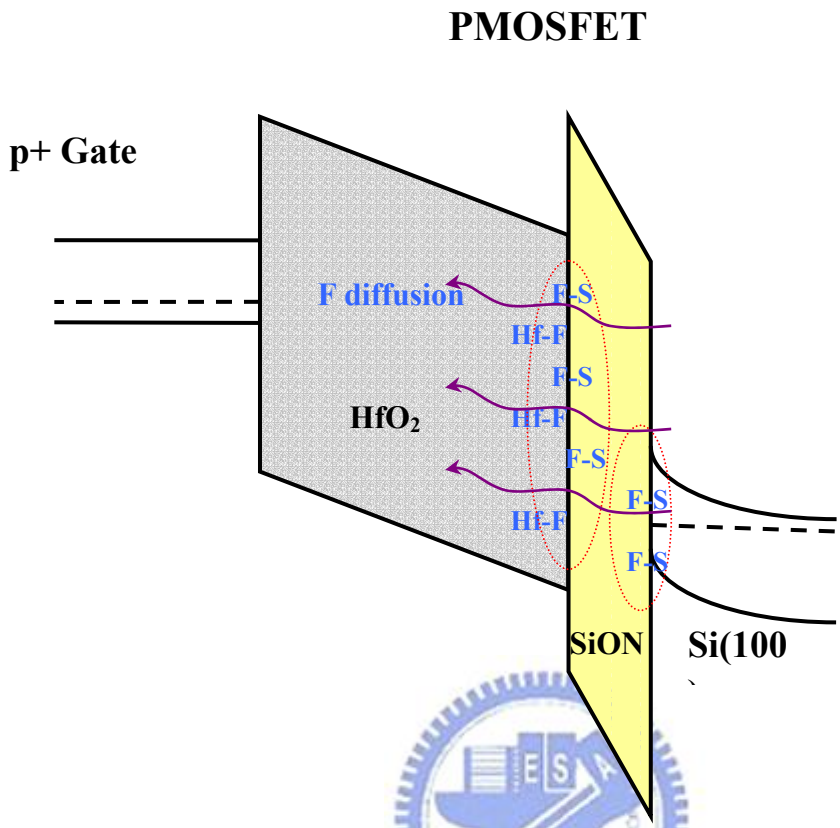


Fig. 3-2 Fluorine diffuses into HfO_2/SiON stack and forms stronger Si-F bonds compared to Si-H bonds , and reduce charging trapping by bonding to Hf dangling bond result in annihilation of oxygen vacancies.

$\triangle V_{th}$ & $\triangle N_{it}$

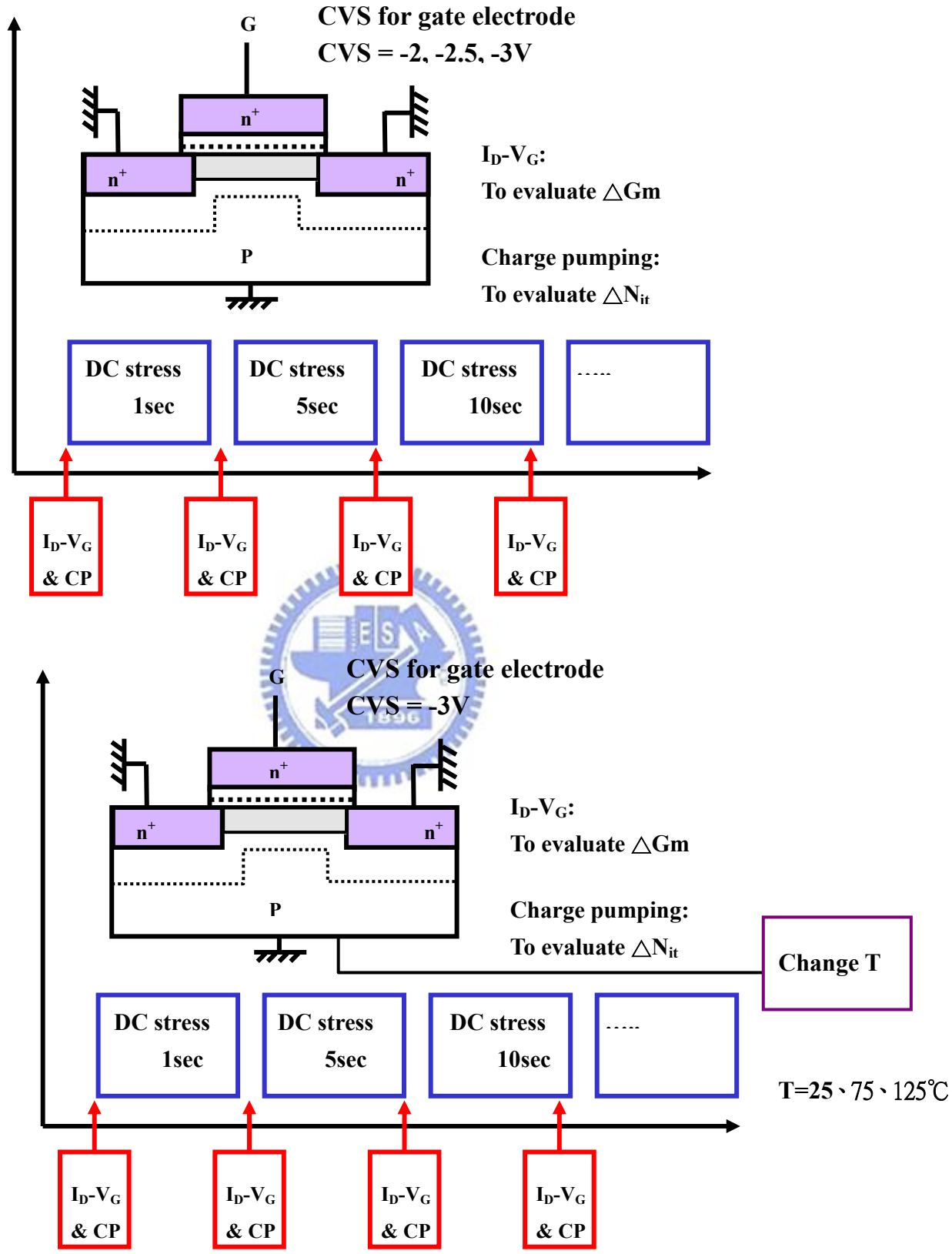
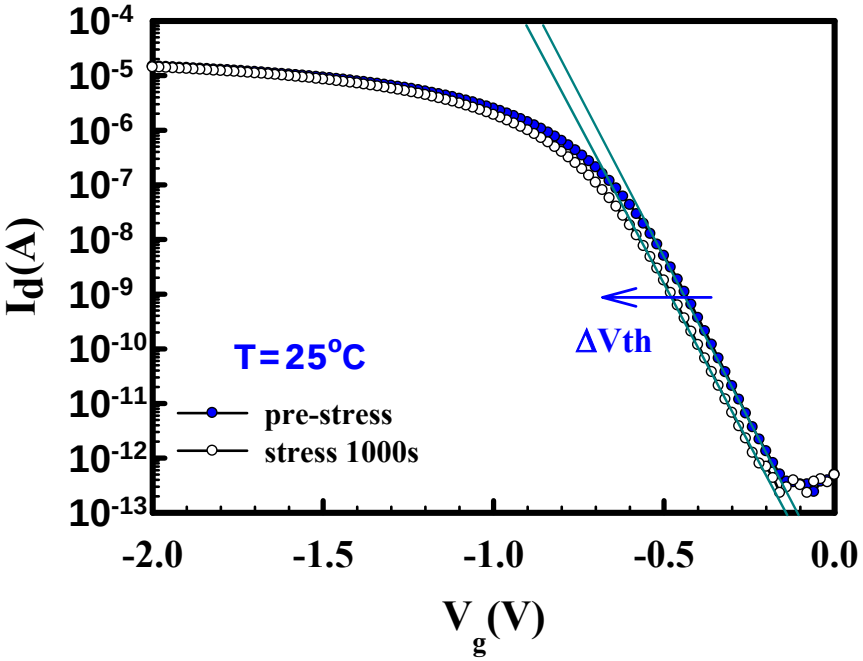
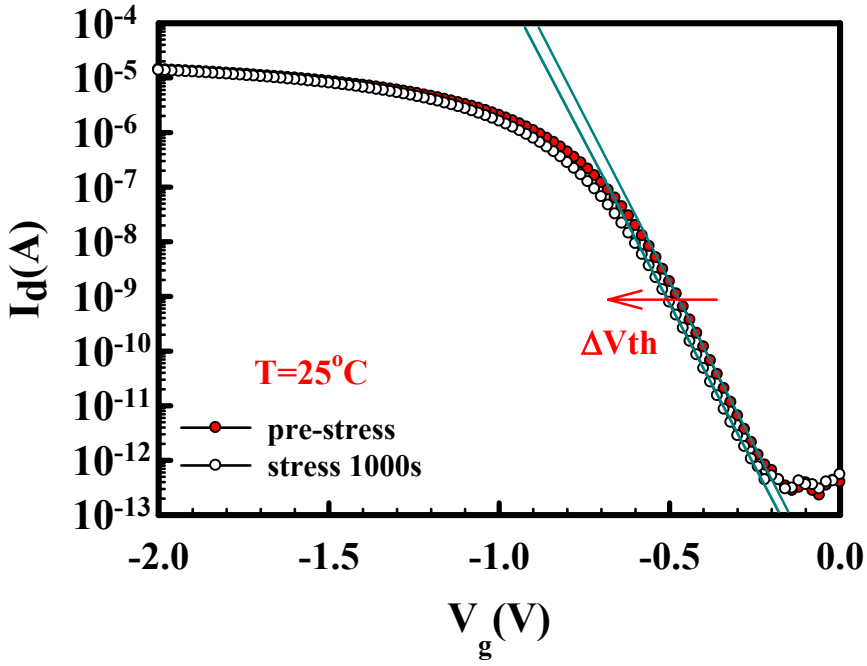


Fig. 3-3 Basic measurement method for (a) CVS (constant voltage stress), and (b)NBTS (negative bias temperature stress).

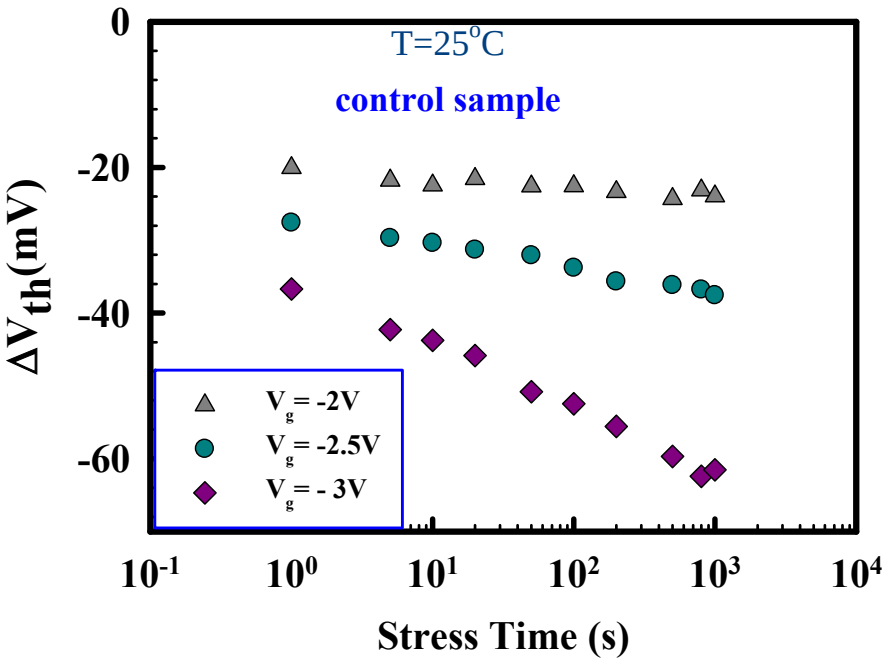


(a)

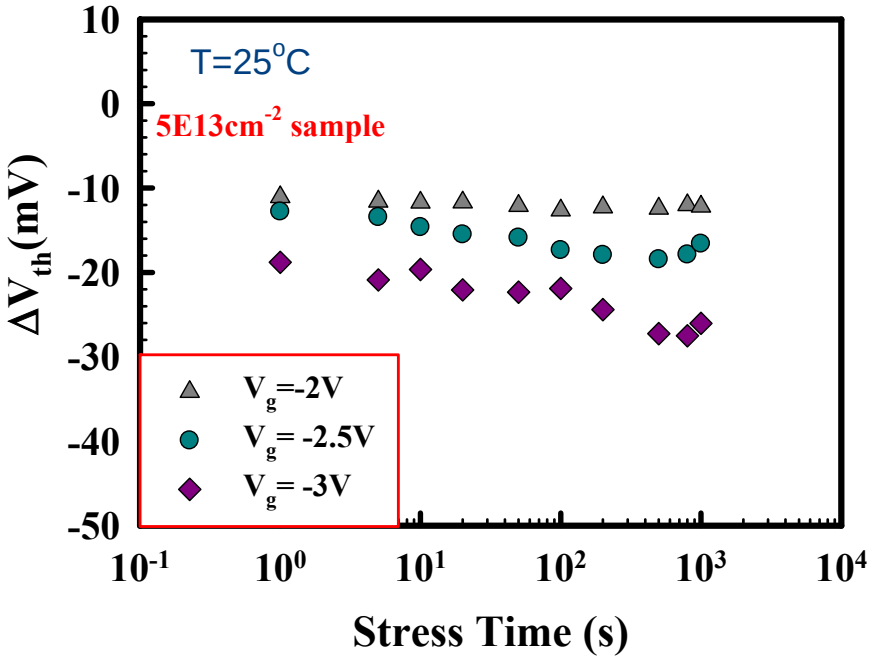


(b)

Fig . 3-4 I_d-V_g characteristics for p^+-gated pMOSFETs before and after stress1000 at 25℃ (a) control sample, and (b) fluorine sample.

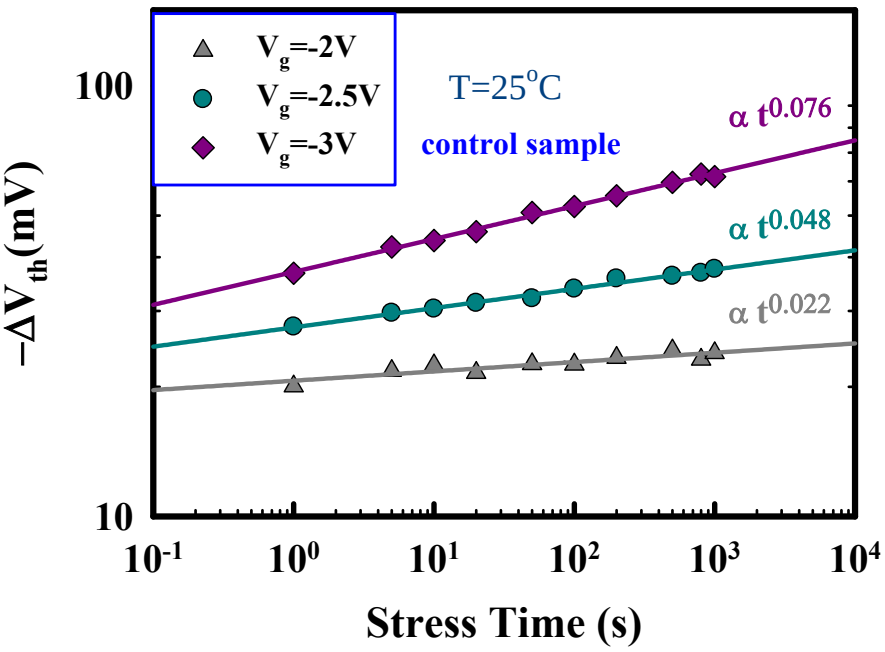


(a)

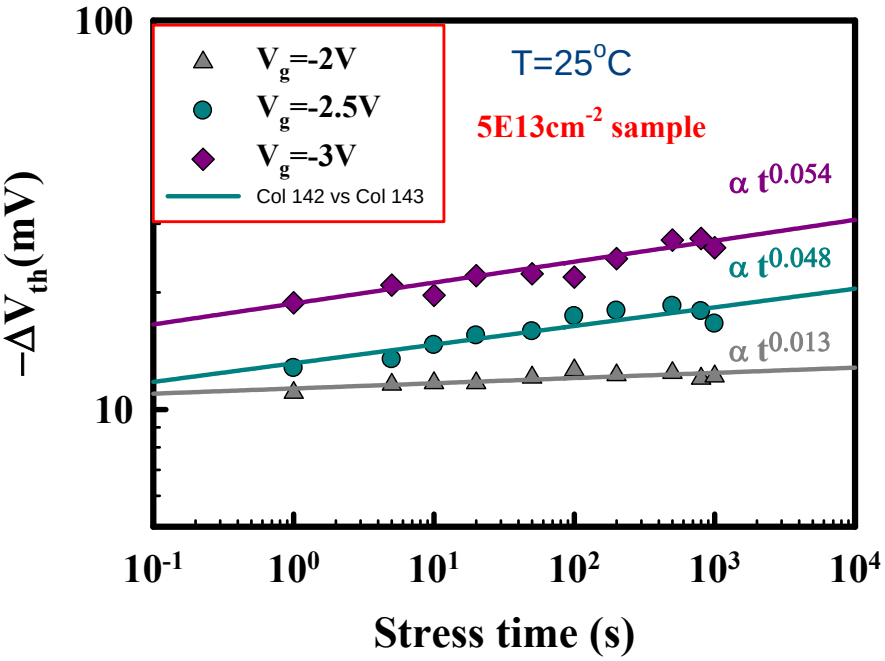


(b)

Fig. 3-5 Threshold voltage shift as a function of stress time, stressed at 25℃, Vg= -2~ -3V in linear scale (a) control sample ,and (b) fluorine sample



(a)



(b)

Fig. 3-6 Threshold voltage shift as a function of stress time, stressed at 25℃, Vg= -2~ -3V in linear scale (a) control sample ,and (b) fluorine sample.

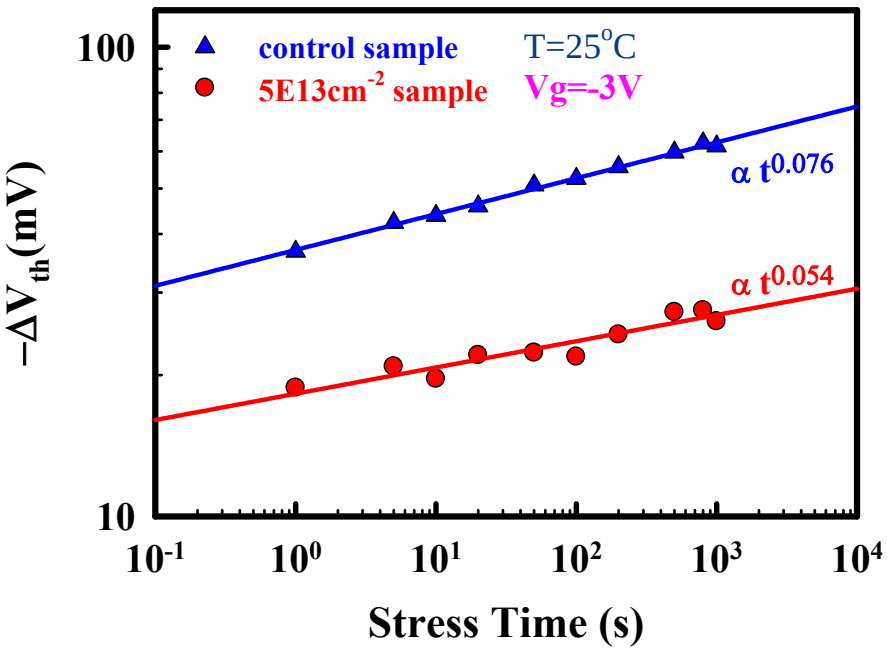
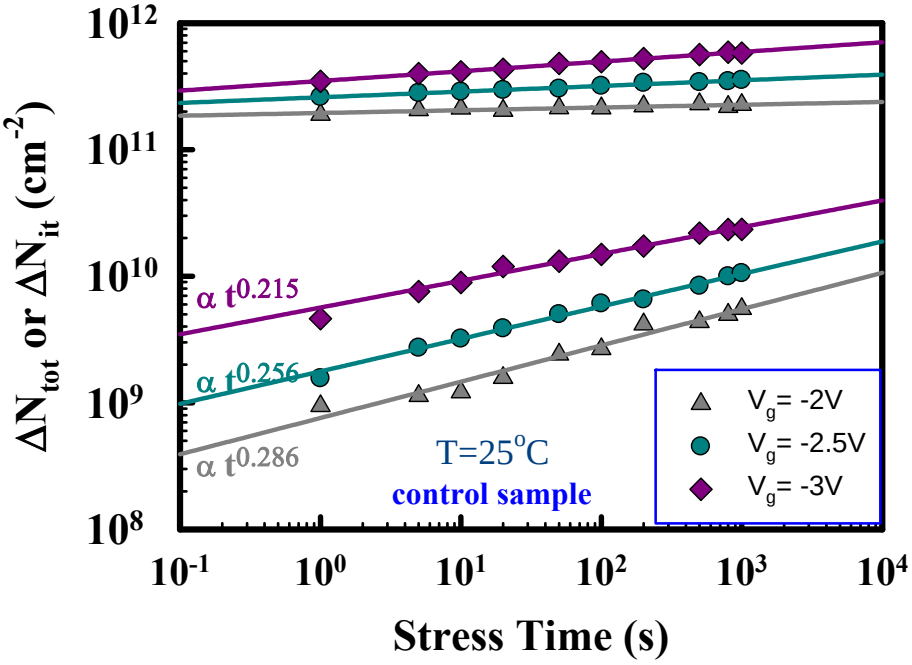
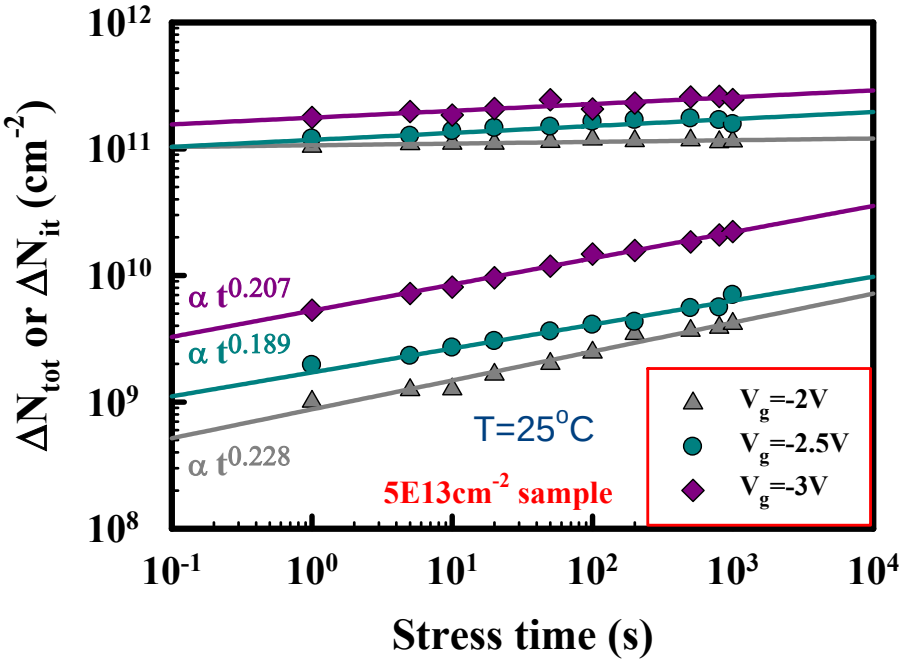


Fig 3-7 Control and fluorine-incorporated sample as function of stress time, stress at 25℃, V_g=-3V.



(a)



(b)

Fig. 3-8 Interface trap density shift , and total trap density increase as a function of stress time (a)control sample ,and (b) fluorine sample.

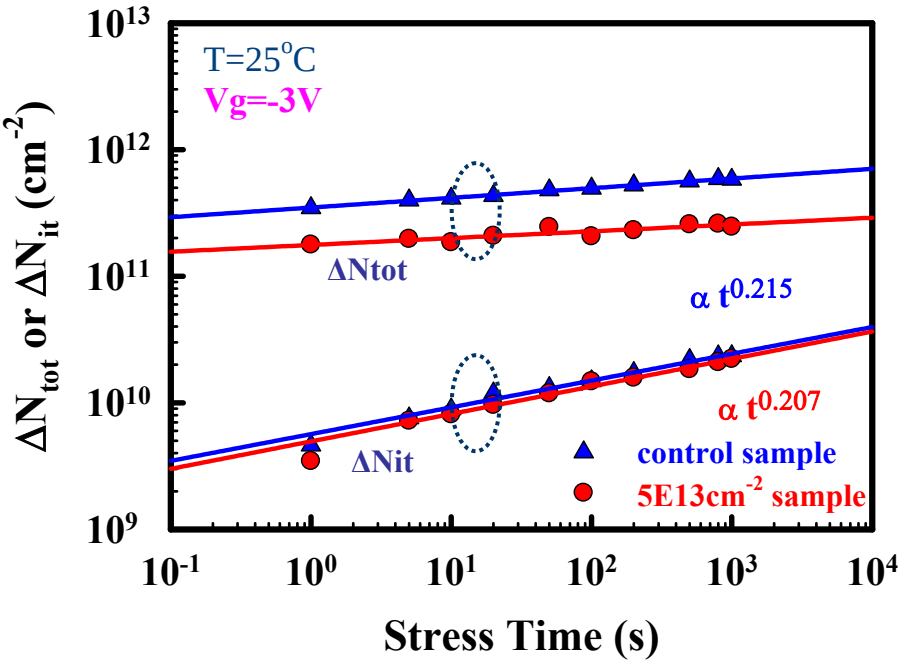
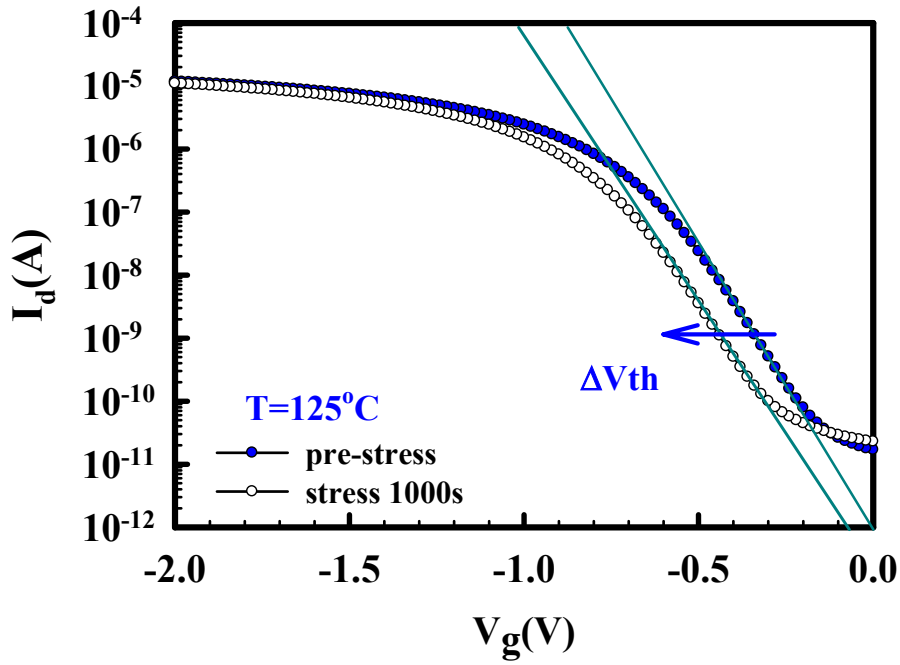
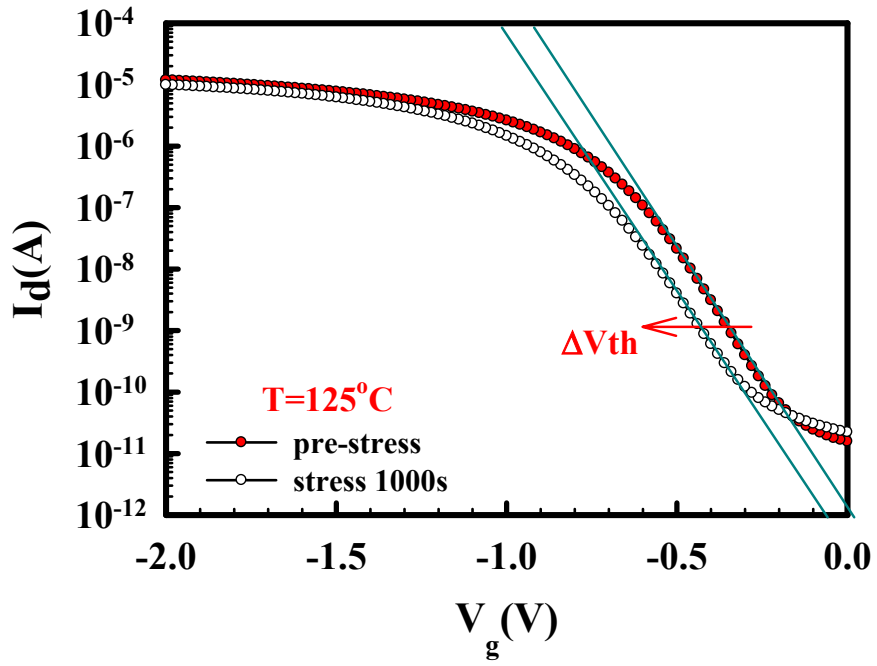


Fig 3-9 interface state increase and total trap density increase versus stressing time for control and fluorine-incorporated sample, stressed at 25℃, Vg=-3V.



(a)



(b)

Fig . 3-10 I_d-V_g characteristics for p^+-gated pMOSFETs before and after stress1000 at 125℃ (a) control sample (b) fluorine sample

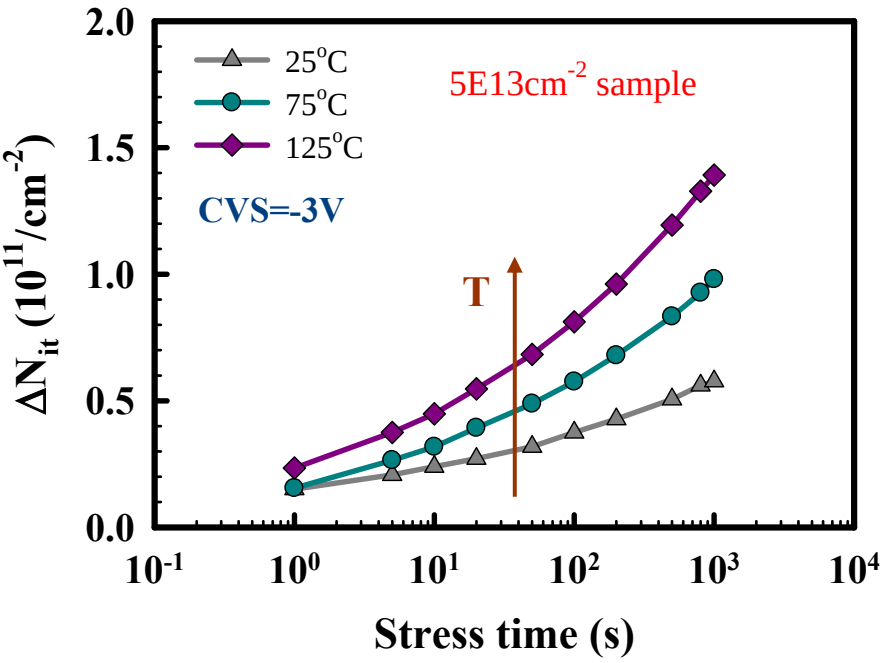
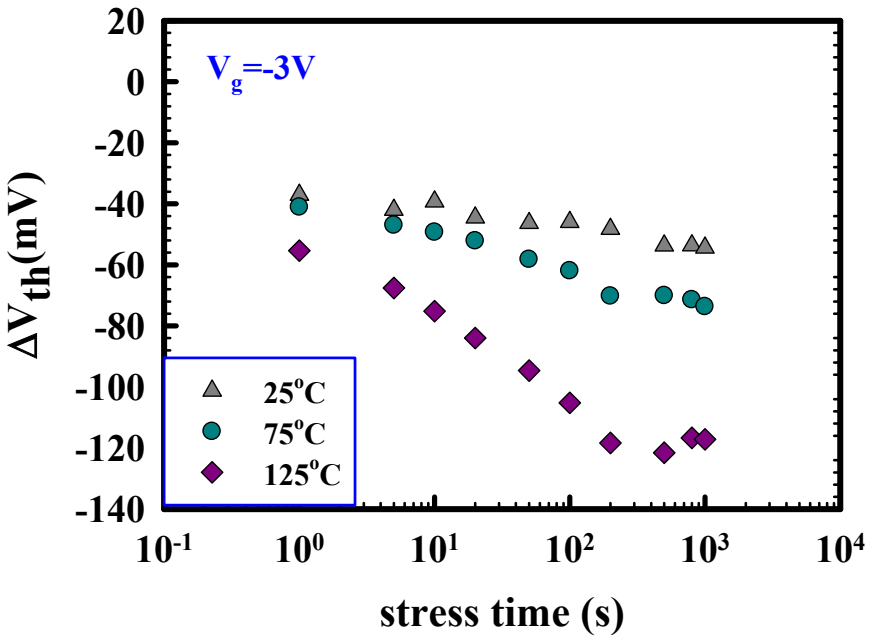
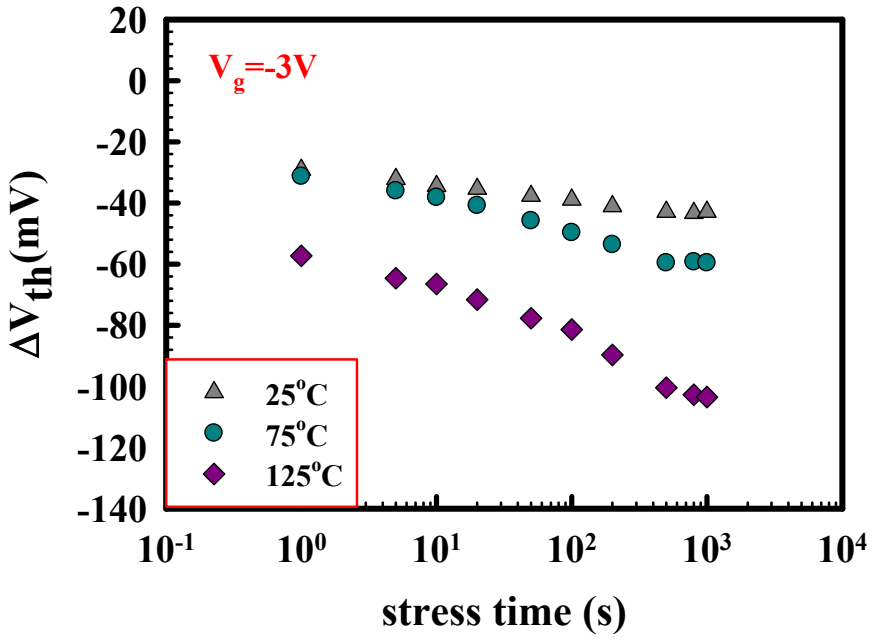


Fig. 3-11 Interface trap density shift as function of stress time under BTS at different stress temperature, Vg=-3V , with fluorine sample

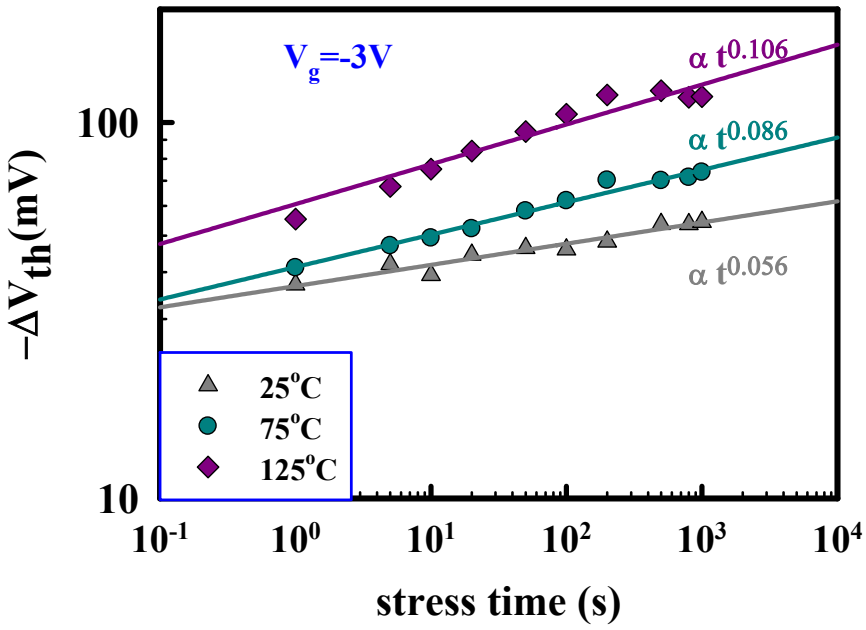


(a)

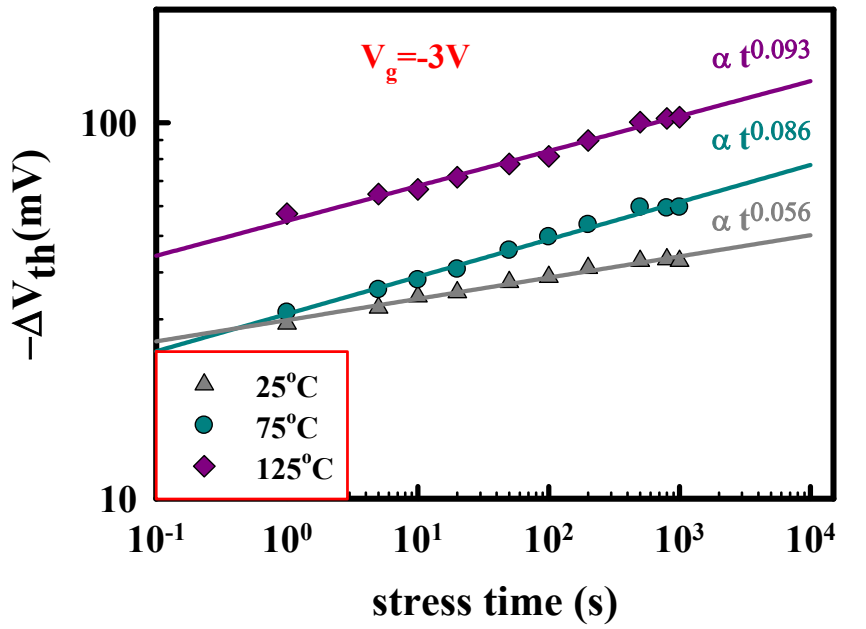


(b)

Fig. 3-12 Threshold voltage shift as a function of stress time under BTS at different stress temperature , V_g=-3V in linear scale (a) control sample, and (b) fluorine sample.



(a)



(b)

Fig. 3-13 Threshold voltage shift as a function of stress time under BTS at different stress temperature , V_g=-3V in logarithm scale (a) control sample, and (b) fluorine sample.

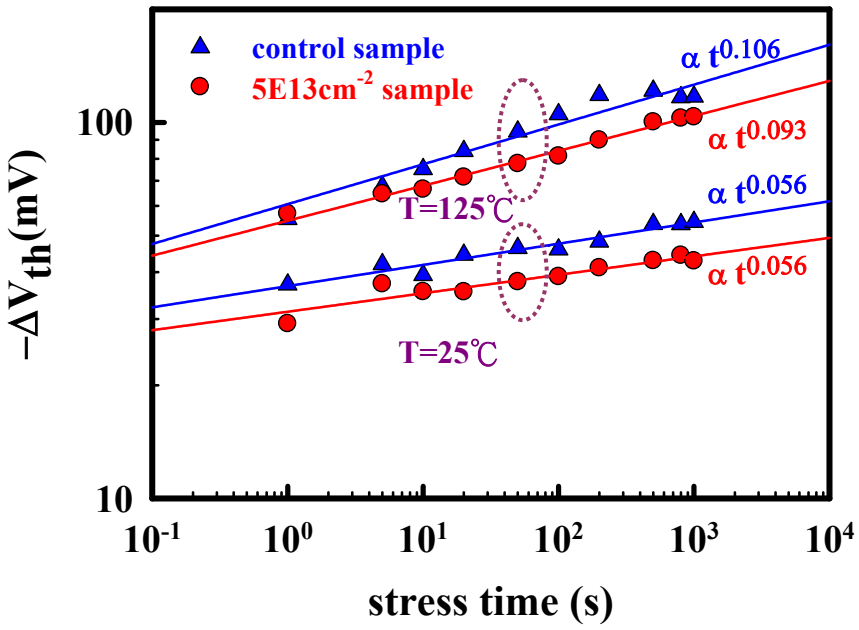
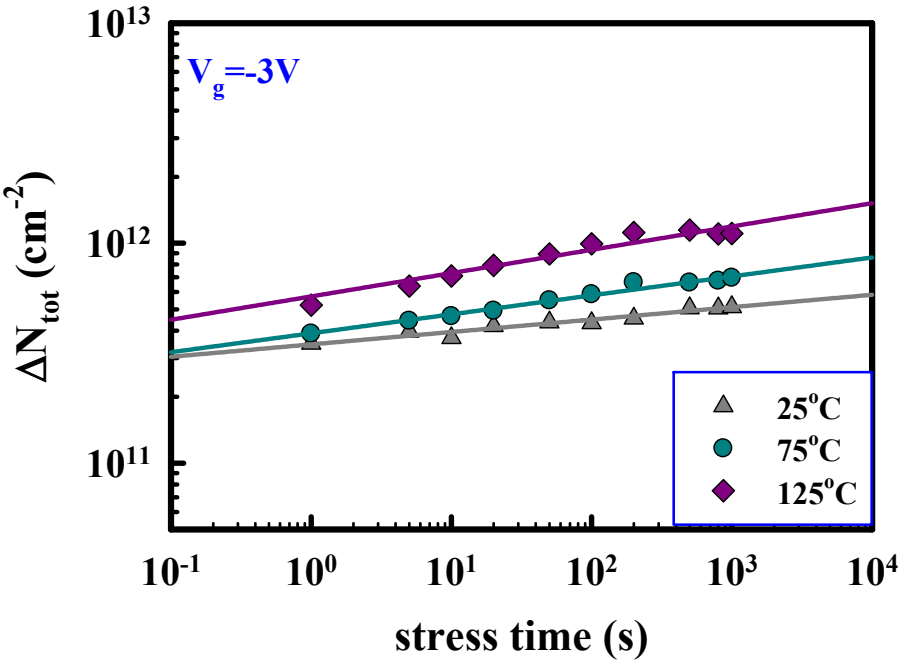
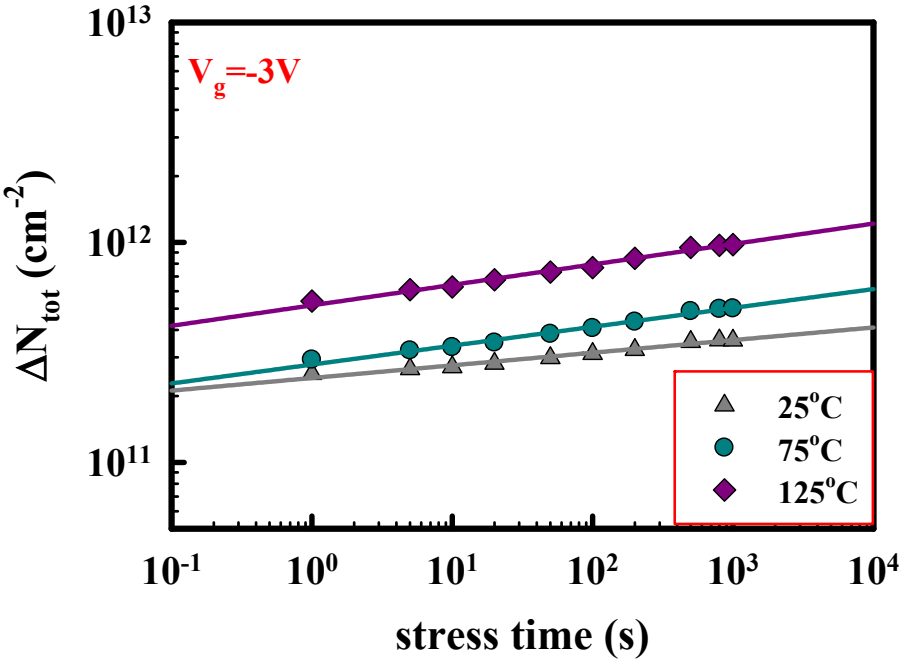


Fig. 3-14 Control and fluorine-incorporated sample as function of stress time under BTS at 25℃ and 125℃，V_g=-3V



(a)



(b)

Fig. 3-15 Total trap density increase as a function of stress time under BTS at different stress temperature , V_g=-3V (a) control sample , and (b) fluorine sample

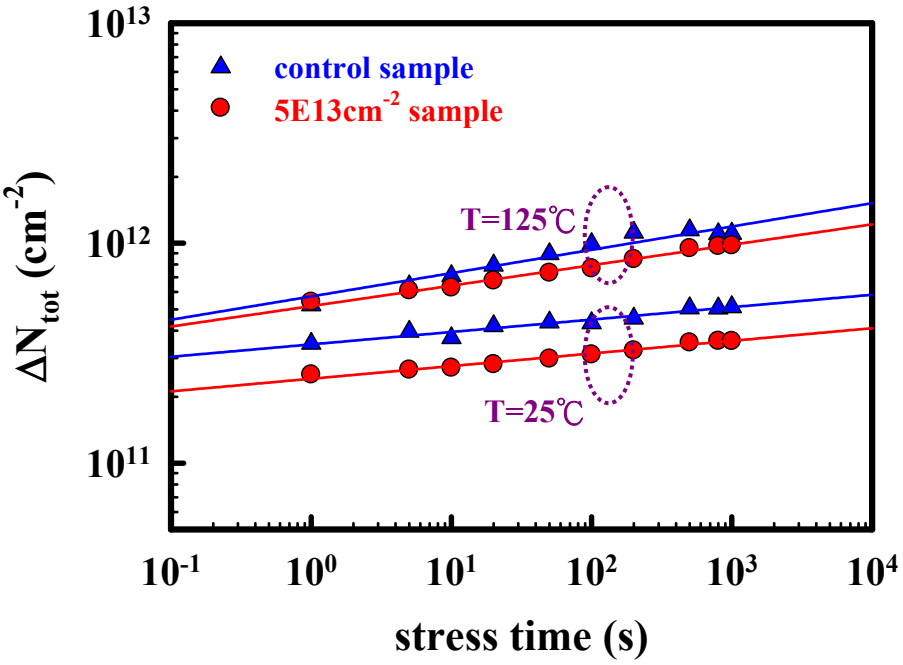


Fig. 3-16 Total trap density increase as a function of stress time under BTS at different stress temperature , V_g=-3V for device with and without fluorine incorporation.

Chapter 4

Conclusions and Future Work

4.1 conclusion

In this thesis, the effects of fluorine incorporation into HfO_2/SiON gate stack were investigated. Several important phenomena were observed and summarized as follows:

First, we have investigated its basic electrical properties. The initial electrical properties of the devices are smaller affected by fluorine incorporation. The gate leakage current is analyzed by the carrier separation measurement, and can be explained by the band structure of the gate stack. The source/drain current I_{SD} that corresponds to the hole current dominates the leakage under inversion region, while the substrate current IB that indicates the electron current dominants the leakage current under accumulation region. All leakage current can be categorized by fitting to be of Frenkel-Poole type.

Secondly, we have studied the CVS and NBTI mechanisms of polysilicon gate HfO_2 dielectric, with and without fluorine incorporation. ΔV_{th} is primarily caused by the charge traps in the HfO_2 dielectric, not by the interfacial degradation. Fluorine incorporation is effective in suppressing ΔN_{tot}, thus improving threshold voltage instability.

4.2 Future Work

There are some evidences and measurements skill we can't complete. We list some goals for future works as follows:

(i) HRTEM is used to verify real thickness and estimate value of the dielectric constant for HfO_2/SiON gate stack.

(ii) SIMS analysis is used to prove fluorine exist in fluorine-incorporated device, and calculate which quantity exists in.

(iii) In actual CMOS circuit operation, AC gate bias with specific frequency and duty cycle is usually utilized. Therefore, AC stress with dynamic AC stress application is more realistic and can provide additional insights into the trapping behavior.

(iv)Fast transient pulsed I_d-V_g measurement is also used to evaluate charge-trapping phenomena precisely.

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簡歷

姓名: 王信智

性別: 男

年齡: 24 (民國 72 年 8 月 30 日)

籍貫: 台灣省台南市

學歷: 國立中山大學物理學系學士 (90.9-94.6)

國立交通大學電子工程研究所 (94.6-96.7)

碩士論文題目:

Effect of Fluorine Incorporation on the Reliability Issue of pMOSFETs with HfO2/SiON Gate Stack

氟摻雜對二氧化鉿堆疊式閘極P型金氧半場效電晶體其可靠性的影響