國立交通大學

電子工程系　電子研究所

碩士論文

金屬奈米點記憶特性及研究

The memory characterization and investigation of metal nanocrystal

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指導教授：羅正忠　博士　　Dr. Jen-Chung Lou

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摘要

早期非揮發性記憶體的製作，是採用整層的複晶矽的浮停閘(Floating Gate)結構，利用此層來當電子的儲存層，當電子由通道注入到這層浮停閘之後，會影響到元件的臨界電壓值(Threshold voltage)，藉由判別臨界電壓的電壓值大小，即可定以邏輯的 “0” & “1” 狀態。但是，因為這種浮停閘結構為整層的半導體薄膜，在電子反覆的從穿遂氧化層進出這層浮停閘，會使得穿遂氧化層裂化以至於出現缺陷，當缺陷一產生之後，所有儲存的電子將會隨這這層缺陷而有了漏電路徑，導致所寫入的電子全部流失掉，無法達到記憶的效果。然而在不久的將來，會因為成本的考量，將元件尺寸縮小至奈米等級，如此一來浮停閘結構所能儲存的電子量也會隨之減少，以至於不足造成臨界電壓的漂移。而尺寸微縮的同時穿遂氧化層的厚度也會隨之減少，以至於此結構記憶體可靠度不佳，這種結構認為到元件微縮至奈米等級左右便是此浮停閘結構的極限。為了應付未來大容量記憶體的需求，科學家努力的研發各種可以取代之的非揮發性記憶體如 PCM、FeRAM、

MRAM 等……

而在這個過渡時期，如何利用現有的技術，帶領快閃記憶體(Flash Memory)在繼續的走過下一個世代。許多研究論文提出了利用半導體或金屬的奈米點來當作電子的儲存層。利用奈米點的好處是，各個奈米點之前被絕緣體所包圍，所以當穿遂氧化層產生缺陷後，電子不會全部流失掉，僅僅流失掉缺陷附近儲存的電子，所以可以進一步應付尺寸的微縮和增加電子的保存能力(retention)。降低穿遂氧化層厚度，使得可以減少操作電壓，增加電子寫入的效率。此外，利用金屬奈米點電晶體還有幾個好處，一個是他能擁有高的狀態密度，再來就是金屬較半導體有著更大的功函數，當電子注入到金屬奈米點之中後是儲存在較深層的能階中，它所看到的能障較高，不易因鄰近元件的操作造成擾動，預期也能提升電子的保存時間。再來，因為各個奈米點注入了電子後，會因為庫倫阻絕(Coulomb blockade)效應，所儲存的電子會排斥後續電子的寫入。故在低電壓操作模式下(例如讀取時)，電子不易被寫入到奈米點內，也就是有比較少的讀取干擾，在辨別邏輯 “0” & “1” 上會較為容易。

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ABSTRACT

In early time, manufacture the nonvolatile memory uses poly-silicon layer treated as electron storage layer named floating gate(FG). When electron inject to this layer from channel. That will be influence the threshold voltage. Two state threshold voltages constitute logic “0” & “1”. For FG structure, the oxide has a defect because of electron repeat impact during the write/erase cycle, all of the charge stored in FG will be lose. FG structure will have reliability problem when device scale down to nano-meter level.

How can use existing technology leads flash memory to pass through the next generation in the continuation. Many research papers proposed the electron storage

layer made by semi-conduct or metal nano-crystal. The benefit is that nano-crystal surrounded by dielectric. When oxide has defect merely lose the electron which nearby the defect stores up. So nano-crystal device can maintain good retention characteristics. Therefore may further deal with the aggressive size scale down, reduce tunneling oxide thickness, may reduce the operation voltage, the efficiency which the increase electron writes in. Otherwise metal nano-crystal has higher density of states, and the design freedom of engineering the work functions to optimize device characteristics. Coulomb blockade effect can effectively inhibit electron tunneling at low gate voltage and improve the flash memory array immunity to read disturbance, can easy recognize logic “0” & “1”.

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Chapter 1
Introduction

1.1 General Background

Since 1960 ages, the first semiconductor transistor is invented. One of great invention is semiconductor memory, semiconductor memory market is expected will have great increase. These memories approximately divide into two categories: random access memories (RAM's) and read-only memory (ROM's). See Fig. 1-1. These two kinds of memories most different in data retention. Data will be reserved or said nonvolatile after power off named ROM, opposite one data will be lost or said volatile after power off named RAM. The volatile memories like SRAM or DRAM, that very dense and have fast speed in writing and reading. RAM is massive applied in computer industry. The nonvolatile memories like EPROM, EEPROM, or Flash, are able to balance the less-aggressive programming and reading performances with no volatility.

Driven by cellular phones, other types of electronic portable equipment (palm top, mobile PC, mp3 audio player, digital camera, and so on) and wireless communication devices, semiconductor memories have been the explosive growth of the Flash memory market. In the future, portable systems will demand even more nonvolatile memories, either with high density and very high program speed for data storage application.

In 1967, D. Kahng and S. M. Sze invented the first floating-gate nonvolatile semiconductor memory at Bell Labs [1.1]. The FG structure device show in Fig. 1-2. It has a poly-silicon gate completely surrounded by dielectric. The floating gate is electrically governed by a capacitive couple control gate (CG). When electrons injected to the floating gate from channel, electrons in the floating gate will influence device threshold voltage, use the threshold voltage difference to recognize logic "0" & "1". Several physical mechanisms are available to accomplish this charge transfer, but the most commonly used ones are either channel hot electron injection (CHEI) or Fowler-Nordheim (FN) tunneling for the write operation, and FN tunneling for the erase operation.

The stacked-gate FG device structure continues to be the most prevailing nonvolatile semiconductor memory(NVSM) implementation, and is widely used in both standalone and embedded memories, and in both code and data storage applications. Although convention FG memories have many advantages over other kinds of nonvolatile memories, it still comes to be in face of their limitation from scaling down issues for the coming generation [1.2]. For conventional floating-gate memories, which offer longer than ten years of data retention time. But have drawbacks of high operation voltage and slowly write/erase speed because of their relatively thick tunnel oxide. Uses the thinner tunnel oxide can resolve the problem above, but why we can't use the thinner oxide as tunnel oxide? The reason is that: (1) when electrons stored in FG, it can tunnel back to channel, so that data can't reserve ten years. Use thicker tunnel oxide can reduce the probability of tunnel back. (2) since poly-silicon is a conducting material, once the tunnel oxide develops a leaky path under repeated write/erase operation, all the store charge will be lost. Therefore the thickness of tunnel oxide can not be scaled down. A thick tunnel oxide requires a high

operation voltage for write/erase, the power consumption will be high, and operation speed will be slower, but only can get good data retention. There is a trade-off between operation speed and data retention.

To overcome the scaling limits of the conventional FG structure, two candidates are mostly mentioned that are SONOS (poly-Si/oxide/nitride/oxide/silicon) [1.3-1.4] and nanocrystal memories [1.6-1.9]. The SONOS structure show in Fig. 1-3, the nitride layer is used as the charge trapping element, and nanocrystal structure show in Fig. 1-4. The basic idea of the "discrete-trap" mechanism is to replace the floating gate of nonvolatile memories by many discrete trapping centers, which can be made by natural traps in an appropriate insulator (for SONOS structure use nitride layer) or by semiconductor nanocrystals (usually silicon dot). The intrinsic distributed storage takes an advantage of SONOS device and nanocrystal device than the FG device, since a single defect will not cause the discharge of memory. Charge trapped in discrete trap centers are more immune to the leakage caused by localized oxide defects, thus allowing more aggressive scale down for the next generation.

1.2 Organization of this thesis

This thesis is divides into several parts. The detail content is describe as follow.

In chapter 1, we introduced the memory type. Then simply introduce two kinds of nonvolatile memory structure. Also show the nonvolatile memory innovations.

In chapter 2, we introduced the two kinds of nonvolatile memory structure and its operation mechanism in physic view.

In chapter 3, this chapter introduces experiment flow and measures these samples. And discuss and analyze the result.

In chapter 4, We make a brief conclusion and future work in the last chapter.

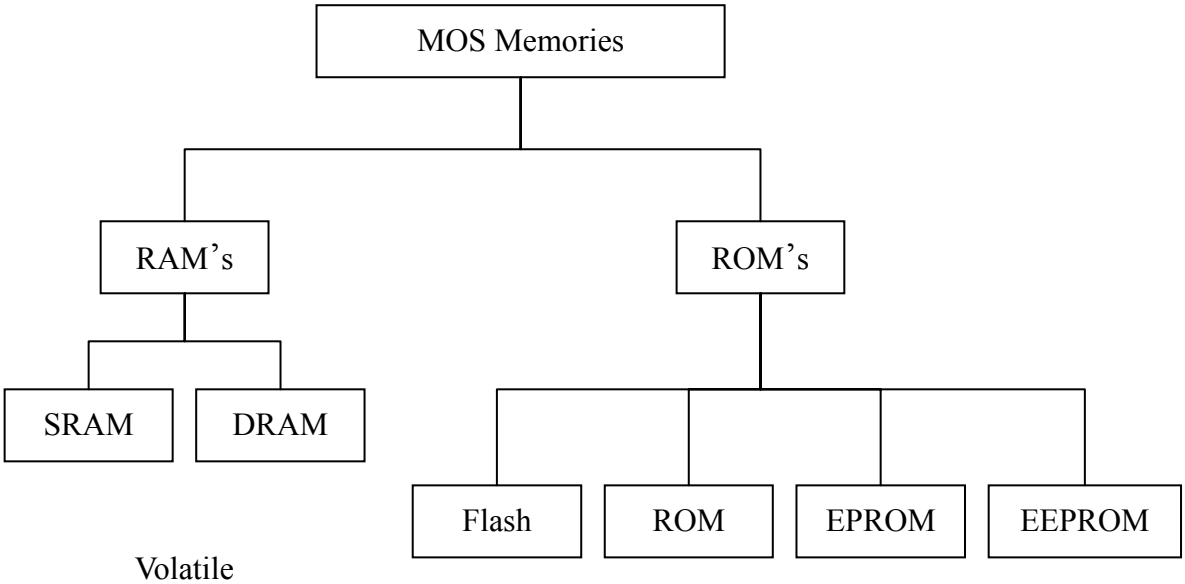


Fig. 1-1 MOS Memory tree

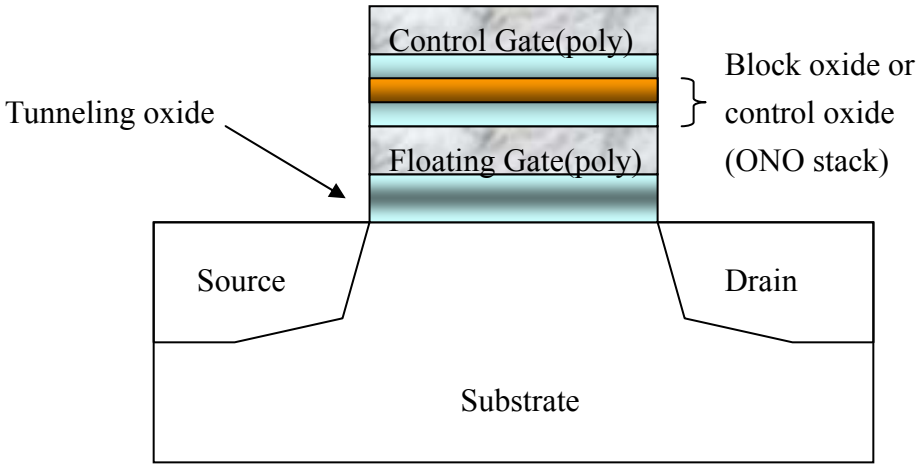


Fig. 1-2 FG structure memory

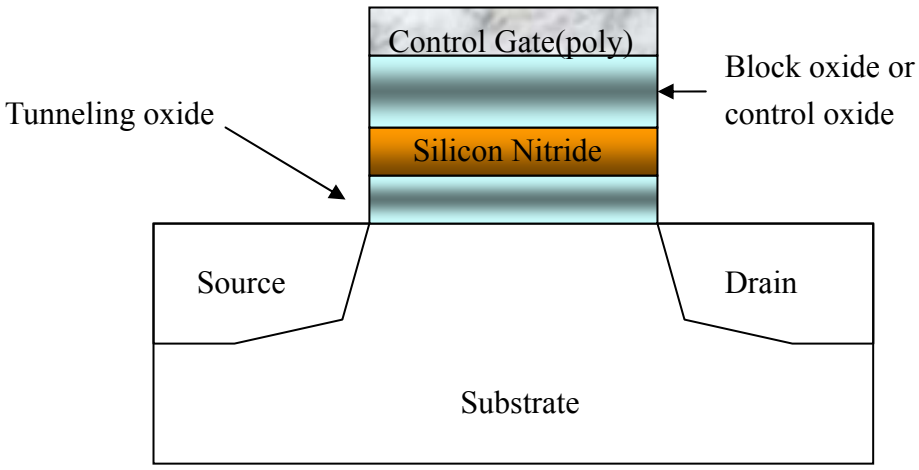


Fig. 1-3 SONOS structure memory

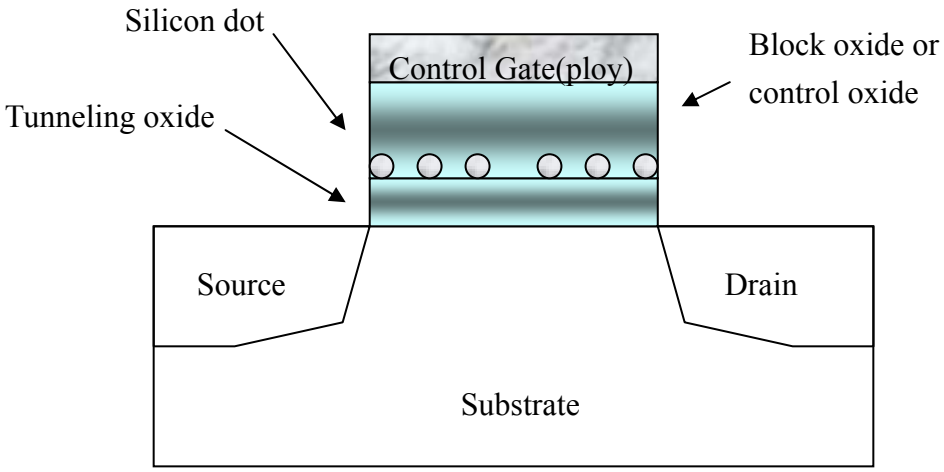


Fig. 1-4 Nanocrystal structure memory

Chapter 2
Nonvolatile memory basic concept and operation mechanism

2.1 Introduce

2.1.1 SONOS nonvolatile memory devices

SONOS structure nonvolatile memory, charge traps distributed throughout the volume of the nitride layer. A typical trap has a density of the order 10^{18}-10^{19} cm^{-3} according to Yang et al [2.1]. SONOS nonvolatile semiconductor memories meet the memory challenges of scaling down issue. In general, NVSMs are required bear to 10K-100K times write/erase cycles (endurance) with 10-years memory retention at the temperatures as high as 125℃. The term “endurance” refers to the ability of the NVSM to bear repeated program cycles and still meet the specification. The term “retention” describes the ability of the NVSM to store and recover information after a number of program cycles at specified temperature.

The SONOS memory device has received a lot of attention due to its advantages over the traditional FG memory device. These include reduced process complexity, lower voltage operation, improved cycling endurance, and elimination of drain induced

turn-on [2.2]. In SONOS memory device with SiO_2 tunnel dielectric, the electrons and holes must tunnel through 3.15eV and 4.5eV energy barriers, respectively, to be injected into the Si_3N_4 charge trap layer. The energy band diagram during retention is show in Fig. 2-1. It can compare to the FG structure band diagram during retention show in Fig. 2-2. For FG structure, the electrons injected from the channel are trapped in poly-silicon conduction band. For SONOS structure, the electrons injected from the channel are trapped in forbidden gap below the nitride conduction band (label with the trap energy level of E_t). In this device, the electrons cannot move freely between the discrete trap locations, hence the SONOS memory device is very robust against the defects inside the tunnel oxide and has better endurance than the floating gate flash memory. In the retention mode, electrons can leak to the substrae through the direct tunneling process shown as path "1" in Fig. 2-1. However, in this device the escape frequency is very small. Alternatively, electrons can be thermally de-trapped into the nitride conduction band and then tunnel back to the channel (this is path "2" in the fig. 2-1). This thermal de-trapping rate is exponentially reduced with a deep trap energy level. For these reasons, the SONOS flash memory can have much better retention time than the floating gate flash memory. A tunnel oxide of 3nm is thick enough to guarantee 10 years retention time in the SONOS flash memory.

2.1.2 Nanocrystal nonvolatile memory devices

In a nanocrystal NVM device charge is not stored on a continuous FG poly-Si layer, but instead on a layer of discrete, mutually isolated, crystalline nanocrystals or 'dots,' typically made of semiconductor material. Nanocrystal memories, first introduced in the early nineties [2.3], are one particular implementation of that concept.

That use silicon nanocrystals as the trapping material [2.4-2.5]. So the nanocrystal memory can robust against the defects inside the tunnel oxide like SONOS memory, and each dot will typically store only small amount of electrons. Collectively the charges stored in these dots control the channel-conductivity of the memory transistor.

As compared to conventional stacked-gate NVM devices, nanocrystal charge-storage offers several advantages, the main one being the potential to use thinner tunnel oxides without sacrificing nonvolatility. This is a quite attractive proposition, since reducing the tunnel oxide thickness is key to lowering operating voltages and/or increasing operating speeds. This claim of improved scalability results not only from the distributed nature of the charge storage, which makes the storage more robust and fault-tolerant, but also from the beneficial effects of Coulomb blockade [2.6]. Quantum confinement effects (band gap widening; energy quantization) can be exploited in sufficiently small nanocrystal geometries (sub-3 nm dot diameters) to further enhance the memory's performance.

There are other important advantages though. First, nanocrystal memories use a more simplified fabrication process as compared to conventional stacked-gate FG NVM's by avoiding the fabrication complications and costs of a dual-poly process. Further, due to the absence of drain to FG coupling, nanocrystal memories suffer less from drain-induced-barrier-lowering (DIBL) and therefore have intrinsically better punchthrough characteristics. One way to exploit this advantage is to use a higher drain bias during the read operation, thus improving memory access time. Alternatively, it allows the use of shorter channel lengths and therefore smaller cell area (i.e., lower cost). Finally, nanocrystal memories are characterized by excellent immunity to stress induced leakage current (SILC) and oxide defects due to the distributed nature of the

charge storage in the nanocrystal layer.

For fabrication demand, a typical requirement the aerial density of nanocrystal dots is at least $10^{12}cm^{-2}$. This is equivalent to approximately 100 particles controlling the channel of a memory FET with a 100 100 nm active area, and requires particle diameters of 5–6 nm and below. And the fabrication process should result in a planar nanocrystal layer, i.e., the thickness of the dielectric layer separating the nanocrystal and the substrate should be well controlled. Poor control of the tunnel oxide thickness will result in wider threshold voltage distributions and will increase the number of erratic bits. More generally, good process control is needed with regards to such nanocrystal features as: size and size distribution; inter-crystal interaction (lateral isolation); uniformity of aerial crystal density; and crystal doping (type and level). Finally, it is preferred that that the fabrication process is simple and that it uses standard semiconductor equipment.

Several nanocrystal fabrication processes have been demonstrated. King *et al*. [2.7] used Ge ion implantation subsequent high-temperature wet oxidation, which causes the implanted Ge atoms to pile up at the Si/SiO_2 interface. And the number of electrons trapped in the Ge nanocrystals was estimated to be $3.5\times10^{12}cm^{-2}$. Lin *et al*. [2.8] make HfO_2 by co-sputtering with pure silicon (99.9999% pure) and pure hafnium(99.9% pure) targets in an oxygen gas ambient deposition a 12-nm amorphous HfSiOx silicate layer. Then samples were subjected to RTA treatment in an O_2 ambient at 900℃ for 1 min to convert the HfSiOx silicate film into the separated HfO_2 and SiO_2 phases, the diffraction patterns show the cell size is 5–8 nm, and the dot density is $0.9\text{-}1.9\times10^{12}cm^{-2}$. Deposition the metal wetting layer 1-5nm, then the film is annealed at elevated temperatures close to its eutectic temperature with the substrate in an inert

ambient to transfer the wetting layer into nanocrystals. This process is achieved through the relaxation of film stress and limited by the surface mobility [2.9]. Other than use deposition method, some special techniques formation nanocrystal are using ion implant [2.10-2.11] and sol-gel-spin-coating [2.12].

Nanocrystal memories have been presented in the midnineties as a possible alternative to conventional FG NVM devices, by allowing a further decrease in the tunnel oxide thickness. In particular, nanocrystal memories promise to enable a further scaling of the tunnel oxide, by relying on Coulomb blockade effects in small semiconductor geometries and on the enhanced robustness and fault-tolerance of distributed charge storage.

Research in this area has focused on the development of nanocrystal materials and fabrication processes, and on the integration of nanocrystal-based storage layers in actual memory devices. Promising device results have been presented, demonstrating low-voltage operation for comparable threshold voltage windows and operating speeds, and thin tunnel oxide retention behavior that suggest meeting long-term nonvolatility requirements.

In spite of these promising results, it is unclear whether nanocrystal memories will ever see commercialization. In order for that to happen, their claimed benefits will need to be more unambiguously substantiated, and a more appealing bundle of memory features will have to be demonstrated.

2.2 Memory basic concept

2.2.1 Reading operation

The data stored in a Flash cell can be determined measuring the threshold voltage of the memories. The best and fastest way to do that is by reading the current driven by the cell at a fixed gate bias show Fig. 2-3. When electrons stored in nanocrystal, the threshold voltage will shift (ΔV_T) that is proportional to the stored electron charge (Q). The threshold voltage shift of a Flash transistor can be written as [2.13-2.14]:

$$\Delta V_T = -\frac{Q}{C} \qquad (2.1)$$

Here Q is the carge stored in nanocrystal, and C is the capacitance between nanocrystal and control gate. It is possible to fix a reading voltage in such way that the current of the “1” cell is very high (in the range of tens of microamperes), while the current of the “0” cell is zero, in the microampere scale. In this way, it is possible to define the logical state “1” from a microscopic point of view as no electron charge (or positive charge) stored in the nanocrystal and from a macroscopic point of view as large reading current. Vice versa, the logical state “0” is defined, respectively, by electron charge stored in the nanocrystal and zero reading current.

2.2.2 Write/Erase operation mechanism

For SONOS structure, the write and erase processes for an n-channel

semiconductor memory device are illustrated schematically in Fig. 2-4. During the write process, a positive gate voltage is applied to inject channel inversion-layer electrons into the nitride layer. During the erase process, a reverse gate bias is applied to cause the electrons to tunnel back into the channel and the accumulation layer holes to tunnel into the nitride from the channel. There are many ways to achieve "programming" or "erasing". In general, hot carrier electron injection and Fowler-Nordheim tunneling (F-N tunneling) are two kinds of common operation mechanism employed in novel nonvolatile memories.

2.2.2.1 Channel Hot-Electron Injection (CHEI)

The physical mechanism of CHEI is relatively simple to understand. An electron traveling from the source to the drain gains energy from the lateral electric field and loses energy to the lattice vibrations (acoustic and optical phonons). At low fields, this is a dynamic equilibrium condition, which holds until the field strength reaches approximately 100kV/cm [2.15]. For fields exceeding this value, electrons are no longer in equilibrium with the lattice, and their energy relative to the conduction band edge begins to increase. Electrons are "heated" by the high lateral electric field, and a small fraction of them have enough energy to surmount the barrier between oxide and silicon conduction band edges. Fig. 2-5 shows schematic representation of CHEI MOSFET and the energy-distribution function with different fields. In the other hand, the effective mass of hole is heavier than one of electron. It is too hard to obtain enough energy to surmount oxide barrier. Therefore, hot-hole injection rarely is employed in nonvolatile memory operation.

2.2.2.2 F-N tunneling

Tunneling is another way writes electrons into nanocrystal from substrate. But during retention electrons could tunnel back to the channel too, constituting a large leakage current. The magnitude of the leakage current depends on both the thickness and the electron barrier height of the tunnel dielectric. The tunneling probability is expressed as:

$$T = \exp(-2\int_0^d \frac{\sqrt{\phi(x) * m_e}}{\hbar} dx) \qquad (2.2)$$

Here $\phi(x)$ is barrier height. It is 3.1eV in Si-SiO_2 for electrons see Table 2.1 [2.16-2.20]. *d* is tunnel dielectric thickness, $\hbar$ the Planck's constant and m_e is the electron mass inside the tunnel dielectric and it is $0.5m_0$ for both nitride and oxide. Many tunneling species can achieve charge transfer. Among them, in the memory operation mechanism, F-N tunneling is most often mentioned. The F-N tunneling mechanism occurs when applying a strong electric field (in the range of 8–10MV/cm) across a thin oxide. In these conditions, the energy band diagram of the oxide region is very steep. Therefore, there is a high probability of electrons passing through the energy barrier itself. The F-N tunneling [2.20] which can be expressed as follow:

$$J = E^2 \exp[-\frac{8\pi\sqrt{2m_e}(q\phi_B)^{3/2}}{3qhE}] \qquad (2.3)$$

Where E is the electric field which is defined as the applied voltage divide by

total thickness of the tunnel and control oxide. As shown in Fig. 2-6, when the voltage drop across the tunnel dielectric exceeds the electron tunnel barrier height ϕ_B, F-N tunneling current depends more on the tunnel barrier height than on the tunnel dielectric thickness. Increasing the tunnel dielectric thickness will not decrease the tunneling current if the same electric field is applied.

2.2.2.3 Direct Tunneling

For nanocrystal memories, the control-gate coupling ratio of nanocrystal memory devices is inherently small. As a result, FN tunneling cannot serve as an efficient write/erase mechanism when a relatively thick tunnel oxide is used, because the strong electric field cannot be confined in one oxide layer. The direct tunneling is employed in nanocrystal memories instead. In the other hand, the direct tunneling is more sensitive to the barrier width than barrier height, two to four orders of magnitude reduction in leakage current can still be achieved if large work function metals, such as Au or Pt.

2.2.3 Data retention

Any nonvolatile memory technology, Flash memories are specified to retain data for over ten years. This means the loss of charge stored in the memory must be as minimal as possible. In updated Flash technology, due to the small cell size, the capacitance is very small and at an operative programmed threshold shift—about 2 V—corresponds a number of electrons in the order of 10^3 to 10^4. A loss of 20% in this number (around 2–20 electrons lost per month) can lead to a wrong read of the cell and then to a data loss. Possible causes of charge loss are: 1) defects in the tunnel oxide; 2)

defects in the interpoly dielectric; 3) mobile ion contamination; and 4) detrapping of charge from insulating layers surrounding the FG [2.21].

2.2.4 Endurance

Flash products are specified for 10^5 write/erase cycles. Cycling is known to cause a fairly uniform wear-out of the cell performance, mainly due to tunnel oxide degradation, which eventually limits the endurance characteristics. The oxide defect will increase stress induce leakage current (SILC), that let electrons store in memory will be lost. Threshold voltage gradually recovery the initial value that before writing, the memory window will be close. Data retention after cycling is the issue that definitely limits the tunnel oxide thickness scaling. For very thin oxide, below 8–9 nm, the number of leaky cells becomes so large that even error-correction techniques cannot fix the problem.

Tunneling layer	Electron barrier (eV)	Hole barrier (eV)
SiO_2	3.15	4.7
SiN	2.4	1.8
Al_2O_3	2.9	4.3
HfO_2	1.6	3.3
Ta_2O_5	0.3	3.0

Table 2-1 Electron and hole barrier high for SiO_2 and Si_3N_4

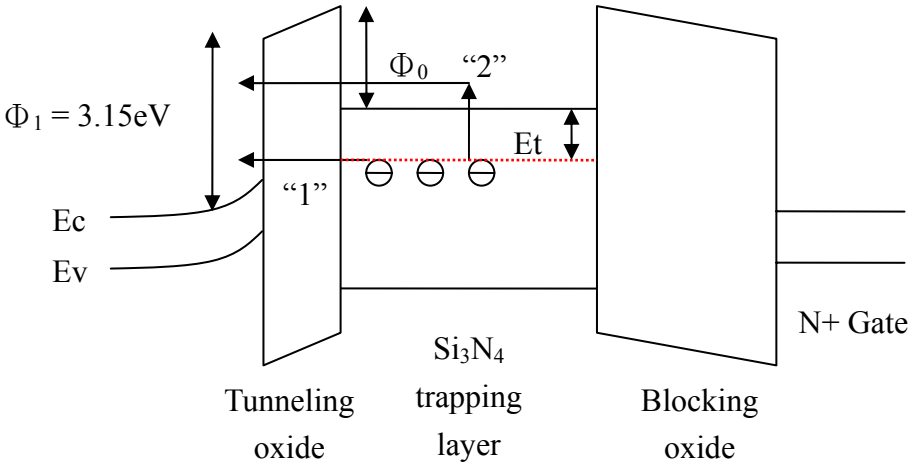


Fig. 2-1 SONOS band diagram during retention mode

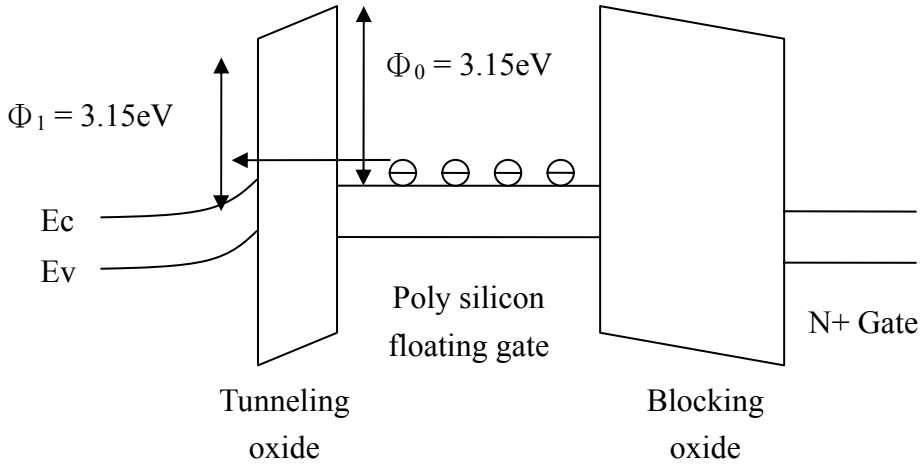
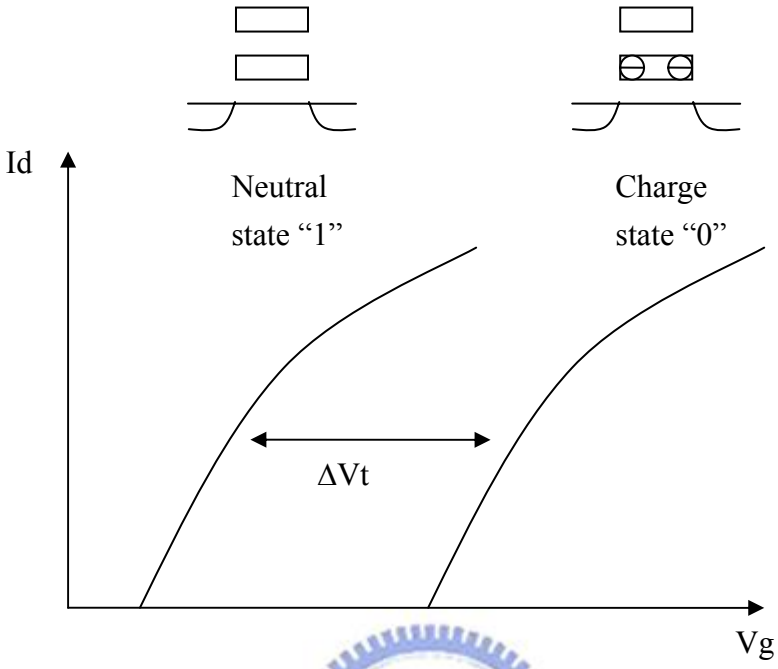
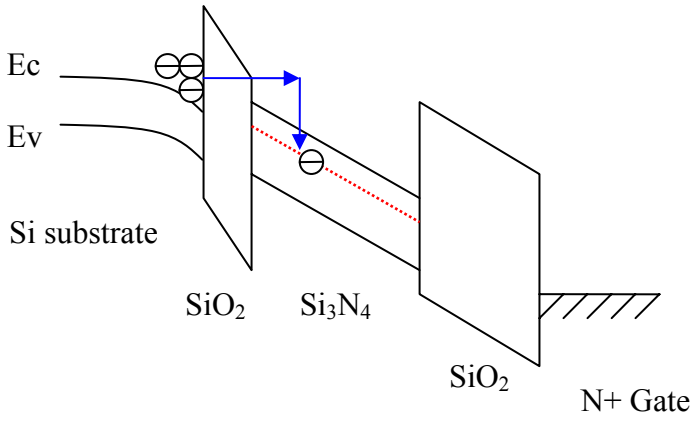


Fig. 2-2 FG band diagram during retention mode

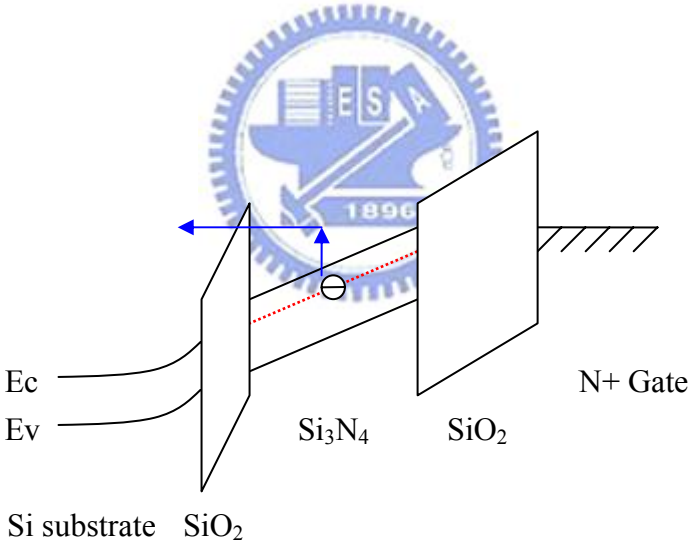


The state “1” threshold voltage is low, the state “0” threshold voltage is high.

Fig. 2-3 Memory reading operation



(a) write mode



(b) erase mode

Fig. 2-4 Memory band diagram in (a)write mode (b)Erase mode

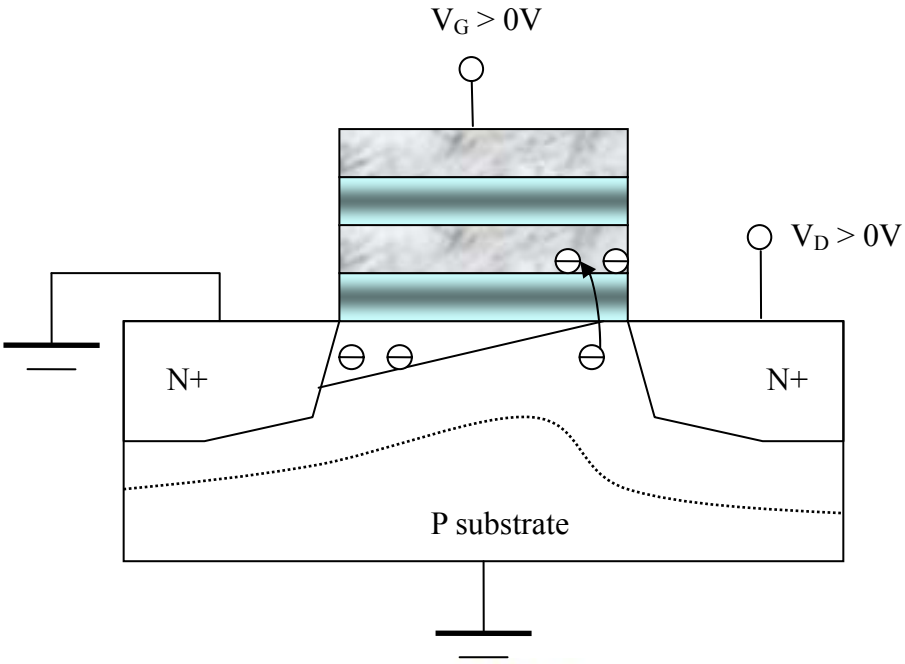
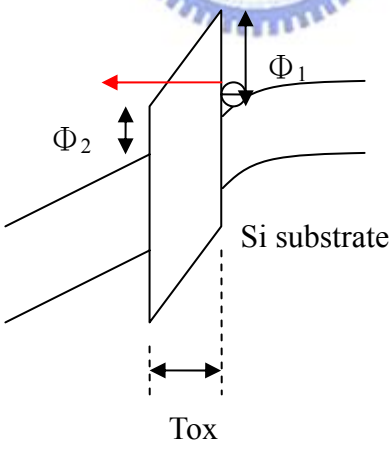


Fig. 2-5 The procedure of channel hot electrons injection



F-N tunneling occur when $|E_{ox}| > \frac{\phi_1}{T_{ox}}$

Fig. 2-6 The procedure of F-N tunneling

Chapter 3
Metal nanocrystal memory use Co nanodot

3.1 Motivation

Memory with discrete charge elements allows more advanced scaling of tunneling oxide and exhibit superior characteristics compared to conventional FG structure memories in terms of operation voltage, write/erase speed, retention and endurance [3.1-3.4]. Scaling tunneling oxide can increase write/erase speed, but simultaneous decrease data retention because of increase electrons tunneling back to substrate from nanocrystals. For the data retention characteristics, however, have not provided sufficient nonvolatility mainly due to the high leakage current of ultrathin SiO_2 tunneling barrier. Metal NC has been proposed in [3.5-3.8] aiming to improve the data retention. Since there are many kinds of metals that have the greater work function than silicon (Pt 5.29eV, Ni 4.84eV, Co 4.18eV), the electrons trapped in such metal NC are less likely to tunnel back to the substrate due to the higher electron barrier height, resulting in the prolonged data retention time. And due to the absence of drain to FG coupling, nanocrystal memories suffer less from drain induced barrier lowering (DIBL) and therefore have intrinsically better punchthrough characteristics. In addition, the large variety of the metal work functions from various metals allows more design flexibility in such device application. Besides for data retention goal, used discrete

storage still one advantage. The advantage is it can store two different data in only one device (i.e. one bit stored near drain side, other one store near source side, see Fig. 3-1) [3.9-3.10]. That can effective use each device and increase the memory size but don't increase die size. The cost will be lower than one bit memory device.

3.2 Experimental procedure

For manufacture nonvolatile memory device, we used P-type (100) silicon wafer. After RCA clean, growth tunneling oxide by furnace system. The oxide measured by ellipsometer is 35~38 Å. Then used E-Gun evaporator deposited Co wetting layer about 40 Å. This Co wetting lay thickness used 40 Å refer to Liu's paper [3.7-3.8] and Lee's paper [3.11]. Some characters about cobalt list in Table 3-1. Then used rapid thermal process (RTP) anneal system of 400℃ ~ 900℃ in N_2 and O_2 ambient was then performed to transform cobalt wetting-layer into cobalt nanocrystals. The split table show in the Table 3-2. The blocking oxide used PE-CVD method deposited about 250 Å SiO_2 for isolation each nanodots. Final deposited Al layer in front and back side as electrode. Here, we use shadow mask in front side to define the cell pattern. The process flowchart show in Fig. 3-2.

3.3 Result and discussion

3.3.1 Self-Assembled Nanocrystal Formation

The basic procedures for metal nanocrystal formation are starting with Si wafer covered by a thin layer of thermal oxide, a metal wetting layer of 1–5 nm is deposited by e-beam evaporation. Then, the film is annealed at elevated temperatures close to its eutectic temperature with the substrate in an inert ambient to transfer the wetting layer into nanocrystals. This process is achieved through the relaxation of film stress and limited by the surface mobility. Some long-range forces such as the dispersion force and the electrical double layers will also affect the nanocrystal size and location distributions [3.12-3.13].

Before RTA, the as-deposited film comes naturally with some thickness perturbation and even nanocrystals start to form (without a clear separation in between, though). When the film is RTA treated to give the atoms enough surface mobility, the film will self-assemble into a lower-total-energy state. To reduce the elastic energy carried by the stress built into the film during the deposition process, the film tends to break into islands along the initial perturbation. However, minimization of the surface energy and the dispersion force between the top and bottom interfaces can help stabilize the film. So the final geometry will depend on the balance between these driving forces. Once the nanocrystals have formed, the work function difference between the metal and the extrinsic substrate generates localized depletion or accumulation region in the substrate. The repulsion force between those regions helps stabilize the nanocrystals and keep a uniform distance between them.

Fig. 3-3 ~ Fig. 3-7 shows the AFM pictures of nanocrystal formation from Co films on top of 3.5 nm thermal oxide and the resulted nanocrystal size distribution. All samples went through the annealing cycle at different temperature for 30s and 60s. After RTA, well-defined nanocrystals with round shape and certain size distribution

can be achieved. The density of NC is decreased and the size of NC is increased as the RTA annealing temperature is increased. These results show that the greater thermal energy induced agglomeration of the metal wetting layer into the larger NCs. For sample6, we observe very dense nanocrystal formation. It be estimated about $3\times10^{11}cm^{-2}$. For the sample7、 sample8、 sample9 and sample10, the dot is baldly bigger than the sample6. But sample6 density is the highest. The higher treatment temperature and time, dots growth larger and the density decreased is agreeable we anticipation. The density for each sample are $1.6\times10^{11}cm^{-2}$ (sample7)、$1.37\times10^{11}cm^{-2}$ (sample8)、$0.971\times10^{11}cm^{-2}$ (sample9)、$0.556\times10^{11}cm^{-2}$ (sample10).

3.3.2 Memory characteristics

In order to confirm the memory operation, high-frequency capacitance–voltage (HF C–V) characteristic of a capacitor with a SiO_2 –cobalt NC–SiO_2 –Al stack was measured, as shown in Fig. 3-9 ~ Fig. 3-12. The observed large hysteresis in HF C–V indicates the charging and discharging process of the NC memory cell. The C-V curves are fail when samples treatment at low temperature (700℃). We guess maybe the metal film treat at low temperature not get enough energy translate film to nanodots. But sample7 although treatment at 700℃, but it C-V curve not express any memory character too. From sample AFM picture Fig. 3-3 and Fig. 3-4, although the dots have formation, but maybe not clear separation in each dot, so that these sample(sample6 and sample7) C-V curve fail. Fig. 3-10 show the capacitance-voltage (C-V) hysteresis after bidirectional bias sweeps between 4V and -4V. According the C-V curve Fig. 3-10, it is found that a low operating voltage (4V) causes a significant flat-band voltage shift up to 2 V, which is enough to be defined as logic “1” or “0” for the circuit

design. In these samples, we found the sample8 have a larger flat-band voltage shift than other sample. It have more charge injection into cobalt NCs. And the sample9, it have a flat-band voltage shift up to 2 V too, but operating voltage is higher than sample8. The sample10 observe from its C-V curve, even then gate bias sweeps between 8V and -8V but not express memory window. And the sample10 AFM picture Fig.3-7, we look the lower dot density than other sample (sample10 only $5.56\times10^{10}cm^{-2}$). It maybe a reason explain this phenomenon. In RTO sample we observe each samples have stable C-V curve Fig. 3-8 but not show any memory window. Maybe the Co's metal-oxide hasn't trap ability.

3.3.3 Programming/Erase characteristics

Programming transient characteristics of cobalt NC memory devices are demonstrate in Fig. 3-13. Only programming in a low voltage 5V can get an obvious flat-band voltage shift. This is due to the fact that cobalt NC provides considerably greater density of available energy states, resulting in the larger amount of electrons stored inside the NC after programming. We compare Fig. 3-13 and Fig. 3-17, we find in the same programming voltage, sample8 flat-band voltage shift is larger than sample9. This is matching our measure in C-V curve. When operate in Erasing mode the gate apply negative bias, operation time over 0.01s the over-erase situation take place see Fig. 3-14. It maybe the hole be writing into NCs from channel or the free electrons in the cobalt be erasing.

3.3.4 Data retention characteristics

Fig. 3-15 and Fig. 3-19 illustrated the retention characteristics of Co NCs at the room temperature. The retention time is very poor for a nonvolatile memory. The charge loss 76% and it can't reach 10 year data retention. Sample9 only remain 0.264V flat-band voltage shift and sample10 remain 0.173V flat-band voltage shift. Some charge loss reasons have be mention in chapter 2. In these reasons, we guess the PE-oxide maybe a main reason for charge loses. Because dots in the surface, their inter-distance are very close only tens nanometer. If PE-oxide quality not very good, it will cause large charge loss in NCs. The blocking oxide leakage current illustrated in Fig. 3-21. Except for this reason, according to Liu's paper [3.7] some dots have inter-connect will induce large leakage current show in Fig. 3-21. The tunneling oxide defect also can make large charge lose, but other experiment can prove the furnace system is clear. One reason can make the tunneling oxide defect generate. When metal film deposition on the tunneling oxide, it rely on heating process to translate metal film into dots. This process is achieved through the relaxation of metal film stress. During stress relaxation, maybe underlay oxide stand the stress. Make the oxide crack or defect generate so that the leakage current get more. Fig. 3-16 and Fig. 3-20 show these samples leakage current.

*3.4 **Summay***

In this chapter, we have investigated the memory effects and performance of cobalt metal nanocrystal memory devices. And the AFM picture proof the dots formation at the 600℃ ~ 900℃. Although it density hasn't as high as 10^{12} cm^{-2}, it still have memory window. And other memory character is measured show in this chapter even than some character is not good that are not agreeable our anticipation.

Cobalt general character	
Name, Symbol, Number	cobalt, Co, 27
Chemical series	transition metals
Group, Period, Block	9, 4, d
Density	8.90 g·cm−3
Melting point	1768 K (1495 °C, 2723 °F)
Boiling point	3200 K (2927 °C, 5301 °F)
Heat of fusion	16.06 kJ·mol−1
Heat of vaporization	377 kJ·mol−1
Heat capacity	(25 °C) 24.81 J·mol−1·K−1
Work function	4.18eV

Table 3-1 Some character about cobalt

Time (s) / Temperature	30s	60s
400℃	Sample1	Sample2
500℃	Sample3	Sample4
600℃	Sample5	Sample6
700℃	Sample7	Sample8
800℃	Sample9	
900℃	Sample10	

Table 3-2 Experiment split table

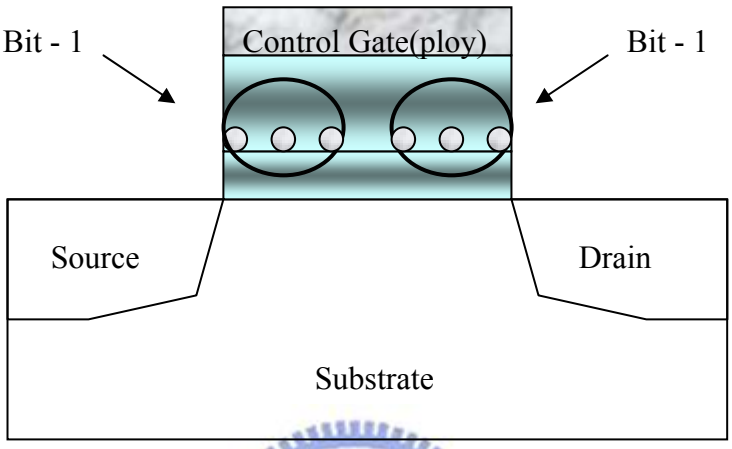


Fig. 3-1 2-bit memory device

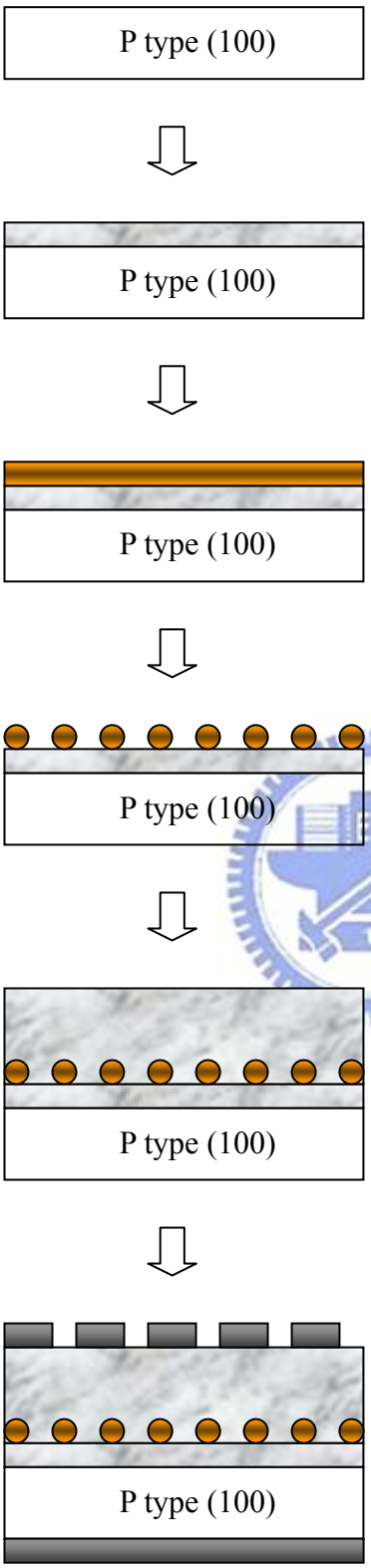


Fig. 3-2 process flowchart

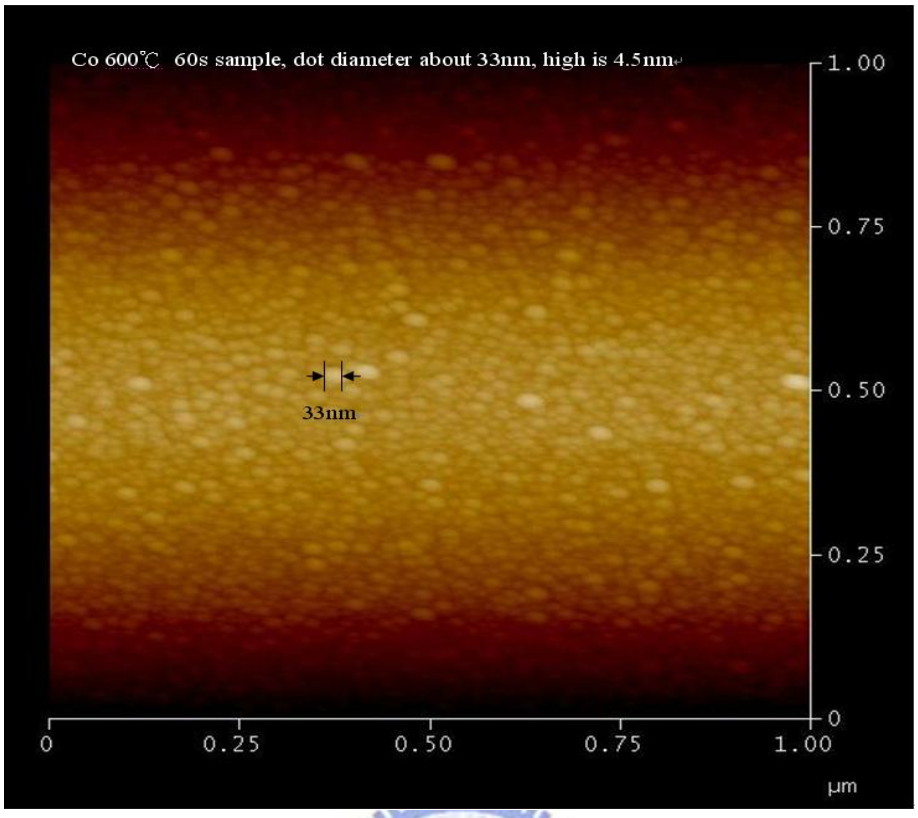


Fig. 3-3 Co RTA 600℃ 60s sample AFM pictcure

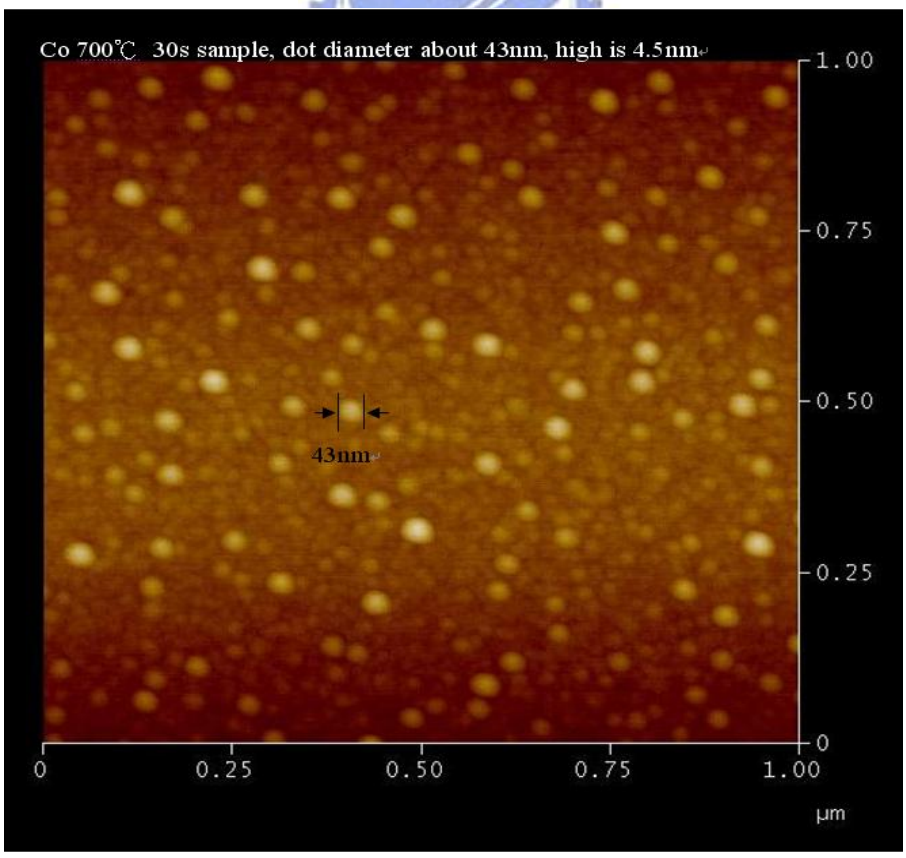


Fig. 3-4 Co RTA 700℃ 30s sample AFM pictcure

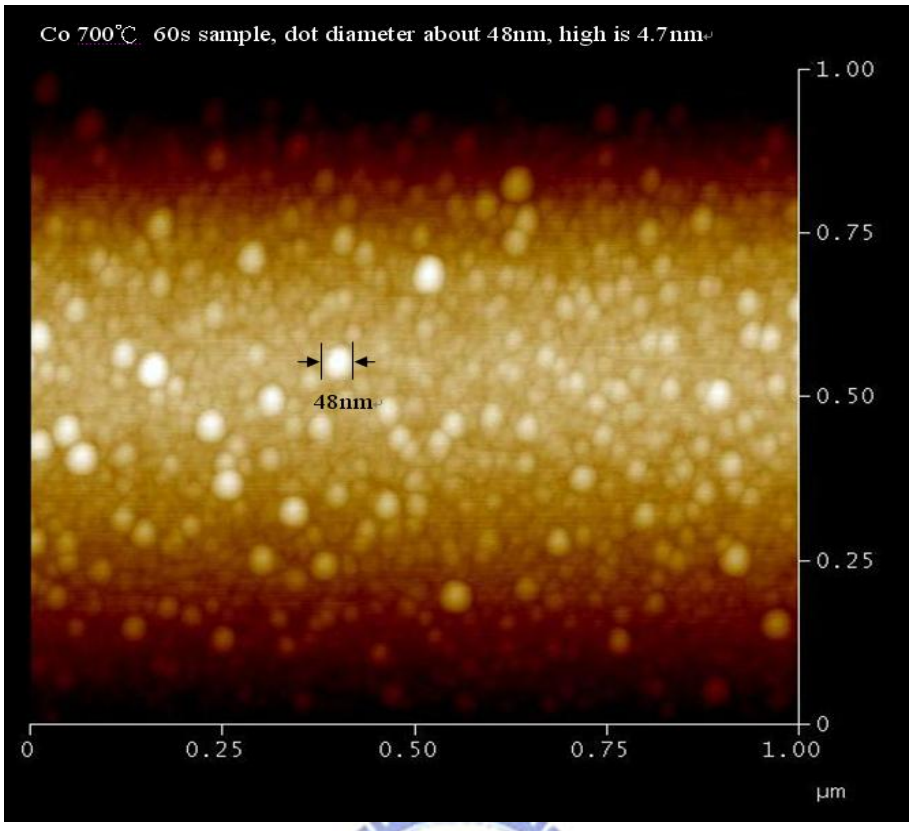


Fig. 3-5 Co RTA 700℃ 60s sample AFM pictcure

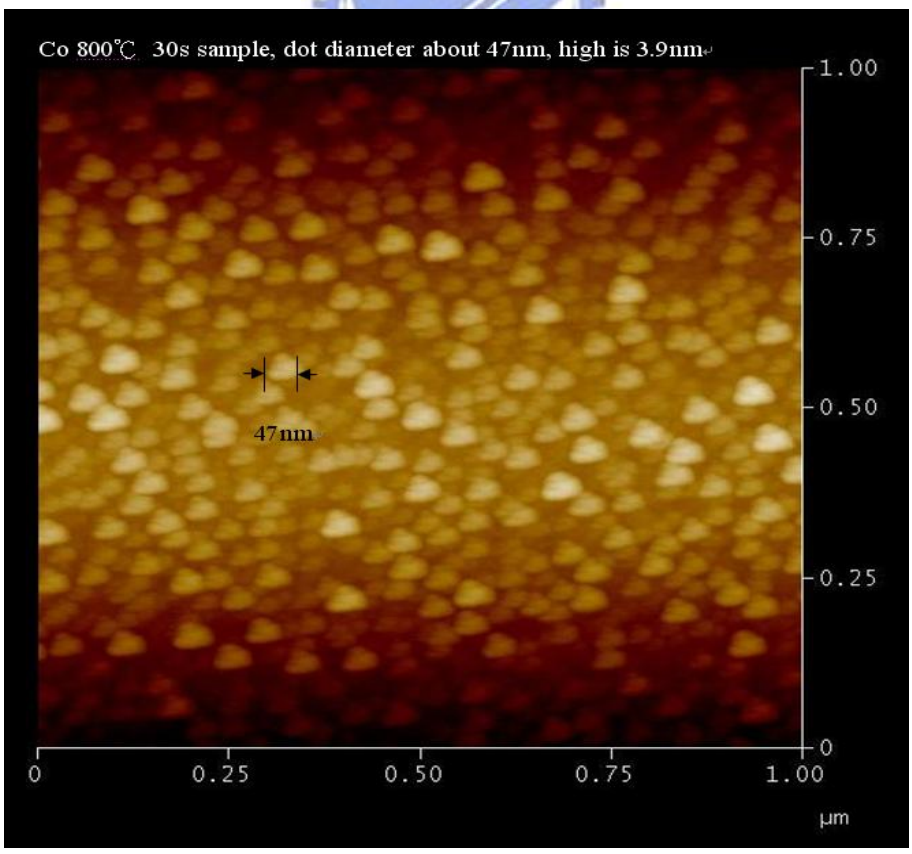


Fig. 3-6 Co RTA 800℃ 30s sample AFM pictcure

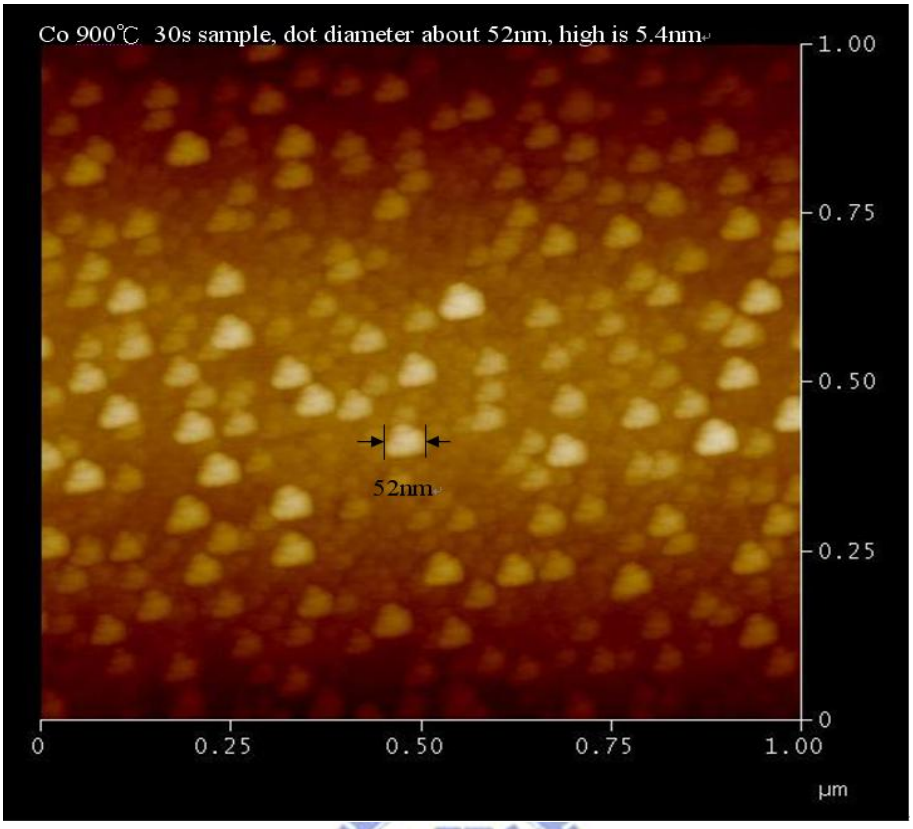


Fig. 3-7 Co RTA 900℃ 30s sample AFM pictcure

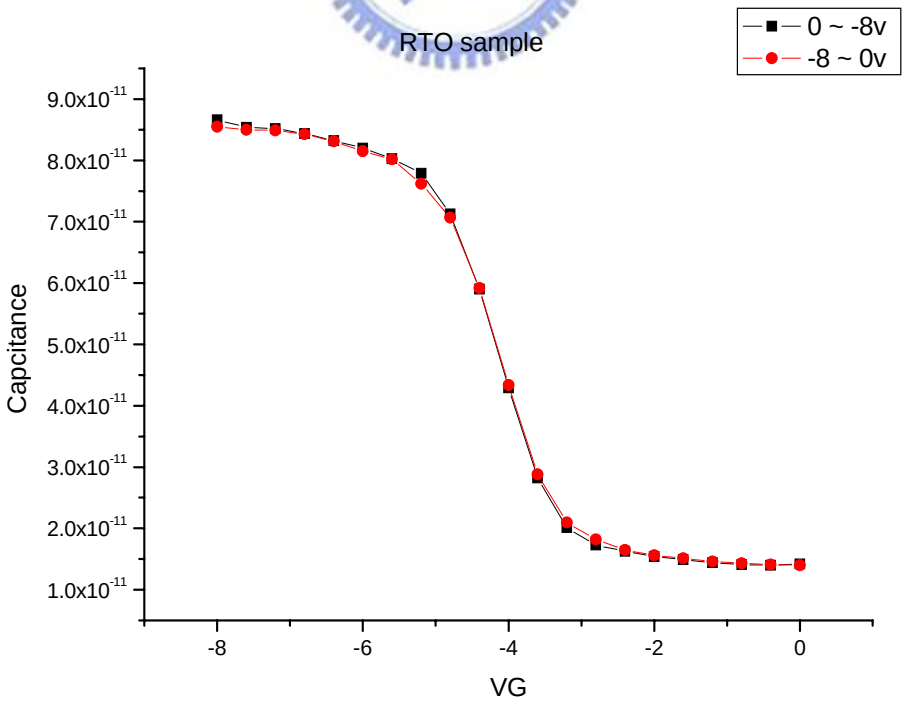


Fig. 3-8 RTO samples C-V curve

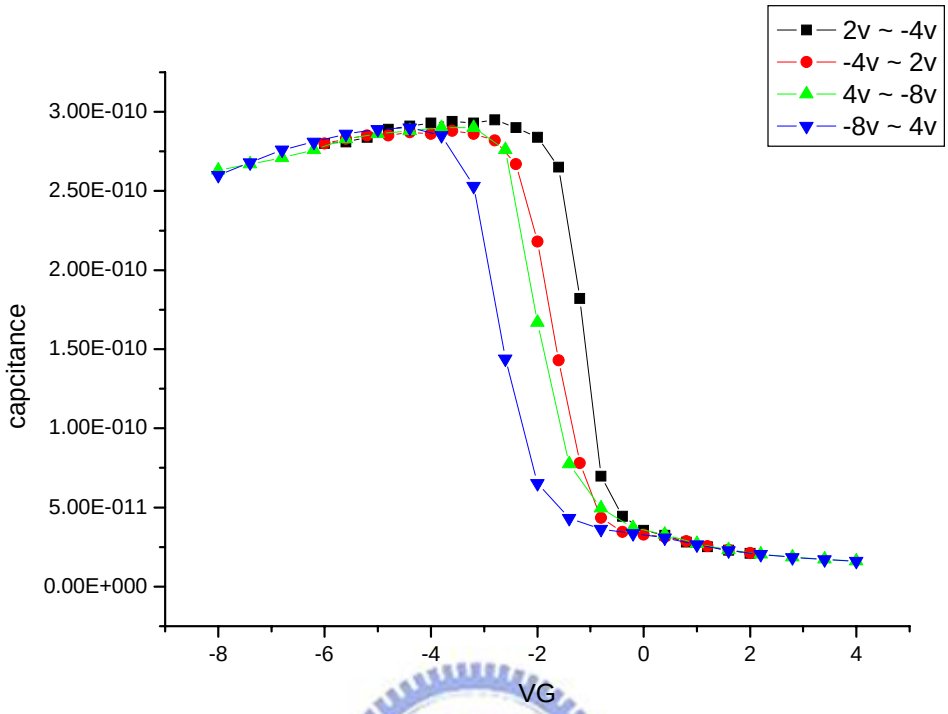


Fig. 3-9 RTA 700℃ 30s sample C-V curve

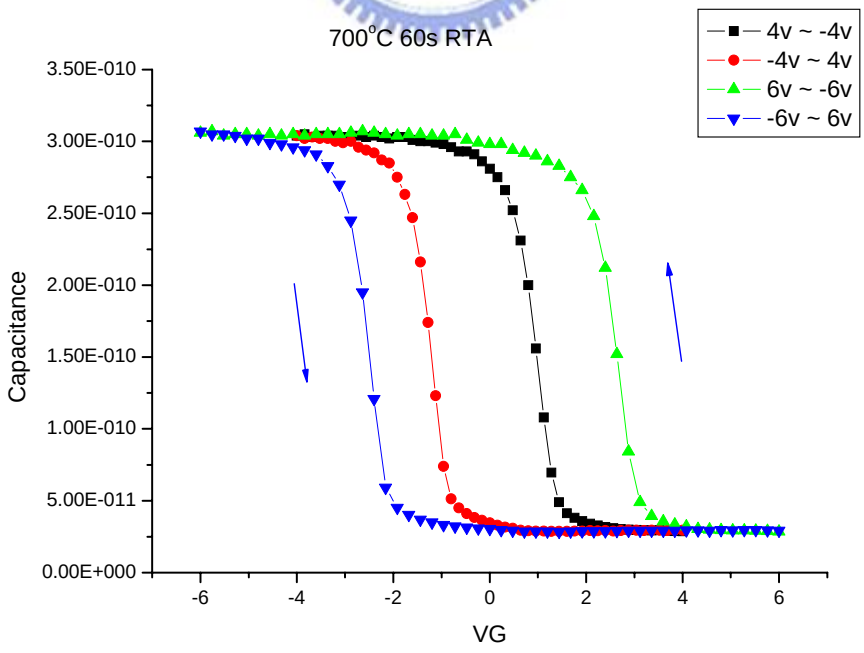


Fig. 3-10 RTA 700℃ 60s sample C-V curve

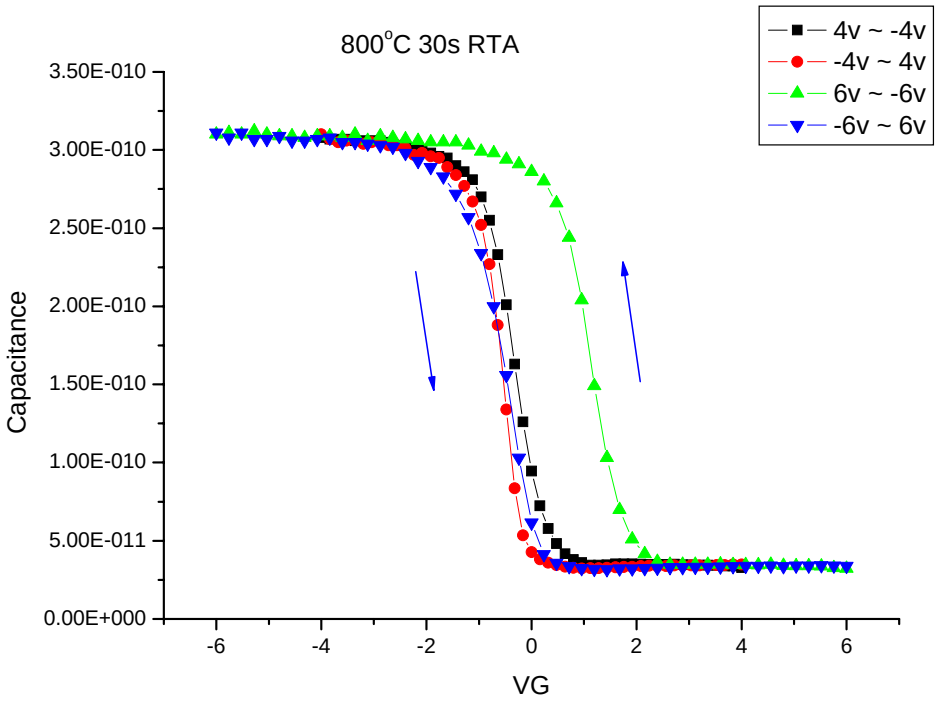


Fig. 3-11 RTA 800℃ 30s sample C-V curve

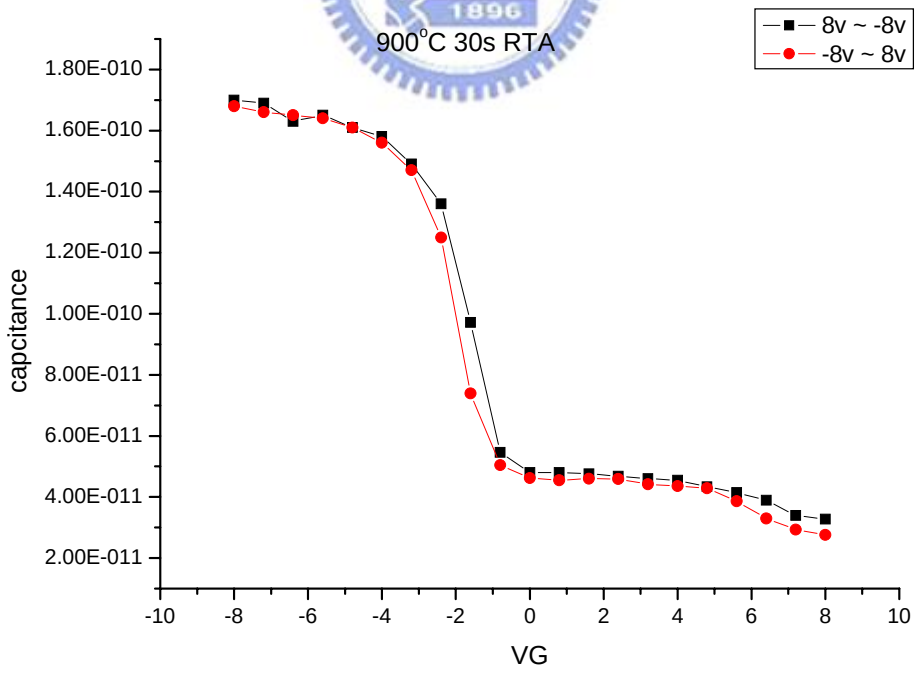


Fig. 3-12 RTA 900℃ 30s sample C-V curve

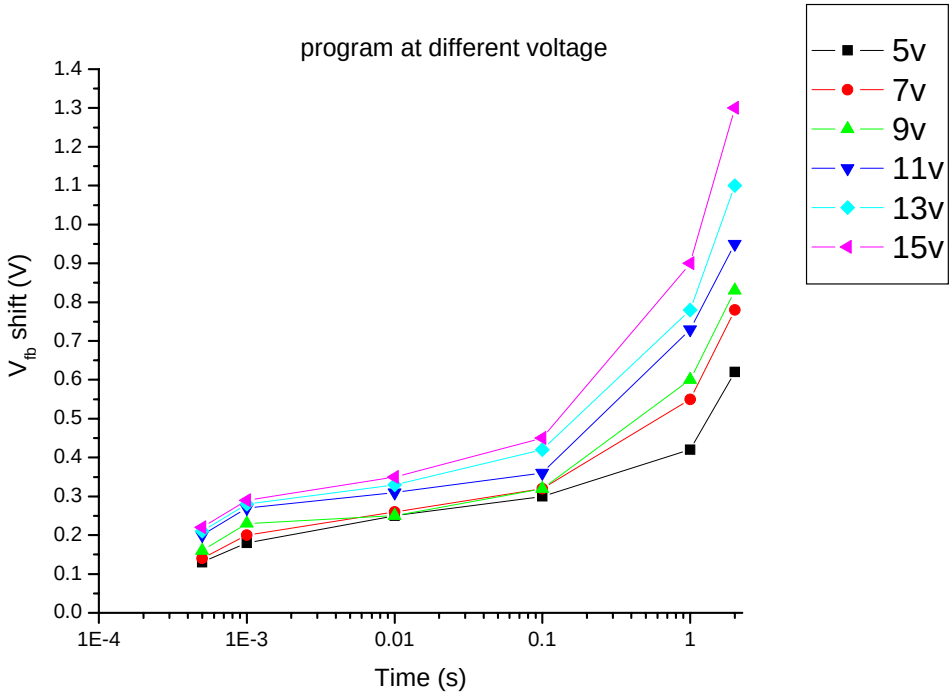


Fig. 3-13　RTA 700℃ 60s sample program speed

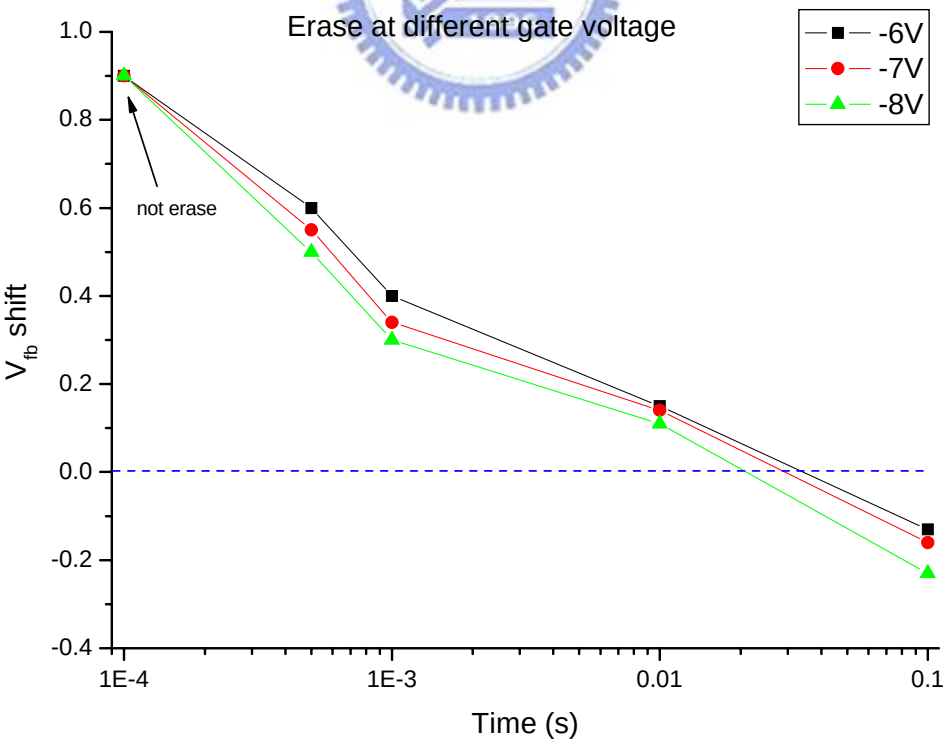


Fig. 3-14　RTA 700℃ 60s sample erase speed

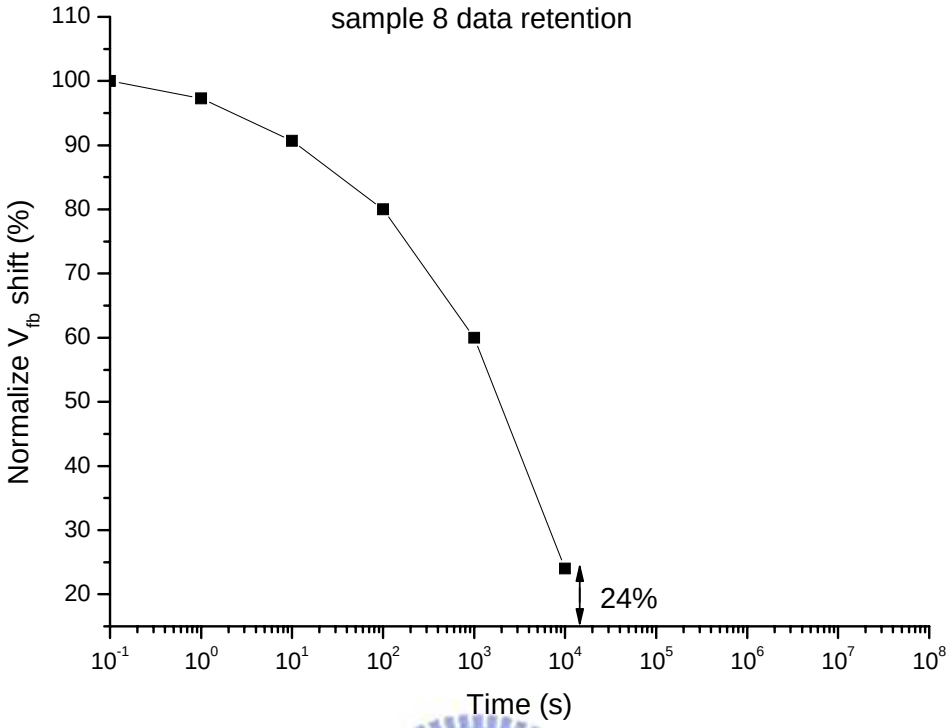


Fig. 3-15 RTA 700℃ 60s sample data retention

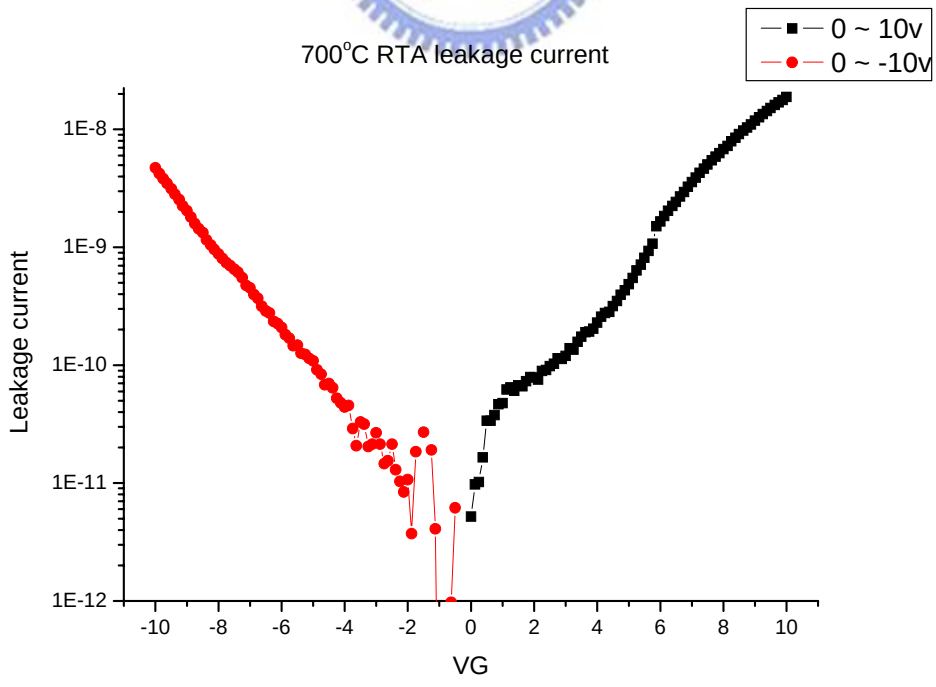


Fig. 3-16 RTA 700℃ 60s sample leakage current

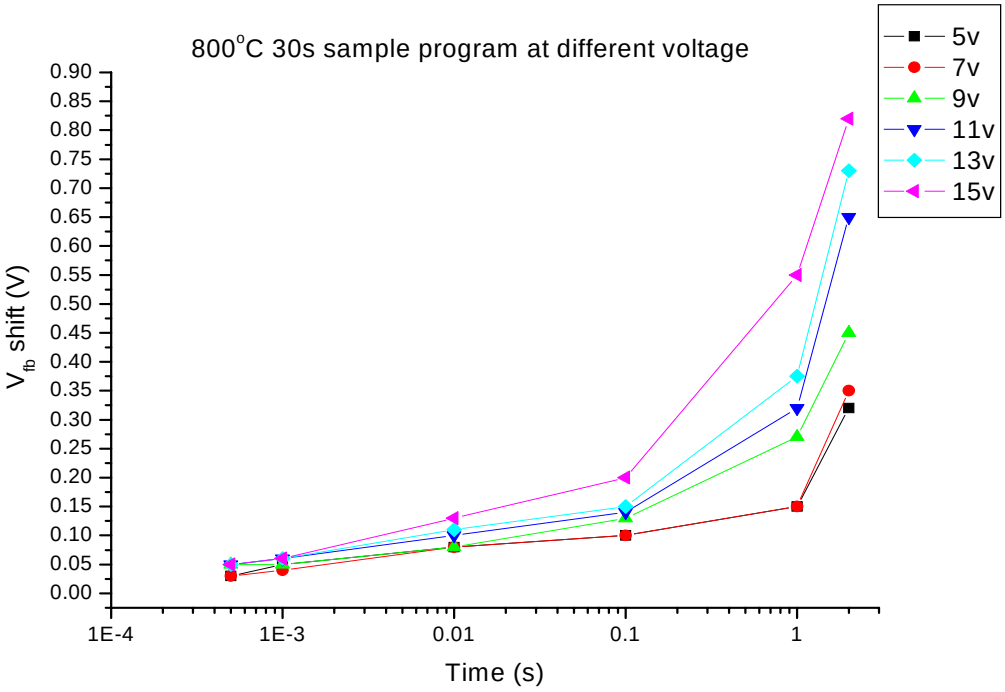


Fig. 3-17 RTA 800℃ 30s sample program speed

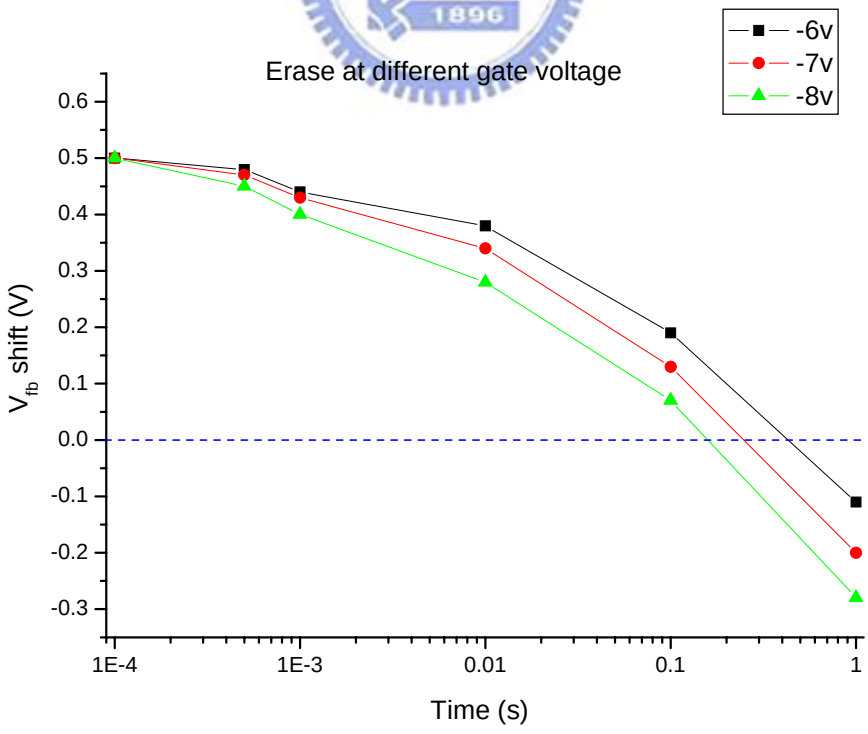


Fig. 3-18 RTA 800℃ 30s sample erase speed

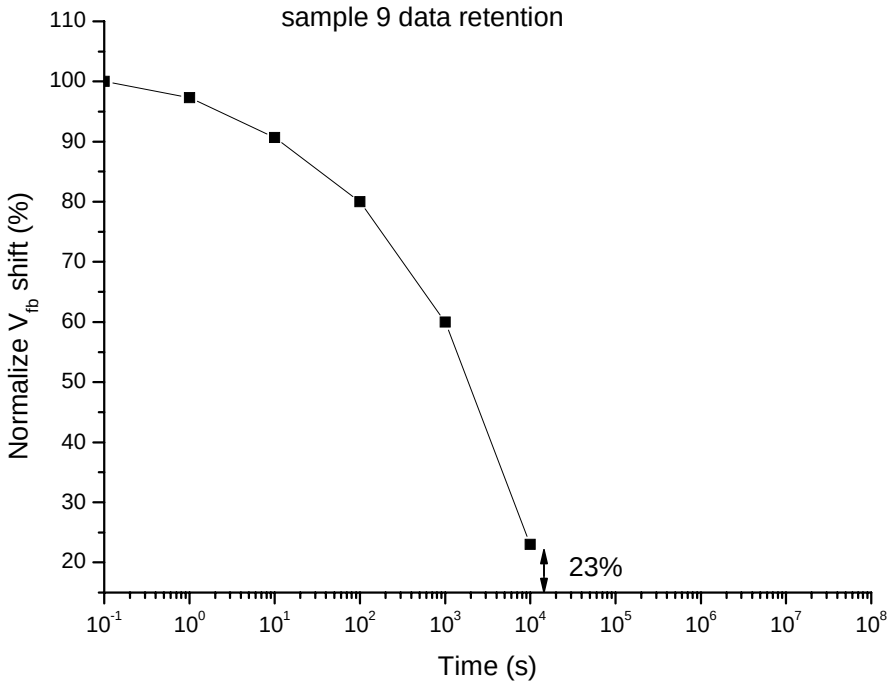


Fig. 3-19 RTA 800℃ 30s sample data retention

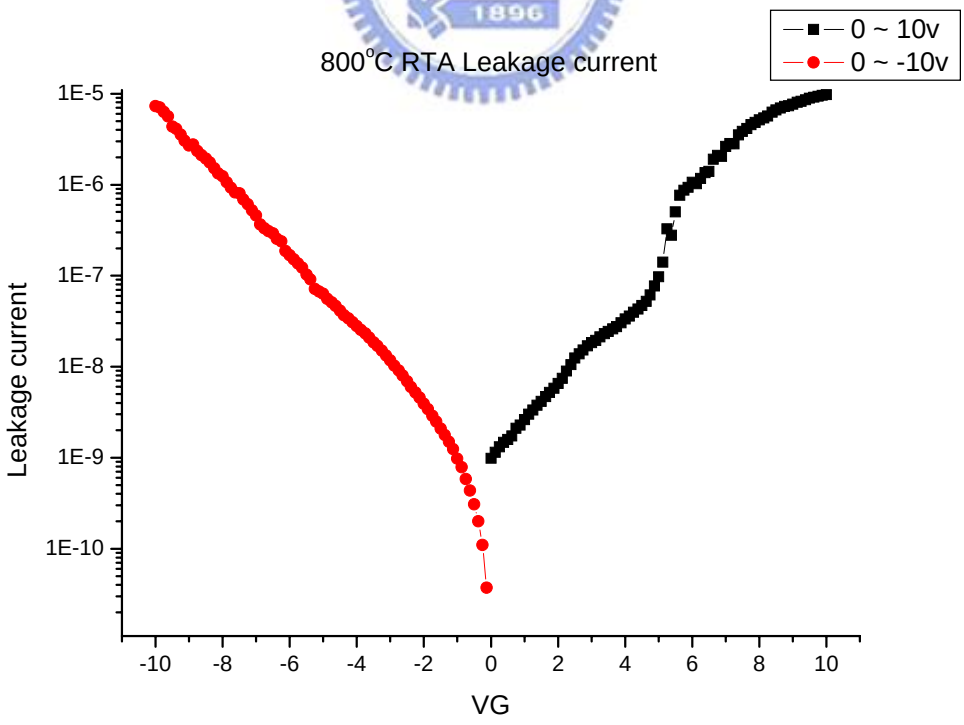


Fig. 3-20 RTA 800℃ 30s sample leakage current

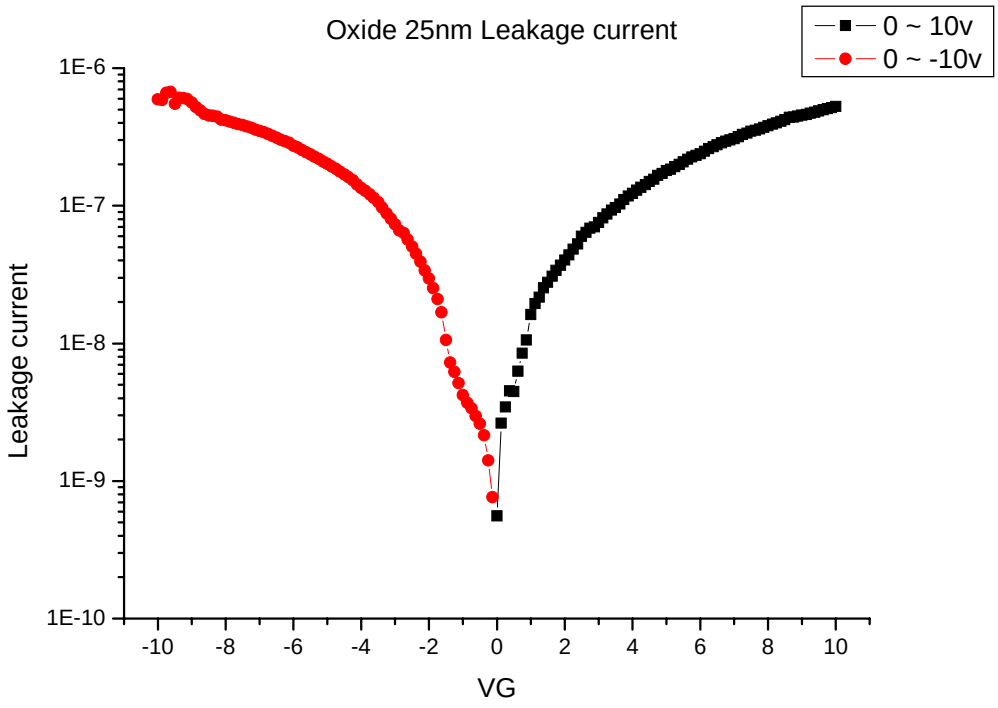


Fig. 3-21 Silicon oxide 25nm leakage current

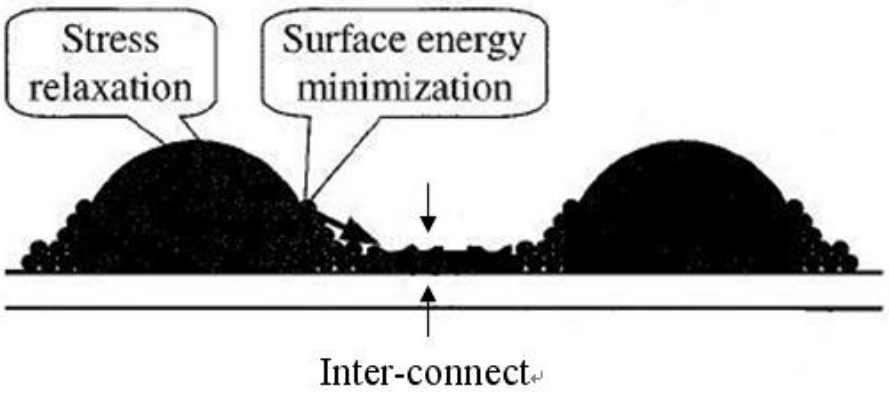


Fig. 3-22 The dot is not fully independent, still have inter-connect

Chapter 4
Conclusions and recommendations for future works

4.1 Conclusion

In this thesis "The memory characterization and investigation of metal nanocrystal", we have investigated the memory effects and performance of cobalt metal nanocrystal memory devices. From our experiment, this memory can use low operation voltage to program and erase. But it has a big problem in data retention that is most important for nonvolatile memory. In our sample demonstrate poor data retention. It has some existing problem need analyze and solve that discuss in the before chapter. Maybe we can find another recipe (process) to improve this problem or maybe this metal is not suit for metal nanocrystal nonvolatile memory.

4.2 Recommendation for future works

1) Use Co and SiO_2 co-sputter that can let the Co dots surround by SiO_2. It can get batter isolation in each dot.

2) Find other metal material has large work function.

3) Used TEM analysis to find exactly dot density and some problems which make poor retention.

4) Use high-K material and metal dots simultaneously to improve data retention.

5) Use cobalt to manufacture nonvolatile memory device. Some high temperature process step in MOSFET manufacture after metal film anneal must be avoid. High temperature process can make metal dots unstable or affect other character. One high temperature process will be encounter that is after S/D implant anneal. We can use implant S/D and anneal before gate oxide growth. After S/D anneal, star gate oxide growth and following process. And use metal gate TiN can avoid in furnace system that to deposition poly-gate.

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