國 立 交 通 大 學

電子工程學系 電子研究所碩士班

碩 士 論 文

射頻金氧半電晶體小訊號等效電路模型參數萃取方法建立以應用於各種偏壓與幾何結構

RF MOSFET Small Signal Equivalent Circuit Model Parameter Extraction for Various Biases and Geometries

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摘要

在本論文中，發展了小訊號等效電路模型及其所對應的參數萃取方法，以應用於射頻互補式金氧半場效電晶體電路模擬上。本研究涵蓋雙埠三端點與四埠四端點的射頻金氧半電晶體。前者即三端點共源組態射頻金氧半電晶體是在電路設計上最為廣泛使用的元件，為了符合雙埠射頻量測系統，其測試元件佈局必須設計成源極與基極連接在一起並接地的雙埠組態結構。事實上，在射頻電路設計中，源極與基極並非總是連接在一起，此傳統的雙埠測試元件將無法得到完整的四端點金氧半電晶體的特點，也無法代表正確之高頻特性。為了解決此關鍵的問題，本研究設計四埠四端點的射頻金氧半電晶體，並利用 0.13um 互補式金氧半場效電晶體製程研製出來探討元件高頻特性及模型的發展。

本論文中，首先介紹了雙埠與多埠散射參數(S 參數)的基本原理，然後，對於雙埠三端點的元件，分別詳盡探討在不同的偏壓條件與幾何結構上的小訊號電路與其所對應的參數萃取方法。基於雙埠三端元件已做的工作上，適時地改良其小訊號電路以相對應於四埠四端點的元件架構，並建立四埠四端點的去寄生效應方法與參數的萃取流程等基本的研究工作。

最後，在不同偏壓下所提出的小訊號等效電路分別透過模擬做更廣泛的驗證，驗證

其模型的準確性以可靠地應用在超過 40GHz 的寬頻範圍，以及不同的偏壓條件如線性區與飽和區。更重要地，所建立的等效電路模型其本身的參數值充分表現出良好的可伸縮性，可預測於固定指叉寬度下變化閘極長度與閘極指叉數目之效應。在各種頻率、偏壓下的準確性和元件幾何參數之可伸縮性，可有效提昇高頻電路的模擬的準確性，以及輔助射頻互補式金氧半場效電晶體積體電路設計。

RF MOSFET Small Signal Equivalent Circuit Model Parameter Extraction for Various Biases and Geometries

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ABSTRACT

Small signal equivalent circuit models and the corresponding parameter extraction methods have been developed in this thesis for RF CMOS circuit simulation. Both two-port 3-terminal (3T) and four-port 4-terminal (4T) RF MOSFETs are covered in this work. The former one – 3T MOSFETs with a common source topology is a conventional one widely used in RF circuits, and the test-key layout is arranged in a two-port configuration with a common ground for source and body tied together to fit the two-port RF measurement system. In fact, source and body terminals are not always connected together in the practice of RF circuit design, the traditional two-port test-key cannot capture a whole spectrum of 4T MOSFET's features and cannot adequately represent 4T MOSFET's characteristics over high frequencies. To solve this critical problem, the latter one – four-port 4T RF MOSFETs are designed and fabricated in 0.13um RF CMOS process for high frequency characterization and model development in this work.

In this thesis, the basic principles of two-port and multi-port scattering parameters (S-parameters) will be reviewed in the first place. Then, the small signal equivalent circuits and parameter extraction methods developed for two-port 3T device under various biases and geometries will be discussed in detail. Based on what have been done for two-port 3T MOSFET, a modified equivalent circuit relevant to four-port 4T test structures, and the corresponding fundamental works, such as de-embedding method and parameter extraction

flow have been carried out.

Finally, an extensive verification has been performed on the proposed small signal equivalent circuit models through simulation under various biases. The model accuracy is certified over a broad frequency up to 40GHz and various bias conditions – linear and saturation. More importantly, the model parameters of the developed equivalent circuit models manifest themselves a promisingly good scalability over various geometries in MOSFETs, such as gate lengths and gate finger numbers under a specified finger width. The accuracy over frequencies and biases and scalability over device geometries is useful to improve accuracy of high frequency circuit simulation and facilitate RF CMOS integrated circuit development.

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Chapter 1

Introduction

1.1 Research motivation

In the area of RF MOSFET modeling, many interesting and challenging effects have to be considered and implemented to achieve the desired accuracy and scalability. Among them, it still is a challenge in the gate resistance and substrate networks modeling and parameters extraction. It has been known that gate resistance is a primary source of the input impedance in an intrinsic MOSFET and the induced excess noise will increase the thermal noise proportional to frequency. In a conventional approach, R_g is assumed as a constant to simplify the model formulation. However, this assumption and the simplified model are no longer valid for simulating devices with various gate lengths in which poly sheet resistance and channel resistance play a trade-off to each other in determining R_g. In this thesis, an improved model is developed considering the feature of distributed TML and non-quasi-static effect in the poly gate and conduction channel. This enhancement can help improve simulation accuracy over a wide range of gate lengths.

As for substrate resistance existing in 4T devices like MOSFETs, it significantly affects the small-signal output characteristics over high frequencies and should be taken into the model for an accurate simulation, particularly under body biasing conditions. A simple substrate RC network adopting a single resistance is frequently used and the accuracy was demonstrated to around 10 GHz. However, the simplified model may lead to tremendous deviation over higher frequencies above 10 GHz and cannot fit RF circuit simulation and design using 4T MOSFET with body biases. As a matter fact, the development of an accurate substrate network model relies on the

four-port S-parameters, which cannot be achieved from conventionally used 3T devices in a two-port test structure. In other words, a reliable substrate network model and four-port 4T test structures depends on each other. In this study, four-port test structures were designed and implemented for four-port S-parameters measurement and model parameter extraction. Note that the supply voltage on each terminals can be independently controlled and a dynamic body biasing scheme can be realized in this scheme.

Based on the mentioned principles and objectives, small signal equivalent circuit models were developed and implemented in this work for three operation conditions, such as off-state, linear, and saturation regions. De-embedding and model parameter extraction methods were implemented and performed on two-port 3T and four-port 4T test structures. The model accuracy was verified through circuit simulation using ADS and comparison with S- and Y-parameters measured from multi-finger RF MOSFETs with various geometries (gate lengths, finger numbers, and finger widths). In the following, the major subject in each chapter will be described.

1.2 Overview

The main objective of this thesis is the development of small signal equivalent circuit models for RF MOSFETs and circuit simulation. This thesis is organized into six chapters as follows:

Chapter 2 provides the introduction to the non-quasi-statistic (NQS) effect for gate resistance in long channel devices and the NQS modeling in SPICE simulation. Two-port and four-port S-parameters, as well as port reduction methods for four-port to two-port will be covered in this chapter.–

In chapter 3 and Chapter 4, the equivalent circuit models will be developed

under different biasing conditions for two-port 3T and four-port 4T MOSFETs, respectively. The model parameters for both intrinsic and extrinsic components will be extracted under appropriate bias conditions. Then, an analysis will be performed on the extracted model parameters in the features under various biases and scalability over different geometries.

In chapter 5, the proposed equivalent circuit models will be verified through ADS simulation. It can be proven that the substrate network extracted from four-port 4T test structures can provide sufficient data base in terms of four-port S- and Y-parameters and facilitate the model accuracy for simulation under body biases.

Chapters 6 will make conclusions and address the future work for further study.

Chapter 2

Fundamental theory and RF MOSFET design

2.1 Non-quasi-statistic (NQS) effect

As the improvement of RF CMOS technology, the cut-off frequency is roughly inversely proportional to the gate length. In the longer channel devices, the channel charge relaxation time is finite, and then, the carries in the channel can not response to the signal immediately. NQS effect should be included for the equivalent circuit model to describe the device behavior accurately over a broad frequency.

2.1.1 Quasi-static (QS) model

In Quasi-static model, the channel charge is assumed to be a unique function of the instantaneous biases, the charges per unit area at any time are assumed to identical at any position. QS model assumption is described in Fig. 2.1, the gate capacitances are lumped into the intrinsic source and drain nodes, the signal form gate will couple to source and drain side directly, this model ignores that the charge built up in the center portion of the channel does not follow a change of gate biases as readily as at the source or drain edge of channel.

2.1.2 NQS model

It has been known that the carriers in the channel can not respond to the signal immediately nearly cut-off frequency, for long channel devices, the channel transit time is roughly inversely proportional to (Vgs-Vth) and proportional to square of channel length, NQS effect become pronounced in the application, considering the

input signal with rapid rise and fall times comparable to the channel transit time in Fig. 2.2, the channel charge is not a unique function of the instantaneous terminal voltage but a function of the history of the voltage, owing to the existence of the NQS effect, QS model will be not suit to the characteristic of devices with NQS effect at the operating frequency accurately.

The method to model NQS effect for RF application, one solution is to represent the channel as n transistors in series, this model wastes on the expense of simulation time but the behavior is accurately. One solution is the RC network approach, NQS model in BSIM3v3.2.2 was based on the circuit of Elmore model, the Elmore equivalent circuit can be viewed as a first step toward an NQS model, the channel charge buildup is modeled with reasonable accuracy because it retains the lowest frequency pole of the original RC network. Fig. 2.3 illustrates the QS and NQS equivalent circuit for SPICE simulation.

The Elmore resistance R_{Elmore} is calculated from the channel resistance in strong inversion as

$$R_{Elomore} = \frac{L_{eff}^2}{e\mu_{eff}Q_{ch}} \propto Rch \sim \frac{L_{eff}}{\mu_{eff}W_{eff}C_{ox}V_{gst}} \tag{2.1}$$

Where e is the Elmore constant with a theoretical value close to 5 and Qch is the total charge in the channel, this formulation is only valid above threshold where the drift current dominates. The overall relaxation time τ is model as two components: τ_{drift} and τ_{diff}. In strong inversion region, τ_{drift} is dominates ; in subthreshold region, τ_{diff} is dominates, the relaxation time τ can be written as follows:

$$\frac{1}{\tau} = \frac{1}{\tau_{diff}} + \frac{1}{\tau_{drift}} \tag{2.2}$$

where

$$\tau_{drift} = R_{Elmore} C_{ox} W_{eff} L_{eff} \sim \frac{L^2}{\mu V_{gst}} \tag{2.3}$$

$$\tau_{diff} = \frac{qL_{eff}^2}{16\mu_0 KT} \tag{2.4}$$

2.2 Scattering parameters

At microwave frequency the Z, Y and H parameters are very difficult to measure, the reason is that short and open circuits to ac signals are difficult to implement at microwave frequencies, so that, the scattering matrix are used usually in the analysis of two port networks usually.

Considering the two-port network with incident wave a1 and reflected wave b1 at port1, and incident wave a2 and reflected wave b2 at port 2, the S parameters can be written in matrix form as:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{2.5}$$

2.2.1 Two-port network parameters conversion

At a given frequency, a two-port network can be described in terms of several parameters. Therefore, there is a conversion relationship between the parameters, for example, the conversion relation between the S and Z parameters can be shown as:

$$[S] = ([Z] + [Z_0])^{-1}([Z] - [Z_0]) \tag{2.6}$$

$$[Z] = [Z_0]([1] + [S])([1] - [S])^{-1} \tag{2.7}$$

where $[Z_0]$ is the characteristic impedance diagonal matrix, and $[1]$ is the unit diagonal matrix. The other conversions among the Z, Y, H, and S parameters also be included in the ADS and ICCAP for using, they are useful to analyze the small signal equivalent circuit.

2.2.2 Four-port scattering parameters

The extension of the formulation to four-port network is simple, the transmission lines are assumed to be lossless with characteristic impedance Z_0, and then, we can write the scattering parameters of the four-port in matrix form

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{bmatrix} \quad ; \quad [b] = [S][a] \tag{2.8}$$

Note that the value of S_{11} in (2.8) will be different from the value of S_{11} in a two-port common source configuration. For example, S_{11} can be arranged form the S matrix in (2.8) as

$$S_{11} = \left.\frac{b1}{a1}\right|_{a2=a3=a4=0} \tag{2.9}$$

To measure S_{11}, the matched resistive terminations of 50Ω are used at ports 2, 3, and 4, and the ratio b1/a1 is obtained. In a two-port common source configuration, S_{11} is measured with reference resistance 50Ω at port 2 and source/body grounding. Similarly, the parameters S_{12}, S_{21}, and S_{22} in four-port S matrix will be different form the parameters in two-port matrix.

2.2.3 Port reduction method in S-parameters

Considering a 4-port networks system, the I-V relationship of the extrinsic and intrinsic parameters can be written as a 4X4 Y matrix

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} & Y_{14} \\ Y_{21} & Y_{22} & Y_{23} & Y_{24} \\ Y_{31} & Y_{32} & Y_{33} & Y_{34} \\ Y_{41} & Y_{42} & Y_{43} & Y_{44} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} \tag{2.10}$$

According to equation (2.10), grounding a terminal is simply giving the corresponding zero supply voltage, and the remained sub-matrix will be the Y matrix representing the resulting configuration of the MOSFET, therefore, the 4 x 4 matrix of the 4-port networks can be reduced to 3-port or 2-port Y matrix.

For example, the common source(CS) configuration is source (port3) and body (port4) grounding, the CS 2-port Y matrix can be obtained by setting the Vs=Vb=0V in the 4-port measurement, in this case, the term of source and body in (2.10) is negligible, the reduced Y matrix can be written as

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{2.11}$$

Similarly, the common gate and common drain Y matrix can be obtained by setting the corresponding supply voltage to zero.

2.3 RF MOSFET design

To understand the dependency of device parameters, and develop better scaling RF model at high frequency, the extraction from the measured S parameters are presented under various bias conditions and geometries, both two-port 3T and four-port 4T RF MOSFETs are covered in this work. In this study, four-port S parameter measurement is supported by Radio Frequency Technology Center of National Nano Device Laboratory (NDL RFIC). The device geometries of two-port 3T and four-port 4T MOSFETs are listed in Table. 2.1 and Table 2.2, respectively.

Table 2.1 The device geometries of two-port 3T MOSFETs

L(um)	W(um)	NF	Dummy Pad	
0.13	4	6,18,36,72	open	short
0.18	4	6,18,36,72		
0.35	4	6,18,36,72		
0.5	4	6,18,36,72		

Table 2.2 The device geometries of four-port MOSFETs

L	W	NF	Dummy Pad	
0.13	4	6	open NF=6	short NF=6
0.13	4	18	open NF=18	short NF=36
0.13	4	36	open NF=36	

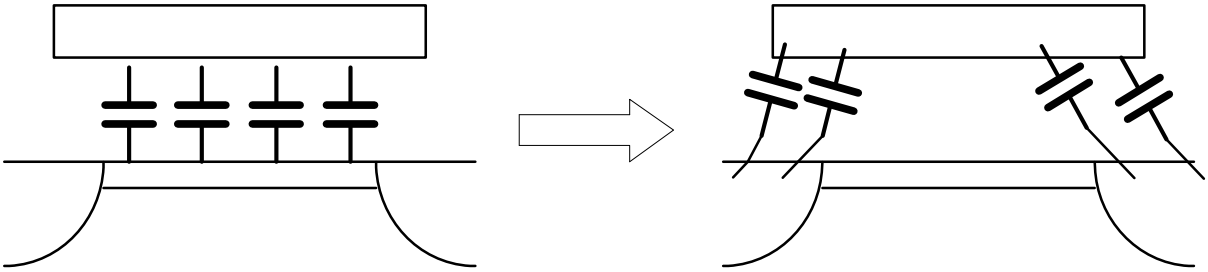


Fig. 2.1 Quasi-static model assumption

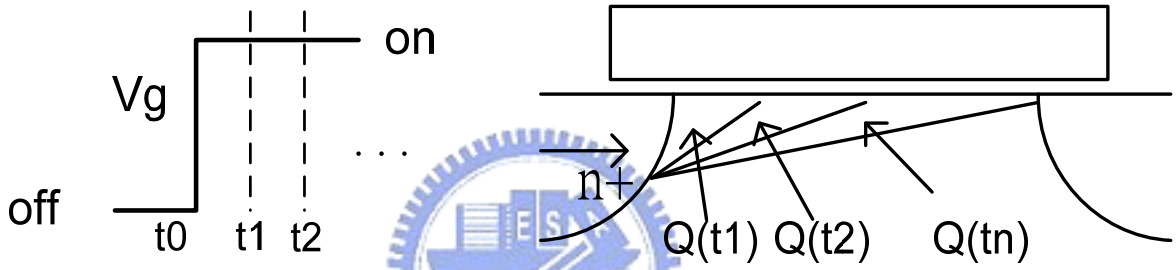


Fig. 2.2 Input signals and the channel charge response

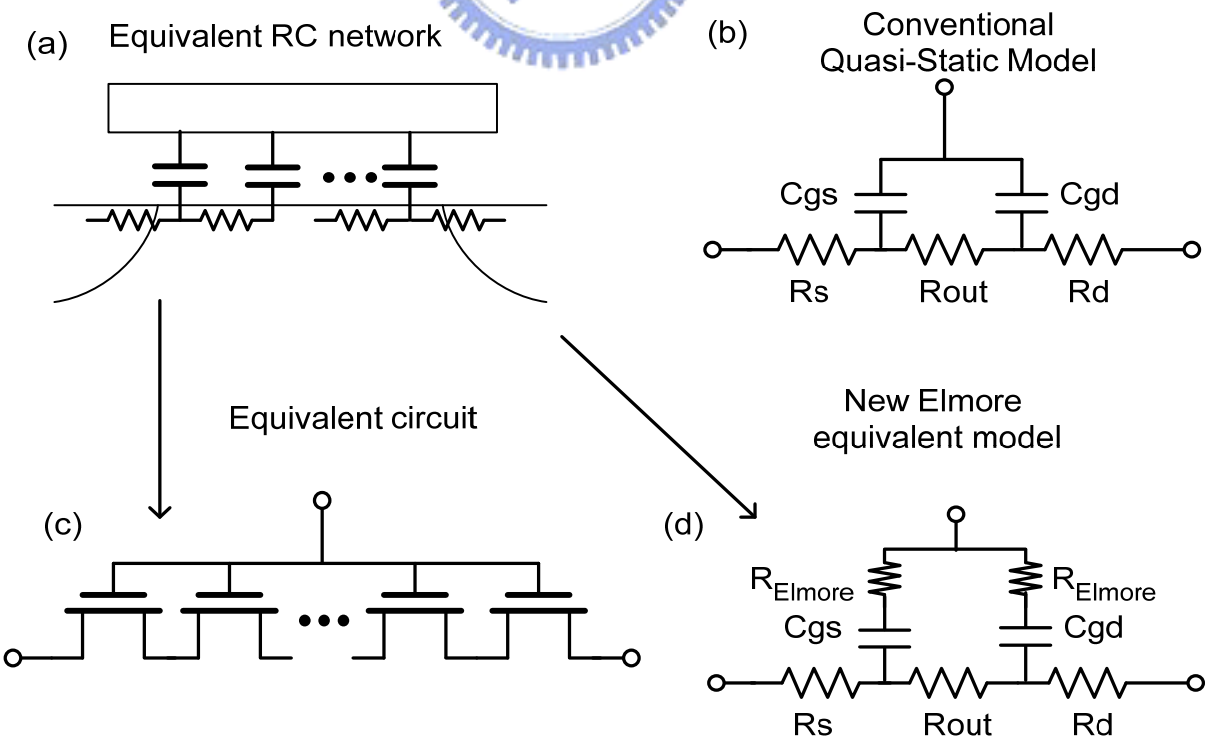


Fig. 2.3 Quasi-Static and Non-Quasi-Static models for SPICE analysis

Chapter 3

Two-port 3T RF MOSFET Model Parameter Extraction

3.1 De-embedding methods and verification

The test structures of the RF MOSFET includes the actual device under test (DUT) and parasitic components form the metal interconnections to the pad structures, in order to model the behavior of the DUT accurately and extracting MOSFET parameters from measured data, to build de-embedding method is necessary for the purpose, and the de-embedding method in the thesis will use “open” and “short” de-embedding method.

3.1.1 Open de-embedding

The dummy open pad is designed to clear the parallel coupling capacitances, the test structures is the full structure take off the layer under metal1(M1), and the open de-embedding step can be describe as follows.

a. Measure the S parameters of the DUT and transform it into Y parameters.

$$S_{mea} \rightarrow Y_{mea} \tag{3.1}$$

b. Measure the S parameters of the dummy open pad and transform them into Y parameters.

$$S_{open} \rightarrow Y_{open} \quad ; \quad Y_{open} = \begin{bmatrix} Y_{C1} + Y_{C3} & -Y_{C3} \\ -Y_{C3} & Y_{C2} + Y_{C3} \end{bmatrix} \tag{3.2}$$

c. Subtract the Y parameter of the open pad from the Y parameters of DUT.

$$Y_{mea\_o} \rightarrow Y_{mea} - Y_{open} \tag{3.3}$$

Fig. 3.1 and Fig. 3.2 represent the equivalent circuit of 3T device with pad and

dummy open pad respectively, the open pad equivalent circuit is composed of capacitance mainly, in Fig. 3.1, Y_{C1} and Y_{C2} are coupling parameters between pads and reference ground, Y_{C3} is the coupling parameter between two signal pads. Z_{RL1} ~ Z_{RL3} parameters are related to the metal line layout in each terminal of device, and the parameters will be discussed later in section 3.1.2. So far, we can get the first de-embed Y parameters of device, and the parameters can be used to calculate the value of the components in equivalent circuit model.

3.1.2 Short de-embedding

The open de-embedding method can de-embed the parasitic components in parallel with the DUT, but there are still the parasitic components in series with the DUT. Thus, the dummy short pad is designed to clear the series parasitical parameters, the dummy short pad structures uses the layout of open pad and connected all terminals together in metal3, the short de-embedding step can be describe as follows.

a. Measure the S parameters of the Short pad and to execute open de-embedding.

$$S_{short} \rightarrow Y_{short} \;\; ; \;\; Y_{short} - Y_{open} = Y_{short\_o} \tag{3.4}$$

b. Convert Y_{mea_o} and Y_{short_o} parameters into Z parameters.

$$Y_{mea\_o} \rightarrow Z_{mea\_o} \;\; ; \;\; Y_{short\_o} \rightarrow Z_{short\_o}$$

$$Z_{short\_o} = \begin{bmatrix} Z_{RL1} + Z_{RL3} & Z_{RL3} \\ Z_{RL3} & Z_{RL2} + Z_{RL3} \end{bmatrix} \tag{3.5}$$

c. Subtract the Z parameter of the Z_{short_o} from the Z parameters of Z_{mea_o}.

$$Z_{dut} = Z_{mea\_o} - Z_{short\_o} \tag{3.6}$$

$$Z_{dut} \rightarrow Y_{dut} \tag{3.7}$$

Remember that all test structure have the parasitic capacitances between the GSG pad and ground, so that, all test structure need to do the open de-embedding first in order to substrate the coupling parameters. The equivalent circuit of short pad is shown In Fig. 3.3, we support that there are only parasitic parameters Z_{RL1}~Z_{RL3} originate from metal interconnections between the terminal of DUT and the pad. The intrinsic Z parameters of the DUT can be obtained through conventional open and short de-embedding discussed above, the final Z matrix also can be converted to Y parameters or S parameters for the need. Fig. 3.4 is a good illustration of showing de-embedding procedures discussed in preceding paragraphs.

3.2 Parasitic resistance and inductance extraction and analysis

The two-port 3T RF MOSFET is implemented with common source configuration that source and body terminals are tied together in metal3 and grounding, and the terminals of DUT connect to GSG pad by metal line. In our experience, the parasitic resistance contributed from the metal line will affect the I-V characteristic of DUT. For the purpose, we will extract the parasitic RL parameters from short pad and extract RL parameters from device directly in this session.

3.2.1 Parasitic RL extraction from short pad

The equivalent circuit of short pad after open de-embedding can be represented as Fig. 3.5. According to the layout, the metal line connects form metal3(M3) to metal8(M8), we assume that it is composed of parasitic resistance and inductance only form metal interconnections between the DUT and the pad, and the parameters with subscript “ext” to represent extrinsic RL parameters.

By analysis the Z parameters of the equivalent circuit of short pad after open

de-embedding, the Z parameters can be express as follow:

$$Z_{short\_o} = \begin{bmatrix} \left(R_{g,ext} + j\omega L_{g,ext}\right) + \left(R_{s,ext} + j\omega L_{s,ext}\right) & R_{s,ext} + j\omega L_{s,ext} \\ R_{s,ext} + j\omega L_{s,ext} & \left(R_{d,ext} + j\omega L_{d,ext}\right) + \left(R_{s,ext} + j\omega L_{s,ext}\right) \end{bmatrix} \quad (3.8)$$

In addition, the parasitic resistance and inductance can be expressed by arrange the (3.8) in the form.

$$\begin{aligned} R_{s,ext} &= \mathrm{Re}\left(Z_{12}^{short\_o}\right) & L_{s,ext} &= \mathrm{Im}\left(Z_{12}^{short\_o}\right)/\omega \\ R_{g,ext} &= \mathrm{Re}\left(Z_{11}^{short\_o} - Z_{12}^{short\_o}\right) \quad ; & L_{g,ext} &= \mathrm{Im}\left(Z_{11}^{short\_o} - Z_{12}^{short\_o}\right)/\omega \\ R_{d,ext} &= \mathrm{Re}\left(Z_{22}^{short\_o} - Z_{12}^{short\_o}\right) & L_{d,ext} &= \mathrm{Im}\left(Z_{22}^{short\_o} - Z_{12}^{short\_o}\right)/\omega \end{aligned} \quad (3.9)$$

The extracted $R_{g,ext}$ and $R_{d,ext}$ have the weak frequency dependence at low frequency, the behavior indicated that there are frequency term without considered at high frequency probably. Although it has the behavior, the parasitic RL parameters are extracted at low frequency.

Table 3.1 The extracted extrinsic resistance and inductance of short pad

Extracted extrinsic RL	R_{g_ext} (Ω)	R_{d_ext} (Ω)	R_{s_ext} (Ω)	L_{g_ext} (pH)	L_{d_ext} (pH)	L_{s_ext} (pH)
AVG(2~5G)	0.355	0.589	0.228	57.05	57.72	15.11

3.2.2 Parasitic RL extraction from device

In chapter 3.2.1, we discuss the approximate parasitic resistance and inductance from short pad, but this part of resistance and inductance come from metal connection between metal3 and metal8 only, in order to determine total terminal resistance come form metal1 to metal8, parasitic parameters are extracted from device after open de-embedding only directly.

When MOSFET operating in strong inversion region and V_{ds}=0V, the equivalent circuit of DUT after open de-embedding can be represented as Fig. 3.6. Refer to the

publishing in our laboratory, parasitic RL extraction method can be summarized as the following equation.

$$\mathrm{Re}\left(Z_{12}^{dut}\right)\approx\frac{R_{ch}}{2}\Rightarrow R_{ch}=2\cdot\mathrm{Re}\left(Z_{12}^{dut}\right) \tag{3.10}$$

$$\mathrm{Re}\left(Z_{12}^{mea\_o}\right)=R_S+\frac{R_{ch}}{2}\quad;\quad R_S\approx R_{s,ext} \tag{3.11}$$

$$\mathrm{Re}\left(Z_{22}^{mea\_o}\right)=R_D+R_S+R_{ch} \tag{3.12}$$

$$\mathrm{Re}\left(Z_{11}^{mea\_o}\right)=R_G+R_S+\frac{R_{ch}}{4} \tag{3.13}$$

$$\begin{aligned}&\mathrm{Im}\left(Z_{12}^{mea\_o}\right)\Big/\omega=L_S-\frac{C_{gd}R_{ch}^2}{4}\\&\mathrm{Im}\left(Z_{22}^{mea\_o}\right)\Big/\omega=L_D+L_S-\frac{C_{gd}R_{ch}^2}{2}\quad,\omega\to0\\&\mathrm{Im}\left(Z_{11}^{mea\_o}\right)\Big/\omega=L_G+L_S-\frac{1}{2\omega^2C_{gd}}\end{aligned} \tag{3.14}$$

3.2.3 Frequency and bias dependence of Parasitic RL

It has been known that gate resistance will influence the input impedance and noise performance of RF MOSFET at high frequency, for the layout of multi-finger MOSFET, the gate/drain terminal is used parallel structure to reduce the gate/drain resistance. The terminal parasitic RL represents the effective lumped resistance and inductance that consists of both intrinsic and extrinsic part.

The effective lumped resistance and inductance can be considered to have a gate bias dependent and a bias independent component, remember that the terminal of DUT connect to the GSG pad by metal only, it means that the bias independent parasitic RL contributed from the extrinsic metal interconnection between M3 and M8, and the bias dependent RL will be contributed from the intrinsic MOSFET device.

We have extract the parameters from devices with various channel length (L) and gate finger number (NF) at several bias conditions under the suitable frequency, and observe that R_D and R_G are almost const in short channel device but sensitive to the gate bias at long channel device, the parasitic resistance decreases with gate bias increases. Thus, the optimizing R_G and R_D verse $(Vgs - Vth)^{-1}$ at different geometry is plotted in Fig. 3.7 and Fig. 3.8.

The effective gate resistance that consists of the distributed channel resistance and the gate electrode resistance, the effective drain resistance that consists of the electrode resistance and the resistance contributed from the channel, the expression for gate/drain resistance model can be written as:

$$R_G = R_{g\_poly} + R_{g\_ch} = R_{g\_const} + \frac{R_{g\_bias}}{V_{gs} - V_{th}} \quad (3.15)$$

$$R_D = R_{d\_poly} + R_{d\_ch} = R_{d\_const} + \frac{R_{d\_bias}}{V_{gs} - V_{th}} \quad (3.16)$$

R_G versus inverse of (Vgs -Vth) is plotted to obtain R_{g_poly} and R_{g_ch}, where R_{g_poly} and R_{g_ch} represent the gate bias independent resistance and gate bias dependent resistance respectively, R_{g_poly} can be determined from the linear regression of measurement data intercept at $(Vgs - Vth)^{-1}=0$, in addition, R_{g_bias} is obtained from the slope of the liner regression equation in Fig. 3.7. Similarly, R_{d_const} can be determined from the linear regression of measurement data intercept at $(Vgs - Vth)^{-1}=0$, R_{d_bias} is obtained from the slope of the liner regression equation in Fig. 3.8. It provides that electrode resistance is bias independent, but distributed channel resistance is bias independent again.

3.2.4 Device geometry dependence

In this session, we will discuss the geometry dependence of gate/drain resistance further, the optimizing R_G verse channel length at different Vgs is plotted in Fig. 3.9, it shows that R_G decreases first as channel length increase while showing a weak bias dependence in the region, then to increase with channel length increase above 0.18um while showing a strong bias dependence. The channel length dependence of R_G is strong on longer device and at lower Vgs.

The U-shape channel length dependence of R_G in Fig. 3.9 can be explained with the consideration of the distributed effects in both distributed transmission line effect on the gate and NQS effect in the channel. It has been well known that the resistance of a poly-silicon resistor is proportional to 1/L, and resistance of NQS effect is proportional to L.

The extracted R_{g_const} and R_{g_bias} decrease with increasing finger number (NF) in the all devices, Fig. 3.10~3.13 show that extracted R_{g_const}, R_{d_const}, R_{g_bias} and R_{d_bias} verse inverse of NF individually, the result support us that the linear regression of the resistances is a good reciprocal function of NF, and the behavior proved that the resistance originate from channel distributed effect obviously.

Using the method to separate the bias and geometry dependent and independent component from the R_G, the total parasitic resistance R_G can be written as below, where α, β almost is constant.

$$\begin{aligned} R_G &= R_{g\_poly} + R_{g\_ch} \\ &= R_{g\_poly} + R_{g\_nqs} \\ &= R_{g\_const} + \frac{R_{g\_bias}}{V_{gs} - V_{th}} \\ &= R_{g\_ext} + \frac{\alpha}{L * NF} + \frac{\beta * L}{NF * (V_{gs} - V_{th})} \end{aligned} \tag{3.17}$$

The calculated R_{g_poly} and R_{g_ch} verse channel length show in the Fig. 3.14 and Fig. 3.15. R_{g_poly} decrease with the channel length increasing, and R_{g_ch} increase with the channel length increasing. When channel is short enough, the contribution of R_{g_ch} is smaller than $R_{g\_poly,}$, R_{g_poly} is gate bias insensitively and dominate the total resistance. As channel length increasing, the NQS effect is more significant, R_{g_ch} will dominate the R_G, and R_G has a strong gate bias dependence. So that, it provides that R_{g_poly} and R_{g_ch} cause the U-shape channel length dependence of the total gate terminal resistance.

3.3 Extraction of device parameters in linear region

In this section, we will discuss that parameters extraction of MOSFET operating in linear region. When gate voltage is smaller than the threshold voltage and at Vds=0V, the equivalent circuit of 3T device with parasitic RL parameters and substrate network components can be shown in Fig. 3.16. Cgs0 and Cgd0 represent the gate-to-source and gate-to-drain zero bias capacitances, respectively. Cgb is the total intrinsic and extrinsic gate-to-body capacitances. Cjs and Cjd are diffusion junction capacitances, Rsub represents the substrate resistance and Cdnw is junction capacitance between substrate and deep N-well.

3.3.1 Capacitance extraction and analysis

Capacitances of RF MOSFET are extracted from the intrinsic Y parameters at low frequency conventionally, short de-embedding is essential for accurate capacitances extraction in our experience. By performing Y parameter analysis on the circuit of intrinsic DUT in Fig. 3.17, the capacitance of equivalent circuit at low frequency can be express by

$$\mathrm{Im}\left(Y_{11}^{dut}\right)=\omega\left(C_{gg}\right) \tag{3.18}$$

$$-\mathrm{Im}\left(Y_{12}^{dut}\right)=\omega C_{gd} \tag{3.19}$$

$$\mathrm{Im}\left(Y_{22}^{dut}\right)=\omega\left(C_{gd}+C_{jd}\right) \tag{3.20}$$

For $V_{gs}>V_{th}$, $C_{gg}=C_{gd}+C_{gs}$. For $V_{gs}<V_{th}$, $C_{gg}=C_{gdo}+C_{gso}+C_{gb}$.

Note that the capacitances Cgs and Cgd are equal almost because the symmetry structure in this bias condition. The extracted gate capacitances includes both intrinsic and extrinsic component of the MOSFET individually, it also can be separated the bias dependent or independent part by the gate voltage. The extracted capacitances appear non-smooth curve in the smaller finger number devices with the frequency, because that small device has the small capacitances compared to the capacitances of the open pad in operating open de-embedding, and the capacitances decreases by a time constant decay with frequency increasing, the issue can be solved by the goodly dummy open/short pad. Thus, we still extract the capacitances of measured data at low frequency as the initial value of the circuit.

3.3.2 Capacitance bias and geometry dependence

The gate-bias dependences of the optimizing capacitances are shown in Fig. 3.18, the intrinsic capacitance is normally bias dependent while the overlap capacitance is bias independent. when gate voltage small than the threshold voltage, To observe the transcapacitances conservation, the gate capacitances cab be rewrite as the equation Cgg=Cgd0+Cgs0+Cgb, As the gate voltage increases, the channel charges build up to increase the intrinsic component of the extracted capacitances, when the channel charge can be supplied by source/drain to channel rather than body in the strong inversion region, the whole Cgb capacitance which through the active

channel area to source/drain region is very small and can be neglected, the gate capacitances can describe as Cgg=Cgd+Cgs.

In the simplified C-V model, the gate capacitance can be described as equation (3.21). under a given gate voltage, we will discuss the capacitance geometry dependence, Fig. 3.19 and Fig. 3.20 show that the gate capacitances are well proportioned to the NF and channel length, the intercept of Y-axis is much closed to zero, and it verifies that the proposed extraction method is accurate and reliable.

$$Q_g = W_{active} L_{active} C_{ox} * V(V_{gs}) \tag{3.21}$$

3.3.3 Channel resistance extraction and analysis

When MOSFET operates at strong inversion region and Vds=0V, the extracted channel resistance Rch discussed above in question (3.10), Rch is considered as a intrinsic parameter originate form the inversion layer channel charge, the bias, NF, and channel length dependent are plotted in Fig. 3.21~Fig. 3.23, individually.

As the Vgs increasing, the channel charge can be supplied by source/drain to channel is increasing, the depths of inversion layer is increasing similarly, the behavior will cause the Rch decrease as vgs increase, Rch also decrease as NF increase base on the multi-finger gate/drain structure, but the total Rch is sum of the distributed channel resistance at the source/drain direction, Rch will increase with the longer channel length. So that, channel resistance is inverse proportion to gate voltage and finger number but is propositional to channel length. Rch is well propositional to geometry provided that the channel resistance is dominated by the intrinsic resistance from the device only.

3.3.4 Substrate resistance extraction and analysis

One of the most important features to be considered when the MOSFET is

operated at high frequencies is the impact of the substrate network on the output impedance. This substrate network consists of the junction capacitances and the substrate loss resistances, the drain junction capacitance and the bulk spreading resistance are represented by Cjd and Rsub, respectively.

As the operation frequency increases, the impedance of the junction capacitance reduces. The signal coupling through the substrate resistances from the drain to the source and from the drain/source to the substrate contact has to be carefully considered for the output admittance. By performing Y parameter analysis on the circuit of intrinsic DUT in Fig. 3.17, the parameters of equivalent circuit at low frequency can be express by:

$$C_{jd} = \mathrm{Im}\left(Y_{22}^{dut} + Y_{12}^{dut}\right)\Big/\omega \tag{3.22}$$

$$R_{sub} = \mathrm{Re}\left(Y_{22}^{dut}\right)\Big/\omega^{2} C_{jd}^{2} \tag{3.23}$$

We will extract the substrate parameters using (3.23) as the initial value, In order to achieve the best fit for the simulated and measured S-parameter data, optimization of all the RF component values must be done. The optimizing Cjd and Rbulk geometry dependence are plotted in Fig. 3.24 and Fig. 3.25.

3.4 Extraction of intrinsic parameters in saturation region

When MOSFET operating in saturation region, the equivalent circuit of DUT after open de-embedding can be represented as Fig. 3.26, the difference between linear region and saturation region is the asymmetry channel structure and current gain. The parameters gm and gds represent the transconductance and the output conductance of the transistor respectively, and uniform channel resistance replace by R_{ch} , R_{ds} and C_{ds} parameters to express the asymmetry inversion layer.

Refer to the thesis in our laboratory, and the extraction method of element can be

summarized as the following equation,

$$g_m = \frac{\partial I_d}{\partial V_{gs}} \quad ; \quad g_{ds} = \frac{\partial I_d}{\partial V_{ds}} \tag{3.24}$$

$$\frac{1}{g_{ds}} = R_{ch} + R_{ds} \quad ; \quad R_{ch}C_{gs} = R_{ds}C_{gd} \tag{3.25}$$

$$C_{jd}\Big|_{V_{gs}=V_{ds}=1.2V} = C_{jd}\Big|_{V_{gs}=0,\ V_{ds}=1.2V} \tag{3.26}$$

3.4.1 Capacitance extraction and analysis

Extraction of capacitance at Vds=0V (3.18~3.20) to be suitable for use at this condition, the gate bias dependences of extracted capacitances are shown in Fig. 3.27 and Fig. 3.28, Cgs and Cgd are composed of the intrinsic and overlap components, the intrinsic capacitance is normally bias dependent while the overlap capacitance is bias independent. As Vgs increases, the channel charges build up and increase the intrinsic component of the extracted capacitances.

Cgs has strong gate bias dependence in Fig. 3.27, Cgs increases strong as gate bias increases near subthreshold region, and is saturation gradually in the strong inversion saturation region. Cgd only increases slightly with gate bias in Fig. 3.28, under saturation conditions, intrinsic capacitances of Cgd are very small because that drain voltage will deplete the drain side capacitance, and the total gate-to-drain capacitance is dominated by the overlap capacitance.

From Fig. 3.27, it is observed that as Vds increases, there is a small increase in Cgs., this is because the transistor is approaching the saturation region and the channel is pinched-off when Vds=Vgs-Vth. The channel charge in the source side increases and the intrinsic capacitance of Cgs also increases. For Cgd, when the channel is approaching the pinch-off condition, the charge in the intrinsic drain region decreases and this decreases the intrinsic capacitance of Cgd.

The capacitance geometry dependence are plotted in Fig.3.29 ~ Fig. 3.32, the gate capacitances are well proportioned to the NF and channel length as the description in section 3.3.2.

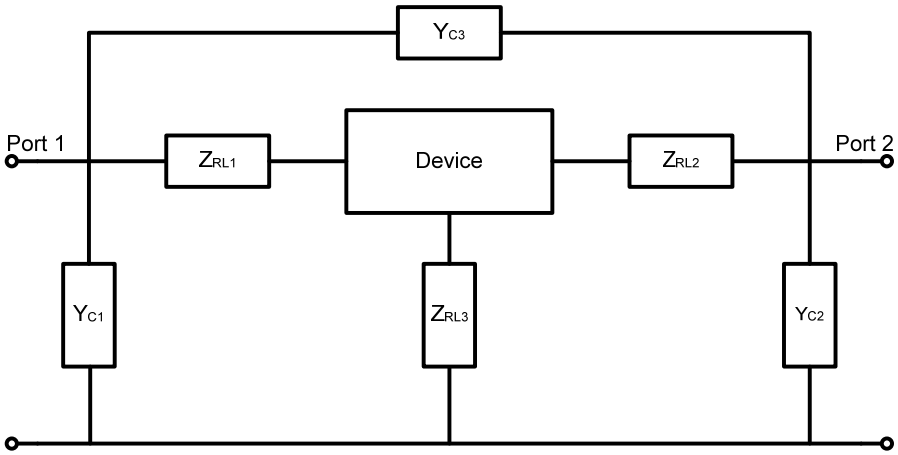


Fig. 3.1 The equivalent circuit of 3T device with pad

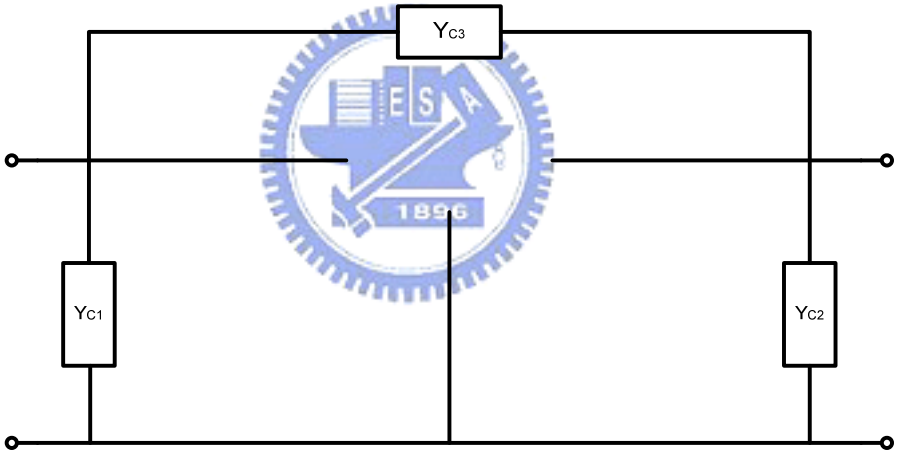


Fig. 3.2 The equivalent circuit of open pad

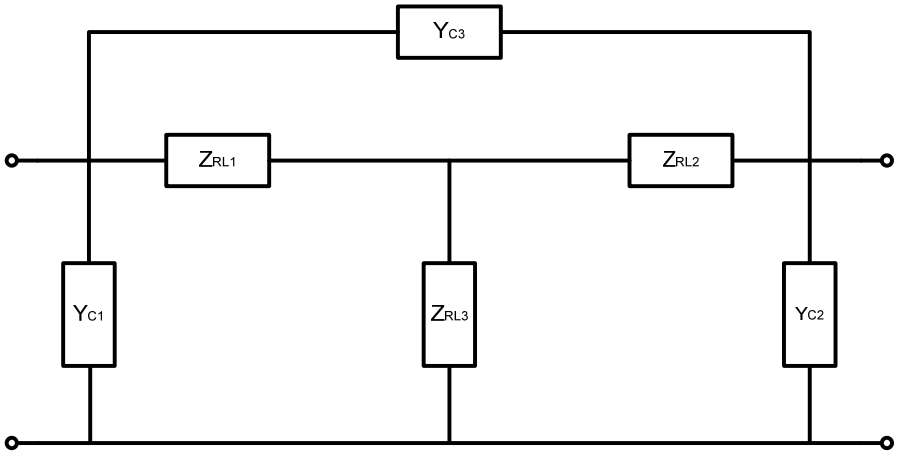


Fig. 3.3 The equivalent circuit of short pad

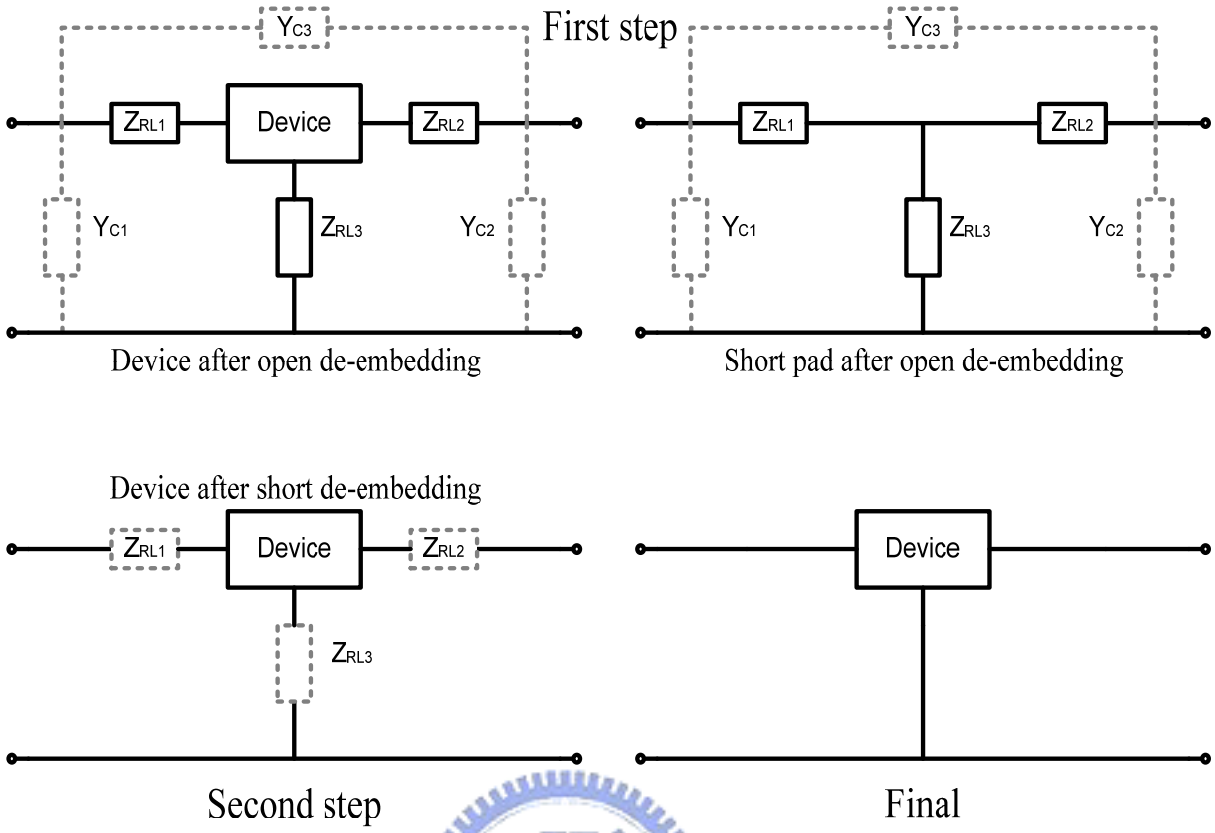


Fig. 3.4 The illustration of de-embedding procedure for 3T device

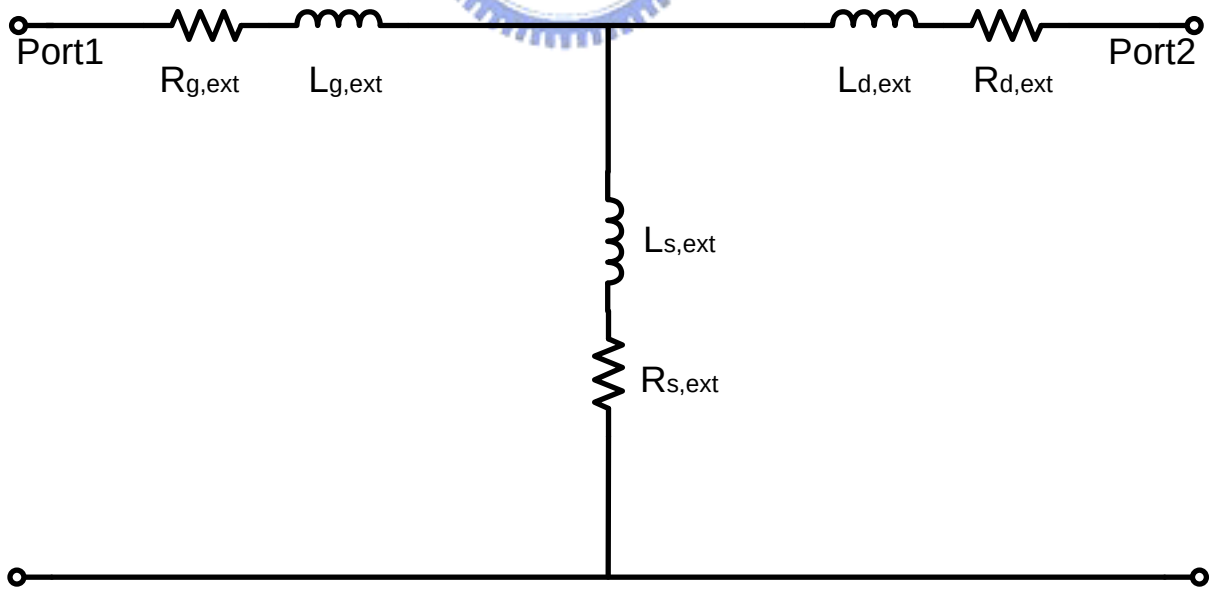


Fig. 3.5 The equivalent circuit of short pad after open de-embedding

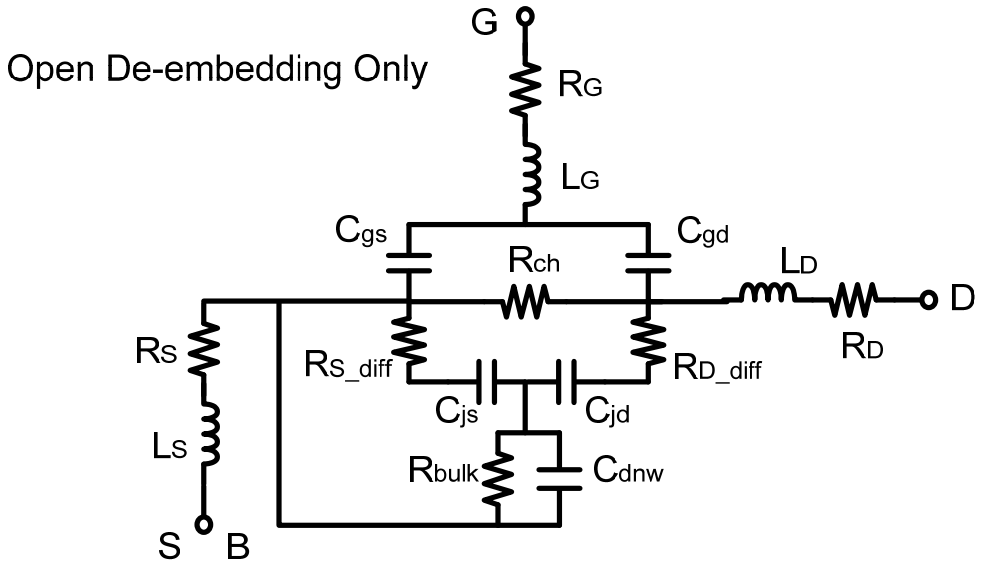


Fig. 3.6 The equivalent circuit of 3T device at V_{gs}>>V_{th}, V_{ds}=0V (Open_de)

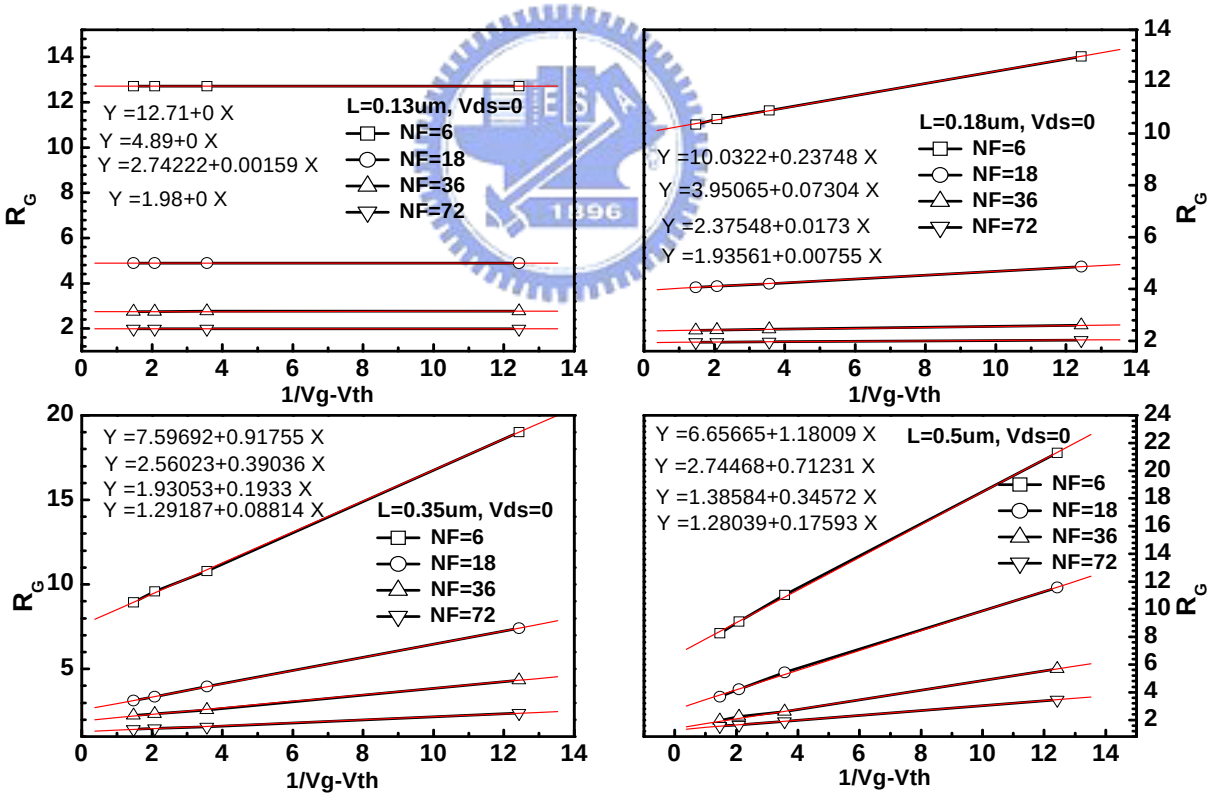


Fig. 3.7 linear regression of optimized R_G versus $(Vgs - Vth)^{-1}$ at Vds=0V

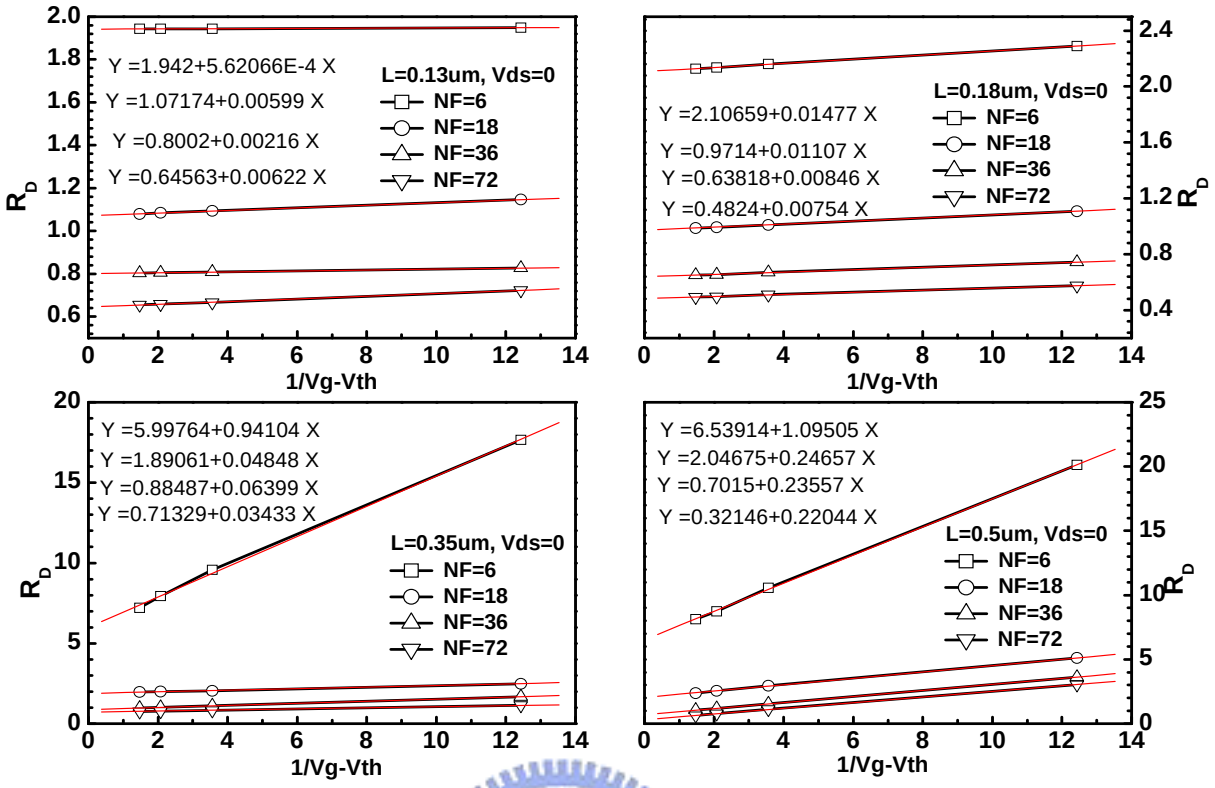


Fig. 3.8 linear regression of optimized R_D versus $(Vgs - Vth)^{-1}$ at Vds=0V

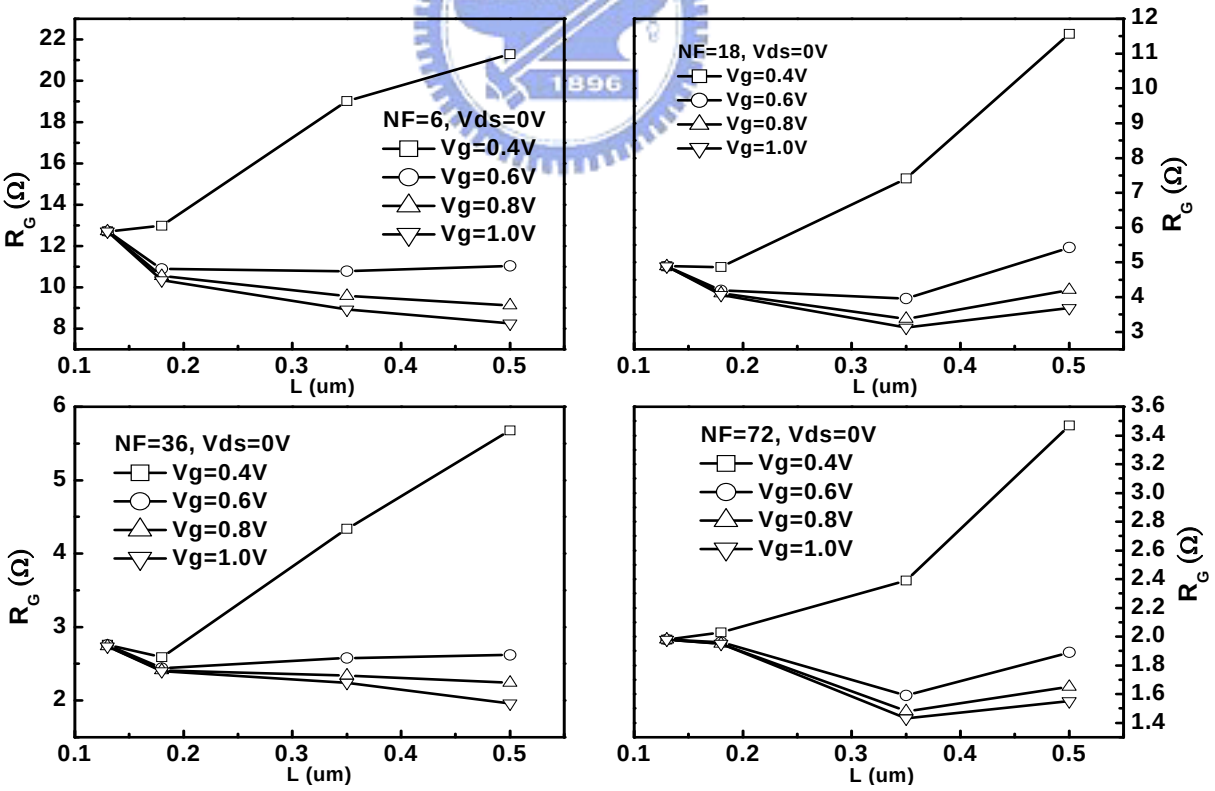


Fig. 3.9 The gate resistance optimized R_G versus channel length at Vds=0V

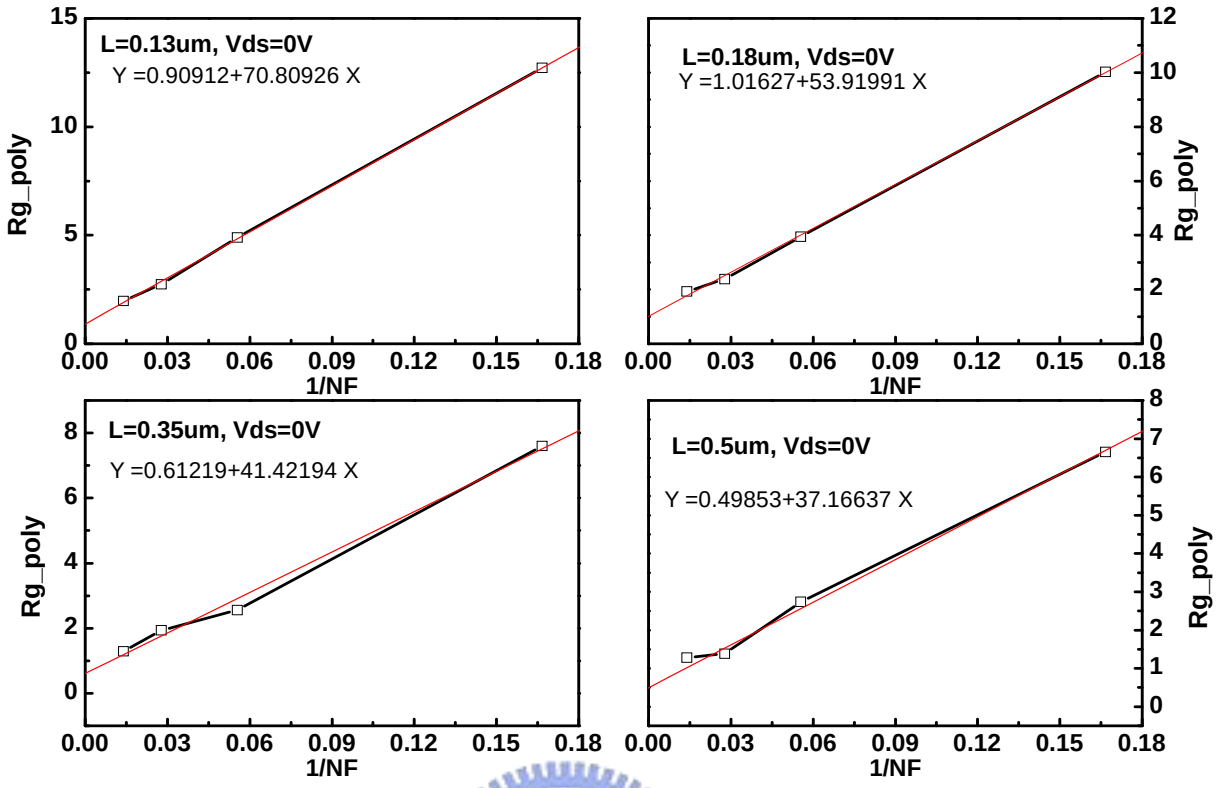


Fig. 3.10 linear regression of R_{g_poly} versus reciprocal of NF at Vds=0V

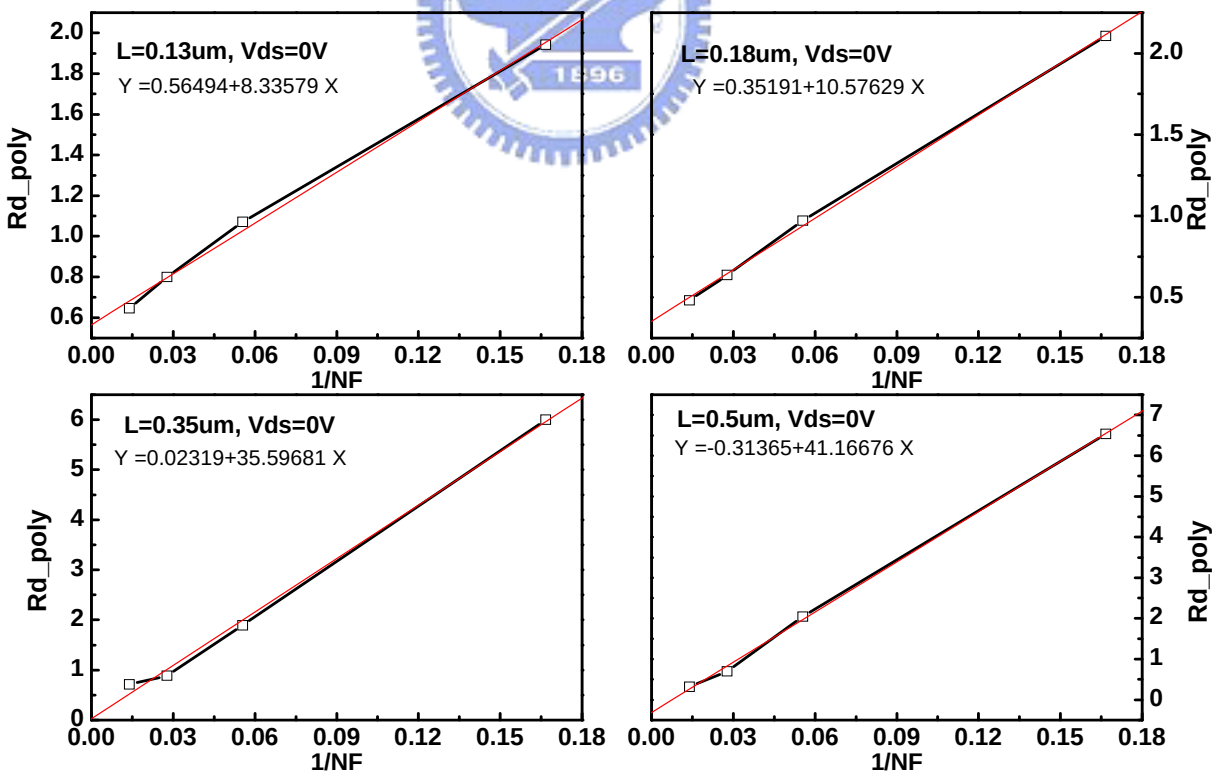


Fig. 3.11 linear regression of R_{d_poly} versus reciprocal of NF at Vds=0V

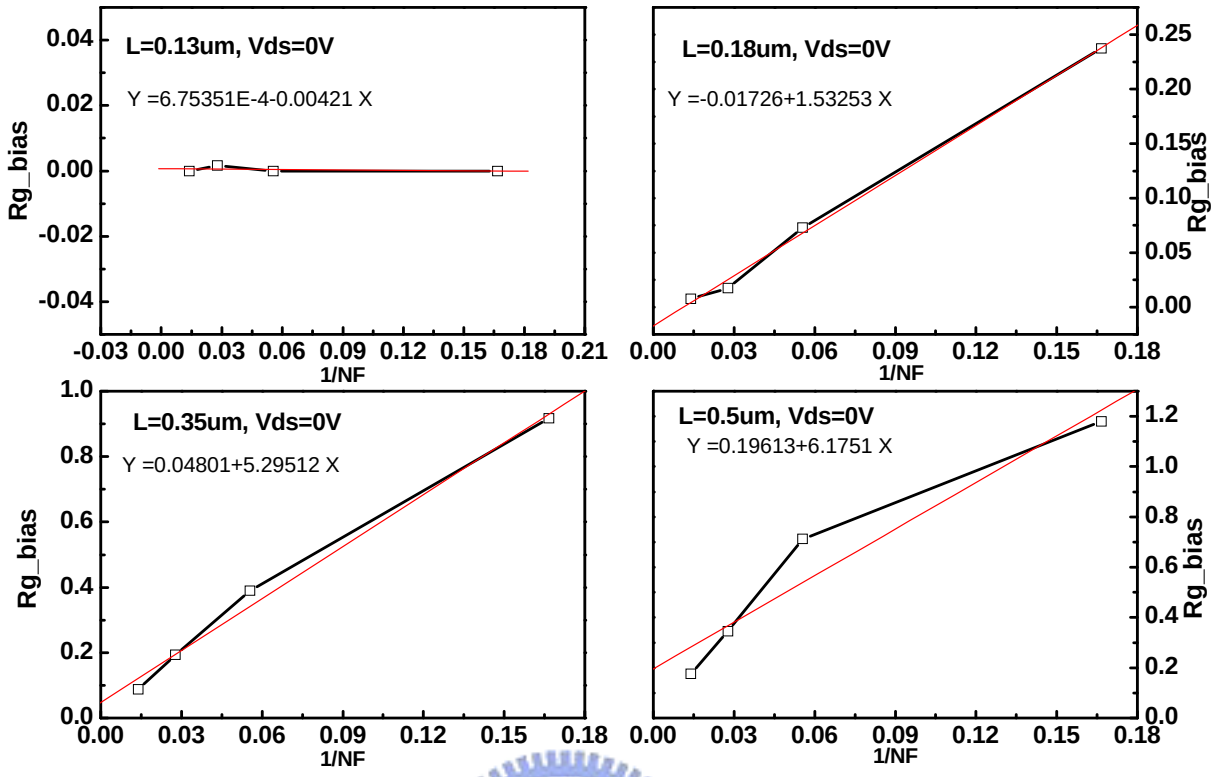


Fig. 3.12 linear regression of R_{g_bias} versus reciprocal of NF at Vds=0V

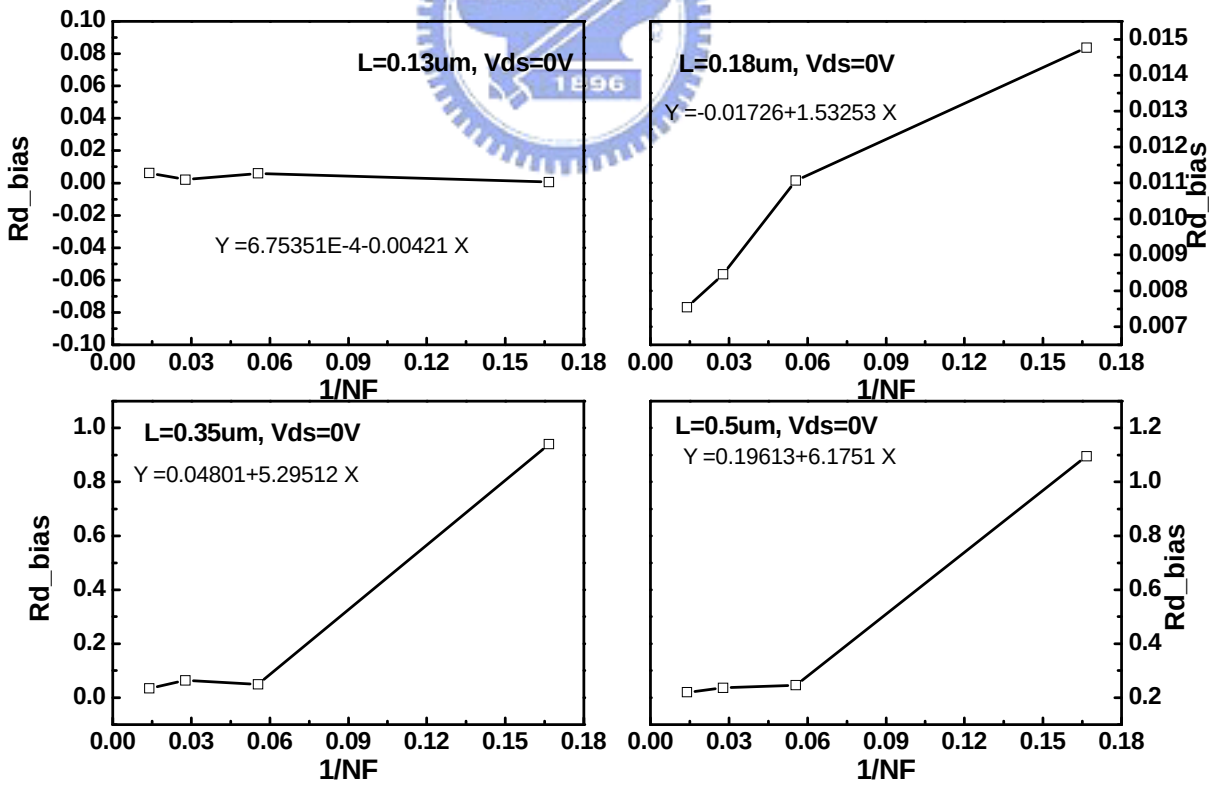


Fig. 3.13 linear regression of R_{d_bias} versus reciprocal of NF at Vds=0V

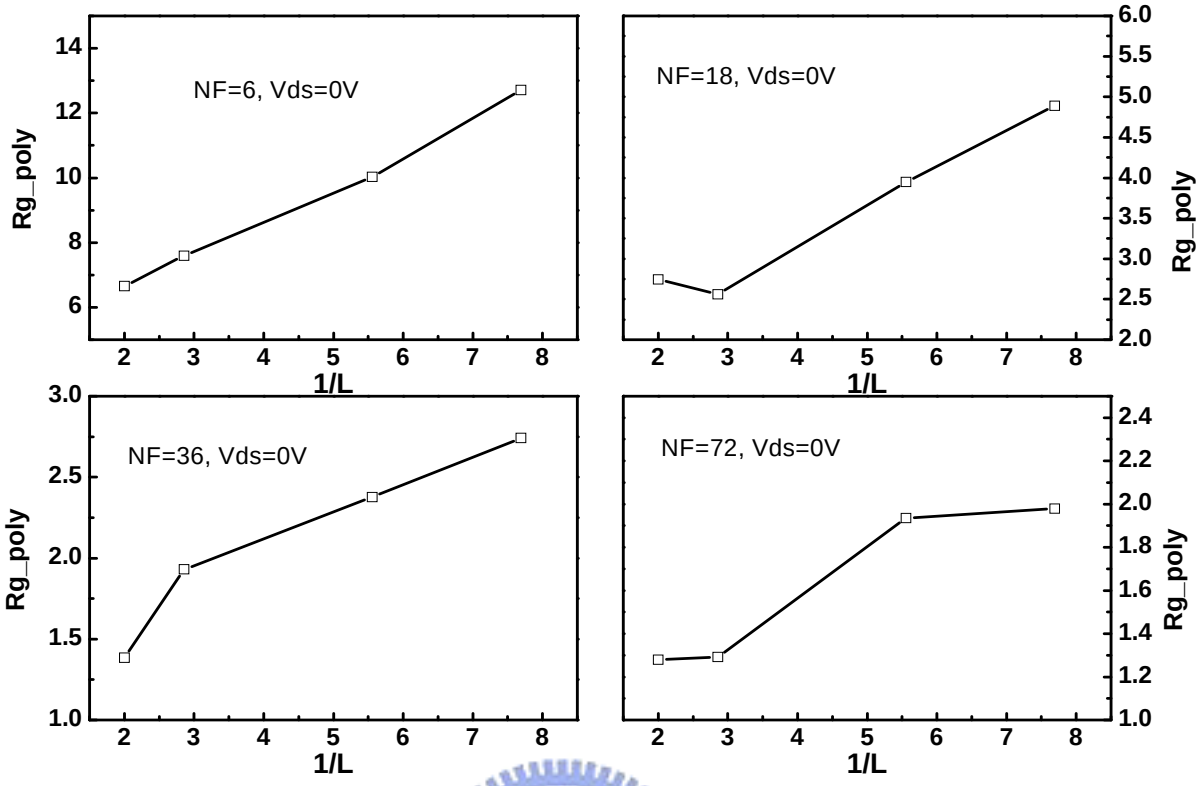


Fig. 3.14 channel length dependence of R_{g_poly} at Vds=0V

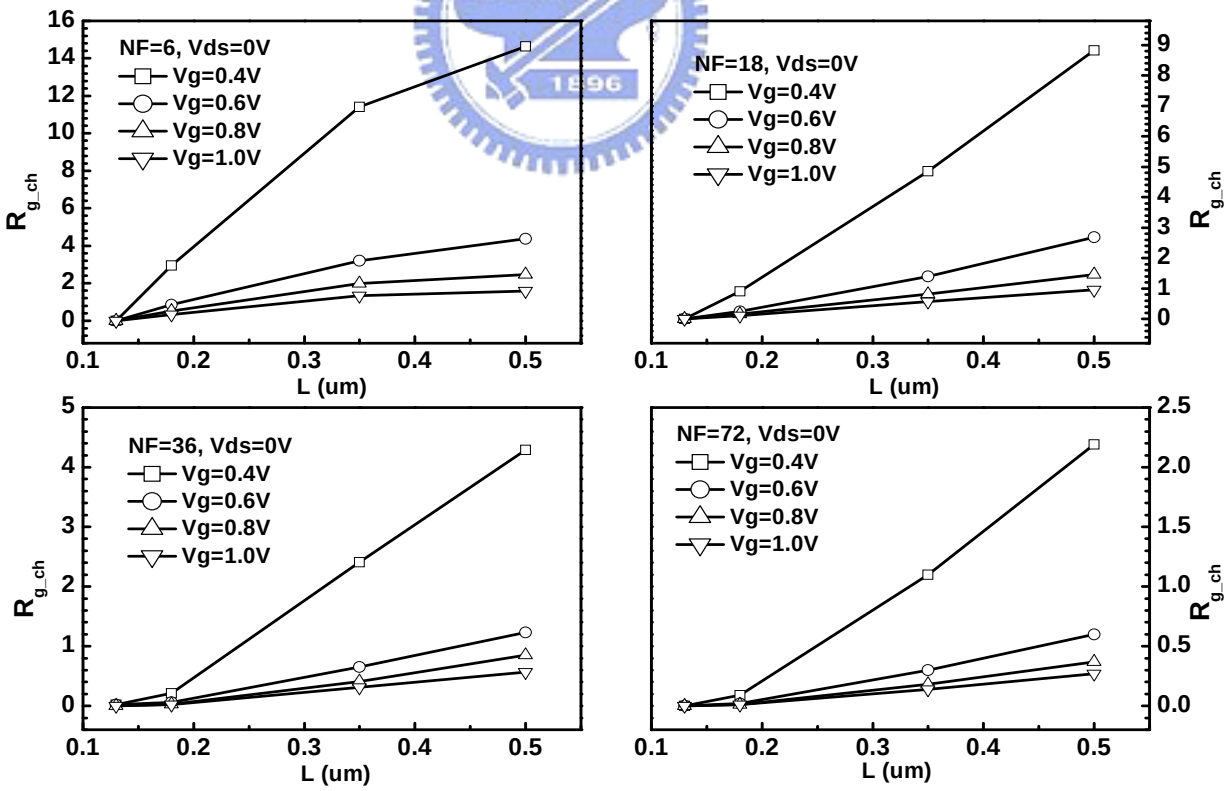


Fig. 3.15 channel length dependence of R_{g_ch} at Vds=0V

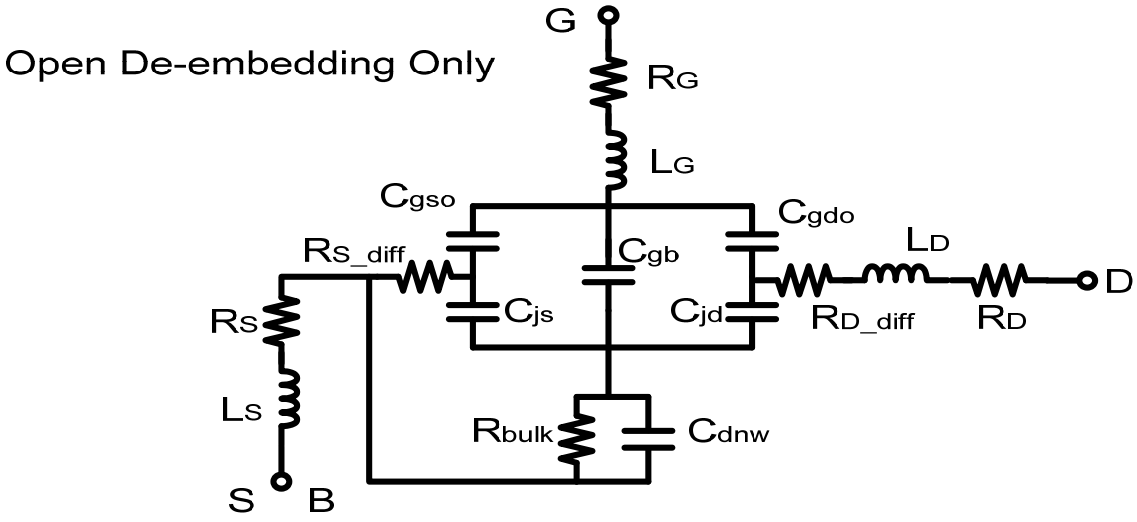
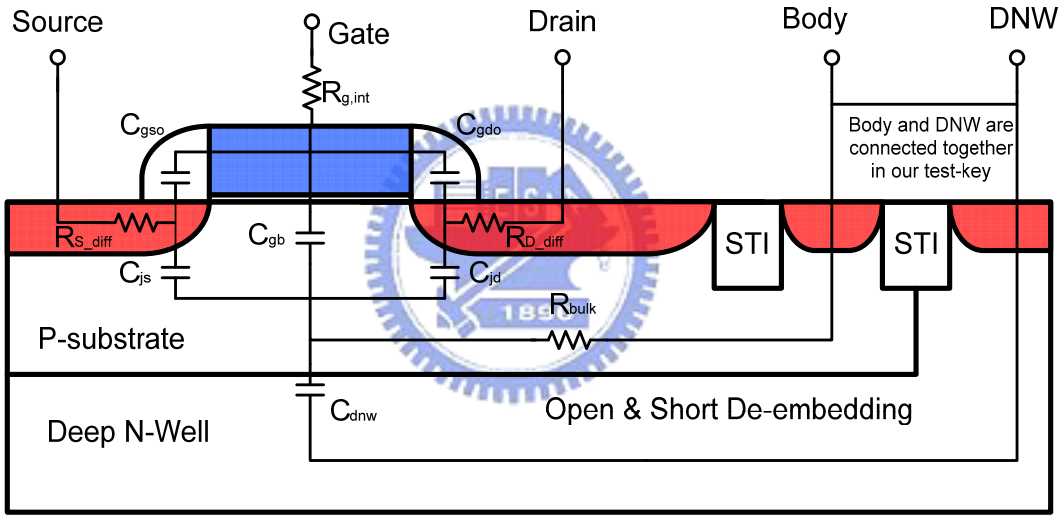


Fig. 3.16 The equivalent circuit of 3T device at V_{gs}=V_{ds}=0V (Open_de)



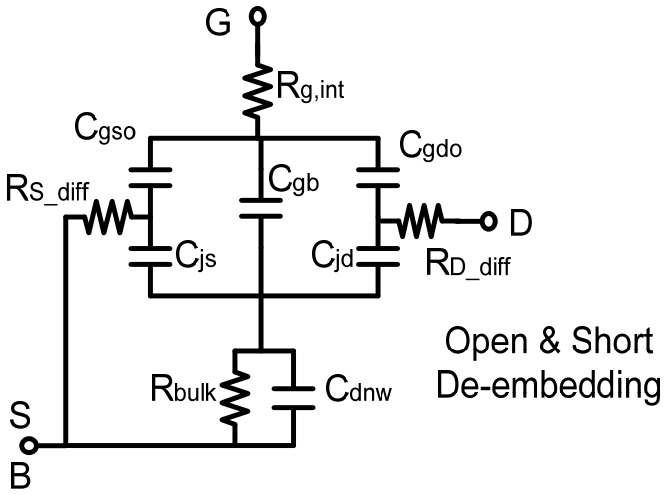


Fig. 3.17 The equivalent circuit of 3T device at V_{gs}=V_{ds}=0V (Open+Short_de)

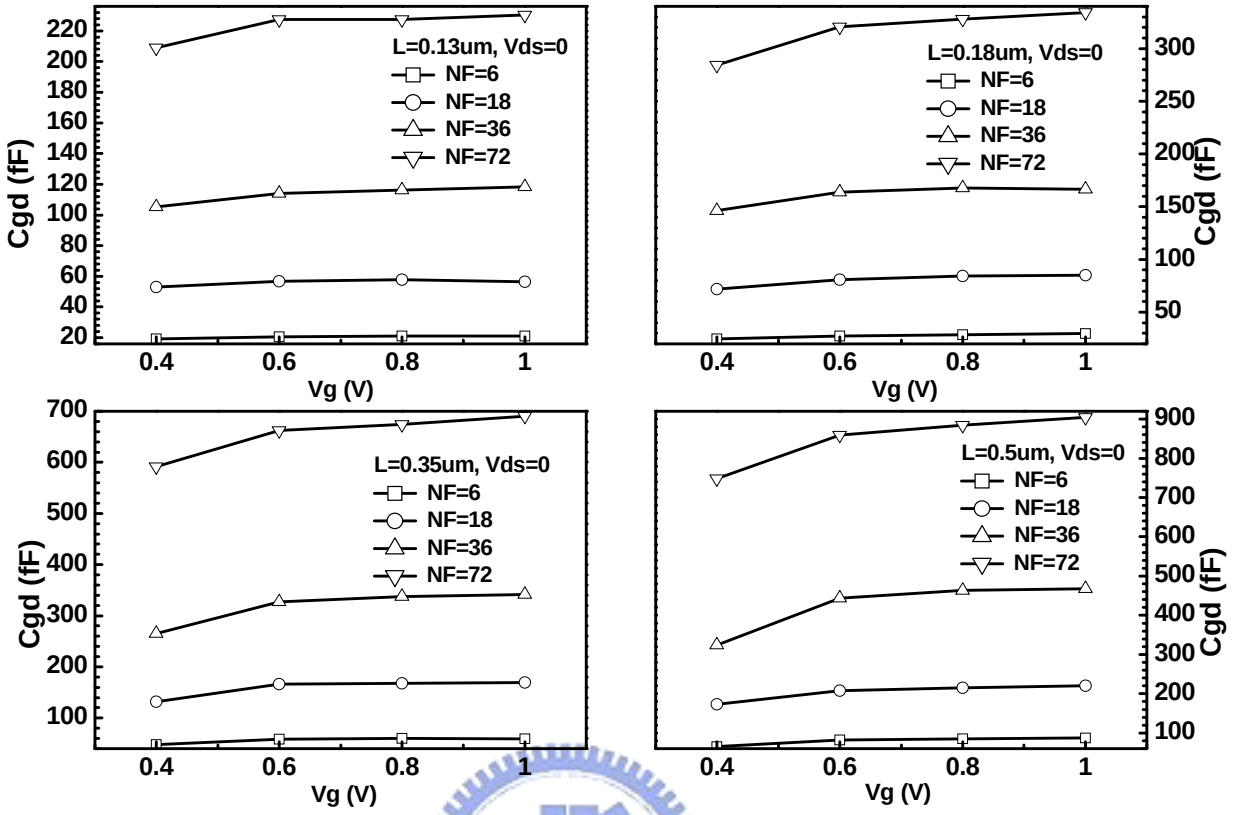


Fig. 3.18 The bias dependence of optimized Cgd at Vds=0V

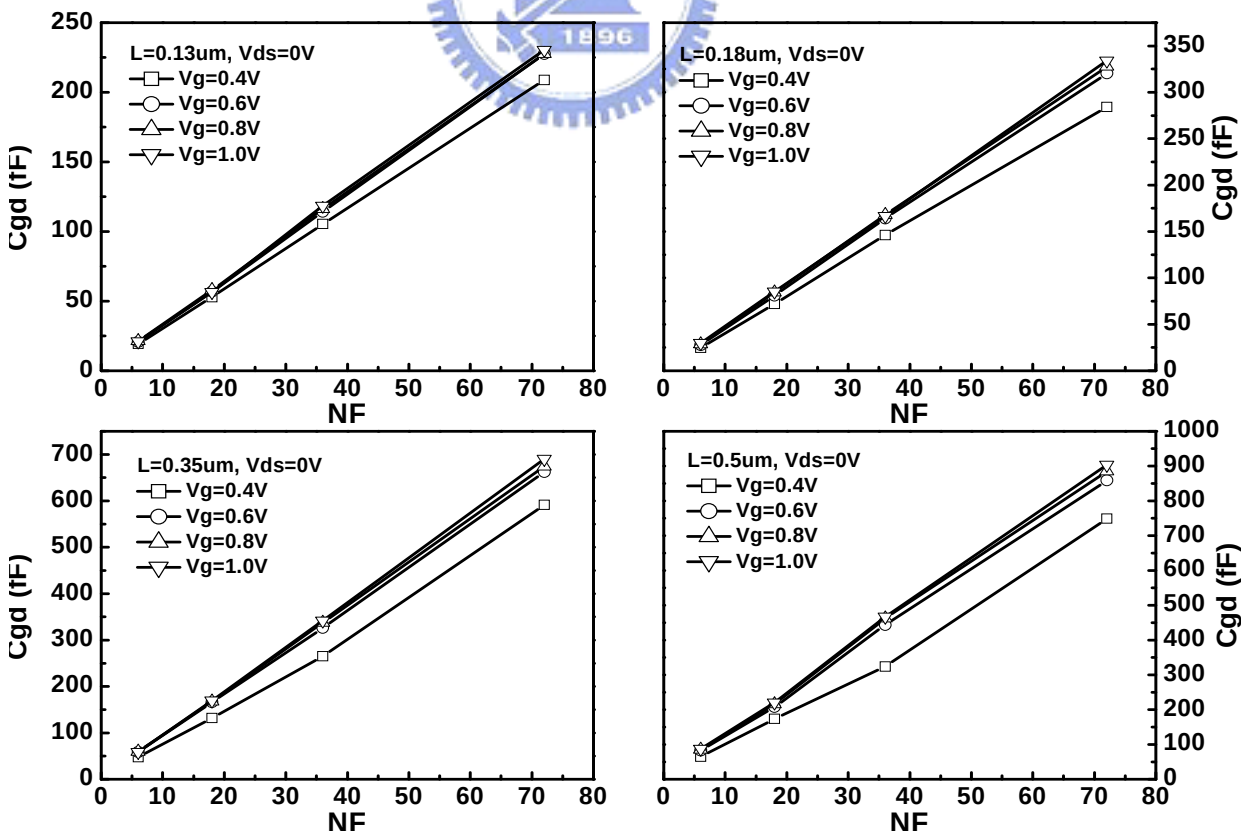


Fig. 3.19 The NF dependence of optimized Cgd at Vds=0V

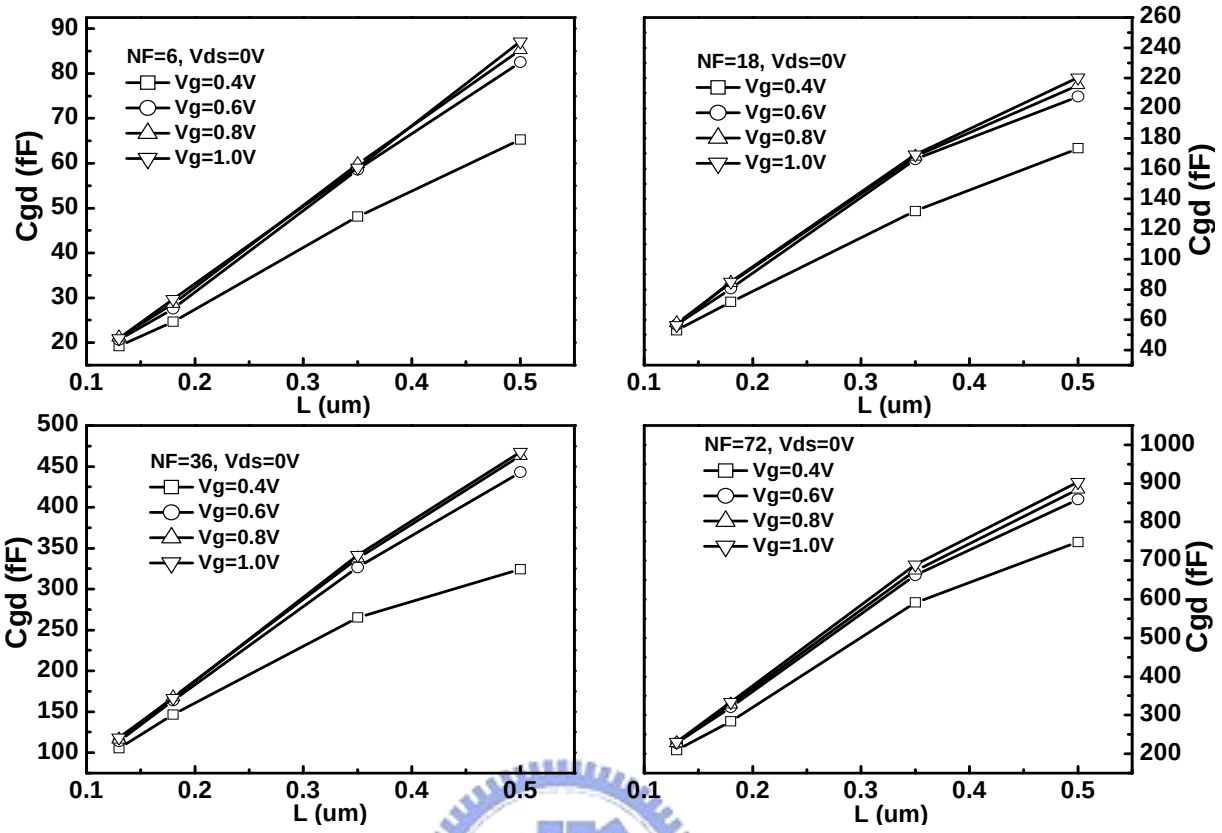


Fig. 3.20 The channel length dependence of optimized Cgd at Vds=0V

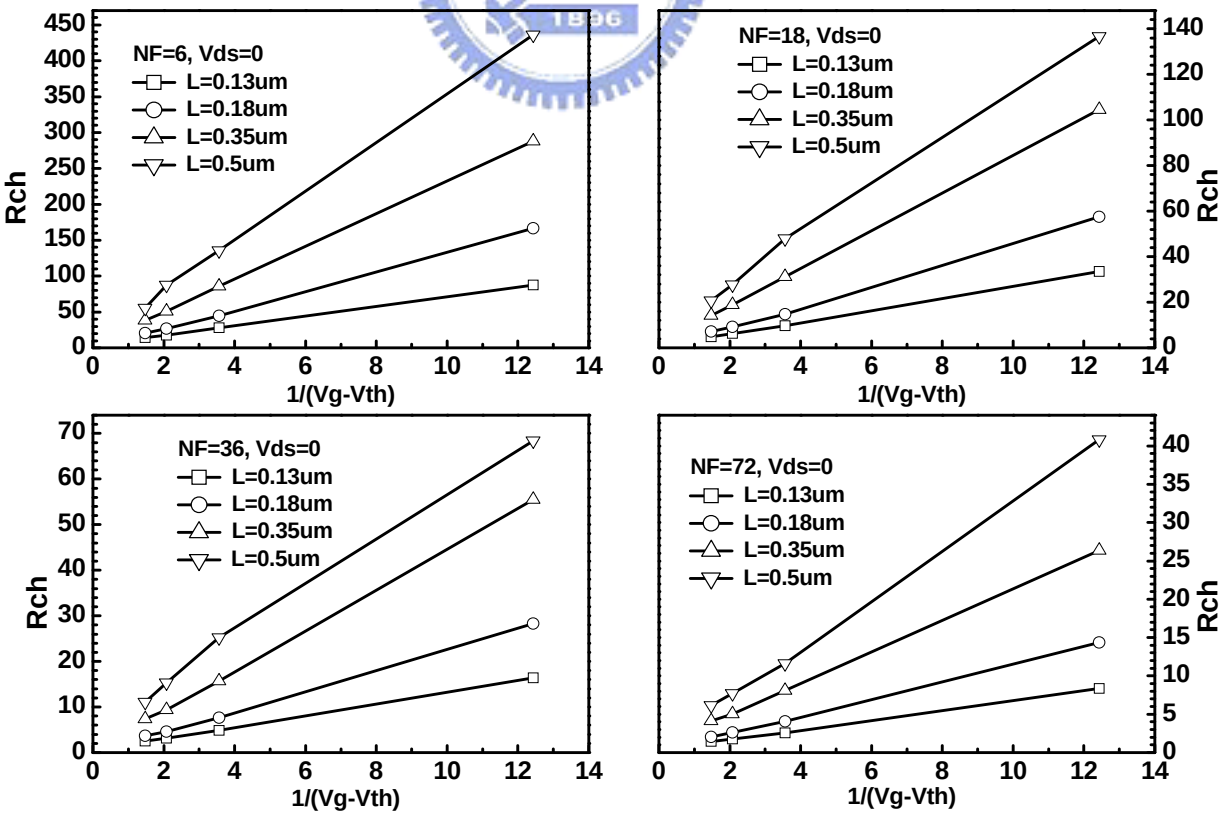


Fig. 3.21 The bias dependence of optimized Rch at Vds=0V

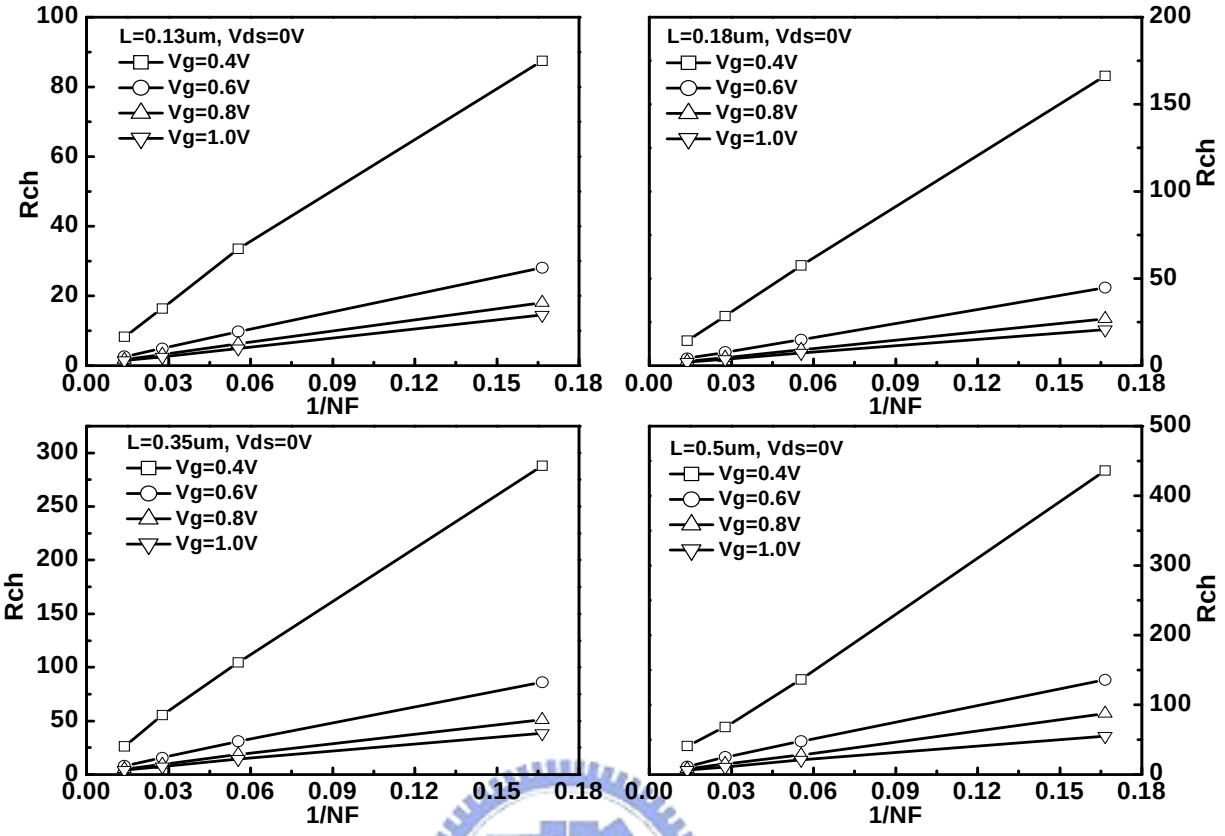


Fig. 3.22 The NF dependence of optimized Rch at Vds=0V

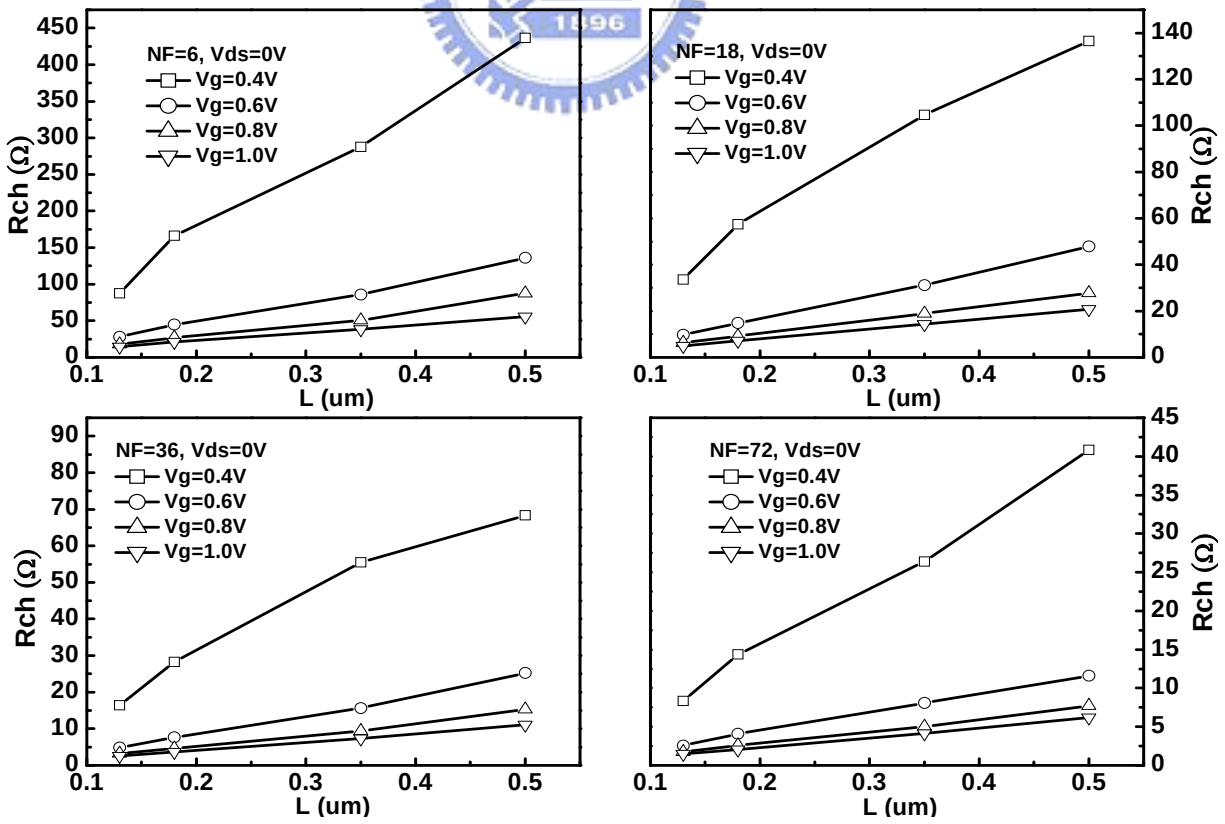


Fig. 3.23 The L dependence of optimized Rch at Vds=0V

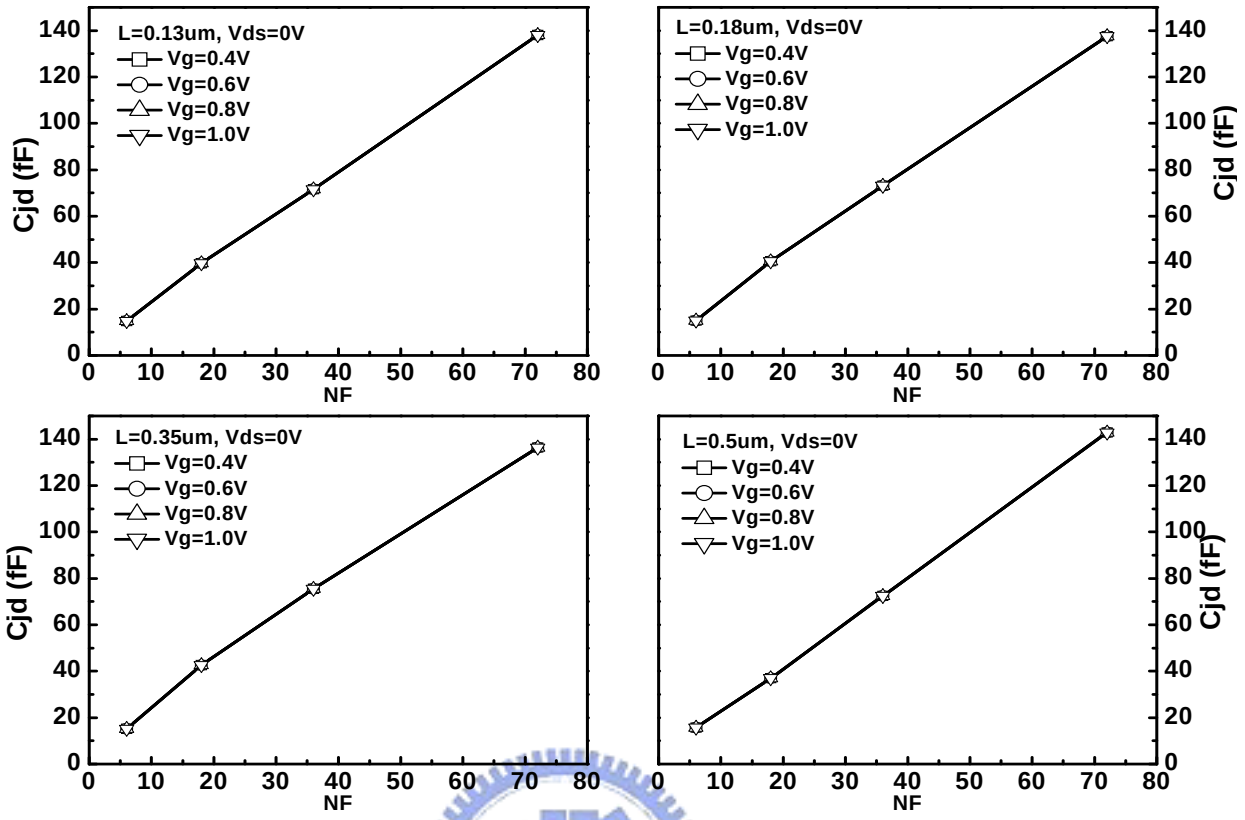


Fig. 3.24 The NF dependence of optimized Cjd at Vds=0V

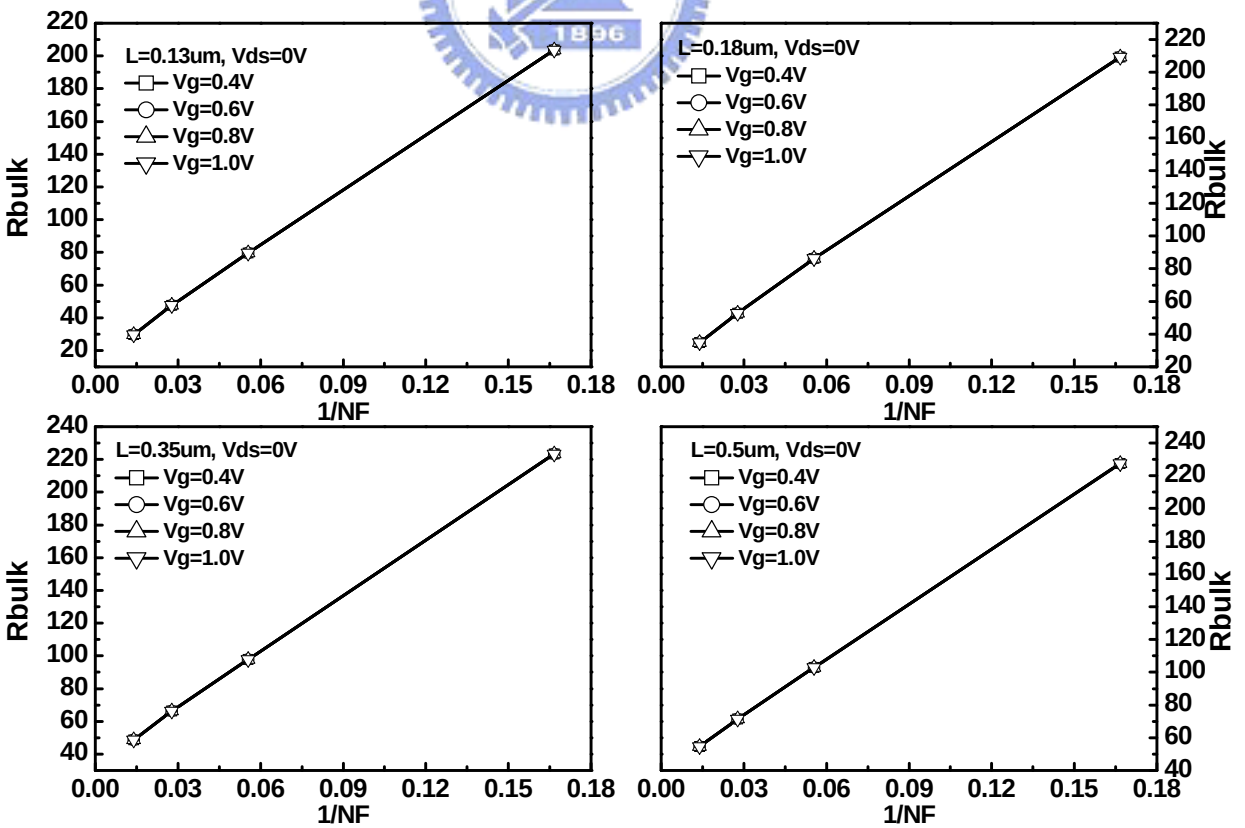


Fig. 3.25The NF dependence of optimized Rbulk at Vds=0V

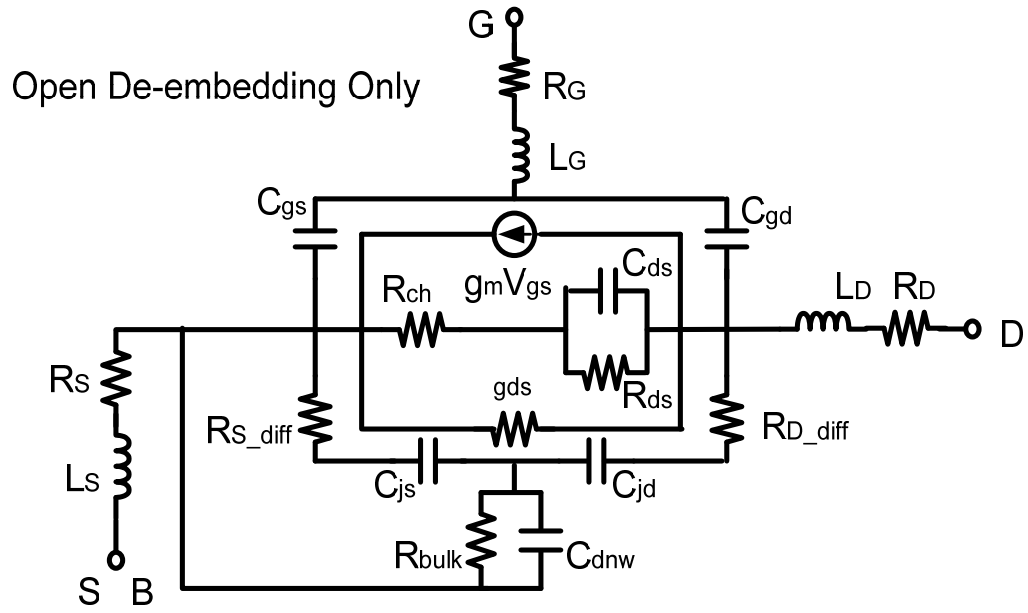


Fig. 3.26 The equivalent circuit of 3T device at V_{gs}=V_{ds}=1V (Open_de)

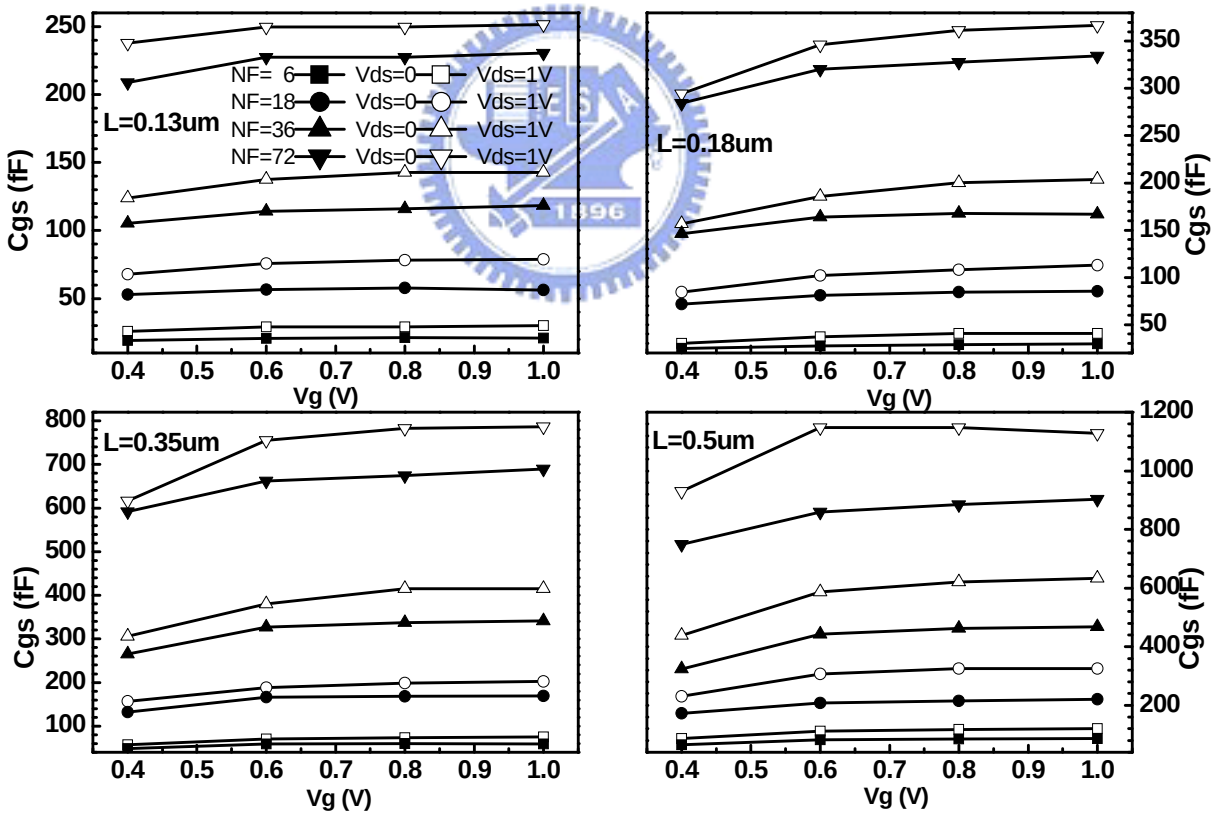


Fig. 3.27 Bias dependence of optimized Cgs at Vds=1V

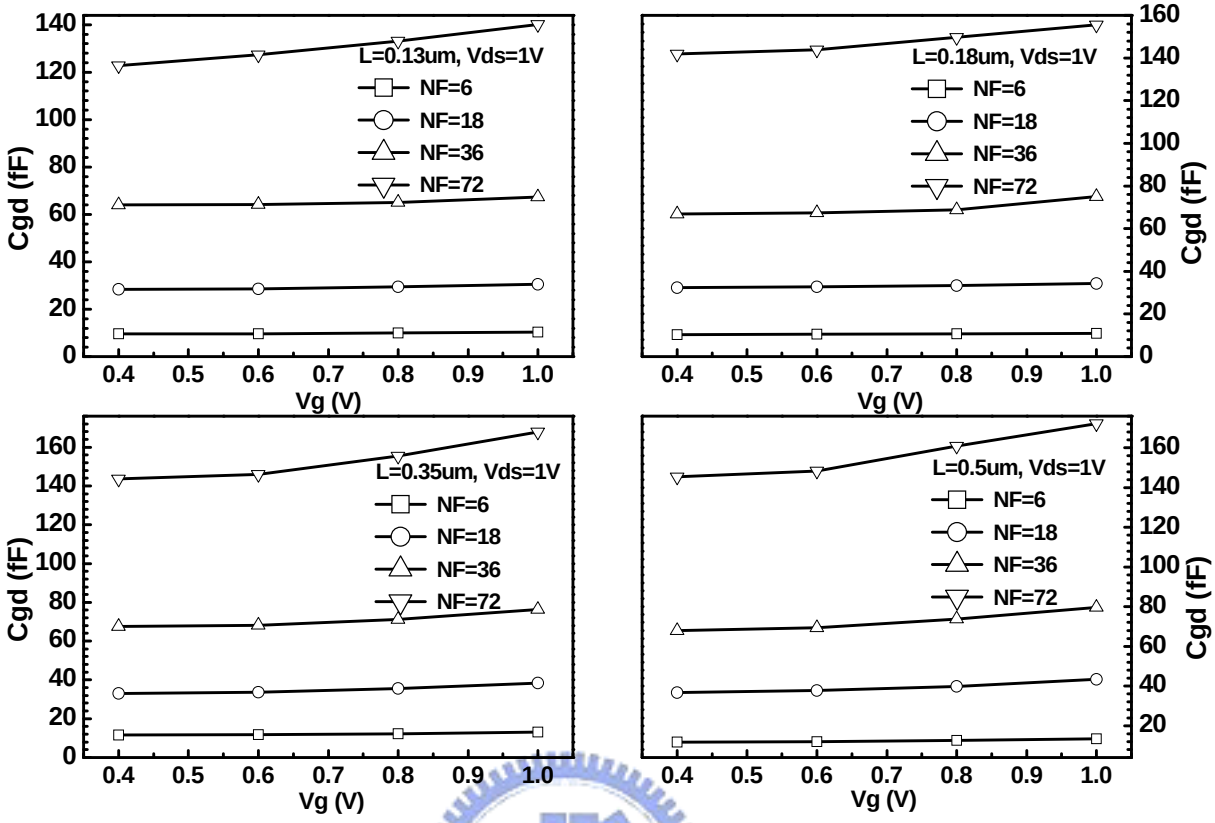


Fig. 3.28 Bias dependence of optimized Cgd at Vds=1V

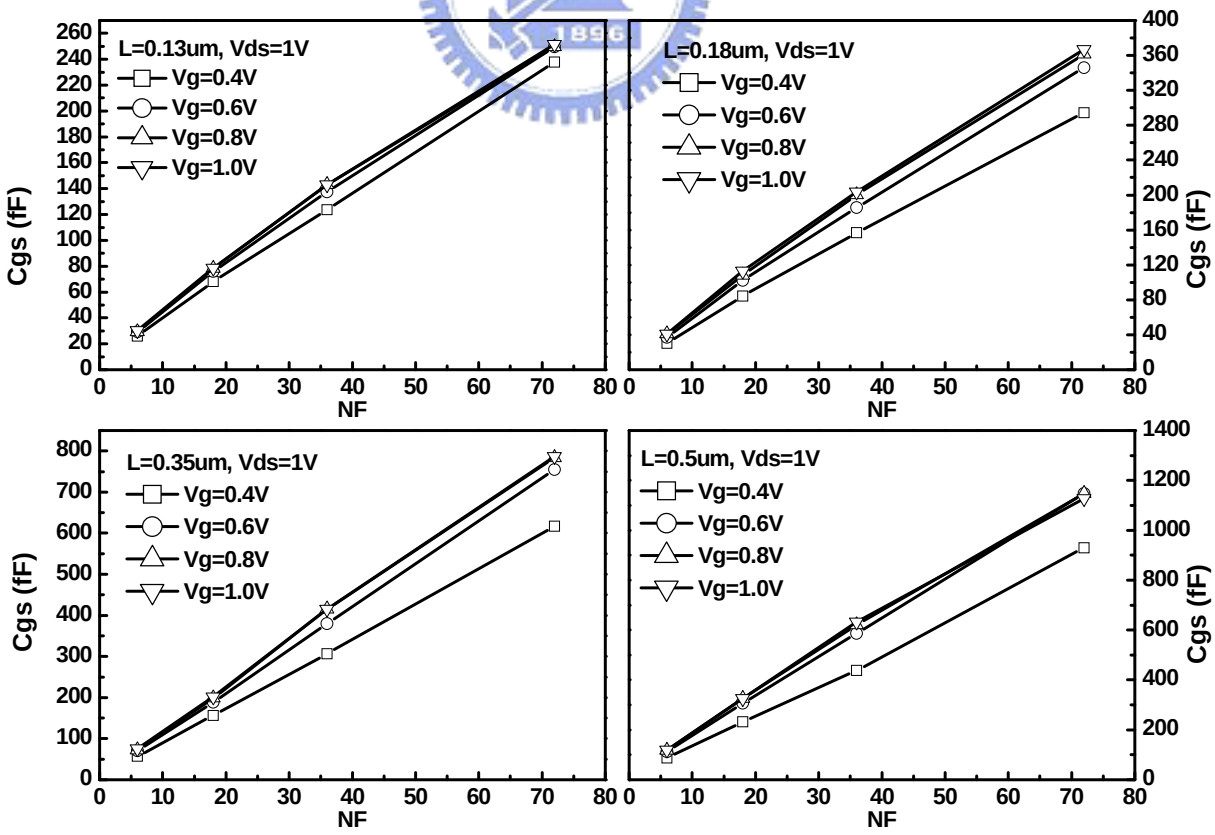


Fig. 3.29 NF dependence of optimized Cgs at Vds=1V

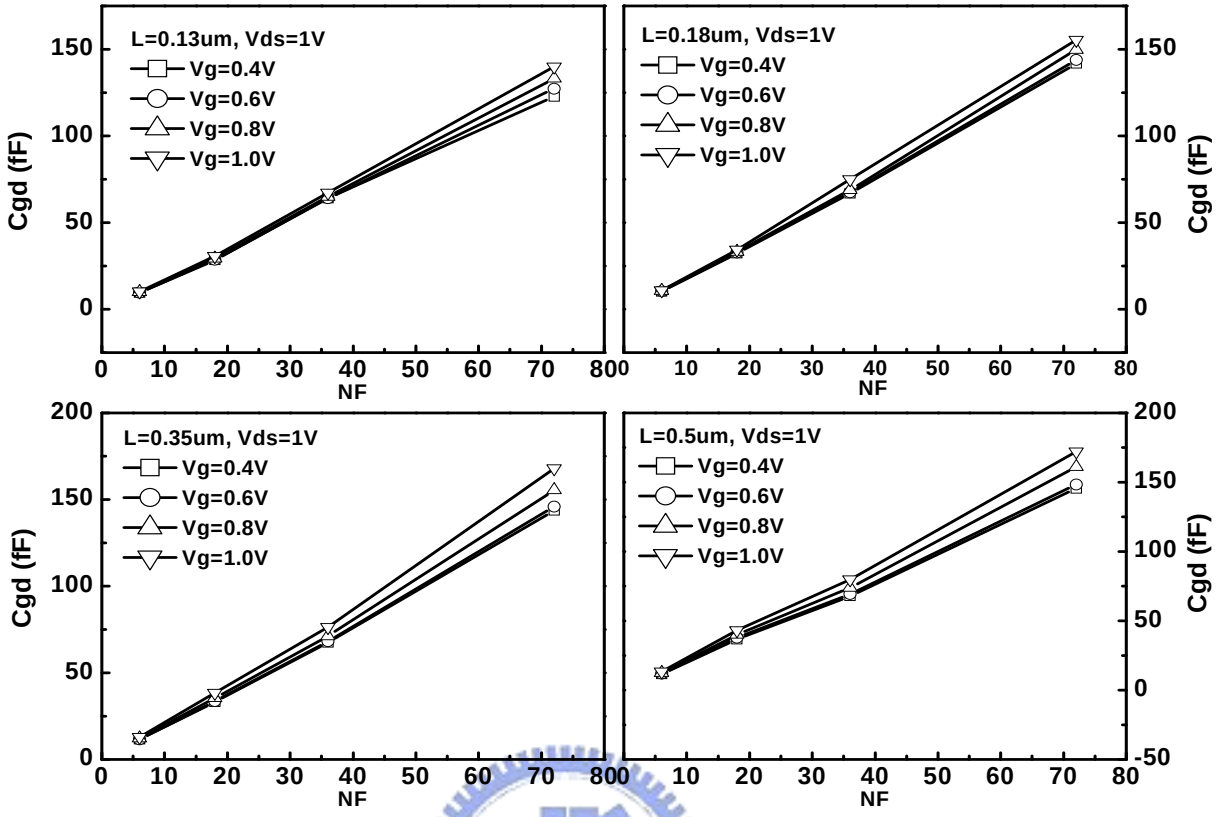


Fig. 3.30 NF dependence of optimized Cgd at Vds=1V

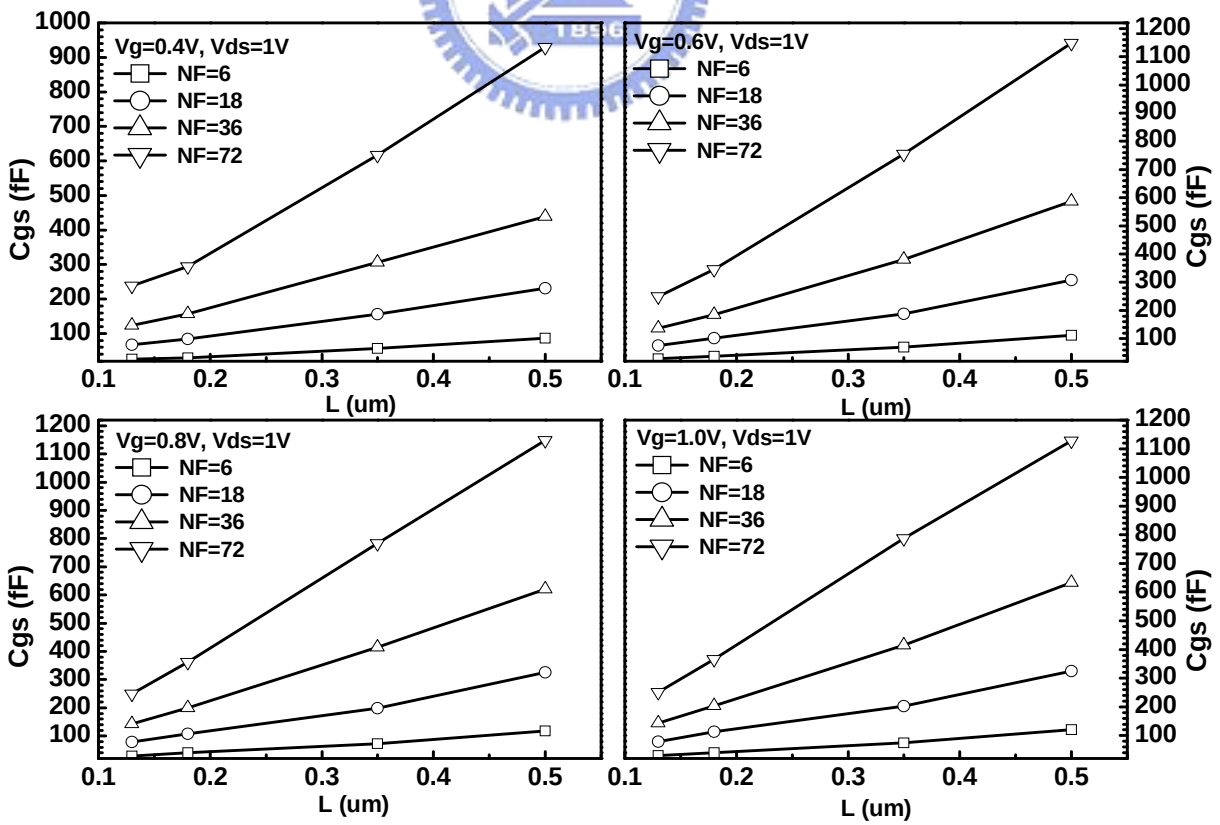


Fig. 3.31 L dependence of optimized Cgs at Vds=1V

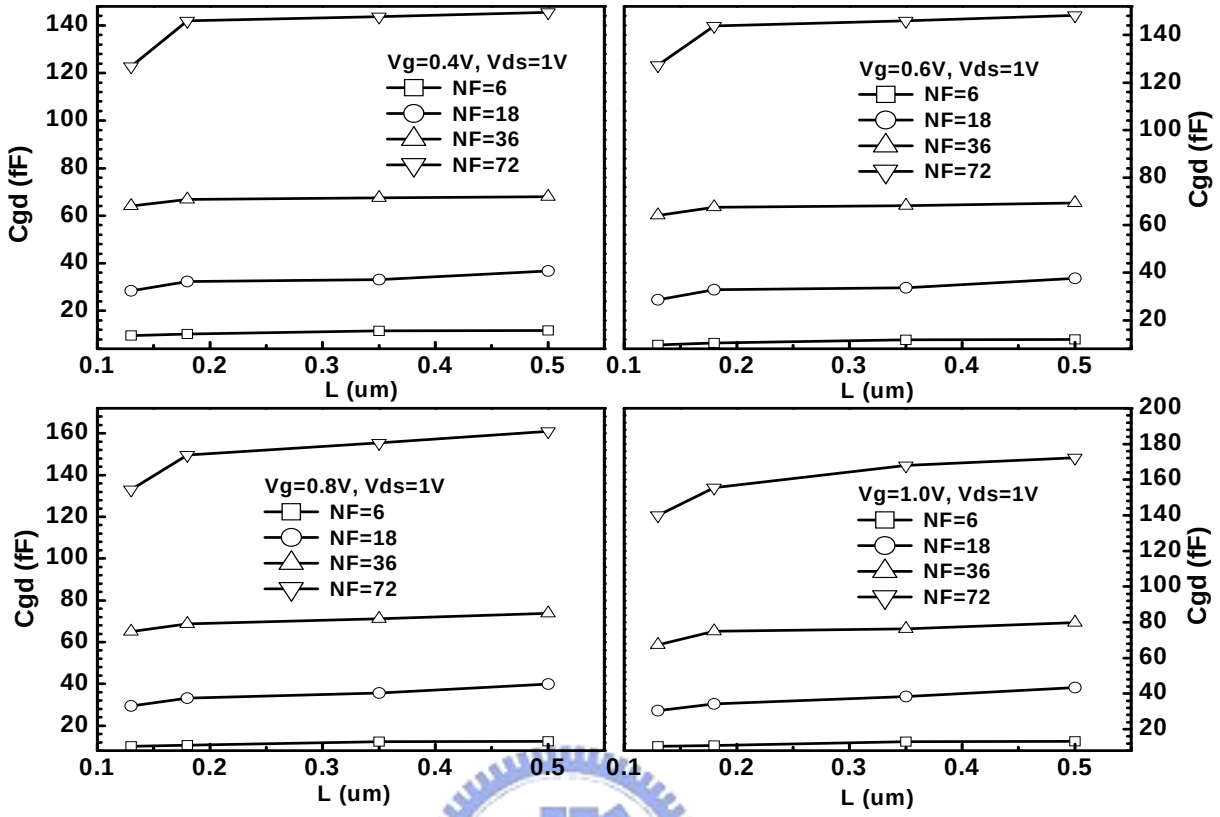


Fig. 3.32 L dependence of extracted Cgd at Vds=1V

Chapter 4

Four-port RF MOSFET Model Parameter Extraction

4.1 De-embedding methods

MOSFETs are designed as common source amplifiers in most RF circuit application, and are implemented by the traditional two-port 3T MOSFET CS configuration that source and body terminals are tied together in metal3 and grounding. In fact, source and body terminals are not always connected together in the application of RFIC design, there are some MOSFETs are designed to operate with the body bias, such as a conventional cascade LNA with source degeneration inductor, the body terminal is always connected to ground, but source terminal is not.

To implement the MOSFET with separate source and body terminals for measurement, source and body terminals will connect to signal pad of the GSG pad, therefore, four terminal of MOSFET can supply the voltage individually for the needs. In this study, the deep N-well (DNW) also connect to ground as the clean-cut reference point to avoid the unanalyzable Z parameter in the four-port devices, and the supplied body bias should be small than the turn on voltage of the junction between the substrate and DNW. One thing is mentioned that test key layout design must conform to the rule of four-port network measurement mechanism, and then the area of the four-port devices will be larger than two-port conventional devices, the full test structure and cross section of four-port devices are plot in Fig. 4.1.

4.1.1 Open and Short de-embedding method

The two port conventional open and short de-embedding method are introduced in session 3.1, basing on the concept of two port de-embedding method, we suppose that the de-embedding method can be apply to the four-port devices, so that, the unique four-port dummy open and short pad will be developed for the purpose. For the open pad, the test structure is the full device structure take off the layer under metal1 (M1), and DNW connecting to ground, the simple 3D illustration is shown in the Fig. 4.2. For the short pad, all signal terminals are connected together in metal3 on the open pad structure, then through the M1 to the ground, remember that M1 grounding is a necessity for the short pad, or it will be as the through pad. However, the simple 3D illustration is shown in the Fig. 4.3.

In this study, the de-embedding method of two-port devices will extend to the four-port networks. According to the conventional de-embedding method of two-port devices, the step can be summarized as:

$$
\begin{aligned}
&S_{mea} \rightarrow Y_{mea}, S_{open} \rightarrow Y_{open}, S_{short} \rightarrow Y_{short} \\
&Y_{mea\_o} = Y_{mea} - Y_{open} \\
&Y_{short\_o} = Y_{short} - Y_{open} \\
&Y_{mea\_o} \rightarrow Z_{mea\_o}, Y_{short\_o} \rightarrow Z_{short\_o} \\
&Z_{dut} = Z_{mea\_o} - Z_{short\_o}
\end{aligned}
\tag{4.1}
$$

Following the above de-embedding step, the intrinsic device Z parameters can be obtained, final Z matrix also can be converted to Y parameters or S parameters for the needs, the parameters in equation (4.1) are all the 4x4 matrix, and the matrix conversion between of S, Y and Z parameters is discussed in session 2.

4.2 Parasitic RL extraction from short pad

The two-port parasitic RL parameters extraction method is discussed in session 3.2. For four-port devices, the equivalent circuit of short pad after open de-embedding can be represented as Fig. 4.4. Similarly, we support that there are only parasitic RL parameters originate from metal interconnections between the terminal of DUT and the pad, by analysis the Z parameters of the equivalent circuit of short pad after open de-embedding, the parameters extraction for four-port devices can be described as

$$\begin{aligned}
R_{g,ext} &= \mathrm{Re}\left(Z_{11}^{short_o} - Z_{12}^{short_o}\right) & L_{g,ext} &= \mathrm{Im}\left(Z_{11}^{short_o} - Z_{12}^{short_o}\right)/\omega \\
R_{s,ext} &= \mathrm{Re}\left(Z_{22}^{short_o} - Z_{12}^{short_o}\right) & L_{s,ext} &= \mathrm{Im}\left(Z_{22}^{short_o} - Z_{12}^{short_o}\right)/\omega \\
R_{d,ext} &= \mathrm{Re}\left(Z_{33}^{short_o} - Z_{12}^{short_o}\right) & L_{d,ext} &= \mathrm{Im}\left(Z_{33}^{short_o} - Z_{12}^{short_o}\right)/\omega \\
R_{b,ext} &= \mathrm{Re}\left(Z_{44}^{short_o} - Z_{12}^{short_o}\right) & L_{b,ext} &= \mathrm{Im}\left(Z_{44}^{short_o} - Z_{12}^{short_o}\right)/\omega \\
R_{sb,ext} &= \mathrm{Re}\left(Z_{12}^{short_o}\right) & L_{sb,ext} &= \mathrm{Im}\left(Z_{12}^{short_o}\right)/\omega
\end{aligned} \quad (4.2)$$

, where $Z_{12}^{short\_o} \cong Z_{21}^{short\_o} \cong Z_{ij,i\neq j}^{short\_o}$

In equation (4.2), the subscript value represents the port number for the measurement respectively. In this study, port1, 2, 3, and 4 represent that gate, source, drain, and body respectively. The result shows that the extracted parasitic RL is not the frequency independent parameters, it may be has a high frequency term without considered in the equivalent circuit, and common part of the resistance is smaller than the resistances come from metal connection between metal3 and metal8, the parasitic RL parameters are extracted at low frequency.

4.3 Extraction and analysis of parameters in linear region

In this section, we will discuss that parameters extraction of four-port devices operating in linear region. For four-port devices, when gate voltage is smaller than the threshold voltage and Vds=0V, the equivalent circuit of four-port devices with parasitic

RL parameters and substrate network components can be shown in Fig. 4.5. The differentiation between two-port and four-port devices is the substrate networks that connection of the body and DNW terminal is not tied together in four-port devices.

4.3.1 Extraction of parameters in linear region

The capacitances of the equivalent circuit are extracted from the intrinsic Y parameters at low frequency conventionally, the circuit is very simple, we assume that the components between gate and the other terminals can be considered as purely capacitances, the terminals resistance is finite in the frequency of our consideration, and it will be smaller than the impedance of the captaincies, according to the assumption, Rs and Rd can be neglected at low frequency to simplified the extraction equation.

For the four-port MOSFET, Ward-Dutton description leads to a total of 16 transcapacitances. This set of 16 elements can be organized as follows in a 4x4 matrix.

$$C = \begin{bmatrix} C_{gg} & C_{gs} & C_{gd} & C_{gb} \\ C_{sg} & C_{ss} & C_{sd} & C_{sb} \\ C_{dg} & C_{ds} & C_{dd} & C_{db} \\ C_{bg} & C_{bs} & C_{bd} & C_{bb} \end{bmatrix} \tag{4.3}$$

In this bias condition, there is not current flow through the devices, so that terminal current does not contain any conductive current component. The elements in each column and low must sum to zero owing to the constraints imposed by charge conservation. As gate capacitances for example, the gate capacitances relationship cab be represented as

$$C_{gg} = C_{gs} + C_{gd} + C_{gb} \tag{4.4}$$

By performing the Y parameter analysis of the equivalent circuit, the Y11

component cab be derived as

$$Y_{11}^{dut} = j\omega C_{gs} + j\omega C_{gd} + \frac{\omega^2 R_{bulk} C_{gb}^2 + j\omega C_{gb}}{1 + \omega^2 R_{bulk}^2 C_{gb}^2} \tag{4.5}$$

Following the Y parameter analysis, the components of Yxy(x=1~4, y=1~4) also can be derived, under the assumption $\omega^2 R_{bulk}^2 C_{gb}^2 << 1$, the capacitances extraction equation can be simplified as bellow:

$$\begin{aligned}
C_{gg} &= \mathrm{Im}\left(Y_{11}^{dut}\right) \\
C_{gs} &= -\mathrm{Im}\left(Y_{12}^{dut}\right)/\omega = -\mathrm{Im}\left(Y_{21}^{dut}\right)/\omega \\
C_{gd} &= -\mathrm{Im}\left(Y_{13}^{dut}\right)/\omega = -\mathrm{Im}\left(Y_{31}^{dut}\right)/\omega \\
C_{gb} &= -\mathrm{Im}\left(Y_{14}^{dut}\right)/\omega = -\mathrm{Im}\left(Y_{41}^{dut}\right)/\omega \\
C_{js} &= -\mathrm{Im}\left(Y_{24}^{dut}\right)/\omega = -\mathrm{Im}\left(Y_{42}^{dut}\right)/\omega \\
C_{jd} &= -\mathrm{Im}\left(Y_{34}^{dut}\right)/\omega = -\mathrm{Im}\left(Y_{43}^{dut}\right)/\omega
\end{aligned} \tag{4.6}$$

The proposed de-embedding method is simpler than that of two-port 4T devices, and the capacitances can be extracted form the intrinsic Y matrix at low frequency directly, especially source junction capacitance, it is hardly to extract Cjs in a traditional two-port 3T CS MOSFET because source and body connected together.

The substrate resistance extraction tends to use the method discussed in the two-port CS configuration devices, the 2x2 matrix will be obtained by using the port reduction method that discussed in session 2.2.3, the remaining parameters R_{s_diff}, R_{d_diff}, and C_{dnw} also can be extraction by the reduced 2x2 Y matrix that bias at Vg=Vd=Vs=Vb=0V in other words.

Similarly, when MOSFETs operate at the strong inversion region and at Vd=Vs=Vb=0V, the equivalent circuit is plotted in Fig. 4.6, extraction of capacitance at Vg=0V (4.6) to be suitable for use at this condition, and the channel resistance will be extracted in the 2x2 matrix that reduce from the 4x4 matrix.

4.3.2 Analysis of parameters in linear region

The extracted capacitances are plotted as a function frequency in Fig.4.7 and Fig. 4.8, the extracted capacitances Cgg, Cgs and Cgs have weak frequency dependence at low frequency, and will be increase with the frequency increasing, there are some inductances without de-embedding completely to cause the behavior at high frequency. Conversely, the extracted capacitances Cgb, Cjs, and Cjd will be decease as the frequency increase, Cgb is extracted from the imaginary part of the intrinsic Y parameters in equation (4.6), and there is a frequency component in the denominator with the RC component, In other words, the capacitances Cgb, Cjs, and Cjd will be decrease as frequency increasing because of the existence of Rblk in equivalent circuit.

The geometry dependence of the optimizing capacitances are shown in Fig. 4.9 and Fig. 4.10, it shows that the capacitances are well proportioned to the NF. As gate voltage increases, the channel charges build up to increase the intrinsic component of the extracted capacitances and Cgs is larger than the Cgd at Vgs=1.2V, because there are one source junction than the drain, the extrinsic capacitances with gate bias dependency of source is more than drain.

When the channel charge can be supplied by source/drain to channel rather than body in the strong inversion region, the whole Cgb capacitance which through the active channel area to source/drain region is very small and can be neglected, the value of the Cgb is close to zero at Vg=1.2V. The extracted junction capacitances also show that the value of Cjs is larger than that of Cjd, because there is one source junction than the drain and gate bias independent almost.

The geometry dependence of the optimizing resistances is shown in Fig. 4.11, it is known that R_{g_poly} is gate bias insensitively and dominate the total resistance in

shorter devices, it also show that R_G is well proportional to reciprocal function of NF.

4.4 Extraction and analysis of parameters in saturation region

When MOSFET operates at saturation region and Vs=Vb=0V, the equivalent circuit can be extend to four-port devices base on ones of the two-port 3T devices, the equivalent circuit of four-port devices with parasitic RL parameters and substrate network components can be shown in Fig.4.12.

4.4.1 Extraction of parameters in saturation region

The capacitance extraction for four-port devices at Vds=0V is discussed chapter 4.3, by performing the Y parameter analysis of the equivalent circuit, the capacitance extraction equation at Vds=1.2V also can be written as:

$$\begin{aligned} C_{gg} &= \mathrm{Im}\left(Y_{11}^{dut}\right) \\ C_{gs} &= -\mathrm{Im}\left(Y_{12}^{dut}\right)/\omega \\ C_{gd} &= -\mathrm{Im}\left(Y_{13}^{dut}\right)/\omega \\ C_{gb} &= -\mathrm{Im}\left(Y_{14}^{dut}\right)/\omega \end{aligned} \quad ; \quad \begin{aligned} C_{js} &= -\mathrm{Im}\left(Y_{42}^{dut}\right)/\omega \\ C_{jd} &= -\mathrm{Im}\left(Y_{43}^{dut}\right)/\omega \end{aligned} \tag{4.7}$$

$$g_m = \frac{\partial I_d}{\partial V_{gs}} \cong \mathrm{Re}\left(\mathrm{Y_{dg}}\right) \ , \quad g_{\mathrm{ds}} = \frac{\partial I_d}{\partial V_{\mathrm{ds}}} \cong \mathrm{Re}\left(\mathrm{Y_{dd}}\right) \tag{4.8}$$

Note that the Yij is not equal to Yji in equation (4.7) because of the existent of current gain and asymmetry in channel.

4.4.2 Analysis of parameters in saturation region

The extracted capacitances are plotted as a function frequency in Fig.4.13 and

Fig. 4.14, the extracted capacitances Cgg, Cgs and Cgs is weak frequency dependet at low frequency, and will be increase with the frequency increasing. There are some inductances without de-embedding completely to cause the behavior at high frequency. Conversely, the extracted capacitances Cgb, Cjs, and Cjd will be decease as the frequency increase, and the extracted Cjs, and Cjd is almost gate bias independence.

The geometry dependence of the optimizing capacitances are shown in Fig. 4.15 and Fig. 4.16, it shows that the capacitances are well proportioned to the NF, and the gate capacitances relationship between of linear and saturation region is described in two-port devices.

For the junction capacitances, according to the equivalent circuit of two-port devices, $Im(Y_{22})$ combine with Cjd, Cgd, Cds, and Cdnw, so it is hardly to extract the Cjd in two-port devices that operate at saturation region. Contrary, it is easy to extract junction capacitances in four-port devices, and the extracted result shows that the Cjd capacitances at Vds=1.2V is smaller than one at Vds=0V, because that the drain-body junction with the reverse bias operation, and Cjs is a gate bias independent parameters.

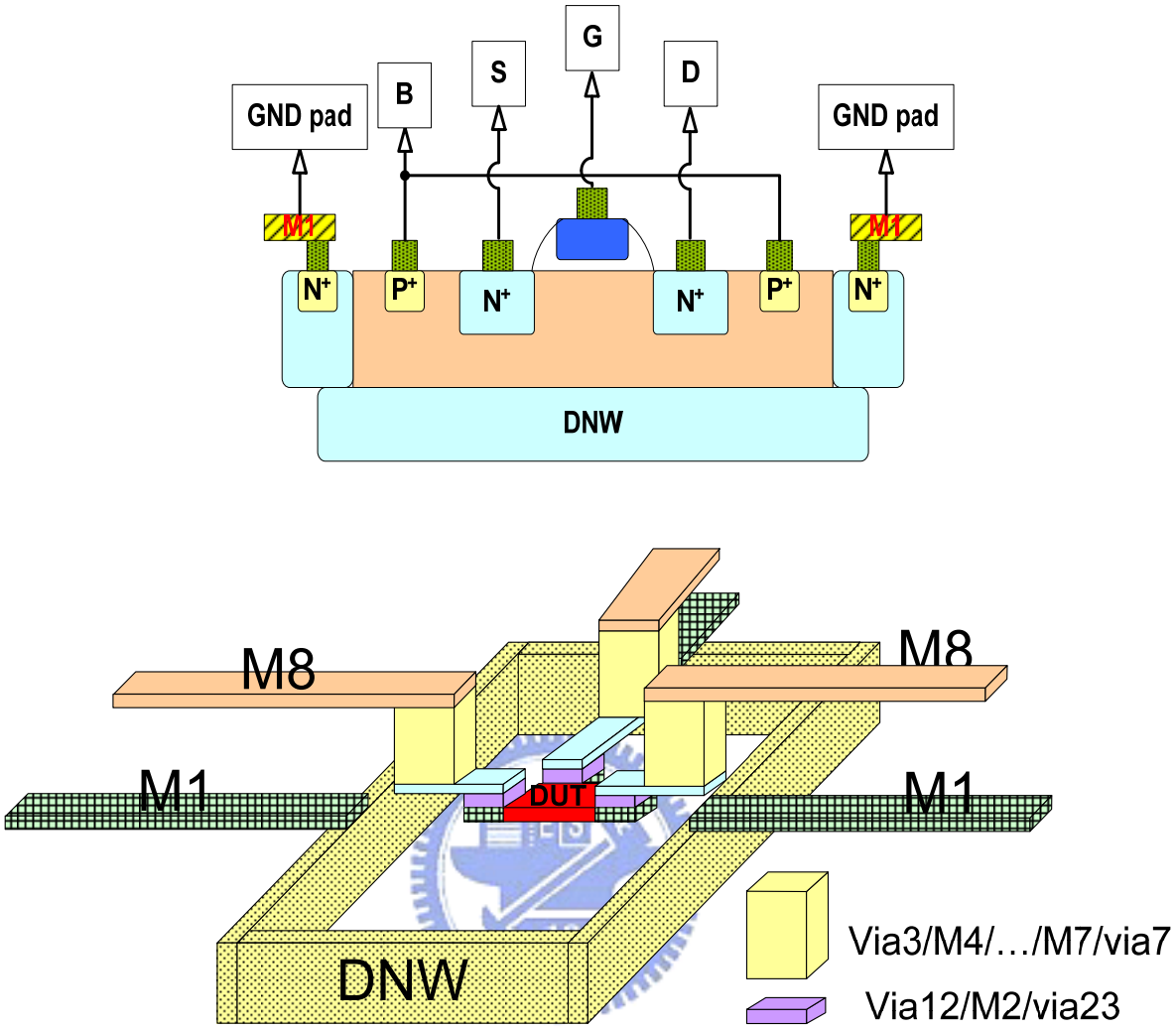


Fig. 4.1 The cross section and structure of four-port MOSFETs

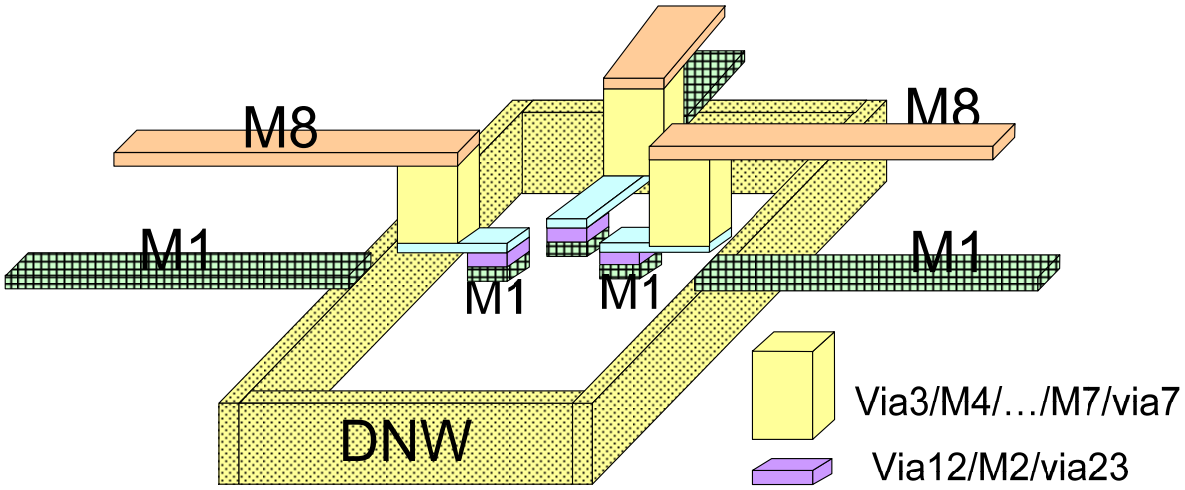


Fig. 4.2 Four-port dummy open structure (M1)

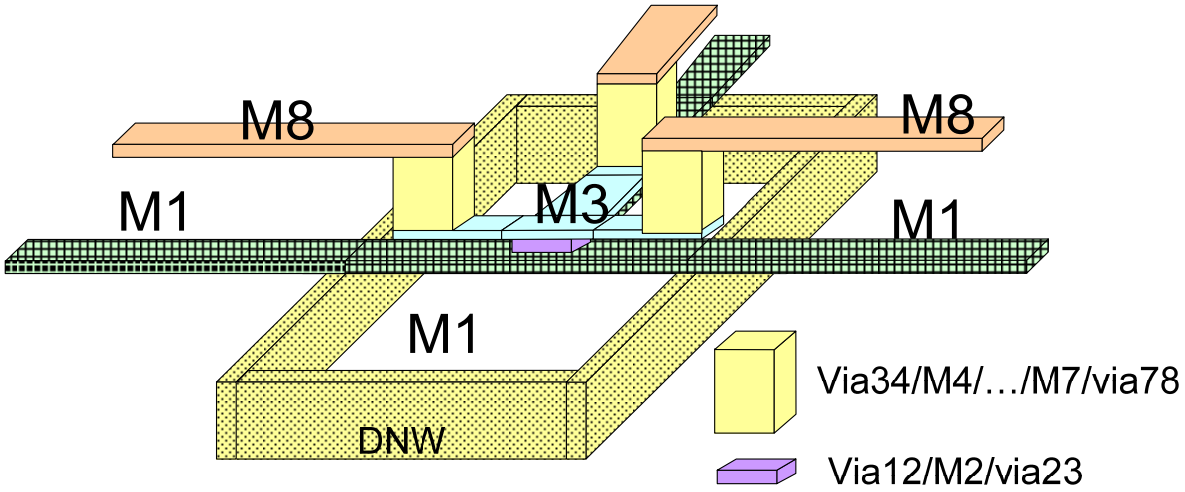


Fig. 4.3 Four-port dummy short structure (M3)

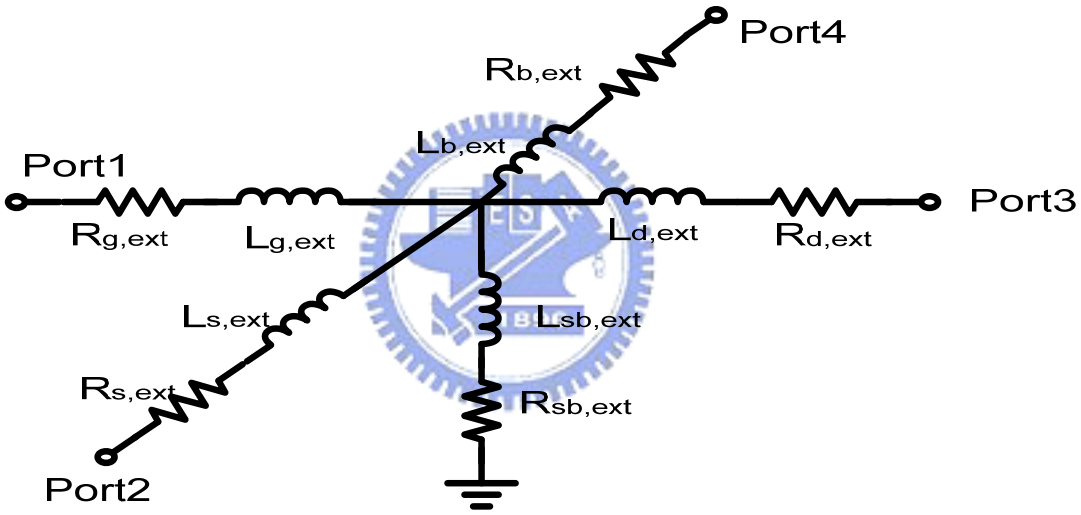


Fig. 4.4 The equivalent circuit of four-port short pad after open de-embedding

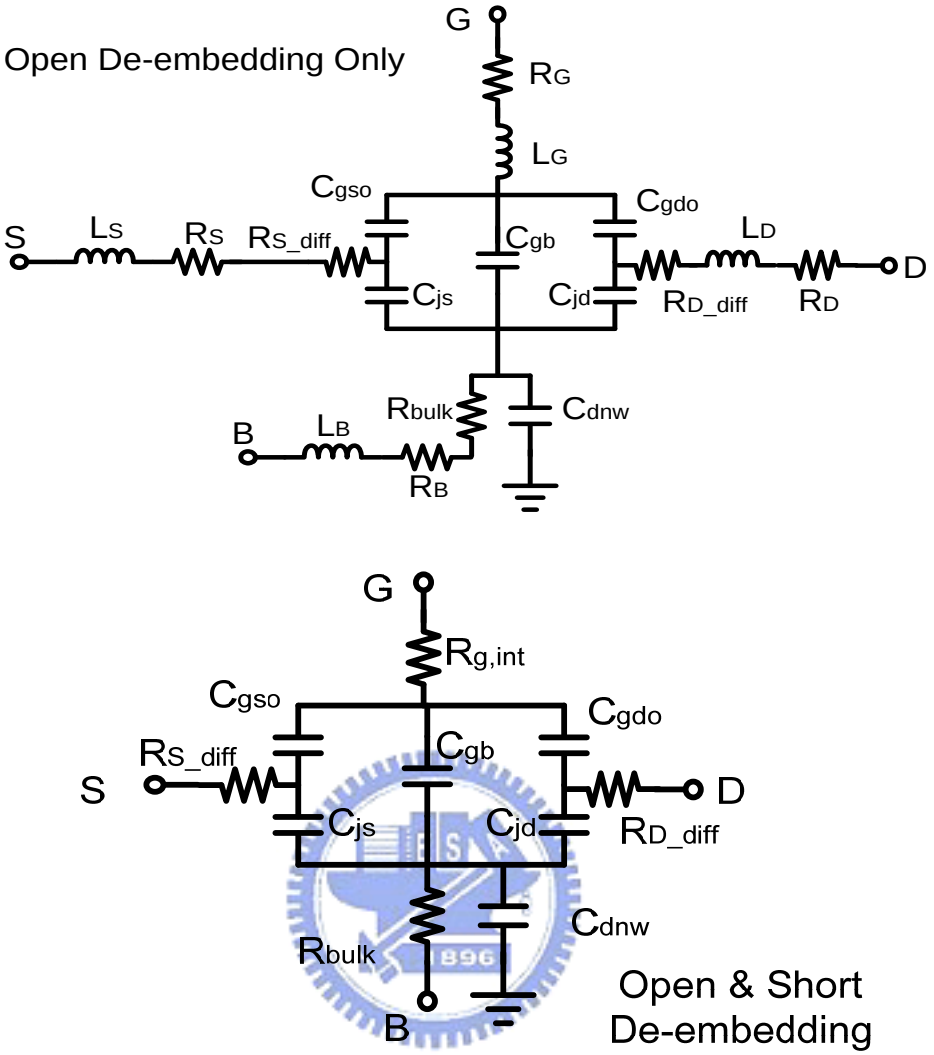


Fig. 4.5 The equivalent circuit of four-port devices at V_{gs}=V_{ds}=0V

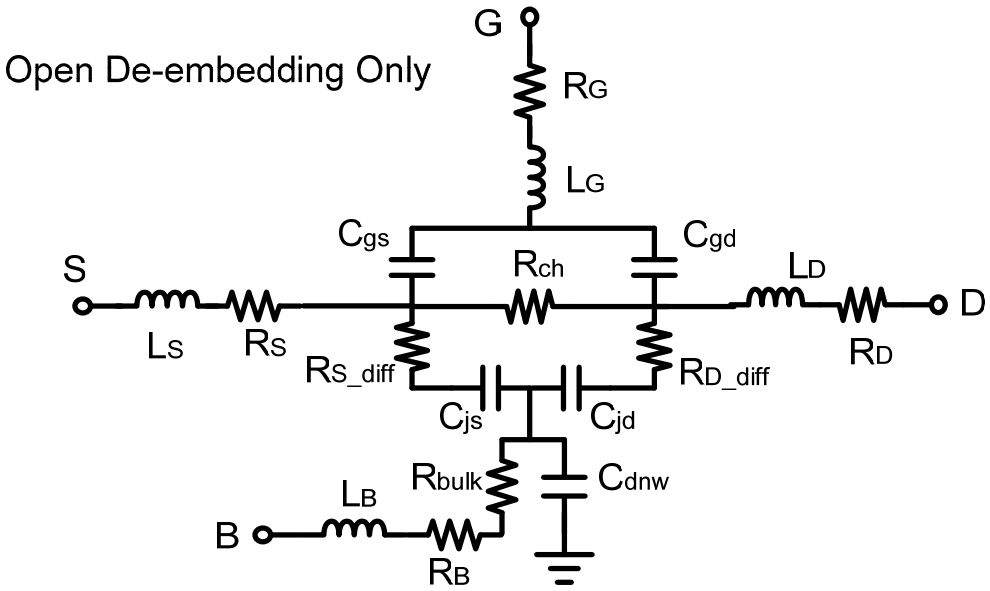


Fig. 4.6 The equivalent circuit of 4-port device at V_{gs}=1.2V, V_{ds}=0V (Open_de)

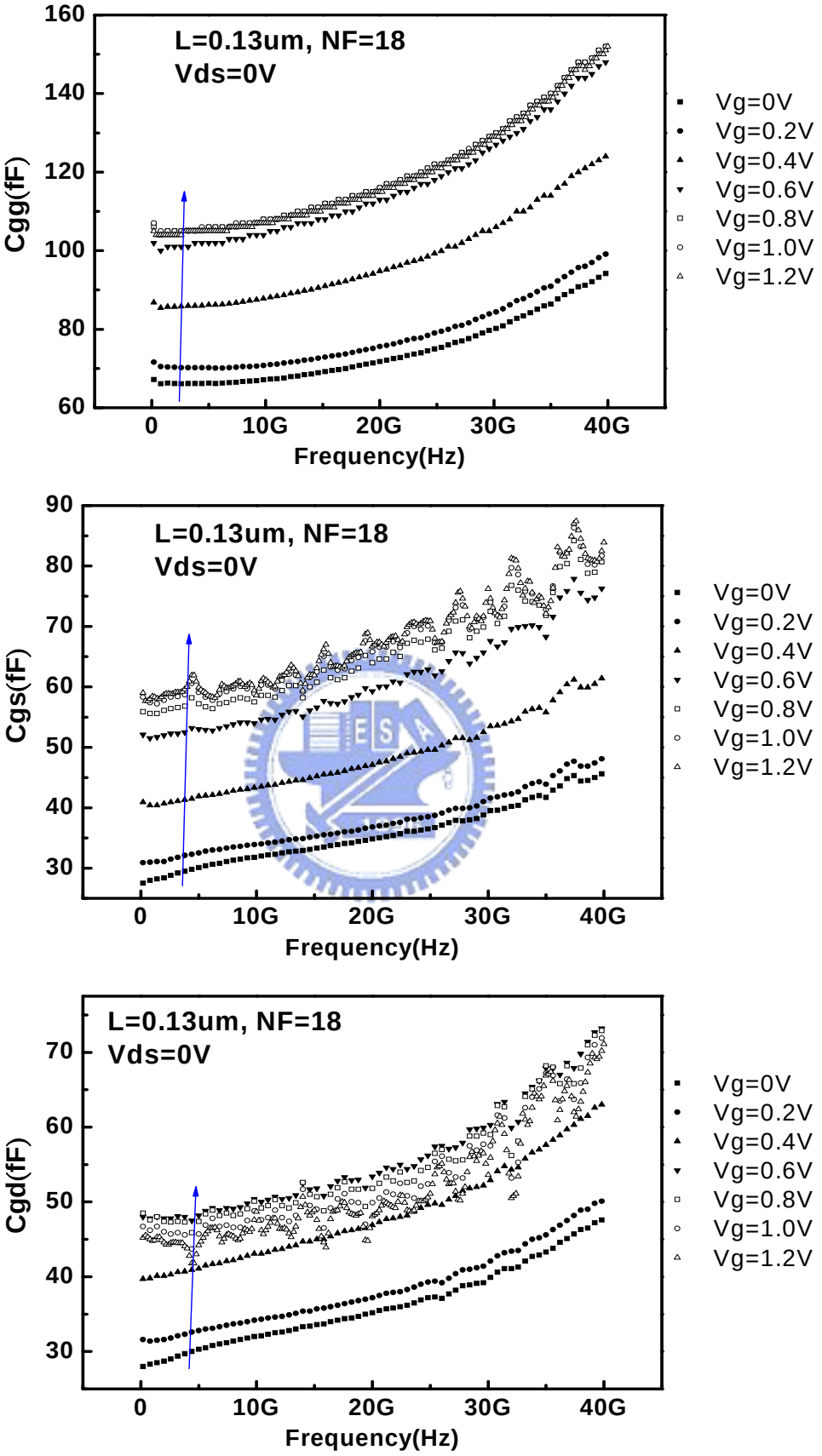


Fig. 4.7 The extracted C_{gg}, C_{gs} , C_{gd} capacitance verse frequency at Vds=0V

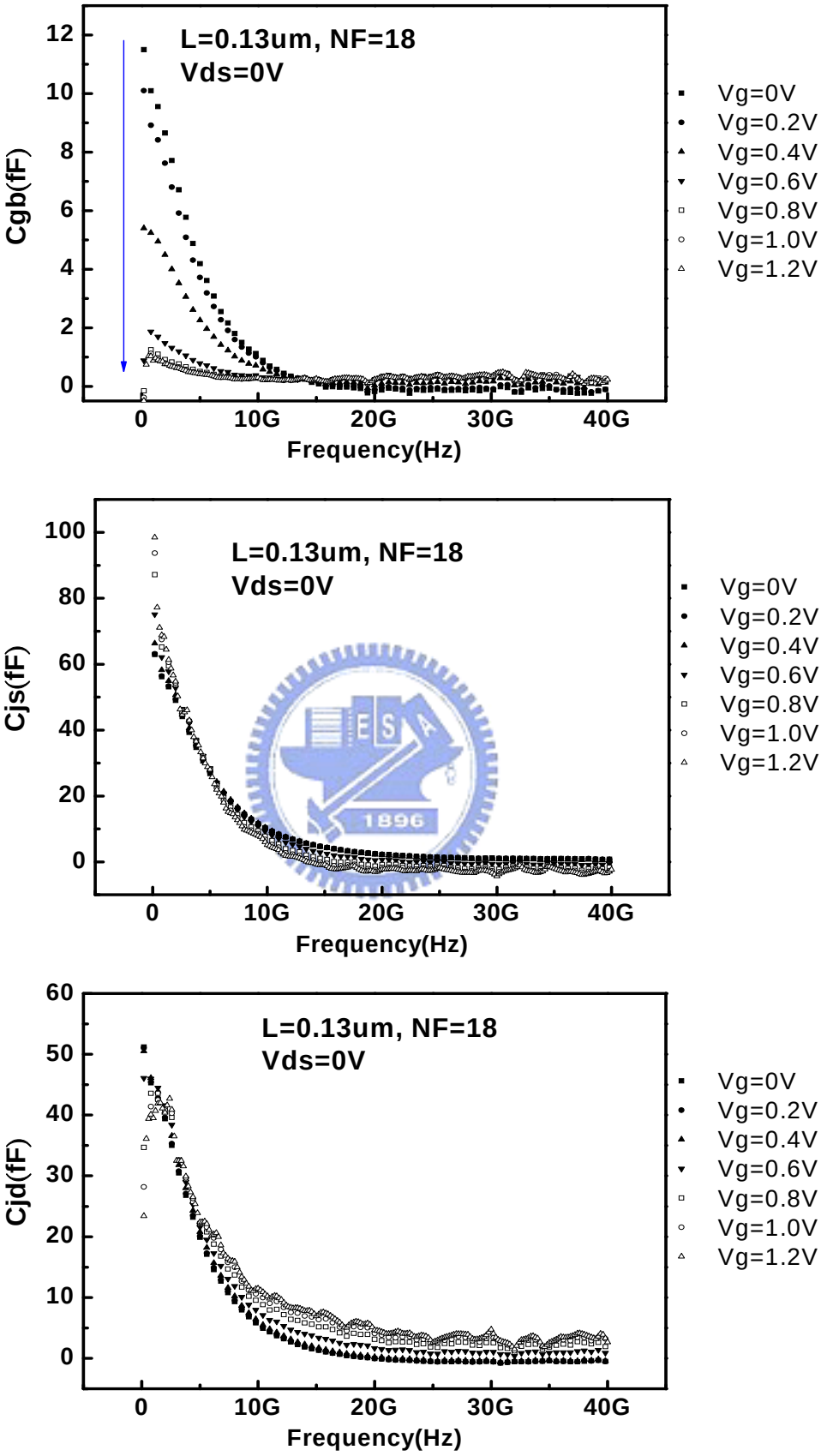


Fig. 4.8 The extracted $C_{gb,}$ C_{js}, C_{jd} capacitance verse frequency at Vds=0V

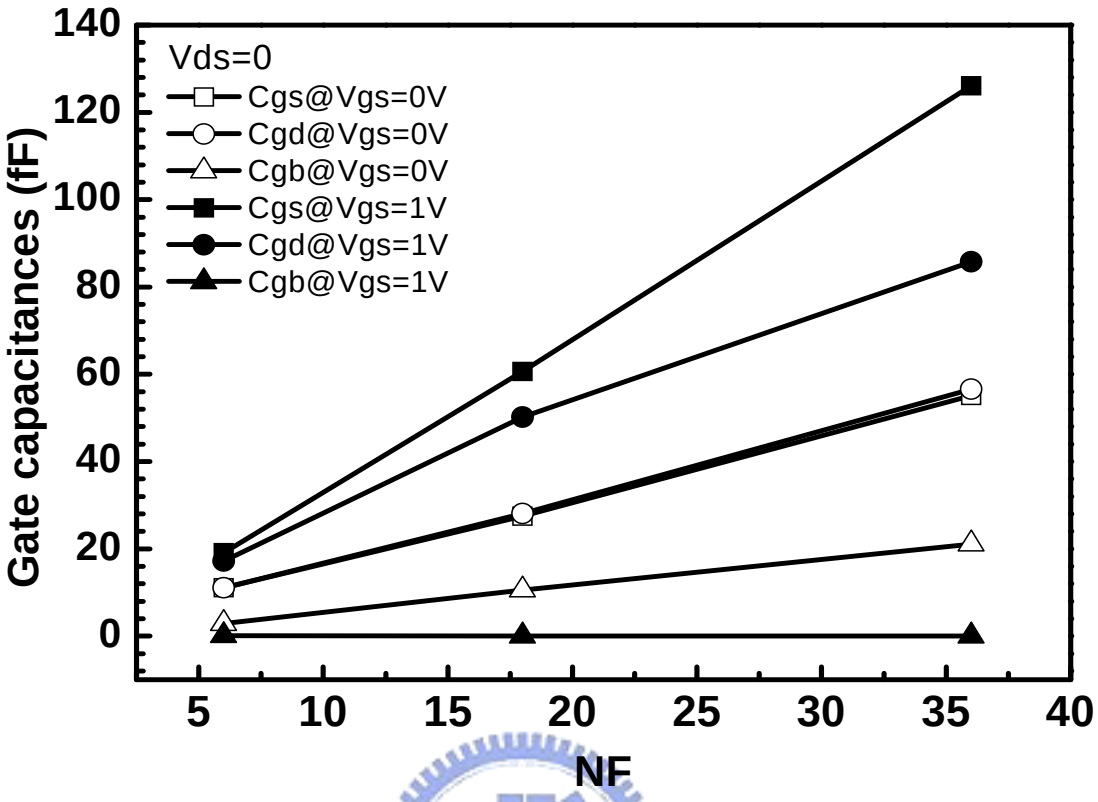


Fig. 4.9 The NF dependence of optimized gate capacitances at Vds=0V

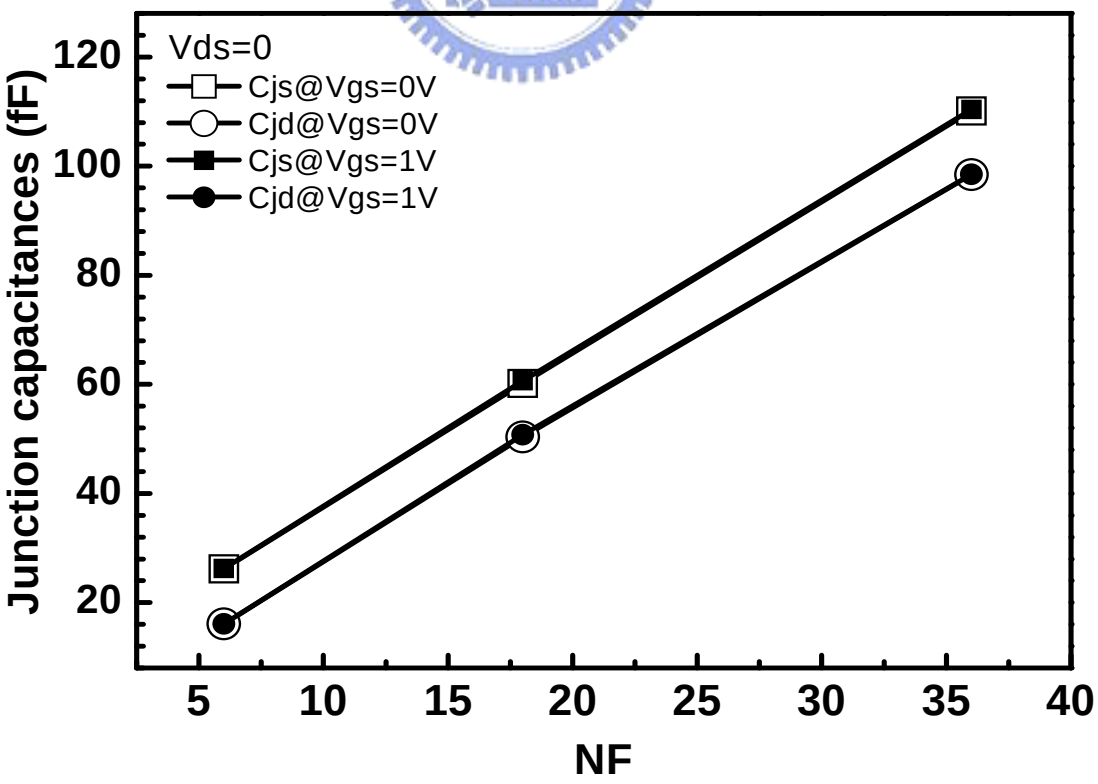


Fig. 4.10 The NF dependence of optimized junction capacitances at Vds=0V

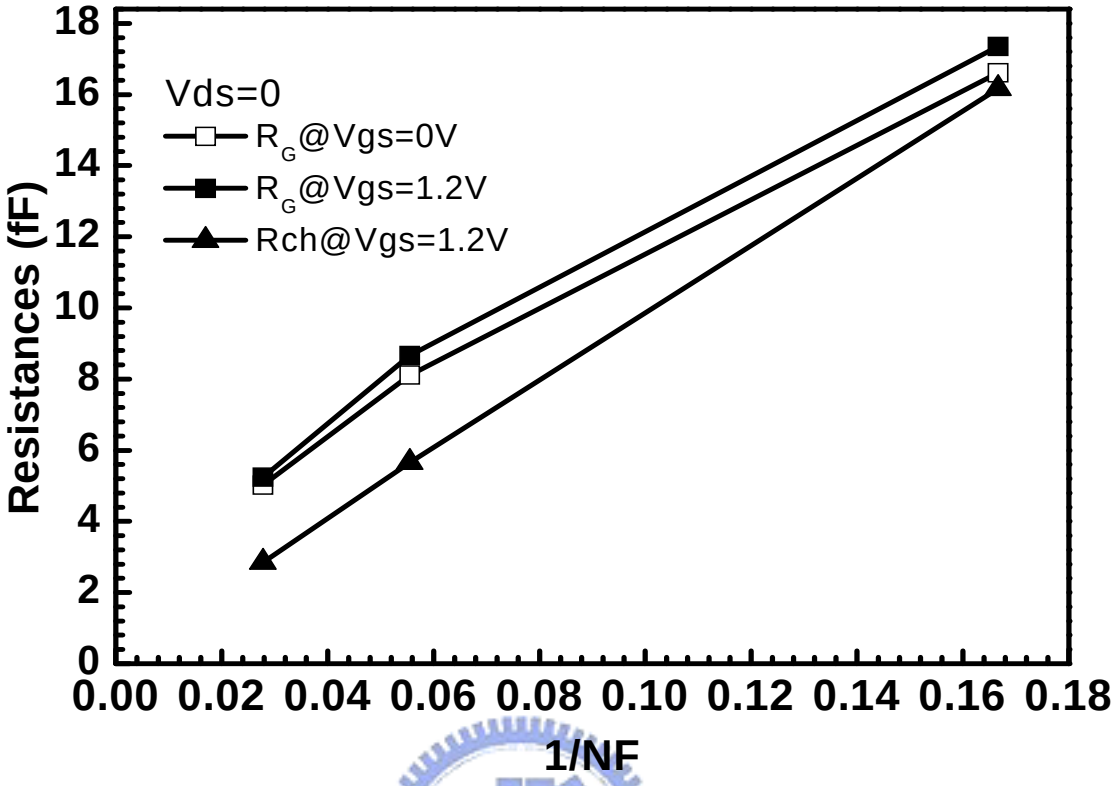


Fig. 4.11 The NF dependence of optimized R_G and Rch at Vds=0V

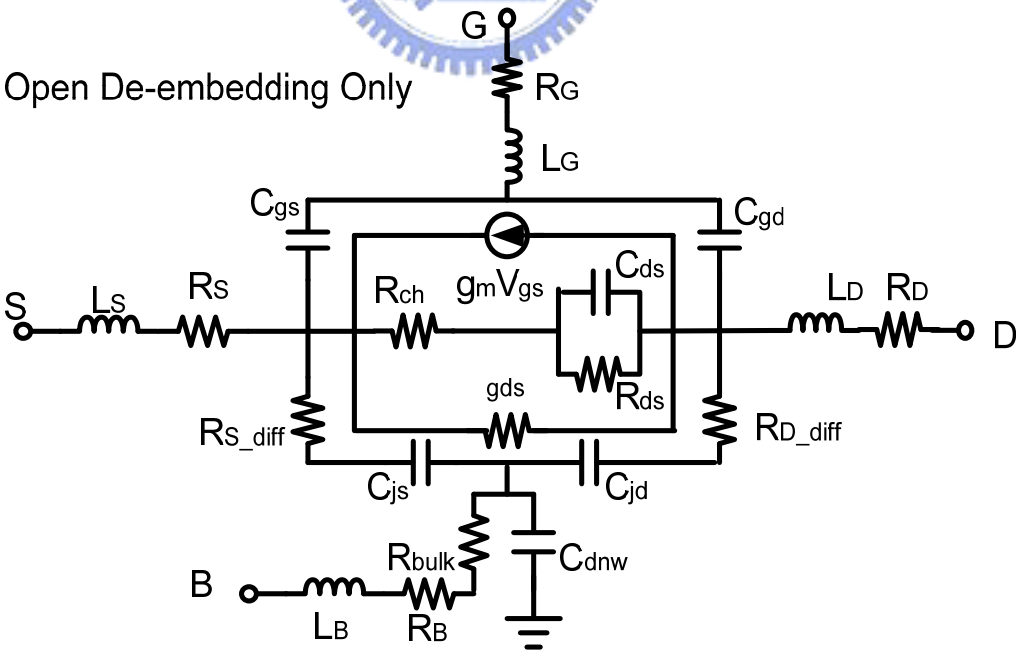


Fig. 4.12 The equivalent circuit of 4-port device at V_{gs}=V_{ds}=1.2V (Open_de)

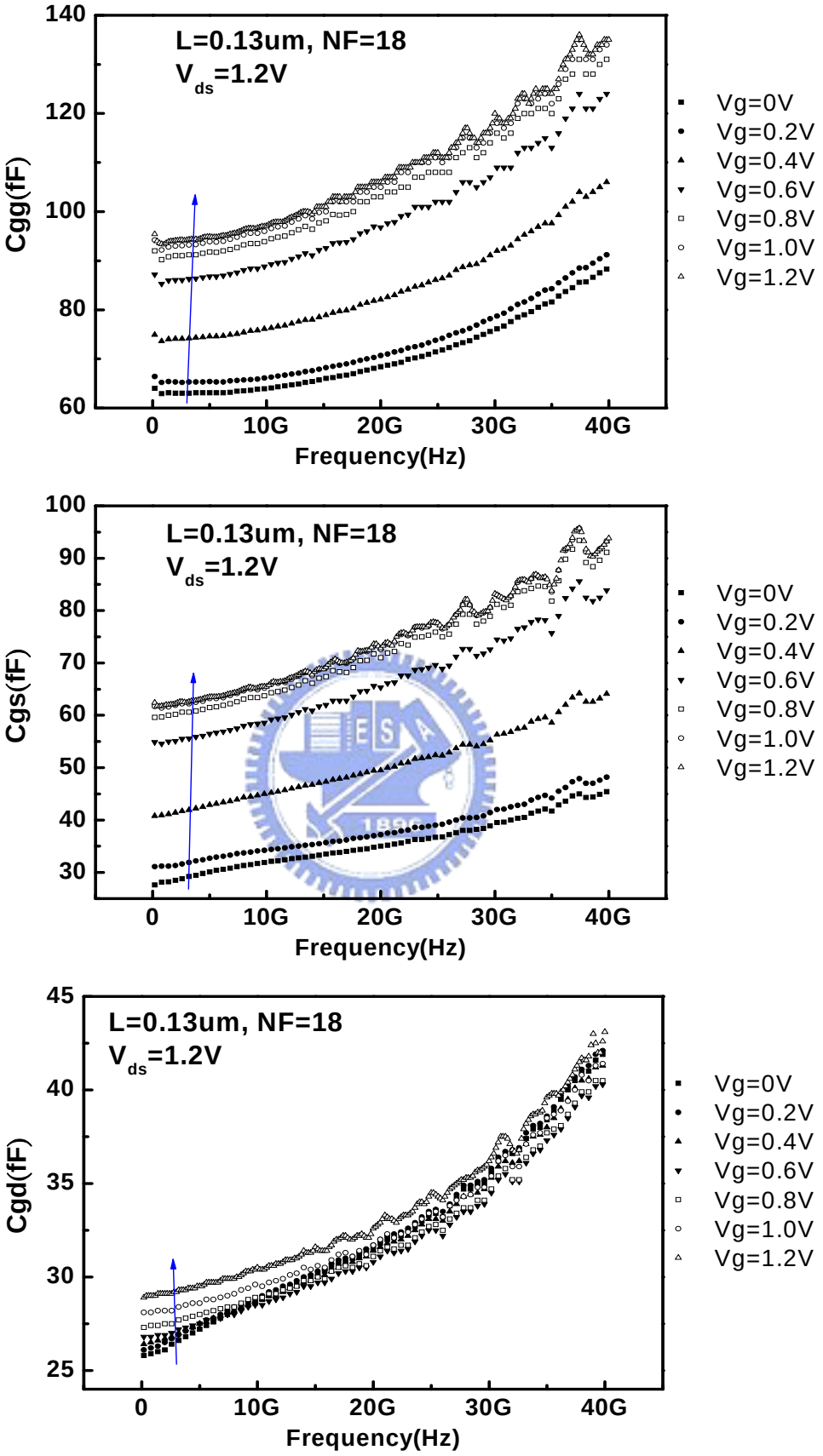


Fig. 4.13 The extracted C_{gg}, C_{gs},C_{gd} capacitance verse frequency at Vds=1.2V

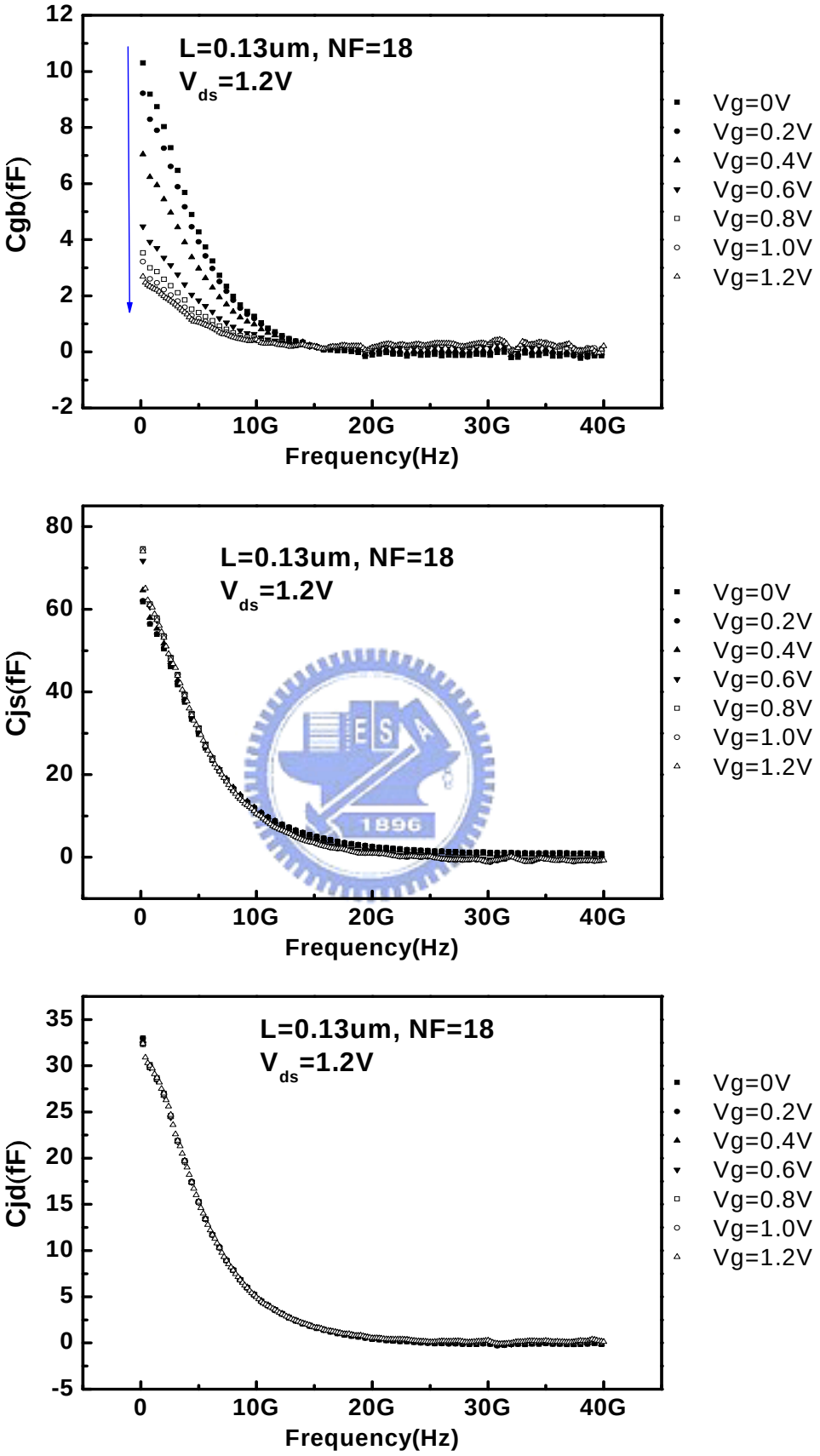


Fig. 4.14 The extracted $C_{gb,}$ $C_{js,}$ C_{jd} capacitance verse frequency at Vds=1.2V

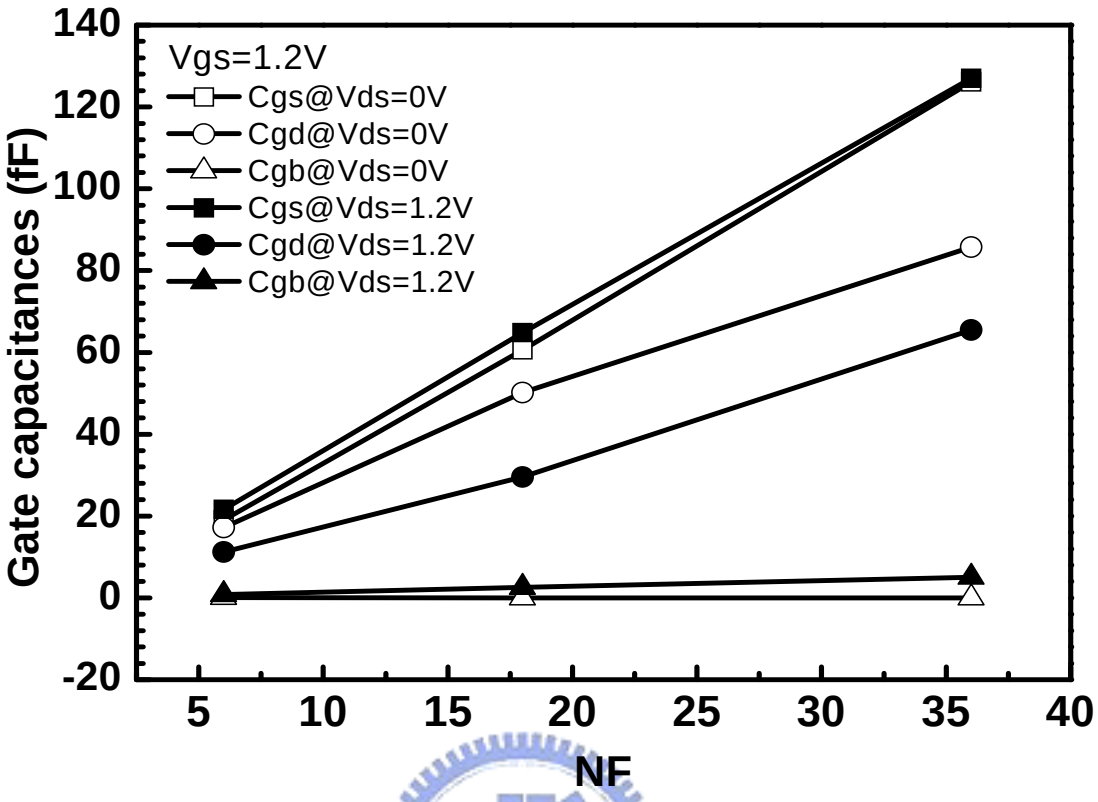


Fig. 4.15 The NF dependence of optimized gate capacitances at Vgs=1.2V

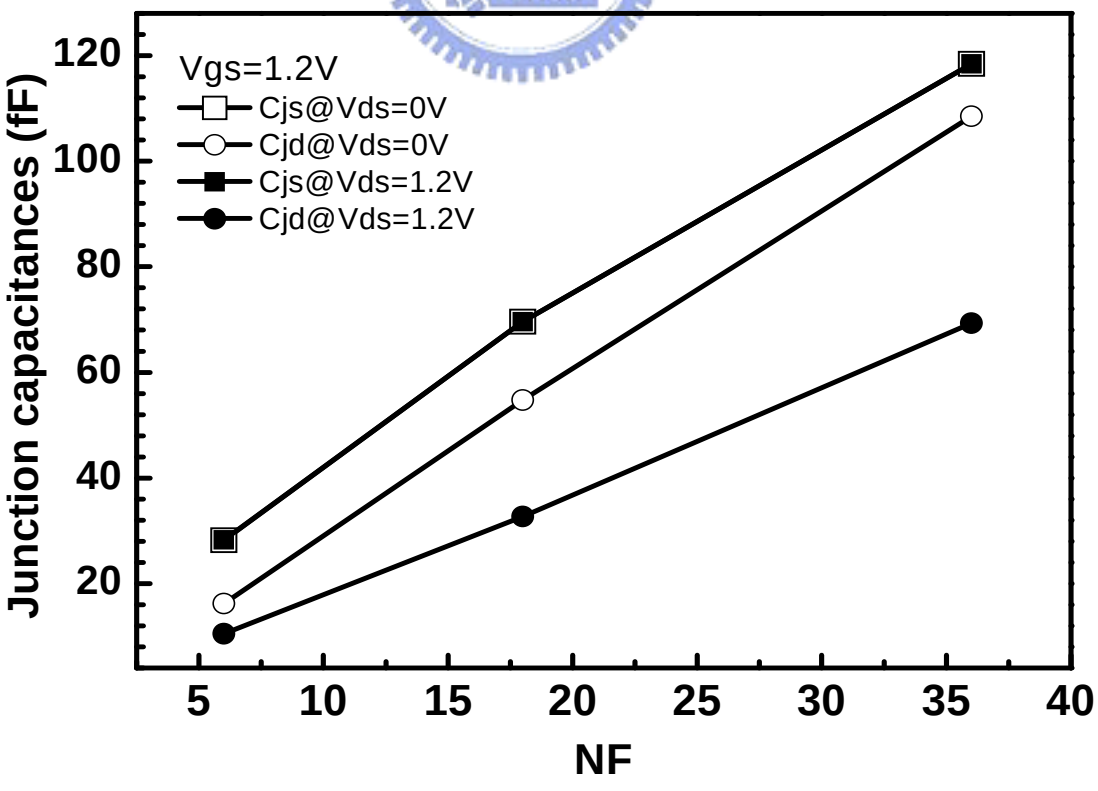


Fig. 4.16 The NF dependence of optimized junction capacitances at Vgs=1.2V

Chapter 5

Model Verification by Circuit Simulation

5.1 Equivalent Circuit model verification

In chapter 3 and 4, the proper equivalent circuit and extraction method for the different bias condition is discussed, after the establishment of the equivalent circuit and the extraction method of parameters, it is essential to verify the validity of the model. Next, the proper equivalent circuit will be verified in this session, the equivalent circuit is simulated by the Advanced Design System (ADS) simulator and ICCAP technology in various bias conditions.

5.2 Two-port 3T MOSFETs under various bias conditions

In this study, three kinds of operate bias condition to consider: 1.off state device (V_{gs}=V_{ds}=0V); 2. Strong inversion in liner region (V_{gs}>>V_{th}, V_{ds}=0V); 3. Strong inversion in saturation region (V_{gs}>>V_{th}, V_{ds}=1V).

5.2.1 3T MOSFETs in linear region

Fig. 3.8 is the illustration of 3T device after open de-embedding at V_{gs}=V_{ds}=0V bias condition, it has been known that substrate resistance will influence the output impedance significantly, inversion layer still doesn't build up in this condition, the signal coming from drain (port2) certainly through Cjd and substrate resistances to the ground, to improve the result between measurement and simulation, it is necessary to adjust the substrate network parameters for optimization. Cdnw does not have the extracted value because the combinatorial substrate network, to fine tune these two

parameters to fit the measurement data by ADS simulation. The model parameters optimized for 3T device under Vgs=Vds=0V are listed in Table 5.1, and the S and Y parameters comparison of simulation and measurement after optimization are plotted in Fig. 5.1.

Table 5.1 The optimized parameters for 3T device at V_{gs}=V_{ds}=0V

L=0.13	Ls(pH)	Ld(pH)	Lg(pH)	Rs	Rd	Rg	Rg_int	Rs_diff	Rd_diff	Cgd(fF)	Cgb(fF)	Cjd(fF)	Rbulk	Cbulk
6	17.52	48.97	41.50	0.22	0.60	0.41	6.11	18.81	23.34	7.26	12.80	14.89	203.60	16.78
18	17.52	47.21	42.31	0.22	0.60	0.41	2.05	6.81	7.57	30.56	15.33	39.68	79.58	33.42
36	17.52	47.21	42.27	0.22	0.60	0.41	1.04	3.52	3.71	66.22	18.42	71.54	47.49	75.53
72	17.52	48.22	42.54	0.22	0.60	0.44	0.53	1.85	1.91	142.30	26.99	138.00	29.58	121.00

L=0.18	Ls(pH)	Ld(pH)	Lg(pH)	Rs	Rd	Rg	Rg_int	Rs_diff	Rd_diff	Cgd(fF)	Cgb(fF)	Cjd(fF)	Rbulk	Cbulk
6	18.10	49.81	42.43	0.22	0.60	0.41	4.26	19.39	24.12	9.05	13.39	15.04	209.20	16.78
18	18.10	47.86	42.43	0.22	0.60	0.41	1.52	7.31	8.13	33.65	16.78	40.65	86.25	33.42
36	18.10	47.38	41.44	0.22	0.60	0.41	0.94	3.79	4.00	72.18	21.42	73.08	52.71	75.53
72	18.10	46.35	42.54	0.22	0.60	0.41	0.53	2.05	2.11	152.30	32.90	137.60	34.92	121.00

L=0.35	Ls(pH)	Ld(pH)	Lg(pH)	Rs	Rd	Rg	Rg_int	Rs_diff	Rd_diff	Cgd(fF)	Cgb(fF)	Cjd(fF)	Rbulk	Cbulk
6	18.10	48.22	43.54	0.22	0.60	0.41	8.29	20.25	25.26	10.05	15.29	15.13	223.50	16.78
18	18.16	48.22	42.92	0.22	0.60	0.41	2.72	7.89	8.76	39.11	20.99	42.68	97.85	33.42
36	18.10	47.53	42.31	0.22	0.60	0.41	1.48	4.34	4.58	81.35	28.16	75.49	66.38	75.53
72	18.01	47.53	43.54	0.22	0.60	0.41	0.68	2.35	2.42	174.20	48.33	136.40	48.57	121.00

L=0.5	Ls(pH)	Ld(pH)	Lg(pH)	Rs	Rd	Rg	Rg_int	Rs_diff	Rd_diff	Cgd(fF)	Cgb(fF)	Cjd(fF)	Rbulk	Cbulk
6	18.10	47.53	44.80	0.22	0.60	0.41	21.29	20.09	25.82	11.41	16.77	15.13	227.60	16.78
18	18.10	48.22	43.54	0.22	0.60	0.41	7.82	7.92	9.28	43.98	24.66	42.68	103.00	33.42
36	18.10	48.22	42.31	0.22	0.60	0.41	4.25	4.34	5.28	87.76	34.64	75.49	71.38	75.53
72	18.10	48.22	43.54	0.22	0.60	0.41	0.53	2.73	2.81	182.20	59.35	136.40	54.57	121.00

The equivalent circuit of 3T device after open de-embedding at Vgs>>Vth and Vds=0V was plotted in Fig. 3.25, we supposed that the substrate network parameters is gate bias independency, the optimized substrate parameters in above session will be used in this circuit, the preliminary result indicate well match in terms S parameters, but has a shift along the frequency in the Y parameter, to improve the behavior at high frequency, terminal inductances and gate resistance will be fine tune for good match, in fact, substrate resistance is lager than the channel resistance in this bias, and drain signal going through channel inversion layer directly, it is almost no different by tuning

the value of substrate resistance, the results suggest that the substrate network does not make any effect under this bias condition. Fine tuning the parameters in these two bias conditions repeatedly, it will be has the same value of parasitic inductance and substrate parameters for the actuary model parameters. The S and Y parameters comparison of simulation and measurement after optimization are plotted in Fig. 5.2, and the model parameters optimized for 3T devices under Vgs=1V,Vds=0V are listed in Table 5.2.

Table 5.2 The optimized parameters for 3T device at V_{gs}=1V, V_{ds}=0V

L=0.13	Ls(pH)	Ld(pH)	Lg(pH)	RS	RD	RG	Rch	Rs_diff	Rd_diff	Cgs(fF)	Cgd(fF)	Cjd(fF)	Rbulk	Cbulk
6	17.52	48.97	41.50	0.19	1.94	12.71	14.56	18.81	23.34	20.99	20.99	14.89	203.60	16.78
18	17.22	47.21	42.31	0.19	1.08	4.89	4.93	6.81	7.57	56.41	56.41	39.68	79.58	33.42
36	17.22	47.21	42.27	0.19	0.80	2.74	2.54	3.52	3.71	118.40	118.40	71.54	47.49	75.53
72	17.52	48.22	42.54	0.19	0.66	1.98	1.47	1.85	1.91	230.50	230.50	138.00	29.58	121.00

L=0.18	Ls(pH)	Ld(pH)	Lg(pH)	RS	RD	RG	Rch	Rs_diff	Rd_diff	Cgs(fF)	Cgd(fF)	Cjd(fF)	Rbulk	Cbulk
6	18.10	49.81	42.43	0.19	2.13	10.35	20.79	19.39	24.12	29.69	29.69	15.04	209.20	16.78
18	18.10	47.86	42.43	0.19	0.99	4.06	7.17	7.31	8.13	85.22	85.22	40.65	86.25	33.42
36	18.10	47.38	41.44	0.19	0.65	2.40	3.69	3.79	4.00	166.70	166.70	73.08	52.71	75.53
72	18.10	46.35	42.54	0.19	0.49	1.95	2.06	2.05	2.11	334.30	334.30	137.60	34.92	121.00

L=0.35	Ls(pH)	Ld(pH)	Lg(pH)	RS	RD	RG	Rch	Rs_diff	Rd_diff	Cgs(fF)	Cgd(fF)	Cjd(fF)	Rbulk	Cbulk
6	18.10	48.22	43.54	0.19	7.21	8.93	38.45	20.25	25.26	59.05	59.05	15.13	223.50	16.78
18	18.16	48.22	42.92	0.19	1.96	3.13	14.31	7.89	8.76	169.40	169.40	42.68	97.85	33.42
36	18.10	47.53	42.31	0.19	0.98	2.24	7.36	4.34	4.58	341.50	341.50	75.49	66.38	75.53
72	18.01	47.53	43.54	0.19	0.76	1.43	4.12	2.35	2.42	690.20	690.20	136.40	48.57	121.00

L=0.5	Ls(pH)	Ld(pH)	Lg(pH)	RS	RD	RG	Rch	Rs_diff	Rd_diff	Cgs(fF)	Cgd(fF)	Cjd(fF)	Rbulk	Cbulk
6	18.10	47.37	43.20	0.19	8.13	8.25	55.37	20.09	25.82	87.13	87.13	15.63	227.60	16.78
18	18.10	47.98	44.75	0.19	2.39	3.69	20.75	7.92	9.28	220.40	220.40	37.07	103.00	33.42
36	18.20	47.58	42.27	0.19	1.06	1.96	11.07	4.34	5.28	467.60	467.60	72.38	71.38	75.53
72	18.20	46.58	43.85	0.19	0.63	1.55	6.19	2.73	2.81	903.80	903.80	142.90	54.57	121.00

5.2.2 3T MOSFETs in saturation region

The equivalent circuit of 3T device after open de-embedding at Vgs>>Vth and Vds=1V was plotted in Fig. 3.39, the equitant circuit is most complicated one because

the current gain and asymmetry between source and drain along the channel. in this bias condition, the optimized substrate network and parasitic RL parameters in Table 5.2 is used for the simulation, there exists large deviation in the simulation S_{22} from the measurement, according to the equivalent circuit, the output impedance compose of the R_{bulk}, C_{jd}, R_{ch}, R_{ds}, C_{ds}, g_m and g_{ds}. The re-optimization required for gm come from the parasitic resistance effect on Id and gm, and the deviation in g_{ds} will impact R_{ch} and R_{ds} derived form the reciprocal of g_{ds}, therefore, re-tuning and optimization on the motioned parameters to enable fit to measurement by simulation. Through the fine tuning by manually and optimization automatic by the simulation tool ICCAP. The S and Y parameters comparison of simulation and measurement after optimization are plotted in Fig. 5.3, and the model parameters optimized for 3T devices under Vgs=Vds=0V are listed in Table 5.3.

Table 5.3 The optimized parameters for 3T device at V_{gs}= V_{ds}=1V

L=0.13	RS	RD	RG	Cgs(fF)	Cgd(fF)	Cjs(fF)	Cjd(fF)	Rch	CDS(fF)	RDS	gm(mS)	gds(mS)
6	0.19	1.94	12.71	30.2	10.32	14.89	11.17	357.70	130.32	282.49	23.99	1.60
18	0.19	2.13	10.35	40.75	10.91	15.04	11.28	546.10	33.65	#######	19.77	0.66
36	0.19	7.21	8.93	75.15	13.04	15.13	8.28	856.00	11.07	#######	12.68	0.15
72	0.19	8.13	8.25	119.9	13.34	15.63	11.07	#######	5.11	#######	10.23	0.18

L=0.18	RS	RD	RG	Cgs(fF)	Cgd(fF)	Cjs(fF)	Cjd(fF)	Rch	CDS(fF)	RDS	gm(mS)	gds(mS)
6	0.19	1.08	4.89	78.76	30.57	39.68	29.76	136.77	282.49	154.18	69.80	5.11
18	0.19	0.99	4.06	112.9	34.26	40.65	30.65	198.33	91.90	677.33	56.00	2.40
36	0.19	1.96	3.13	202.4	38.39	42.68	26.42	383.00	37.07	#######	38.60	0.62
72	0.19	2.39	3.69	325	43.32	37.07	24.99	497.60	29.11	#######	29.11	0.38

L=0.35	RS	RD	RG	Cgs(fF)	Cgd(fF)	Cjs(fF)	Cjd(fF)	Rch	CDS(fF)	RDS	gm(mS)	gds(mS)
6	0.19	0.80	2.74	142.9	67.32	71.54	53.68	85.98	739.10	80.50	143.50	10.05
18	0.19	0.65	2.40	203.6	75.05	73.08	54.81	145.20	125.40	277.60	103.00	4.50
36	0.19	0.98	2.24	415	76.31	75.49	49.09	193.60	80.35	787.60	73.00	1.22
72	0.19	1.06	1.96	633.4	79.69	72.38	53.08	254.60	72.95	#######	57.30	0.55

L=0.5	RS	RD	RG	Cgs(fF)	Cgd(fF)	Cjs(fF)	Cjd(fF)	Rch	CDS(fF)	RDS	gm(mS)	gds(mS)
6	0.19	0.66	1.98	251.5	140.10	138.00	105.00	60.94	#######	51.50	221.00	18.00
18	0.19	0.49	1.95	366.9	155.50	137.60	104.20	94.60	256.40	97.50	193.40	6.80
36	0.19	0.76	1.43	787	167.90	136.40	91.72	118.40	174.20	310.10	138.30	1.60
72	0.19	0.63	1.60	1128	172.20	142.90	80.35	165.20	123.50	853.40	109.90	0.85

5.3 Four port MOSFETs under various bias conditions

For four port devices, three kinds of operate bias condition to consider: 1.off state device (V_{gs}=V_{ds}=0V); 2. Strong inversion in liner region (V_g=1.2V, V_{ds}=0V); 3. Strong inversion in saturation region (V_g=1.2V, V_{ds}=1.2V).

5.3.1 4T MOSFETs in linear region

The equivalent circuit of four-port devices after open de-embedding at V_g=V_d=V_s=V_b=0V was plotted in Fig. 4.7. Using the extracted model parameters for primary simulation and fine tune the parasitic inductance according to the imaginary part of Y parameters along the frequency, gate resistance according to the Re(Y_{11}) at high frequency, substrate resistance according to the Im(Y_{24}), Im(Y_{34}) with the RC decay behavior, in this condition, to maintain the charge conservation in body terminal, it should be add a parameter Cbb in body terminal, and use a parameter Rbb connect with Cbb to control the RC decay behaviors in Im(Y_{44}), and Cbb can be calculated from the equation (5.1).The modified equivalent circuit are plotted in Fig. 5.4 and Fig. 5.5, the substrate networks compose with a lumped RC equivalent circuit in a multi-finger device, to simplify substrate networks, substrate resistance represent as a total distributed effect resistance, and Cbb represent as the nearest capacitance between substrate and DNW, when the impedance of Cbb smaller than the Rbulk with operate frequency increasing, the body signal can coupling to DNW by the Cbb directly and connection to GND with a resistance. The S and Y parameters comparison of simulation and measurement after optimization are plotted in Fig. 5.6~Fig. 5.13. And the model parameters optimized for four-port devices under Vg=Vd=0V are listed in Table 5.4.

$$C_{\mathrm{bb}}+C_{\mathrm{dnw}} \cong \mathrm{Im}\left(Y_{44}^{dut}-Y_{41}^{dut}-Y_{42}^{dut}-Y_{43}^{dut}\right)/\omega \qquad (5.1)$$

Table 5.4 The optimized parameters for four-port device at V_{gs}= V_{ds}=0V

NF	Lg(pH)	Ls(pH)	Ld(pH)	Lb(pH)	RG	RS	RD	RB	Rs_diff	Rd_diff
6	69.65	69.54	66.59	65.12	16.61	0.73	0.73	0.73	20.11	26.82
18	79.65	73.59	79.59	76.90	8.11	0.73	0.73	0.73	8.66	9.63
36	81.64	79.59	81.59	79.11	5.02	0.71	0.73	0.73	4.17	4.40

NF	Cgs(fF)	Cgd(fF)	Cgb(fF)	Cjs(fF)	Cjd(fF)	Rbulk	Cdnw(fF)	Cbb(fF)	Rbb
6	11.06	11.06	2.84	26.19	16.09	352.13	24.04	39.25	93.60
18	27.47	28.08	10.55	60.17	50.34	272.51	27.76	61.02	103.12
36	55.15	56.62	21.05	110.10	98.40	185.70	66.10	75.46	113.78

According to the equivalent circuit of four-port device after open de-embedding at Vg>>Vth, Vd=Vs=Vb=0V and the additional substrate parameters Cbb, Rbb, the model parameters optimized for four-port devices under Vg=1.2V, Vd=0V are listed in Table 5.5.

One thing mentioned that the substrate networks component is ignorable in two-port 3T devices in this supplied bias condition, because channel resistance is smaller than the impedance of substrate network from drain to source. For four-port devices, owing to body terminal connected to signal pad and separate from source terminal, substrate resistance will affect the behavior in body terminal directly, it is essential element to model the substrate network. Looking at the parameters that Y_{GG}, Y_{GD}, Y_{DG}, and Y_{DD} can be express the two-port CS configuration MOSFET characteristic under this bias condition, it is always unchanged with the varying R_{bulk} and the result is expectable.

Table 5.5 The optimized parameters for four-port device at V_{gs}=1.2V, V_{ds}=0V

NF	Lg(pH)	Ls(pH)	Ld(pH)	Lb(pH)	RG	RS	RD	RB	Rs_diff	Rd_diff
6	69.65	69.54	66.59	65.12	16.61	0.73	0.73	0.73	20.11	26.82
18	79.65	73.59	79.59	76.90	8.66	0.73	0.73	0.73	8.66	9.63
36	81.64	79.59	81.59	79.11	5.24	0.71	0.73	0.73	4.17	4.40

NF	Rch	Cgs(fF)	Cgd(fF)	Cgb(fF)	Cjs(fF)	Cjd(fF)	Rbulk	Cdnw(fF)	Cbb(fF)	Rbb
6	16.16	19.10	17.21	0.10	28.21	16.19	352.13	24.04	39.25	93.60
18	5.66	60.60	50.18	0.01	69.61	54.77	272.51	27.76	61.02	103.12
36	2.85	129.11	85.76	0.02	118.40	108.50	185.70	66.10	75.46	113.78

5.3.2 4T MOSFETs in saturation region

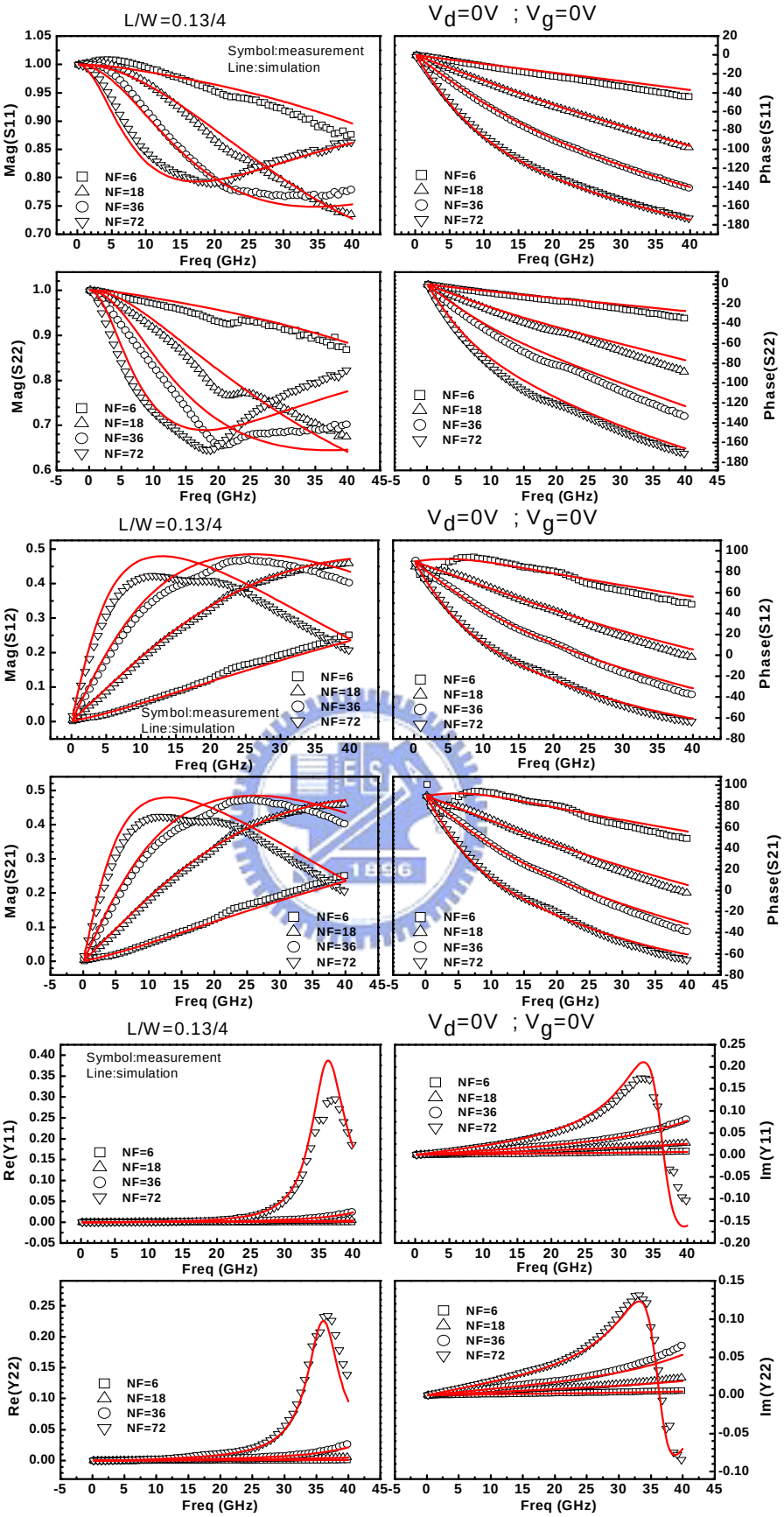
The equivalent circuit of four-port device after open de-embedding at V_g=V_{ds}=1.2V, Vs=Vb=0V was plotted in Fig. 4.20, it must be add a current gain g_{mb} parameters between drain and source to fit the Im(Y_{24}) and Im(Y_{34}), the current gain g_{mb} can be extracted from the Re(Y_{db}).The modified equivalent circuit is plotted in Fig. 5.14, the S and Y parameters comparison of simulation and measurement after optimization are plotted in Fig. 5.15~Fig. 5.18. And the model parameters optimized for four-port devices under Vgs=Vds=1.2V are listed in Table 5.6.

Table 5.6 The optimized parameters for four-port device at V_{gs}=V_{ds}=1.2V

NF	Lg(pH)	Ls(pH)	Ld(pH)	Lb(pH)	RG	RS	RD	RB	Rs_diff	Rd_diff
6	69.65	69.54	66.59	65.12	16.36	0.73	0.73	0.73	20.11	26.82
18	79.65	73.59	79.59	76.90	8.50	0.73	0.73	0.73	8.66	9.63
36	81.64	79.59	81.59	79.11	5.28	0.71	0.73	0.73	4.17	4.40

NF		Cgs(fF)	Cgd(fF)	Cgb(fF)	Cjs(fF)	Cjd(fF)	Rbulk	Cdnw(fF)	Cbb(fF)	Rbb
6		21.66	11.24	0.80	28.29	10.47	352.13	24.04	39.25	93.60
18		64.84	29.52	2.61	69.61	32.68	272.51	27.76	61.02	103.12
36		127.00	65.49	5.02	118.40	69.32	185.70	66.10	75.46	113.78

NF	Rds	Cds	Rch		Gm(ms)	Gds(ms)	Gmb(ms)
6	1630.00	5.92	302.00		19.50	1.90	3.96
18	323.38	8.30	185.43		51.62	5.59	14.10
36	215.14	29.22	31.77		86.12	10.72	28.60


L/W=0.13/4
V_d=0V ; V_g=0V
Symbol:measurement
Line:simulation
NF=6
NF=18
NF=36
NF=72
Mag(S11)
Phase(S11)
Mag(S22)
Phase(S22)
Mag(S12)
Phase(S12)
Mag(S21)
Phase(S21)
Re(Y11)
Im(Y11)
Re(Y22)
Im(Y22)
Freq (GHz)

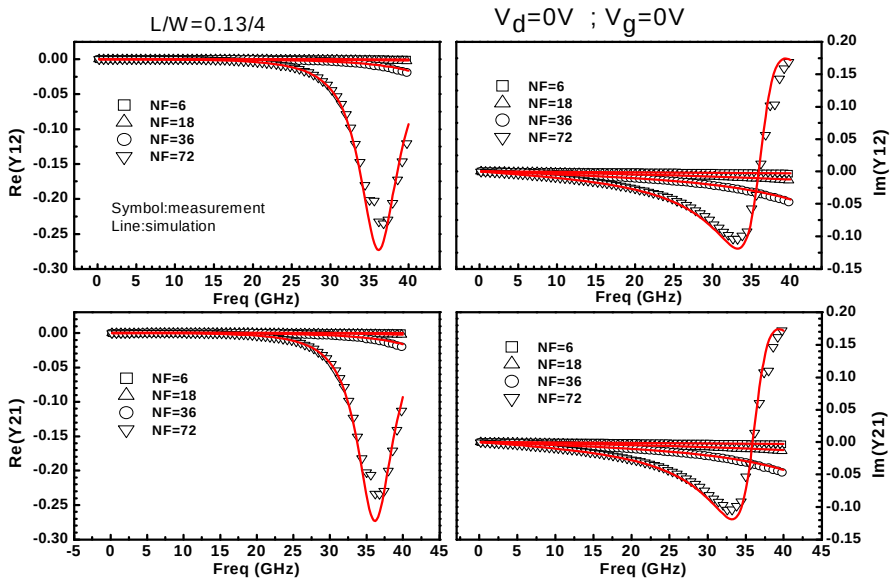
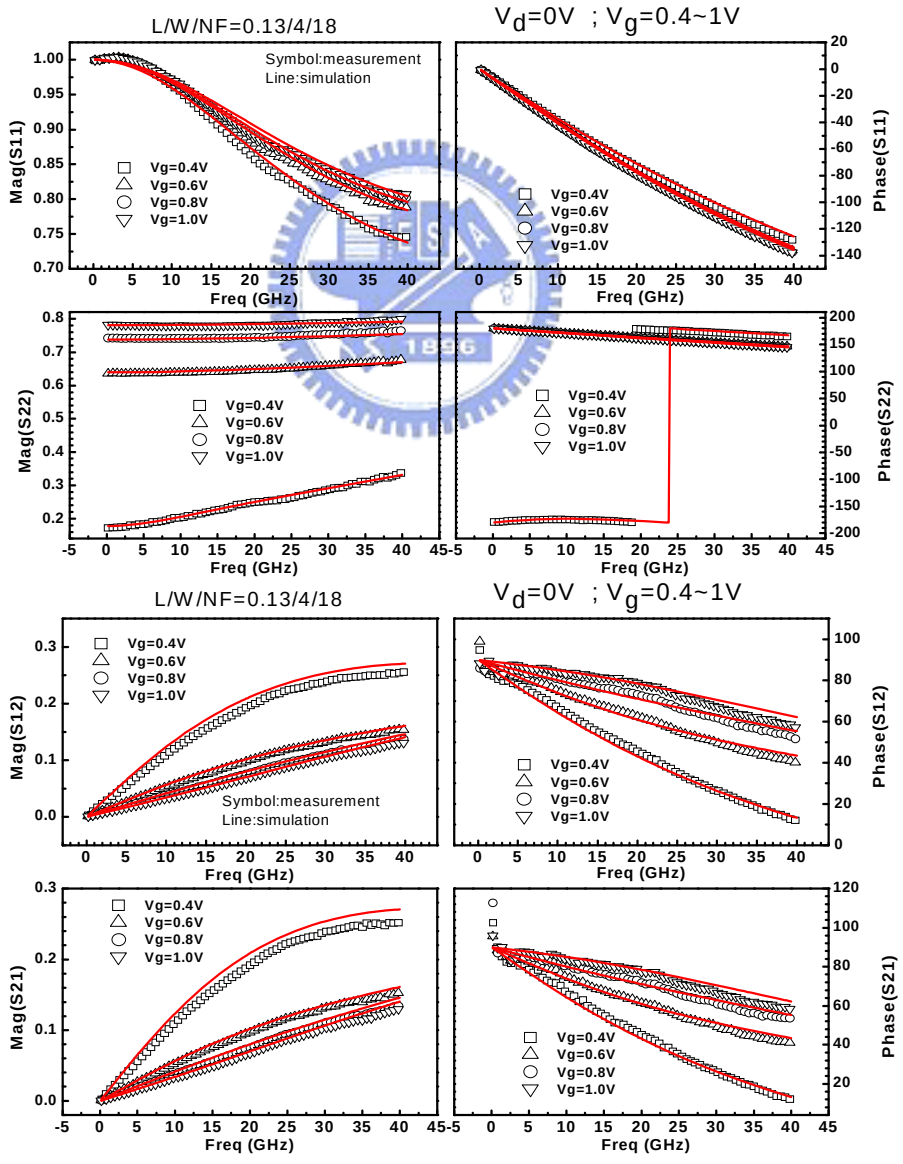


Fig. 5.1 The comparison of 3T devices at Vgs=Vds=0V and L=0.13um



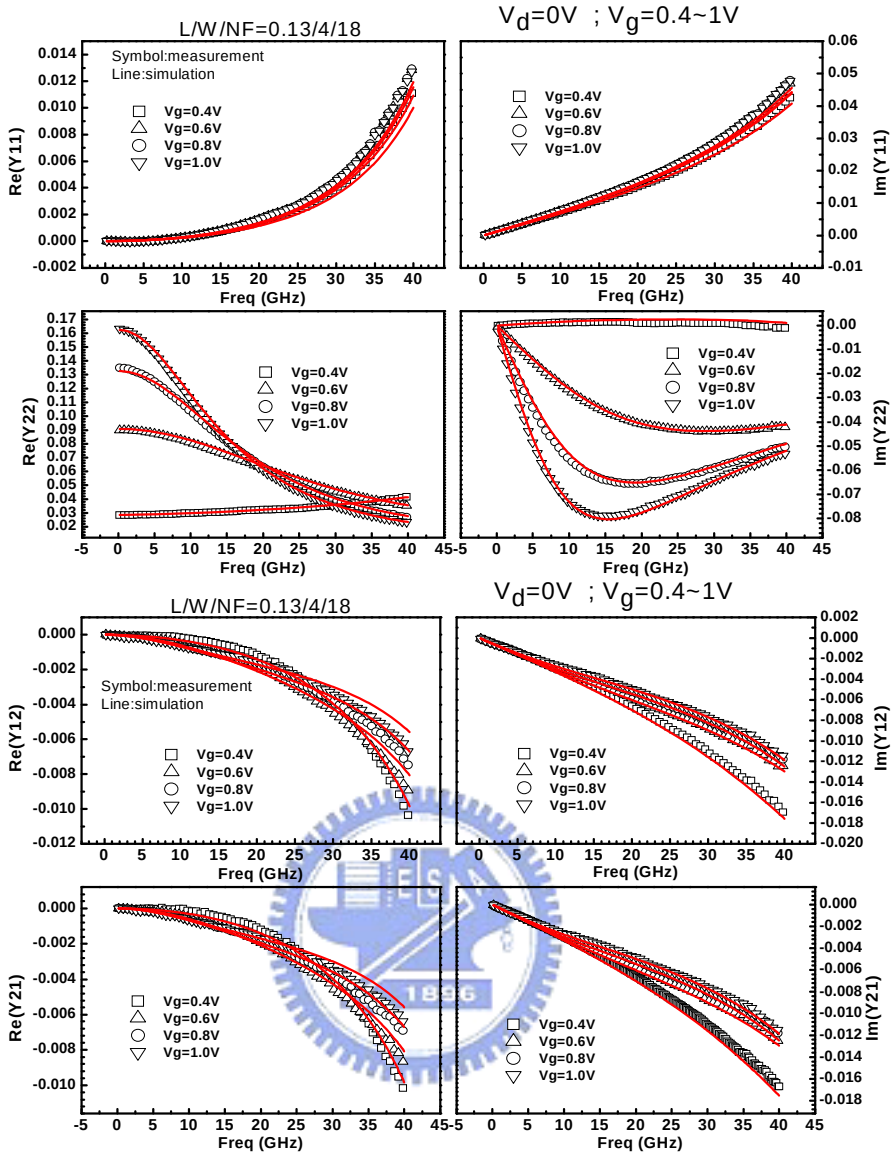
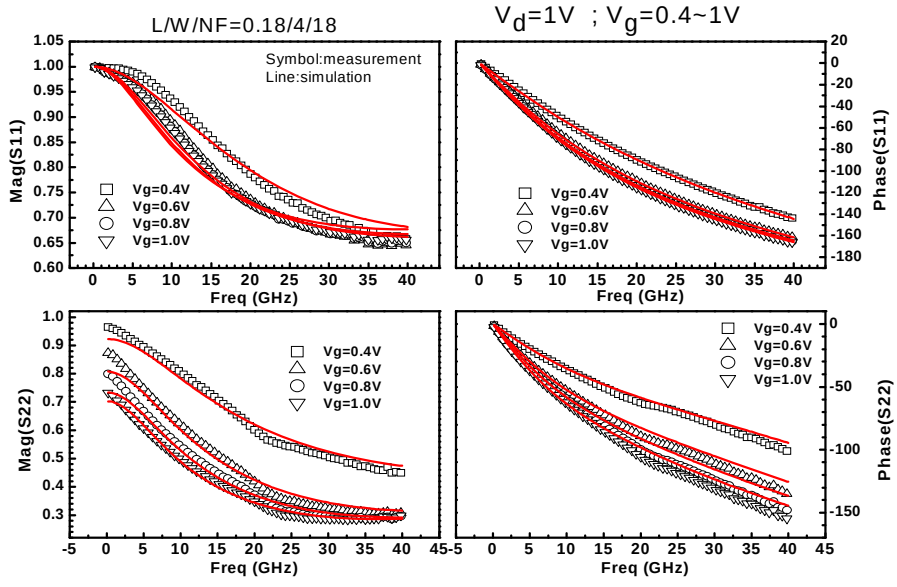


Fig. 5.2 The comparison of 3T devices at Vgs>>Vth, Vds=0V and L=0.13um



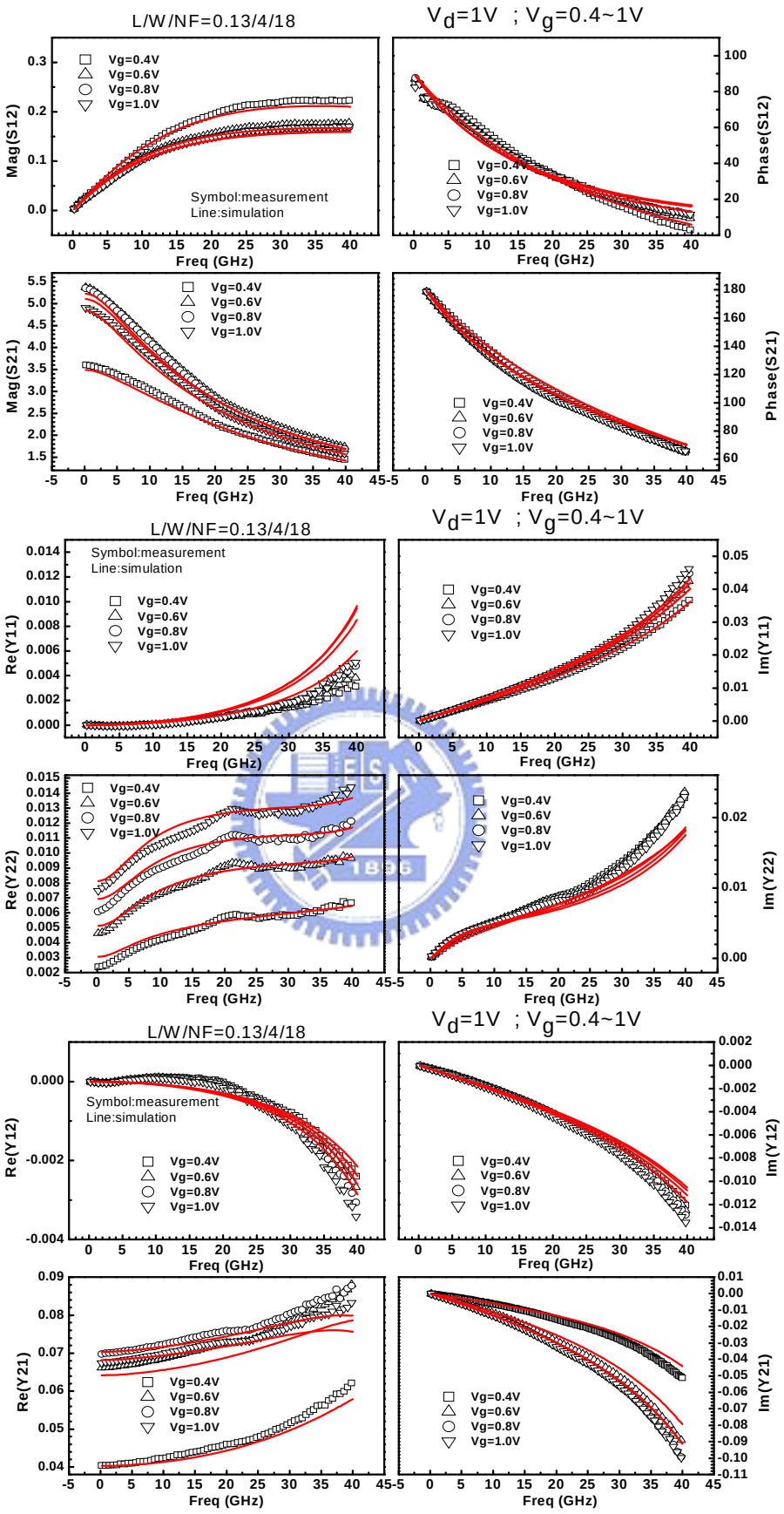


Fig. 5.3 The comparison of 3T devices at Vgs>>Vth, Vds=1V and L =0.13um

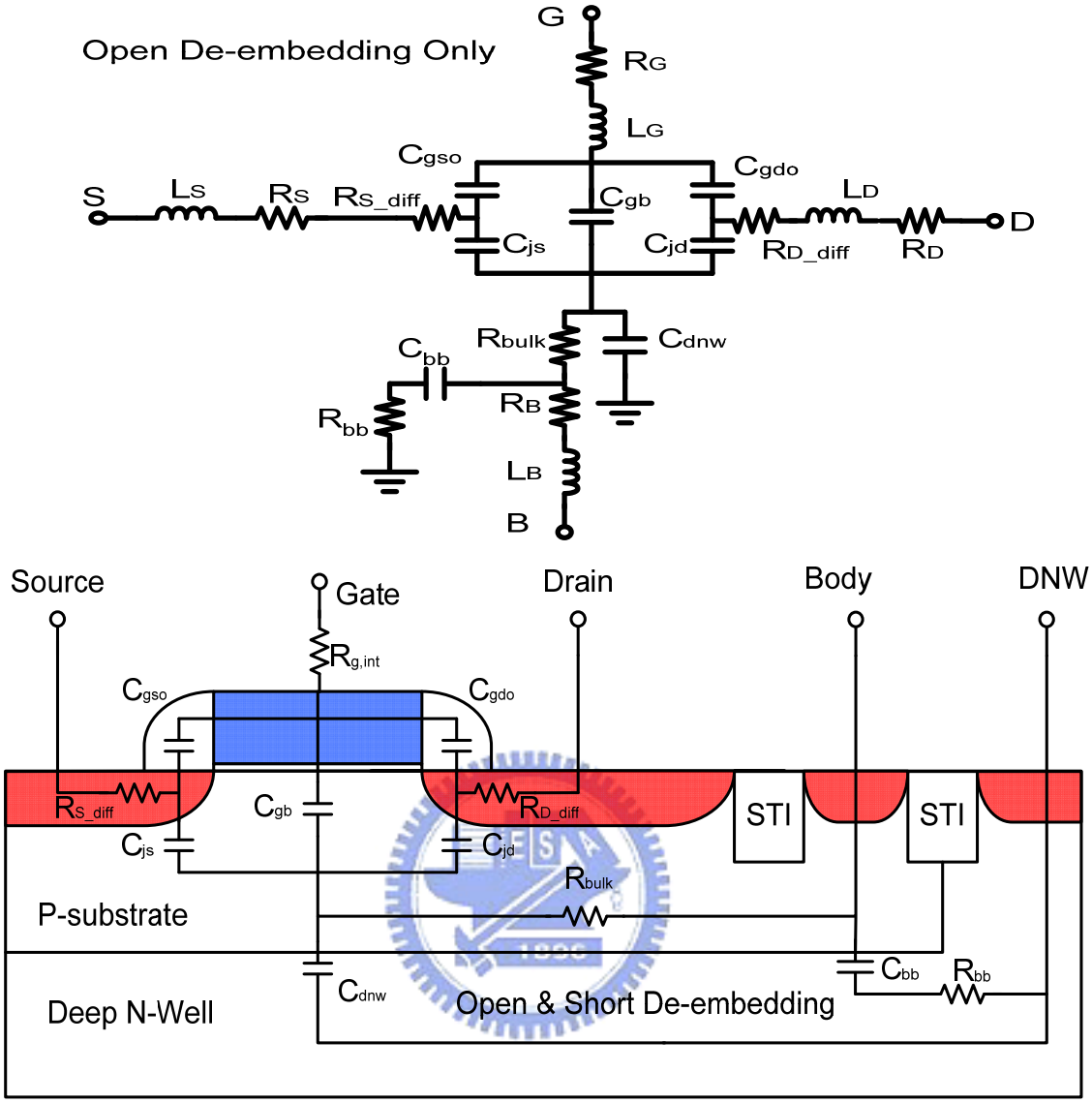


Fig. 5.4 The modified equivalent circuit of 4-port device at Vgs=Vds=0V

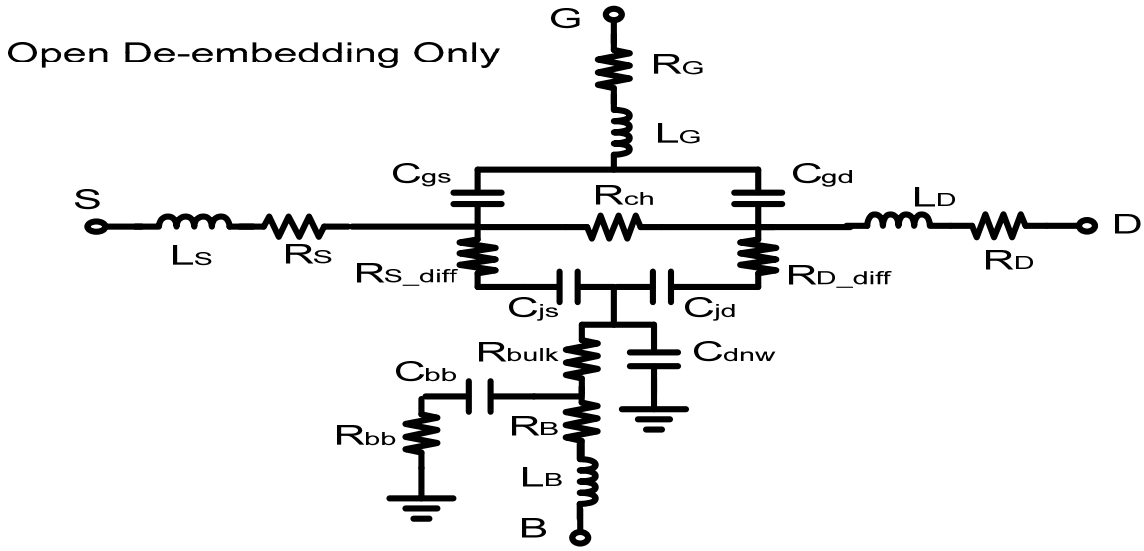
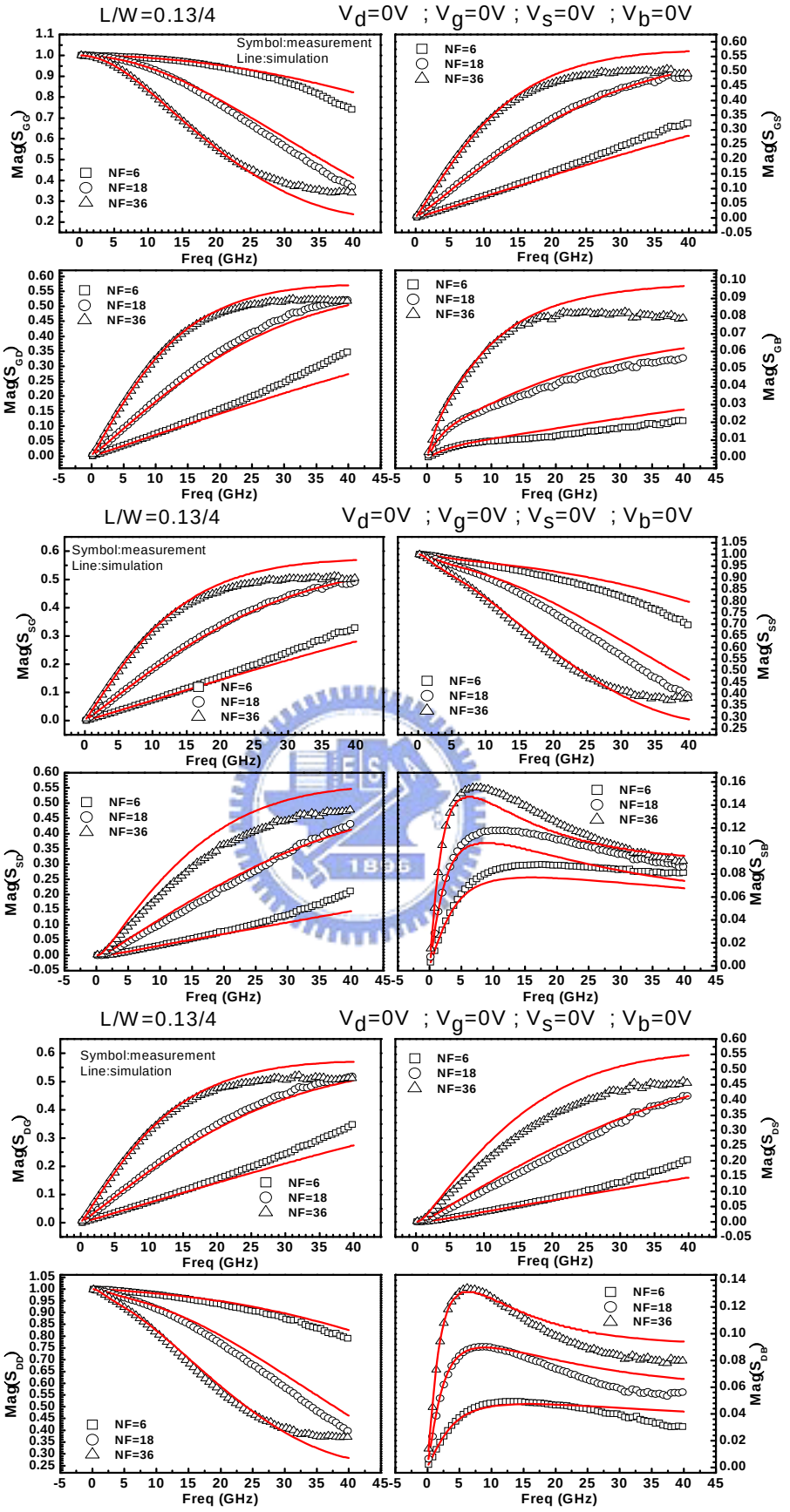


Fig. 5.5 The modified equivalent circuit of 4-port device at V_{gs}=1.2V, V_{ds}=0V


L/W=0.13/4
V_d=0V ; V_g=0V ; V_s=0V ; V_b=0V
Symbol:measurement
Line:simulation
NF=6
NF=18
NF=36
Freq (GHz)
Mag(S_{GG})
Mag(S_{GS})
Mag(S_{GD})
Mag(S_{GB})
L/W=0.13/4
V_d=0V ; V_g=0V ; V_s=0V ; V_b=0V
Symbol:measurement
Line:simulation
NF=6
NF=18
NF=36
Freq (GHz)
Mag(S_{SG})
Mag(S_{SS})
Mag(S_{SD})
Mag(S_{SB})
L/W=0.13/4
V_d=0V ; V_g=0V ; V_s=0V ; V_b=0V
Symbol:measurement
Line:simulation
NF=6
NF=18
NF=36
Freq (GHz)
Mag(S_{DG})
Mag(S_{DS})
Mag(S_{DD})
Mag(S_{DB})

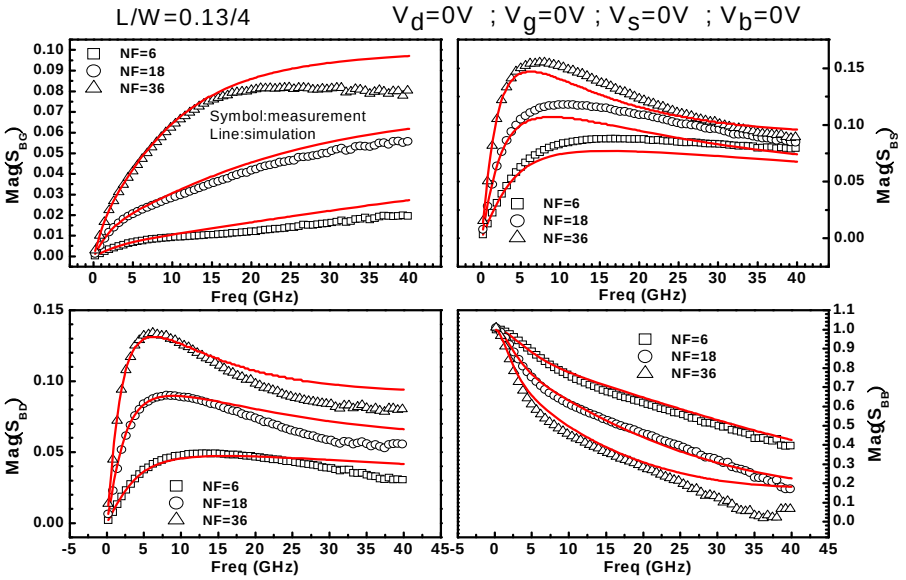
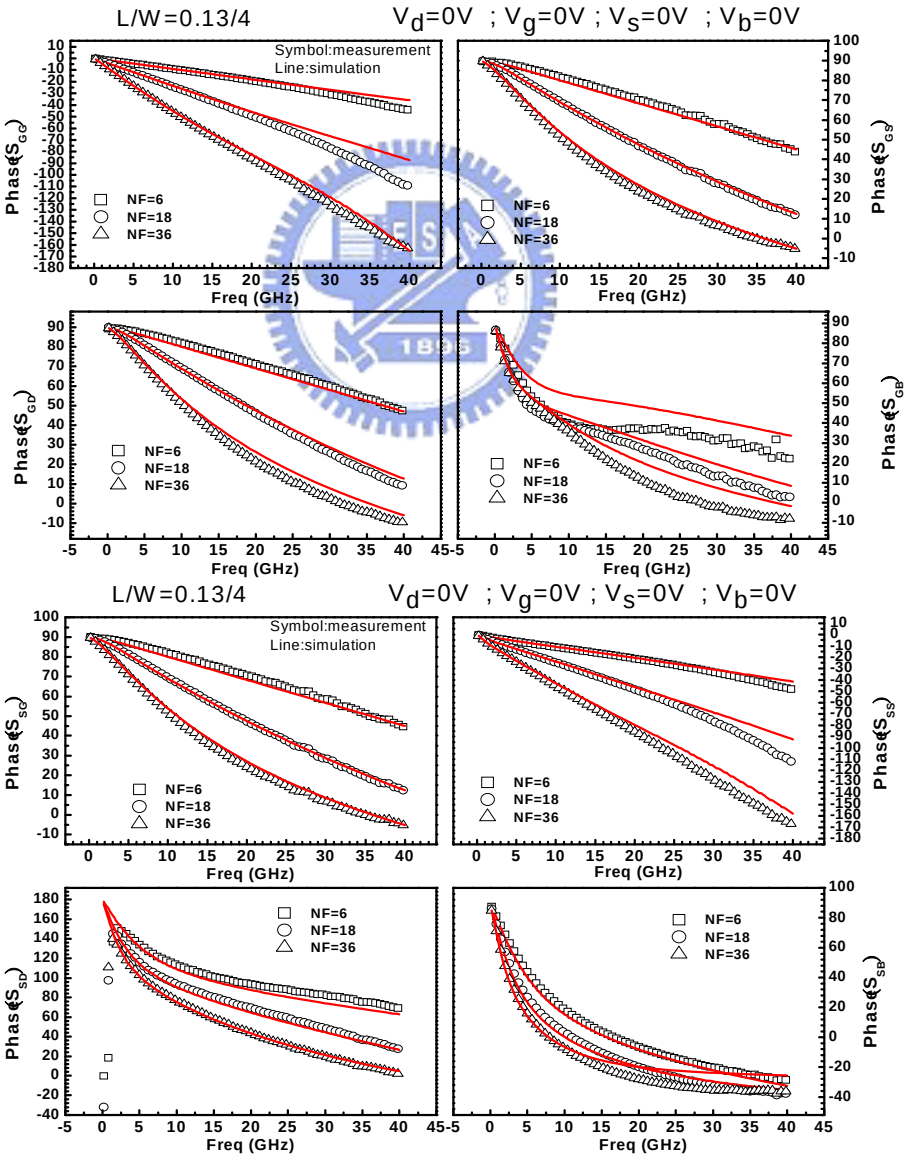


Fig. 5.6 The measured and simulated Mag(S) of 4-port devices at Vgs=Vds=0V



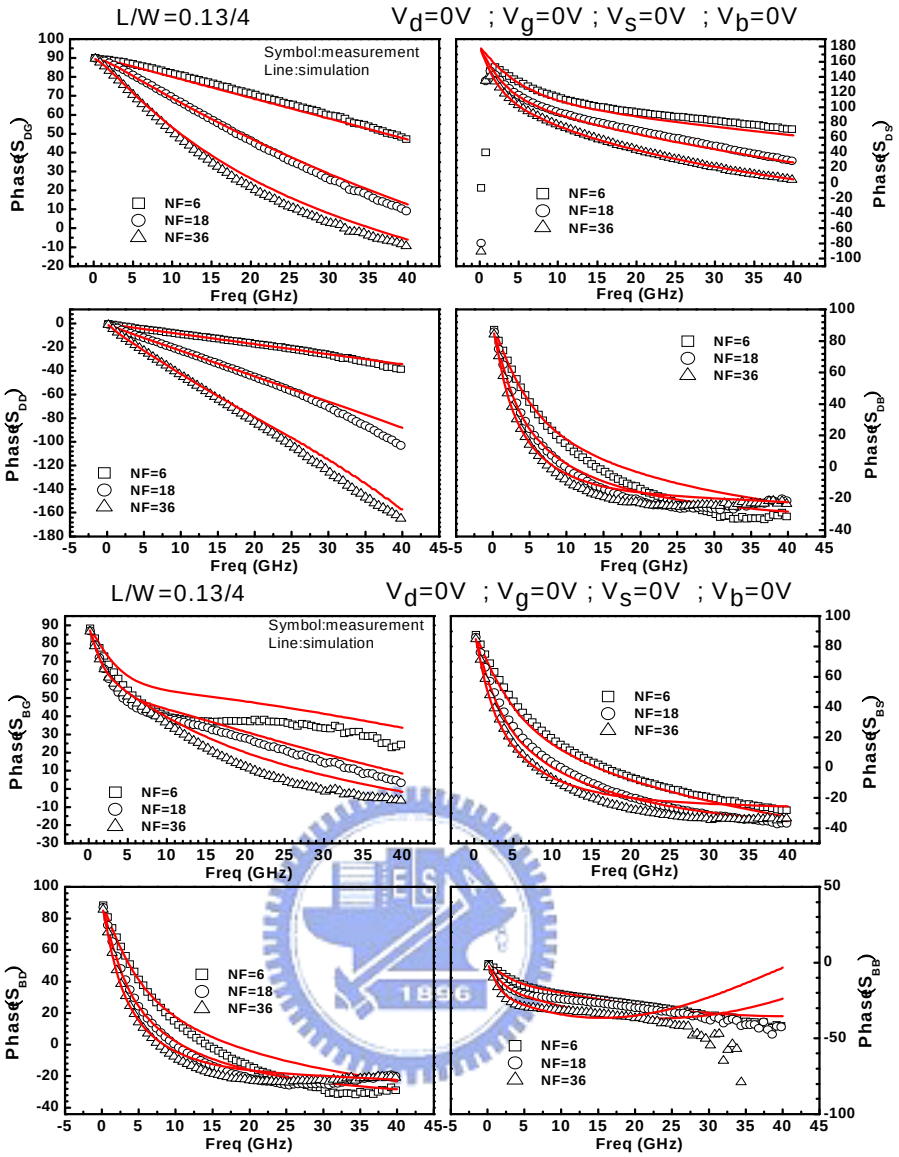
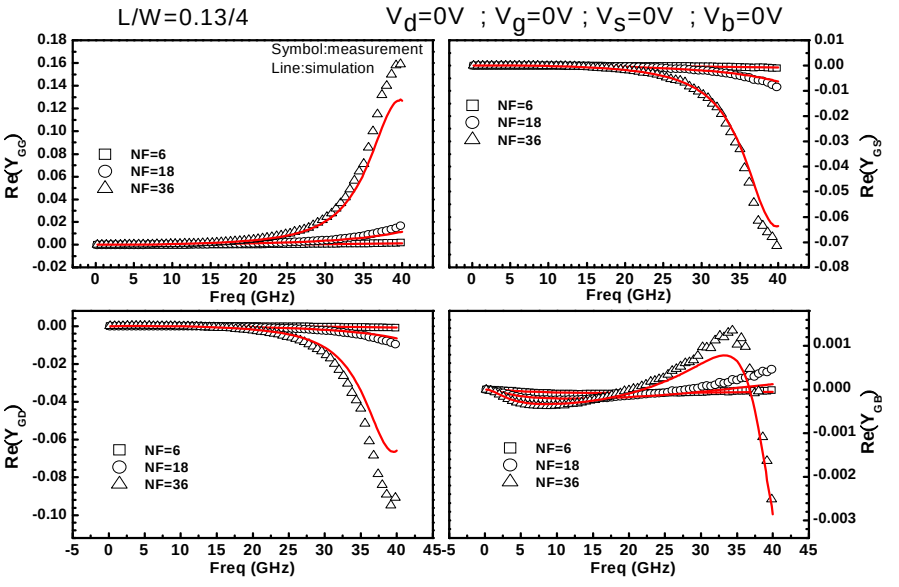


Fig. 5.7 The measured and simulated Phase(S) of 4-port devices at Vgs=Vds=0V



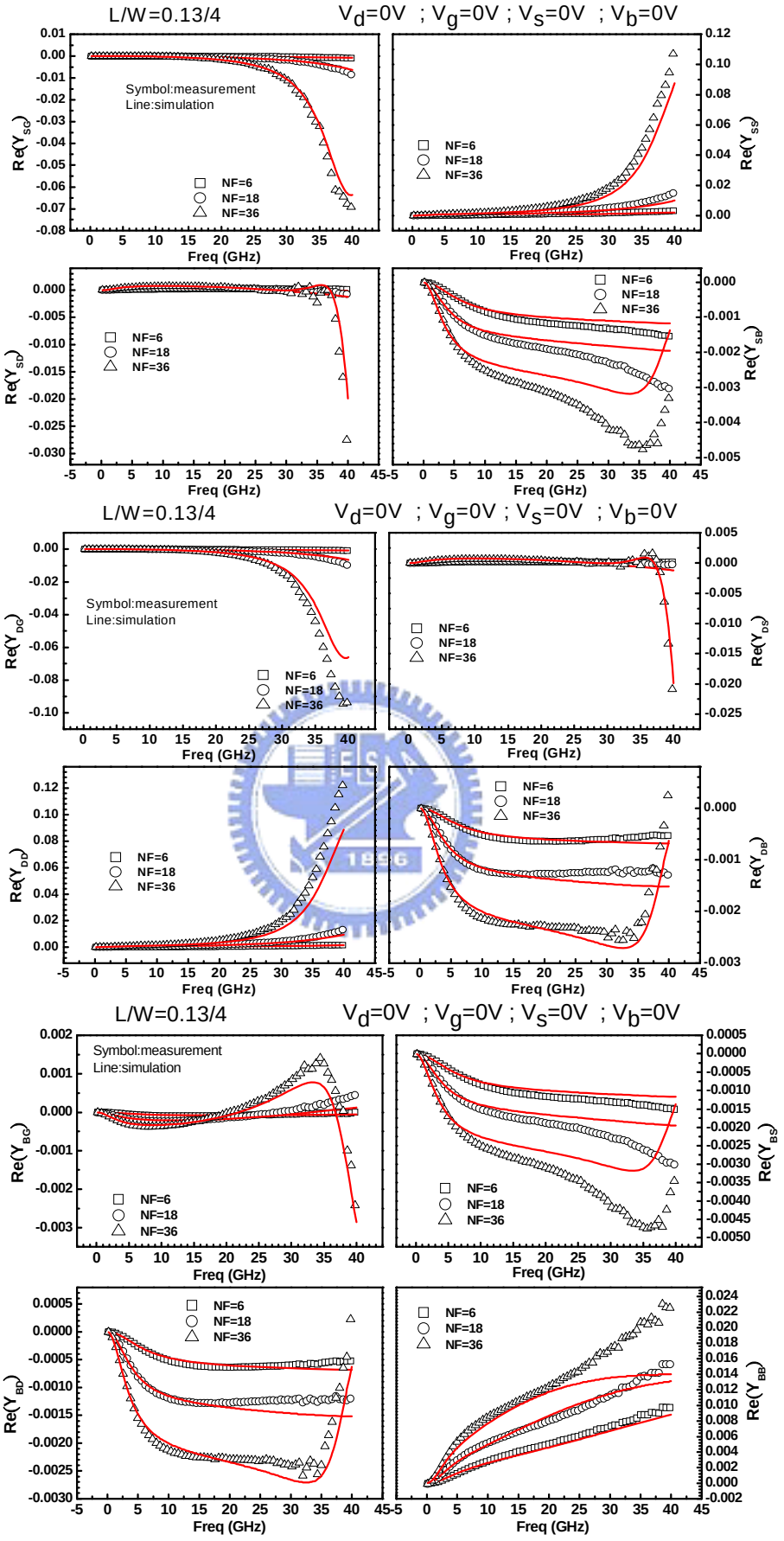
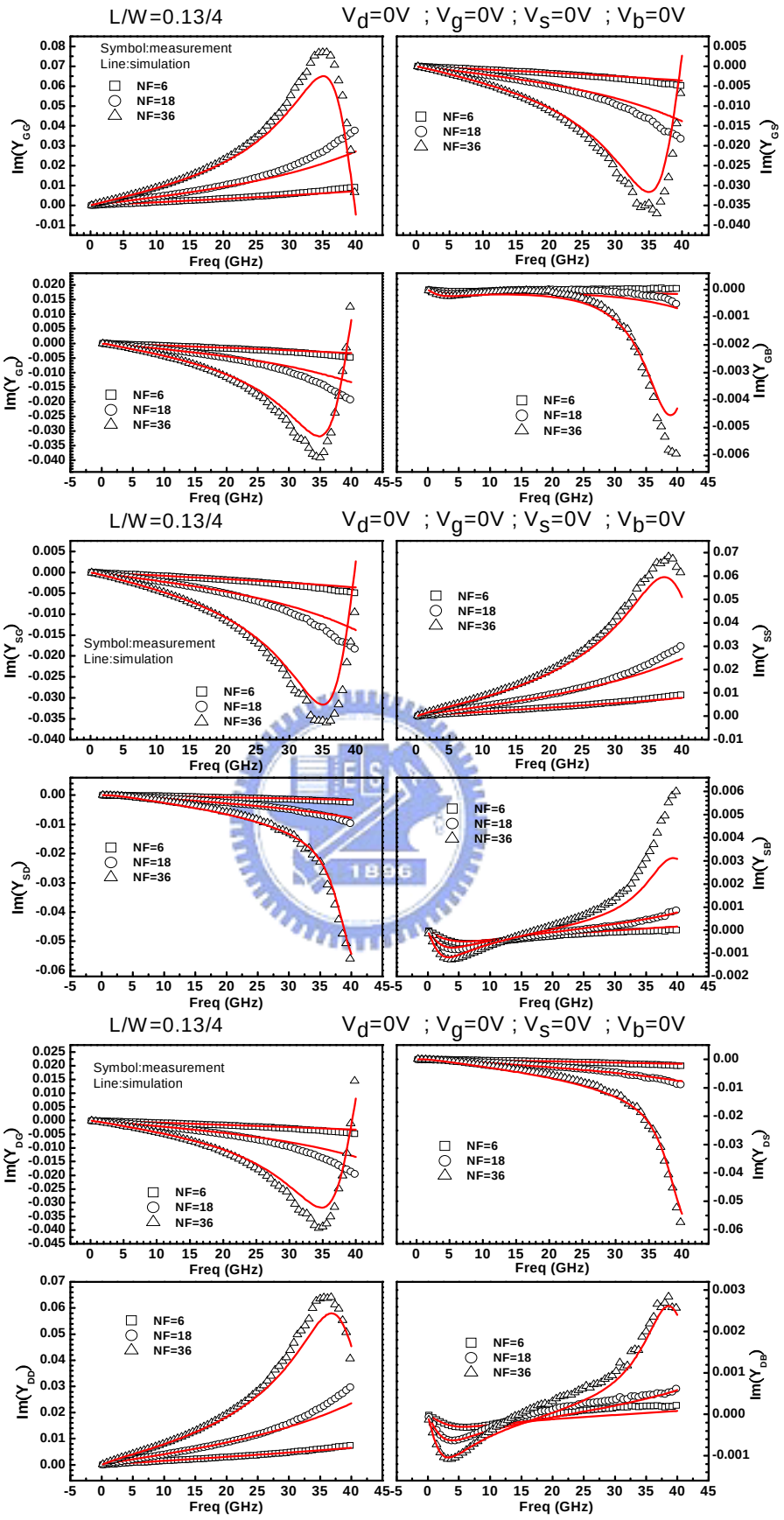


Fig. 5.8 The measured and simulated Re(Y) of 4-port devices at Vgs=Vds=0V


L/W=0.13/4
Vd=0V ; Vg=0V ; Vs=0V ; Vb=0V
Symbol:measurement
Line:simulation
NF=6
NF=18
NF=36
Freq (GHz)
Im(YGG)
Im(YGS)
Im(YGD)
Im(YGB)
Im(YSG)
Im(YSS)
Im(YSD)
Im(YSB)
Im(YDG)
Im(YDS)
Im(YDD)
Im(YDB)

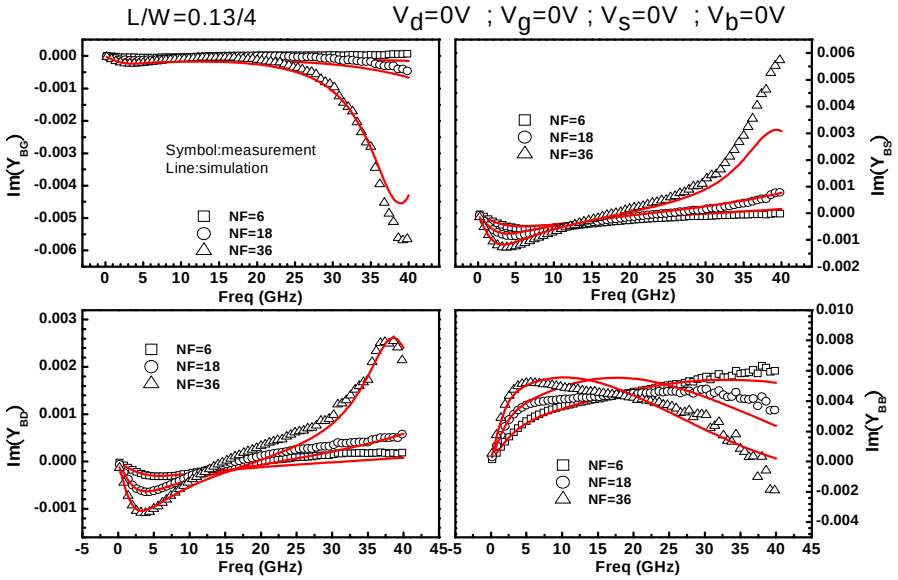
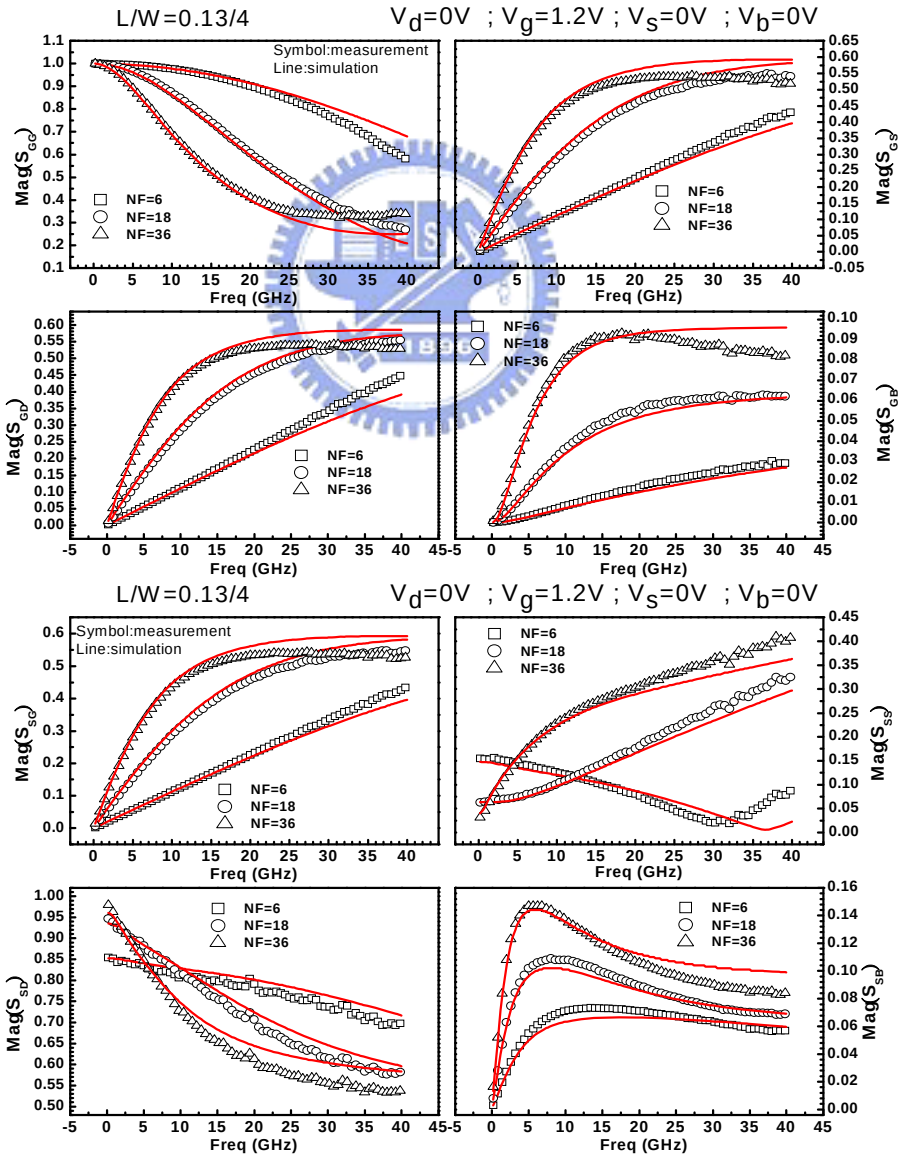


Fig. 5.9 The measured and simulated Im(Y) of 4-port devices at Vgs=Vds=0V



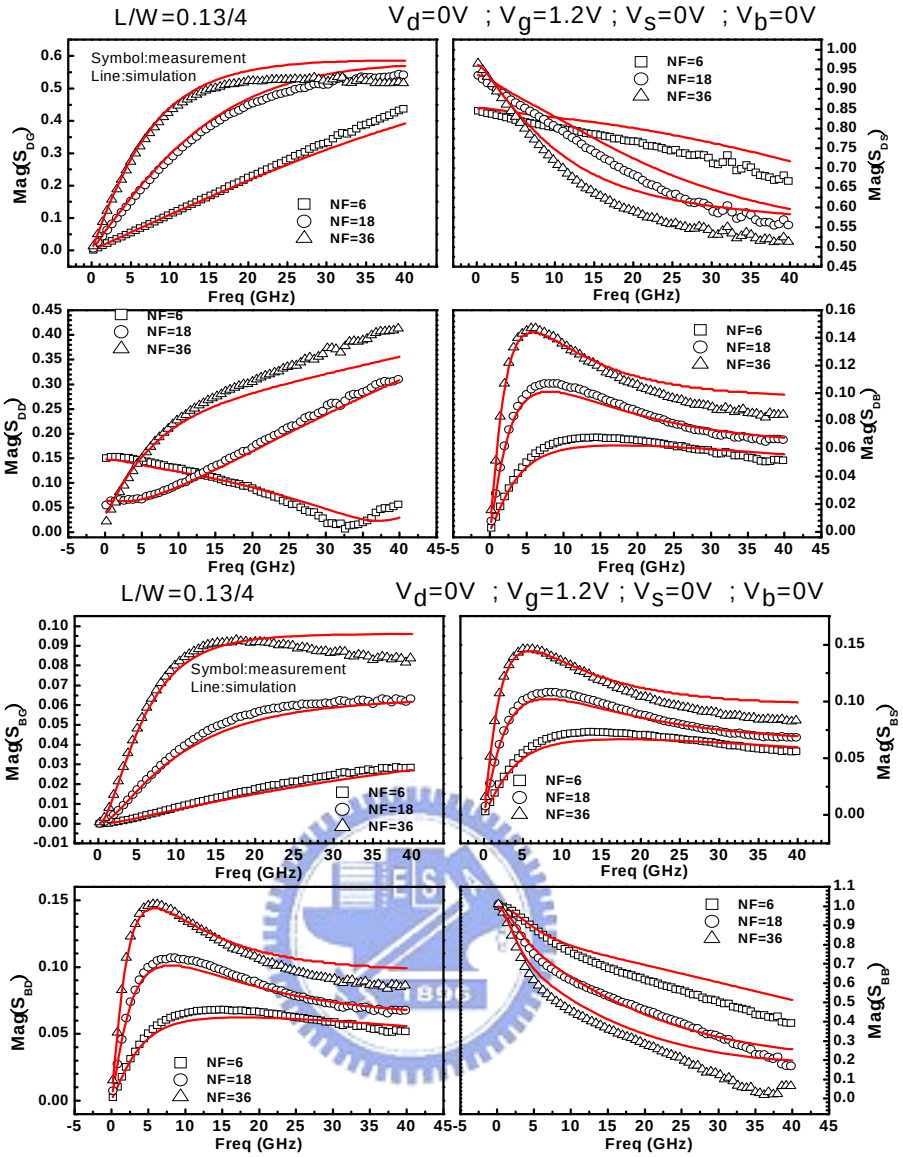
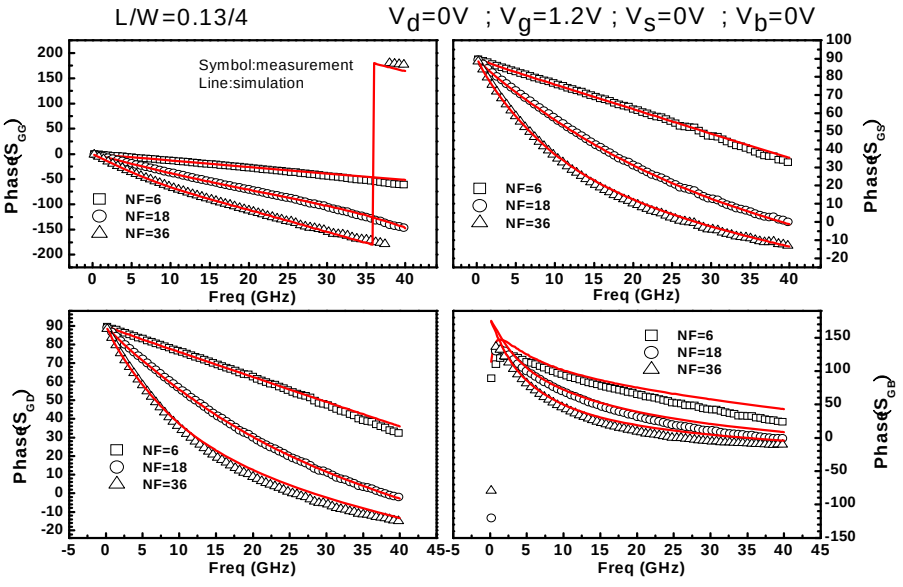


Fig. 5.10 The measured and simulated Mag(S) of 4-port devices at Vgs=1.2V, Vds=0V



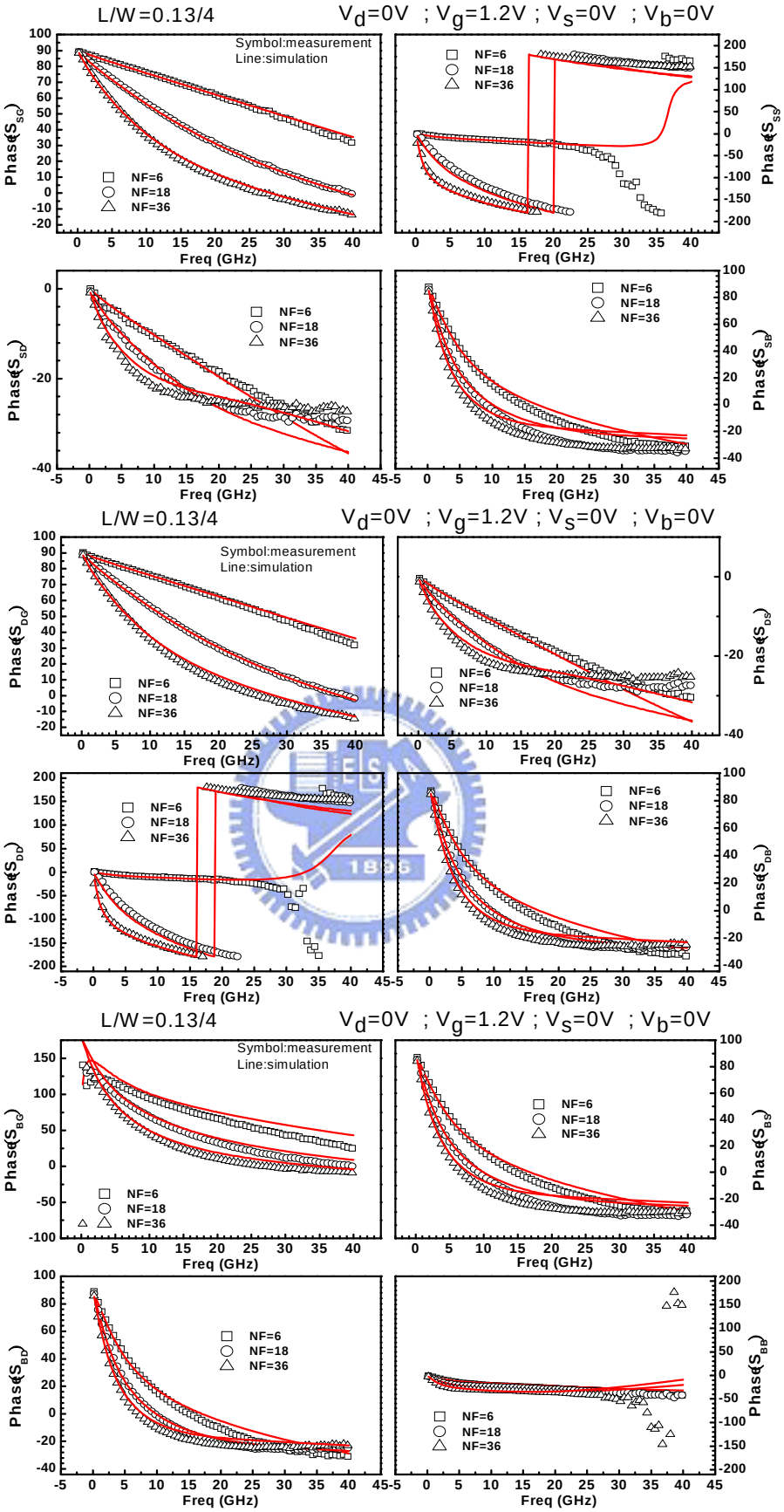
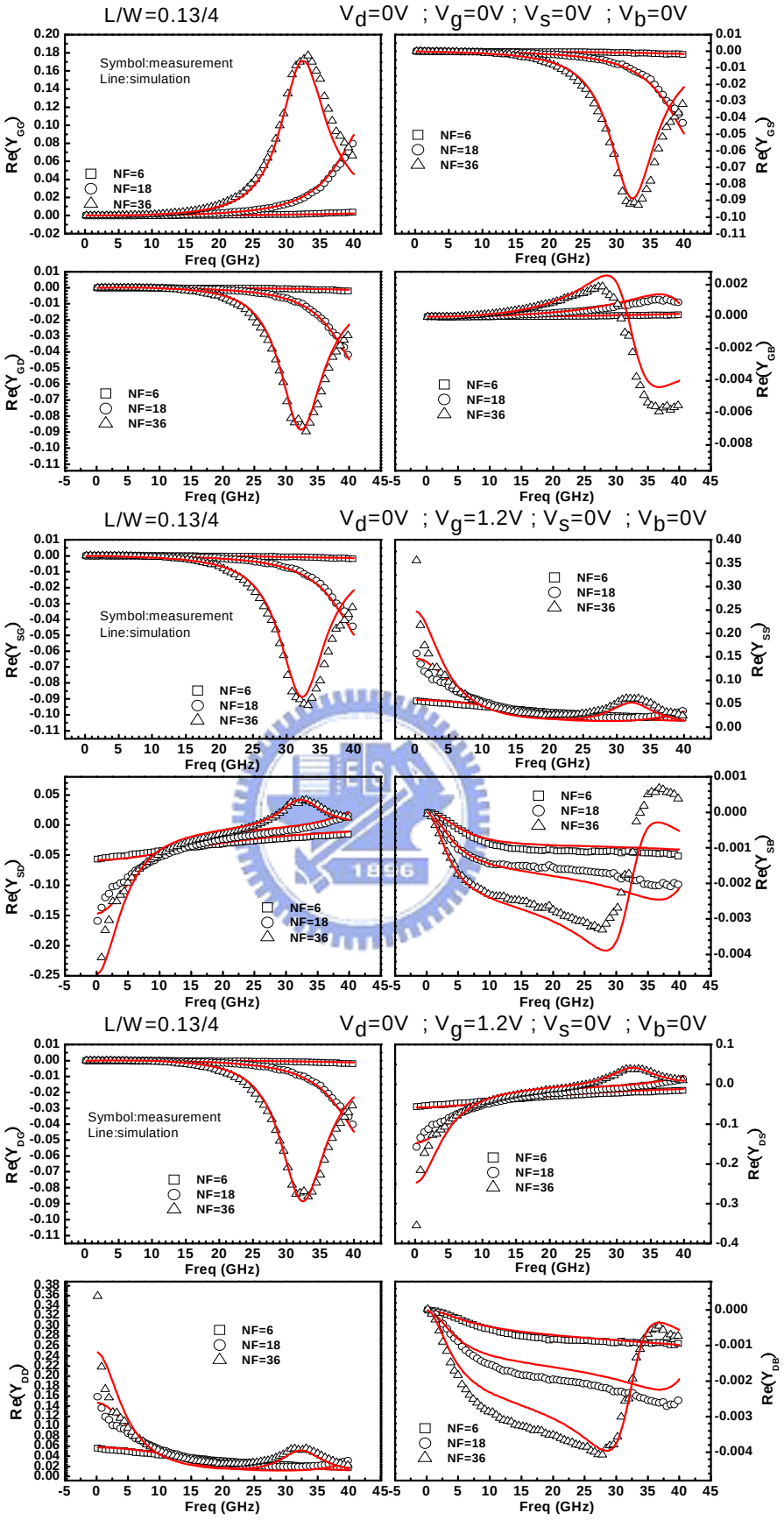


Fig. 5.11 The measured and simulated Phase(S) of 4-port devices at Vgs=1.2V, Vds=0V


L/W=0.13/4
V_d=0V ; V_g=0V ; V_s=0V ; V_b=0V
Symbol:measurement
Line:simulation
NF=6
NF=18
NF=36
Freq (GHz)
Re(Y_{GG})
Re(Y_{GS})
Re(Y_{GD})
Re(Y_{GB})
L/W=0.13/4
V_d=0V ; V_g=1.2V ; V_s=0V ; V_b=0V
Re(Y_{SG})
Re(Y_{SS})
Re(Y_{SD})
Re(Y_{SB})
L/W=0.13/4
V_d=0V ; V_g=1.2V ; V_s=0V ; V_b=0V
Re(Y_{DG})
Re(Y_{DS})
Re(Y_{DD})
Re(Y_{DB})

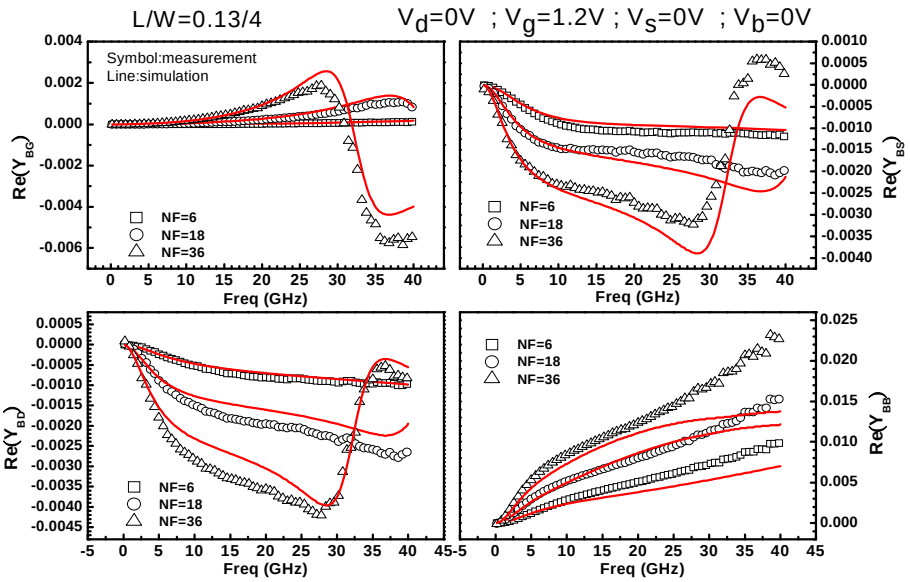
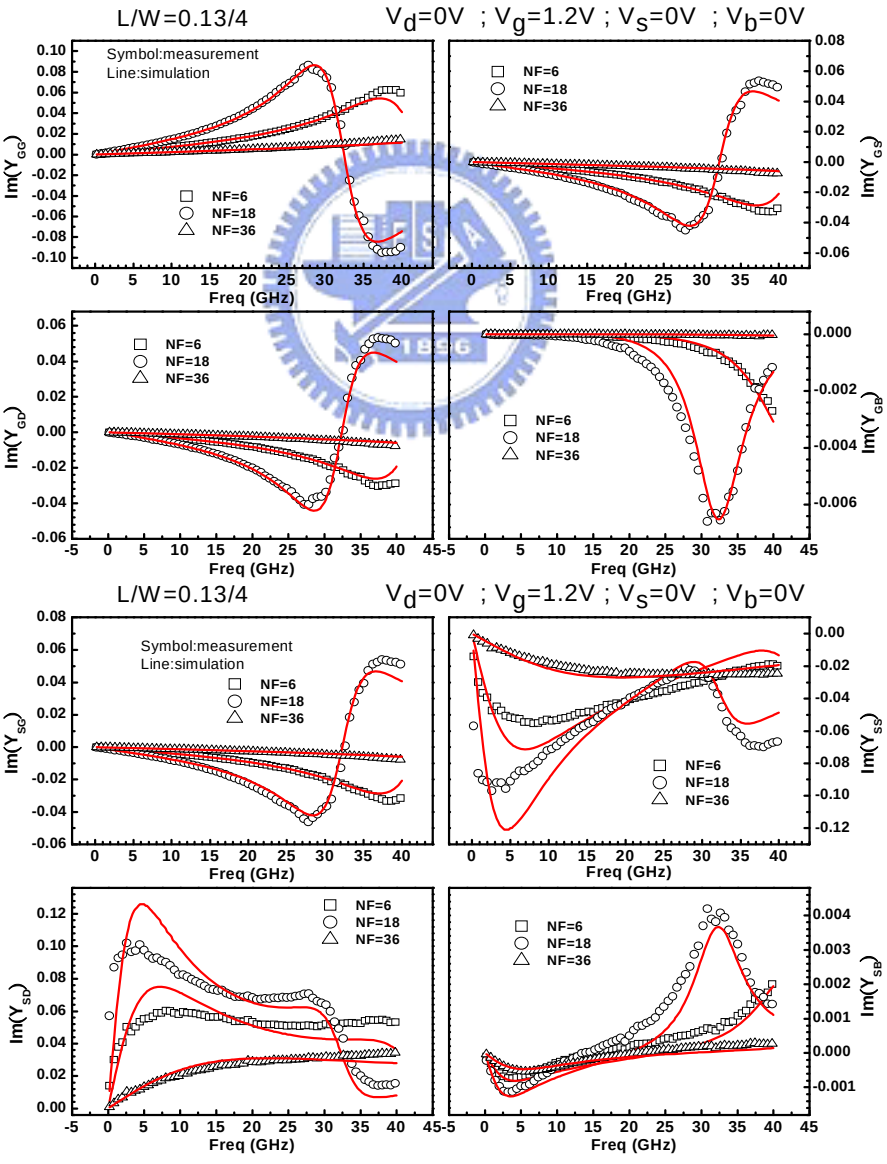


Fig. 5.12 The measured and simulated Re(Y) of 4-port devices at Vgs=1.2V, Vds=0V



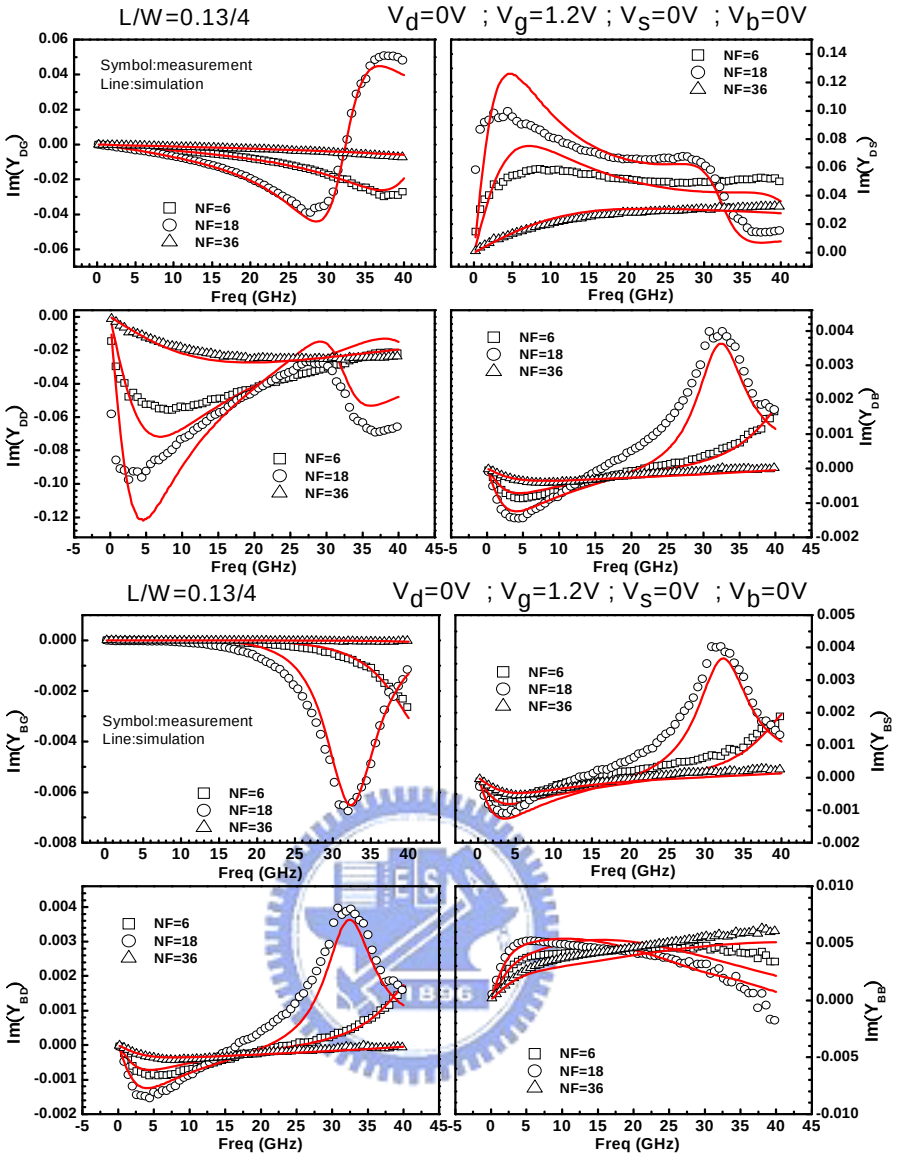


Fig. 5.13 The measured and simulated Im(Y) of 4-port devices at Vgs=1.2V,Vds=0V

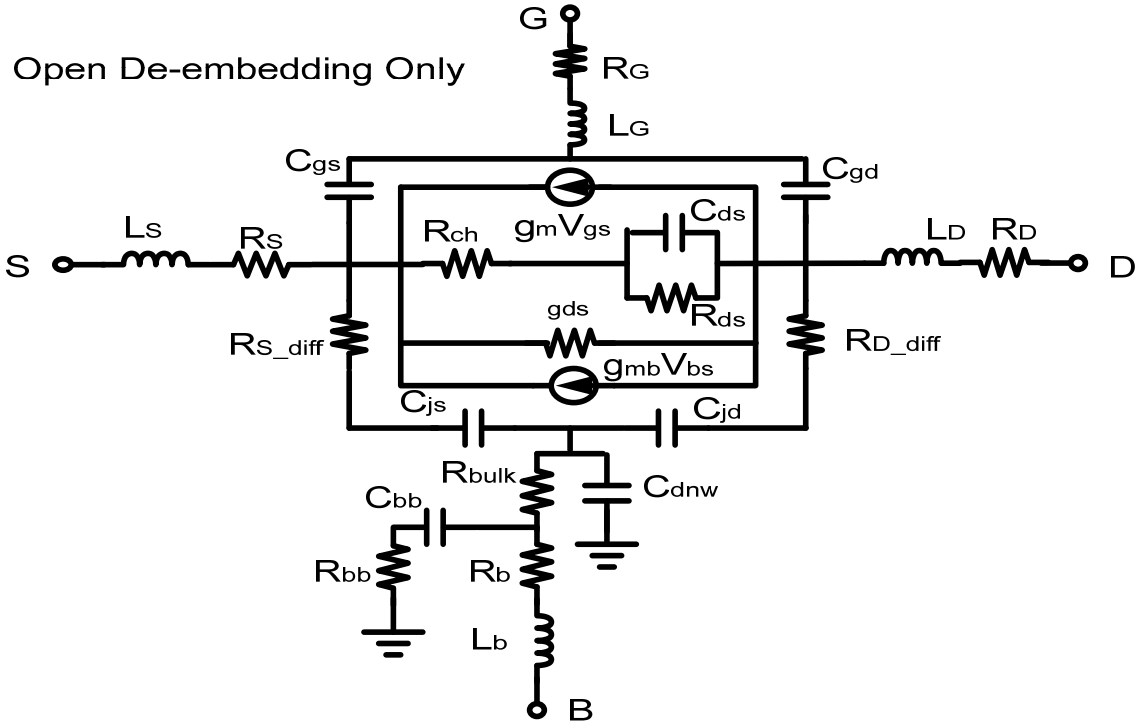
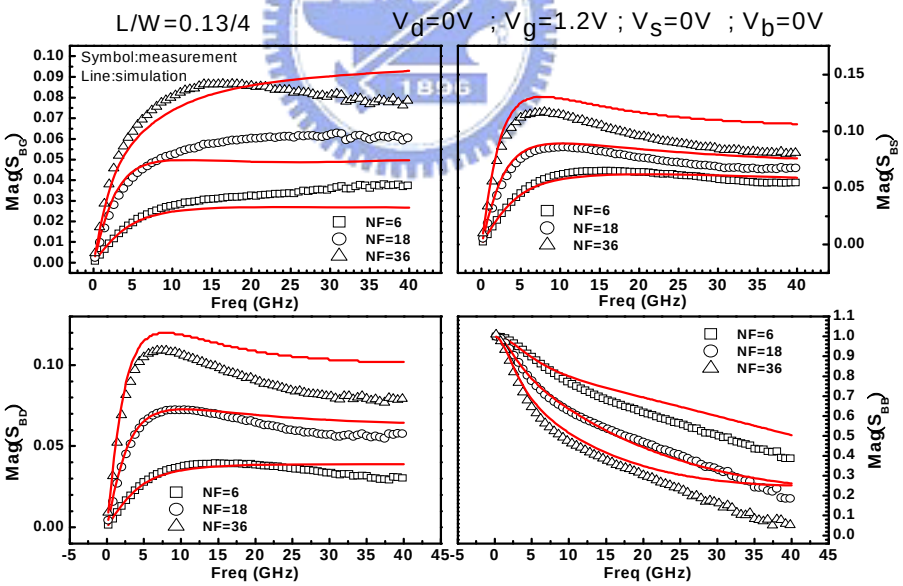


Fig. 5.14 The modified equivalent circuit of 4-port device at V_{gs}=1.2V, V_{ds}=1.2V



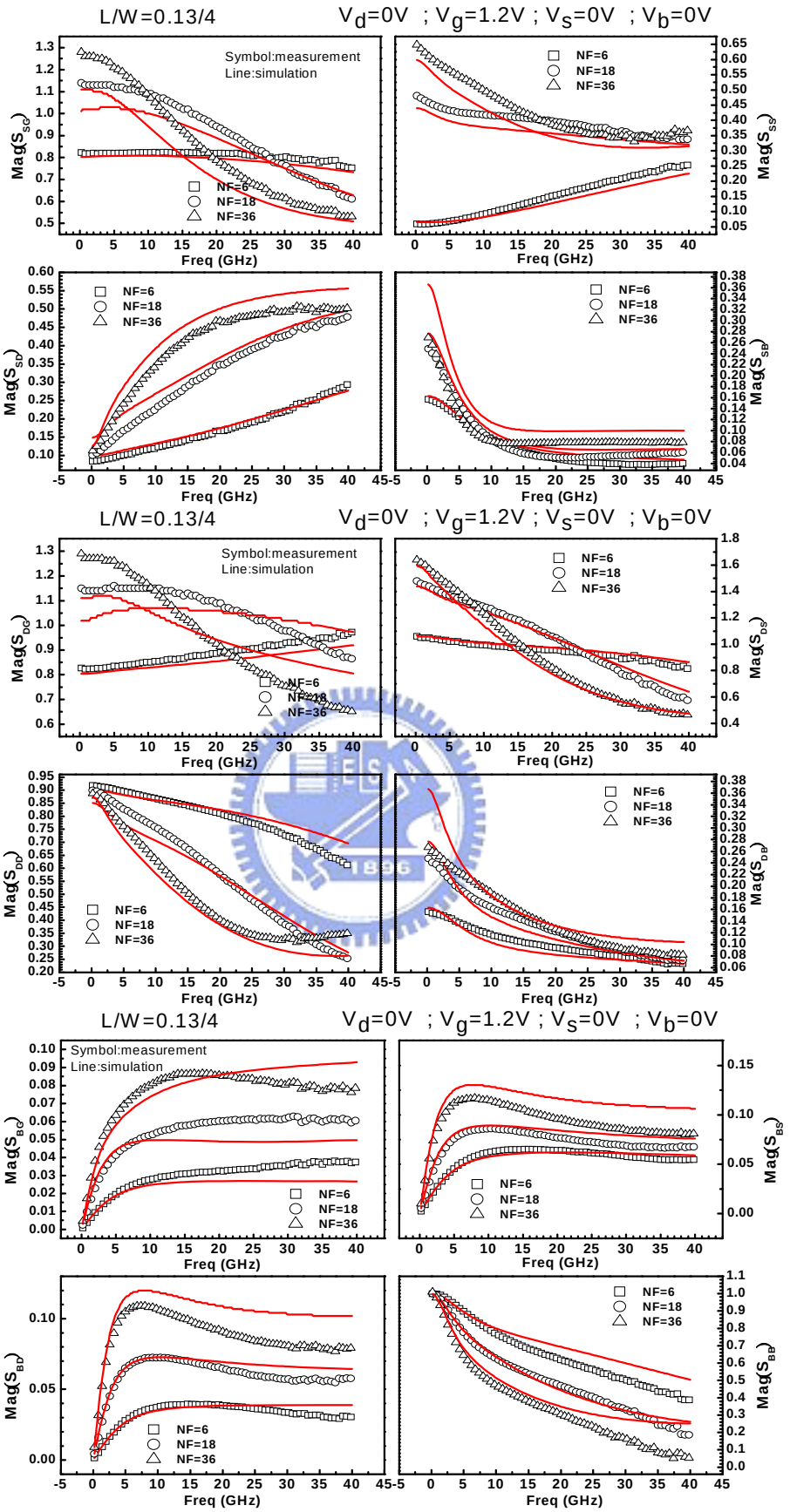
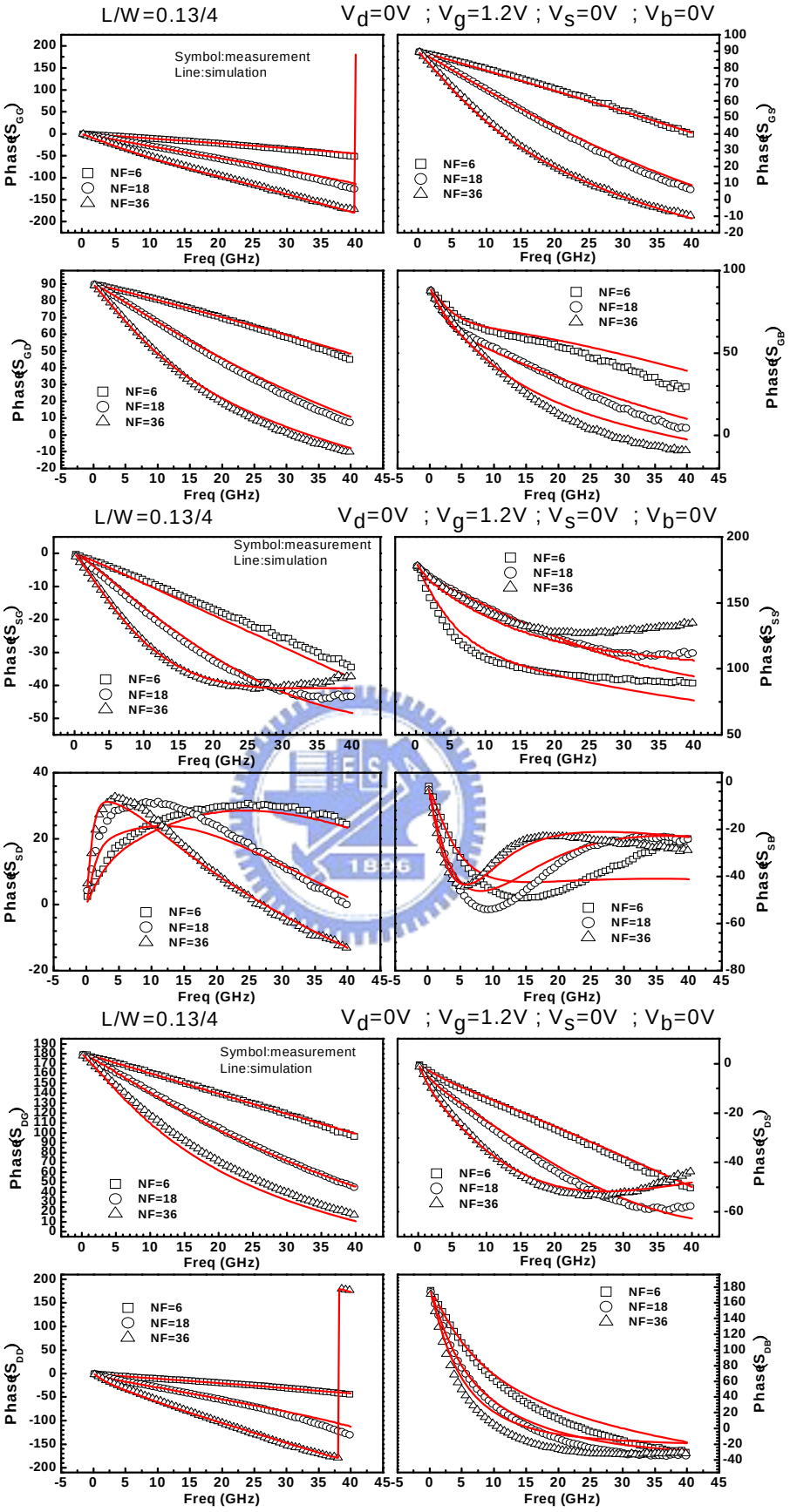


Fig. 5.15 The measured and simulated Mag(S) of 4-port devices at Vgs=Vds=1.2V


L/W=0.13/4
Vd=0V ; Vg=1.2V ; Vs=0V ; Vb=0V
Symbol:measurement
Line:simulation
NF=6
NF=18
NF=36
Freq (GHz)
Phase(SGG)
Phase(SGS)
Phase(SGD)
Phase(SGB)
Phase(SSG)
Phase(SSS)
Phase(SSD)
Phase(SSB)
Phase(SDG)
Phase(SDS)
Phase(SDD)
Phase(SDB)

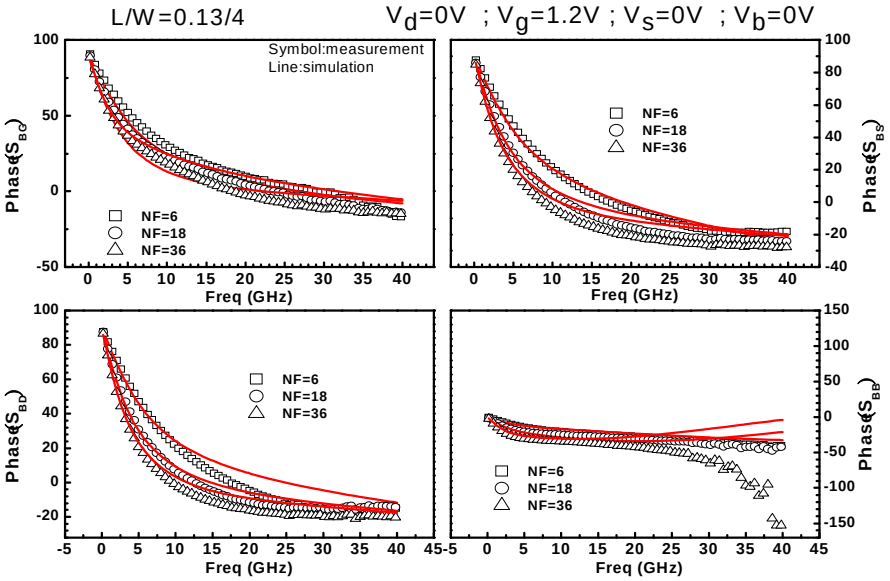
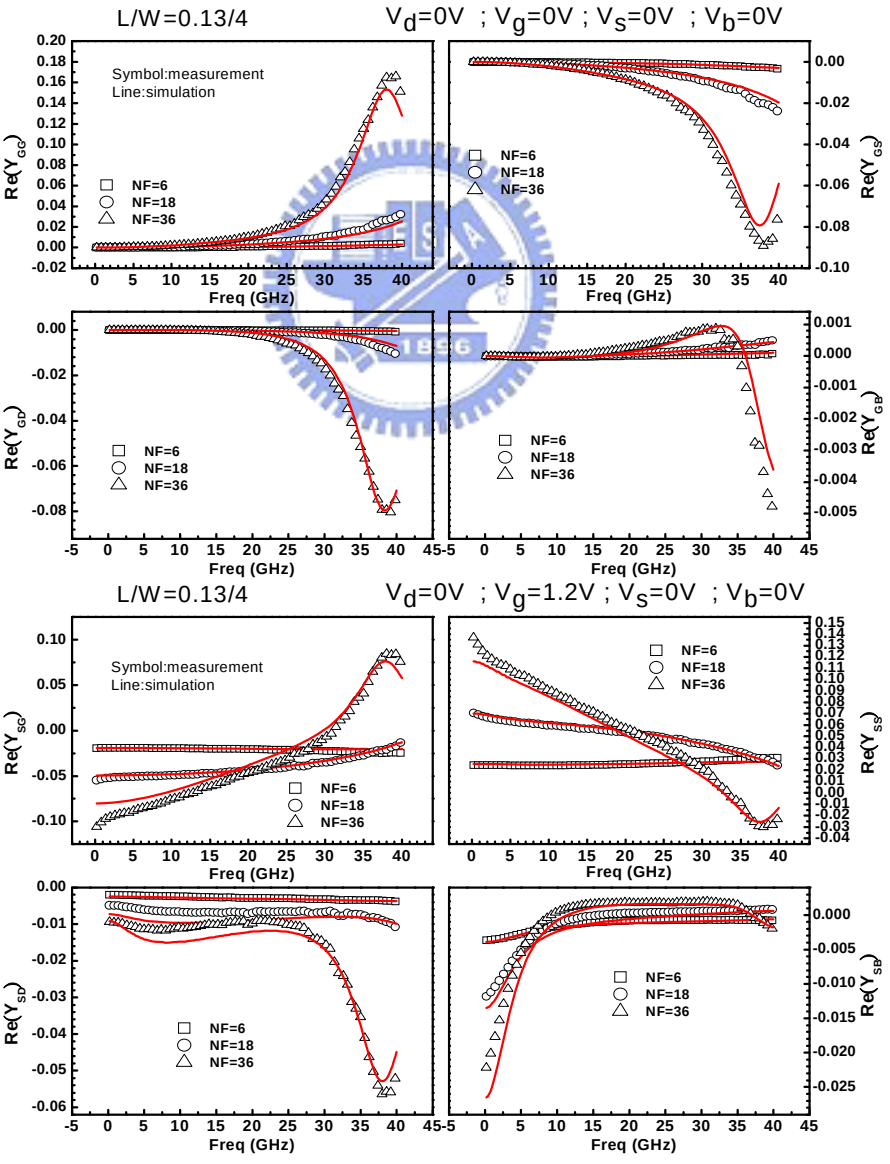


Fig. 5.16 The measured and simulated Phase(S) of 4-port devices at Vgs=Vds=1.2V



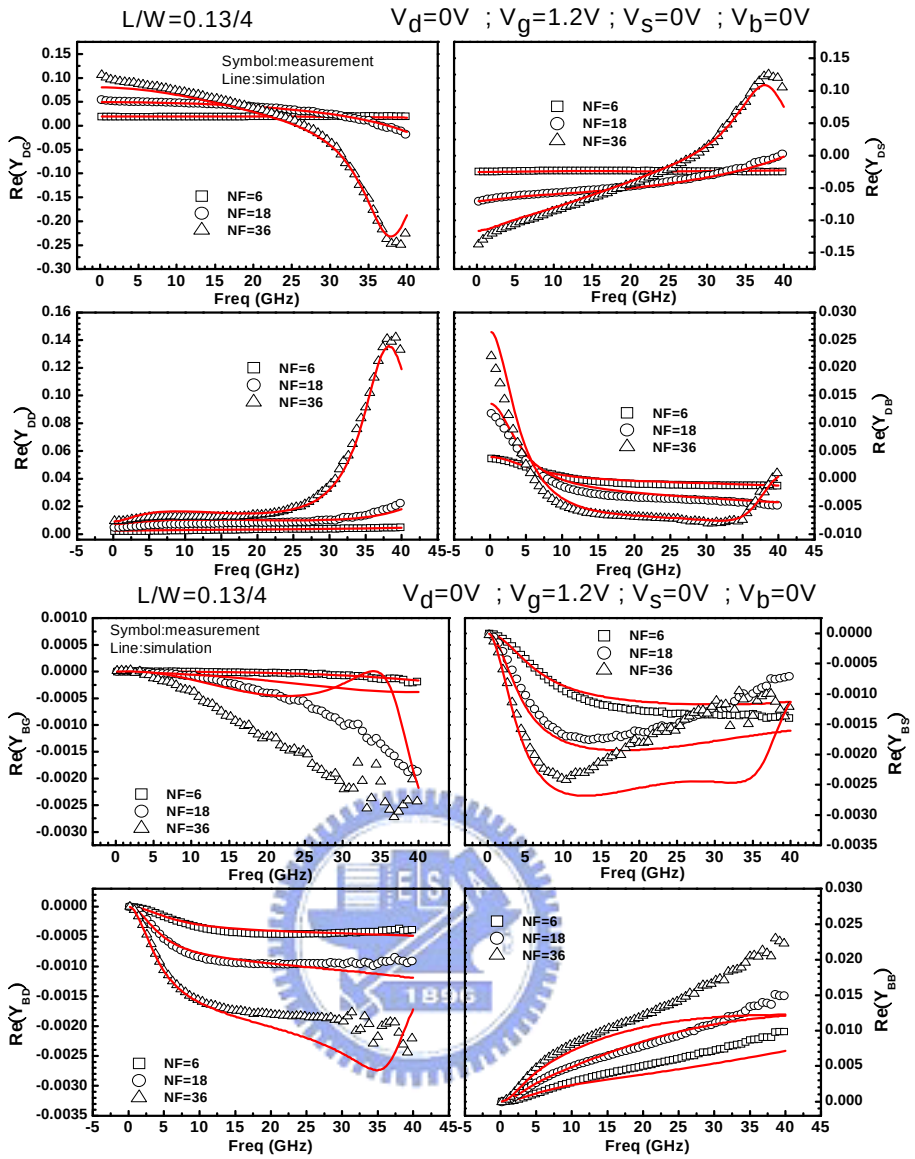
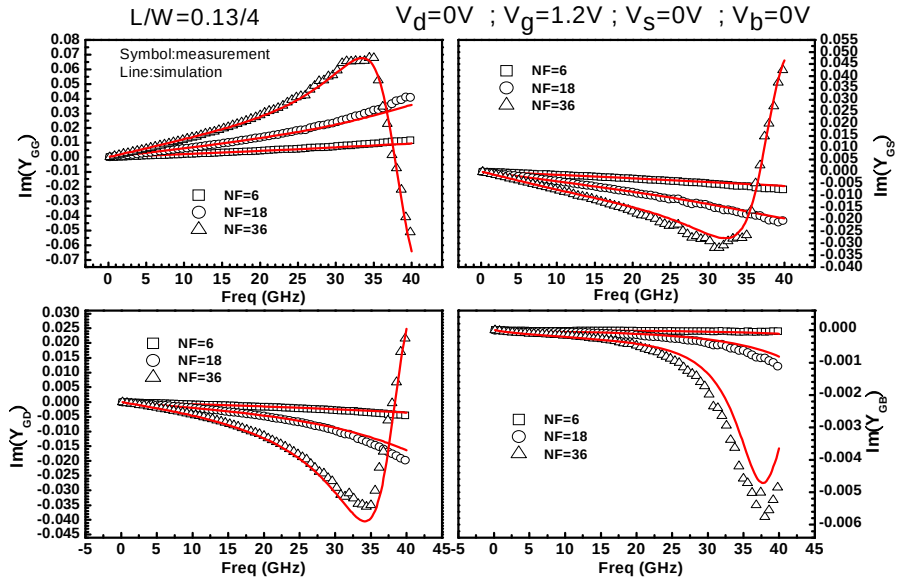


Fig. 5.17 The measured and simulated Re(Y) of 4-port devices at Vgs=Vds=1.2V



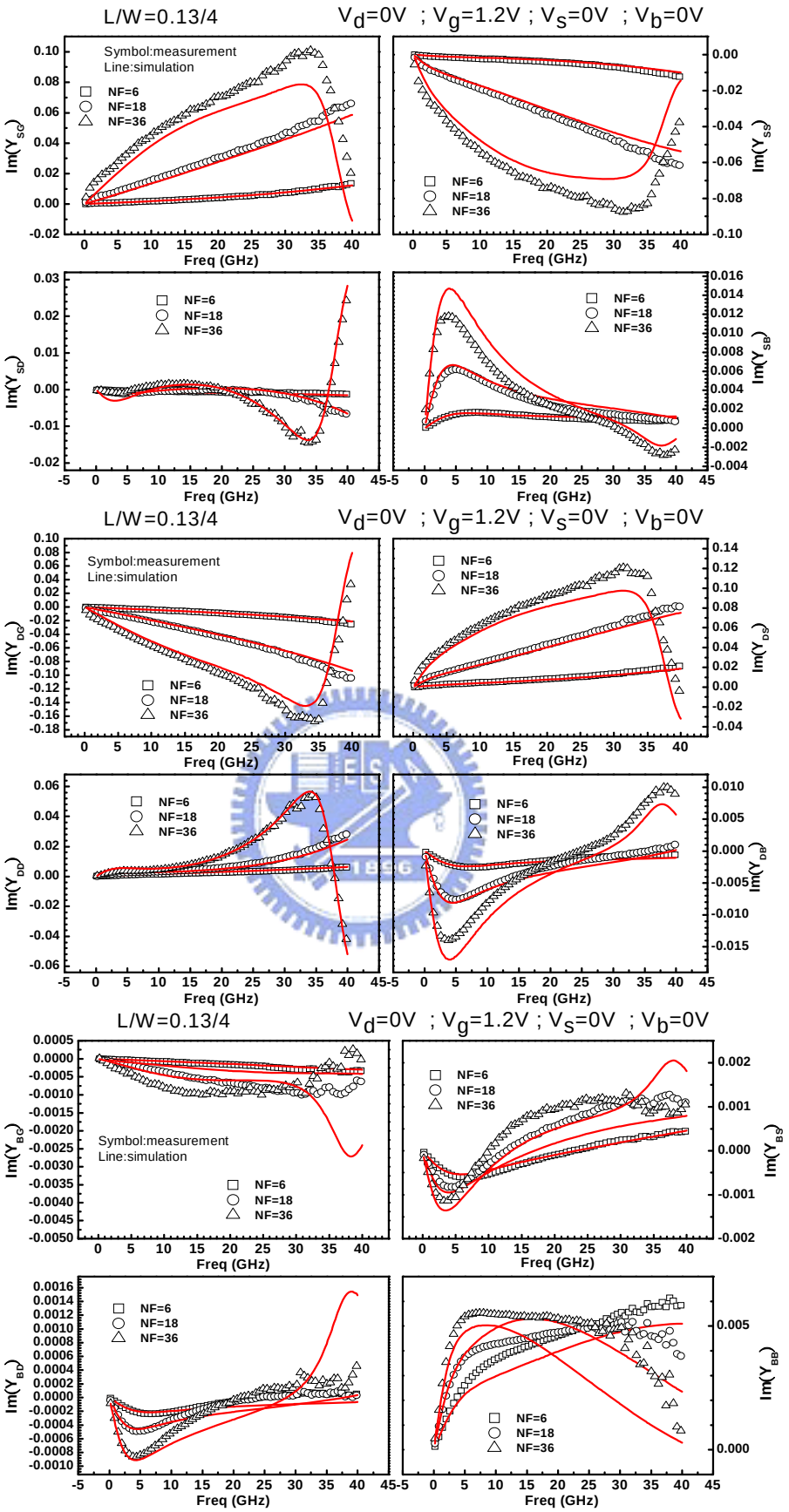


Fig. 5.18 The measured and simulated Im(Y) of 4-port devices at Vgs=Vds=1.2V

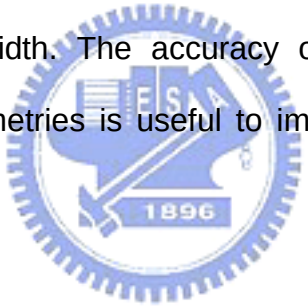
Chapter 6

Conclusions and Future Work

6.1 Conclusions

Base on the small signal equivalent circuit and model parameter extraction method are proposed previously in our laboratory, to develop the equivalent circuit and extraction method relevant to the test structures under various biases further, both two-port 3T and four-port 4T RF MOSFETs are covered in this work.

An extensive verification has been performed on the proposed small signal equivalent circuit models through simulation under various biases. The model parameters manifest a good scalability over gate lengths and gate finger numbers under a specified finger width. The accuracy over frequencies and biases and scalability over device geometries is useful to improve accuracy of high frequency circuit simulation.



6.2 Future Work

6.2.1 Parasitic resistance extraction

According to the equivalent circuit of short pad, the extracted resistance should be frequency independent, the extracted results show that the common part of resistance is almost const with the frequency, but the terminal resistance is not. To develop the parasitic resistance and inductance extraction method and the suitable dummy structure to de-embed in the future.

6.2.2 Substrate resistance extraction

Substrate resistance is a significant parameter for the MOSFET modeling, the

substrate network parameters extraction discussed in many researches, and it is a challenging issue for the accuracy extraction and modeling until now, it is mentioned that the substrate resistance effect the Im(Y24) and Im(Y34) with the frequency, in this study, substrate resistance extracted from the reduced 2x2 matrix, according to the equivalent circuit of four-port MOSFET, it is a feasible way to extract substrate resistance directly on four-port MOSFET in theory, even when the MOSFET operate at saturation region.

6.2.3 Small signal equivalent circuit with body biases

The equivalent circuit established in three kinds of different operate region, the simulation result is approximately match with measurement when Vds=0V, but the equivalent circuit operate at saturation region, the output impedance have to improve the extraction method and modified the equivalent circuit to make the accurate simulation behaviors.

According to four-port devices, introduction of the equivalent circuit establishment and the extraction method when Vbs=0V. it is necessary to develop the equivalent circuit when operate with body biases in the feature, it have to include the asymmetry channel phenomenon, transcapacitances, transconductance (gm, gds, g_{mb}), the complicated substrate networks and others physical mechanism parameters in the completed MOSFET small signal equivalent circuit modeling.

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