國 立 交 通 大 學

電子工程學系　　電子研究所

碩 士 論 文

原子層沉積高介電係數氧化鋁閘極介電層之鍺金氧半場效電晶體電物性研究

Electrical and physical characterization of Ge-MOSFETs with atomic-layer-deposited Al_2O_3 high-κ gate dielectric

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摘 要

我們已經利用原子層沉積技術（*Atomic layer depositon, ALD*）成功地製作出了以鍺為基版的金氧半場效電晶體；並且，透過電容結構（*Pt / ALD Al_2O_3 / p-type Ge / Al gate stacks*）電物性的研究分析，我們對於製作過程中鍺揮發的機制有了相當地了解。在我們所使用的原子層沉積系統裡，選擇三甲基鋁和水為金屬源和氧化劑。氧化鋁是一個相當有潛力的氧化物，它擁有和二氧化矽相當類似的特性以及大於二氧化矽約2.5倍的介電係數。我們藉由寫下的一條與反應物表面覆蓋程度和表面錯合物反應機率相關的式子模擬了一套原子層沉積系統可達到的成長速率。這條式子，對於我們實驗結果裡相對於已經發表的數據有較高的成長速率以及較高的最高速率沉積溫度做了合理的解釋。除了鍺揮發機制，我們也研究出了原子層沉積薄膜裡殘留物和捕捉缺陷（*trap*）以及氧化層固定電荷(*fixed oxide charge*）種類之間的相對關係。我們將會呈現前後一致有關於應用兩

種理論– 雙頻（*High-Low frequency, HLF*）以及電導（*Conductance, G-V*）–所得到的介面態位密度（*interface state density*）計算結果。經由這些在鍺電容結構電物性上的研究分析結果，我們發現一個不需任何後續熱處理和事前表面鈍化也可以在鍺基板上沉積少量鍺嵌入（*Ge-incorporated*）以及近乎當量化原子層沉積薄膜的溫度窗口（大約在*140 ~ 170 °C*之間）。

最後，我們陳列這些關於鍺基板金氧半場效電晶體的基本電性量測和指標參數粹取結果。高源集極串聯電阻、高介面態位密度、高摻雜物流失、和高接面漏電流是當處理這樣棘手基板時會遇到的主要議題。經由這些所粹取的指標性參數，在縮短通道長度的同時，我們看到了短通道效應（*short channel effect, SCE*）和反向短通道效應（*reverse short channel effect, SCE*）。壓軸出現的是鍺基板上等效載子遷移率（*effective mobility,* μ_{eff}）以及場效載子遷移率（*field effect mobility,* μ_{EF}）與矽基板電晶體的宇宙曲線（*universal curve*）比較結果。

Electrical and physical characterization of Ge-MOSFETs with atomic-layer-deposited Al_2O_3 high-κ gate dielectric

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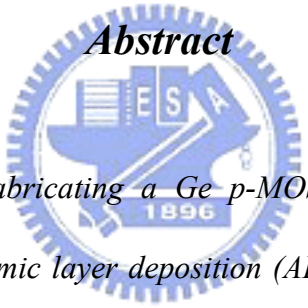

Abstract

We had succeeded in fabricating a Ge p-MOSFET with Al_2O_3 high-k gate dielectric deposited by an atomic layer deposition (ALD) system and figured out the whole story about the mechanism of Ge out-diffusion through the studies of Pt / ALD Al_2O_3 / p-type Ge / Al gate stacks by physical and electrical analyses in this research. In this ALD system, tri-methyl-aluminum (TMA), $Al(CH_3)_3$, and H_2O were chosen as the metal source and oxidant. Al_2O_3 is a very promising material shows similar properties and about 2.5 times dielectric constant of SiO_2. We wrote down an equation consists of surface coverage of the reactants and probability of formation of the TMA- and H_2O-related surface complexes to simulate the growth rate of an ALD system. By use of this equation, we explained reasonably the somewhat higher growth rate and highest growth rate temperature (T_{HGR}) in comparison to that reported in literatures.

Beside the mechanism of Ge out-diffusion, we also studied out the relationship between the residues and the type of the trap or the fixed oxide charge in an ALD film. We would show the consistent results of calculation of interface state density by two theories – High-Low frequency (HLF) and Conductance (G-V) methods. Through the studies of physical and electrical characteristics of the Ge-MOSCAPs, we found a window of temperature (about 140 ~ 170 °C) to deposit a less Ge-incorporated and almost stoichiometric ALD film on Ge without any post thermal treatment and prior surface passivation.

Finally, we showed those measurements of essential electrical performance and extraction of indicative parameters of the Ge p-MOSFETs. High source drain series resistance, interface state density, dopant lost, and junction leakage are the major issues when deal with such a nasty substrate. From the extracted parameters, we saw the short channel effect (SCE) and reverse short channel effect (RSCE) while decreasing the channel length. Effective mobility (μ_{eff}) and Field effect mobility (μ_{EF}) would also present in comparison to the universal curve related to Si-based transistors at last.

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效諭(rain)、搞笑脫線的欣哲、一整個好笑的敬倫、以及一整根的弘森。在儀器中心的同仁裡 — 蕭建男 博士，很謝謝您的指導、以及幫忙，謝謝您！志忠學長，謝謝你在 ALD 專業上的指導、資源的提供、以及做事態度的分享，謝謝您！鐵雄學長，謝謝你願意分享你的工作以及人生經驗，有你在，做實驗一點都不無聊，謝謝您！劉帥學長，謝謝你在 XRR 量測上的指導、資料的提供，很謝謝你的幫忙，沒有你，我的論文會失去好多色彩，謝謝您！致傑學長，你的搞笑幽默讓我 19 了！謝謝你常陪我做實驗、幫我照 TEM、帶來歡樂，祝福妳趕快脫離單身吧！每次看到你我就會 19 起來！謝謝您！健穎學長，你我本素昧平生，很謝謝你 AFM 量測上大力挺護，謝謝您！彬哥，謝謝您帶我去量 TEM，謝謝您！李博，謝謝你在議會上的陪伴、指導，你的說話方式讓人覺得很輕鬆、沒有壓迫，謝謝您！

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你們是我生命中最大的支柱，有你們，我的生命才能有意義！

劉峻丞

於 新竹交通大學

2007 年

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Introduction

1-1 General Background

In 1965, Moore predicted that in pursuit of a more convenient life would double the number of transistors per square inch on integrated circuits every two years [1]. This prediction observed over forty years later, referred to as "Moore's law," still upholds. To achieve this, transistor dimensions have been drastically downscaled, at the same time bettering the electrical performance. Making a comprehensive survey of the history of integrated circuits, many difficult challenges should be overcome while shrinking the dimensions of the transistor for pushing the technology node towards deep sub-0.1 um electronics generations. Specifications, required for every technology generations, outlined by the International Technology Roadmap for Semiconductors (ITRS) (consult Table 1-1) [2] indicate that there is no solution known for a variety of critical technologies. In particular, it is clear that today's gate dielectric material, silicon dioxide (SiO_2), will soon reach the predicted limits of scaling process. In order to relax several progressively worse physical limitations associated with device scaling engineering, alternative materials and novel device

structures are being researched. Because of the thickness of conventional SiO_2 less than 1.5 nm, i.e., around three atomic layers in the film, carriers transporting through the gate oxide via direct tunneling results in the exponential increase of gate leakage current. The resulting leakage current increases the power dissipation and deteriorates the device performance as well as the circuit stability for VLSI application. Therefore, pushes the progress of research in high-k material base on the concept of increasing the physical thickness of gate insulator while maintaining the same equivalent oxide thickness (EOT) without diminishing the performance of devices. However, because of the poor interface, significant inter-diffusion and chemical reaction related to the instability of some high-k materials; it is required to form an extra interfacial layer between a high-k gate insulator and a Si substrate to eliminate those issues. In addition, unfortunately, another more critical property of high-k materials is that the energy band-gap is inversely proportional to the dielectric constant in most high-k materials. Therefore, in spite of the alleviation of leakage current through the application of high-k materials, the narrower energy band-gap, smaller band offset, and defectiveness of composition will severely enhance Schottky emission of carriers, Frenkel-Poole emission, trap-assisted tunneling, and the hopping effect compared with SiO_2 and, consequently, increase the gate leakage instead. Thus, there are some criteria and requirements tabulated in Table 1-2 for

guiding the researcher to better choices of high-k gate dielectrics. Besides high-k materials and metal gates, replacing the traditional SiO_2 and poly-Si as transistor dielectric and gate material, respectively, high mobility substrate is another feasible way to replace silicon as channel material further increasing transistor speed. Figure 1-1, the room temperature properties of semiconductors, shows that germanium (Ge) and gallium Arsenide (GaAs) etc…substrate having higher carrier mobility might be the main stream substrate materials in the future semiconductor researches.

On the other hand, developments in the future microelectronics industry will be critically dependent on progress in ultra-thin film deposition technology, in particular, that will require the deposition of gate oxide films as thin as several angstroms. The ability to grow thin oxide films for use as dielectrics and insulators will be central to silicon processing. In addition to elegant thickness control, it will be substantial to have the ability to deposit conformal films on three-dimensional structures with high aspect ratios in future dynamic random access memory (DRAM) technology. To the end of thin film processing limitation is the deposition of only one monolayer to control precisely the film thickness and simultaneously maintain conformal deposition on three-dimensional structures.

Atomic layer controlled deposition technique provides the means to achieve conformality and precise thickness control. The development of atomic layer

controlled growth has been a major focus of recent research. For atomic layer epitaxy (ALE) or atomic 1ayer processing (ALP) of two-component films from elemental molecular sources, the adsorption of each element showing self-regulating and up to a full monolayer, by means of self-terminating surface reactions, can be employed to deposit a acceptable film in every deposition cycle. One advantage of the employ of atomic layer controlled growth is that the surface reaction kinetics should not affect the film growth rate. The only requirements for ALE or ALP are that the surface temperature and reactant exposure must be sufficient for a complete reaction everywhere on the substrate. Atomic layer deposition is getting attention recently. It could be applied to gate insulator technique and inner connector engineering whatever the thickness of gate dielectric and aspect ration of trench you meet and might be one of the solutions in the electronics generations later.

1-2 Motivation – Why atomic-layer-deposited Al_2O_3 Gate Dielectric on Germanium Substrate ?

Based on the first order current-voltage approximation, the drive current I_{DS} for a MOSFET can be showed as below

$$I_{DS} = \frac{1}{2} C_{ox} \mu_n \left(\frac{W}{L_{eff}} \right) (V_{GS} - V_{th})^2 \qquad (1.1)$$

Where C_{ox} is the gate oxide capacitance and mainly determined by the permittivity and the thickness of the gate insulator. μ_n is the mobility for the electrons or holes, W is the channel width, L_{eff} is the effective channel length, V_{GS} is the applied gate-to-source voltage, and V_{th} is the threshold voltage. All the parameters in the above formula can be properly adjusted to further improve the device driving capability for fulfilling the specification expected.

On grounds of the formula mentioned above, we proceeded to study how to tune the two parameters, C_{ox} gate capacitance and μ_n substrate carrier-mobility, through the uses of a high-k gate insulator, aluminum oxide (Al_2O_3), and a high-mobility substrate material, germanium (Ge), in substitution for the traditional device conformation, being about to go out of use some day, to catch up with the coming of new electronics industry era. The choice of Ge substrate forces us in face of two major issues─ illness Ge native oxide and narrower energy band-gap. The problem

involved in an unsound native oxide not only deforms the interface and the gate-stack integrity, but also restrains the temperatures selected for activation process following the ion implantation to define the source-drain (S/D) regions. Additionally, since the probability of higher junction leakage current resulted from a narrower band-gap of Ge, increases the difficulties to trade off an adequate activation temperature. Incomplete dopant activation might trigger the increase of junction leakage through Frenkel-Poole emission, trap-assisted tunneling, and the hopping effect, etc…but, because of the illness Ge native oxide, would poor the gate-stack conformation as choose a higher activation temperature.

In this research, the most special thing is the exploitation of an atomic layer deposition system to form a gate insulator for excellent thickness and conformality control. We exploit an ALD system to grow Al_2O_3 by uses of tri-methyl-aluminum $Al(CH_3)_3$ (TMA) and H_2O two molecular vapor reactants based on the mechanism─self-limiting atomic layer controlled growth [3.4]. The precursors utilized allow us to receive a film grown at a relatively low growth temperature. The growth mechanism associated with (A) and (B) reactions [4] can define the ABAB... binary reaction sequence chemistry. One advantage of the ABAB... binary reaction sequence approach is that the surface reaction kinetics should not affect the film growth rate.

We chosen the Al_2O_3 as the gate insulator not only for his energy band-gap,

showed in Figure 1-2 illustrating the band-gap and band alignment for several high-k gate dielectrics calculated by Robertson [5], wide enough to be compared to SiO_2, but also for the favorable conduction barrier high, tabulated in Table 1-3 [6], whatever the substrate materials are applied. Most high-k materials that have other desirable properties do have relatively low band offsets and small band-gaps and show unstable thermal characteristics. Al_2O_3 is probably the only material that has a band-gap, band alignment and thermal stability similar to those of SiO_2. Especially, it also shows adequate valence barrier high to block the direct tunneling leakage current related to hole transportation as we use Ge as substrate for its mobility about 2.5x (~ 3900 $cm^2/V \cdot s$ for electron) and 4x (~ 1900 $cm^2/V \cdot s$ for hole), respectively, better than a silicon substrate (~ 1500 $cm^2/V \cdot s$ and ~ 450 $cm^2/V \cdot s$).

1-3 Organization of This Thesis

In chapter 2, at the beginning, we studied the physical properties of the metal-oxide-semiconductor (MOS) capacitances with different post thermal treatments and atomic-layer deposited Al_2O_3 films on Ge substrates for paving the way for an achievement of a Ge MOSFET. Various material analysis techniques, such as Ellipsometer, Atomic Force Microscopy (AFM), Angle-Resolved X-ray Photoelectron Spectroscopy (AR-XPS), Grazing Incidence X-ray Reflectivity (GI-XRR), Secondary Ion Mass Spectroscopy (SIMS), High Resolution Transmission Electron Microscopy (HRTEM) and Electron Dispersive Spectra (EDS) were performed to observe the surface morphology, gate stack composition, and the physical thickness of the ALD-Al_2O_3 for calculation of EOT after the formation of such a MOSCAP gate stack. Beside studies of the effect of post thermal treatments, we also showed the impact of different deposition temperatures of ALD-Al_2O_3 on the physical characteristics of those Pt / ALD Al_2O_3 / p-type Ge / Al capacitances and claimed a possible growth mechanism along with an equation as a function of temperature behind an atomic layer deposition system. We established a five layers model to simulate the composition, density, and interface roughness of those MOSCAPs by use of the software ─ Mercury. The results of the simulation were

confirmed with the help of Grazing-Incidence X-Ray Reflectivity (GIXRR), Secondary Ion Mass Spectroscopy (SIMS), Atomic Force Microscopy (AFM), X-ray Photoelectron Spectroscopy (XPS), and High Resolution Transmission Electron Microscopy (HRTEM). By this, we had figured out the Ge out-diffusion mechanism in this chapter, too.

In chapter 3, we illustrated all the essential measurements of electrical performance of Ge MOSCAPS had been studied in chapter 2. We also did the calculation of the interface state by Conductance-Voltage (G-V) and high-low frequency method and further improved it by 300 °C forming gas annealing. We studied out the relationship between the residues and the type of trap and fixed oxide charge through studies of trap behavior.

In chapter 4, we first demonstrated a Ge P-MOSFET by conventional four masks process with aluminum (Al) gate and boron implanted source-drain. It showed the most critical step of this process ─ the P-N junction engineering, and the limitation of the performance of such conventional transistor fabrication. Indicative parameters were extracted for judge by the performance of those MOSFETs more professionally. It showed the difficulty to eliminate high junction leakage current, high interface state density, high source drain series resistance, and high dopant lost. Various kinds of mobility were calculated in comparison to that on Si-based transistors.

In chapter 5, finally, it gave the conclusions and suggestions of this thesis for the future work.

Table 1-1. INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2006 UPDATE PROCESS INTEGRATION, DEVICES, AND STRUCTURES
High-Performance Logic Technology Requirements—Near-term

ITRS 2006

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*
EOT (A) *(Equivalent Oxide Thickness)*	*12*	*11*	*11*	*10*	*9*	*6.5*	*5*
$I_{d,sat}$ (μA/μm) *(Effective NMOS Drive Current)*	*1.02E+03*	*1.13E+03*	*1.20E+03*	*1.21E+03*	*1.18E+03*	*2.05E+03*	*2.49E+03*
$J_{g,limit}$ (A/cm^2) *(Maximum Gate Leakage Current Density)*	*1.88E+02*	*5.36E+02*	*8.00E+02*	*1.18E+03*	*1.10E+03*	*1.56E+03*	*2.00E+03*
τ = CV/I (ps) *(NMOSFET Intrinsic Delay)*	*0.87*	*0.74*	*0.64*	*0.54*	*0.51*	*0.4*	*0.34*

Manufacturable solutions are known

Manufacturable solutions are NOT known

Table 1-2. Criteria nad Material Requirement of High-k Gate Dielectrics.

Criteria	*Requirements*
EOT scalability <10Å	*Dielectric constant > 15*
Negligible FIBL effect	*Dielectric constant < 60*
Leakage current < 1 A/cm^2	*Bandgap > 5 eV, Barrier height > 1 eV*
Thermal stability	*No silicidation and reduction*
Hysteresis	*< 20 mV*
Dispersion	*< 1 % /decade*
Interface state density	*< 10^{11} /eV cm^2*
Mobility	*> 85 % of SiO_2*
Reliability	*> 10 years*

Room temperature properties of semiconductors

Quantity	*Symbol*	*Ge*	*Si*	*InAs*	*InP*	*GaAs*	*GaP*	*GaN*	*(Unit)*
Crystal structure		D	D	Z	Z	Z	Z	W	–
Gap: Direct (*D*) / Indirect (*I*)		*I*	*I*	*D*	*D*	*D*	*I*	*D*	–
Lattice constant	a_0 =	5.64613	5.43095	6.0584	5.8686	5.6533	5.4512	a_0 = 3.189 c_0 = 5.185	Å Å
Bandgap energy	E_g =	0.66	1.12	0.354	1.35	1.42	2.26	3.4	eV
Intrinsic carrier concentration	n_i =	2×10^{13}	1×10^{10}	7.8×10^{14}	1×10^{7}	2×10^{6}	1.6×10^{0}	1.9×10^{-10}	cm^{-3}
Effective DOS at CB edge	N_c =	1.0×10^{19}	2.8×10^{19}	8.3×10^{16}	5.2×10^{17}	4.4×10^{17}	1.9×10^{19}	2.3×10^{18}	cm^{-3}
Effective DOS at VB edge	N_v =	6.0×10^{18}	1.0×10^{19}	6.4×10^{18}	1.1×10^{19}	7.7×10^{18}	1.2×10^{19}	1.8×10^{19}	cm^{-3}
Electron mobility	μ_n =	3900	1500	33,000	4600	8500	110	1500	cm^2/Vs
Hole mobility	μ_p =	1900	450	450	150	400	75	30	cm^2/Vs
Electron diffusion constant	D_n =	101	39	858	120	220	2.9	39	cm^2 / s
Hole diffusion constant	D_p =	49	12	12	3.9	10	2	0.75	cm^2 / s
Electron affinity	χ =	4.0	4.05	4.9	4.5	4.07	3.8	4.1	V
Minority carrier lifetime	τ =	10^{-6}	10^{-6}	10^{-8}	10^{-8}	10^{-8}	10^{-6}	10^{-8}	s
Electron effective mass	m_e* =	1.64 m_e	0.98 m_e	0.022	0.08 m_e	0.067 m_e	0.82 m_e	0.20 m_e	–
Heavy hole effective mass	m_{hh}* =	0.28 m_e	0.49 m_e	0.40	0.56 m_e	0.45 m_e	0.60 m_e	0.80 m_e	–
Relative dielectric constant	ε_r =	16.0	11.9	15.1	12.4	13.1	11.1	8.9	–
Refractive index	$\overline{n}$ =	4.0	3.3	3.5	3.4	3.4	3.0	2.5	–
Absorption coefficient near E_g	α =	10^3	10^3	10^4	10^4	10^4	10^3	10^5	cm^{-1}

- D = Diamond. Z = Zincblende. W = Wurtzite. DOS = Density of states. VB = Valence band. CB = Conduction band
- The Einstein relation relates the diffusion constant and mobility in a nondegenerately doped semiconductor: $D = \mu\,(k\,T / e)$
- Minority carrier diffusion lengths are given by $L_n = (D_n\tau_n)^{1/2}$ and $L_p = (D_p\tau_p)^{1/2}$
- The mobilities and diffusion constants apply to low doping concentrations ($\approx 10^{15}$ cm^{-3}). As the doping concentration increases, mobilities and diffusion constants decrease.
- The minority carrier lifetime τ applies to doping concentrations of 10^{18} cm^{-3}. For other doping concentrations, the lifetime τ is given by $\tau = B^{-1}\,(n + p)^{-1}$, where $B_{GaAs} = 10^{-10}$ cm^3/s and $B_{Si} = 10^{-12}$ cm^3/s.

Fig. 1-1 Room temperature properties of semiconductors.

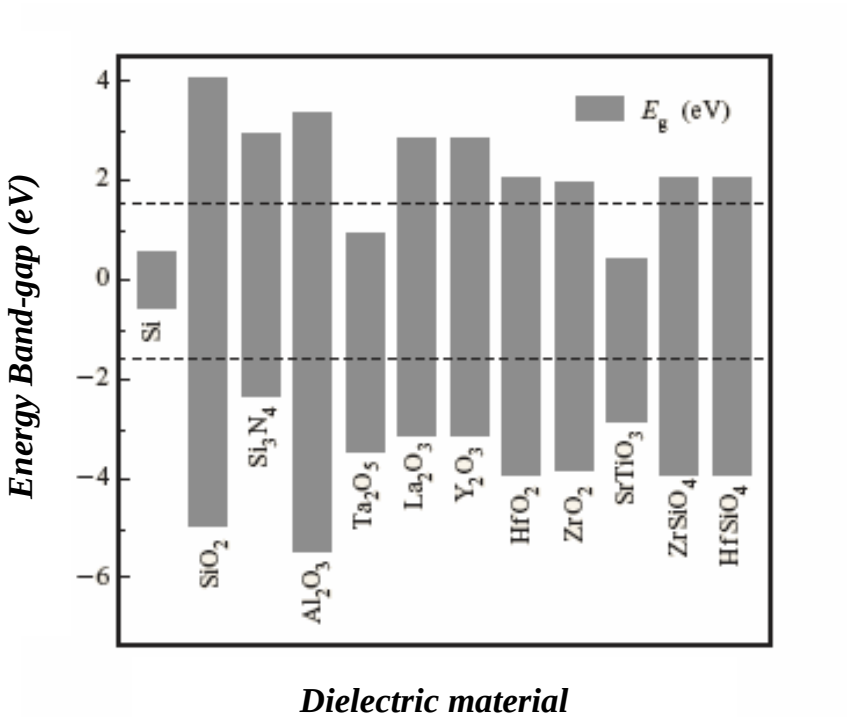


Fig. 1-2 Energy Band-gap and band alignment of high-k gate dielectrics with respect to silicon.

Table 1-3. The calculated conduction band offsets for different high-k dielectrics on variety substrate materials.

	HfO_2	ZrO_2	$HfSiO_4$	La_2O_3, Y_2O_3, Sc_2O_3	$LaAlO_3$	$SrTiO_3$	Ga_2O_3	Gd_2O_3	Si_3N_4	Al_2O_3
Si	1.48	1.4	2.03	2.36	1.53	0.11	0.83	2.21	1.7	2.6
Ge	1.68	1.63	2.2	2.56	1.72	0.37	1.03	2.44	1.9	2.8
AlP	0.65	0.68	1.12	1.53	0.70	−0.49	0.03	1.5	0.85	1.7
GaP	0.77	0.73	1.3	1.65	0.82	−0.52	0.13	1.54	1.0	1.9
InP	1.74	1.64	2.3	2.6	1.79	0.33	1.08	2.45	1.97	2.9
AlAs	1.05	1.0	1.6	1.9	1.1	−0.27	0.4	1.8	1.27	2.2
GaAs	1.51	1.42	2.1	2.4	1.55	0.1	0.86	2.23	1.90	2.7
InAs	2.48	2.44	3.0	3.35	2.52	1.19	1.84	3.24	2.7	3.6
AlSb	1.05	0.98	1.6	1.9	1.1	−0.3	0.4	1.8	1.28	2.2
GaSb	1.58	1.53	2.12	2.46	1.63	0.27	0.94	2.34	1.8	2.7
InSb	2.18	2.14	2.7	3.06	2.23	0.9	1.54	2.95	2.4	3.3
AlN	−1.5	−1.5	−1.05	−0.64	−1.5	−2.65	−2.1	−0.7	−1.3	−0.5
GaN	1.09	1.1	1.57	1.97	1.13	−0.1	0.46	1.9	1.3	2.16
InN	2.9	3.0	3.4	3.8	3.0	1.8	2.3	3.8	3.1	4.0
SiC 3C	1.65	1.49	2.27	2.53	1.70	0.12	0.98	2.3	2.08	2.98
SiC 6H	1.07	0.94	1.66	1.94	1.11	−0.4	0.4	1.75	1.5	2.35
ZnO	2.2	2.2	2.7	3.1	2.2	0.8				

Chapter 2

Physical characteristics of atomic-layer-deposited Al_2O_3 on Ge substrate

2-1 Introduction

In view of the clean technique and the knowledge of intrinsic properties of Ge investigated by C. C. Cheng et al. [7-8], we preferred a low temperature technique to suppress the instable thermal properties of Ge substrate material while depositing the gate dielectrics on it. An atomic-layer-deposition (ALD) system is a good candidate to achieve this requirement. Figs. 2-1~2-5 present the ALD mechanism [9]. Taking advantage of the self-cease reaction cycles [10], we could deposit the gate dielectrics in a layer-by-layer manner with very good step coverage and atomic-scale uniformity. Taking the film quality into account, although it should be better to grow the film at deposition temperature higher than 200 °C [4], we could only receive a good Al_2O_3/Ge interface below 200 °C in our study. In addition, the conventional techniques, such as plasma enhancement [11] and ozone precursor in place of H_2O [12-14], have also been studied recently to further decrease the deposition temperature by lowering the reaction barrier or increasing the chemical activity of the

reactants. We chose Al_2O_3 as our high-k gate insulator for the reasons that Al_2O_3 and SiO_2 showed similar properties such as high energy band-gap, high thermal stability [15], good conduction and valence band alignments not only on Si but also Ge. In chapter 2, we focus ourselves on the characteristics of atomic-layer-deposited Al_2O_3 films with different deposition temperatures on Ge substrate with 60 cycles and analyze the electrical performance until chapter 3 based on these observations. On the basis of studies in chapter 2 and 3, we could chose a good condition to form the gate dielectrics for fabricating the Ge MOSFETs studied in chapter 4. By uses of the physical analysis, such as Ellipsometer (EP), Atomic Force Microscopy (AFM), Angle-Resolved X-ray Photoelectron Spectroscopy (AR-XPS), Grazing Incidence X-ray Reflectivity (GI-XRR), Secondary Ion Mass Spectroscopy (SIMS), High Resolution Transmission Electron Microscopy (HRTEM) and Electron Dispersive Spectra (EDS), we showed the thermal and intrinsic properties of the ALD Al_2O_3 films that revealed the effects of the growth and annealing temperature on the interface roughness and the compositions of the Al_2O_3 films. What deserves to be mentioned is that we figured out the growth mechanism as a function of deposition temperature through the studies of the effects of different deposition temperatures on the thickness of the ALD dielectrics. We would also show the relationship between the physical properties and the essential electrical performance in chapter 3; and did further

calculation of the interface states along with the modeling result from the GIXRR measurements.

2-2 Experimental Procedures

The gallium (Ga, concentration ~ 2e14 /cm^2) doped Ge substrates were used to fabricate the Pt/ALD-Al_2O_3/Ga-doped Ge/Al MOSCAPs. After broking the flesh Ge wafer into fragments, we consulted the results of the research of C. C. Cheng et al. [7-8] to clean the Ge fragments in several cycles of sequential dilute HF (HF:H_2O ~ 1:30) and deionized (D.I.) water rinses followed by a last-HF dip and N_2 drying. Then, in order to investigate the effect of deposition temperature on such a MOS gate stack in all respects and calculate the growth rate, we used an atomic-layer-deposition system to grow the gate dielectrics at different temperatures in variant deposition cycles on the cleaned and HF-lasted p-type Ge substrates in Instrument Technology Research Center (ITRC). In this ALD system, tri-methyl-aluminum (TMA), $Al(CH_3)_3$, and H_2O were chosen as the metal source and oxidant that were pulsed alternatively into the reactor for 1 sec; and per pulse separated by N_2 purge of 10 sec to remove redundant reactants during the process. TMA were often-used as the aluminum precursor due to its thermal stability, high vapor pressure (8.4 torr) and highly exothermic reaction with H_2O. During each cycle of reactions, the chamber was held out at a constant pressure about 10 torr. Then, some samples were subjected to 30 sec 400 °C post deposition annealing (PDA), by a rapid thermal annealing (RTA) system

in N_2 (pressure~ 1 atm) ambient, for further improving the film quality. With the help of shadow mask, we left out the lithography process and defined the platinum (Pt) gate electrodes through a reactive sputtering system in Ar (flow rate~ 24 sccm) ambient. Before thermally coating aluminum (Al) on the backsides of the semi-manufactured samples, we split them into several groups so that post metallization annealing (PMA), by a rapid thermal annealing (RTA) system in N_2 (pressure~ 1 atm) ambient, could be performed at different temperatures (400 and 600 °C) but equal time duration (30 seconds) for studies of the thermal stability of such a MOS gate stack. The overall fabrication processes of the Ge MOSCAPs were illustrated summarily in Fig. 2-6 for simple and easy to follow. After the fabrication of the MOSCAPs, we measured the Al_2O_3 film thickness by Ellipsometer (EP) and High Resolution Transmission Electron Microscopy (HRTEM); and, furthermore, inspected the surface morphology by Atomic Force Microscopy (AFM). Particularly and significantly, we used Angle-Resolved X-ray Photoelectron Spectroscopy (AR-XPS), Grazing Incidence X-ray Reflectivity (GI-XRR), Secondary Ion Mass Spectroscopy (SIMS), and Electron Dispersive Spectra (EDS) to investigate the composition of the MOS gate stacks subjected to different thermal processes. For AR-XPS analysis, we used an Al $K\alpha$ radiation source operating at 1486.6 eV for excitation, and the photoelectrons were collected at the take-off angles, 60°, with respect to the surface

horizontal and the binding energy was calibrated by the C 1s peak at 284.5 eV. By using the commercial XPSPEAK software package, we also went further doing peak fitting of the Ge 3d XPS spectra for understanding the mechanism of formation of GeOx and how Ge out diffuses. For GI-XRR analysis, we used a Bede GI-XRR system to measure the reflected X-ray signal at angle range from 0 to 7600 arc-second. In this system, a parallel collimated and monochromatic beam (Cu Ka radiation, λ = 1.5406 $\mathring{A}$) was used and a dynamic intensity range of ca. 5 orders of magnitude was accessible after further purifying the X-ray source by a silicon of single crystal. Data evaluation was carried out with the commercial Bede REFS Mercury software package [16]. It employs the optical matrix method, based on the expressions of Parratt [17] and N'evot and Croce [18], for the analytical calculation of XRR curves of layered systems. We modeled a five layer composition of oxide semiconductor to fit the measurement results and insert the available information from AFM, AR-XPS, and HRTEM physical measurement for more accurate fitting. From a best fit of the experimental data – i.e. from the minimization of a cost function χ^2 – individual film thicknesses, roughnesses, and densities of a multilayer stack can be extracted.

2-3 Results and Discussion

2-3-1 The growth mechanism and the surface morphology of the post-deposited Al_2O_3 films.

Figure 2-7 illustrates the growth rate of the ALD system at 200 °C which is the temperature associated with the thickest Al_2O_3 film in Fig. 2-8 – the growth mechanism of an ALD system. In literature [4], it had pointed out that an ALD system shows almost complete reactions of the two self-cease sequential cycles and more than 80 % (~ 100 % at temperature– 300 K) of coverage of the reactants on alumina membranes during deposition process (explained below) at the temperature of highest growth rate. We also labeled the calculated growth rate (~ 1.2 angstrom/cycle) in Fig. 2-7. The growth rate is similar to that reported somewhere and implies that it is unnecessary to consider the transient region during an initial stage of atomic layer deposition [19] and precursor concentration effect [20] duriing the deposition process. This means that the ALD system has been fine tuned so that we could avoid mentioning the problems might be considered in application of an ALD system.

Referring to some publications [19, 21] and combining our hypothesis inspired from Statistical Mechanics, we did further simulation of the growth mechanism of the ALD system for constant deposition cycles in Fig 2-8 by the following equation;

$$\text{Thickness of an ALD } Al_2O_3 \text{ film} \propto e^{-\Delta U_S(\text{internal energy})/kT} \cdot \theta \qquad (2.1)$$

k is the Boltzmann constant and T is temperature in Kevin. Besides, θ and ΔU_s (internal energy) (≥ 0), respectively, stand for the surface coverage of reactants and the difference of internal energy of the reactants before and after transforming into a surface complex while adsorbing on the surface. As soon as a surface complex (explained later) formed, it transforms into the surface species such as $Al(CH_3)^{2-}$ or $Al(OH)^{2-}$ adsorbance [4, 22] on alumina membranes. In Fig. 2-8, the thicknesses of the films deposited at 60 cycles were estimated from the results of the measurements by High Resolution Transmission Electron Microscopy (HRTEM), arranged in Fig. 2-9; and, in addition, we employed Electron-Dispersive-Spectra (EDS) technique to check the composition of the dielectric films roughly in Fig. 2-10. In eq. 2.1, we assumed approximately that, in a reaction cycle, the distribution of the binding and nonbinding reactants, as the TMA- and H_2O-surface complexes, of a precursor followed the classical Boltzmann distribution despite an open system arising during the deposition process. Based on this ideal, we presumed that the probability, P (binding), of the reactants bind while adsorbing on the surface in a reaction cycle could be represented by this equation;

$$P(\text{binding}) \propto e^{-\Delta U_S(\text{internal energy})/kT} \qquad (2.2)$$

Besides, moreover, it is well known that the adsorption rate can generally be expressed in the following equation [19, 21] without taking account of dissociation of

the precursors;

$$\frac{d\theta}{dt} = \gamma_a p_i (1-\theta)^n - \gamma_d \theta^l \qquad (2.3)$$

θ : *coverage of precoursor*
n : *adsorption order*
l : *desorption order*
γ_a : *adsorption rate constant*
γ_d : *desorption rate constant*
P_i : *partial pressure of reactant*

In many cases, the adsorption rate is much higher than the desorption rate, so that desorption rate can be ignored in deriving eq. 2.3 [19]. Supposing that ideal 2-dimention (2-D) growth occurred (set n=1) during the reactions and solving eq. 2.3, we obtained the solution;

$$\theta(t,T) = 1 - A(T)\exp\{-\gamma_a p_i \cdot t\} \qquad (2.4)$$

A(T) is an arbitrary function of temperature that can be determined by a proper boundary condition (B.C). Since the ALD system has been fine adjusted, we can always obtained saturated coverage of the absorbances in per pulse of precursor injection. Then, we further considered the probability of dissociation of the precursor– TMA, which had been pointed out that it dissociated appreciably and deposited aluminum on the surface [23] at temperature above 650 K [4]. We replaced the ideal coverage, 1 (for 300K), by a function of pressure and temperature – B(T,P) (≤ 1, for 2-D growth). Furthermore, from the researches of A.W. Ott's et al. [4] and by

intuition of mathematics somewhat, it was conjecturable that this function was almost linearly proportional to temperature, and eq. 2.4 could be rewritten as eq. 2.5 at saturation mode;

$$\theta(T,P) = B(T,P) \cong \alpha_O \cdot (T_O - T) \qquad (2.5)$$

It has the relationship to effective adsorption constant (α_O) and complete-dissociated temperature (T_O). Both are related to the partial pressure of a precursor in reactor. Combing eq. 2.2 with eq. 2.4, we arrived at the eq. 2.1. For associating eq. 2.1 with temperature and pressure only, we made the use of eq. 2.5 to modify the equation in a more acceptable form below;

$$\text{Thickness of an ALD } Al_2O_3 \text{ film} \propto \alpha_O \cdot e^{-\Delta U_S(\text{internal energy})/kT} \cdot (T_O - T) \qquad (2.6)$$

Then, by multiplying an independent constant C, the growth rate equation could be rewritten as;

$$\text{Growth rate} = C \cdot \alpha_O \cdot e^{-\Delta U_S(\text{internal energy})/kT} \cdot (T_O - T) \qquad (2.7)$$

Constant C could be determined approximately by simulating the outcome of an experiment with the value of the complete-dissociated temperature ($T_O = 800\,K$, the result of A.W. Ott et al.), the temperature of highest growth rate (T_{HGR} defined below, at which it has the almost 80 % coverage and calculated $\alpha_O \sim 0.0023$ 1/K for $T_O = 800\,K$), and the solution of eq. 2.12 (explained later). Additionally, the temperature corresponding to highest growth rate in our study (see Fig. 2-8) is higher

than that reported somewhere [3, 4]. In A. W. Ott's article, it showed the outcome on cleaned Si wafers followed by H_20 plasma treatment that oxidized the Si (100) sample and left the SiO_2 surface completely hydroxyllated.

To further discuss the shift in the temperature of highest growth rate (HGR) (abbreviated as T_{HGR} below), we did the simulations involving modulating the four parameters (C, α_O, T_O, and ΔU_S) encountered in eq. 2.7 individually and investigated the effects of the modulations on the curves of growth rate in Figs. 2-12~15. Before discussing in depth, we must have a sketch of the range of values and the characteristics of those parameters and their relationship. Equation 2.8 shows the first differentiation of eq. 2.7 for calculating T_{HGR}.

$$\text{First differentiation of eq.(2.7)} \propto \frac{1}{T^2}\cdot(T^2 - \frac{\Delta U_S}{k}T + \frac{\Delta U_S}{k}T_O)\cdot e^{-\Delta U_S/kT} \qquad (2.8)$$

For getting this temperature, it is necessary that eq. 2.8 be equal to zero;

$$\frac{1}{T^2}\cdot(T^2 + \frac{\Delta U_S}{k}T - \frac{\Delta U_S}{k}T_O)\cdot e^{-\Delta U_S/kT} = 0 \qquad (2.9)$$

By solving the quadratic equations with Quadratic Formula and extracting directly, we have all the possible solutions;

$$T_{HGR} = 0,\ \infty,\ \text{and}\ -\frac{\Delta U_S}{2k}\cdot(1 \mp \sqrt{1 + 4\cdot\frac{k}{\Delta U_S}\cdot T_O})\ \ (K) \qquad (2.10)$$

And above all, the solution makes sense is;

$$T_{HGR} = -\frac{\Delta U_S}{2k}\cdot(1 - \sqrt{1 + 4\cdot\frac{k}{\Delta U_S}\cdot T_O})\ \ (K) \qquad (2.11)$$

We could, next, further rewire eq. 2.11 and associate ΔU_S with T_O in a more compact form as;

$$\frac{\Delta U_S}{k} = \frac{T_{HGR}^{\ 2}}{T_O - T_{HGR}} \quad (K) \qquad (2.12)$$

After substituting the parameters with the available values ($T_{HGR} \sim 450\,K$ and $T_O \sim 800\,K$) in A.W. Ott's article and regarding the reasonable range of T_O (~ 600 – 800, 900 K) [24, 25], we got the computation that ΔU_S (~ 600 – 1200 k Joule) has order of value about $10^{-1} \sim 5x10^{-2}$ eV consistent with that calculated by First Principle in Mathew D. Halls's research [26], in which it describes that the reactant complex between TMA and the surface is more weakly bound than the H_2O-surface complex with a calculated binding energy of only 0.03 and 0.04 eV. We had summarized the calculation results in Fig. 2-11 and Table 2-1. Besides, we could estimate the value of the independent constant, C (~ 5.2 $\mathring{A}$ /cycle), and the effective adsorption constant, α_O (~ 0.0023 1/K). Since the value of ΔU_S is close to the energy to break a (weak) chemical bond involving electromagnetic force, we do really have a self-consistent derivation of the ALD mechanism and reasonable estimation of the values of the parameters. Taking a look at eq. 2.12, moreover, we could suggest that T_{HGR} being almost independent of the parameter– $\alpha' = C \cdot \alpha_O$. Therefore, it is expectable that the shift of T_{HGR} would be related to different partial pressures of the precursors, surface treatment before depositing a dielectric film, or both mentioned.

It is ready now to discuss the results of the simulation in Figs. 2-12~15. Figs. 2-12 and 2-13 show the curves corresponding to the modulation of the two parameters – C and α_O. The range of values of α_O (corresponding to 5 % ~ 95% coverage of the reactants on the surface) in the simulation was the possible coverage level at the temperature, T_{HGR}, about 450 K. For parameter – C, it was just chosen around the value estimated through the simulation of the growth rate of A.W. Ott's results to observe the variation related to it. We found that the growth rate is up with increase of the values of C and α_O (a function of partial pressure of the precursors), but the temperature, T_{HGR}, is almost independent of what referred above (in Fig. 2-12 (d) and 2-13 (d)). This observation is consistent with what concluded from eq. 2.1. And, moreover, the pressure during deposition processes and the growth rate calculated in our studies were higher than that recorded in A.W. Ott's article. By intuition, higher deposition pressure might lead to higher partial pressure and surface coverage of the precursors; and, then, resulted in higher growth rate calculated in our research. Then, let's go on to Figs. 2-14 and 2-15 which explain the shift of T_{HGR} intimately. In Fig. 2-14, the range of the value of T_O was about 600 to 800-900 K, which were close to the values ever emerged in references. It shows that the growth rate of an ALD system and the temperature of a HGR point, T_{HGR}, would go up with the increase of complete-dissociated temperature, T_O, related to the partial pressure

of the precursors in reactor to a certain extent. But, something different for the simulation of the modulation of ΔU_S, we could find that in contrast with T_{HGR}, the growth rate decreases with the increase of ΔU_S. In our study compared with that of A.W. Ott et al., in which the data we exploited most, we carried out the deposition process at a higher pressure and on a substrate with different clean technique involving a last-HF dip to make the surface H-terminated that would show higher barrier for reactants adsorbing on to the surface. Then, based on the results of the simulation and by intuition somewhat, we came to the conclusion that higher growth rate and T_{HGR} observed in our research were resulted from higher α_O, T_O, and ΔU_S occurred during the processes.

Now, we must show consideration for the surface morphology, measured by Atomic Force Microscopy (AFM) in Fig. 2-16. It might be related strongly to uniformity of the film, Chemical Vapor Deposition (CVD) behavior for an ALD system designed imperfectly, crystal phase of the film, and crystallization of a dielectric film during processes, etc. In this figure, it shows an acute issue involving CVD reaction while depositing a film at a lower temperature and this symptom alleviated at deposition temperature above 200 °C. We speculated that the CVD phenomenon should be due to an imperfect designed ALD chamber and higher viscosity of TMA at lower deposition temperature. Although less CVD reaction occurred at higher

deposition temperatures, it would result in severe formation of pinhole related to Ge out-diffusion through the formation of vapor-like GeO from the substrate surface at deposition temperature higher than 200°C. So it is better to deposit an ALD film at temperature around 200 °C for a more sound surface and less CVD reaction.

2-3-2 Analyses of Angle-Resolved X-ray Photoelectron Spectroscopy (AR-XPS) and Secondary Ion Mass Spectroscopy (SIMS).

Figure 2-17 illustrates the setup for AR-XPS measurement and the definition of take-off angle. Fig. 2-18 shows the inelastic mean free path (IMFP) versus (photo-) electron kinetic energy and the universal curve calculated by M. P. Seah and W. A. Dench [27, 28, 29]. Before discussing the results of AR-XPS measurements of the samples deposited at 60 cycles, we should estimate the range of detectable depth (DD) of the elements monitored by combining the outcome of the measurement and the information in Fig. 2-18. We could trace back where the photoelectron (PE) came from and conjecture what happened within this distance from sample surface through the estimation of IMFP alone with the measurement results. But, our case is incompatible with the calculation of IMFP in M. P. Seah's research. However, around the mid-1980s, it was suggested that the appropriate length scale to substitute into the quantification equation was not the IMFP but the "attenuation length (AL)". Powell [30, 31] defined the AL as "a value resulting from overlayer-film experiments on the

basis of a model in which elastic electron scattering is assumed to be insignificant. So, we applied the C. J. Powell's formula, eq. 2.13 for calculating AL, to estimate the length so called, "IMFP," in the past and summarized the calculation in Table 2-2.

$$\lambda_{AL} = 0.316 \cdot a^{3/2} \cdot \{ \frac{E}{Z^{0.45} \cdot [\ln(E/27) + 3]} + 4 \} \ (nm) \qquad (2.13)$$

λ_{AL} : *attenuation length*
E : *the electron kinetic energy (in eV)*
Z : *the atomic number of the matrix*
a : *the lattice parameter*

$$a = 10^{8} \cdot (\frac{\mu}{\rho N_{Av}})^{\frac{1}{3}} \qquad (2.14)$$

N_{Av} : *Avogadro constant*
μ : *the average atomic mass of the matrix (in g)*
ρ : *the density of the matrix (in* $kg \cdot m^{-3}$ *)*

Additionally, in Table 2-2, effective detectable depth (EDD) represents a DD that we had token the take-off angle into account. We could find that it is well to deposit the ALD films with ~ 60 cycles for investigating the MOS gate stack characteristics. From the calculation of EDD and the thicknesses estimated in Fig. 2-9, it is conjecturable that all the Ge 2p3 XPS core-level signals should almost come from the bulk of the Al_2O_3 *films. So, we could monitor if the Ge incorporates into and diffuses away from the dielectric films. Furthermore, by monitoring the signal of Ge 3d compared with that of Ge 2p3, we could also sure if the near interface consists of a few layers containing Ge atoms in intermediate oxidation states i.e.,* GeO_x*, etc. during*

deposition processes.

Now, let's discuss the Ge 3d spectra with peak fitting by the commercial XPSPEAK software package (the XPS peak fitting parameters had been summarized in Table 2-3) in Figs. 19, 21, 23, and 25 that are corresponding to the ALD films deposited at R.T. (~ 50 °C), 100 °C, 200 °C, and 300 °C, respectively. Although the Gibbs free energy of GeO_2 is larger in magnitude than that of Ge native oxide [32], we found that the formation of Ge native oxide (GeO_x, x ~ 1) was easier than that of Ge dioxide for the as-deposited ALD films. We considered it is because that higher concentration (conc.) of $Ge_{(s)}$ and $GeO_{2\,(s)}$ occurred initially promoted GeO_x to form through the reaction mechanism – eqs. 2.15 and 2-16 [33] – at initial stage; but, the onset of disproportionation through eq. 2.17 was observed at temperature about 245±25 °C [34, 35], so that we obtained a GeO_x-rich film rather than a GeO_2-rich one for the rudeness ALD films.

$$Ge_{(s)} + GeO_{2\,(s)} \rightarrow GeO_{(g)} \qquad (2.15)$$

$$GeO_{(g)} \rightarrow GeO_{(s)} \qquad (2.16)$$

$$GeO_{(s)} \rightarrow Ge_{(s)} + GeO_{2\,(s)} \qquad (2.17)$$

After PMA 400 °C, we can see that the amount of GeO_2 increases but decreases for that of GeO_x since the annealing temperature had triggered off disproportionation to produce Ge and GeO_2. Further increasing the annealing temperature to 600 °C, we

had almost lost track of the Ge oxide signal of the film deposited at R.T. (~ 50 °C), 100 °C, and 300 °C due to the Ge out-diffusion and full disproportionation (at temperature about 525±50 °C) [34, 35] happened during the thermal process. Ge out-diffusion was confirmed by monitoring the Ge 2ps XPS spectra in Figs. 20 (a), 22 (a), 24 (a), and 26 (a); and, it also shows that the Ge 2p3 peak position gets close to original position gradually. But something different for the 200 °C ALD film in Fig. 2-23, the oxide signal enhanced while suffering to such a high annealing temperature. Through inspecting the oxygen (O) SIMS spectra of the as-deposited film in Fig 2-34 (a), we supposed that because of higher O conc. permeated into the substrate during film deposition and thicker film showed in Fig. 2-9 or 2-33 leaded to such dense GeO_2 residue in the 200 °C ALD Al_2O_3 film. By the way, let's take a look at the carbon (C) SIMS spectra of the as-deposited film in Fig 2-34 (b). In this figure, it reveals severe C incorporation into the dielectrics for a lower deposition temperature since incomplete ALD reaction could lead to non-reacted CH_3^- bond remained. The variation of Ge oxide in the film subjected to various thermal processes had been summarized in Fig. 2-29 through the XPS PE intensity ratio of Ge oxide to Ge as eq. 2-18;

$$Intensity\ ratio = \frac{I_{GeO} + I_{GeO_2}}{I_{Ge}} \times 100\,\% \qquad (2.18)$$

After studying the Ge 3d and Ge 2p3 XPS spectra, we surveyed the Al 2p and O

1s XPS core-level spectra related to how stoichiometric the film is in Figs 20 (b) (c), 22 (b) (c), 24 (b) (c), and 26 (b) (c). In those figures, the peak position of the Aluminum-hydrogen-carbonate (AHC), gamma (γ), and alpha (α) aluminum oxide had been labeled as guide for eyes. Those spectra imply that we would get a more and more destroyed film when increase the annealing temperature but a less destroyed film when deposited it at temperature about 200 °C due to a more complete ALD reaction. The extent of destruction can be represented somewhat by the extent of shift of the Al 2p and O 1s XPS peak position in Fig. 2-30. All the films show an energy rising-up phenomenon which were conjectured due to C and H residues in the film or near the surface (see Fig. 2-34 (b)). Furthermore, by extracting the XPS spectra areas, we can calculate the elementary ratio between the detected elements through eq. 2.19 [36, 37, 38] with some error due to using this equation on an improper case.

$$\{O\} \cong \frac{I_{O\,1s}/S_{O\,1s}}{I_{Ge\,2p3}/S_{Ge\,2p3} + I_{Al\,2p}/S_{Al\,2p} + I_{O\,1s}/S_{O\,1s}} \times 100\,(at.\%) \qquad (2.19)$$

$I_{Ge\,2p3,\,Al\,2p,\,O\,1s}$: *the measured XPS intensities of Ge 2p3, Al 2p, and O 1s*

$S_{Ge\,2p3,\,Al\,2p,\,O\,1s}$: *the relative XPS sensitivities of Ge 2p3, Al 2p, and O 1s against the sensitivity of C 1s (= 1.00)*

The equation was used to estimate the atom % (at. %) oxygen {O} of $Ge_xAl_yO_z$ dielectrics where $I_{Ge\,2p3}$, $I_{Al\,2p}$, and $I_{O\,1s}$ are the measured XPS intensities of Ge 2p3, Al 2p, and O 1s core-level of an ALD film almost. $S_{Ge\,2p3}$, $S_{Al\,2p}$, and $S_{O\,1s}$ are the relative

XPS sensitivities of Ge 2p3 (=24.15), Al 2p (=0.537), and O 1s (=2.89) core-level against the sensitivity of C 1s (=1.00), respectively. Similarly, we could also calculate the at. % {Ge} and {Al} of the films; and all the results of calculation were summarized in Figs. 2-27, 2-28, and Table. 2-4. However, what should be further mentioned is that this equation is more correct and useful to calculate a uniform and unique composed film for the detected elements. The calculation shows that the ALD films got more stoichiometric when increased the deposition (but not for the 300 °C case) and anneal temperature. But this is inconsistent with the conclusion what followed the discussions on the shift of the Al 2p, O 1s, and Ge 2p3 XPS peak position in Fig. 2-30. In addition, the calculation of the film deposited at 300 °C shows a contradictive behavior due to an improper use of eq. 2-19. All the questions mentioned can be explained as a result of the mixed signals from Ge substrate. But despite this, it is still worthy to see the conc. of O and Ge decreased when increased the deposition and anneal temperature in Fig 2-28. This implies the Ge out-diffusion through the formation of vapor-like GeO. We need a credible method to judge the extent of stoichiometry of those ALD films yet. Energy spacing might be a trusty and convenient definition to show how stoichiometric a film is [12, 39]. It is explained as the inst in Fig 2-32 and eq. 2-20;

$$\text{Energy spacing of } Al_2O_3 = B.E._{O\,1s} - B.E._{Al\,2p} \qquad (2.18)$$

This equation describes that energy spacing is the difference between the binding energy of O 1s and Al 2p XPS peak position in magnitude. Fig. 2-32 shows the energy spacings of various phases of aluminum oxide as references for determining what the phase an ALD film has. Fig. 2-31 summarized the energy spacings of those ALD films subjected to different thermal processes and the energy spacing of γ- and α- aluminum oxide also labeled in it. It shows a more consistent result with what mentioned above than that concluded from the calculation of at. % {element}. So far along with Fig. 2-31, we can conclude the results of AR-XPS analysis that;

1- *We get a more stoichiometric and Ge incorporated ALD film with increase of deposition temperature.*

2- *We get a more GeOx and C (might be due to non-reacted CH_3^- bond remained) incorporated ALD film with decrease of deposition temperature.*

3- *The incomplete reacted ALD films get more destroyed with increase of annealing temperature.*

4- *The almost complete reacted ALD films (deposited at temperature~ 200 °C) get less destroyed with increase of annealing temperature in comparison to that described in point 2 but have more O permeated into*

the substrate during film deposition.

5- *We have a proper range of temperature about 140 °C ~ 170 °C to deposit a more stoichiometric, complete reacted, and less GeO_x and C incorporated ALD Al_2O_3 film.*

In order to get further comprehending more information about the density and interface roughness of the ALD films, we must applied the GI-XRR technique to figure out the possible composite layers through the films; and, then, individual film thicknesses, roughnesses, and densities of a multilayer stack can be extracted.

2-3-3 Analyses of Grazing-Incidence X-ray Reflectivity.

We use a Bede GI-XRR system to measure the as-deposited and semi-manufactured samples (without Pt gate electrodes and Al back-contact) to estimate the thicknesses, densities, roughnesses, and possible distributions of elements of the ALD Al_2O_3 films deposited at various temperatures. Fig. 2-36 collects all the measured results to show what is different between those as-deposited films. After measurements, data evaluations were carried out with the commercial Bede REFS Mercury software package. For a better consistency of the fitting results and a minimization of the number of fitting parameters, we took the available data from other measurements, such as HRTEM and AFM measurements, into the fitting

parameters and kept them fixed during the fitting. Table. 2-5 summarizes the thermal-dynamics related formation energy of the possible formed compounds as reference for helping modeling a multilayer stack to fit the obtained raw data. Combining with the results of the analysis of AR-XPS and Table 2-5, we model a stack with 5 layers showed in Figs. 2-37, 38, 39, and 40 for figuring out the possible distributions of the elements overall the dielectrics. Figs. 2-35 displaces the fitting outcomes with minimized cost functions, χ^2, and gets fitting curves compared with the measured data to show how better the fitting is. From the best fitting with the 5 layer stack model, individual layer thicknesses, roughnesses, and densities can be extracted. We had summarized all the fitting results in Table 2-6, Fig. 2-41, 42, and 43. Combining the thicknesses of Al_2O_3 and $Ge_xAl_yO_z$ layers we obtain the thickness of an ALD Al_2O_3; and, further taking the thickness of GeO_2 into account, we obtain a thickness corresponding to that measured by HRTEM. So, we could find that the simulated error of thickness at lower and higher temperature relative to 200 °C in Fig. 2-8 is due to the formation of GeO_x and Ge out-diffusion at initial stage of a deposition process, respectively. The GI-XRR fitting shows a consistent result with the analysis of AR-XPS and explains why the observation of Ge 2p3 XPS core-level signal was most easier for the films deposited at higher temperatures after PMA 400 °C through modeling a Ge incorporated layer between the modeled GeO_2 and pure Al_2O_3

layers. The fitted interface roughnesses along with the GeO_2 interfacial layer help us explaining why the MOS gate stack with Al_2O_3 film deposited at 100 °C has the minimized interface states. Fig. 2-42 (a) shows that;

1- *The thickness of GeO_x interfacial layer decreased with increase of deposition temperature.*

2- *We got a more terrible interface roughness between the Ge substrate and GeO_x interfacial layer with increase of deposition temperature.*

3- *We got a more severe Ge incorporated ALD films with increase of deposition temperature. This might be why the observation of Ge 2p3 XPS core-level signal was most easier for the films deposited at higher temperatures after PMA 400 °C.*

4- *The almost complete reacted ALD films (deposited at temperature~ 200 °C) get less destroyed with increase of annealing temperature in comparison to that described in point 2 but have more O permeated into the substrate during film deposition.*

Fig. 2-42 (b) implies that;

1- *The trend of density of GeO_x interfacial layer implies that we wolud get a*

more porous-like GeO_x for lower deposition temperature.

2- *Higher and lower density of the substrate and O in-diffusion layer of the film deposited at 200 °C are intimately related to higher O incorporation during the deposition process confirmed by Fig. 2-34 (b)*

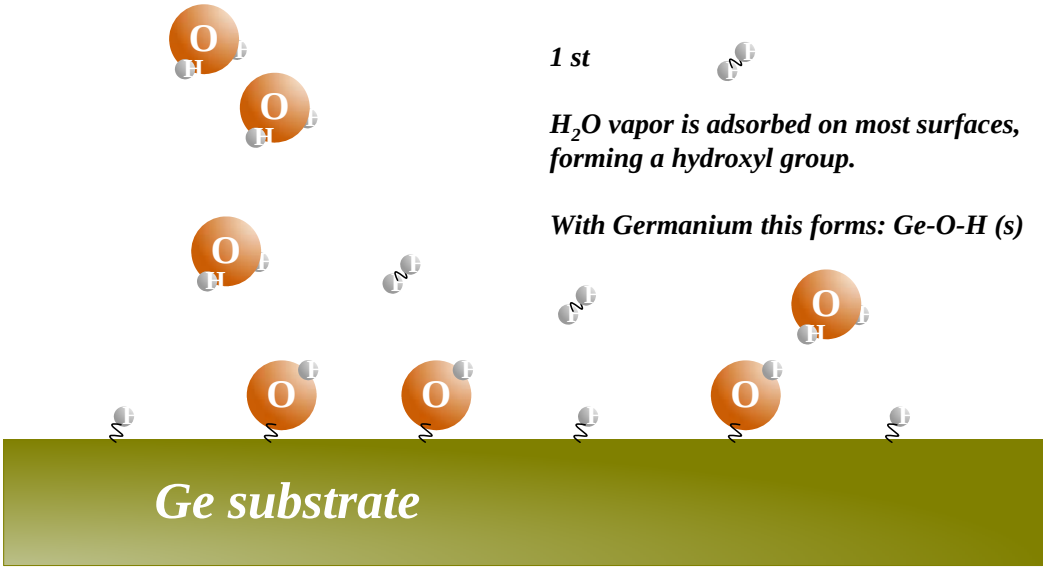
3- *Higher density and thicker thickness of the GexAlyOz layer resulted in that the observation of Ge 2p3 XPS core-level signal was most easier for the films deposited at higher temperatures after PMA 400 °C.*

4- *The trend of Al_2O_3 density implies a more stoichiometric film would be obtained while increasing the deposition temperature.*

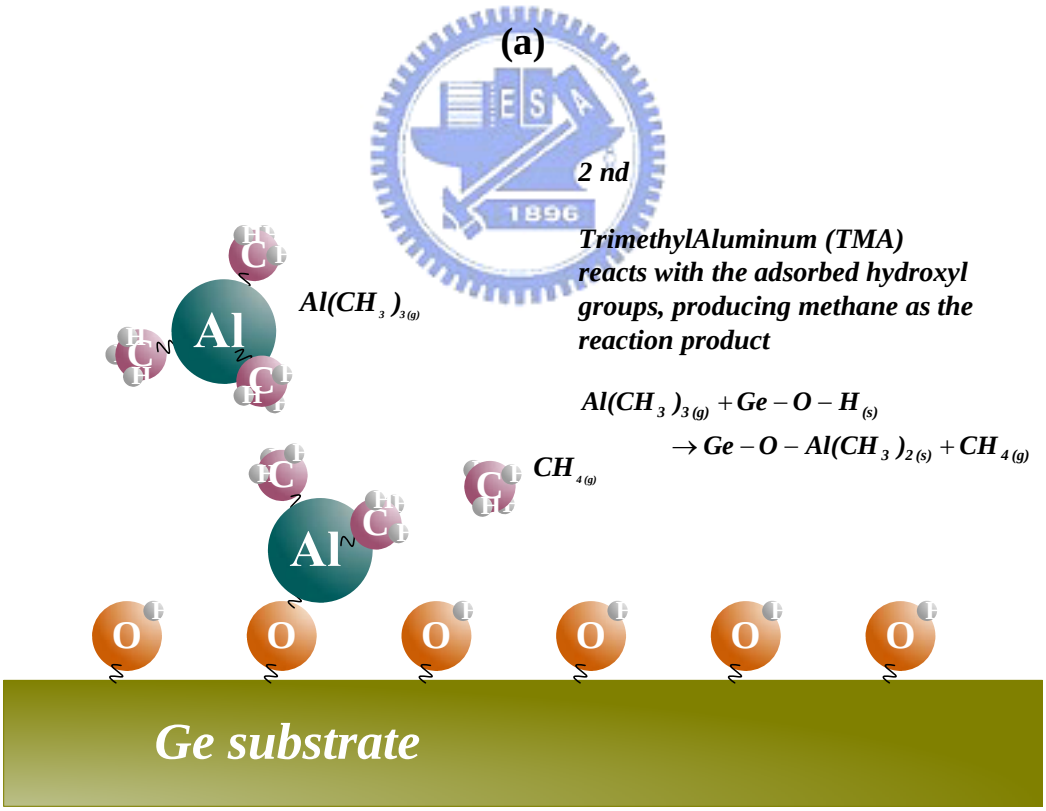
Fig. 2-3 summarizes the trend of Al_2O_3 density in comparison to the ideal values of density of α- and γ- Al_2O_3 as guide for eyes. It also shows a consistent result with the conclusions followed the discussions of Fig. 2-31.

2-4 Summary

We proposed a mechanism and provided an equation to simulate the growth rate of an ALD system. By doing first differentiation of the equation and simulating the four parameters in equation in comparison to the experiment results in literatures, we explain reasonably why we had a different growth rate and T_{HGR} of this ALD system. Based on the AR-XPS, SIMS, and GI-XRR analyses, we figured out the possible distribution of elements overall the dielectrics and confirmed the onset and full disproportionation through the variation of Ge 3d and Ge 2p3 XPS core-level signals with peak fitting by the XPSPEAK software package. From the analysis of GI-XRR and data evaluation by our proposed 5 layer stack model along with the Bede REFS Mercury software package, we could keep track of the thicknesses, densities, and roughnesses of an ALD film. Based on the analyses mentioned above, we find a window of temperature to deposit a less GeO_x, less Ge incorporated, more stoichiometric, and more complete reacted ALD Al_2O_3 film during deposition process. Those results of physical measurements inspired us to explain the electrical performance of the MOSCAPs and MOSFETs discussed in chapter 3 and 4, respectively. So far, we are ready to see the electrical characteristics involving deposition of ALD Al_2O_3 films on Ge substrates.



(a)



(b)

Fig. 2-1 The (a) 1st step and (b) 2nd step of the ALD deposition mechanism.

3 rd

TrimethylAluminum (TMA) reacts with the absorbed hydroxyl groups, until the surface is passivated.

TMA does not react with itself, terminating the reaction to one layer.

This causes the perfect uniformity of ALD.

The excess TMA is pumped away with the methane reaction product.

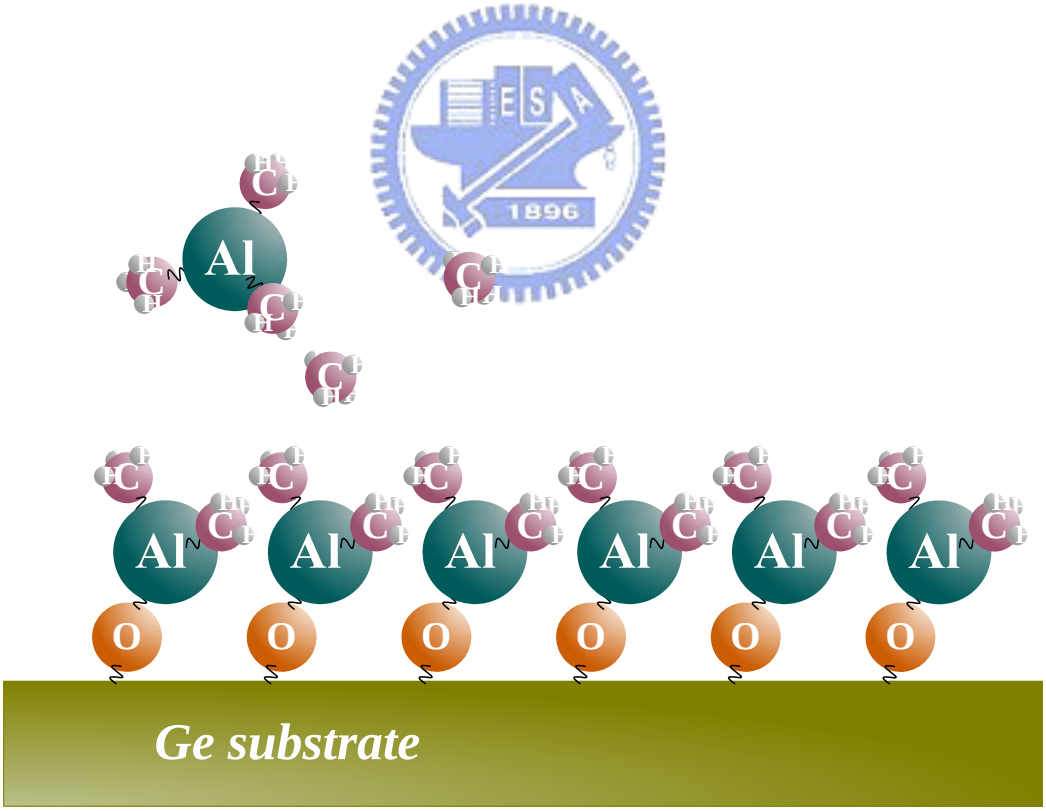
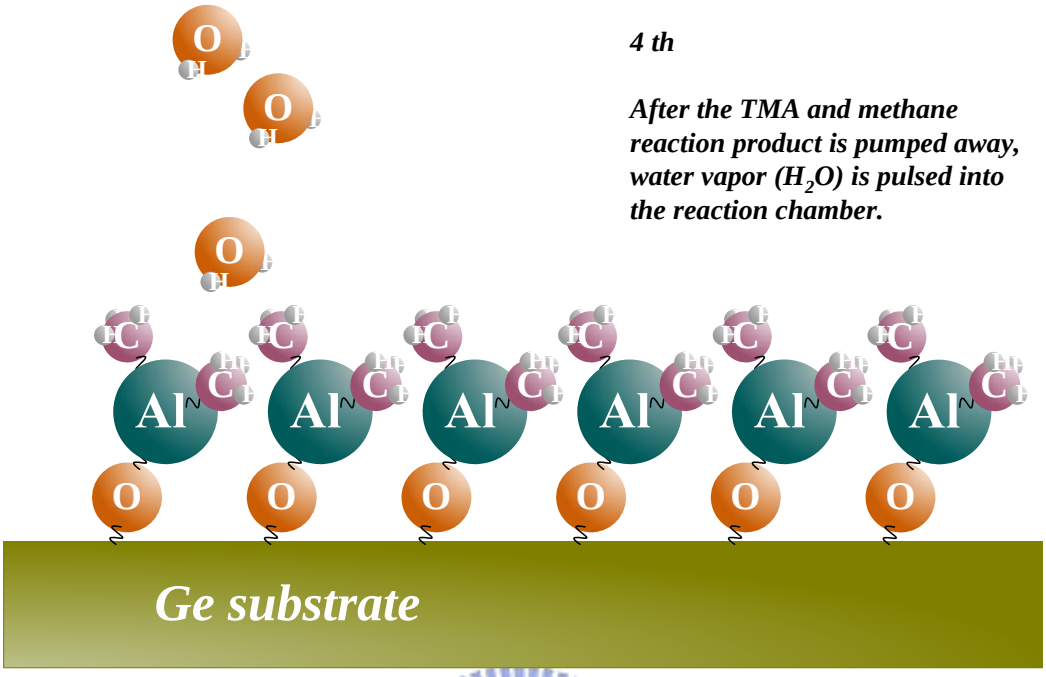
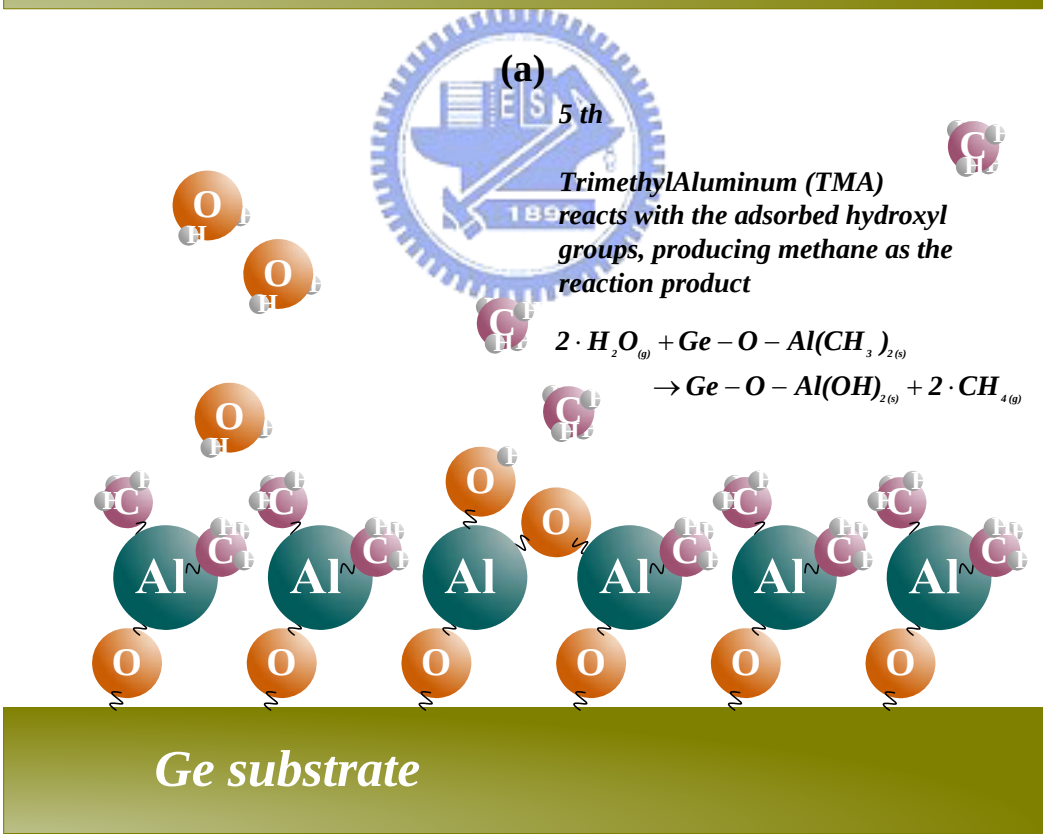


Fig. 2-2 The 3rd step of the ALD deposition mechanism.



(a)



(b)

Fig. 2-3 The (a) 4th step and (b) 5th step of the ALD deposition mechanism.

6 th

The reaction product methane is pumped away.

Excess H_2O vapor does not react with the hydroxyl surface groups, again causing perfect passivation to one atomic layer.

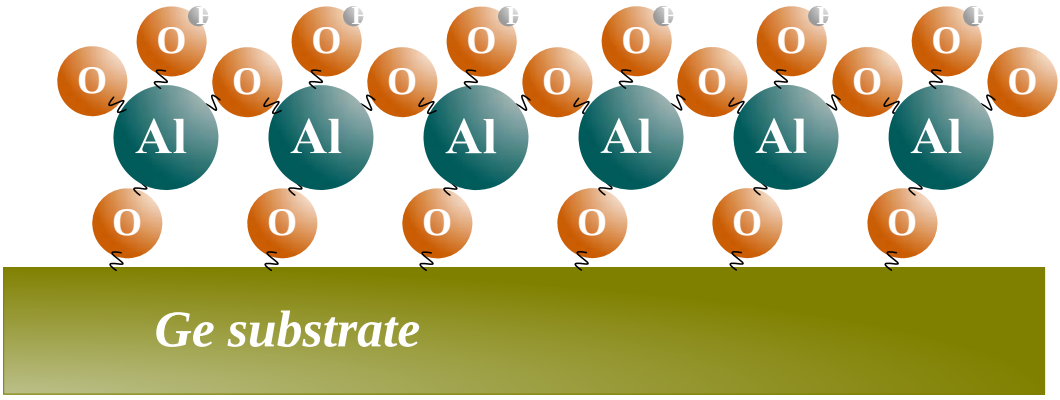


Fig. 2-4 The 6th step of the ALD deposition mechanism.

7 th

One TMA and one H_2O vapor pulse form one cycle.

Here three cycles are shown, with approximately one angstrom per cycle.

Two reaction steps in each cycle:

$$Al(CH_3)_{3(g)} + Al-O-H_{(s)} \rightarrow Al-O-Al(CH_3)_{2(s)} + CH_{4(g)}$$

$$2 \cdot H_2O_{(g)} + Al-O-Al(CH_3)_{2(s)} \rightarrow Al-O-Al(OH)_{2(s)} + 2 \cdot CH_{4(g)}$$

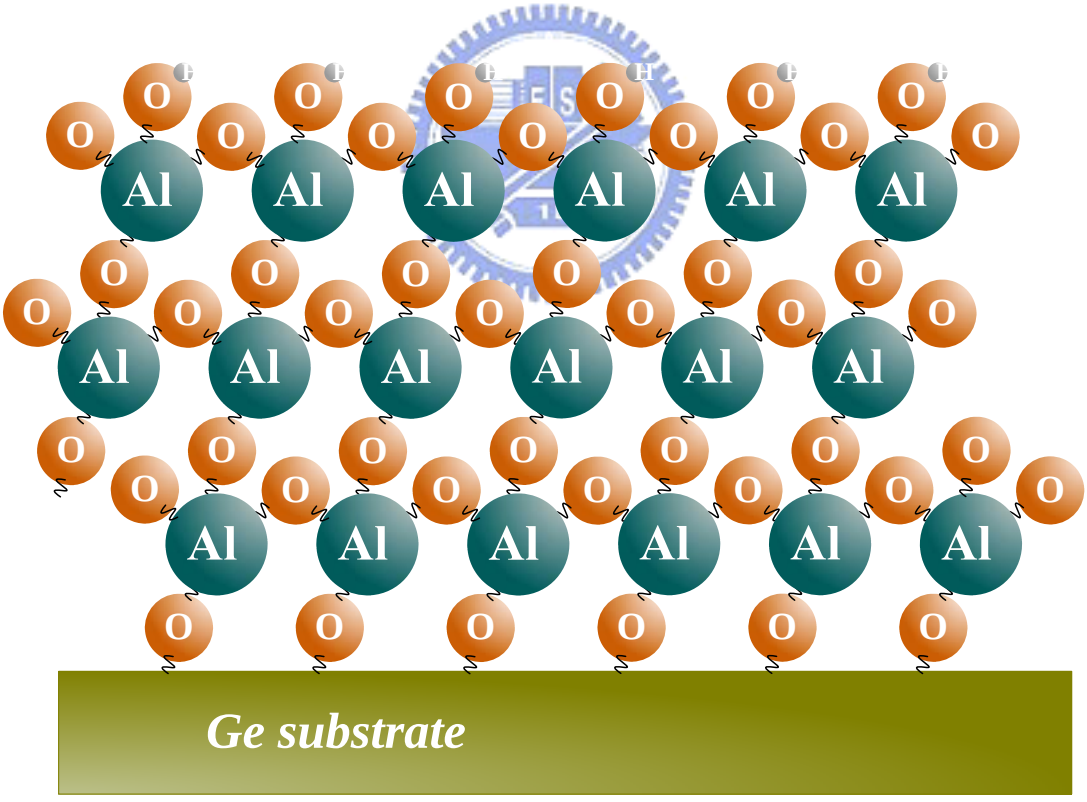


Fig. 2-5 The 7th step of the ALD deposition mechanism.

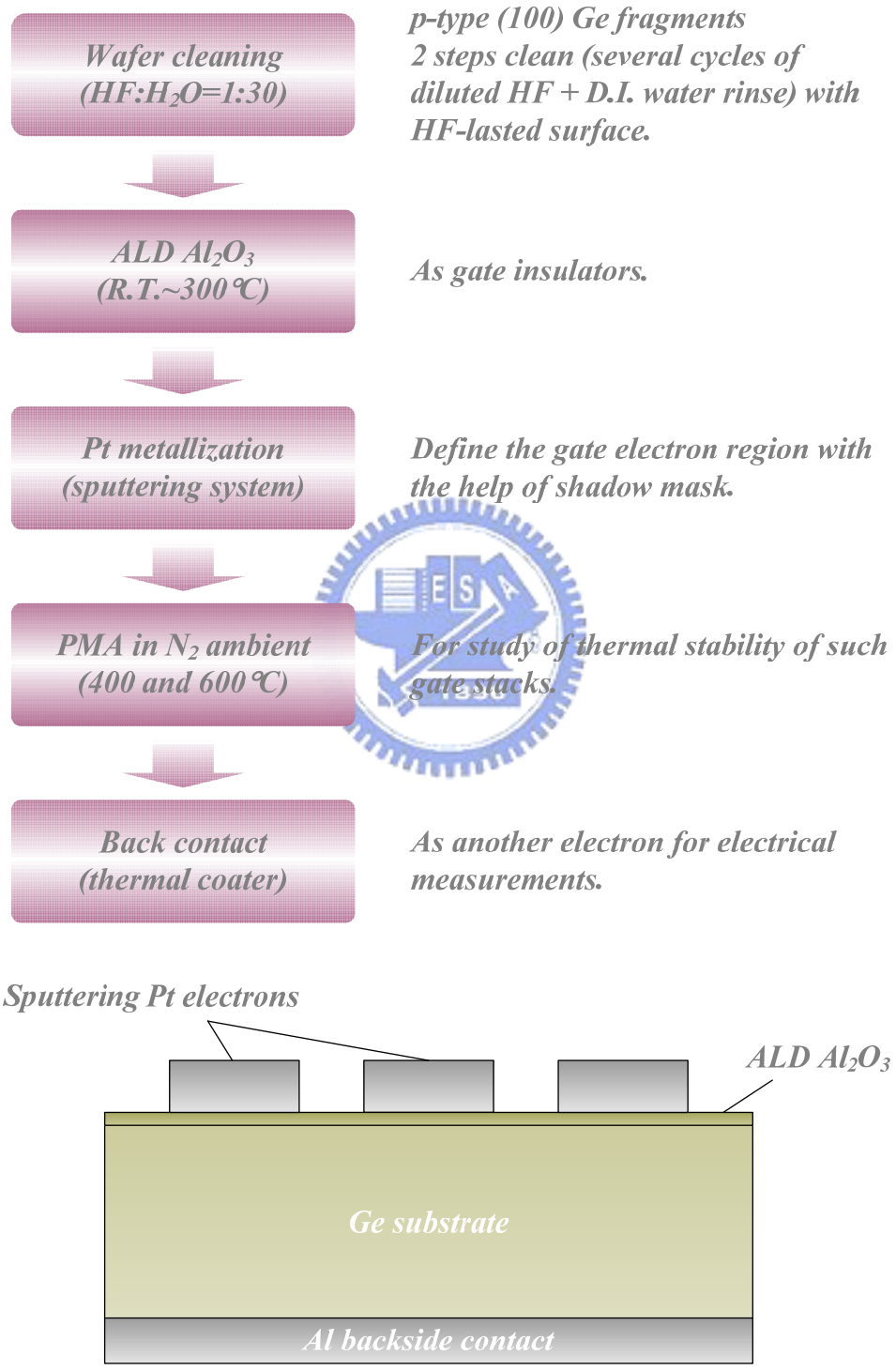


Fig. 2-6 MOSCAP fabrication flow chart.

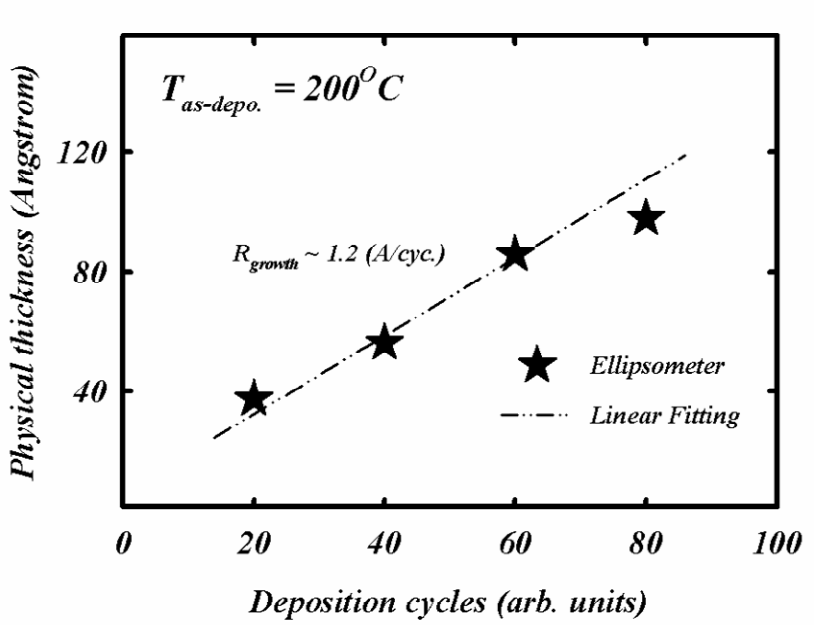


Fig. 2-7 Deposition cycles v.s. physical thickness of Al_2O_3 films measured by an Ellipsometer system with a linear fitting curve (guide for eyes).

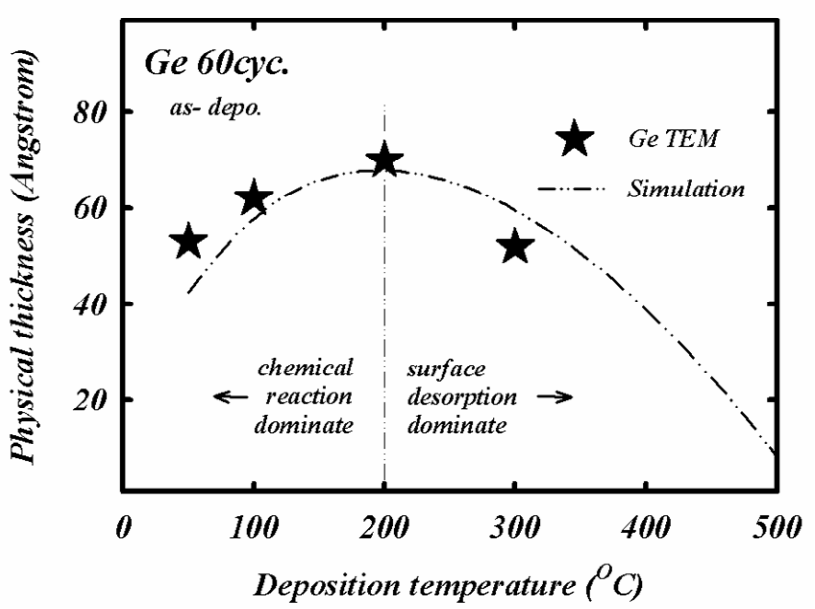


Fig. 2-8 ALD growth mechanism as a function of deposition temperature with a simulation fitting curve (guide for eyes).

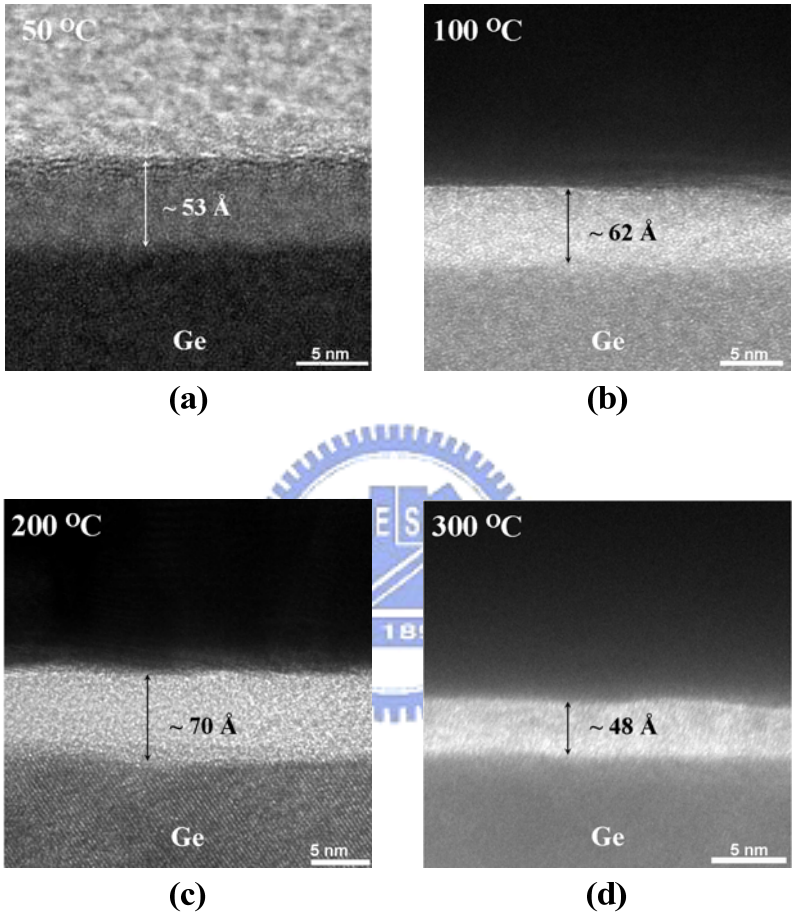
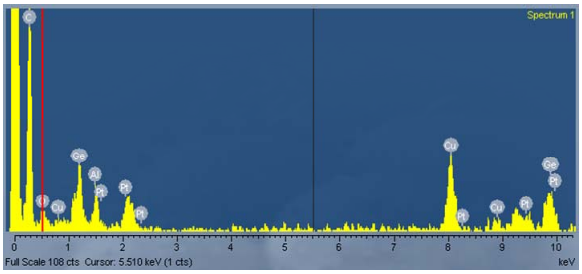
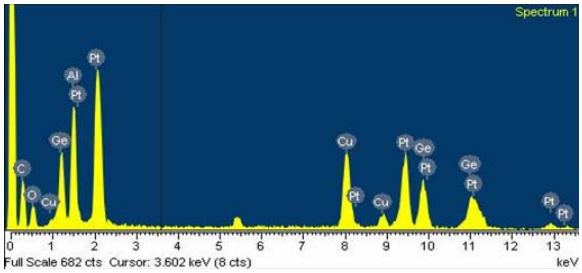


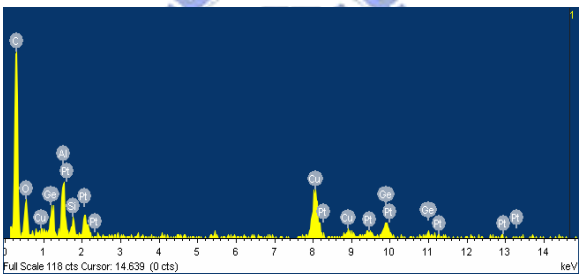
Fig. 2-9 High Resolution Transmission Electron Microscopy (HRTEM) cross-section images of the samples corresponding to the deposition temperatures, (a) 50℃, (b) 100℃, (c) 200℃, (d) 300℃.



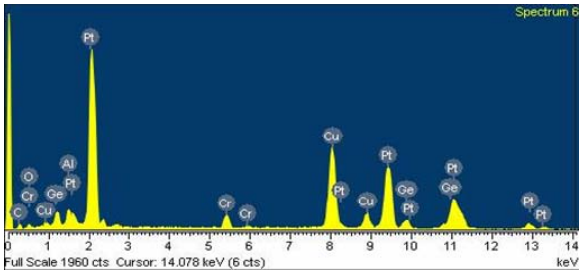
(a)



(b)



(c)



(d)

Fig. 2-10 Electron Dispersive Spectra (EDS), associated with the HRTEM images showed in Fig. 2-9, of the Al_2O_3 films deposited at temperatures, (a) 50 ^{O}C, (b) 100 ^{O}C, (c) 200 ^{O}C, (d) 300 ^{O}C.

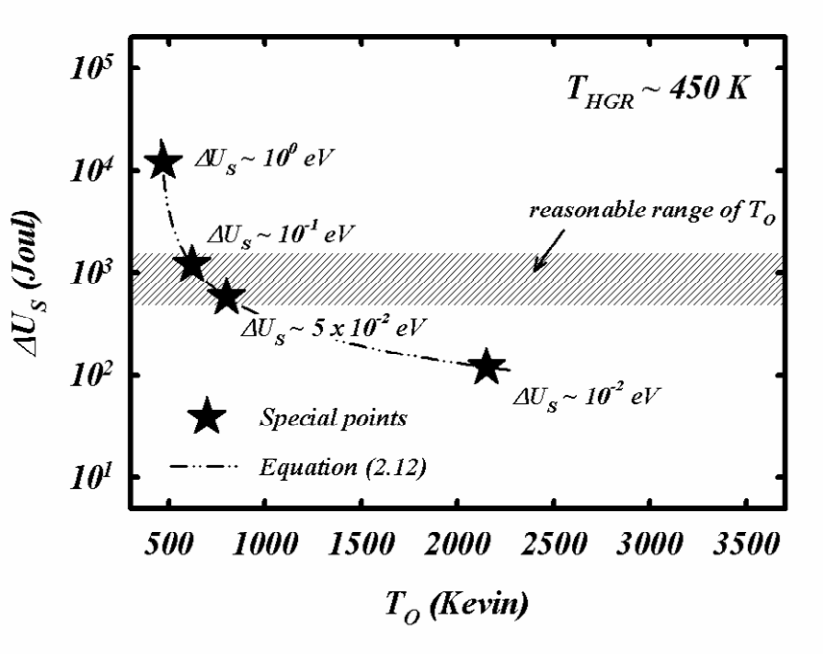
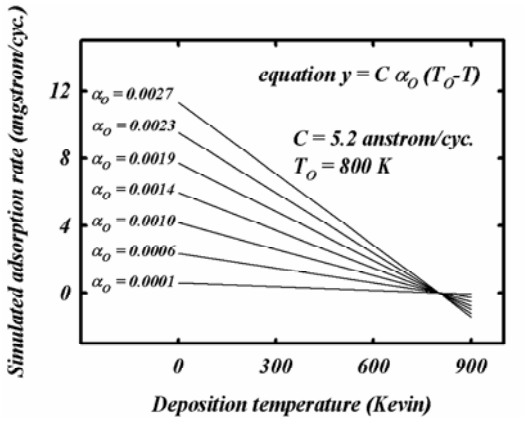


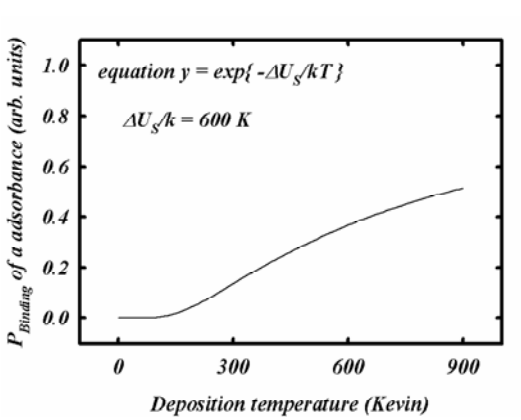
Fig. 2-11 Equation (2.12), the dash-dot-dot curve, and several special points, solid start, related to particular order of values of US. The region of oblique lines indicates the reasonble region of complete-dissociated temperature

Table 2-1. The coordinates of the points (star mark) indicated in Fig. 2-11.

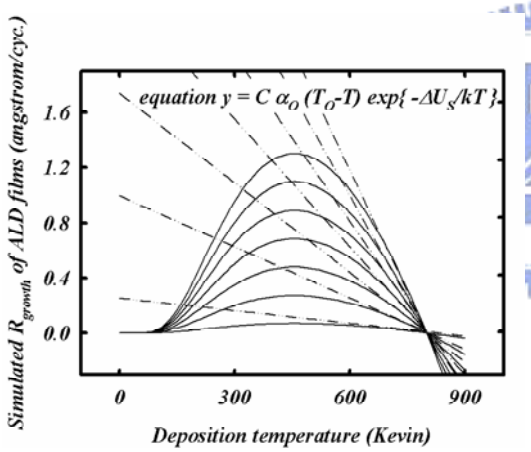
Star Mark	T_O (K)	$\Delta U_S/k$ (K)	ΔU_S (eV)
Mark 1	~ 470	~ 12000	$\sim 10^0$
Mark 2	~ 620	~ 1200	$\sim 10^{-1}$
Mark 3	~ 800	~ 580	$\sim 5 \times 10^{-2}$
Mark 4	~ 2200	~ 120	$\sim 10^{-2}$



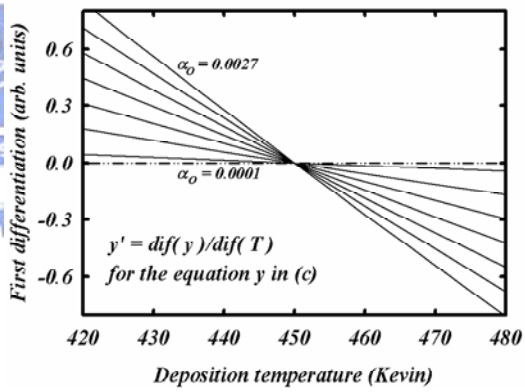
(a)



(b)



(c)



(d)

Fig. 2-12 Simulation of the effects of different effective-adsorption-constant, α_O, on the growth rate of ALD Al_2O_3 films. (a) the curves related to different α_O (2-D growth condition), (b) the curve of P (binding) while setting $\Delta U_S/k$ = 600 K, (c) the curves, combing (a) with (b), of simulated growth rate of ALD Al_2O_3 films (the dash lines represent the curves in (a), just guide for eyes), (d) the first differentiation of the solid curves showed in (c) (the dash line indicates the value of zero differentiation, and the intersection point of this line and a solid line corresponds to the HRG point).

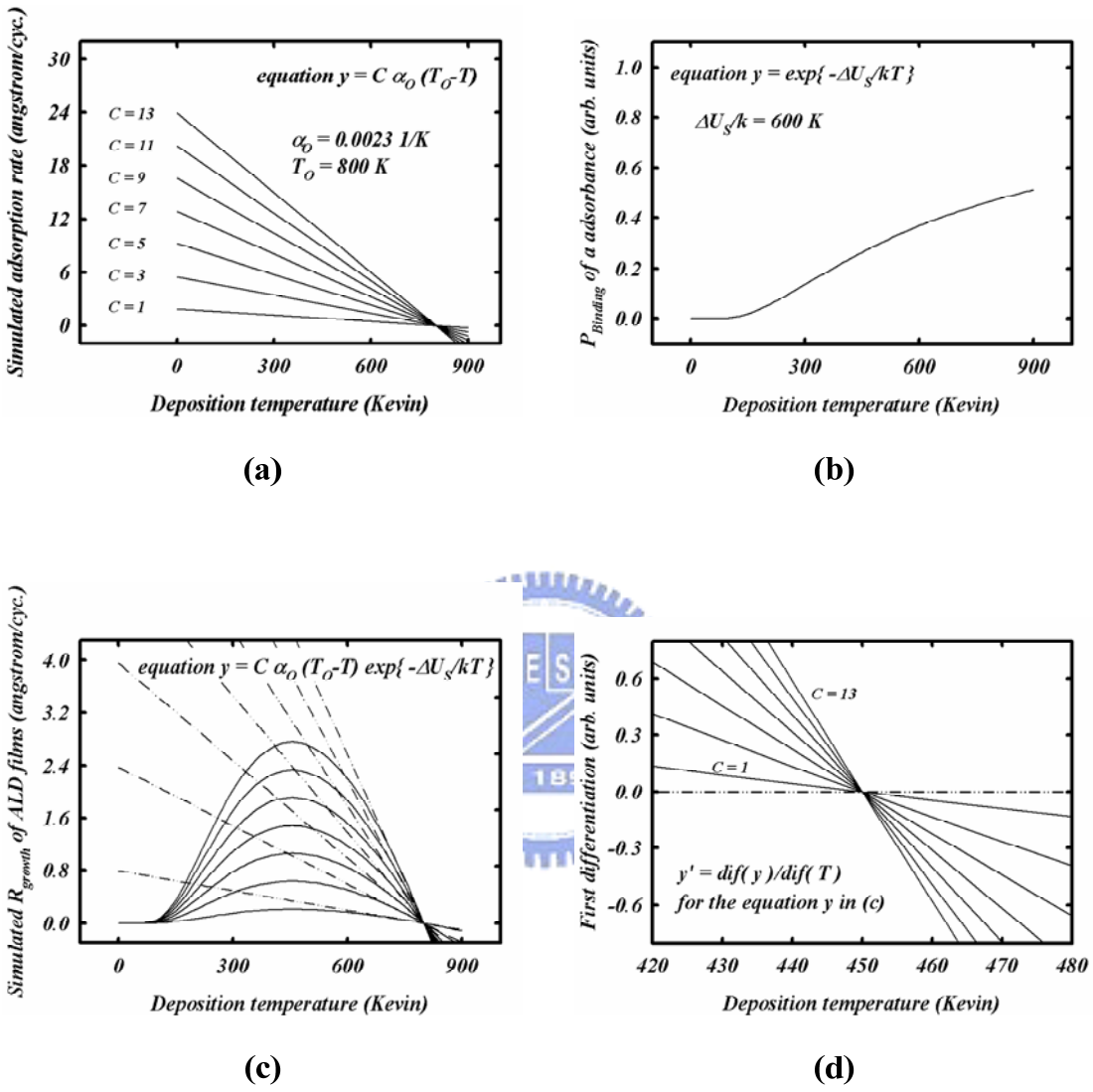


Fig. 2-13 Simulation of the effects of different independent-constant, C, on the growth rate of ALD Al_2O_3 films. (a) the curves related to different C (2-D growth condition), (b) the curve of P (binding) while setting $\Delta U_S/k$ = 600 K, (c) the curves, combing (a) with (b), of simulated growth rate of ALD Al_2O_3 films (the dash lines represent the curves in (a), just guide for eyes), (d) the first differentiation of the solid curves showed in (c) (the dash line indicates the value of zero differentiation, and the intersection point of this line and a solid line corresponds to the HRG point).

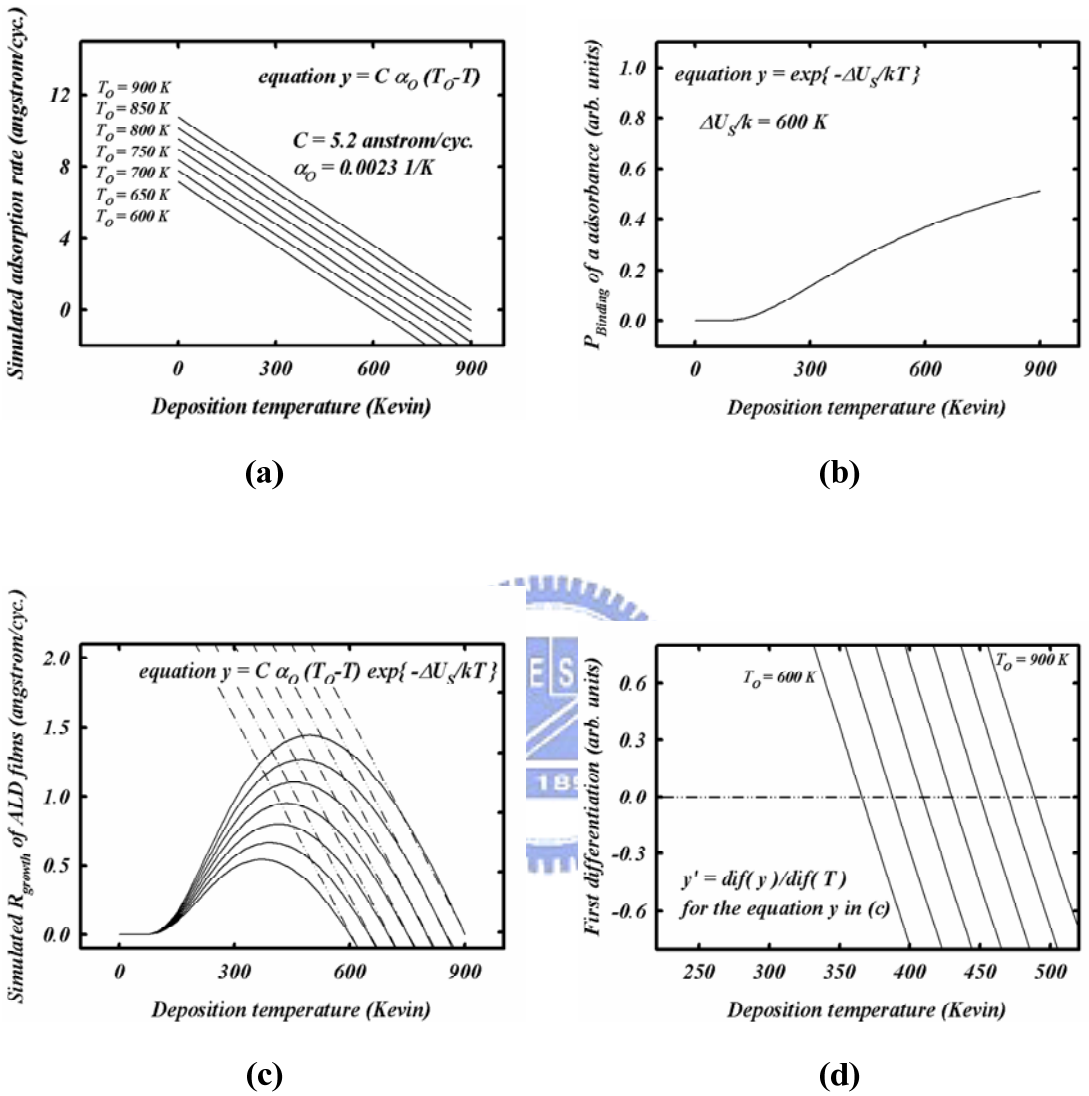


Fig. 2-14 Simulation of the effects of different complete-dissociated temperature, T_O, on the growth rate of ALD Al_2O_3 films. (a) the curves related to different T_O (2-D growth condition), (b) the curve of P (binding) while setting $\Delta U_S/k$ = 600 K, (c) the curves, combing (a) with (b), of simulated growth rate of ALD Al_2O_3 films (the dash lines represent the curves in (a), just guide for eyes), (d) the first differentiation of the solid curves showed in (c) (the dash line indicates the value of zero differentiation, and the intersection point of this line and a solid line corresponds to the HRG point).

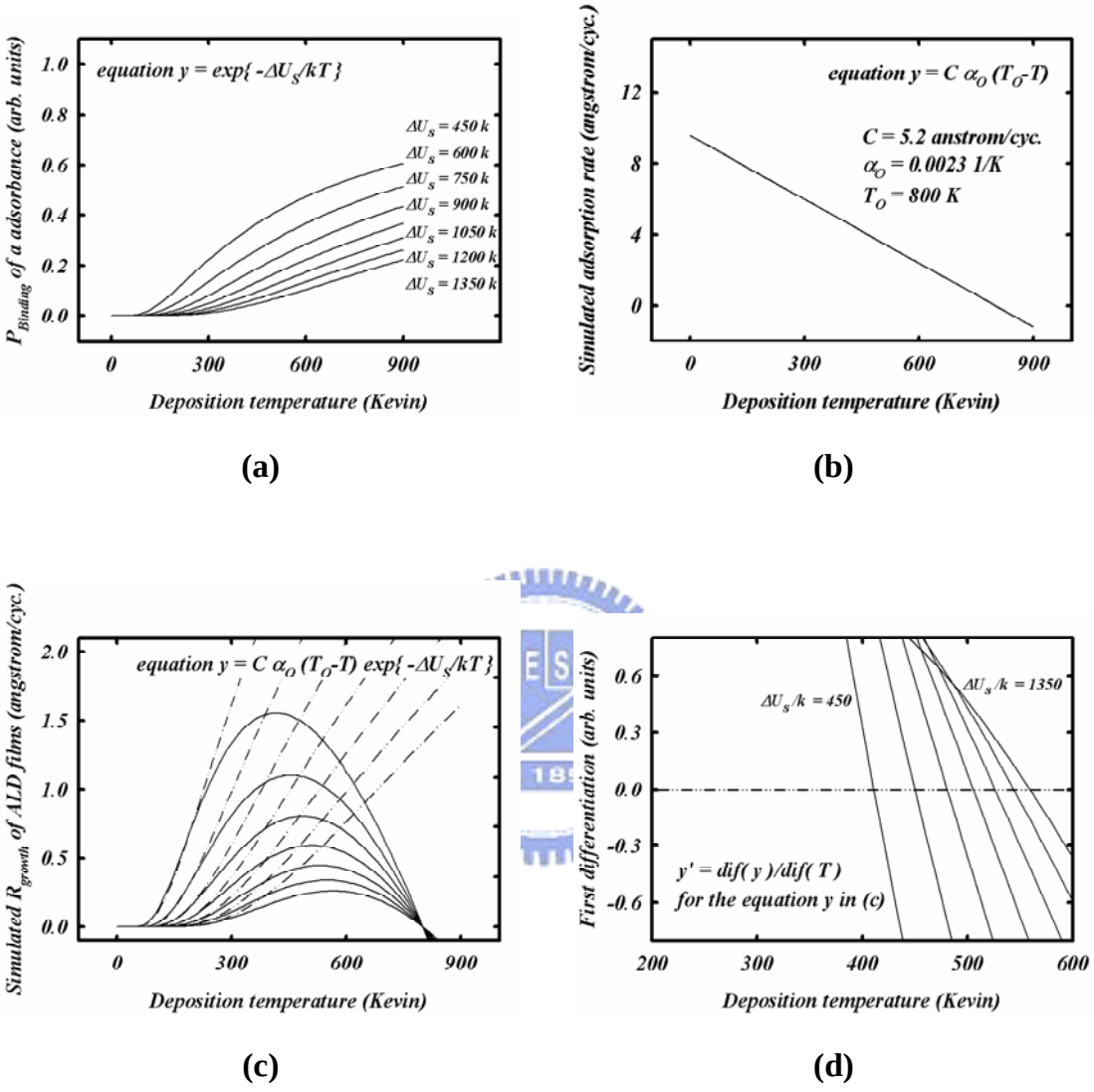


Fig. 2-15 Simulation of the effects of different difference-of-internal-energy, ΔU_S, on the growth rate of ALD Al_2O_3 films. (a) the curves related to different ΔU_S (2-D growth condition), (b) the curve of $C \cdot \theta$ while setting $C = 5.2$, $\alpha_O = 0.0023$, and $T_O = 800$, (c) the curves, combing (a) with (b), of simulated growth rate of ALD Al_2O_3 films (the dash lines represent the curves in (a), just guide for eyes), (d) the first differentiation of the solid curves showed in (c) (the dash line indicates the value of zero differentiation, and the intersection point of this line and a solid line corresponds to the HRG point).

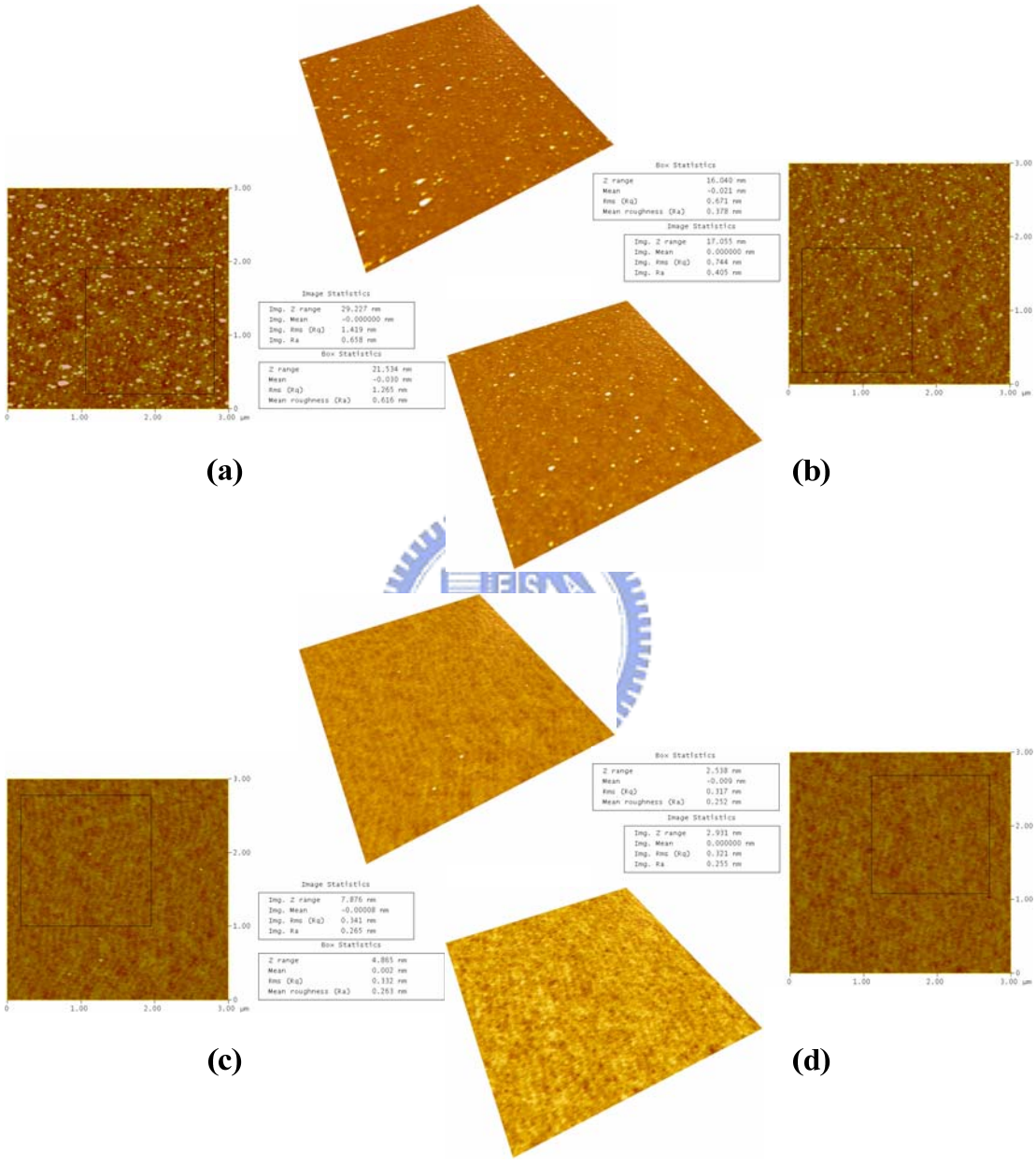


Fig. 2-16 Atomic Force Microscopy (AFM) surface morphology images of the samples corresponding to the deposition temperatures, (a) 50 ^{O}C, (b) 100 ^{O}C, (c) 200 ^{O}C, (d) 300 ^{O}C.

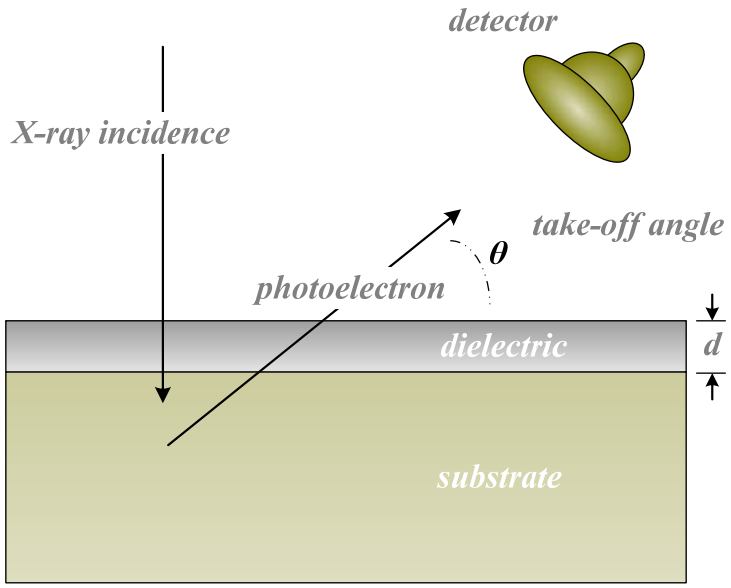


Fig. 2-17 AR-XPS measurement setup.

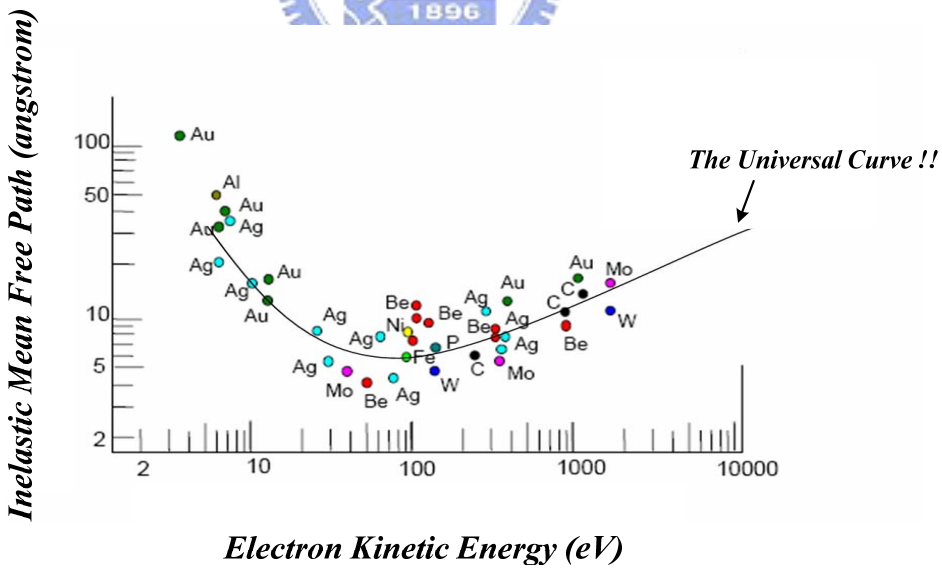


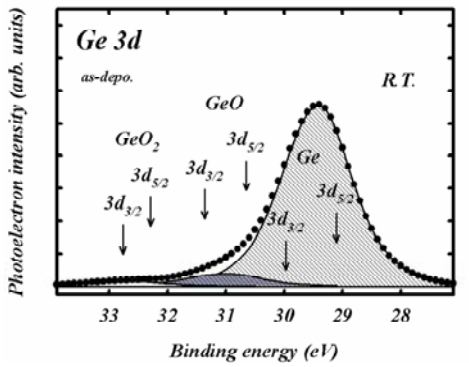
Fig. 2-18 X-ray Photoelectron Inelastic Mean Free Path v.s. Electron Kinetic Energy and the Universal Curve (guide for eyes).

Table 2-2. The detected elements and the calculated detectable depth ~ 3 - 5 λ. Effective detectable depth considers the take-off angle, 60^{O}, of the measurements.

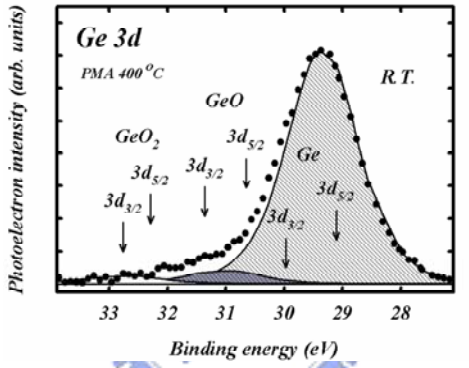
Detected element	*Escaped length λ (A)*	*Detectable depth (A)*	*Effective detectable depth (A)*
O_{1s}	~ 20.0	60.0 – 100.0	52.0 – 86.6
Al_{2p}	~ 26.0	78.0 – 130.0	66.8 – 111.3
Ge_{2p}	~ 8.5	25.5 – 42.5	22.1 – 36.8
Ge_{3d}	~ 28.0	84.0 – 140.0	73.5 – 122.5

Table 2-3. The parameters set for peak fitting of the Ge 3d AR-XPS spectra.

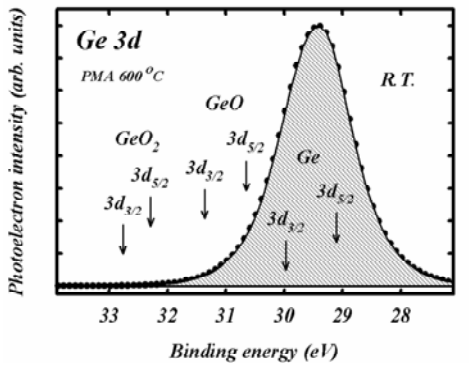
Peak fitting element	*Peak position (eV)*	*FWHM (eV)*	*Ratio (G:0, L:100)*
Ge	29.4	1.2	80
GeO	30.8	1.2	80
GeO_2	32.5	1.2	80



(a)

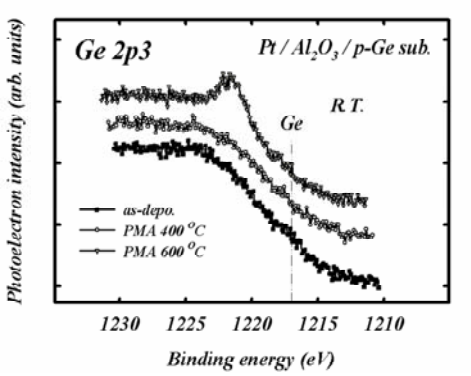


(b)

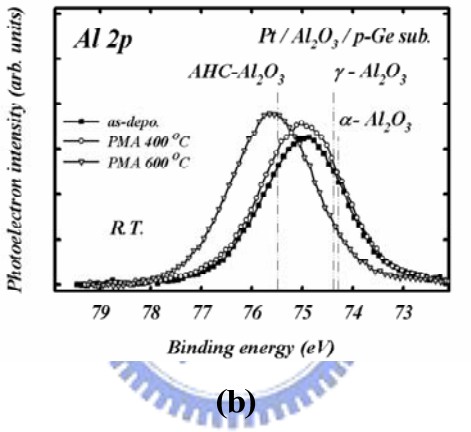


(c)

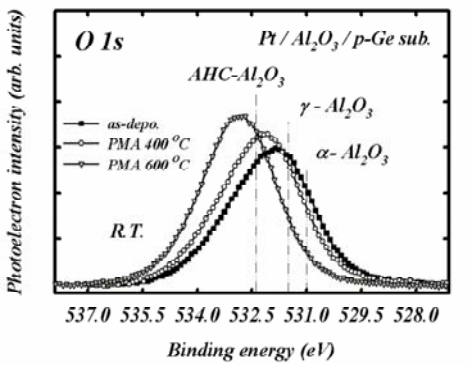
Fig. 2-19 AR-XPS spectra of the 60 cycles ALD films deposited at R.T. (~50 °C) with different thermal treatment for 30 sec; (a) as-depo, (b) PMA 400 °C, and (c) PMA 600 °C.



(a)

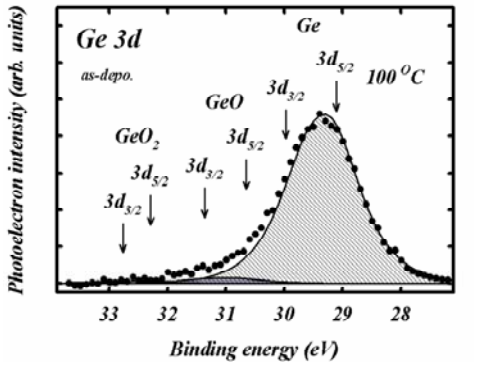


(b)

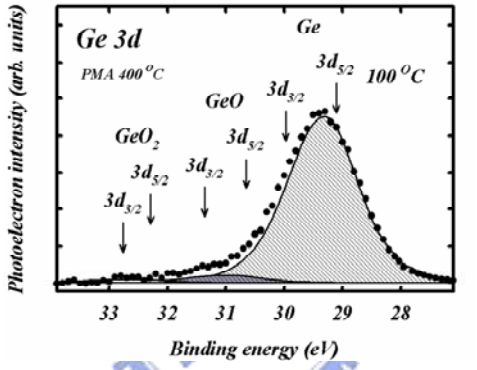


(c)

Fig. 2-20 (a) Ge 2p3, (b) Al 2p, and (c) O 1s AR-XPS spectra of the 60 cycles ALD films deposited at R.T. (~50 ^{O}C) with different thermal treatment for 30 sec.



(a)



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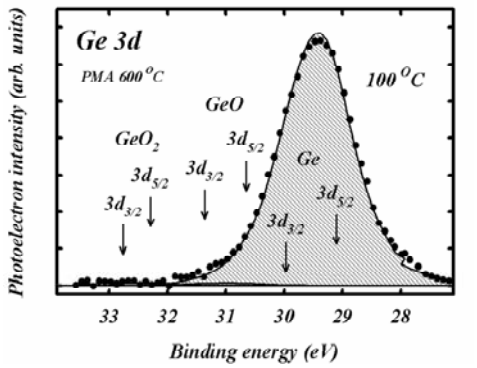
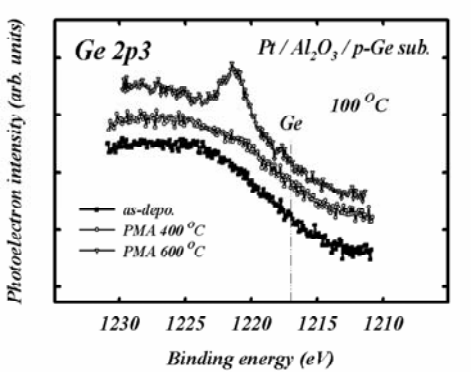
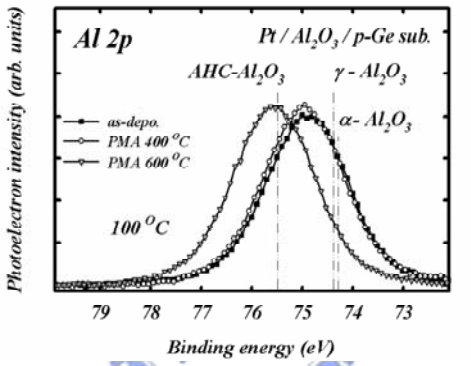


(c)

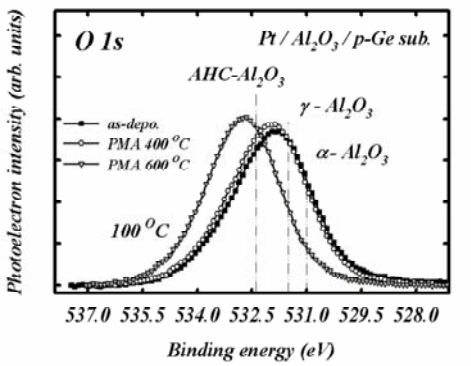
Fig. 2-21 AR-XPS spectra of the 60 cycles ALD films deposited at 100 ^{O}C with different thermal treatment for 30 sec; (a) as-depo, (b) PMA 400 ^{O}C, and (c) PMA 600 ^{O}C.



(a)

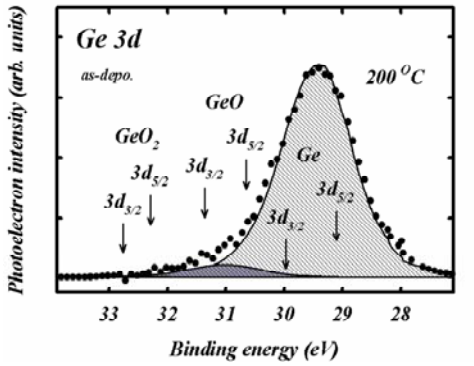


(b)

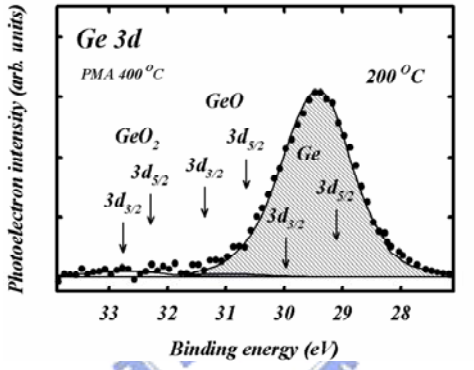


(c)

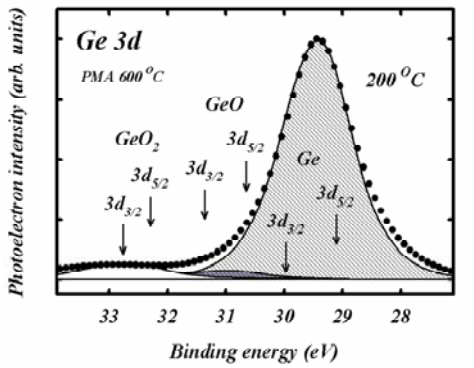
Fig. 2-22 (a) Ge 2p3, (b) Al 2p, and (c) O 1s AR-XPS spectra of the 60 cycles ALD films deposited at 100 °C with different thermal treatment for 30 sec.



(a)

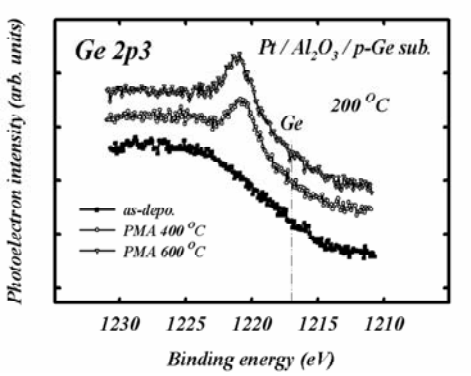


(b)

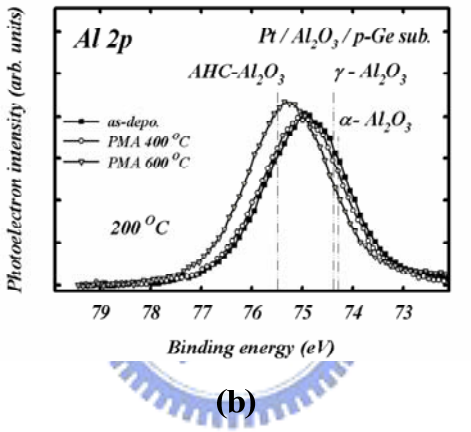


(c)

Fig. 2-23 AR-XPS spectra of the 60 cycles ALD films deposited at 200 °C with different thermal treatment for 30 sec; (a) as-depo, (b) PMA 400 °C, and (c) PMA 600 °C.



(a)



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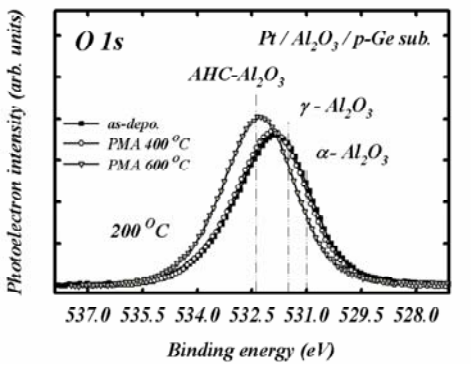
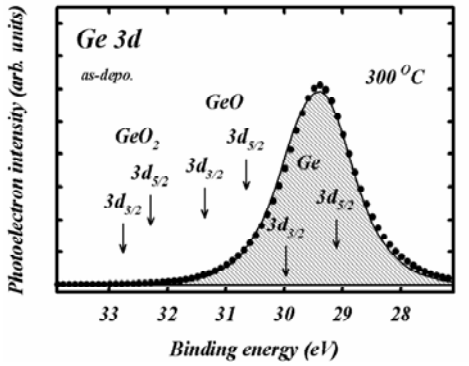
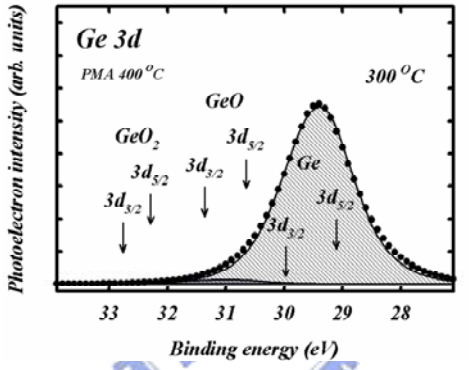


(c)

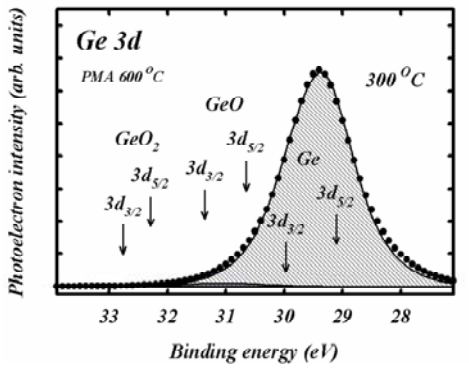
Fig. 2-24 (a) Ge 2p3, (b) Al 2p, and (c) O 1s AR-XPS spectra of the 60 cycles ALD films deposited at 200 °C with different thermal treatment for 30 sec.



(a)

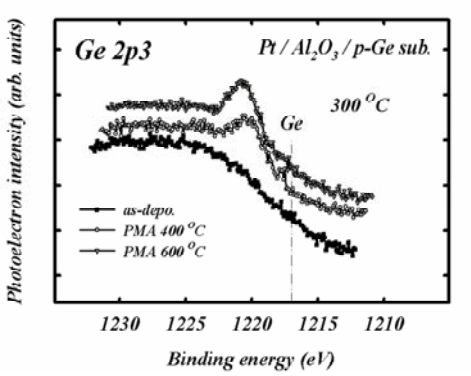


(b)

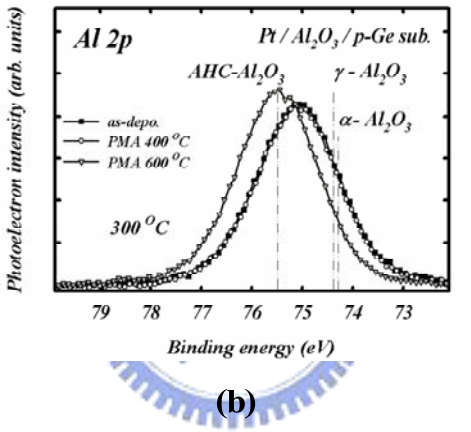


(c)

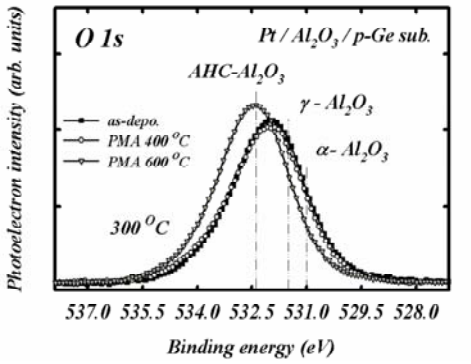
Fig. 2-25 AR-XPS spectra of the 60 cycles ALD films deposited at 300 °C with different thermal treatment for 30 sec; (a) as-depo, (b) PMA 400 °C, and (c) PMA 600 °C.



(a)



(b)



(c)

Fig. 2-26 (a) Ge 2p3, (b) Al 2p, and (c) O 1s AR-XPS spectra of the 60 cycles ALD films deposited at 300 °C with different thermal treatment for 30 sec.

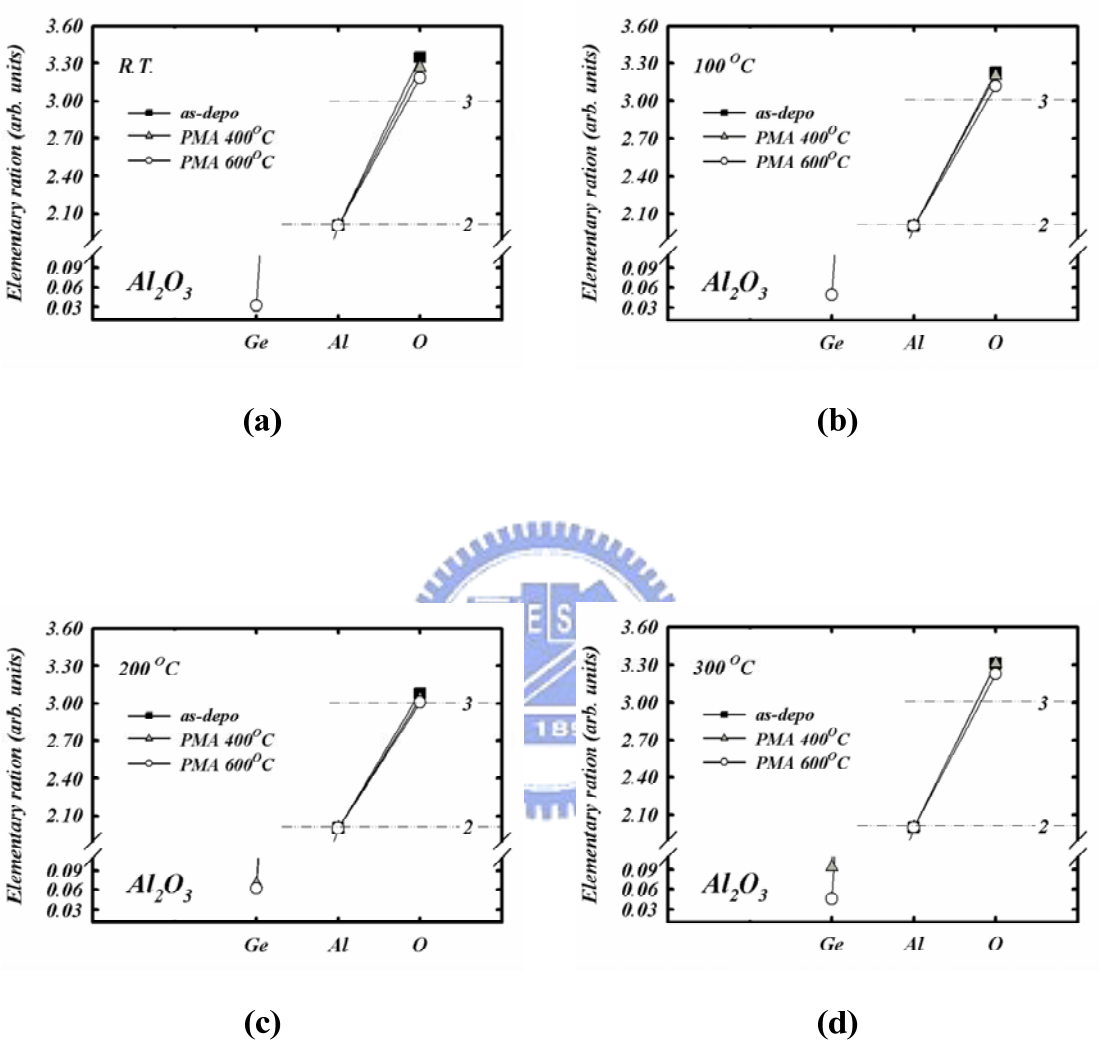
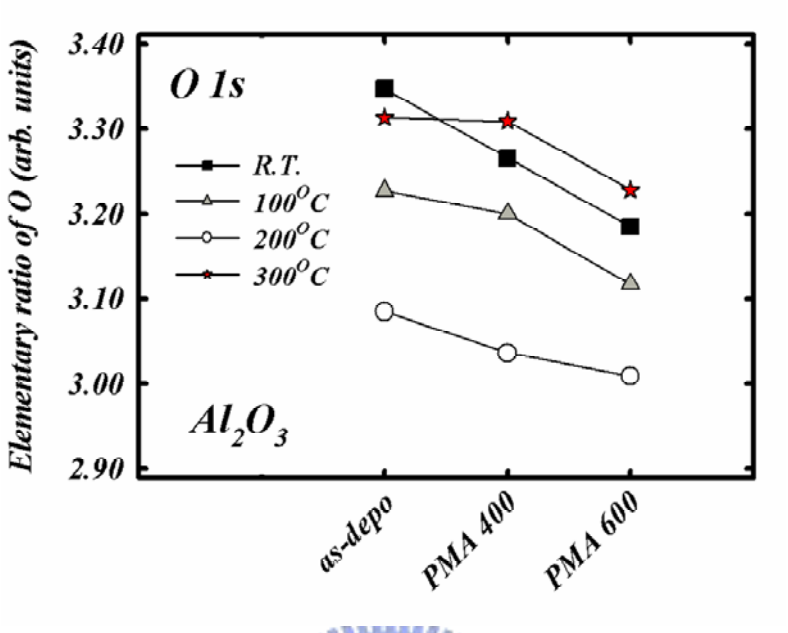


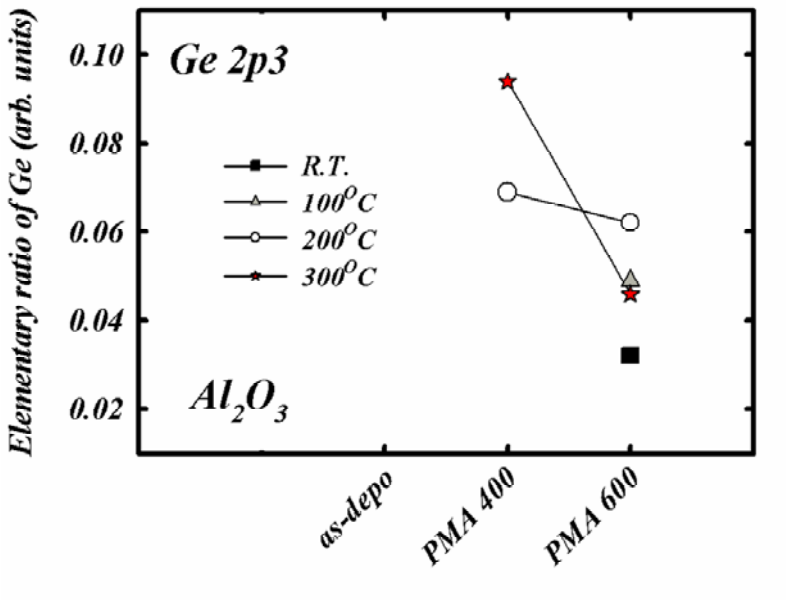
Fig. 2-27 Calculated elementary ratio between Ge (by Ge 2p3 XPS spectra), Al (by Al 2p XPS spectra), and O (by O 1s XPS spectra) of the ALD films deposited at (a) R.T. (~ 50 ^{O}C), (b) 100 ^{O}C, (c) 200 ^{O}C, and (d) 300 ^{O}C; and subjected to different thermal treatment.

Table 2-4. Calculated elementary ratio between Ge (by Ge 2p3 XPS spectra), Al (by Al 2p XPS spectra), and O (by O 1s XPS spectra) of the ALD films deposited at different temperature and subjected to different thermal treatment.

deposition temperature (^{O}C)		***Ge***	***Al***	***O***
R.T. (~ 50)				
	As-depo	***0.06***	***2.00***	***3.35***
	PMA 400 ^{O}C	***0.07***	***2.00***	***3.27***
	PMA 600 ^{O}C	***0.03***	***2.00***	***3.19***
100				
	As-depo	***0.07***	***2.00***	***3.23***
	PMA 400 ^{O}C	***0.09***	***2.00***	***3.20***
	PMA 600 ^{O}C	***0.05***	***2.00***	***3.12***
200				
	As-depo	***0.06***	***2.00***	***3.09***
	PMA 400 ^{O}C	***0.07***	***2.00***	***3.04***
	PMA 600 ^{O}C	***0.06***	***2.00***	***3.01***
300				
	As-depo	***0.06***	***2.00***	***3.31***
	PMA 400 ^{O}C	***0.09***	***2.00***	***3.31***
	PMA 600 ^{O}C	***0.05***	***2.00***	***3.23***



(a)



(b)

Fig. 2-28 Calculated (a) O 1s and (b) Ge 2p3 ratio of the ALD films.

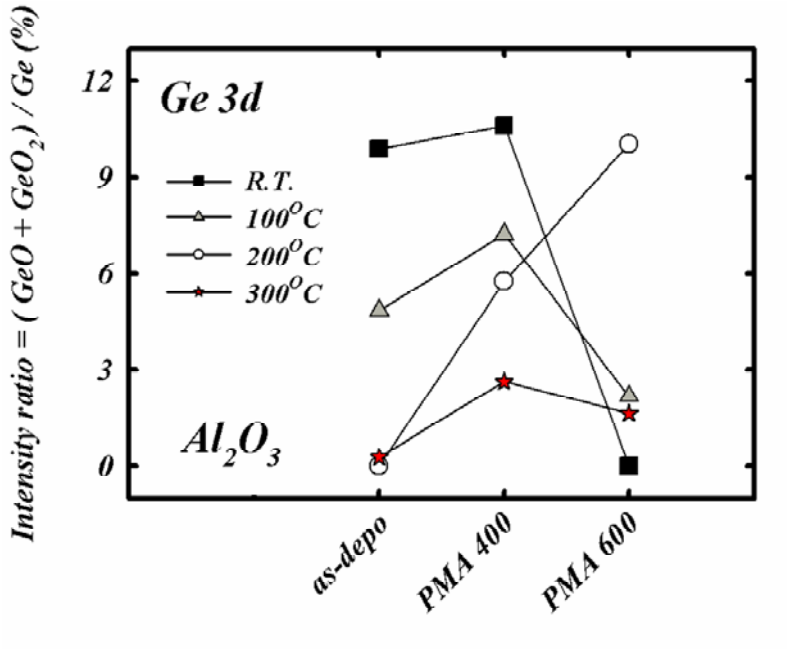
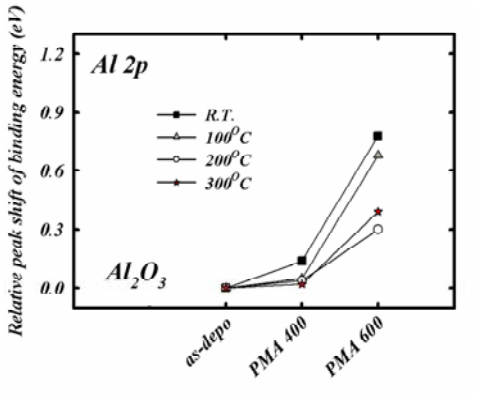
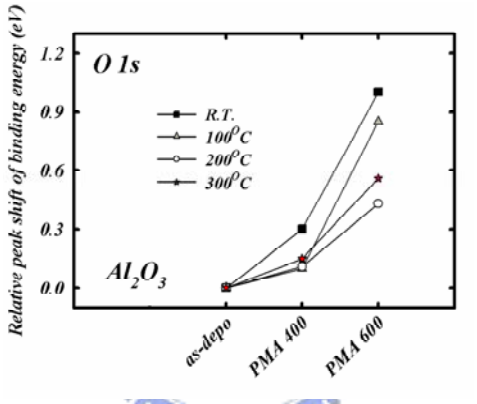


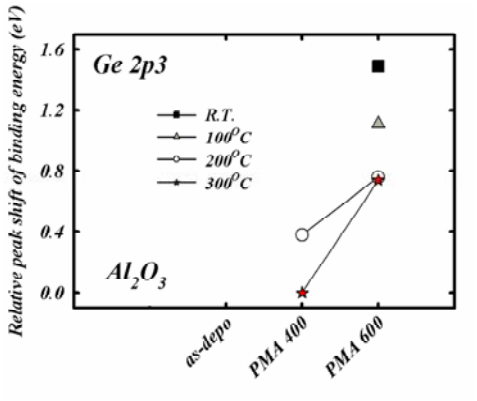
Fig. 2-29 AR-XPS intensity ratio between Ge and GeO_x .



(a)



(b)



(c)

Fig. 2-30 Relative peak shift of (a) Al 2p, (b) O 1s, and (c) Ge 2p3 AR-XPS spectra.

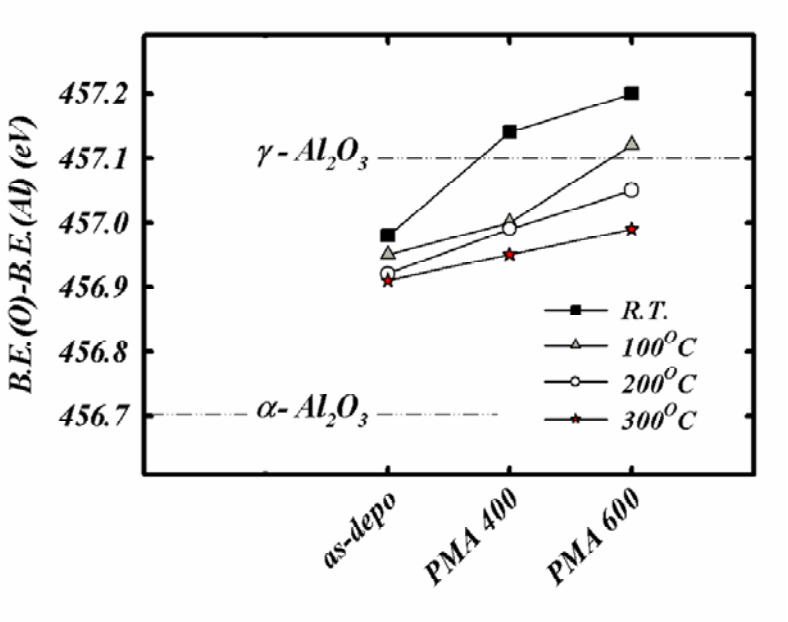


Fig. 2-31 Energy spacing between Al 2p and O 1s AR-XPS spectra peak position.

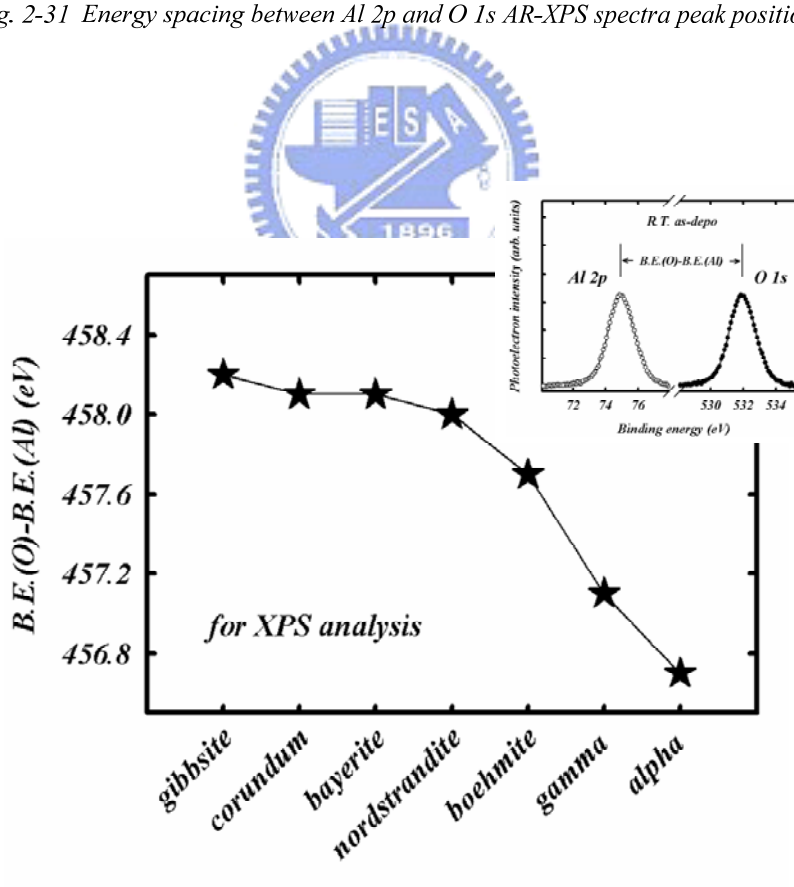


Fig. 2-32 Energy spacing v.s. various Al_2O_3 phase. Inset shows the definition of energy spacing of binding energy between Al 2p and O 1s AR-XPS spectra peak position.

Table 2-5. The standard state database (for temperature of 298.15 K) of the elements formed possibly during the ALD process.

$\Delta H_f°$: Standard enthalpy of formation
ΔG_f : Gibb free energy of formation
S° : Standard molar entropy

compound	$\Delta H_f°$ (kJ/mol)	S° (J/mol)	$\Delta G_f°$ (kJ/mol)
$AlO_{(S)}$	66.94	218.33	1.44
$Al_2O_{(S)}$	-145.19	252.24	-220.86
$AlO_{2(S)}$	-86.19	251.83	-161.74
$Al_2O_{2(S)}$	-394.55	280.90	-478.82
$Al_2O_{3(S)}$	-1675.70	50.92	-1690.98
$GeO_{2(S)}$	-580.00	39.71	-591.91
$H_2O_{(g)}$	-241.83	188.84	-298.48
OH^-	-230.02	-10.90	-226.76
$CO_{(g)}$	-110.53	197.66	-169.83
$CO_{2(g)}$	-393.51	213.79	-457.65
CO_3^{-2}	-675.23	-50.00	-660.23
HCO_3^{-1}	-689.93	98.40	-719.45

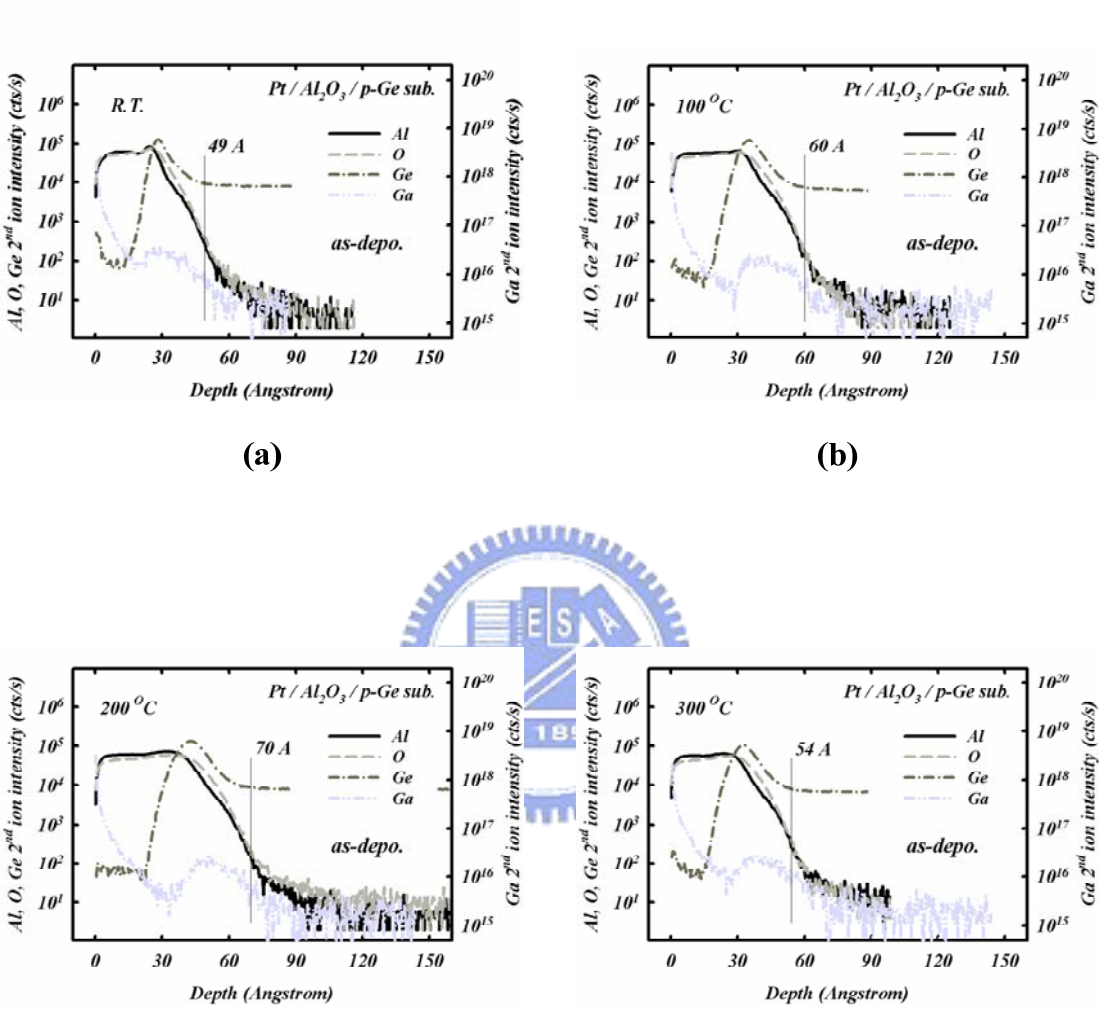
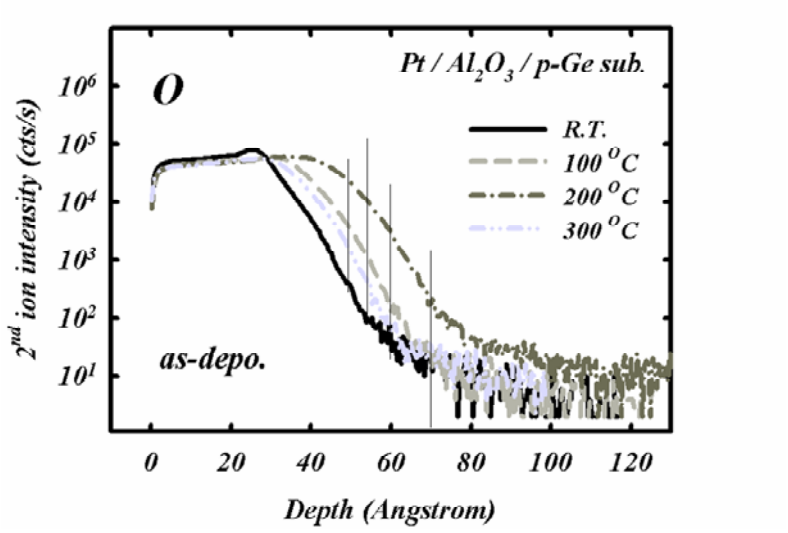
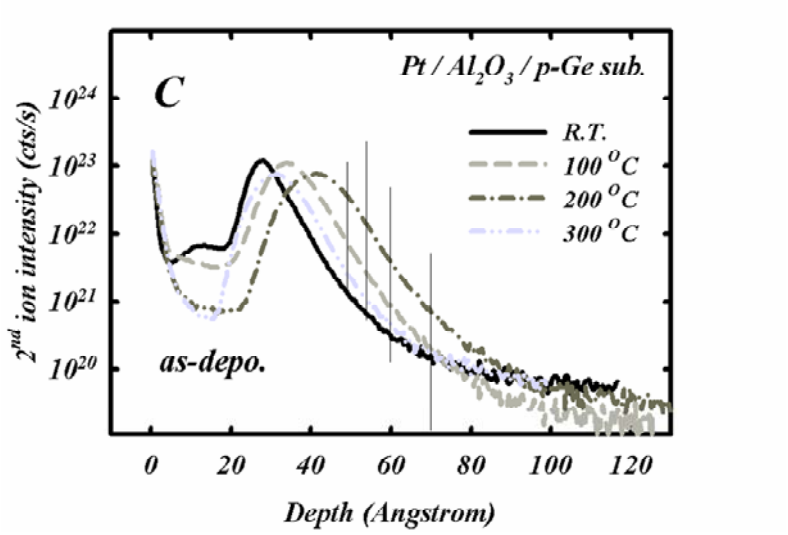


Fig. 2-33 Elements distribution, measured by Secondary Ion Mass Spectroscopy (SIMS), of the ALD films deposited at (a) R.T. (~ 50 ^{O}C), (b) 100 ^{O}C, (c) 200 ^{O}C, and (d) 300 ^{O}C.



(a)



(b)

Fig. 2-34 Measured (a) O and (b) C Secondary Ion Mass Spectroscopy (SIMS) distribution in the ALD films deposited at R.T. (~ 50℃), 100℃, 200℃, and 300℃. The solid lines indicate the film thicknesses.

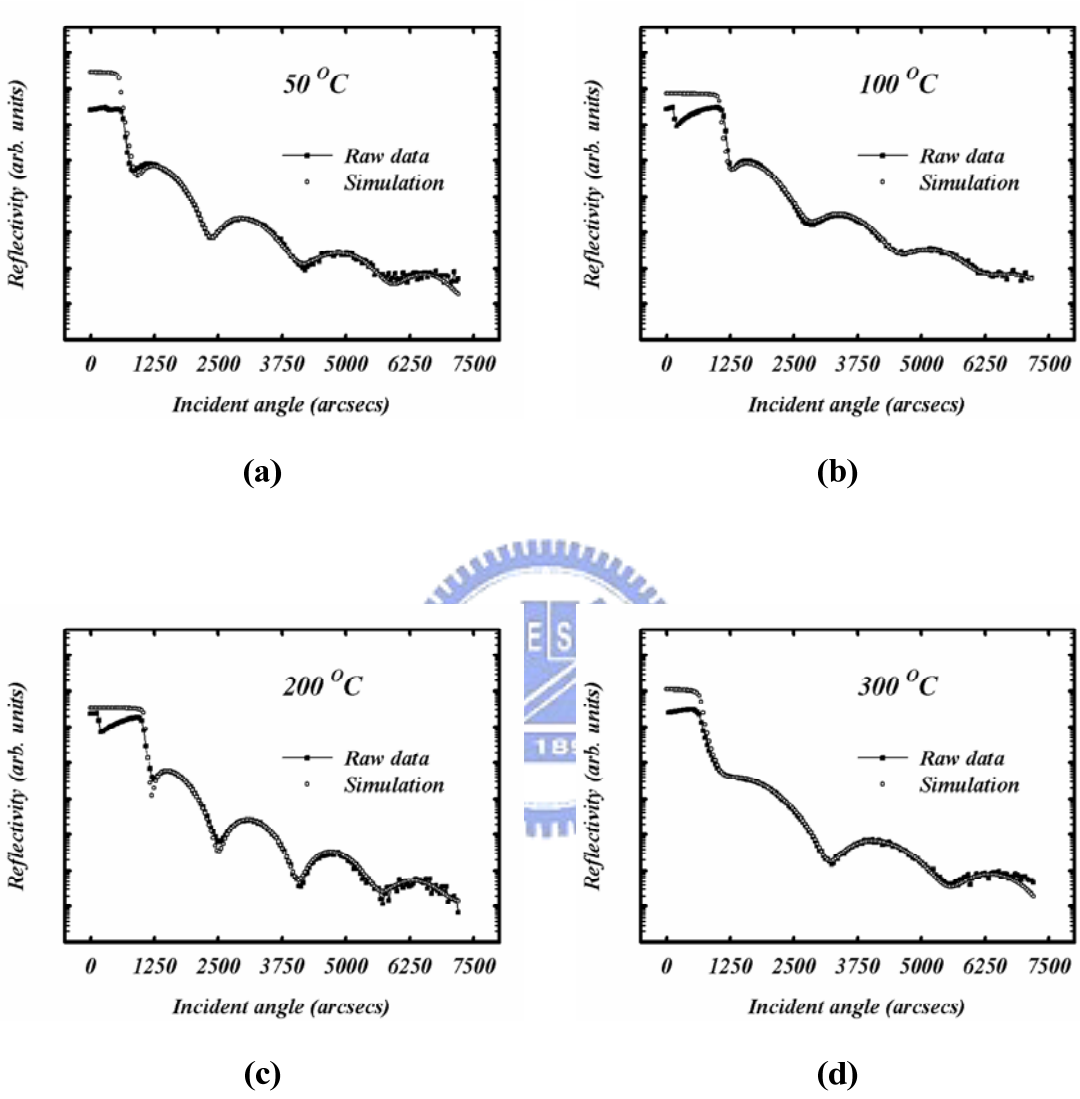


Fig. 2-35 Grazing-Incidence X-Ray Reflectivity (GIXRR) measurement and fitting results of the as-deposited samples grown at (a) R.T. (~ 50℃), (b) 100℃, (c) 200℃, and (d) 300℃.

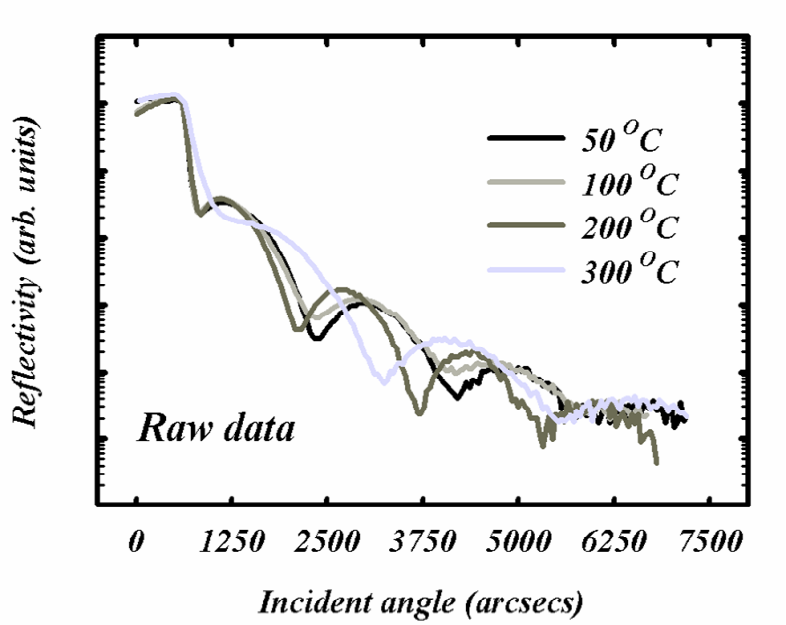


Fig. 2-36 Collection of the Grazing-Incidence X-Ray Reflectivity (GIXRR) measurement results of the samples deposited at R.T. (~50℃), 100℃, 200℃, and 300℃.

Table 2-6. Grazing-Incidence X-Ray Reflectivity (GIXRR) fitting results of the as-deposited samples grown at various temperatures by the professional XRR fitting software —Mercury.

deposition temperature (°C)	fitting layer	thickness (Å)	density (g/cm^3)	roughness (Å)
R.T. (~ 50)				
	Ge		5.27	
	O in-diffus.	9.6	4.69	← 1.5
	GeO_2	7.3	2.92	
	$Ge_xAl_yO_z$	1.5	1.91	
	alpha Al_2O_3	42.2	3.30	← 1
100				
	Ge		5.38	
	O in-diffus.	23.7	3.99	← 1.5
	GeO_2	2.2	3.54	
	$Ge_xAl_yO_z$	2.2	4.12	
	alpha Al_2O_3	56.6	3.53	← 3.6
200				
	Ge		6.76	
	O in-diffus.	17.1	3.94	← 6.7
	GeO_2	~ 0		
	$Ge_xAl_yO_z$	10.1	4.04	
	alpha Al_2O_3	58.6	3.57	← 2.8
300				
	Ge		5.38	
	O in-diffus.	8.3	4.14	← 9.6
	GeO_2	~ 0		
	$Ge_xAl_yO_z$	15.8	3.51	
	alpha Al_2O_3	31.0	3.73	← 1.9

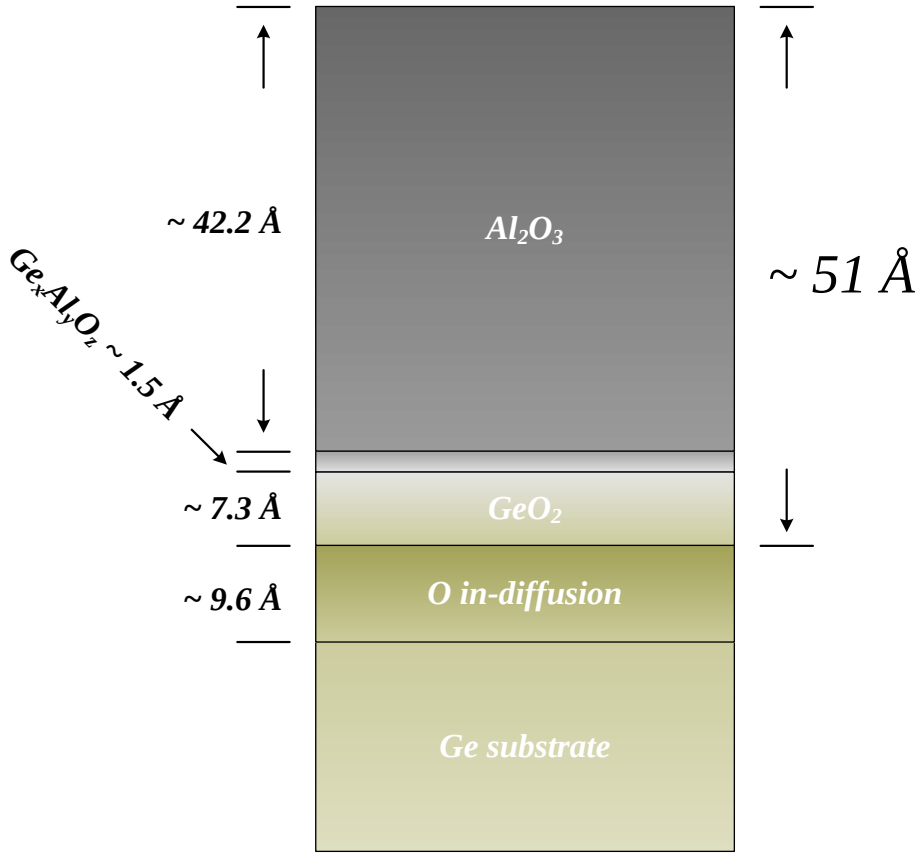


Fig. 2-37 Illustration of the XRR modeling structure and result of the film deposited at 50 °C.

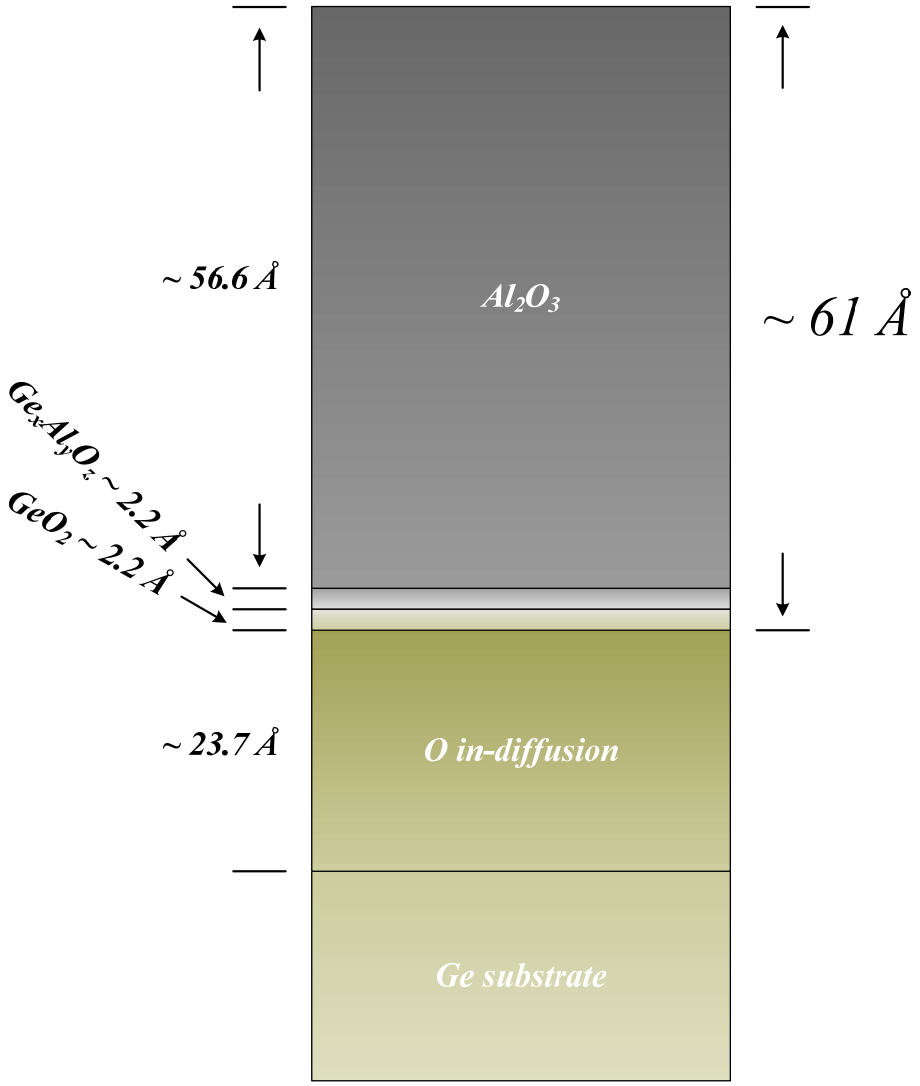


Fig. 2-38 Illustration of the XRR modeling structure and result of the film deposited at 100 °C.

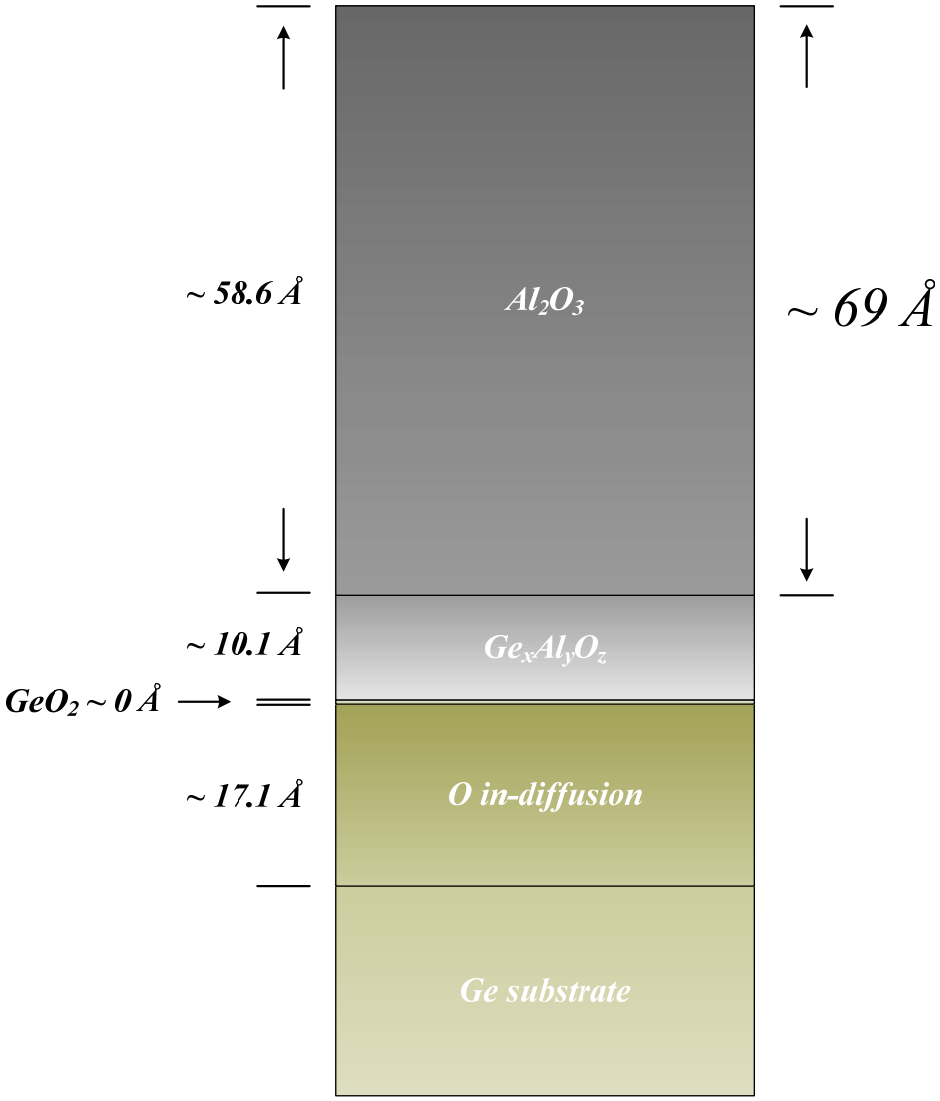


Fig. 2-39 Illustration of the XRR modeling structure and result of the film deposited at 200 °C.

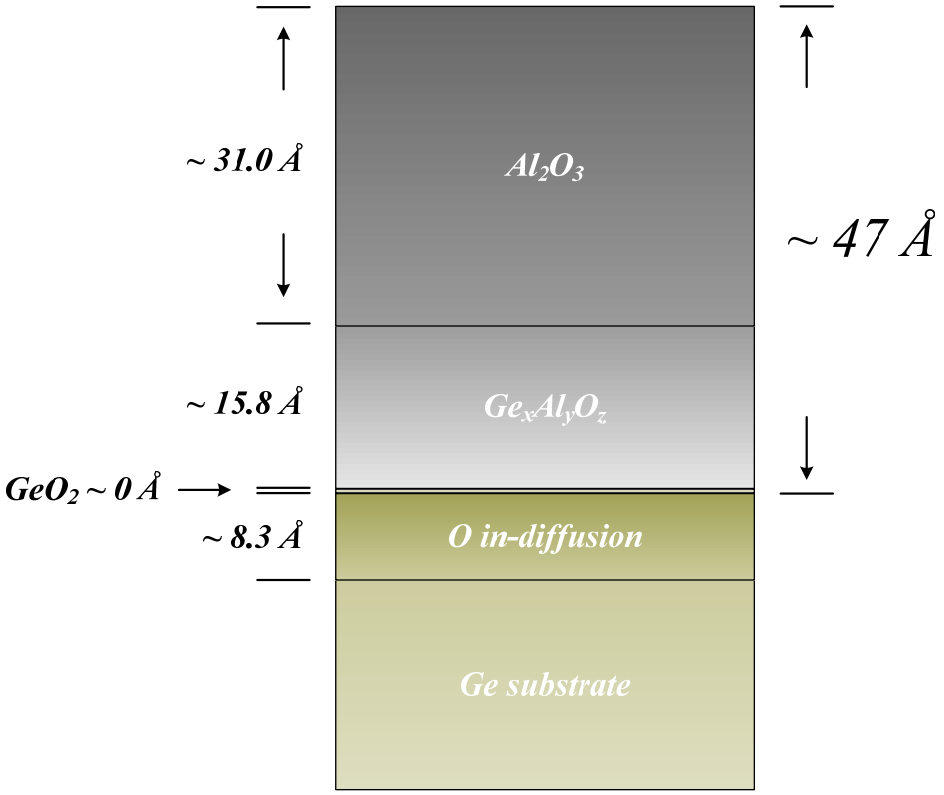


Fig. 2-40 Illustration of the XRR modeling structure and result of the film deposited at 300 °C.

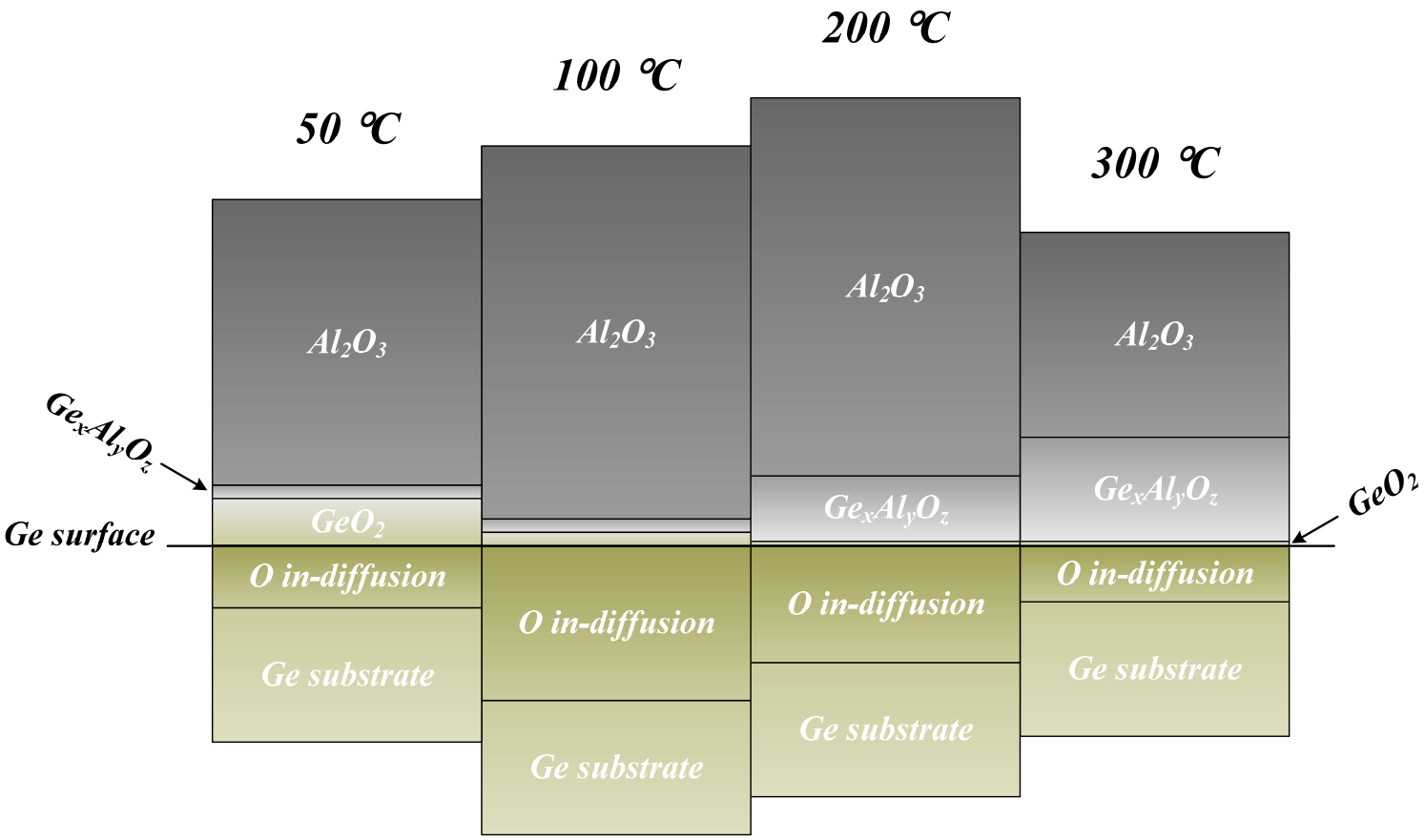
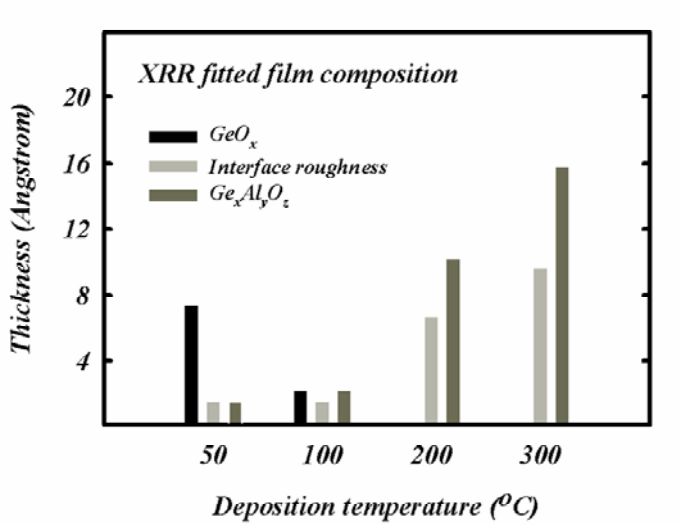
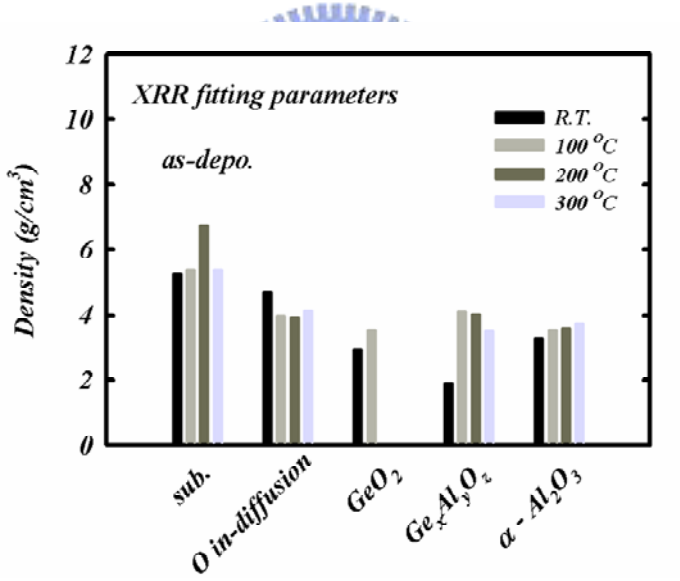


Fig. 2-41 Collection of all the XRR modeling structures and results of the film deposited at 50 ~ 300 °C.



(a)



(b)

Fig. 2-42 Collection of the GIXRR curve fitting parameters of the ALD films deposited at R.T. (~ 50℃), 100℃, 200℃, and 300℃.

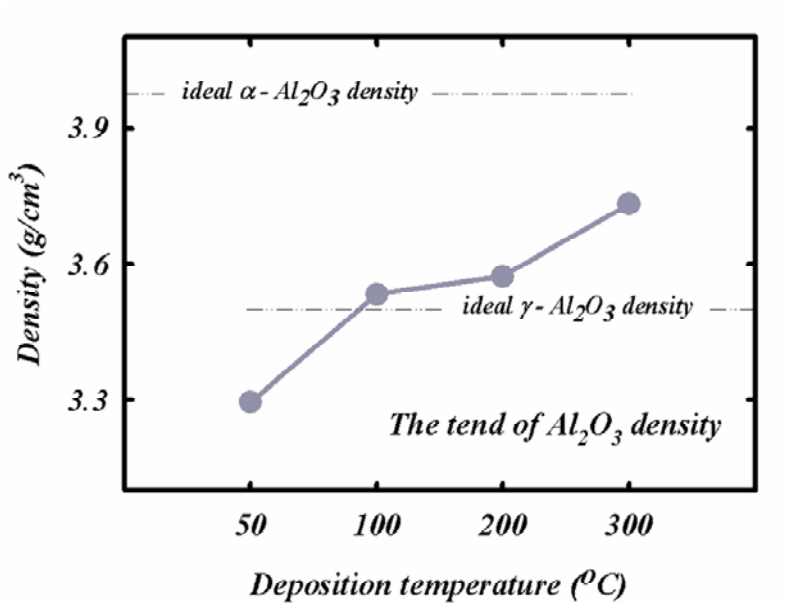


Fig. 2-43 Comparison of the GIXRR fitting density of the Al_2O_3 films deposited at R.T. (~50℃), 100℃, 200℃, and 300℃.

Chapter 3

Electrical characteristics of atomic-layer-deposited Al_2O_3 on Ge substrate

3-1 Introduction

In order to fabricate an ideal Ge MOSFET with ALD Al_2O_3 gate dielectric, both electrical and physical characteristics of the gate stack must be studied comprehensively in all respects. In chapter 2, we had showed the essential analyses of physical characteristics and figured out the whole story about the thermal and intrinsic properties of the ALD films subjected to various thermal processes. In this chapter, it is necessary to complete the analyses of electrical performances; and, then, we could go on to the next chapter involving fabricating a MOSFET along with the observations in those two chapters. At the beginning of this chapter, we would show the study on different kinds of thermal treatments on the films deposited at 200 °C for improving the gate stack and pick out several proper conditions – PMA 400 and 600 °C – to execute on the gate stacks which had been studied in chapter 2. Then we displaced the effects of various thermal processes, which contained different deposition and annealing temperatures, on the C-V and I-V characteristics of them.

Flat band voltage and hysteresis are also extracted for their relationship with the qualities and trap behavior of those films. Interface states density (Dit) is a much important parameters that will affect the switch efficiency of a MOSFET through body effect coefficient and the performance of mobility through coulomb or surface roughness scattering. We utilize two methods – High-Low Frequency and Conductance method – to estimate how many Dit exist near the substrate surface and show if the calculations by those two method are consistent with each other. Then, we did further improving this film which has minimum Dit by Forming gas Annealing (FGA) and calculated the extent of improvement by Conductance method. By combining the results of chapter 2 with chapter 3, we got a window of temperature to deposit the ALD Al_2O_3 for fabricating the Ge p-MOSFETs.

3-2 Experimental Procedures

The gallium (Ga, concentration ~ 2e14 /cm^2) doped Ge substrates were used to fabricate the Pt/ALD-Al_2O_3/Ga-doped Ge/Al MOSCAPs. After broking the flesh Ge wafer into fragments, we consulted the results of the research of C. C. Cheng et al. [7-8] to clean the Ge fragments in several cycles of sequential dilute HF (HF:H_2O ~ 1:30) and deionized (D.I.) water rinses followed by a last-HF dip and N_2 drying. Then, in order to investigate the effect of deposition temperature on such a MOS gate stack in all respects, we used an atomic-layer-deposition system to grow the gate dielectrics at different temperatures in variant deposition cycles – 60 and 80 cycles – on the cleaned and HF-lasted p-type Ge substrates in Instrument Technology Research Center (ITRC). In this ALD system, tri-methyl-aluminum (TMA), $Al(CH_3)_3$, and H_2O were chosen as the metal source and oxidant that were pulsed alternatively into the reactor for 1 sec; and per pulse separated by N_2 purge of 10 sec to remove redundant reactants during the process. TMA were often-used as the aluminum precursor due to its thermal stability, high vapor pressure (8.4 torr) and highly exothermic reaction with H_2O. During each cycle of reactions, the chamber was held out at a constant pressure about 10 torr. Then, some samples were subjected to 30 sec 400 °C post deposition annealing (PDA), by a rapid thermal annealing (RTA) system in N_2

(pressure~ 1 atm) ambient. With the help of shadow mask, we left out the lithography process and defined the platinum (Pt) gate electrodes through a reactive sputtering system in Ar (flow rate~ 24 sccm) ambient. Before thermally coating aluminum (Al) on the backsides of the semi-manufactured samples, we split them into several groups so that post metallization annealing (PMA), by a rapid thermal annealing (RTA) system in N_2 (pressure~ 1 atm) ambient, could be performed at different temperatures (400 and 600 °C) but equal time duration (30 seconds) for studies of the thermal stability of such a MOS gate stack. The overall fabrication processes of the Ge MOSCAPs were illustrated summarily in Fig. 2-6 for simple and easy to follow. After the fabrication of the MOSCAPs, we measured the capacitance-voltage (C-V) and current-voltage (I-V) characteristics by HP4284 precision LCR meter and Keithley 4200 semiconductor characterization system, respectively. For calculating the Dit by conductance method, we also measured the conductance-voltage (G-V) by HP4284 precision LCR meter along with the measurements of capacitance-voltage (C-V) and current-voltage (I-V) characteristics. The frequencies of electrical measurements are range form 1 kHz to 1 MHz for Dit fitting by conductance method. In addition, for the ascertaining the types of the trap and fixed oxide charge, all the electrical measurements were operated from accumulation (negative gate bias) to inversion mode (positive gate bias) except for trap analyses involving one direction only.

3-3 Results and Discussion

3-3-1 The effects of various thermal treatments on the electrical performance of the gate stacks with ALD Al_2O_3 films deposited at 200 °C.

Figures 3-1~3 illustrate the electrical characteristics of the films with PDA 400 °C+PMA 400 °C, No PDA+PMA 400 °C, No PDA+PMA 500 °C, and No PDA+PMA 600 °C thermal treatments. The solid line located at about 1.1 V is labeled to indicate the ideal flat band voltage (V_{fb}) in our cases. By comparing the first two cases – PDA 400 °C+PMA 400 °C and No PDA+PMA 400 °C, we preferred a PMA process rather than a PDA one which increased the gate leakage current severely and interface states somewhat. It also shows that increase of PMA temperature would eliminate the hump near conduction band in spite of the deviation of V_{fb} rising up with increase of annealing temperature. Fig. 3-3 (a) presents the trend of shift of V_{fb} against the thermal treatments. V_{fb} could be extracted while the measured capacitance is equal to the flat band capacitance defined as eq. 3.1;

$$C_{FB} = \frac{C_{L_D} \cdot C_{acc}}{C_{L_D} + C_{acc}} \qquad (3.1)$$

C_{FB} : *flat band capacitance*
C_{acc} : *accumulation capacitance*
C_{L_D} : *Debye length related capacitance*

$$L_D = \sqrt{\frac{\varepsilon_{Ge}}{qN_d}\left(\frac{kT}{q}\right)}$$

L_D : *Debye length*
ε_{Ge} : *germanium substrate permitivity*
N_d : *substrate doping level*

But, it is difficult to extract the value of V_{fb} *by eq. 3.1 due to thicker* L_D *resulted form lower doped Ge substrte we used and lower* C_{FB} *that always has a calculated value out of the range of measured C-V. So, we use eq. 3.2 instead of eq. 3.1 to estimate* V_{fb}*;*

$$C_{FB} = \frac{5 \cdot C_{L_D} \cdot C_{acc}}{5 \cdot C_{L_D} + C_{acc}} \qquad (3.2)$$

The dash line designates the position of ideal V_{fb}*. There are two possible mechanisms to cause the* V_{fb} *shift up;*

1- *Negative fixed oxide charge (NFOC).*

2- *Electron trap (ET).*

And, there are two possible mechanisms to cause the V_{fb} *shift down;*

1- *Positive fixed oxide charge (PFOC).*

2- *Hole trap (HT).*

Based on the trap analyses of the films deposited at various temperature with 60 cycles in Figs. 3-19 and 3-20, we could conclude that PDA 400 °C+PDA 400 °C would leaded to a lot of NFOC in comparison to No PDA+PDA 400 °C case. By combining with the results from chapter 2, we could find that more incorporation of Ge and GeO_2 into the ALD films would build up many HT and more PFOC for severely destroyed film resulted from Ge out-diffusion through the vapor-like GeO while increasing the PMA temperature. Both those two mechanisms would lower down the value of V_{fb}. In addition, from Figs. 3-19 and 3-20, we could find that the ALD films are easily to trap electron disregarding what the deposition temperature you chose. Based on those discussed above, we could understand why the hysteresis has the behavior showed in Fig. 3-3 (b). Then, further taking consideration of the proper temperature range [40, 41, 42, 43] for activating the boron (B) doped P-N junction that will be discussed in chapter 4, we studied the effects of PMA 400 and 600 °C on those gate stacks with ALD dielectrics deposited at various temperatures.

3-3-2 The effects of various thermal treatments on the electrical performance of the gate stacks with ALD Al_2O_3 films deposited at R.T. (~ 50 °C), 100 °C, 200 °C, and 300°C.

Figures 3-4~5 show the essential C-V and I-V electrical performance. The I-V implies that the films deposited at 100 and 200 °C were robust to resist the thermal

stress while suffering to PMA 600 °C. For the film deposited at 50 °C, we considered that the increase of gate leakage current after annealing at 600 °C is due to the high conc. of non-reacted CH_3^- bond incorporated (caused by less complete ALD reaction) into the film as leakage medium for carriers. For the film deposited at 300 °C, that is the contribution of higher Ge incorporation and interface roughness to such high gate leakage while suffering from PMA 600 °C thermal treatment. Fig. 3-6 implies that the hump near conduction band increased with deposition temperature and got eliminated while being annealed at 600 °C. By extracting Vfb and hysteresis in Fig. 3-7 and combining the results showed in Fig. 3-19~20 and chapter 2, we could boldly conclude that an unsound film deposited at 50 °C and high Ge-related compounds (Ge, GeO_x, and GeO_2) incorporated film deposited at 200 ~ 300 °C would produce many HT and NFOC, respectively. We could also find that the destroyed film suffered from Ge out-diffusion would cause many PFOC from the case of film deposited at 300 °C while being subjected to PMA 400 and 600 °C thermal treatments. Fig. 3-8 shows the relationship between Capacitance Equivalent Thickness (CET) and gate leakage current extracted at $V_g = V_{fb} - 1.5$ V along with the results on SiO_2/Si gate stacks. The same color of the symbols represents the films subjected to one kind of thermal treatments and the same kind of symbols represents the films deposited at the same temperature. It shows that the dielectric constant of the films deposited at 100 or 300

°C can achieve 9.6 ~ 9.8 while suffering from PMA 600 °C thermal treatment. For that of the film deposited at 200 °C, we could only receive a film with dielectric constant about 6 due to thicker GeO_x interfacial layer or higher Ge-related compounds incorporation. For that deposited at 50 °C, both higher C incorporation and more porous like of the film leaded to unacceptable gate leakage and lower dielectric constant about 6. We believe that higher CET of those samples annealed at 400 and 500 °C is due to thicker GeO_x interfacial layer. Based on High-Low frequency (HLF) method, we did further calculation of Dit of those gate stacks with PMA 400 °C and summarized that in Fig. 3-9. It shows that the gate stack with ALD film deposited at 100 °C would own the minimum amount of Dit due to flat interface and less formation of GeO_x compared with that of the 50 °C one. Because of higher interface roughness, we obtained a film with higher Dit at higher deposition temperature. For more precision calculations and a more consistency result, we calculated Dit by the powerful method – Conductance (G-V) method – in comparison to that calculated by HLF method mentioned above.

3-3-3 The powerful Dit calculation method – Conductance (G-V) method.

Figures 3-10 ~ 11 show the $\langle G_P \rangle/w$ (discrete symbols) calculated by eq. 3.3 and the curves (solid lines) simulated by eq. 3.4 for the films subjected to PMA 400 and

600 °C [44, 45] thermal treatments and Fig. 3-12 shows that for $V_g = V_{th}$ for rough comparison.

$$\frac{< G_P >}{w} = \frac{w C_{ox}^2 G_m}{G_m^2 + w^2 \cdot (C_{ox} - C_m)^2} \tag{3.3}$$

$$w = 2\pi \cdot f$$

C_m : *the measured capacitance*
G_m : *the measured conductance*
C_{ox} : *the oxide layer capacitance*
f : *the measurement frequency*

$$\frac{< G_P >}{\omega} = \frac{q D_{it} (2\pi \cdot \sigma_S^2)^{-0.5}}{2\xi} \int_{-\infty}^{\infty} exp\{ -\frac{\eta^2}{2\sigma_S^2} - \eta \} \cdot ln\{ 1 + \xi^2 \cdot exp\{ 2\eta \} \} \cdot d\eta$$

$$\eta = v_S - < v_S >$$
$$\xi = w \cdot \tau_P$$

D_{it} : *interface state density*
σ_S^2 : *the variance of band bending (in units of kT/q)*
τ_P : *characteristic time of holes*
v_S : *the band bending*
$< v_S >$: *the mean value of band bending*

$$\frac{< G_P >}{\omega} = \frac{q D_{it}}{\sigma_S \sqrt{2\pi}} \left\{ arctan(B\omega \bar{\tau}_{max}) - arctan(\omega \bar{\tau}_{max} / B) \right\} \tag{3.4}$$

$$B = exp\{ \sqrt{2\pi} \cdot \sigma_S / 2 \}$$

By simulating the calculated data from C_m and G_m by eq. 3.4, we could extract the

value of Dit that had been summarized in Fig. 3-13. It shows a consistent result with that of the Dit calculation by HLF method. The film deposited at 100 °C still has the minimum amount of Dit (~ $2x10^{12}$ /cm^2) and all of the Dit of those films deposited at various temperatures increased with increase of PMA temperature. For further improving the Dit of the gate stack with ALD film deposited at 100 °C, we performed the FGA thermal treatment to minimize the value of Dit. Figs. 3-14 and 3-15 show, respectively, the multi-frequencies of the measured C-V characteristics and fitting results of the calculated $<G_P>/w$ for the as-deposited and FGA treated films. We summarized the Dit extraction in Fig. 3-16 from the simulated results in Fig. 3-15 and got a Dit improved film about 1/10 times Dit of that as-deposited. We also displaced the effects of all the thermal treatments on the gate stacks with Al_2O_3 dielectrics deposited at 100 °C in Figs.3-17 ~ 18. We could do really get a film with Dit less than 10^{12} /cm^2 after subjecting it to the thermal treatment – FGA.

3-4 Summary

We had displaced all the electrical performances what should be present of those ALD films deposited at 50, 100, 200 and 300 °C in this chapter. By analyzing the trap characteristics through continuing increasing the bias voltage in one sweep direction, extracting V_{fb} while getting the measured capacitance equal to the value of C_{FB} defined by eq. 3.2, and calculating the hystereses of those samples with different thermal processes, we figured out the possible mechanisms contributing to HT, ET, PFOC, and NFOC along with the results from chapter 2. We also showed the relationship between CET and leakage current of our results in comparison to that on the traditional SiO_2/Si gate stacks and estimated the dielectric constants (about 6 ~ 9.8) roughly by inserting the physical thicknesses measured by HRTEM of those as-deposited ALD films. Based on the results from chapter 2, we pointed out the possible reasons for those unacceptable conditions showed in Fig. 3-8. We have tow consistent results of Dit calculation by G-V and HLF methods and succeed further improving it of the best condition (deposition temperature ~ 100 °C) to form a gate stack with Dit less than 10^{12} /cm^2 by use of the thermal treatment – FGA.

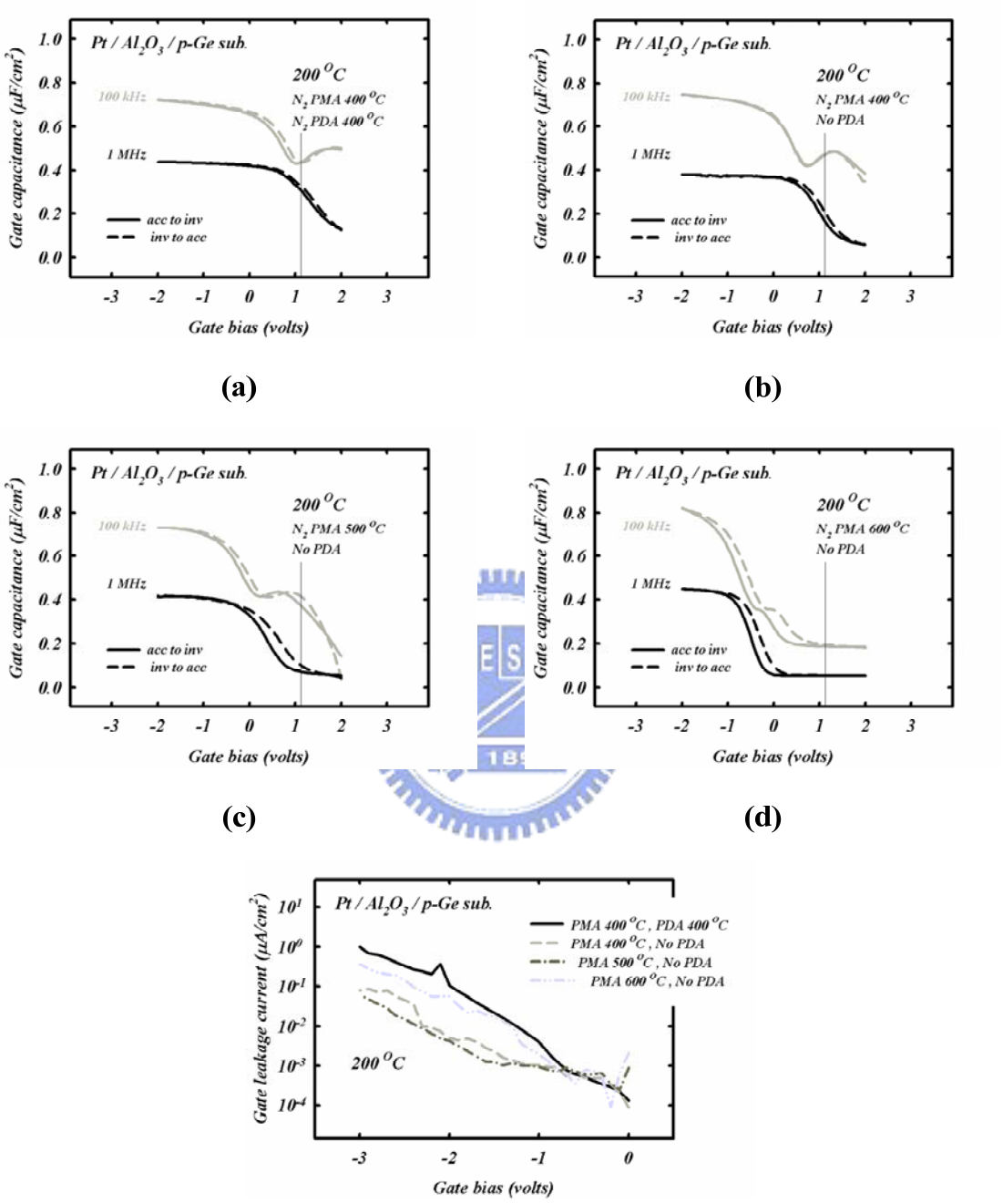
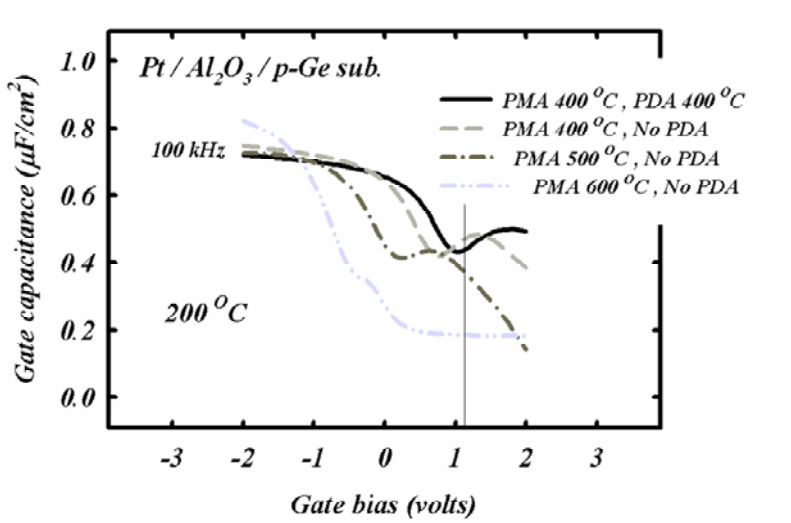
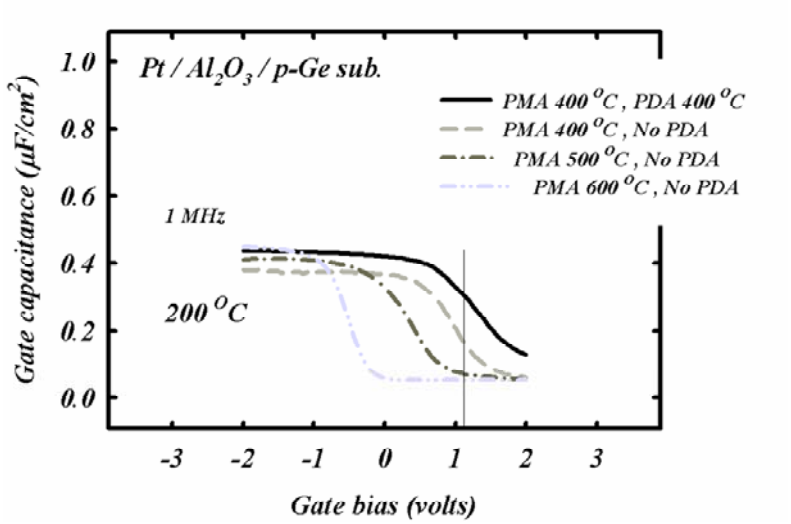


Fig. 3-1 The (a) ~ (d) C-V and (e) I-V electrical performance of the 80 cycs. ALD Al_2O_3 films deposited at 200℃ with different thermal treatment; (a) PDA 400℃ + PMA 400℃, (b) No PDA + PMA 400℃, (c) No PDA + PMA 500℃, (d) No PDA + PMA 600℃, for 30 sec.

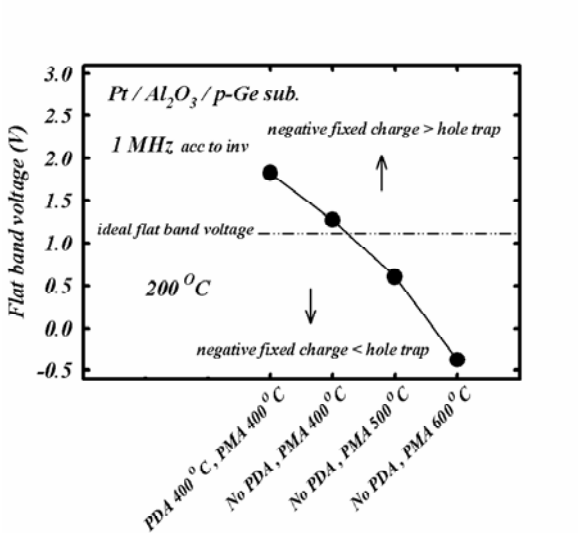


(a)

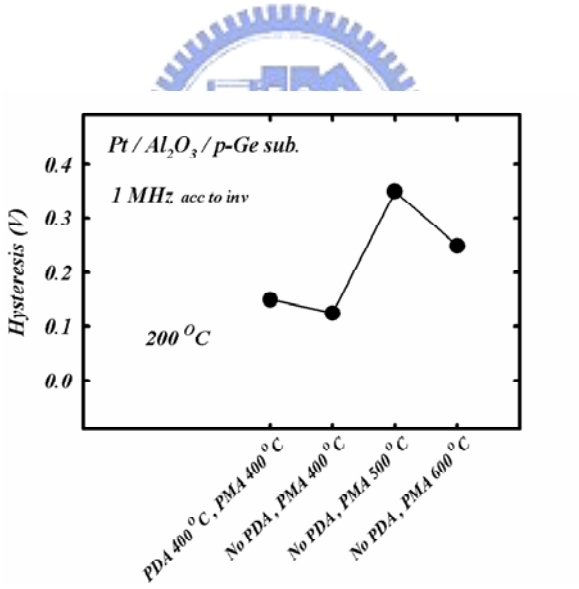


(b)

Fig. 3-2 The (a) 100 kHz C-V and (b) 1 MHz C-V electrical performance of the 80 cycs. ALD Al_2O_3 films deposited at 200℃ with various thermal treatments.



(a)



(b)

Fig. 3-3 The (a) 1 MHz flat band voltage and (b) 1 MHz hysteresis of the corresponding C-V electrical performance of the 80 cycs. ALD Al_2O_3 films deposited at 200℃ with various thermal treatments.

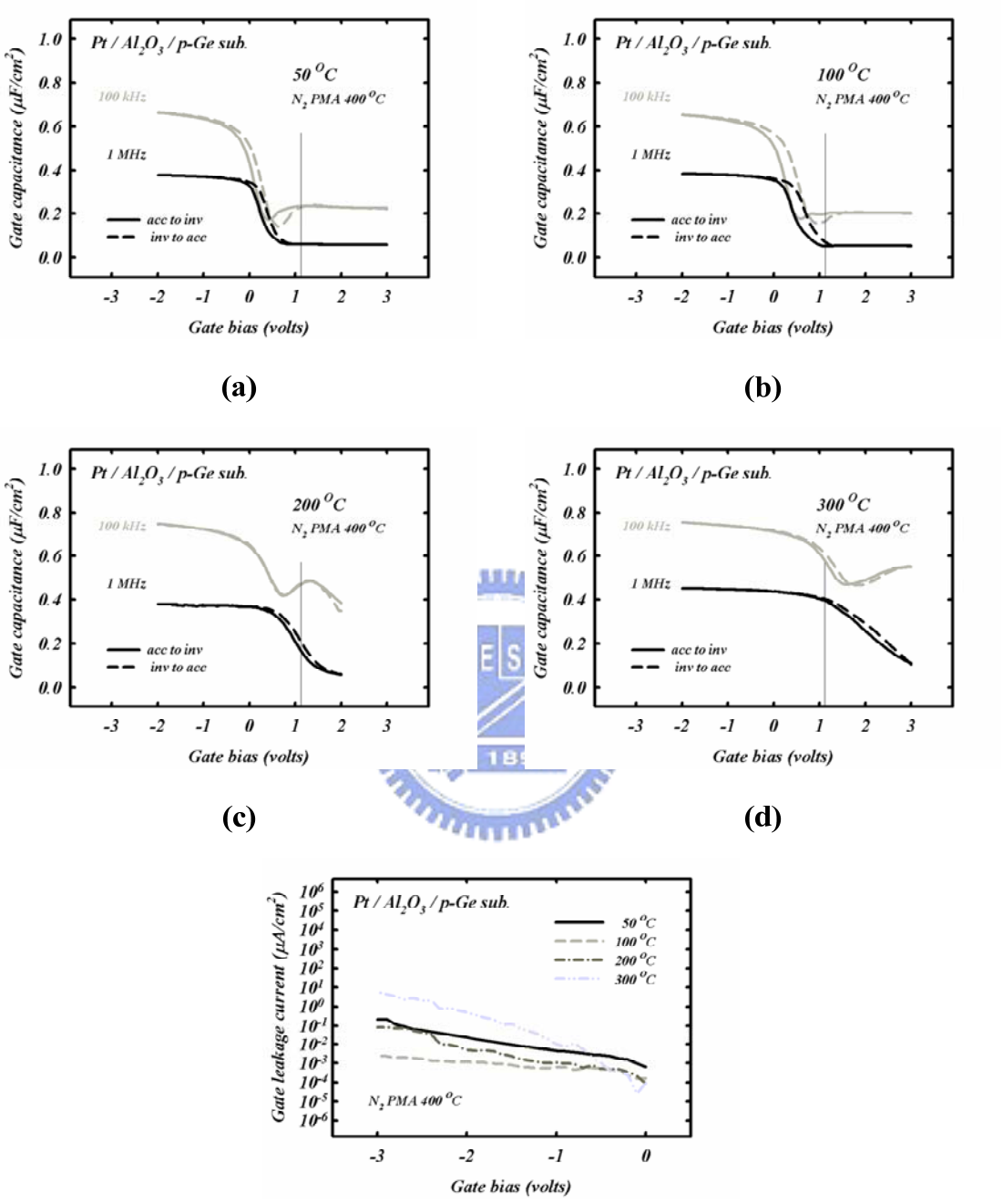


Fig. 3-4 The (a) ~ (d) C-V and (e) I-V electrical performance of the 80 cycs. ALD Al_2O_3 films deposited at (a) R.T. (~ 50℃), (b) 100℃, (c) 200℃, and (d) 300℃; and all subjected to PMA 400℃ thermal treatment.

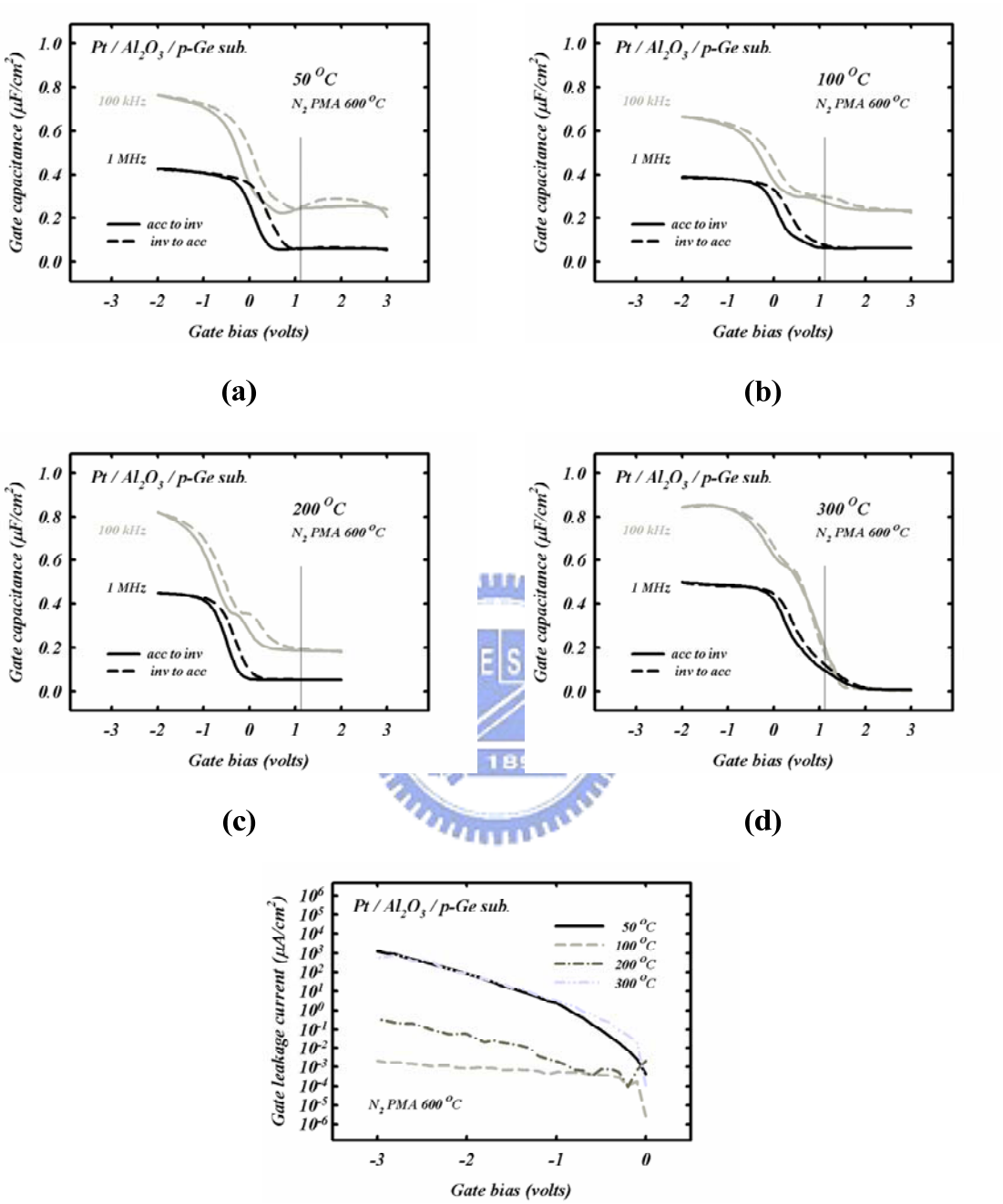


Fig. 3-5 The (a) ~ (d) C-V and (e) I-V electrical performance of the 80 cycs. ALD Al_2O_3 films deposited at (a) R.T. (~ 50℃), (b) 100℃, (c) 200℃, and (d) 300℃; and all subjected to PMA 600℃ thermal treatment.

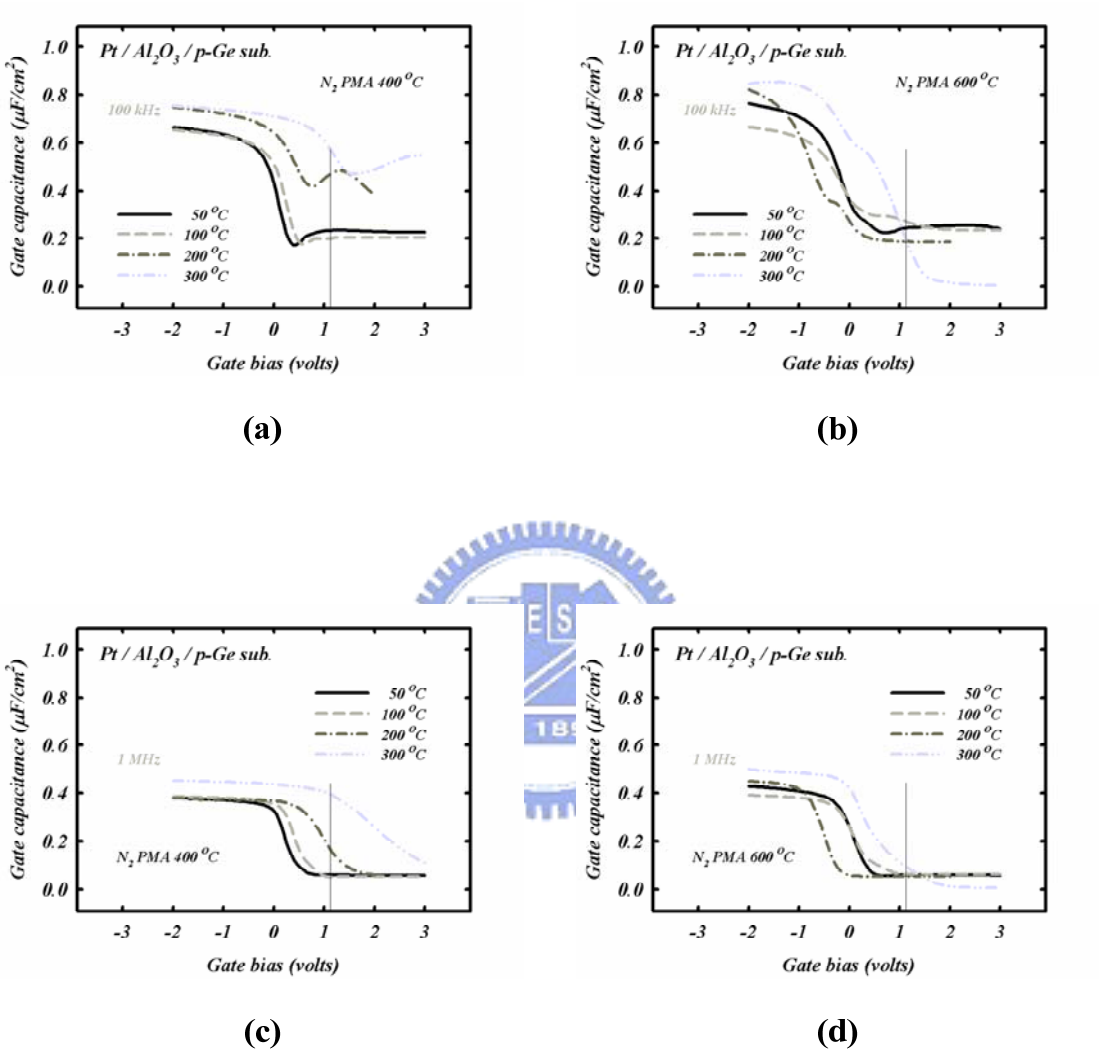
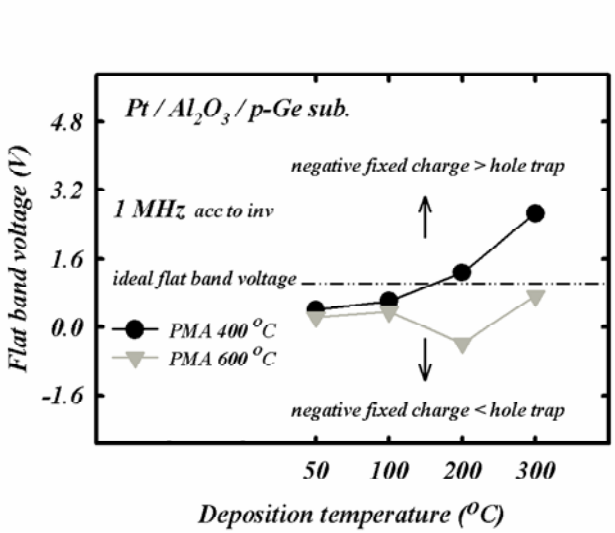
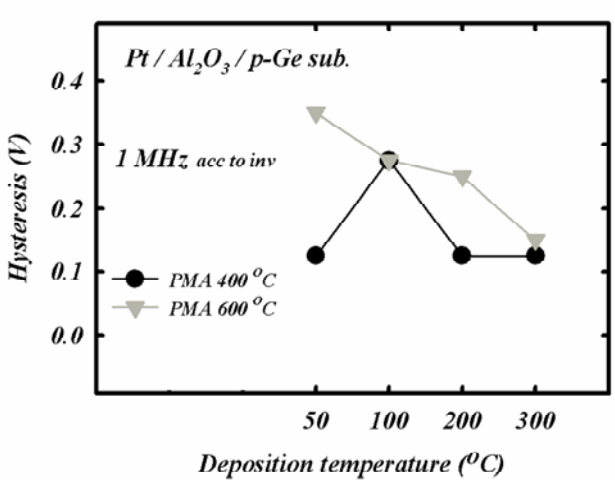


Fig. 3-6 Collection of the (a) (b) 100 kHz and (c) (d) 1 MHz C-V electrical performance of the 80 cycs. ALD Al_2O_3 films deposited at R.T. (~ 50℃), 100℃, 200℃, and 300℃; and subjected to (a) (c) PMA 400℃ and (b) (d) 600℃ thermal treatment.



(a)



(b)

Fig. 3-7 The (a) 1 MHz flat band voltage and (b) 1 MHz hysteresis of the corresponding C-V electrical performance of the 80 cycs. ALD Al_2O_3 films deposited R.T. (~ 50℃), 100℃, 200℃, and 300℃ with PMA 400℃ and 600℃ thermal treatments.

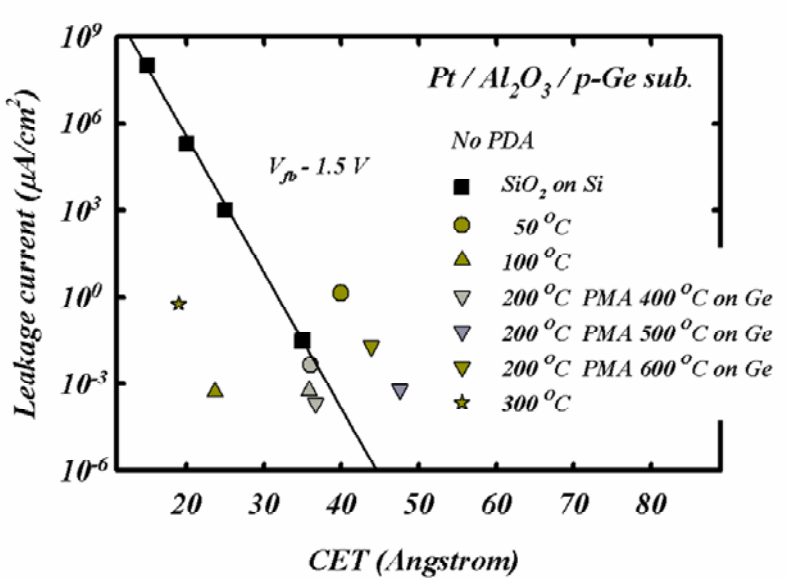


Fig. 3-8 Capacitance equivalent thickness (CET) v.s. gate leakage current density at $V_g = V_{fb}$ -1.5 V. One kind of simple and color represent one kind of deposition temperature and thermal treatment, respectively.

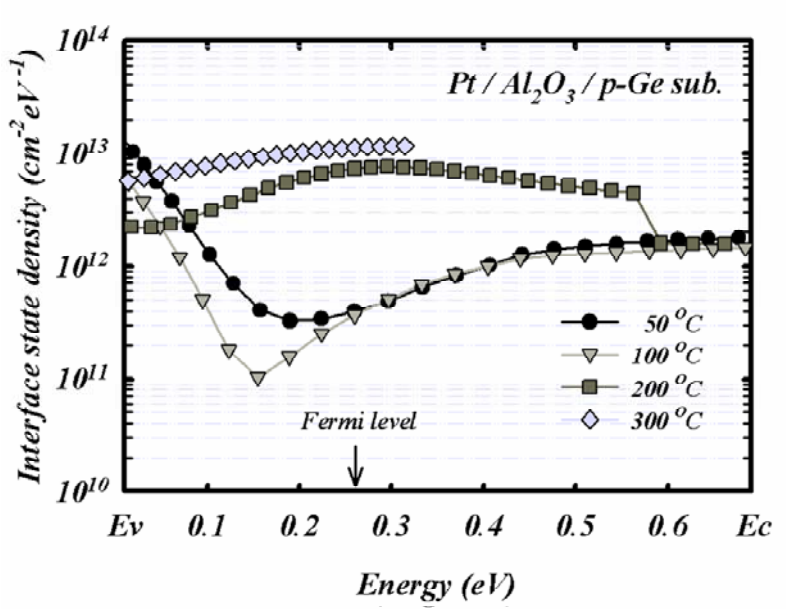


Fig. 3-9 Dit v.s. position in the Ge bandgap near the substrate surface. Interface state density (Dit) was calculated by the High-Low frequency method from the C-V characteristics showed in Fig. 3-6 (a) (c).

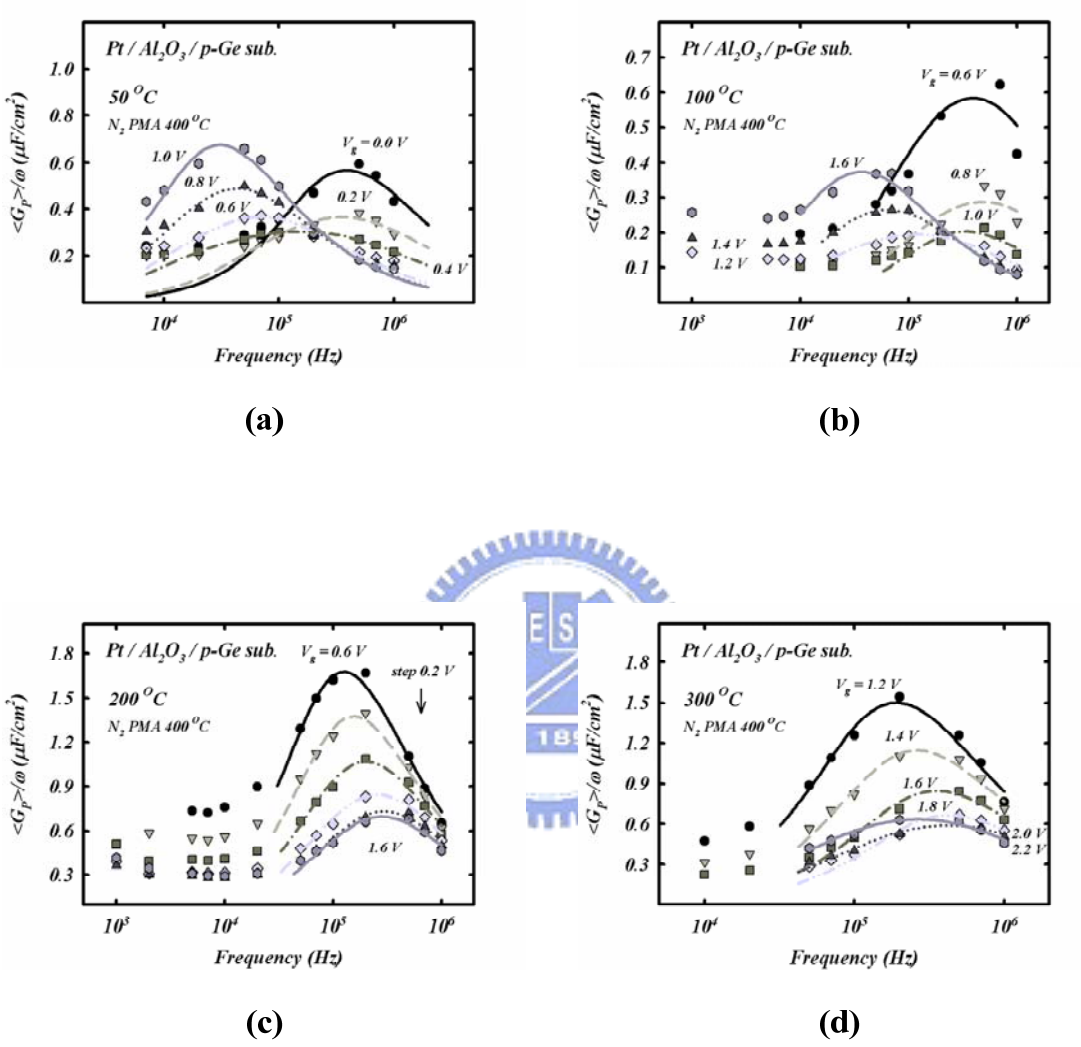


Fig. 3-10 Calculated $<G_P>/\omega$, by 1 kHz ~ 1 MHz C-V and G-V electrical performance, of the 60 cycs. ALD Al_2O_3 films deposited at (a) R.T. (~ 50℃), (b) 100℃, (c) 200℃, and (d) 300℃; and all subjected to PMA 400℃ thermal treatment. The symbols and solid lines represent the calculated and simulated data, respectively.

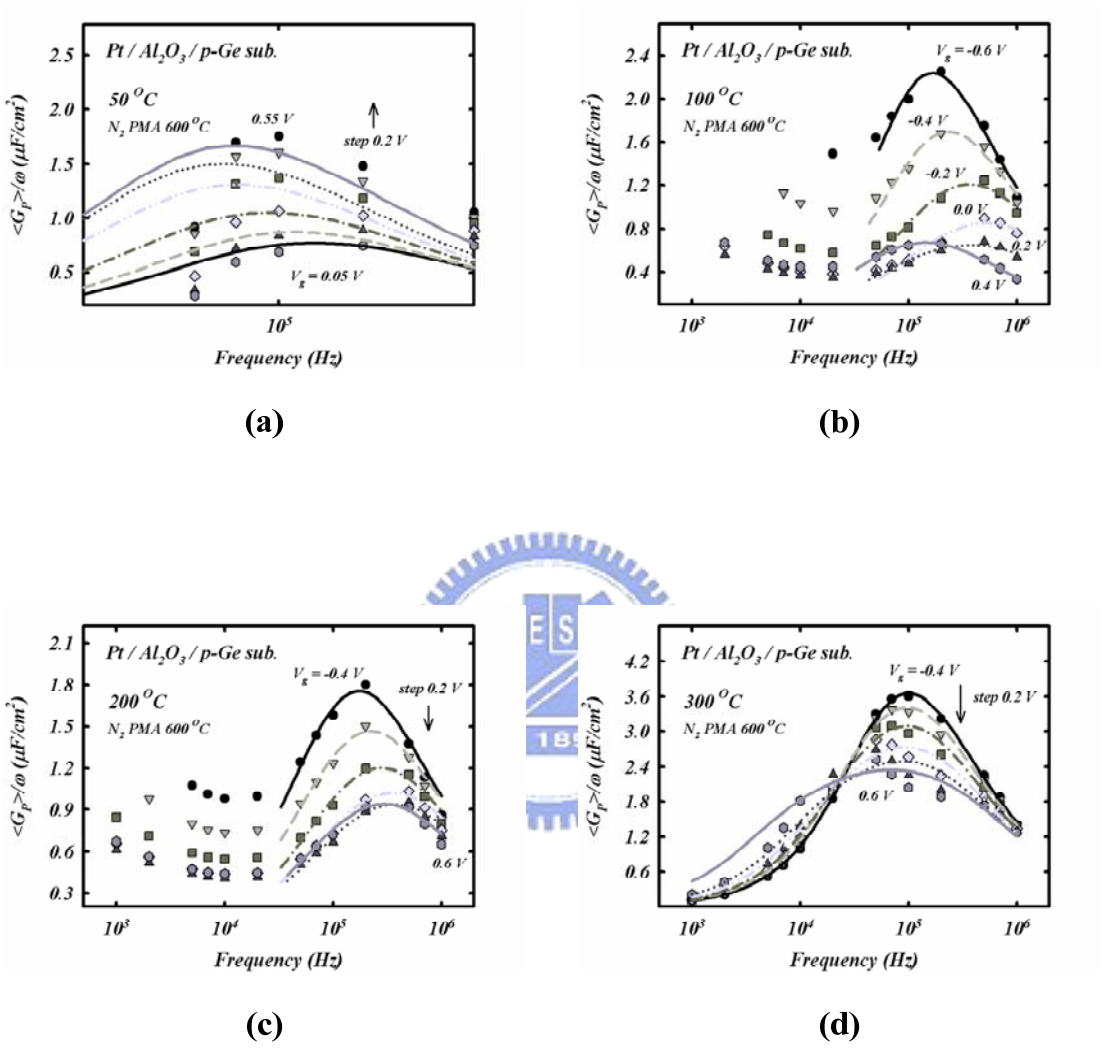
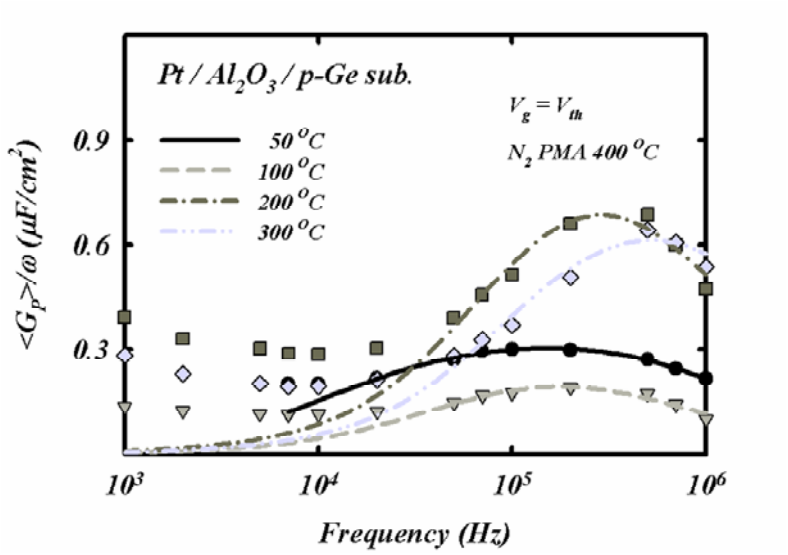
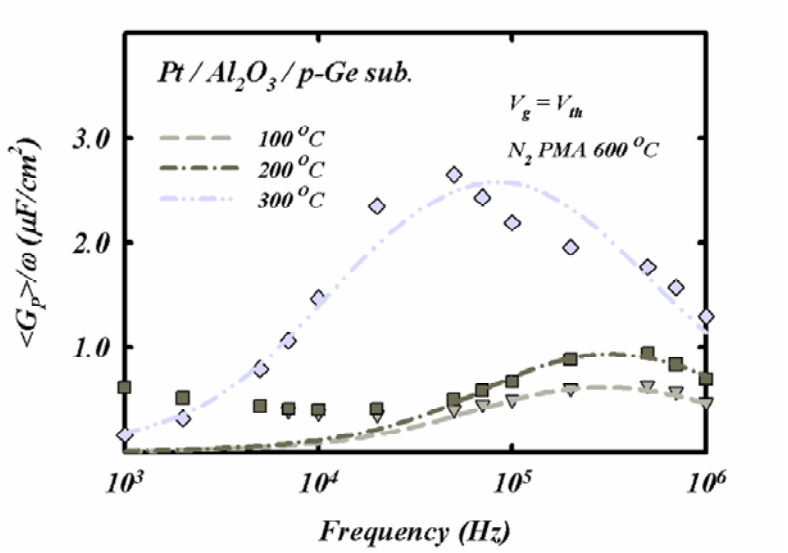


Fig. 3-11 Calculated $<G_P>/\omega$, by 1 kHz ~ 1 MHz C-V and G-V electrical performance, of the 60 cycs. ALD Al_2O_3 films deposited at (a) R.T. (~ 50℃), (b) 100℃, (c) 200℃, and (d) 300℃; and all subjected to PMA 600℃ thermal treatment. The symbols and solid lines represent the calculated and simulated data, respectively.

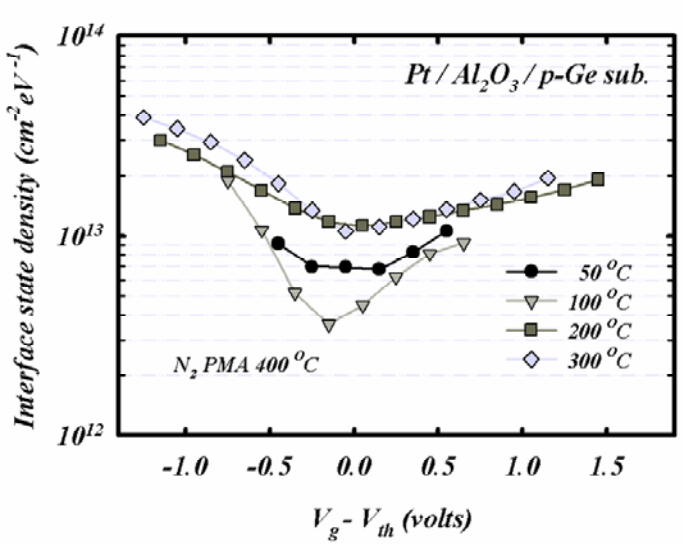


(a)

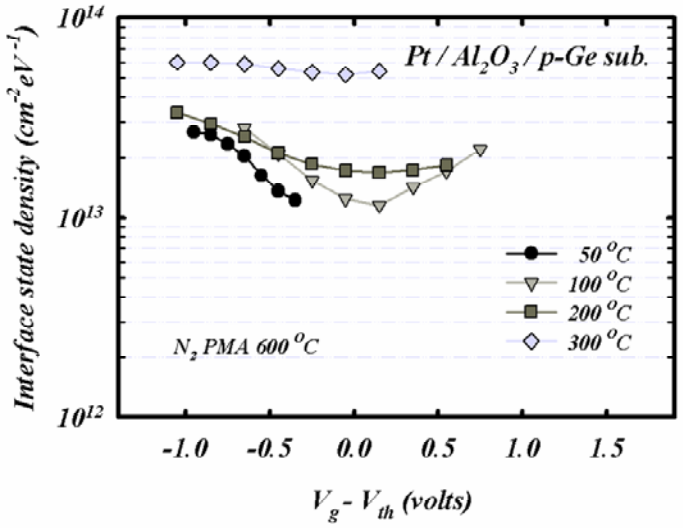


(b)

Fig. 3-12 Collection of the calculated $<G_P>/\omega$ curves (for $V_g = V_{th}$) showed in (a) Fig. 3-10 for PMA 400℃ and (b) Fig. 3-11 for PMA 600℃. The symbols and solid lines represent the calculated and simulated data, respectively.

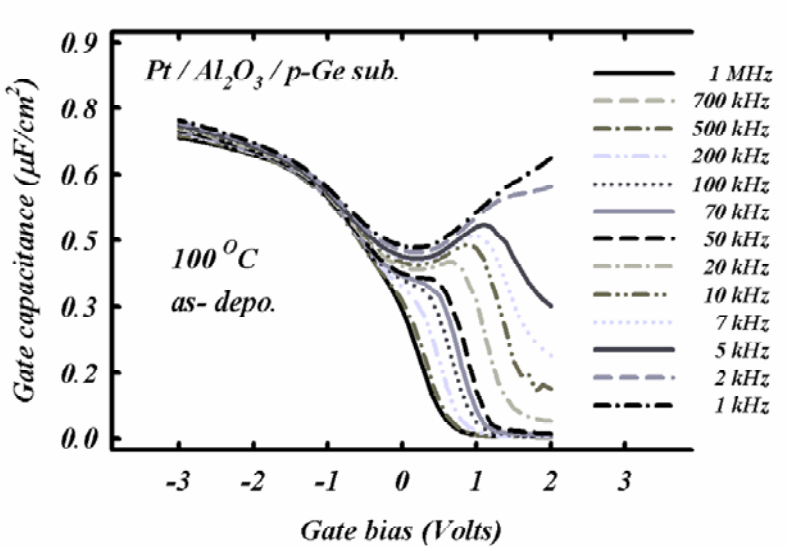


(a)

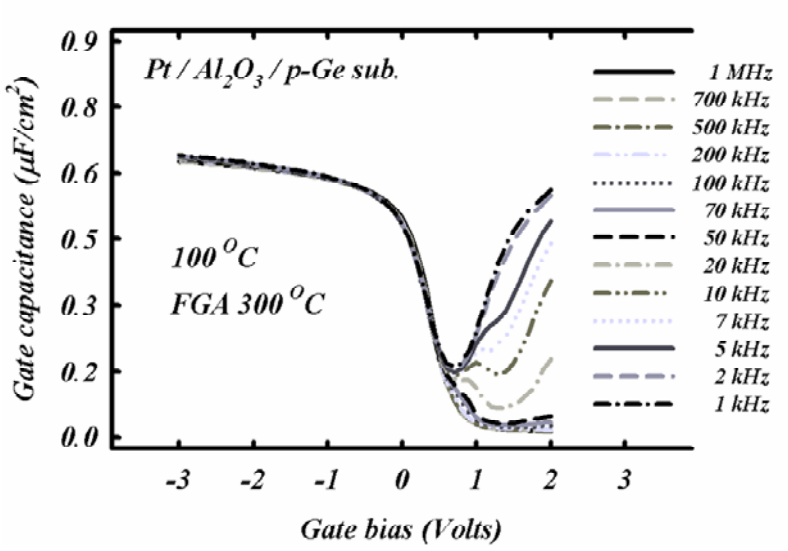


(b)

Fig. 3-13 Dit v.s. V_g - V_{th} for the 60 cycs. ALD Al_2O_3 films subjected to (a) PMA 400℃ and (b) PMA 600℃. Interface state density (Dit) was calculated by the G-V method from the calculated $<G_P>/\omega$ curves showed in (a) Fig. 3-10 and (b) Fig. 3-11.

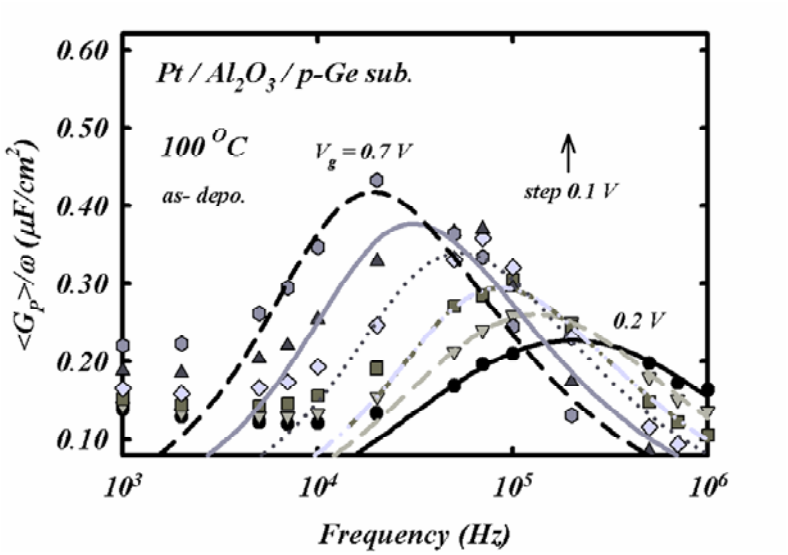


(a)

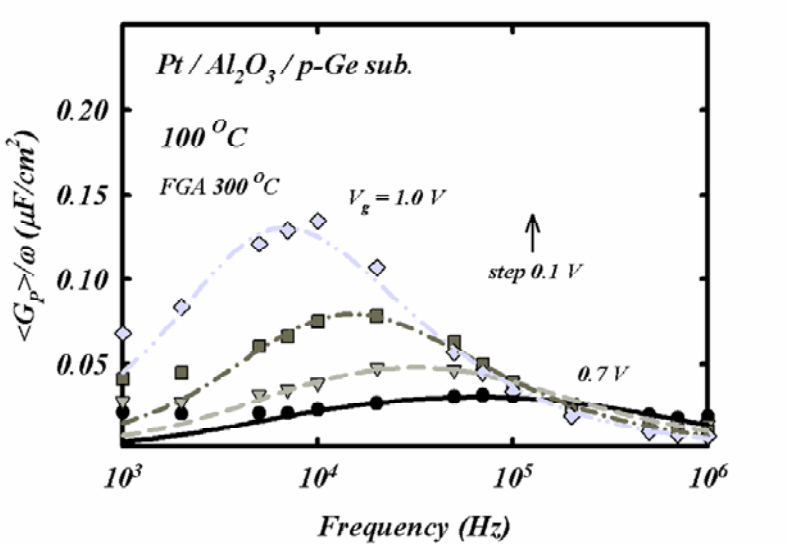


(b)

Fig. 3-14 The multi-frequency C-V electrical performance of the 60 cycs. ALD Al_2O_3 films deposited at 100℃ (a) without thermal treatment (as-depo.) and (b) with 300℃ Forming Gas Annealing (FGA).



(a)



(b)

Fig. 3-15 Calculated $<G_P>/\omega$, by 1 kHz ~ 1 MHz C-V and G-V electrical performance, of the 60 cycs. ALD Al_2O_3 films deposited at 100℃ (a) without thermal treatment and (b) with FGA 300℃. The symbols and solid lines represent the calculated and simulated data, respectively.

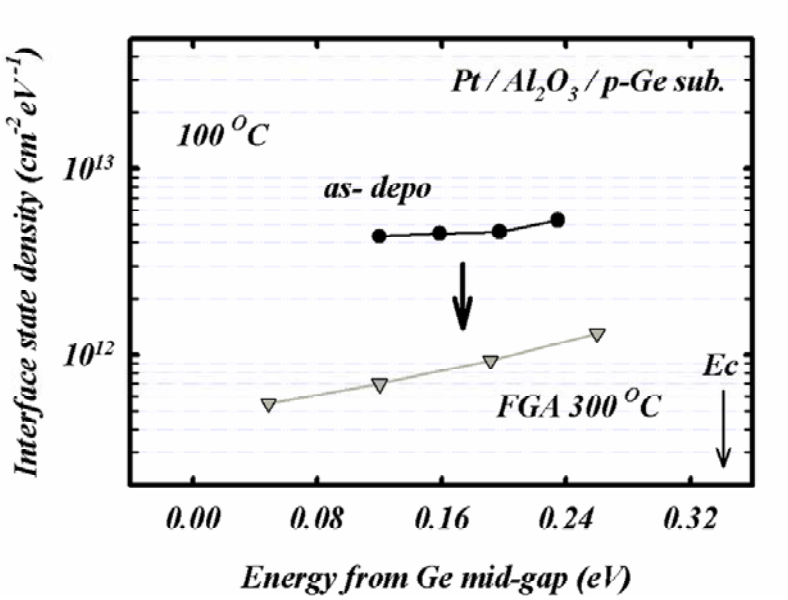


Fig. 3-16 Dit v.s. Energy from Ge mid-gap near the substrate surface for the 60 cycs. ALD Al_2O_3 films deposited at 100℃ (a) without thermal treatment and (b) with FGA 300℃. Interface state density (Dit) was calculated by the G-V method from the calculated $<G_P>/\omega$ curves showed in Fig. 3-15.

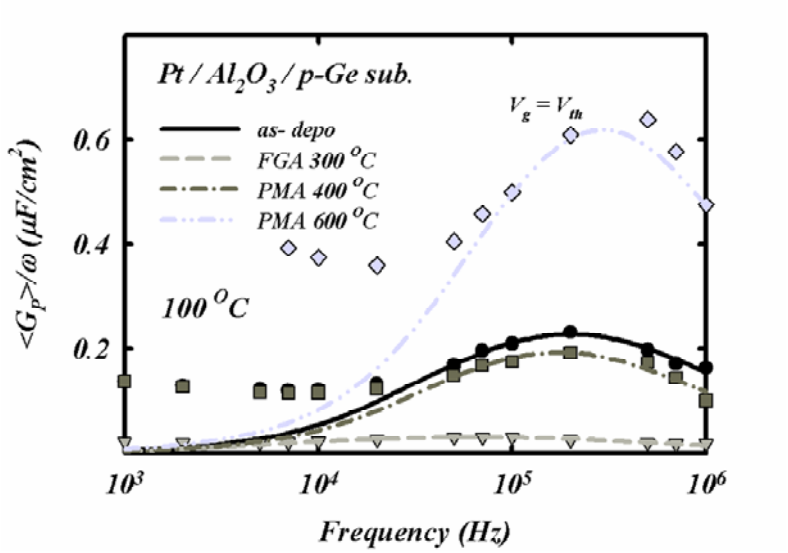


Fig. 3-17 Calculated $<G_P>/\omega$ (for $V_g = V_{th}$), by 1 kHz ~ 1 MHz C-V and G-V electrical performance, of the 60 cycs. ALD Al_2O_3 films deposited at 100℃ with various thermal treatment. The symbols and solid lines represent the calculated and simulated data, respectively.

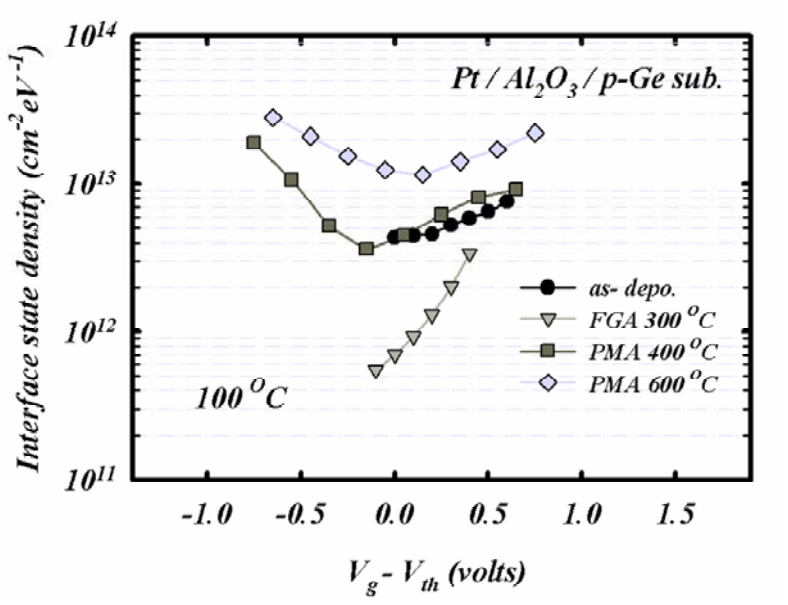


Fig. 3-18 Dit v.s. V_g - V_{th} for the 60 cycs. ALD Al_2O_3 films deposited at 100℃ without various thermal treatment. Interface state density (Dit) was calculated by the G-V method from the calculated $<G_P>/\omega$ curves showed in Fig. 3-10, 3-11, and 3-15.

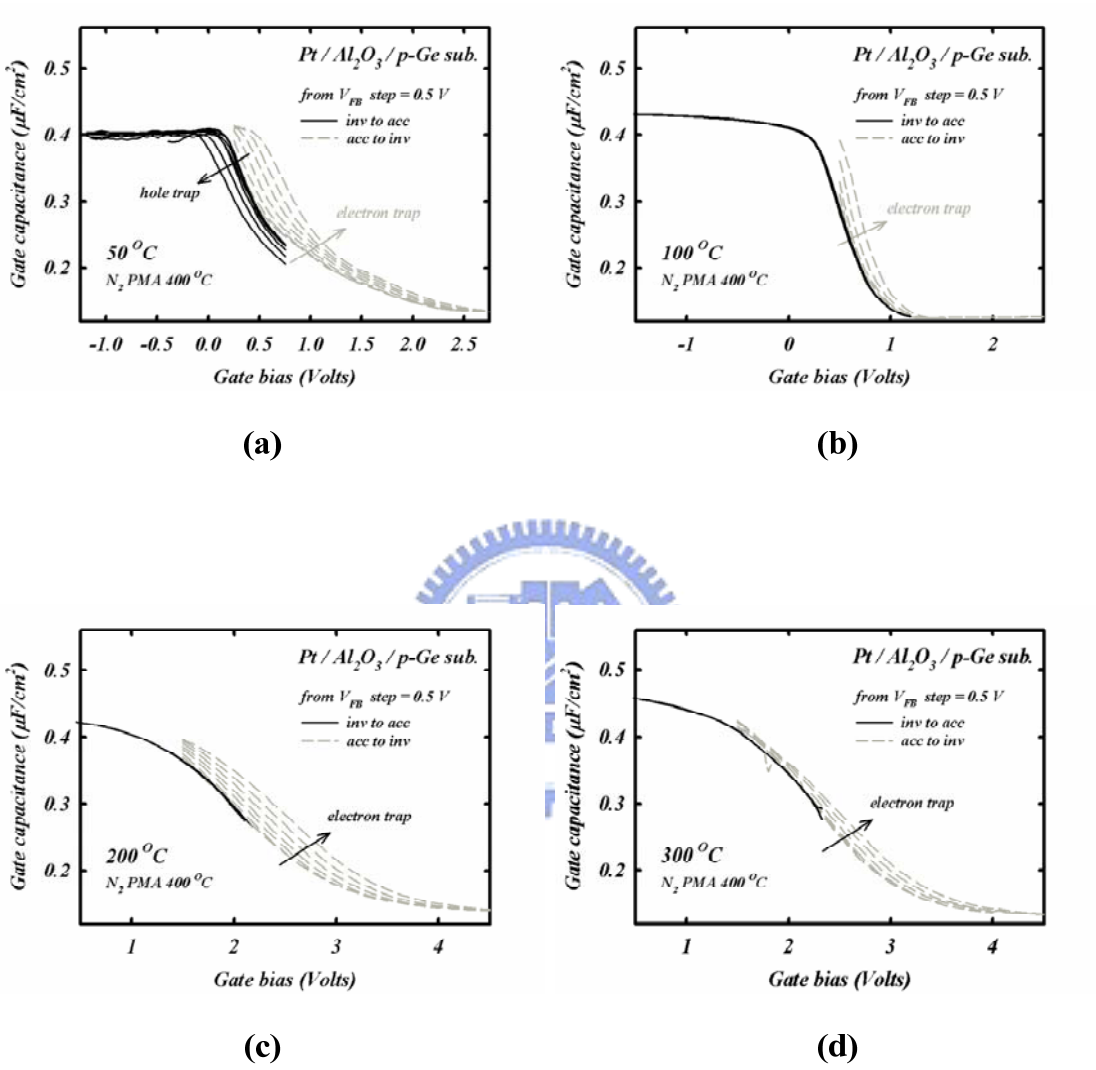


Fig. 3-19 Trap analyses of the 60 cycs. ALD Al_2O_3 films deposited at (a) R.T. (~ 50℃), (b) 100℃, (c) 200℃, and (d) 300℃; and all subjected to PMA 400℃ thermal treatment. The sweep voltage from the flat band voltage, V_{FB}, increases by 0.5 V (or -0.5 V) for every times until the absolute value of the sweep range bigger than 3.0 ~ 4.5 V.

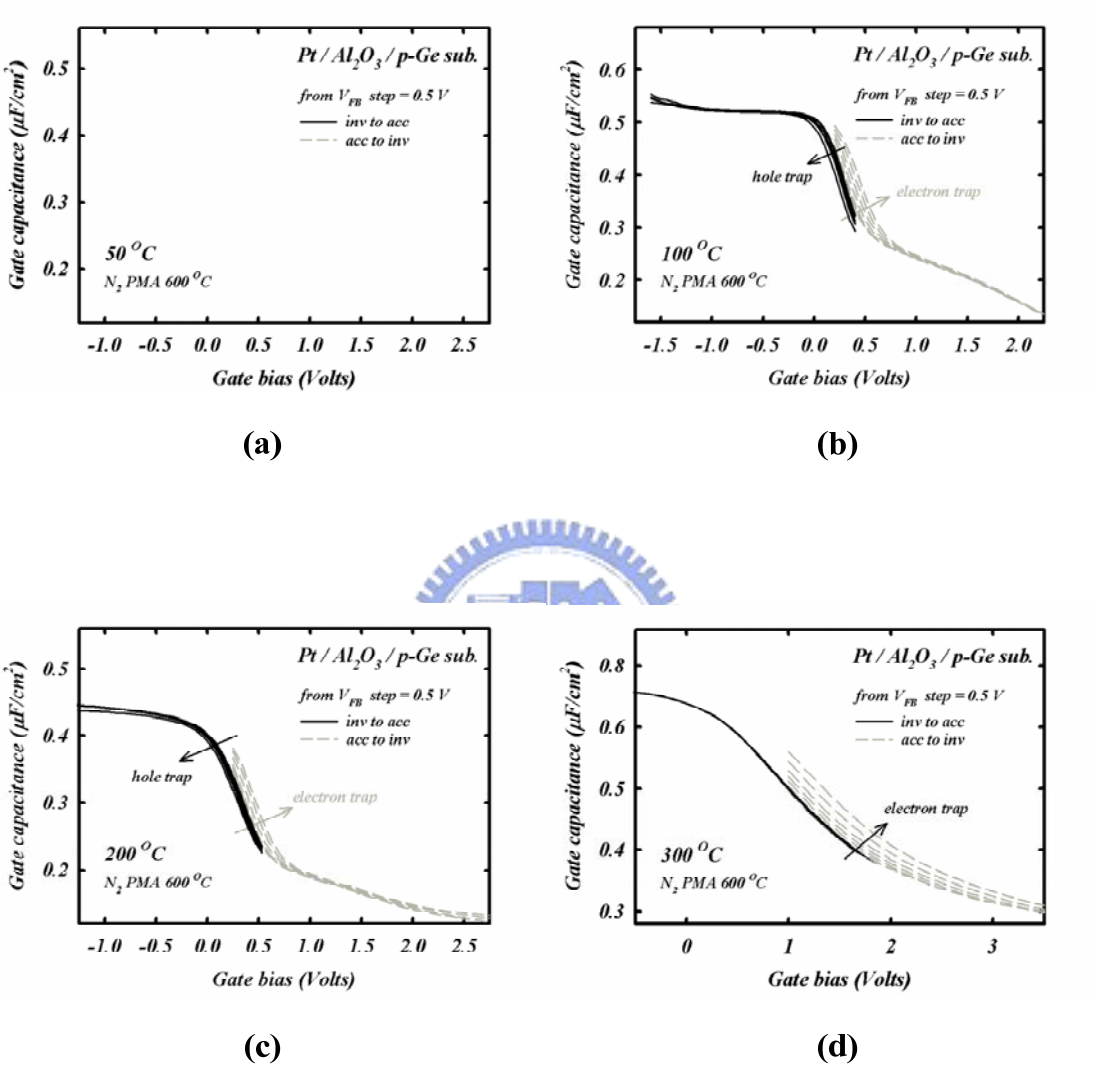


Fig. 3-20 Trap analyses of the 60 cycs. ALD Al_2O_3 films deposited at (a) R.T. (~ 50℃), (b) 100℃, (c) 200℃, and (d) 300℃; and all subjected to PMA 600℃ thermal treatment. The sweep voltage from the flat band voltage, V_{FB}, increases by 0.5 V (or -0.5 V) for every times until the absolute value of the sweep range bigger than 3.0 ~ 4.5 V.

Chapter 4

Electrical characteristics of Ge p-MOSFETs with atomic-layer-deposited Al_2O_3 gate dielectric and boron doped P-N junction

4-1 Introduction

In chapter 2 and 3, we had studied the physical and electrical characteristics of such a MOS gate stack – i.e., Pt / ALD Al_2O_3 / p-type Ge / Al – in detail and found a window of temperature about 140 ~ 170 °C to deposit a dielectric film by an ALD system. After further referring to publications of doping information on Ge [40-43, 46-50], we have enough knowledge to fabricate a Ge MOSFET by a standard 4 mask process. We chose three points of activation temperature and two kinds of implantation energy to realize a Ge-based switch function. For semiconductors with large values of intrinsic carrier (n_i, such as Ge), it is well known that the diffusion component will dominate at room temperature and the reverse current will follow the Shockley equation, first item of eq. 4.1 (if n_i is small, such as Si, the generation current may dominate, second part of eq. 4.1);

$$J_R = q\sqrt{\frac{D_P}{\tau_p}}\frac{n_i^2}{N_D} + \frac{qn_iW}{\tau_e} \qquad (4.1)$$

$$J_{R,Ge} \Big/ J_{R,Si} \sim 5\times 10^4$$

By this, you may expect to see high junction leakage current in our studies. In addition, Ge has a smaller bandgap compared with Si that would results in higher junction leakage through direct tunneling. Moreover, it shows high risk of stressing the substrate while activating the dopant due to terrible thermal stability of Ge material. In this chapter, we demonstrated the realization of Ge-based MOSFETs with high saturation drain current and discussed the parameters extracted from the essential electrical measurements – I_d - V_g and I_d - V_d, such as Sub-threshold Swing (S.S), Threshold Voltage (V_{th}), Source Drain Series Resistance (R_{SD}), dopant in-diffusion length (ΔL), Effective Mobility (μ_{eff}), and Field Effect Mobility (μ_{EF}). We will also displace the comparison between those extracted parameters and activation conditions or channel length and point out the mechanisms of those observed phenomenon as possible as we can.

4-2 Experimental Procedures

The Antimony (Sb, concentration ~ 2e14 /cm^2) doped Ge substrates were used to fabricate the Ge-based p-MOSFETs. After broking the flesh Ge wafer into fragments, we consulted the results of the research of C. C. Cheng et al. [7-8] to clean the Ge fragments in several cycles of sequential dilute HF (HF:H_2O ~ 1:30) and deionized (D.I.) water rinses followed by a last-HF dip and N_2 drying. Then, we used a Plasma Enhanced Chemical Vapor Depositon (PECVD) system to deposit the SiO_2 filed oxide for isolation of devices. To form a boron (B) doped P-N diode for restricting the flow of drain current just underneath the substrate surface, we defined the source drain region by Mask 1 and etched SiO_2 by the solution – Buffer Oxide Etching (BOE) – followed by an B^+ (with dopant dose ~ 1e15 /cm^2) Ion Implantation process (tilt 7° and twist 23°). Before removing the dummy gate by Mask 2, we activated the B doped P-N diode by a rapid thermal annealing (RTA) system in N_2 (pressure~ 1 atm) ambient according to the split conditions – Table. 4-1. As soon as the dummy gate removed, we used an atomic-layer-deposition system to grow the gate dielectrics at ~ 170 °C with 100 deposition cycles in Instrument Technology Research Center (ITRC). In this ALD system, tri-methyl-aluminum (TMA), $Al(CH_3)_3$, and H_2O were chosen as the metal source and oxidant that were pulsed alternatively into the reactor for 1 sec;

and per pulse separated by N_2 purge of 10 sec to remove redundant reactants during the process. During each cycle of reactions, the chamber was held out at a constant pressure about 10 torr. Finally, right after excavating the contact hole by Mask 3, we coated aluminum (Al) on the semi-manufactured wafers thermally with the help of a thermal coater and defined electrodes by the last mask – Mask 4. The overall fabrication processes of the Ge p-MOSFETs were illustrated summarily in Fig. 4-1 for simple and easy to follow. After the fabrication of the MOSCAPs, we measured the capacitance-voltage (C-V) and current-voltage (I-V) characteristics by HP4284 precision LCR meter and Keithley 4200 semiconductor characterization system, respectively.

4-3 Results and Discussion

4-3-1 The I_d – V_g , I_d – V_d , and I_{junc} – V_{junc} essential electrical performance of the Ge p-MOSFETs with various implantation and activation conditions.

Figures 4-2 ~ 4 illustrate the electrical characteristics of the devices with 10 μm gate length and 100 μm gate width. Fig. 4-7 (a) and (b) show the comparison between the 550 °C activated MOSFETs with different implantation energy. From those figures mentioned, we could find that the I_d – V_g performance of a device with higher implantation energy and lower activation temperature shows a more ideal V_{th} (ideal V_{th} is about ~ -0.2 V) and higher saturation current. For the I_d – V_d characteristics, we preferred the 60 keV implantation energy and 550 °C activation temperature to fabricate the MOSFET. It shows higher series resistance while suffering to 600 and 650 °C activations that might be due to high dopant lost into air during the activation process [40, 41]. With increase of activation temperature, both 30 and 60 keV implanted MOSFETs have degraded I_d – V_g and I_d – V_d curves. By inspecting the performance of the P-N diodes illustrated in Fig. 4-4 and 4-7 (c), we presumed that the suddenly increase of reverse junction current at high reverse bias resulted in the suddenly increase of drain current at high drain forward bias. Besides, it shows that 60 keV and 550 ℃ activation temperature is the best condition to form a P-N junction.

The decrease of forward current (increase of series resistance) and increase of reverse current imply getting worse of dopant lost and substrate stress while increasing the activation temperature.

4-3-2 The V_{th} , R_{SD} , ΔL , S.S. , μ_{eff} , and μ_{FE} extracted from the essential electrical performance of the Ge p-MOSFETs with various implantation and activation conditions.

From essential measurements of $I_d - V_g$ and $I_d - V_d$, we could extract and calculate those important parameters such as V_{th} , R_{SD} , ΔL , S.S. , μ_{eff} , and μ_{FE} to judge by the quality of the MOSFETs more professionally.

– V_{th} –

V_{th} was extracted by Linear Extrapolation (LE) method with the drain current measured as a function of gate voltage at a low drain voltage of typically 50-100 mV to ensure operation in the linear MOSFET region. According to eq. 4.2 which is valid only above threshold for non-zero and asymptotic decrease of I_d below threshold, we have zero drain current for $(V_g - V_{th} - \frac{V_d}{2}) = 0$. Hence the I_d v.s. V_g curves are extrapolated to I_d = 0, we can determine V_{th} from the extrapolated or intercept gate voltage $V_{g,ex}$ by eq. 4.3 with some error due to non-negligible series resistance.

$$I_d = \frac{W_{eff} \cdot \mu_{eff} \cdot C_{ox}}{L_{eff}} \cdot (V_g - V_{th} - \frac{V_d}{2}) \cdot (V_d - I_d \cdot R_{SD}) \qquad (4.2)$$

$$W_{eff} = W - \Delta W$$

$$L_{eff} = L - \Delta L$$

$$V_{th} = V_{g,ex} - \frac{V_d}{2} \qquad (4.3)$$

All the extrapolating results of devices with 10 μm gate length were summarized in Fig. 4-9 against the mask channel length. We dug out short channel effect (SCE) regarding which device was discussed and reverse short channel effect (RSCE) for the 650 °C activated devices. We considered that RSCE is due to parallel MOSFETs (Series Transistor Effect) resulted from B transient enhanced diffusion (TED) and compensation effect (CE) at the damaged region caused by implantation (where B aggregated) near substrate surface. RSCE got more appreciable for the 650 °C activated devices.

– S.S. –

We used the definition of S.S. as eq. 4.4 ($C_{D,\,max}$ is the equivalent semiconductor capacitance corresponding to maximum substrate depletion width – W_{max}) to extract this parameter which is related intimately to switch ability of a MOSFET.

$$S.S. = \left(\frac{d}{dV_g} logI_d \right)^{-1} = 2.3 \cdot \frac{kT}{q} \cdot (1 + \frac{C_{D,max}}{C_{ox}}) \qquad (4.4)$$

The ideal value of S.S. for our case is about 60 mV/decade calculated by the second term in eq. 4.4. Fig. 4-10 illustrates all the extracted values against the mask channel length for all the MOSFETs mentioned. It shows the usual and unusual occurrence of SCE and S.S.-related RSCE, respectively. We presumed that S.S.-related RSCE was due to increase of W_{max} resulted from Charge Sharing Effect (CSE). And the somewhat lower values of S.S. of the 600 °C activated MOSFETs might be also due to CSE for high diffusion ability of B.

– R_{SD} and ΔL –

Equation 4.2 can be rewritten as eq. 4.5;

$$R_m = \frac{V_d}{I_d} = R_{ch} + R_{SD} = \frac{L - \Delta L}{W_{eff} \cdot \mu_{eff} \cdot C_{ox} \cdot (V_g - V_{th})} + R_{SD} \qquad (4.5)$$

R_{ch} *: channel resistance*
R_{SD} *: source drain series resistance*

It is more valid for use of this equation to extract R_{SD} and ΔL when $V_g - V_{th} >> \frac{V_d}{2}$ is satisfied and $V_g - V_{th}$ is chosen so that eq. 4.2 is suitable to describe the $I_d - V_g$ behavior at linear region. We had summarized the calculated outcome and linear fitting curves in Fig. 4-8. Table. 4-2 summarized the extracted values of V_{th} , S.S. ,

R_{SD} , and ΔL of the devices with 10 μm gate length. The lost extraction of R_{SD} and ΔL for higher activation temperature might be resulted from ΔL-related R_{SD} and severe B out-diffusion into air. We had the minimum value of R_{SD} for 60 keV implanted and 550 °C activated devices and found that higher implantation energy and activation temperature would lead to longer dopant in-diffusion (larger ΔL). The increase of R_{SD} is another evidence of dopant lost while increasing the activation temperature.

– μ_{eff} and μ_{FE} –

Equation 4.6 and 4.7 are the definition of Effective Mobility (μ_{eff}) and Filed Effect Mobility (μ_{FE}), respectively.

$$\mu_{eff} = \frac{\frac{\partial I_d}{\partial V_d}}{C_{ox} \cdot \frac{W_{eff}}{L_{eff}} \cdot (V_g - V_{th})} = \frac{g_D}{C_{ox} \cdot \frac{W_{eff}}{L_{eff}} \cdot (V_g - V_{th})} \qquad (4.5)$$

$$\mu_{EF} = \frac{\frac{\partial I_d}{\partial V_g}}{C_{ox} \cdot \frac{W_{eff}}{L_{eff}} \cdot V_d} = \frac{g_m}{C_{ox} \cdot \frac{W_{eff}}{L_{eff}} \cdot V_d} \qquad (4.5)$$

The calculation results are illustrated in Fig. 4-11 and 4-12 for μ_{eff} and μ_{FE} , respectively. The black dash-dot-dot line represents the outcome of Si-based MOSFETs for easy comparison. The lower value of μ_{eff} compared with μ_{eff} might be

due to higher R_{SD} . Lower value of mobility compared with that of Si might be resulted from severe surface roughness and phonon scattering.

4-4 Summary

We had succeeded in demonstrating a Ge-based p-MOSFET by the standard 4 mask process. Almost all the electrical performances and indicative parameters that should be present and calculated were illustrated for those Ge p-MOSFETs with different dopant activation conditions in this chapter. High carrier diffusion coefficient, high intrinsic carrier conc, and narrower energy bandgap lead to high junction leakage in our studies. Junction leakage may be the most severe issue in realizing a high mobility, excellent switch ability, and low power consumption Ge-based transistor. By analyzing the $I_d - V_g$ and $I_d - V_d$ electrical characteristics and extracting those parameters such as V_{th} , R_{SD} , ΔL , S.S. , μ_{eff} , and μ_{FE} , we have the ideal about what would happen and should be paid heed to when deal with such a nasty substrate material. 60 keV and 550 °C is the best condition to form a P-N junction. Dopant lost during activation process is another issue in Ge p-MOSFET fabrication. It should be better to continue improving the Ge-based P-N diode for realization of an acceptable transistor in the future.

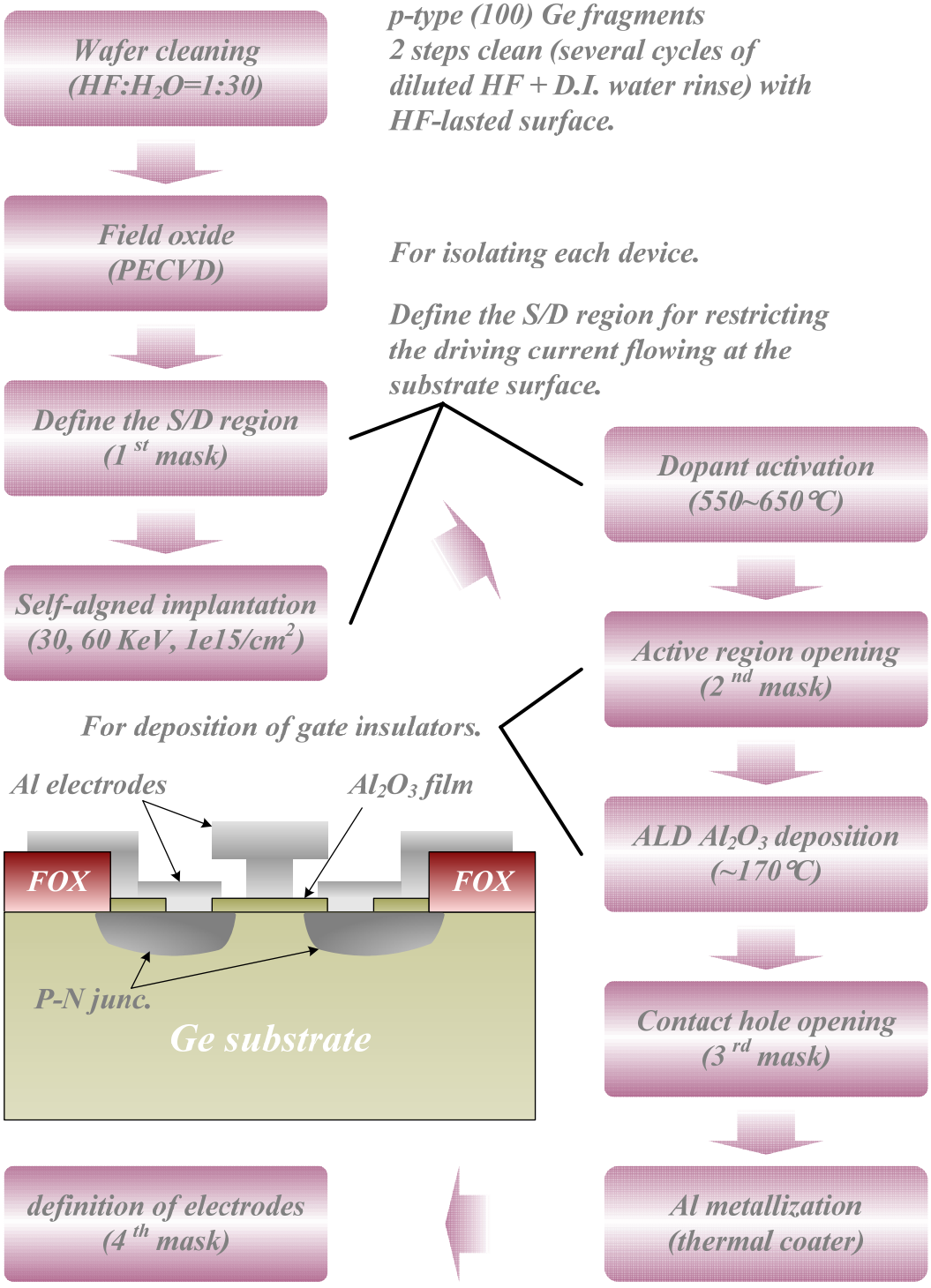
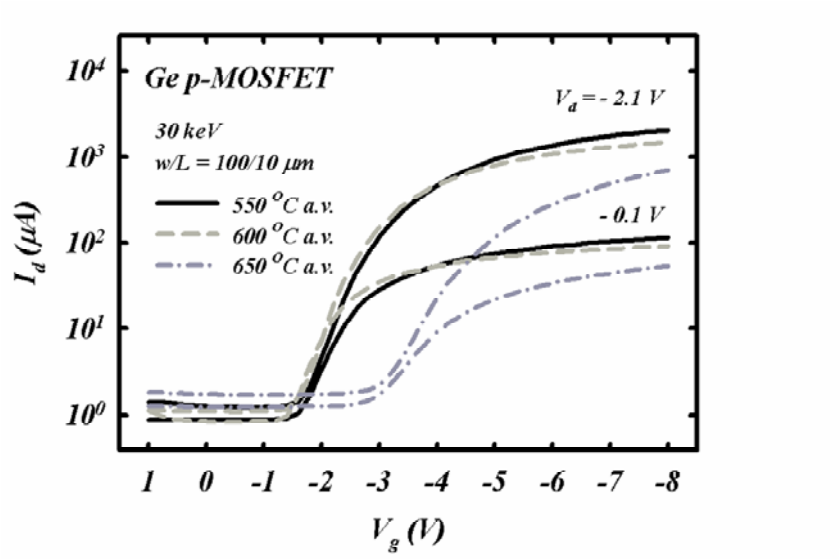


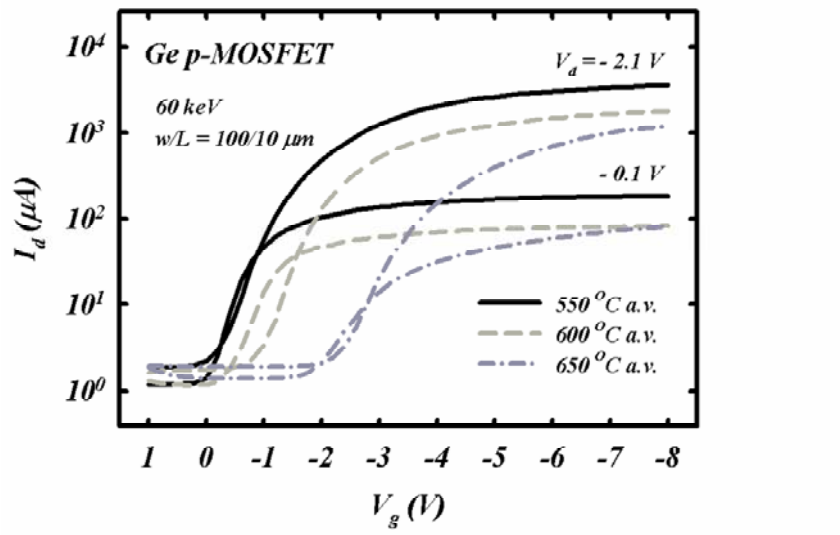
Fig. 4-1 MOSFET (with P-N junction) fabrication flow chart.

Table 4-1. The conditions of dopant (boron) activation of the P-N diodes.

	A55	A60	A65	B55	B60	B65
dopant kind	B^+	B^+	B^+	B^+	B^+	B^+
dopant dose ($1/cm^2$)	1e15	1e15	1e15	1e15	1e15	1e15
implant. energy (keV)	30	30	30	60	60	60
act. tempe. (℃)	550	600	650	550	600	650
act. time (sec)	30	10	10	30	10	10



(a)



(b)

Fig. 4-2 The $I_d - V_g$ electrical performance of the Ge p-MOSFETs with dopant implantation energy (a) 30 keV and (b) 60 keV. Gate length (L) = 10 μm and gate width (w) = 100 μm.

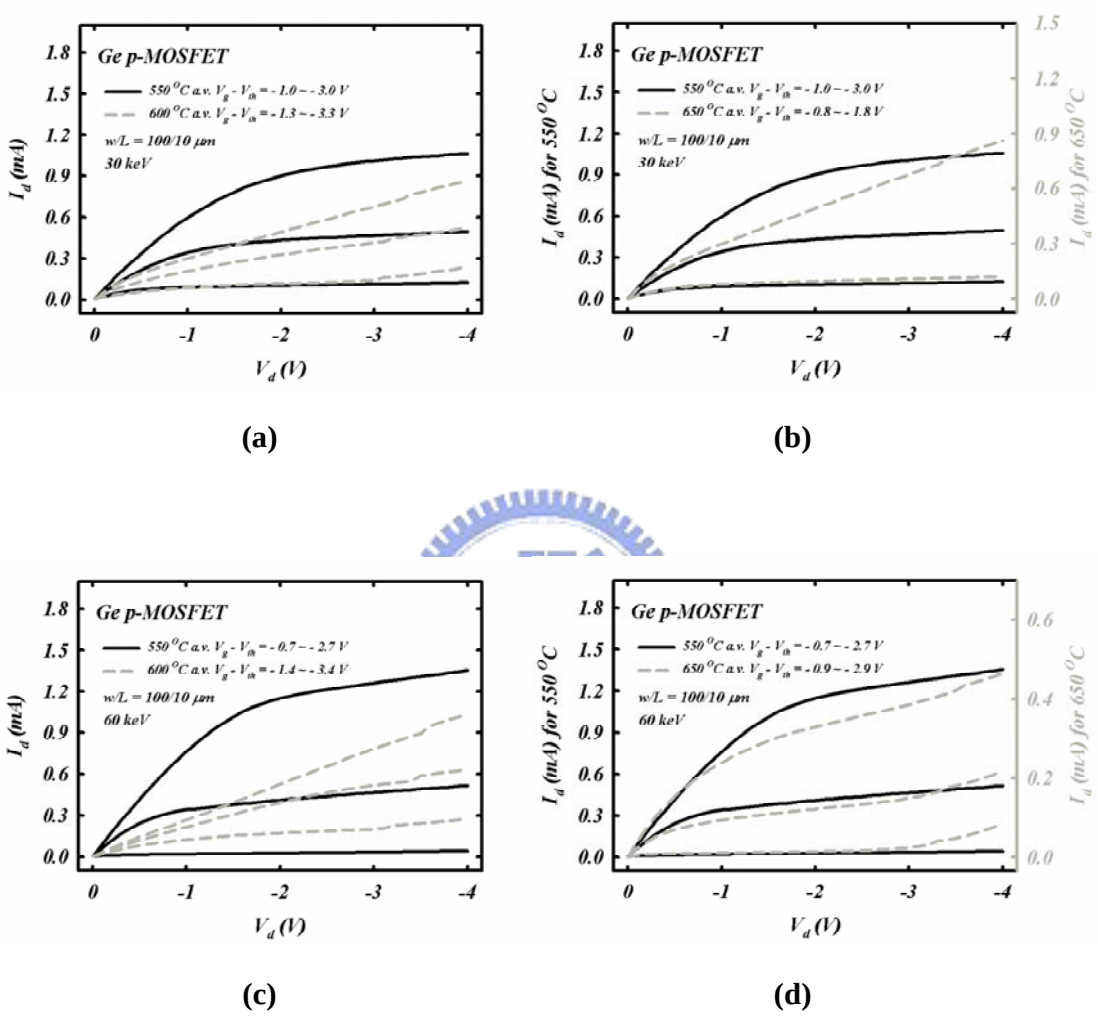
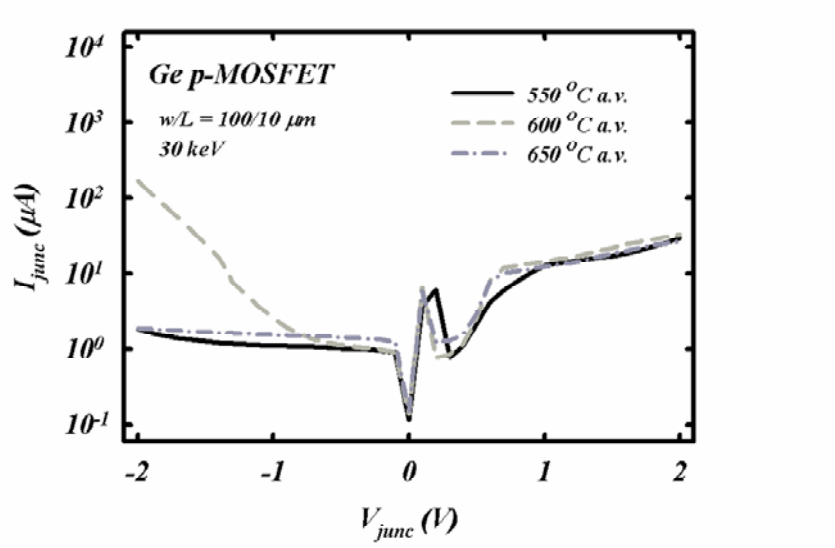
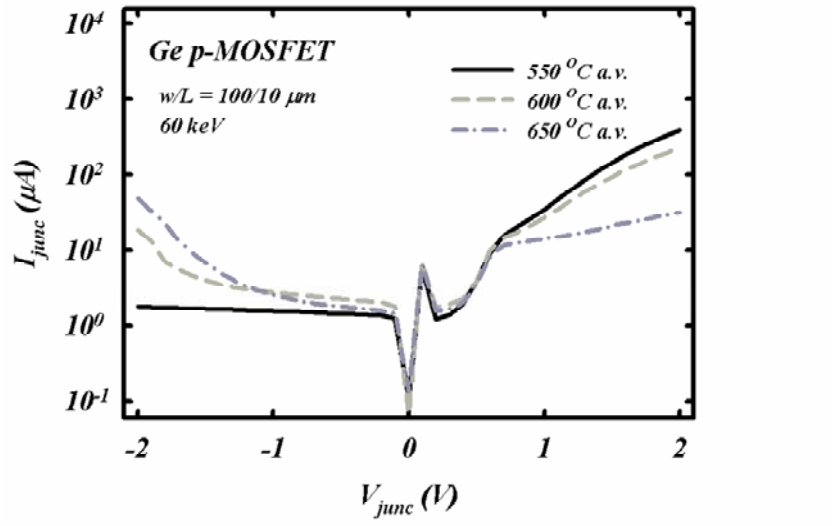


Fig. 4-3 The $I_d - V_d$ electrical performance of the Ge p-MOSFETs with dopant implantation energy (a) (b) 30 keV and (c) (d) 60 keV. Gate length (L) = 10 μm and gate width (w) = 100 μm.

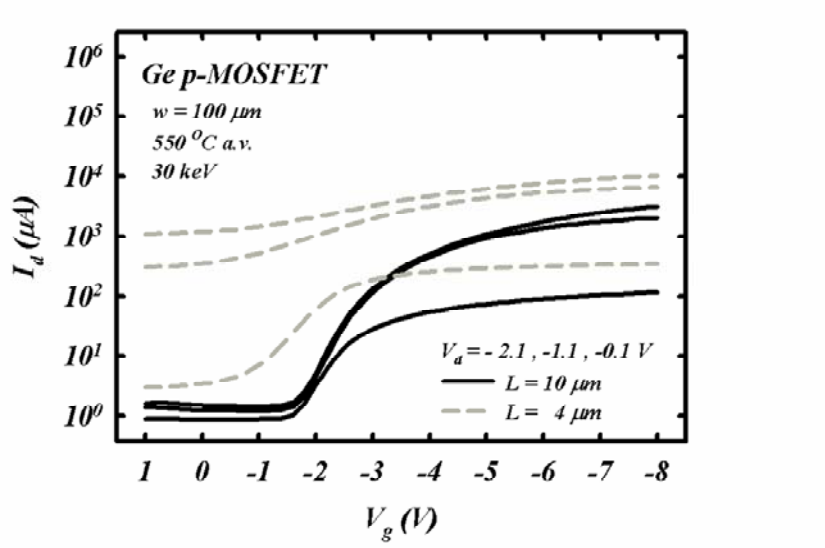


(a)

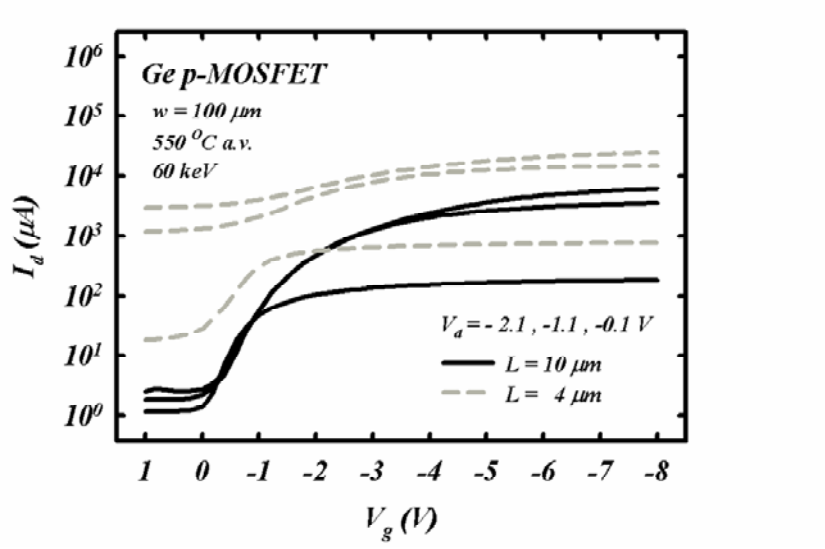


(b)

Fig. 4-4 The P-N diode $I_{junc} - V_{junc}$ electrical performance of the Ge p-MOSFETs with dopant implantation energy (a) 30 keV and (b) 60 keV. Gate length (L) = 10 μm and gate width (w) = 100 μm.

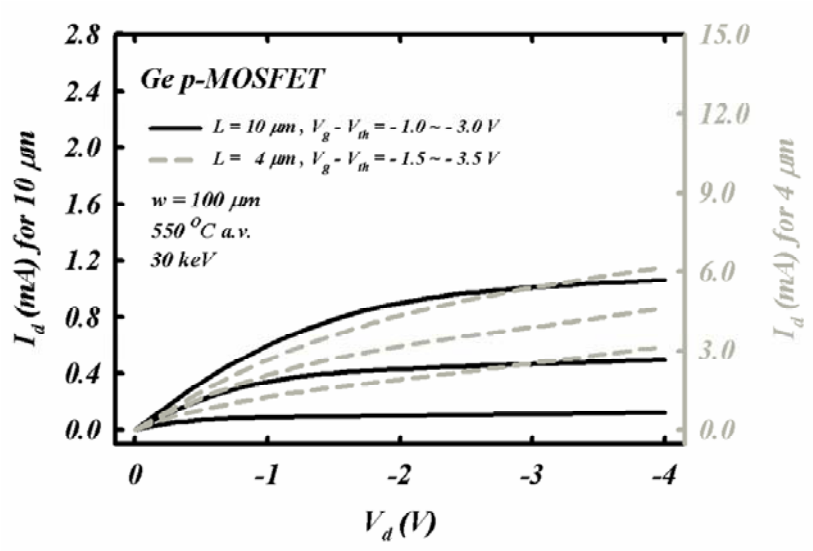


(a)

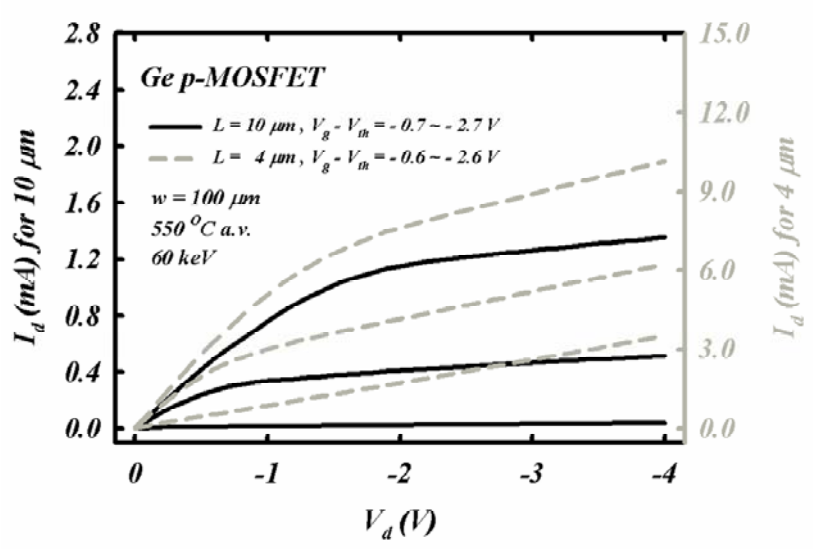


(b)

Fig. 4-5 The channel length dependent $I_d - V_g$ electrical performance of the 550℃ activated Ge p-MOSFETs with dopant implantation energy (a) 30 keV and (b) 60 keV . Gate width (w) = 100 μm.

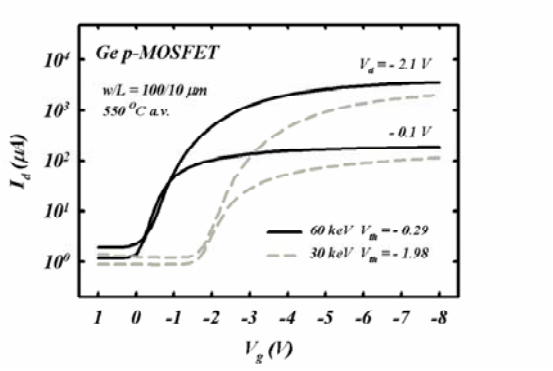


(a)

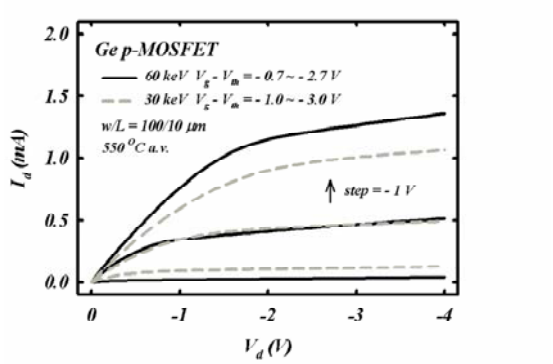


(b)

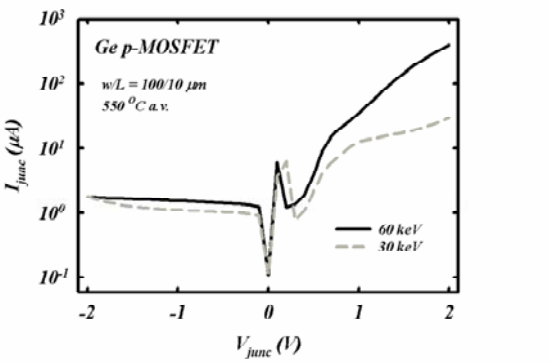
Fig. 4-6 The channel length dependent $I_d - V_d$ electrical performance of the 550℃ activated Ge p-MOSFETs with dopant implantation energy (a) 30 keV and (b) 60 keV. Gate width (w) = 100 μm.



(a)



(b)



(c)

Fig. 4-7 The (a) $I_d - V_g$, (b) $I_d - V_d$, and (c) $I_{junc} - V_{junc}$ electrical performance of the 550℃ activated Ge p-MOSFETs with dopant implantation energy 30 keV in comparison with that with 60 keV. Gate length (L) = 10 μm and gate width (w) = 100 μm.

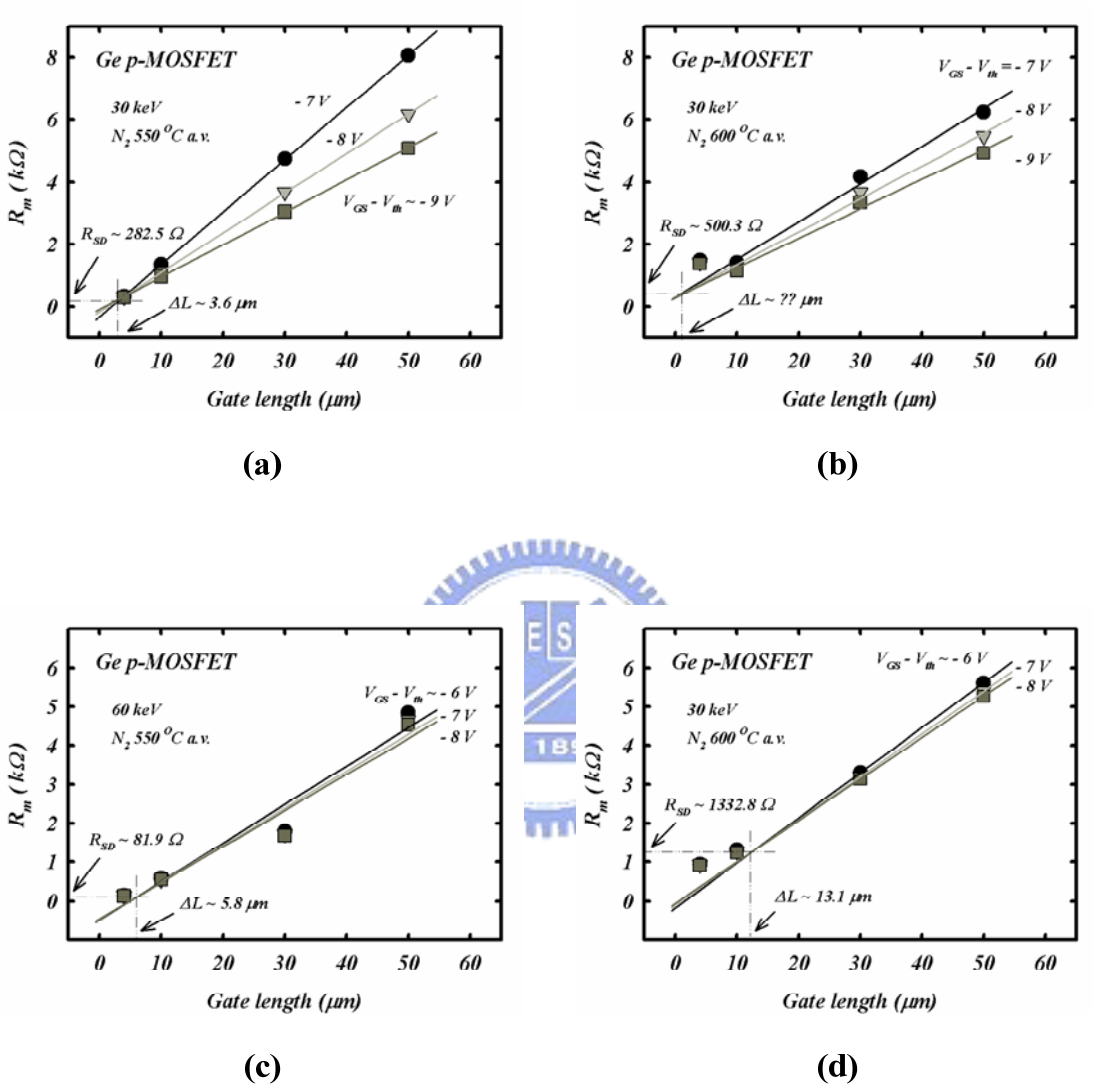
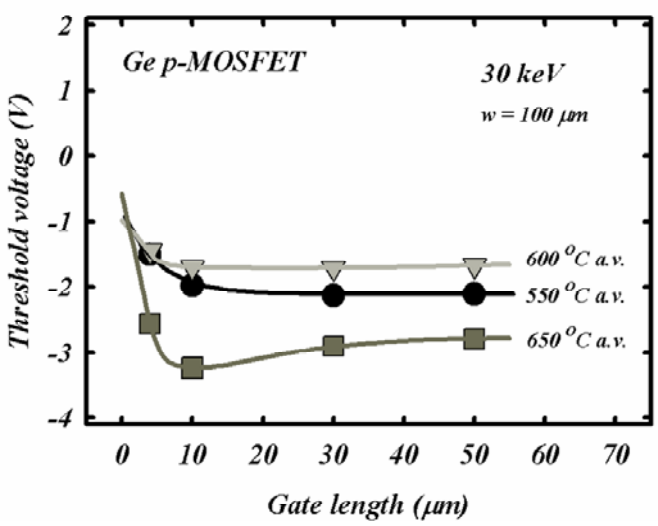


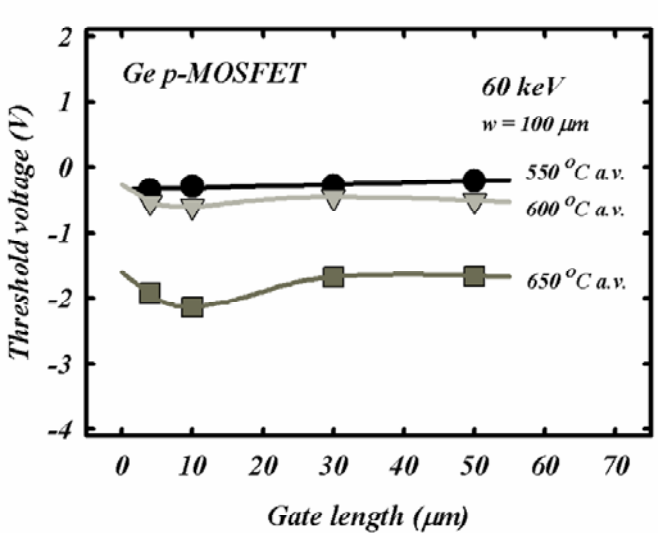
Fig. 4-8 The $R_m - L_g$ curves for extraction of R_{SD} and ΔL. (a) (b) and (c) (d) show the results of the Ge p-MOSFETs with dopant implantation energy 30 keV and 60 keV, respectively. (a) (c) and (b) (d) show the curves of activation temperature of 550 and 600℃, respectively.

Table 4-2. The extraction values from the I_d - V_g electrical performance of the Ge p-MOSFETs that have L = 10 μm and w = 100 μm.

	A55	A60	A65	B55	B60	B65
V_{th} (V)	- 1.98	- 1.70	- 3.24	- 0.29	- 0.60	- 2.14
S. S. (mV/decade)	580	497	836	471	446	678
R_{SD} (Ω)	282.5	500.3	- - -	81.9	1332.8	- - -
ΔL (μm)	3.6	- - -	- - -	5.8	13.1	- - -

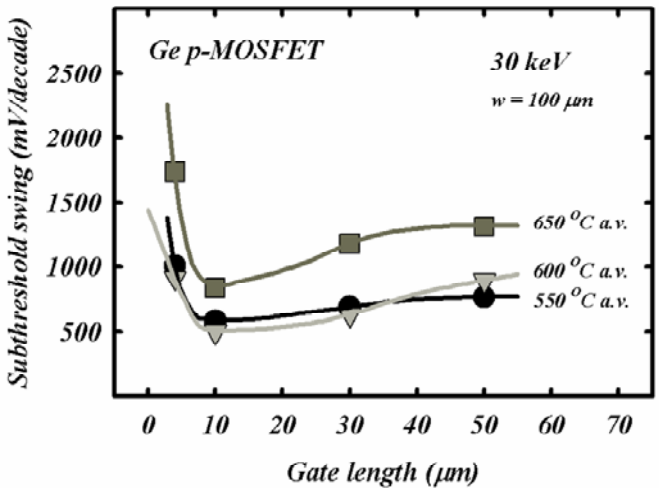


(a)

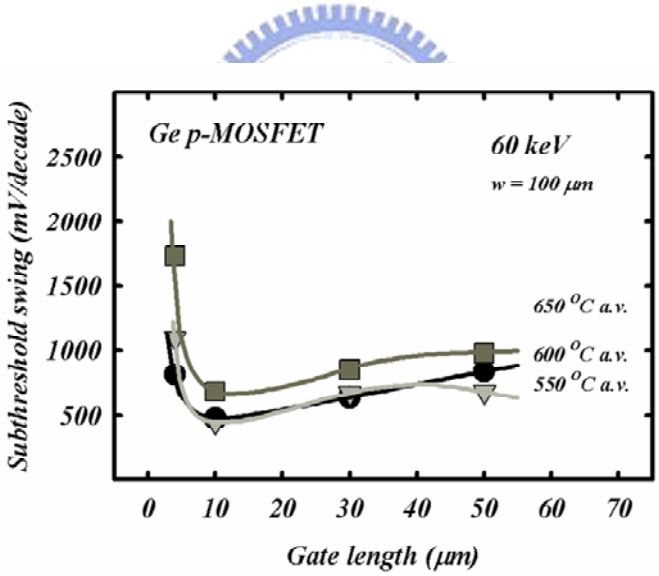


(b)

Fig. 4-9 The channel length dependent V_{th} of the 550℃, 600℃, and 650℃ activated Ge p-MOSFETs with dopant implantation energy (a) 30 keV and (b) 60 keV. Gate width (w) = 100 μm.

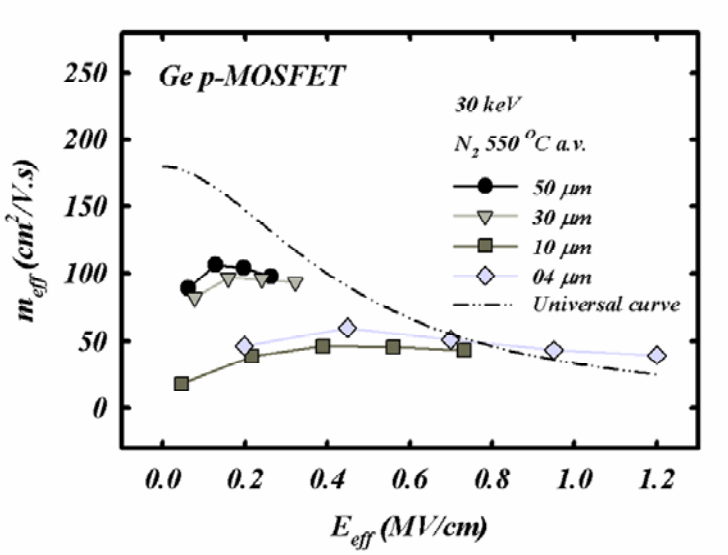


(a)

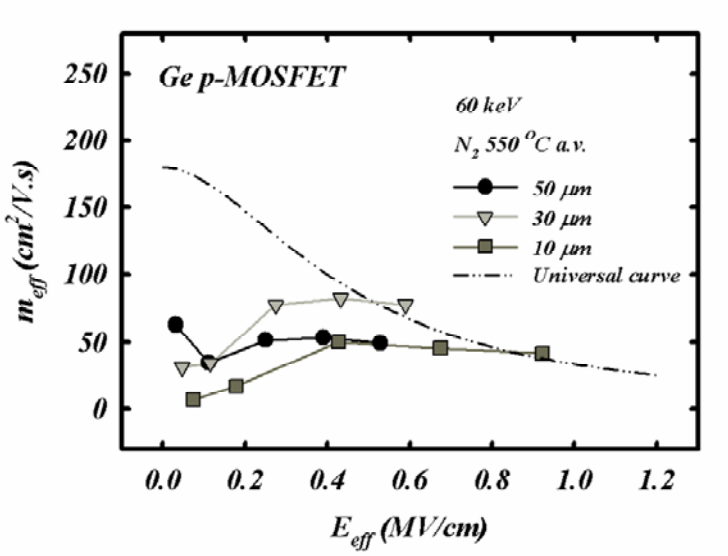


(b)

Fig. 4-10 The channel length dependent S.S. of the 550℃, 600℃, and 650℃ activated Ge p-MOSFETs with dopant implantation energy (a) 30 keV and (b) 60 keV. Gate width (w) = 100 μm.

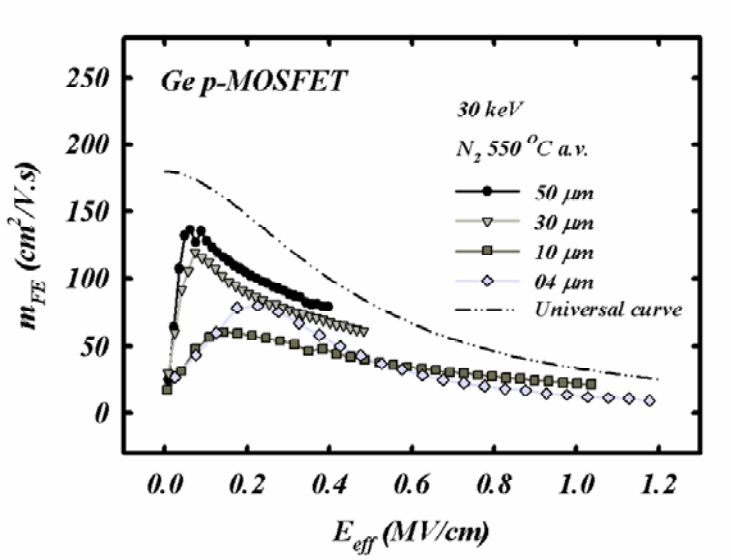


(a)

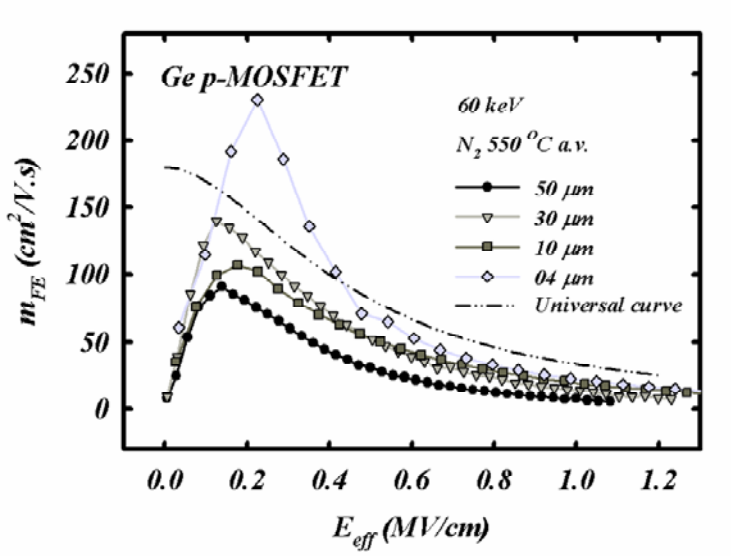


(b)

Fig. 4-11 The Effective mobility of the 550℃ activated Ge p-MOSFETs with dopant implantation energy (a) 30 keV and (b) 60 keV. Gate width (w) = 100 μm. The dash line shows the universal curve of Si p-MOSFET.



(a)



(b)

Fig. 4-12 The Field effect mobility of the 550℃ activated Ge p-MOSFETs with dopant implantation energy (a) 30 keV and (b) 60 keV. Gate width (w) = 100 μm. The dash line shows the universal curve of Si p-MOSFET.

Chapter 5

Conclusions and Suggestions for Future Work

5-1 Conclusions

– p-type Ge MOSCAPs –

We had succeeded in simulating the growth rate and explaining our experiment outcome by writing down an equation consists of surface coverage of reactants and probability of formation of surface complexes. This research showed a window of temperature (about 140 ~ 170 °C) to deposit an Al_2O_3 gate dielectric on Ge substrate by an Atomic Layer Deposition (ALD) system through the studies on the gate stack – Pt / ALD Al_2O_3 / p-type Ge / Al. In chapter 2, we discussed the physical properties of those gate stacks. By use of those physical analyses – such as AR-XPS, GI-XRR, AFM, SIMS, and HETEM – and the table of thermodynamics-related formation heat of the possible compounds formed during the ALD deposition process, we almost figured out the whole story about Ge out-diffusion, variance of interface roughness, and the trend of dielectric density comprehensively. We had a more stoichiometric but high Ge-incorporated film at high deposition temperature. In chapter 3, we studied the electrical properties and showed the consistency results of calculation of interface

state density (Dit) by two method – High-Low frequency (HLF) and Conductance (G-V) methods. The films deposited at 100 °C have the minimum Dit that could be further improved by forming gas annealing (FGA) at 300 °C. By combining with the results of chapter 2 and the studies of the trap behavior of the ALD films , we ascertained the reasonable mechanism about the shift of flat band voltage (V_{fb}) and the formation of fixed oxide charge (FOC.

– Ge p-MOSCAPs –

After studying the physical and electrical properties of the MOSCAPs with ALD dielectric films, we fabricated the Ge pMOSFETs by the traditional 4 mask process and studied their electrical performance through the essential electrical measurements – I_d v.s. V_g and I_d v.s. V_d – and the extrapolation of those indicative parameters – such as V_{th} , R_{SD} , ΔL , S.S. , μ_{eff} , and μ_{FE} – from the measurements. We found that $I_d - V_g$ and $I_d - V_d$, and $I_{junc} - V_{junc}$ got more and more degraded while increasing the activation temperature and choosing a lower implantation energy. Those extracted parameters – V_{th} and S.S. against the mask channel length – revealed short channel effect (SCE) and reverse short channel effect (RSCE). The P-N diodes with 60 keV implantation energy and 550 °C activation temperature gained the best rectification performance and lowest source drain series resistance (R_{SD}) but

somewhat longer dopant in-diffusion length (ΔL) compared with that of 30 keV. We also showed the calculated effective mobility (μ_{eff}) and field effect mobility (μ_{EF}) in comparison to that of Si-based transistors. I showed somewhat non-anticipated results that might be due to high junction leakage, larger R_{SD} , and dense Dit at the surface between a insulator and a substrate.

5-2 Suggestions for Future Work

– p-type Ge MOSCAPs –

1- Surface passivation is needed to eliminate Ge out-diffusion and improve the interface state density.

2- We require a system to deposit a high quality GeON before depositing the gate dielectric. It had been studied recently as a good buffer layer on Ge.

3- Alternative clean technique to make the surface completely hydroxyllated for a more complete ALD reaction should be study out in the future.

4- We still claim a better thermal treatment to improve the Ge-based gate stacks by a more powerful system such as laser pulse annealing (LPA).

– Ge p-MOSFETs –

1- We could replace the Ge-based P-N diode by the Si-based one for lower junction leakage and the use of silicidation process to minimize contact resistance and source drain series resistance.

2- Alternative Ge-related substrate such as Si-capped / epi-Ge / Si (SGS) substrate may be a good candidate for low coast transistor with high carrier mobility.

3- We may use a more elaborate process to fabricate the transistors.

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1– *Jun-Cheng Liu, Chao-Hsin Chien, Chi-Chung Kei, Guang-Li Luo, Chao-Ching Cheng, Chien-Nan Hsiao, Tsong-Pyng Perng, and Chun-Yen Chang, " Atomic-layer-deposited Al_2O_3 thin films on Ge and Si substrates," AVS 6th International Conference on Atomic Layer Deposition 2006, July 24 ~ 26, 2006, Seoul, Korea.*

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of Ge-MOSFETs with atomic-layer-deposited Al_2O_3 high-κ gate dielectric)