國 立 交 通 大 學

電子工程學系　　電子研究所

碩士論文

新穎含氮氧化層應用於二氧化鉿儲存層快閃記憶體之研究

Study on Novel Oxynitride Layer Applied to Flash Memory using HfO_2 as Charge Trapping Layer

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中 華 民 國 九 十 六 年 七 月

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碩 士 論 文

A Thesis
Submitted to Department of Electronics Engineering &
Institute of Electronics
College of Electrical and Computer Engineering
National Chiao Tung University
in Partial Fulfillment of the Requirements
for the Degree of
Master of Science
in Electronics Engineering
July 2007
Hsinchu, Taiwan, Republic of China

中 華 民 國 九 十 六 年 七 月

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摘要

本論文著重於如何改善快閃記憶體的可靠度問題，如儲存資料的保留時間(retention)及元件的耐久度(endurance)。傳統快閃記憶體的穿隧氧化層(tunnel oxide)是採用乾氧成長二氧化矽(dry SiO_2)。但當氧化層厚度小於7奈米時，氧化層中的缺陷很容易產生漏電流路徑，使得被儲存在捕捉層(trapping layer)的電荷透過穿隧氧化層中的漏電路徑而流失，而造成資料的誤判。因此本論文採用新的含氮氧化層的技術取代傳統的乾氧化層，藉由減少界面狀態及層內的缺陷(interface states and bulk defects)來提升快閃記憶體的可靠度特性。而本論文所提出的新含氮氧化層製程技術是符合互補式金氧半(CMOS)場效電晶體的標準製程，因此對於目前工業界的生產技術是可行的改善方法。

傳統的非揮發性記憶體是採用複晶矽浮停閘(Poly-Silicon Floating Gate)作為電荷載子儲存的單元，而電荷在複晶矽中是均勻分佈的，因此若出現漏電路徑，儲存的電荷將會全部流失。而電荷在氮化矽中是屬於離散式的分佈，因此SONOS的結構被提出而取代傳統的複晶矽浮停閘。但為了提升快閃記憶體的寫入速度及降低操作電壓，本論文採用二氧化鉿層作為電荷捕捉層，稱之為SOHOS結構。我們一開始先從測試電容結構來找出最佳的二氧化鉿層退火條件，再將最佳條件運用於完整的快閃記憶體元件上，最後再做完整的電性測量分析。

由本論文的結果，可知道新的含氮氧化層可完全運用在快閃記憶體元件上，並且可以透過提升穿遂氧化層的品質，而達到改善快閃記憶體的可靠度問題。因此對於未來元件的尺寸微縮及改善特性，新穎的含氮氧化層製程技術是很有潛力及備受期待的。

Study on Novel Oxynitride Layer Applied to Flash Memory using HfO_2 as Charge Trapping Layer

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Abstract

This study focuses on how to improve the reliabilities of Flash memory, including the data retention and device endurance. The tunnel oxide of conventional Flash memory is dry SiO_2 layer. When the thickness of tunnel oxide layer is thinner than 7nm, the defects of tunnel oxide will form the leakage path easily. The trapped charges in trapping layer leak out through the leakage path and let we read the wrong data information. Therefore, the novel oxynitride process proposed in this study can replace the conventional dry oxide layer and improve the reliabilities of Flash memory by reducing the interface states and bulk defects. Moreover, the novel oxynitride process is compatible with standard CMOS process today and it is practicable improvement in industry manufacturing.

The charge storage unit of conventional nonvolatile memory is Poly-Silicon Floating Gate and the charges in poly-Si distribute uniformly. If there were leakage path, the trapping charges would all lead out. While the charges distribute discretely in Si_3N_4 layer, the SONOS structure was proposed and replaced the conventional poly-Si floating gate. To promote the program speed and lower the operating voltage, the HfO_2 layer worked as trapping layer in this study and was called SOHOS structure. At first we found the better PDA conditions of HfO_2 film from the test capacitors and applied the optimum condition in integrated Flash memory devices. Finally, the complete electrical measurements and analysis were carried out.

From the result of this study, we confirm that the novel oxynitride process can be applied in Flash memory cells fully. The oxynitride can promote the reliabilities of Flash memory by improving the quality of tunnel oxide. Therefore, in order to reach the scaling down and modification of memory device in the future, the novel oxynitride process is potential and expectable gradually.

誌謝

能在交大擁有兩年的碩士班學習生活，是十分令我驕傲且欣喜的事，在這個充滿豐富資源及挑戰性的環境下，培養我許多多元思考及製程實作的經驗，相信在未來，這些體驗都是彌足珍貴的；兩年來，感謝羅正忠教授提供實驗環境予我們專心學習，並且在IC技術這門課上辛勤的教學，更是讓所有電子所的學生能夠精確地掌握製程技術的關鍵，也才讓我能順利完成學業。此外也要感謝林伯村學長，常提供寶貴的建議及和我一起討論實驗上的細節，並且替實驗室籌畫了許多活動，凝聚實驗室的向心力，讓我可以在團結的力量下成長，也留下了許多深刻的回憶。也要感謝課堂上許多教授的諄諄教誨，讓我可以吸收許多知識及經驗，得以在實驗中發揮及體認IC技術的精髓。

在實驗室生活中，感謝大峰、宏仁、智仁、信智、德安、建宏的相伴，在碩一沈重的課業壓力下，大家一起討論課業內容及挑燈苦讀準備考試的情景，都是十分難忘的回憶，並且在無塵室中通宵趕進度的沈悶環境下，也是有各位的相互支持，大家才可以順利完成實驗，也要感謝瓊惠學姊、宏春學長、紀伯、國源、文昱、一桀、俐婷、睿龍、勝凱及無塵室內的許多工程師，有大家相互幫忙之下，營造出一個優質的研究環境。

最後這一刻的喜悅，要獻給我的父親林文義先生、母親陳麗詩女士及胞弟正華，有你們的支持與關懷及提供強力的後盾，可以讓我在求學生涯中無後顧之憂的往前邁進；此外要謝謝宜貞，彼此相互扶持度過了實習生活及碩士班入學考試，並且在這兩年內作為我的心靈導師，總是給我安慰與鼓勵，也指導我許多GRE的準備方向，感謝妳並祝福妳早日順利完成夢想。要感謝的人太多，在此向所有幫助過我的人致上最深的敬意，祝福大家都健康、平安、順利，感恩。

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CHAPTER 1

Introduction

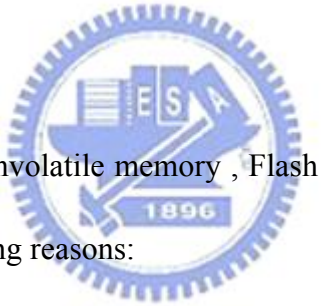
1.1General Background

The application of semiconductor memory is more and more indispensable for the modern living. For instance, the semiconductor memories are used in personal computers, cellular phones, digital cameras, smart-media, networks, automotive systems, global positioning systems. Table 1.1 lists the characteristics of different types of semiconductor memory that either have been commercialized or are being developed in the industry.

Since the demonstration of the MOSFET in 1960, one of the most revolutionary technology driver to decide the direction of semiconductor industries development is the semiconductor memories. Because of the high cost, large volume, and high power consumption of the magnetic-core memory, the electronic industries urgently needed a new kind of memory device to replace the magnetic-core memory. In 1967, D. Kahng and S. M. Sze invented the first floating-gate (FG) nonvolatile semiconductor memory at Bell Labs [1]. To date, the stacked-gate floating gate device structure, as shown in Fig. 1-1, continues to be the most prevailing nonvolatile-memory implementation, and is widely used in both standalone and embedded memories. The invention of FG memory impacts more than the replacement of magnetic-core memory, and creates a huge industry of portable electronic systems. The most

widespread memory array organization is the so-called Flash memory, which has a byte-selectable write operation combined with a sector “flash” erase.

In the past decade, memory chips with low power consumption and low cost have attracted more and more attention due to the booming market of portable electronic devices such as cellular phones and digital cameras. These applications require the memory to have ten years data retention time, so that the nonvolatile memory (NVM) device has become indispensable. There are mainly four types of nonvolatile memory technology: Flash memory, Ferro-electric Random Access Memory (FeRAM), Magnetic Random Access Memory (MRAM) and Phase Change Memory (PCM).



Among four types of nonvolatile memory , Flash memory is presently the most suitable choice for the following reasons:

(1)FeRAM is not a perfect nonvolatile memory since its reading mode is a kind of destructive operation. A programming verification is required to restore the data after reading. On the contrary, Flash memory doesn’t need the additional action. This means that the reading operation of Flash memory is not destructive, and the operation affects slighter data retention disturbance than FeRAM.

(2) Flash memory can achieve the highest chip density. A Flash memory cell consists of only one transistor [2]. A FeRAM memory cell generally consists of one transistor and one capacitor [3], while a MRAM cell needs a transistor and a magnetic tunnel junction [4]. Phase Change Memory was expected to be a promising

nonvolatile memory [5]; however, its memory cell consists of one resistor and a bipolar junction transistor. Until now, only a 256MB phase change memory chip has been demonstrated. It will take more effort to demonstrate whether the Phase Change Memory is really a promising technology.

(3) Flash memory possesses the multi-bit per cell storage property [6]. Four distinct threshold voltage (V_{th}) states can be achieved in a Flash memory cell by controlling the amount of charge stored in its floating gate. Two-bits/cell (with four V_{th} states) Flash memory cells have already been commercialized. A four-bits/cell Flash memory device is feasible and is under development now [7]. Multi-bit storage increases memory density and thus reduces the cost per bit significantly. Furthermore, Matrix Semiconductor Inc. demonstrated multi-layer (sometimes called "three-dimensional integration") SONOS Flash memory recently [8]. This novel idea offers another possibility to achieve even higher density and lower cost technologies based on Flash memory.

(4) Flash memory fabrication process is compatible with the current CMOS process and is a suitable solution for embedded memory applications. A Flash memory cell is simply a MOSFET cell, except that a poly-silicon floating gate [9] (or Silicon Nitride charge trap layer [8]) is sandwiched between a tunnel oxide and an inter-poly oxide to form a charge storage layer. All other nonvolatile memories require integration of new materials that are not as compatible with a conventional CMOS process. It is easier and more reliable to integrate Flash memory than other nonvolatile memories with logic and analog devices in order to achieve better chip performance for wireless communication and wireless computation [10].

Since Flash memory possesses above four key advantages, it has become the mainstream nonvolatile memory device nowadays.

The Flash memory cell structure was presented for the first time by D. Kahng and S. M. Sze in 1967. And the famous commercial Flash memory is Intel ETOX (EPROM Tunnel Oxide) structure in 1988 [11]. The ETOX device structure is shown in Fig. 1-2. The operation principal is using the underside poly-silicon which is named Floating Gate (FG) as the charge store unit for the device. And the ETOX are "written" and "erase" by Channel-Hot-Electron (CHE) programming and Fowler-Nordheim tunneling (F-N) or Band-to-Band-Hot-Hole (BTBHH),respectively. After electrons which injected from channel, the threshold voltage of devices will be shifted. The logical "0"and "1" definition of nonvolatile memory devices are used for the difference between threshold voltage (Fig. 1-3). This detail of the concept will be described in Chapter 2.

Although a huge commercial success, conventional FG devices have their limitations. Two of the most primary limitations are: (1) the limited potential for continued scaling down of the device structure. This scaling down limitation results from the extreme requirements of the tunnel oxide layer. The tunnel oxide must be thin enough to allow quick and efficient charge transport to and from the floating gate (FG). On the other hand, the tunnel oxide needs to provide superior isolation under retention, endurance, and disturbed conditions in order to maintain information integrity over periods of up to a decade. When the tunnel oxide is thinner for

operation speed consideration, the retention characteristics may be degraded. And when the tunnel oxide is made thicker to take the isolation into account, the speed of the operation will be slower. Therefore, for mass production, there is a trade-off between speed and reliability for the optimal tunnel oxide thickness. (2) The quality and strength of tunnel oxide after plenty of program/erase cycles. Once a leaky path has been created in the tunnel oxide, all the charges stored in the floating gate will be lost. Therefore, two suggestions, Poly-Silicon/Oxide/Nitride/Oxide/Silicon (SONOS) [12-14] and nanocrystal nonvolatile memory devices [15-17], are proposed to overcome this oxide quality limit of the conventional FG structure. These technologies replace the floating gate structure with a great number of charge-storage nodes in the dielectric or in the nanocrystal. Unlike the floating gate, stored charges in isolated nodes cannot easily redistribute among themselves and the local leaky path will not cause the fatal loss of information for the nanocrystal nonvolatile memory device. This effectively prevents the leakage of all the stored charges out of the floating gate.

The charge storage elements in SONOS memory (Fig. 1-4) are the charge traps distributed throughout the volume of the Si_3N_4 layer. A typical trap has a density of the order 10^{18}~10^{19} cm^{-3} according to Yang et al [18] and stores both electrons and holes (positive charges) injected from the channel. The nitride-based memory devices were extensively studied in the early 70s after the first metal-gate nitride device metal/nitride/oxide/silicon (MNOS) was reported in 1967 by Wegener et al [19]. Initial device structures in the early 1970s were p-channel metal-nitride-oxide-silicon

(MNOS) structures with aluminum gate electrodes and thick (45nm) silicon nitride charge storage layers. Write/erase voltages were typically 25-30 V. In the late 1970s and early 1980s, scaling moved to n-channel silicon-nitride-oxide-silicon (SNOS) devices with write/erase voltages of 14-18 V. In the late 1980s and early 1990s, n- and p-channel SONOS devices emerged with write/erase voltages of 5-12 V. In the SONOS device, an oxide layer is introduced between the gate and the nitride region. Thus, it forms the $SiO_2/Si_3N_4/SiO_2$ (ONO) gate dielectric stack instead of capping the nitride layer with just a metal or semiconductor gate. The purpose of the top blocking oxide is to reduce the charge injection from the control gate into the nitride layer, limiting the memory window of both MNOS and SNOS devices.

During programming, the control gate is biased positively so that electrons from the channel can tunnel across the SiO_2 into the nitride layer. Some electrons will continue to move through the nitride layer then across the control oxide finally into the control gate. The remaining trapped charges in the nitride layer provide the electrostatic screening of the channel from the control gate. Therefore, there is a threshold voltage (V_{th}) shift resulting from trapped charges in nitride and because of that SONOS can be used as a memory device just like conventional floating gate devices.

In past decade, about 20% of semiconductor market is given by the semiconductor memory. And the output value of Flash memory is expected to reach US$ 60 billions in 2010. Developing the higher-capacity and faster Flash nonvolatile

memory is always one of the most important issues for a wide range of applications. In order to pursue the goal, down sizing or multi-bit is the key point for pushing next generation development. And the most important performances of Flash memory are reliability characteristics, such as program/erase cycling and data retention. It is well known that the tunnel oxide degradation during FN (Fowler-Nordheim) stress is due to the oxide trap and interface trap generation. Thus, how to improve the reliability of Flash memory is the focus in this study.

1.2 Motivation

According to the International Technology Roadmap for Semiconductors (ITRS) [20], high-k dielectric materials would be able to maintain an equivalent potential difference from the floating gate to the device body for a larger thickness compared to SiO_2. The charge leakage of trap layer would be minimized and the scaling limits would be extended.

In addition, using high-k dielectric trapping layer (which is called SOHOS, Poly-Silicon/Silicon-Oxide/High-k/Silicon-Oxide/Silicon) show some advantages, for instance, high program/erase speed, easy to fabricate, low power consumption and low programming voltage, better potential for scalability below the 70-nm node, according the ITRS. Hafnium oxide (HfO_2) is consider to replace the Si_3N_4 trapping layer of SONOS-type Flash memory[21]. HfO_2 is expected to have better charge trapping characteristics than the conventional Si_3N_4 film. Because of the density of trap state and deep trap energy level SOHOS can achieve longer retention time than

SONOS [22-24].

Although SONOS Flash memory device has attracted much attention due to its advantages over the traditional floating-gate Flash memory device, it still faces challenges for further improvement. For example, the tunnel oxide thickness cannot be reduced below 25Å to improve the programming speed, if 10-years retention time must be guaranteed [25]. As shown in Fig. 1-5, there are two charge-loss mechanisms: (1) direct tunneling, with an associated barrier height φ_o+E_t ; and (2) thermally assisted de-trapping into the nitride conduction band and subsequent tunneling through the tunnel oxide, with associated barrier height φ_o. A high conduction band offset φ_o between the trapping layer and the tunnel oxide is essential for achieving long retention time. The offset φ_o for a nitride trapping layer is only 1.05 eV and the offset φ_o for HfO_2 trapping layer is up to 1.6 eV. Because of the valid reason we choose the HfO_2 film as the trapping lever rather than Si_3N_4 film in this research.

The other method to modify the retention and endurance of Flash memory is improving the tunnel oxide quality and strength. When the Flash memory device through plenty of program/erase (P/E) cycles, the tunnel oxide degradation during FN (Fowler-Nordheim) stress is due to the oxide traps and interface traps generation. If the oxide thickness is reduced below 10nm, high-field stress manifests through a degradation of the insulating properties of the oxide well before the occurrence of breakdown. Stress-induced leakage currents (SILC) are responsible for serious data retention problems in Flash memory and represent the main concern in the process of

scaling the tunnel oxide thickness to lower values. Thus, a JVD silicon-nitride was studied to replace the dry tunnel oxide due to its higher dielectric constant and the low stress-induced leakage current (SILC) in recently years [26-27]. However, the interface between Nitride/Silicon is not as good as the SiO_2/Silicon interface and the Si-SiN barrier height is lower than that of Si-SiO_2 [27-28]. Therefore, the oxide layer with nitrogen treatment (called Oxynitride film) is also a popular choice and has been studied broadly because of its excellent endurance [29-30]. This film proves the promising candidate to substitute thermal oxide right now.

In this study , we proposes a novel process for forming an ultrathin oxynitride film with high nitrogen topping. The oxynitride growth includes three main process stages－chemical oxide growth, nitridation and subsequent dry oxidation. By this technique, the desirable nitrogen concentration profile can be obtained to meet the requirement of device performance. By replacing the conventional dry oxide film with novel oxynitride film, we expect to advance the reliabilities of the Flash memories.

1.3 Organization of This Thesis

This dissertation is divided into four chapters. The contents in each chapter are described as follows.

In chapter 1, the potential memory devices about nonvolatile memory (NVM)、conventional Flash、SONOS and SOHOS devices are introduced in this chapter.

In chapter 2, this section focus on the basic program and erase mechanisms of

Flash memory device.

In chapter 3, the SOHOS structure with HfO_2 trapping layer , oxynitride and oxide as tunnel oxide layer is proposed in this section. Finally, compare the oxynitride layer with convention oxide layer, the device characteristics will be discussed between two different tunnel oxide process conditions.

In chapter 4, this section includes the conclusions and the future work of this study..

Memory type	DRAM	SRAM	Flash-NOR	Flash-NAND	FRAM	MRAM	Phase change memory
Cell size factor (F^2)	6~12	90~150	**8~10**	**4**	18	10~20	5~8
Largest array built (Mb)			**256**	**2Gb**	64	1	4
Volatile/Non-volatile	Volatile	Volatile	**NV**	**NV**	NV	NV	NV
Endurance write/read	∞ /∞	∞ /∞	10^6 / ∞	10^6 / ∞	10^{12} / 10^{12}	10^{14} / ∞	10^{12} / ∞
Read	Destructive	Partially-destructive	**Non-destructive**	**Non-destructive**	Destructive	Non-destructive	Non-destructive
Read/Program voltage (V)	**~1**	**~1**	2/10	2/18	1.5/1.5	3.3/3.3	**0.4/1**
Program/Erase/Read speed, ns	50/50/8	**8/8/8**	1us/1-100ms (block)/60ns	1ms/1-100ms/60 ns	80/80/80	30/30/30	50/50/50
Direct over-write	Yes	Yes	**No**	**No**	Yes	Yes	Yes
Bit/byte Write/Erase	Yes	Yes	Yes	Block erase	Yes	Yes	Yes
Read dynamic range (margin)	100-200mV	100-200mV	**Delta current**	**Delta current**	100-200mV	20-40% R	10X-100XR
Programming energy	*Medium*	*Medium*	*High*	*Low*	*Medium*	*Medium*	Low
Transistors	Low performance	High performance	High voltage	High voltage	Low performance	High performance	High performance
CMOS logic compatibility	Bad	Good	Ok, but Hi V needed	Ok, but Hi V needed	Ok, but Hi V needed		Good
New materials	Yes	No	No	No	Yes	Yes	Yes
Scalability limit	Capacitor	6T (4T possible)	Tunnel oxide/HV	Tunnel oxide/HV	Polarizable capacitor	Current density	Lithography
Multi-bit storage	No	No	**Yes**	**Yes**	No	No	No
3D potential	No	No	Possible	Possible	?	?	No
SER susceptibility	Yes	Yes	No	No	Yes	No	No
Relative cost per bit	Low	High	Medium	Medium	High	?	Low
Extra mask needed for embedded memory			6-8		2	4	3-4
In production	Yes	yes	Yes	Yes	Yes	2004	N/A

Table 1.1: Performance Comparison between volatile memory (DRAM and SRAM) and nonvolatile memory (Flash, FRAM, MRAM and phase change memory) devices. Among the nonvolatile memories, Flash memory is the only memory compatible with the current CMOS process flow. Overall, the Flash memory exhibits the best performance except for the disadvantages of high programming voltage and slow program/erase speed.

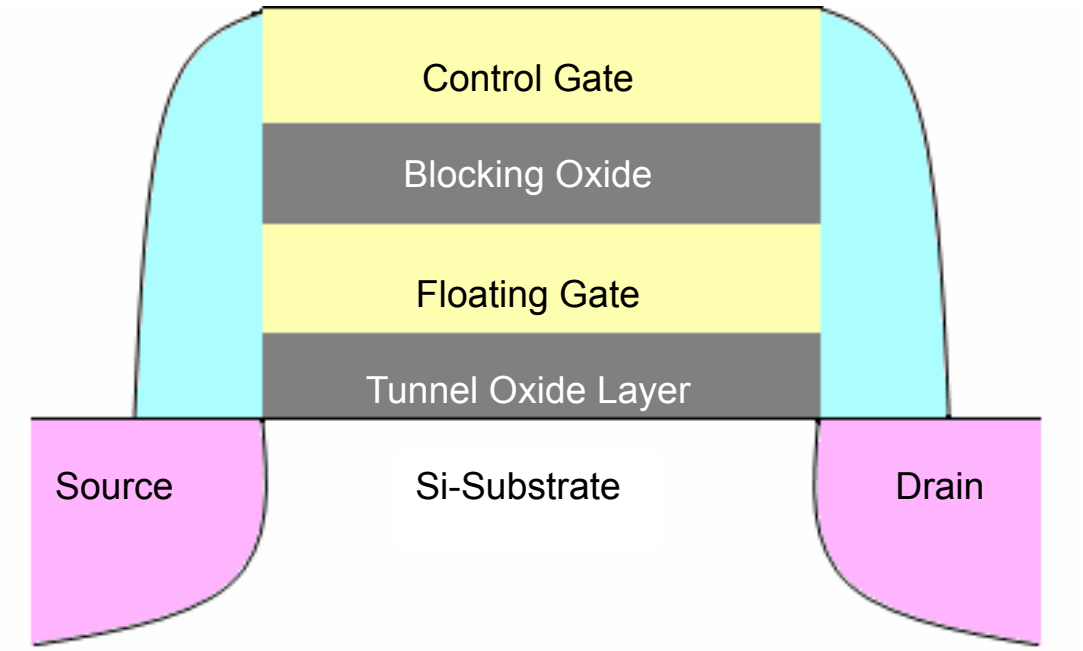


Fig1-1: Schematic cross section of the conventional floating gate nonvolatile memory device. Poly-Si floating gate is used as the charge storage element.

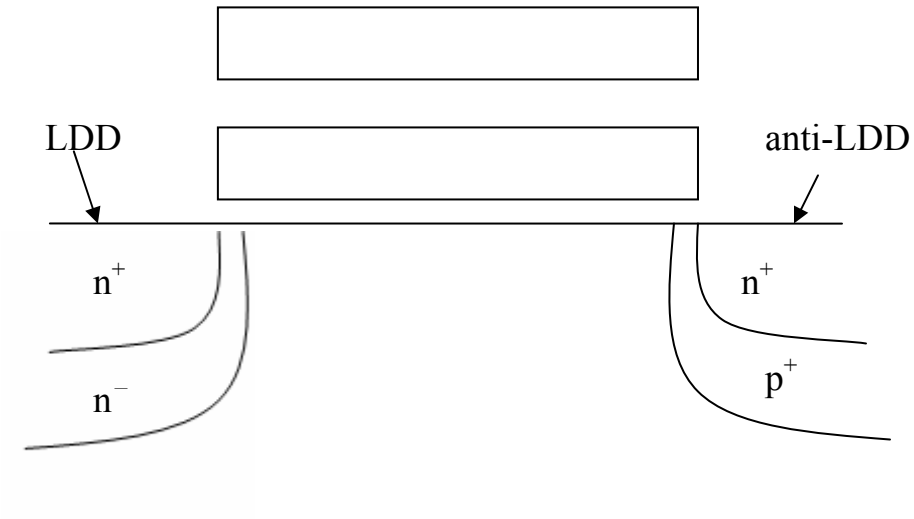


Fig1-2: Schematic cross section of ETOX device.

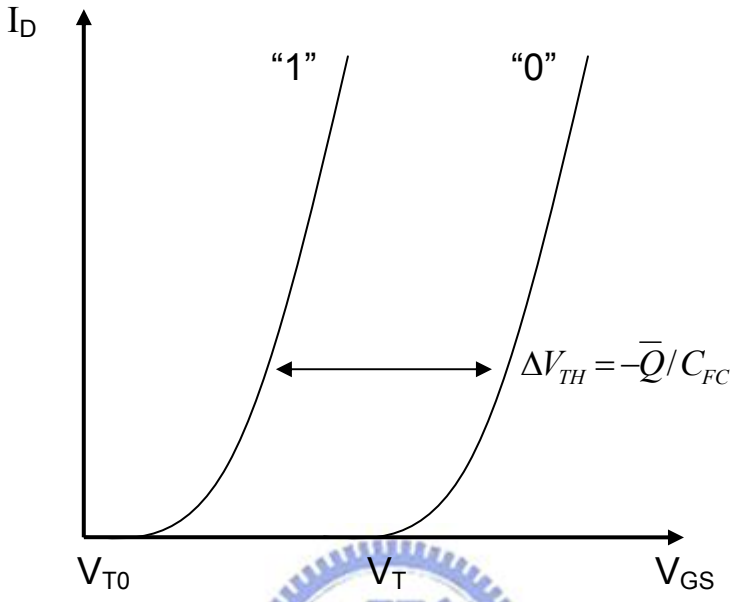


Fig1-3: I-V curves of a floating gate device when there is no charge stored in the FG ("1"-curve) and when a negative charge $\bar{Q}$ is stored in the FG ("0"-curve).

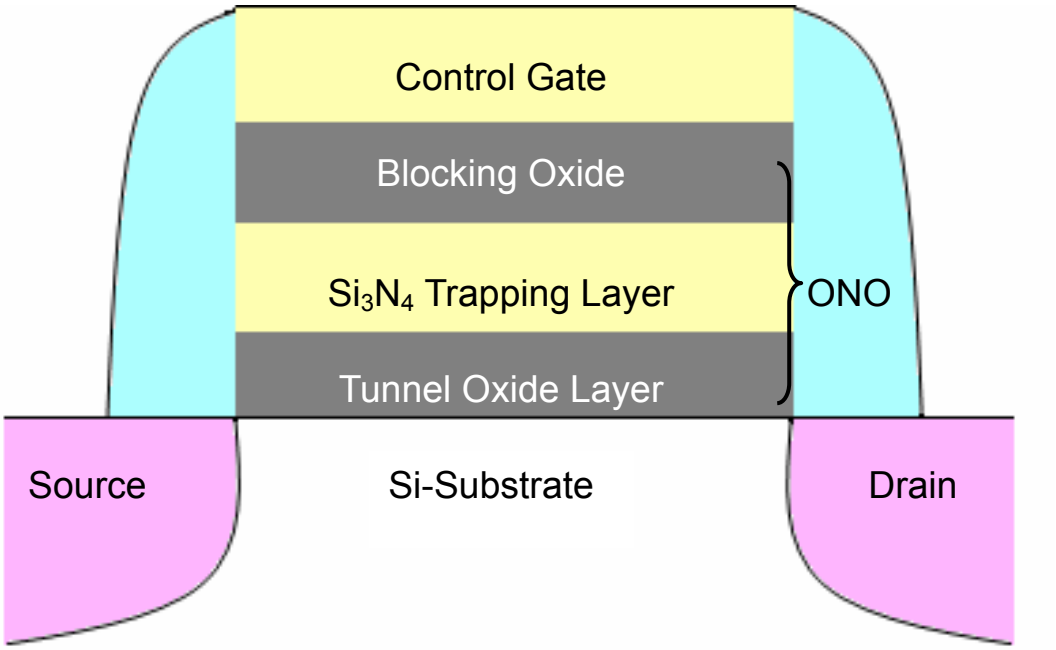


Fig1-4: Schematic cross section of the SONOS nonvolatile memory device. The nitride layer is used as the charge-trapping element.

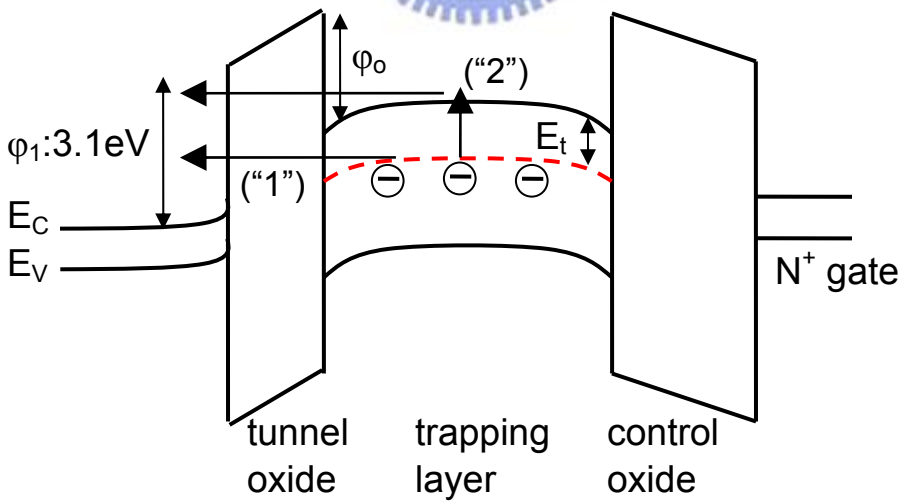


Fig1-5: Energy band diagrams of SONOS Flash memory. Large φ_o will block electron leakage effectively and improve retention time.

CHAPTER 2

Basic Principles of Nonvolatile Memory

2.1 Program/Erase Operation Mechanisms

Most of operations on novel nonvolatile memories, such as nanocrystal and SONOS memories are base on the concept of Flash memory. If charge has to be stored in a bit of the memory, there are some different procedures. The threshold voltage shift of a Flash memory transistor can be written as [31-32]:

$$\Delta V_{TH} = -\frac{\overline{Q}}{C_{FC}} \quad \text{.....eq. 2-1}$$

where $\overline{Q}$ is a negative charge stored in the FG, and C_{FC} is the capacitances between the floating gate (FG) and control gate. The threshold voltage of the memory cell can be altered by changing the amount of charge present between the gate and the channel, corresponding to the two states of the memory cell, i.e., the binary values ("1" and "0") of the stored bit. Figure 1-3 shows the threshold voltage shift between two states in a Flash memory. Regarding a nonvolatile memory, it can be "written" into either state "1" or "0" by either "programming" or "erasing" operation, which are decided by the definition of memory cell itself. There are many solutions to achieve "programming" or "erasing". In general, hot carrier electron injection (HCEI), F-N tunneling and band to band tunneling (BTBT), are three kinds of common operation mechanism employed in novel nonvolatile memories. The three mechanisms will lead difference characteristics for nonvolatile memories.

2.1.1 Channel Hot-Electron Injection (CHEI)

The physical mechanism of CHEI is relatively simple to understand qualitatively. An electron traveling from the source to the drain gains energy from the lateral electric field and loses energy to the lattice vibrations (acoustic and optical phonons). At low fields, this is a dynamic equilibrium condition, which holds until the field strength reaches approximately 100kV/cm [33]. For fields exceeding this value, electrons are no longer in equilibrium with the lattice, and their energy relative to the conduction band edge begins to increase. Electrons are "heated" by the high lateral electric field, and a small fraction of them have enough energy to surmount the barrier between oxide and silicon conduction band edges. Figure 2-1 shows schematic representation of CHEI MOSFET and the energy-distribution function with different fields. On the other hand, the effective mass of hole is heavier than one of electron. It is too hard to obtain enough energy to surmount oxide barrier. Therefore, hot-hole injection rarely is employed in nonvolatile memory operation. For an electron to overcome this potential barrier, three conditions must hold [34].

(1) Its kinetic energy has to be higher than the potential barrier.

(2) It must be directed toward the barrier.

(3) The field in the oxide should be collecting it.

During programming, the positive voltages applied to the gate and drain while the source is grounded. These voltages generate a lateral and vertical electric field along the channel. The electrons will move from the source to the drain and be accelerated by high lateral field near the drain junction in the channel. Once the

electrons gain enough energy, they can surpass the energy barrier of the oxide layers and inject into trapping layer and be trapped. The current density of CHEI is expressed as

$$I_{inj} = A_d I_{ds} (\frac{\lambda E_m}{\varphi_b})^2 e^{(-\varphi_b / E_m \lambda)} \quad \text{.....eq. 2-2}$$

Here I_{ds} is the channel current and A_d is a constant.

2.1.2 Tunneling Injection

Tunneling mechanisms are demonstrated in quantum mechanics. Basically, tunneling injection must to have available states on the other side of the barrier for the carriers to tunnel into. If we assume elastic tunneling, this is a reasonable assumption due to the thin oxide thickness involved. Namely, no energy loss during tunneling processes. The tunneling probability, depending on electron barrier height ($\varphi(x)$), tunnel dielectric thickness (d), and effective mass (m_e), is express as

$$T = \exp(-2\int_0^d \frac{\sqrt{\varphi(x)^* m_e}}{\hbar} dx) \quad \text{.....eq. 2-3}$$

Tunneling through the oxide can be attributed to different carrier-injection mechanisms. Which process applies depends on the oxide thickness and the applied gate field or voltage. Direct tunneling (DT), Fowler-Nordheim tunneling (FN), modified Fowler-Nordheim tunneling (MFN) and trap assistant tunneling (TAT) are the main programming mechanisms employed in memory [35-38].

2.1.2-(a) Direct Tunneling (DT)

For nanocrystal memories, the control-gate coupling ratio of nanocrystal memory devices is inherently small [39]. As a result, FN tunneling cannot serve as an efficient write/erase mechanism when a relatively thick tunnel oxide is used, because the strong electric field cannot be confined in one oxide layer. The direct tunneling is employed in nanocrystal memories instead. In the other hand, the direct tunneling is more sensitive to the barrier width than barrier height, two to four orders of magnitude reduction in leakage current can still be achieved if large work function metals, such as Au or Pt [40].

2.1.2-(b) Fowler–Nordheim Tunneling (FN)

The Fowler–Nordheim (FN) tunneling mechanism occurs when applying a strong electric field (in the range of 8~10MV/cm) across a thin oxide. In these conditions, the energy band diagram of the oxide region is very steep. Therefore, there is a high probability of electrons' passing through the energy barrier itself. Using a free-electron gas model for the metal and the WKB (Wentzel-Kramers-Brillouim) approximation for the tunneling probability [41], one obtains the following expression for current density [42]:

$$J = E_{ox}{}^{2} \exp\left[\frac{-8\pi(2m_{ox}^{*})^{1/2}(q\Phi_{B})^{3/2}}{3hqE_{ox}}\right] \quad \text{.....eq. 2-4}$$

Where Φ_B is the barrier height (3.1eV for Si-SiO_2) , m_{ox}^{*} is the effective mass

of the electron in the forbidden gap of the dielectric, *h* is the Planck's constant, *q* is the electronic charge, and *Eox* is the electric field which is defined as the applied voltage divided by total thickness of the tunnel and control oxide. Figure 2-2 shows the F-N tunneling mechanism.

2.1.2-(c) Modified Fowler–Nordheim Tunneling (MFN)

Modified Fowler–Nordheim tunneling (MFN) is similar to the traditional FN tunneling mechanism, yet the carriers enter the nitride at a distance further from the tunnel oxide-nitride interface. MFN mechanism is frequently observed in SONOS memories. The SONOS memory is designed for low-voltage operation (<10V, depending on the Equivalent oxide thickness), a relatively weak electrical field couldn't inject charges by DT or FN tunneling mechanism. Figure 2-3 shows the MFN tunneling mechanism.

2.1.2-(d) Trap Assistant Tunneling (TAT)

The charge storage mediums with many traps may cause another tunneling mechanism. For example, the charges tunnel through a thin oxide and arrive to the traps of nitride layer at very low electrical field in SONOS systems. During trap assisted injection the traps are emptied with a smaller time constant then they are filled. The charge carriers are thus injected at the same distance into the nitride as for MFN injection. Because of the sufficient injection current, trap assistant tunneling may influence in retention [43]. Figure 2-4 shows the TAT tunneling mechanism.

2.1.3 Band to Band Tunneling (BTBT)

In MOS structures, band-to-band tunneling typically occurs at high source or drain voltage and low gate voltage. In Flash memory devices, these conditions take place in cells under erase operations, or in unselected cells sharing the same bit line with a cell under programming. BTBT contributes to the so called Gate Induced Drain Leakage current (GIDL) [44-45] , which can be a significant fraction of the subthreshold drain leakage current and can compromise proper functioning of the substrate bias generators.

Band to band tunneling application to nonvolatile memory was first proposed in 1989. I. C. Chen and et al. demonstrated a high injection efficiency (~1%) method to programming EPROM devices [46]. Band-to-band Tunneling (BTBT) process occurs in the deeply depleted doped surface region under the gate to drain or gate to source overlap region. Figure 2-5 shows the band diagram of a MOS and illustrates BTBT mechanism. In this condition, the band-to-band tunneling current density is expressed as

$$J_{b-b} = \frac{\sqrt{2m^*}q^3\varepsilon V_{app}}{4\pi^3\hbar^2 E_g^{1/2}}\exp[-\frac{4\sqrt{2m^*}E_g^{3/2}}{3q\varepsilon\hbar}] \quad \text{.....eq. 2-5}$$

2.1.3-(a) Band to Band Hot Electron Tunneling Injection

When band-bending is higher than the energy gap of the semiconductor, the tunneling electron from the valence band to the conduction band becomes significant.

The mechanism is at the condition for positive gate voltage and negative drain voltage. Hence, the hot electrons are injected through the tunnel oxide and then recombine the stored holes as shown in Figure 2-6.

2.1.3-(b) Band to Band Hot Hole Tunneling Injection

The injection is applied for p-type substrate nonvolatile memory device. The mechanism is at the condition for negative gate voltage and positive drain voltage. Hence, the hot holes are injected through the tunnel oxide and then recombine the stored electrons as shown in Figure 2-7.

2.2 Nonvolatile Memory Device Reliability

For a nonvolatile memory, the performance worthy to concern is distinguishing between two states of memory cell. However, in many times operation and charges storage for a long term, the states are not easily distinguishable because of charges loss. The nonvolatility of NVM implies at least 10 years of charge retention, and the cell has to store information also after many read/program/erase cycles. Endurance (also called Cycling) and retention experiments are performed to investigate Flash memory cell reliability.

2.2.1 Retention

In any nonvolatile memory technology, it is essential to maintain data for over ten years. This means the loss of charge stored in the storage medium must be as

minimal as possible. For instance, in 16Mbit Flash cell, floating gate capacitance is approximately 1fF, a threshold voltage shift of 3V is requested, and a programmed cell stores around 10,000 electrons in its floating gate. A loss of only 10% in this number can lead to a wrong read of the cell, therefore a loss of less than 2 electrons per week can be tolerated.

For SONOS memory devices, data are represented as electrons stored in the silicon nitride layer, the stored electrons leak away from the trapping layer through the tunnel oxide or through the interpoly dielectrics; moreover, the lateral migration of charges trapped in the silicon nitride layer also result in the wrong information [47-48]. Possible causes of charge loss are: (1) by tunneling or thermionic emission mechanisms; (2) defects in the tunnel oxide; and (3) detrapping of charge from insulating layers surrounding the storage medium.

First, several discharge mechanisms may be responsible for time and temperature dependent retention behavior of nonvolatile memory devices. Figure 2-8 shows a bandgap diagram of a SONOS device in the excess electron state, illustrating trap-to-band tunneling, trap-to-trap tunneling, and band-to-trap tunneling, thermal excitation and Poole-Frenkel emission retention loss mechanisms [49]. These mechanisms may be classified into two categories. The first category contains tunneling processes which are not temperature sensitive (trap-to-band tunneling, trap-to-trap tunneling and band-to-trap tunneling). The second category contains the other mechanisms which are temperature dependent. Moreover, trapped electrons may

redistribute vertically inside the nitride by Poole–Frenkel emission, which will give rise to a shift in the threshold voltage.

Secondly, the generation of defects in the tunnel oxide can be divided into an extrinsic and an intrinsic one. The former is due to defects in the device structure; the latter to the physical mechanisms which are used to program and erase the cell. Finally, electrons can be trapped in the insulating layers surrounding the storage medium during wafer processing. The electrons can subsequently de-trap with time, especially at high temperature. However, the charge variation results in a variation of the storage medium potential.

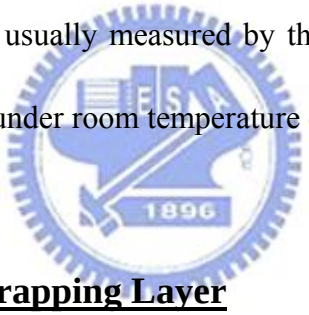
Retention capability of Flash memories has to be checked by using accelerated tests which usually adopt high electric fields and hostile environments at high temperature.

2.2.2 Endurance

Endurance is the number of erase/write operations that the memory can still complete and continue to operate as specified in the data sheet. In general, Flash cells are requested to guarantee 10^5 erase/program cycles. This endurance requirement is sufficient for the user to take 700 photos with a 1MB size every day for 10 years [48]. As the experiment was performed applying constant pulses, the variations of program and erase threshold voltage levels are described as “program/erase threshold voltage window closure” and give a measure of the tunnel oxide aging [50-51]. In particular,

the reduction of the programmed threshold with cycling is due to trap generation in the oxide and interface state generation at the drain side of the channel. The evolution of the erase threshold voltage reflects the dynamics of net fixed charge in the tunnel oxide as a function of the injected charge. The initial lowering of the erase is due to a pile-up of positive charge which enhances tunneling efficiency, while the long-term increase of the erase is due to a generation of negative traps.

The endurance characteristics give the memory threshold voltage window, which is the threshold voltages difference between the programmed state and the erased state. It is the parameters to describe how reliable is a nonvolatile memory cell. The program/erase cycles are usually measured by the FN tunneling or channel hot electron injection mechanism under room temperature environment.



2.3 High-k Material as Trapping Layer

In order to improve the programming speed and/or lower the programming voltage of a SONOS-type memory device, it is desirable to use a trapping material with a lower conduction band edge (higher electron affinity) to achieve a larger offset φ_o, as well as to provide for programming by direct tunneling at low voltages. Recently, high-k ("high-permittivity") dielectric materials such as HfO_2 and ZrO_2 have been investigated to replace thermal oxide as the MOSFET gate dielectric [52-53]. A comparison of dielectric material properties is given in Table 2.1. Such materials have a lower conduction band edge than does silicon nitride. Thus, it should be advantageous to use a high-k material as the trapping layer in a SONOS-type

memory device, provided that it contains a sufficient density of deep trap states. The electron trap level E_t has been reported to be 1.0 eV for ZrO_2 [52]; it has been reported to be 1.5eV for JVD HfO_2 [53]. In principle, the trap density and trap energy level in a high-k trapping layer can be tuned by adjusting the deposition process parameters.

For SOHOS (Poly-Silicon/Oxide/High-k/Oxide/Silicon) devices, the charges may be trapped in electron and hole traps in the HfO_2 layer or by charge confinement in the quantum well. From the ideal energy band diagrams of SONOS and SOHOS structures shown in Fig. 2-9 (a) and (b), respectively, the quantum well formed by the conduction band is deeper for the SOHOS structure as compared to the SONOS structure (1.6 eV compared to 1.05 eV) [54-55]. Therefore, at the same gate bias where modified Fowler–Nordheim (MFN) tunneling dominates, the electrons must tunnel through a thicker energy barrier in SONOS to the conduction band of the charge storage layer (Si_3N_4) as compared to SOHOS. The conduction band offset of Si_3N_4 with respect to silicon is 2.05 eV, as compared to a 1.5 eV conduction band offset of HfO_2 with respect to silicon. This is illustrated in Fig. 2-10, where the modified F–N tunneling consists of direct tunneling through the thin tunnel oxide layer and F–N tunneling through the charge storage layer. Hence, electron tunneling and storage in the quantum well will be easier in SOHOS as compared to SONOS devices.

Material	Si_3N_4	HfO_2	ZrO_2
Conduction band(eV)*	2.05	1.5	1.5
φ_o (eV)	1.05	1.6	1.6
K	7.5	24	24
E_t(eV)	0.8~1.0	1.5	1.0

* relative to Si conduction band.

Table 2.1: Trapping material properties

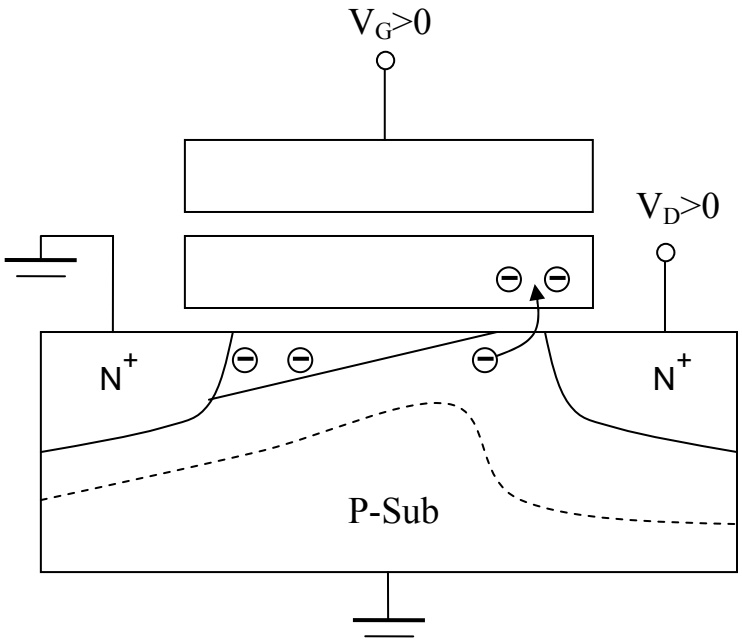


Fig 2-1: The procedure of channel hot electrons injection (CHEI).

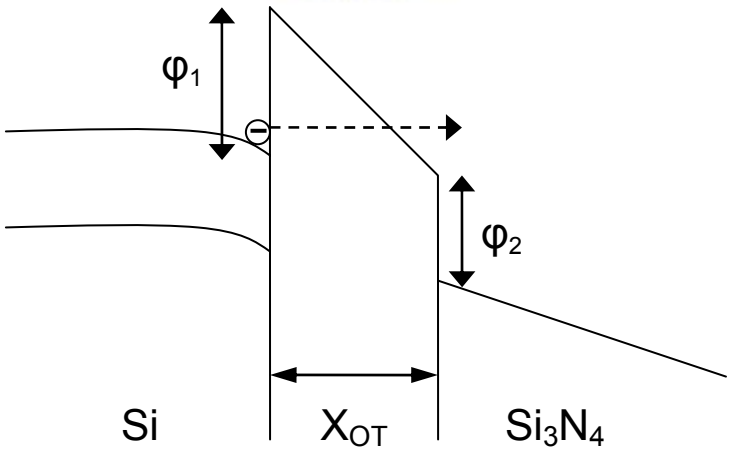


Fig 2-2: The approach of FN programming method, when $|E_{OT}| > \frac{\phi_1}{X_{OT}}$

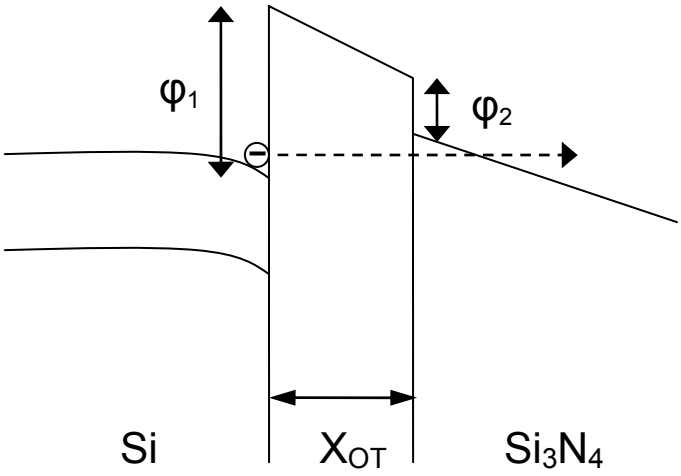


Fig 2-3: The approach of MFN programming method,

$$\text{when}\ \frac{\phi_1-\phi_2}{X_{OT}} > |E_{OT}| > \frac{\phi_1-\phi_2}{X_{OT}+\left(\varepsilon_{OX}/\varepsilon_N\right)X_N}$$

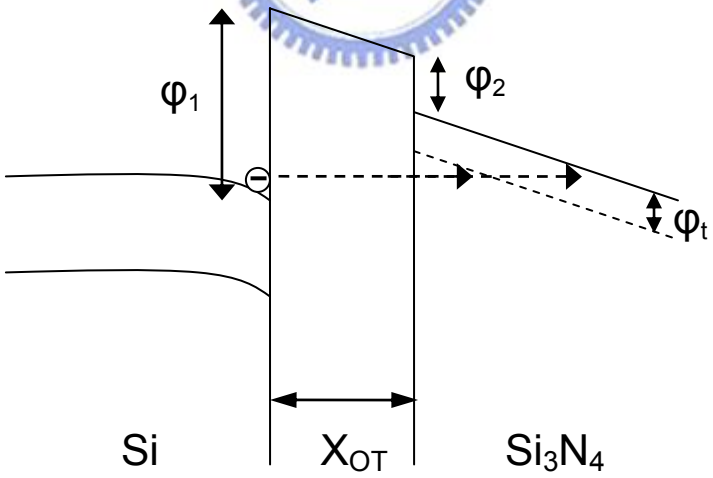


Fig 2-4: The approach of TAT programming method,

$$\text{when}\ \frac{\phi_3}{X_{OT}} > |E_{OT}| > \frac{\phi_3}{X_{OT}+\left(\varepsilon_{OX}/\varepsilon_N\right)X_N}, \phi_3 = \phi_1-\phi_2-\phi_t$$

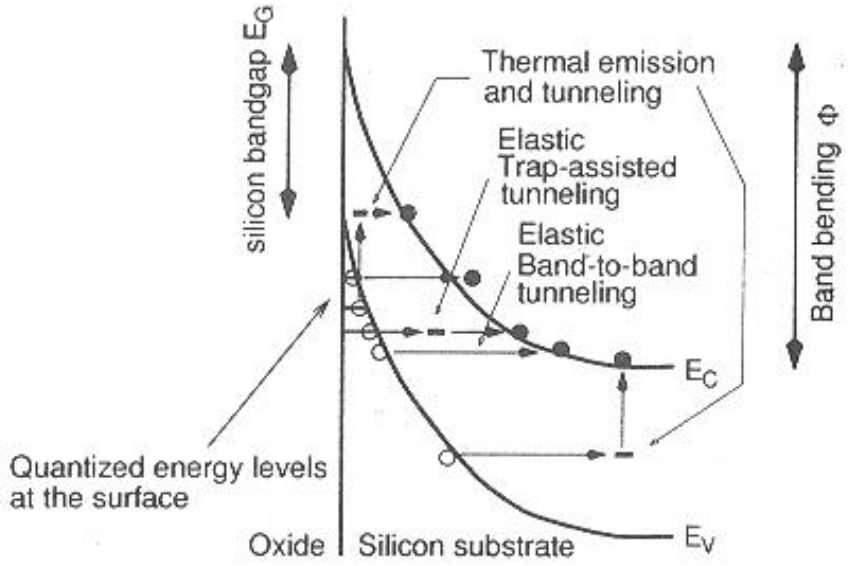


Fig 2-5: Band diagram of a MOS structure along the vertical direction through the depletion region illustrating band-to-band and trap-to-band tunneling mechanisms.

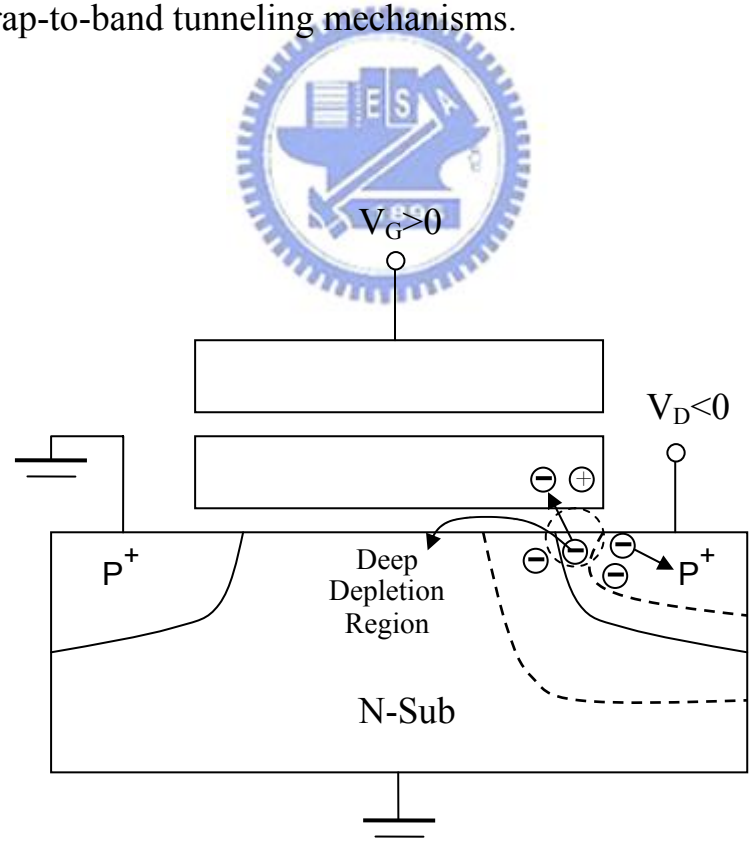


Fig 2-6: The procedure of band to band hot electron injection.

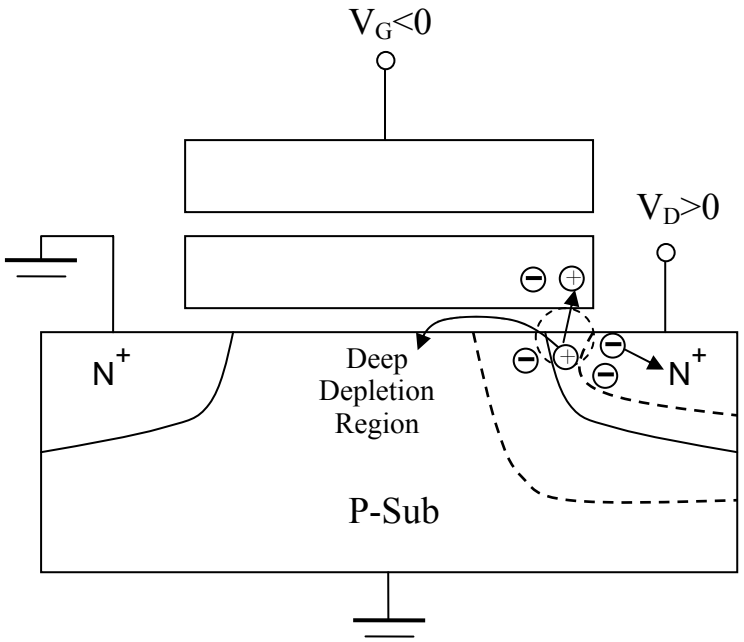


Fig 2-7: The procedure of band to band hot hole injection.

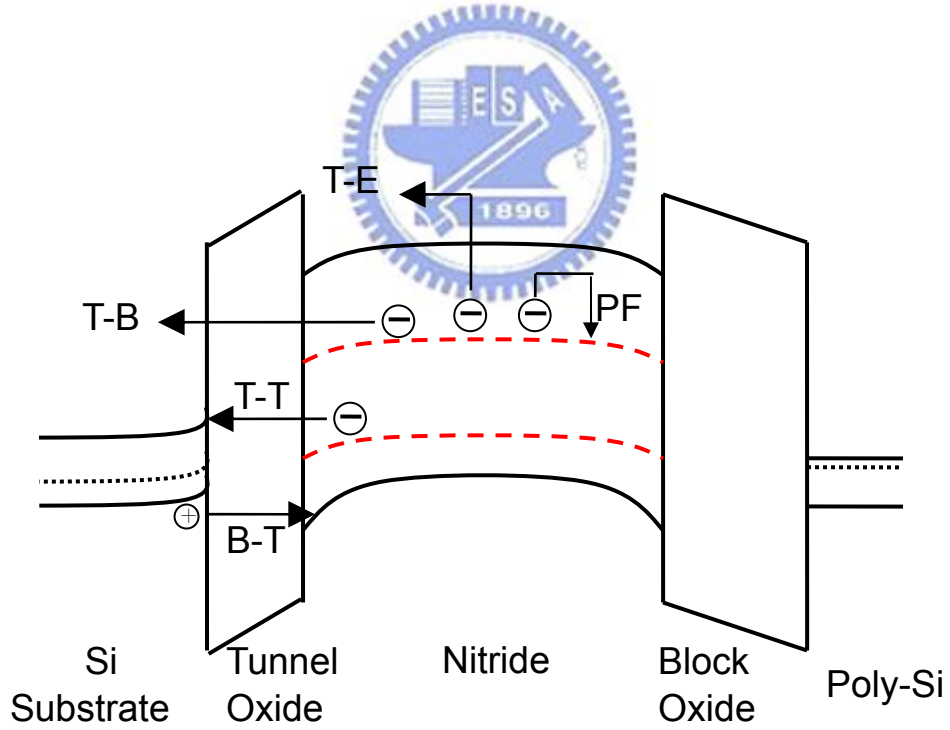


Fig 2-8: Bandgap diagram of a SONOS device in the excess electron state, showing retention loss mechanisms: trap-to band tunneling (T-B), trap-to-trap tunneling (T-T), band-to-trap tunneling (B-T), thermal excitation (TE) and Pool-Frenkel emission (PF).

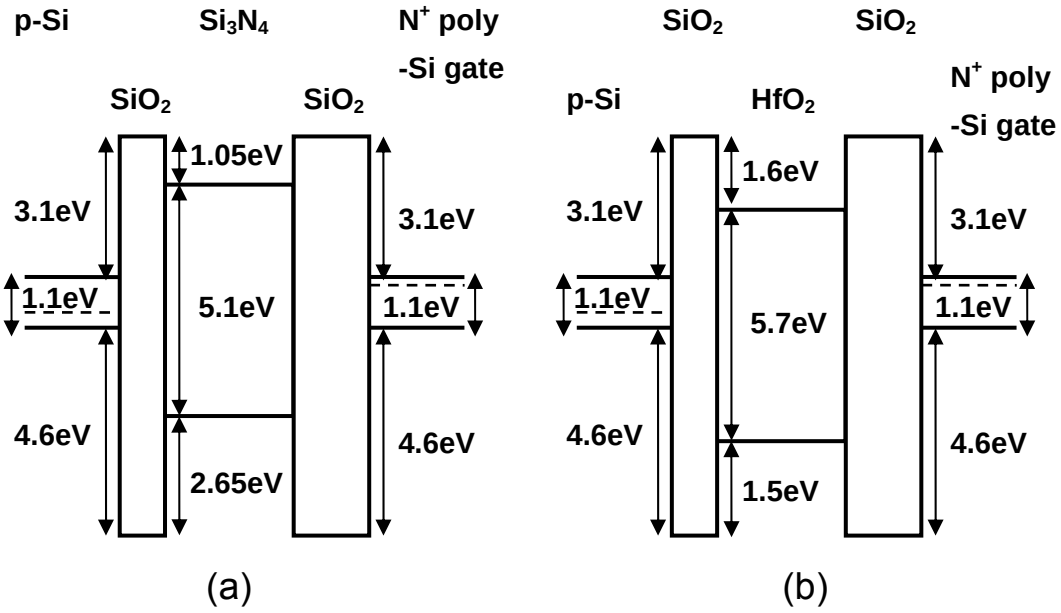


Fig 2-9: Ideal energy band diagrams for (a) SONOS and (b) SOHOS structures.

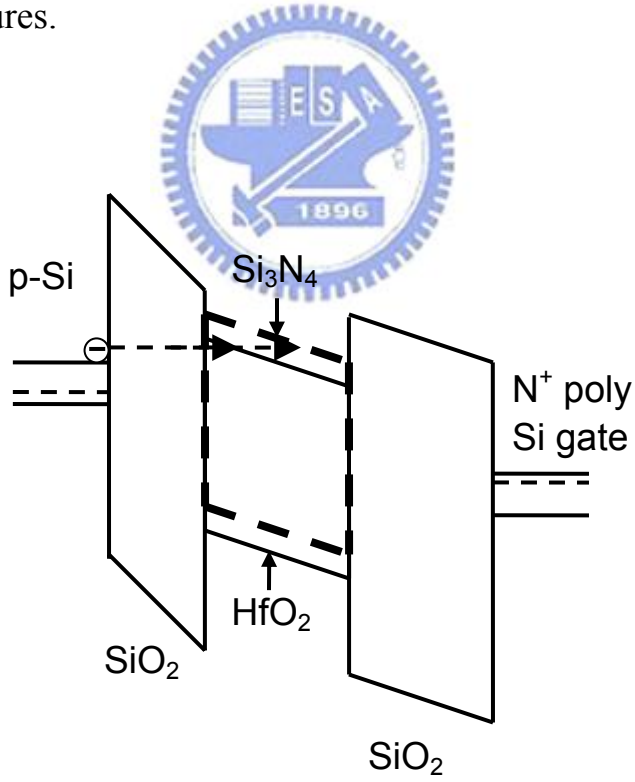


Fig2-10: Energy band diagram schematic of the SONOS structure with HfO_2 (solid lines) or Si_3N_4 (dashed lines) as the charge storage layer during write (program) operations.

CHAPTER 3

Device Fabrication and Characterization

3.1 Introduction

The high-k memory structure has drawn increasing attention in application for nonvolatile Flash memory device due to it's superior charge trapping properties compared to the conventional poly-silicon floating gate. The high-k material sandwiched between two silicon oxide (SiO_2) layers to form the Poly-Silicon/Oxide/High-k/Oxide/Silicon (SOHOS) structure, stores charges in spatial deep level traps, making it less vulnerable to a single defect in the tunnel oxide. This significantly helps to minimize the discharge of the memory cell [56]. During the program operation of the SOHOS n-channel transistor device, electrons tunneled through the tunnel oxide and are stored in the deep level traps [57]. During the erase operation under negative gate bias, electrons trapped in the high-k material are detrapped via tunneling through the oxide layer into the silicon substrate. Therefore, the HfO_2 material is selected in our research and we will look for the optimum process conditions.

Recently, oxynitride film is applied in Flash memory because of the small charge trapping amount and the low stress-induced leakage current [58-59]. In general, benefit of a silicon oxynitride film is that the nitrogen accumulates at the silicon interface to reduce the concentration of strained Si-O bond and the creation of hot

electrons as many as three orders of magnitude. Nowadays, lower process temperature and thinner oxynitride films are preferred in ULSI technology. In this study, we proposed a novel approach for forming an oxynitride tunnel dielectric with high nitrogen content. In the oxyenitride, we can obtain Si-rich at the bottom and N-rich at the top. The desirable structure can be obtained to meet the requirement of the SONOS type nonvolatile memory device performance.

3.2 Experiments

Firstly, we make the test HfO_2 capacitors in order to obtain the optimum condition of the process temperature for the SOHOS memory device in this study. The detail of all process parameters (also called split table) will be describes later.

3.2.1 Fabrication of Test HfO_2 Capacitor

Figure 3-1 (a)-(b) schematically depicts the cross-section and the process flow of the proposed test HfO_2 capacitors. The fabrication process of the capacitors were carried out on 4-inch p-type (100)-oriented silicon substrate wafers. The resistivity of the wafer is about 15-25 Ω cm. First of all, the wafers were cleaned down by standard RCA cleaning. Before growing the tunnel oxide film, the all wafers were dipped into diluted HF solution to remove the chemical oxide which grown during the standard RCA cleaning.

Subsequently, the cleaned wafers were steeped into H_2O_2 solution at room

temperature immediately. The immersion process let wafers grow about 10 Å chemical oxide in 20 min [60]. Then the chemical oxide carried out the nitridation process through LPCVD (Low Pressure Chemical Vapor Deposition) furnace in low-pressure (180 mTorr) NH_3 ambient at 750℃ for 15 min. Next, the nitrided chemical oxide was placed in atmospheric O_2 ambient at 900℃ for 70 sec. Now, the whole tunnel oxide process is completed, and the initial chemical oxide already became the oxynitride film. Nevertheless, the tunnel oxide of another control sample is only grown in atmospheric furnace at 900℃. Then 45~50 Å HfO_2 film was deposited by Dual E-gun evaporate deposition system, followed by post-deposition annealing (PDA) in the nitrogen ambient using a RTA (Rapid Temperature Annealing) system. The split table of PDA temperature is listed in Table 3.1. Afterward, about 150 Å blocking oxide was deposited by PECVD (Plasma Enhanced Chemical Vapor Deposition). In order to improve the quality of the blocking oxide film, the samples were carried out RTA densification in O_2 ambient at 600℃ for 30 sec.

To form the top electrode, about 5000 Å aluminum (Al) metal film was deposited by sputtering system. Then the Al film was patterned and sintered to define the capacitors. Finally, a 5000 Å Al film was also deposited on the backside of the wafers as the lower electrode of the capacitors. Before the lower electrode film deposition, the backside native oxide must be stripped by using BOE (Buffered Oxide Etchant) to reduce the contact resistance.

In the same process condition, a nitrogen distribution profile across the 35Å

oxynitride tunnel oxide layer was revealed by secondary ion mass spectrometry (SIMS) in Fig. 3-2. Apparent high nitrogen concentration with a peak located at the tunnel oxide top surface is observed. Such high nitrogen concentration is more helpful in resisting the boron penetration phenomenon of the gate dielectric from the P^+-poly-silicon gate. Moreover, the lower nitrogen concentration at the interface lying in between tunnel oxide and Silicon substrate also improves the reliability of the devices.

3.2.2 Fabrication of HfO_2 Trapping Layer Memory Device

Figure 3-3 (a)-(b) schematically depicts the cross-section and the process flow of the SOHOS Flash memory cell with HfO_2 trapping layer. The experimental process of the memory device were carried out on 4-inch p-type (100)-oriented silicon substrate wafers. The resistivity of the wafer is about 15-25 Ω cm. First of all, the wafers were cleaned down by standard RCA cleaning. Before growing the tunnel oxide film, the all wafers were dipped into diluted HF solution to remove the chemical oxide which grown during the standard RCA cleaning.

In the same way, the characteristics of HfO_2 memory devices should be compared between the control and experimental samples. Therefore, the tunnel oxide of control sample grew in atmospheric furnace at 900℃. Subsequently, the experimental devices were steeped into H_2O_2 solution at room temperature immediately. The immersion process let wafers grow about 10 Å chemical oxide in 20 min. Then the chemical oxide carried out the nitridation process through LPCVD

(Low Pressure Chemical Vapor Deposition) furnace in low-pressure (180 mTorr) NH_3 ambient at 750℃ for 15 min. Next, the nitrided chemical oxide was placed in atmospheric O_2 ambient at 900℃ for 70 sec. Now, the whole tunnel oxide process is completed, and the initial chemical oxide already become the oxynitride film. Then 45~50 Å HfO_2 film was deposited by Dual E-gun evaporate deposition system, followed by post-deposition annealing (PDA) in the nitrogen ambient using a RTA (Rapid Temperature Annealing) system. Afterward, about 150 Å blocking oxide was deposited by PECVD (Plasma Enhanced Chemical Vapor Deposition). In order to improve the quality of the blocking oxide film, the samples were carried out RTA densification in O_2 ambient at 600℃ for 30 sec. Then, the poly-silicon gate 3000 Å is formed by LPCVD at 900℃ for 30 min. After poly-silicon/blocking oxide/HfO_2/tunnel oxide stack formation, gate pattern were defined by lithography and etched back. Subsequently, the Source/Drain was formed in $POCl_3$ ambient at 900℃ for 30 min and then carried out Drive-in process in nitrogen ambient at 900℃ for 30 min. Next, the passivation layer 5000 Å followed removing the PSG (Phosphorous Silicon Glass) on the gate, source and drain region. Then we define the contact hole by lithography and BOE etching back.

To form the top metal pad, about 5000 Å aluminum (Al) metal film was deposited by sputtering system. Then the Al film was patterned and sintered to define the metal pad. Finally, a 5000 Å Al film was also deposited on the backside of the wafers as the substrate contact of the device. Before the substrate contact film deposition, the backside native oxide must be stripped by using BOE (Buffered Oxide

Etchant) to reduce the contact resistance.

Figure 3-4 schematically describes the construction of measurement system. The electrical characteristics of SOHOS memory device and test capacitors are measured by HP4284 Precision LCR Meter and HP4156C Precision Semiconductor Parameter Analyzer.

3.3 Results and Discussions

We probe into the electrical characteristics of the test capacitors and the HfO_2 SOHOS memory devices in this section.

3.3.1 Electrical Characteristic of HfO_2 Capacitor

Fig 3-5(a),(b) is the capacitance-voltage (C-V) hysteresis curve of Cap-N6 and Cap-O6. The counterclockwise direction of the hysteresis curve is present. At first the upper electrode of capacitor was biased from 8V to -8V, and the inversion layer of silicon substrate turned into the accumulation layer gradually. When the capacitor was operated in the positive gate voltage, the electrons of inversion layer inject into the trapping layer through F-N tunneling mode. Then these electrons will be trapped in the HfO_2 layer and let the V_{FB} (flat-band voltage) of capacitor shift to the positive side. On the other hand, when the capacitor is biased from negative voltage, the trapped electrons maybe tunnel back to substrate or the holes can also inject into the trapping layer and combine with the trapped electrons. These two phenomenon can reduce the

amount of trapped electrons in charge storage layer and form the left C-V curve. Subsequently, Fig 3-6(a),(b) show the program characteristics of Cap-N6、Cap-O6 in different program voltages. We can observe that Cap-O6 is slower than Cap-N6. This is attributed to the thicker tunnel oxide layer of Cap-O6. Because the less electric field across the thicker tunnel oxide results in the less F-N tunneling current. The erase characteristics of Cap-N6、Cap-O6 with different erase voltages is expressed in Fig 3-7(a),(b). Next, we start to concern about the reliability of capacitors. Fig 3-8(a),(b) show the retention characteristic of Cap-N6、Cap-O6 at room temperature. After 10 years (about 3×10^8 sec.), there is the larger V_{FB} shift window between program state and erase state in Cap-N6 than Cap-O6. The data retention degradation attributes to the charge loss. Some possible causes of charge loss are defects in tunnel oxide, defects in blocking oxide or mobile ion contamination. Therefore, the better retention characteristic in Fig 3-7(a) reveals that the oxynitride tunnel oxide has less defects and can improve the retention of Flash memory. In order to confirm the improvement, the retention after 10^5 program/erase cycles is introduced in Fig 3-9(a),(b). After 10 years, the V_{FB} shift window shrink for Cap-N6 and Cap-O6, while the retention characteristics of Cap-N6 still better than Cap-O6. These retention results reveal that the oxynitride process can reduce the defects of tunnel oxide effectively and reform the date integrity of Flash memory [61-62] . The endurance characteristics of Cap-N6 and Cap-O6 is shown in Fig 3-11. After repeatedly program/erase operation, the V_{FB} window between program and erase states is narrower in Cap-O6 and make the distinguishability of program and erase states difficult. Therefore, the oxynitride

tunnel oxide process can also modify the endurance characteristic of Flash memory.

The counterclockwise C-V hysteresis curve of 700℃、800℃、900℃ samples are shown in Fig 3-12(a),(b)、Fig 3-13(a),(b)、Fig 3-14(a),(b). These indicate that the tunneling electrons are dominant from the substrate, not from the gate of capacitor. The clockwise C-V hysteresis curve relates to the gate injection phenomenon and isn't expected for Flash memory. The program characteristics of other capacitors is shown in Fig 3-15(a),(b)、Fig 3-16(a),(b)、Fig 3-17(a),(b), respectively. To compare the program speed simply, the time for V_{FB} shift reach 2V is listed in Tab 3.2. The higher PDA temperature, the faster speed is present, especially for 800℃ samples. The reason for faster program speed is that HfO_2 trapping layer is more crystallized in complete PDA treatment [63]. Fig 3-18(a),(b)、Fig 3-19(a),(b)、Fig 3-20 (a),(b) are the erase characteristics of other capacitors. Now, we analyze the retention characteristics in Fig 3-21(a),(b)、Fig 3-22(a),(b)、Fig 3-23(a),(b)、Fig 3-24(a),(b)、Fig 3-25(a),(b)、Fig 3-26(a),(b). The data retention of oxynitride tunnel oxide is better than conventional oxide tunnel oxide. There are rising phenomenon in erase state curve of Fig 3-9(a),(b)、Fig 3-24(a),(b)、Fig 3-25(a),(b)、Fig 3-26(a),(b). The rising tendency results from the degradation of PECVD blocking oxide after plenty of program/erase operations and some electrons inject into the trapping layer through degraded blocking oxide. Similarly, the all retention characteristics is collected and analyzed in Fig 3-27(a),(b)、Fig 3-28(a),(b)、Fig 3-29(a),(b). Finally, the endurance characteristic of other capacitors is still better for oxynitride than conventional oxide tunnel oxide,

as shown in Fig 3-30, Fig 3-31, Fig 3-32.

3.3.2 Electrical Characteristic of HfO_2 Memory Device

This section will analyze the electric characteristics of the SOHOS Flash memory with HfO_2 trapping layer. The former paragraph already revealed and investigated the test capacitors and found the optimum condition for fabricate the integrated Flash memory devices. The condition chosen by us is PDA 800℃ for 30 sec. in N_2 ambient and the split table is listed in Table 3.3. The cause is it has the faster program/erase speed and the more suitable retention characteristic. Although PDA 900℃ sample performs the best program characteristic, the initial and after cycles retention isn't satisfied. Therefore, we thought that the 900℃ PDA will induce more traps with shallower energy level in the trapping layer, which give rise to larger memory window and poor charge retention[64]. Fig 3-33(a) and Fig 3-33(b) show the I_D-V_G curve of Flash memory devices. Then the memory devices are programmed by CHE and erased by FN tunneling, as shown in Fig 3-34(a), Fig 3-34(b), Fig 3-35(a), Fig 3-35(b). The CHE (channel hot electron) program is to set V_D=V_G=6V or V_D=V_G=7V and the FN erase is to set V_G=-5V or V_G=-6V in device cells. Subsequently, the compared retention property of Device-N and Device-O is shown in Fig 3-36. The result that the Device-N performs the better retention characteristic is observable. This indicates that the novel oxynitride process is applied not only in capacitor structures but in integrated Flash memory cells and can improve the data retention all. Similarly, the endurance of two memory devices is shown in Fig 3-38

and the Device-N is superior than Device-O. Therefore, from the measurements of test capacitors and devices, we understand the tunnel oxide with oxynitride process can modify the reliabilities of Flash memory indeed.

3.4 Summary

In order to verify the novel oxynitride process proposed in this study can reform the reliabilities of Flash memories, we began looking for the optimum process conditions form test capacitors and applied them in integrated memory device cells. From the electrical measured results, we can confirm that the thinner conventional tunnel oxide has the drawback of reliability and will limit the scaling down technology of Flash memories. If we replace the conventional oxide with oxynitride process technology, the initial interface states and defects generation after repeatedly operations can be diminished. This is helpful to the integrity of stored data and to recognize the states of Flash memory. Moreover, we adopt standard CMOS manufacturing processes in this study. It means that the improvement method doesn't need impracticable process in industry manufacturing. So the novel oxynitride process is suitable for the foundries which request low cost and efficiency today.

	PDA 600℃	PDA 700℃	PDA 800℃	PDA 900℃
Oxynitride layer (35 Å)	Cap-N6	Cap-N7	Cap-N8	Cap-N9
Oxide layer (41 Å)	Cap-O6	Cap-O7	Cap-O8	Cap-O9

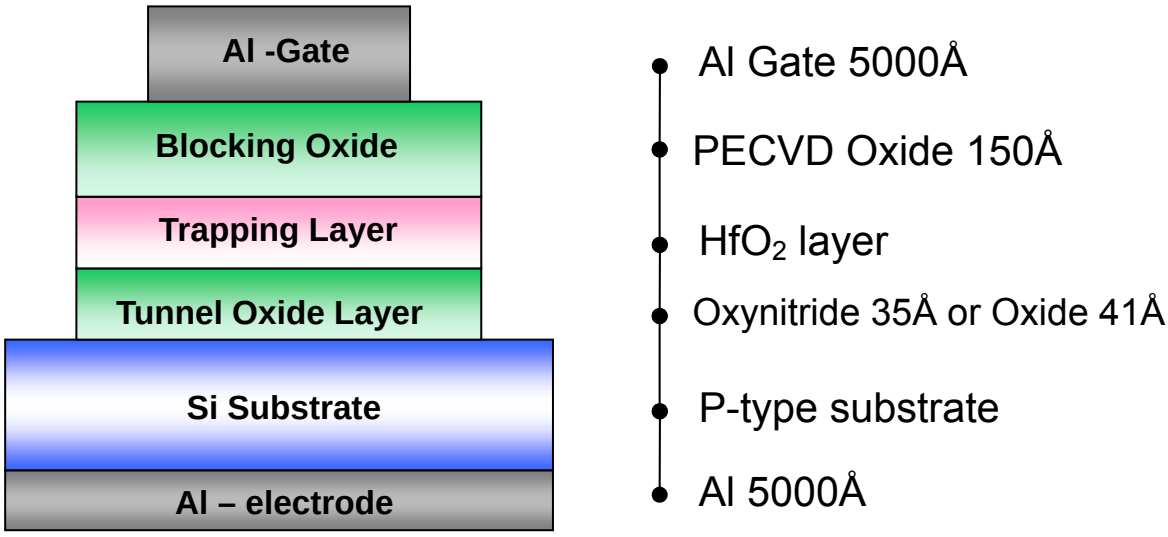
Table 3.1: The split table of test capacitors.

	PDA 600℃	PDA 700℃	PDA 800℃	PDA 900℃
Oxynitride layer	8.6×10^{-1}	0.93	1.12×10^{-2}	9.97×10^{-4}
Oxide layer	9.3×10^{-1}	1.3	1.68×10^{-2}	2.05×10^{-3}

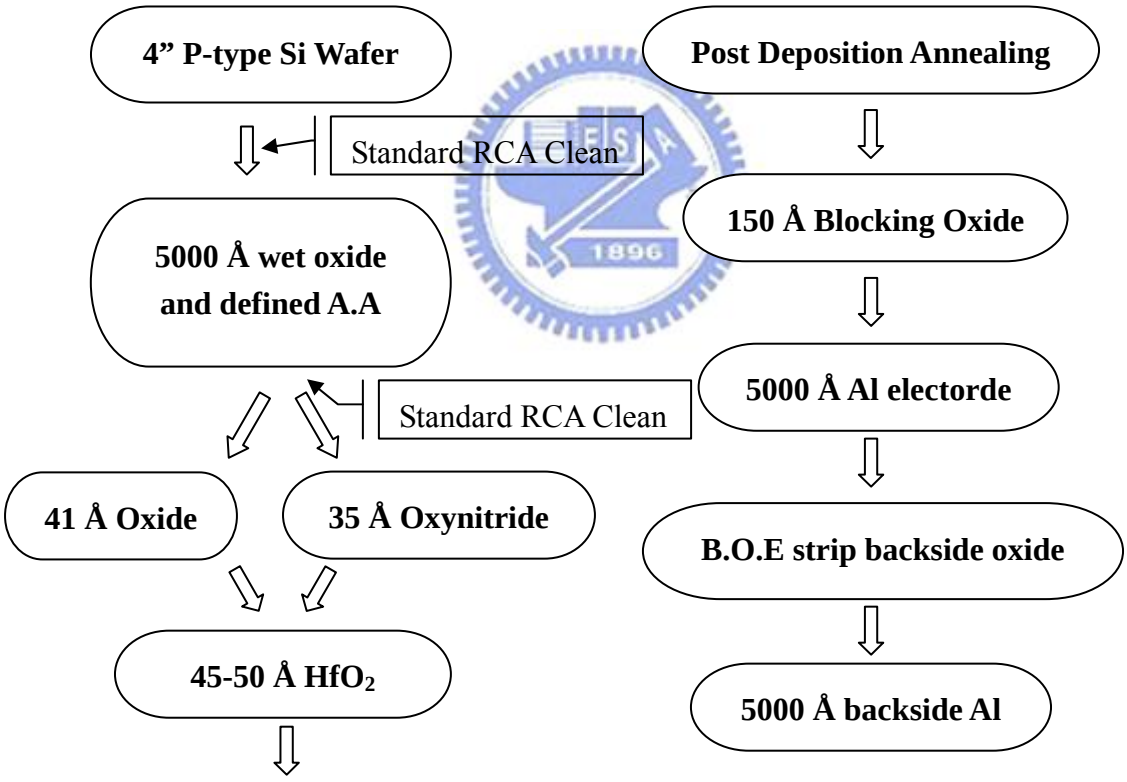
Table 3.2: The time for V_{FB} shift reach 2V with V_G=18V (unit:sec.).

Tunnel oxide layer	Oxynitride	Oxide
PDA 800℃	Device-N	Device-O

Table 3.3: The split table of SOHOS Flash memory devices.



(a)



(b)

Figure 3-1: (a)Schematic cross section of the HfO_2 test capacitors. (b) Process flows for fabricating various HfO_2 test capacitors.

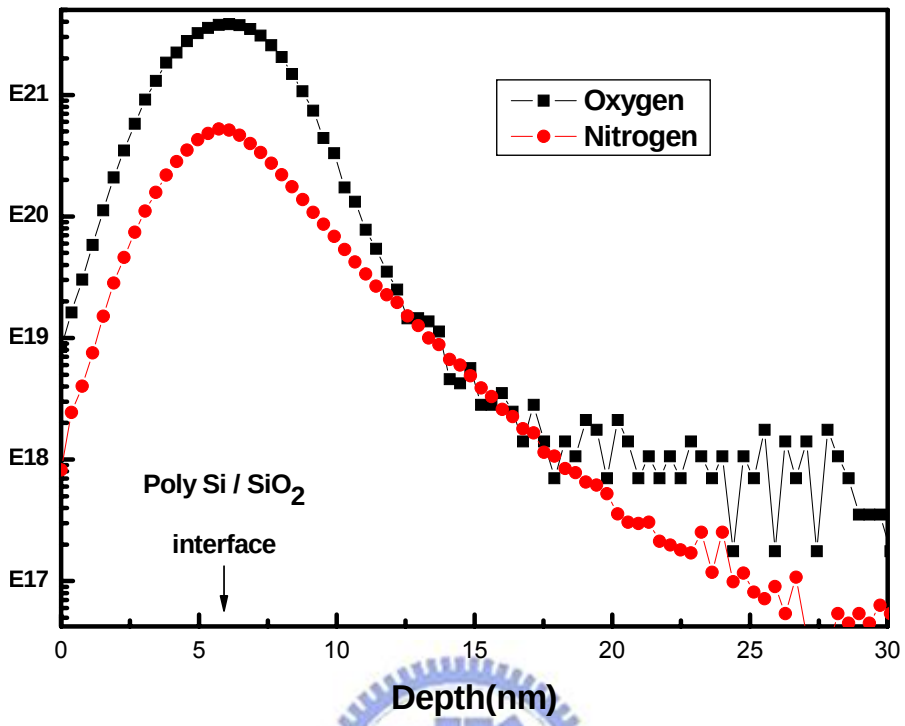
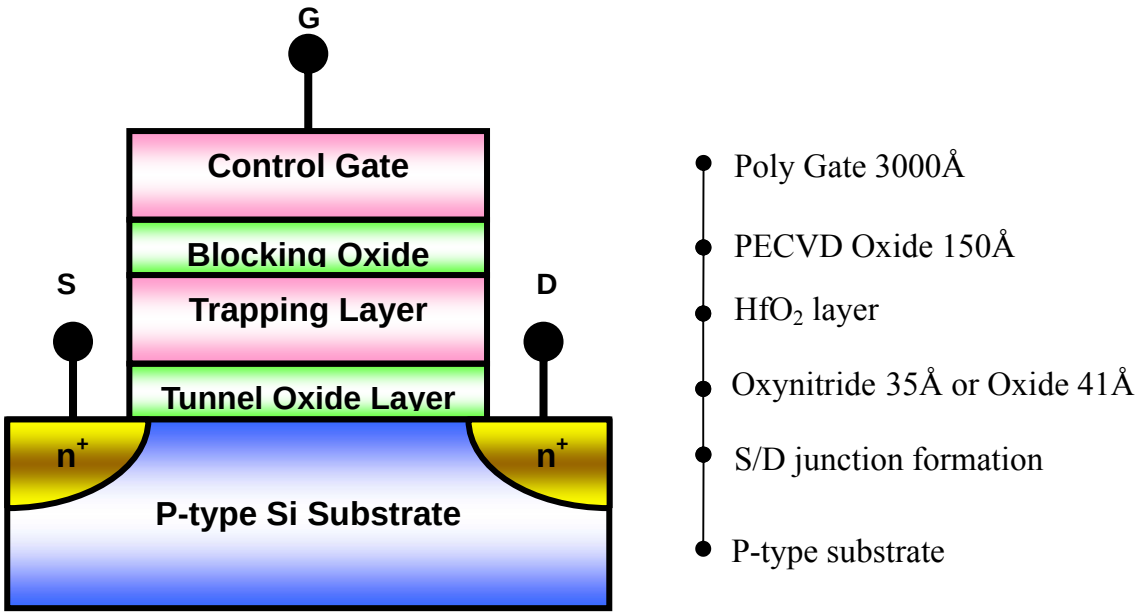
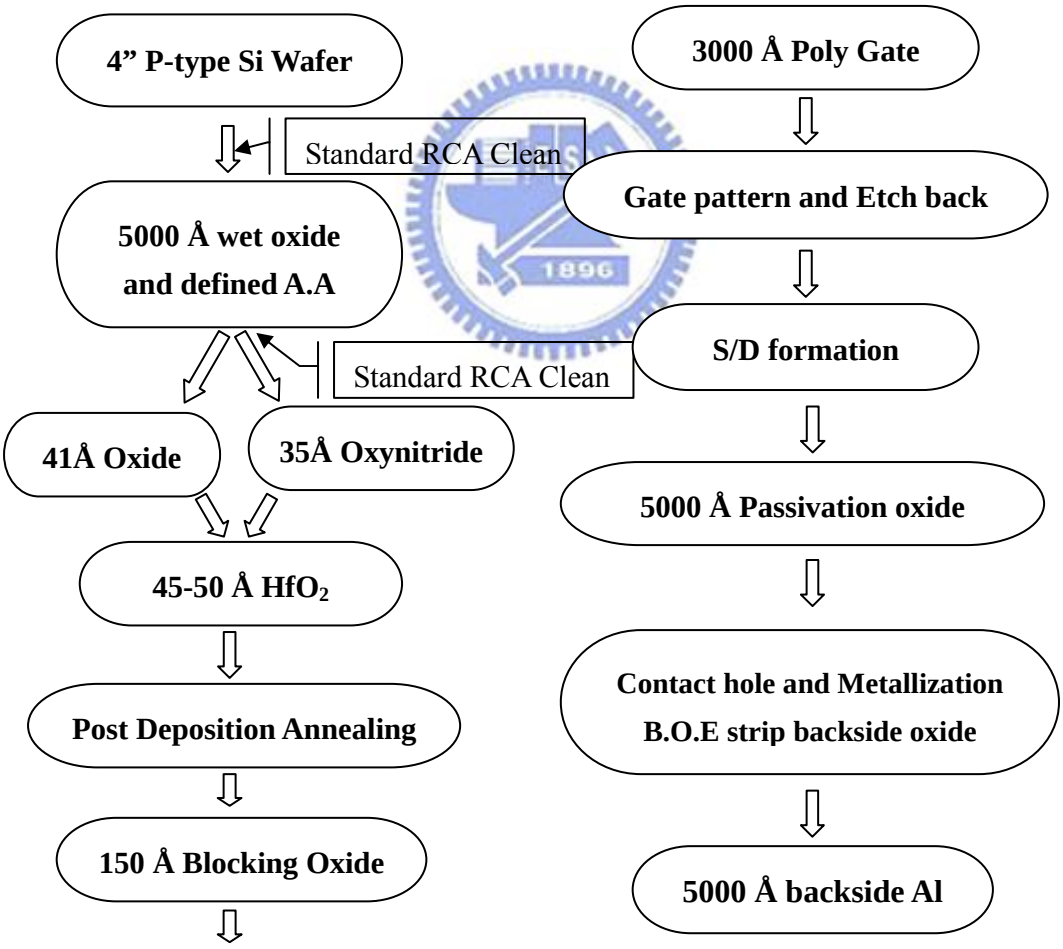


Fig. 3-2: SIMS profile of nitrogen distribution of 35Å oxynitride



(a)



(b)

Figure 3-3: (a)Schematic cross section of the HfO_2 SOHOS Device. (b) Process flows for fabricating HfO_2 SOHOS Device.

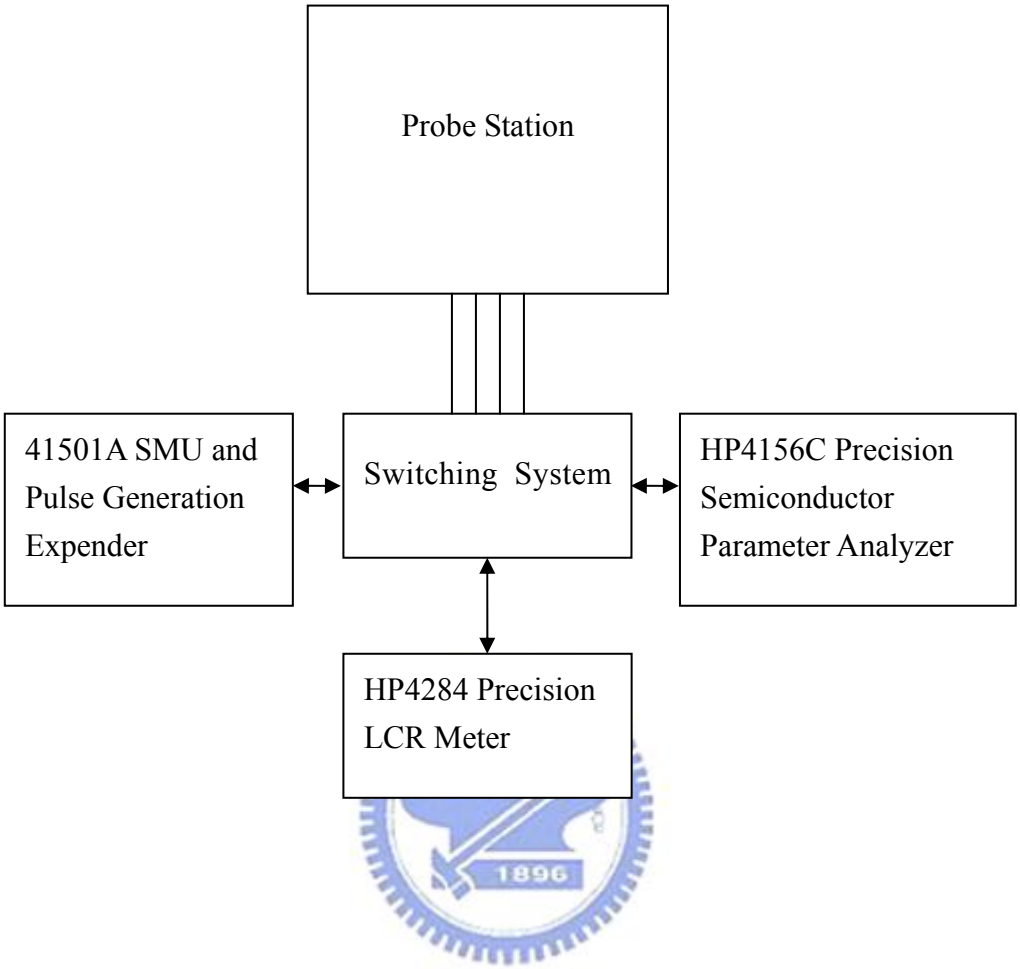
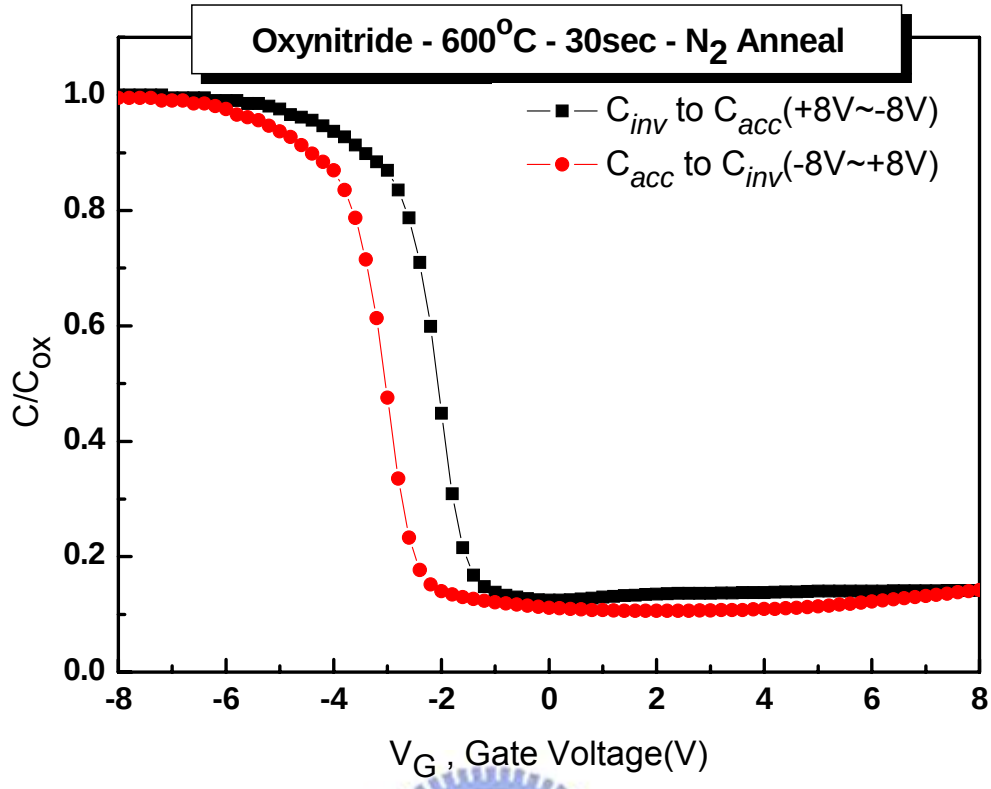
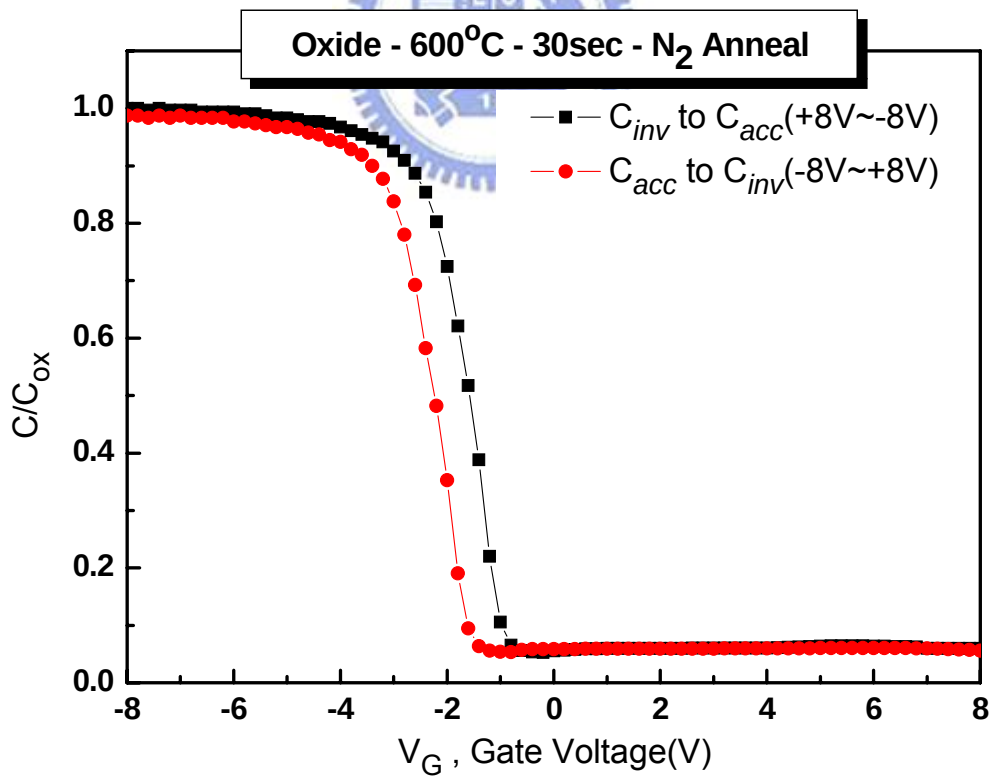


Figure 3-4: The construction of measurement system.

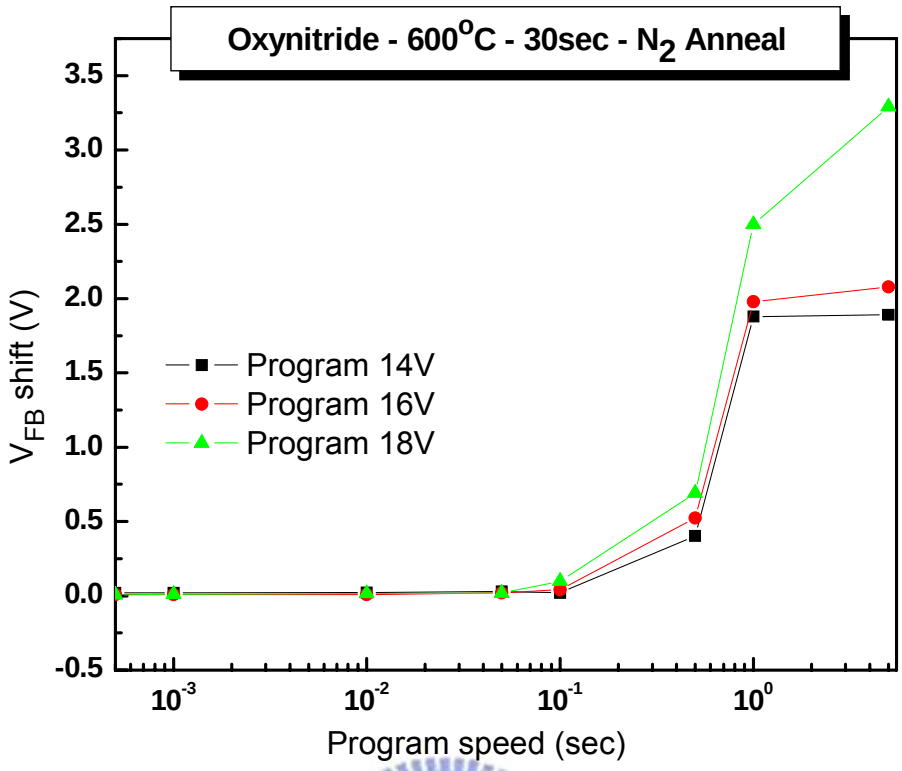


(a)

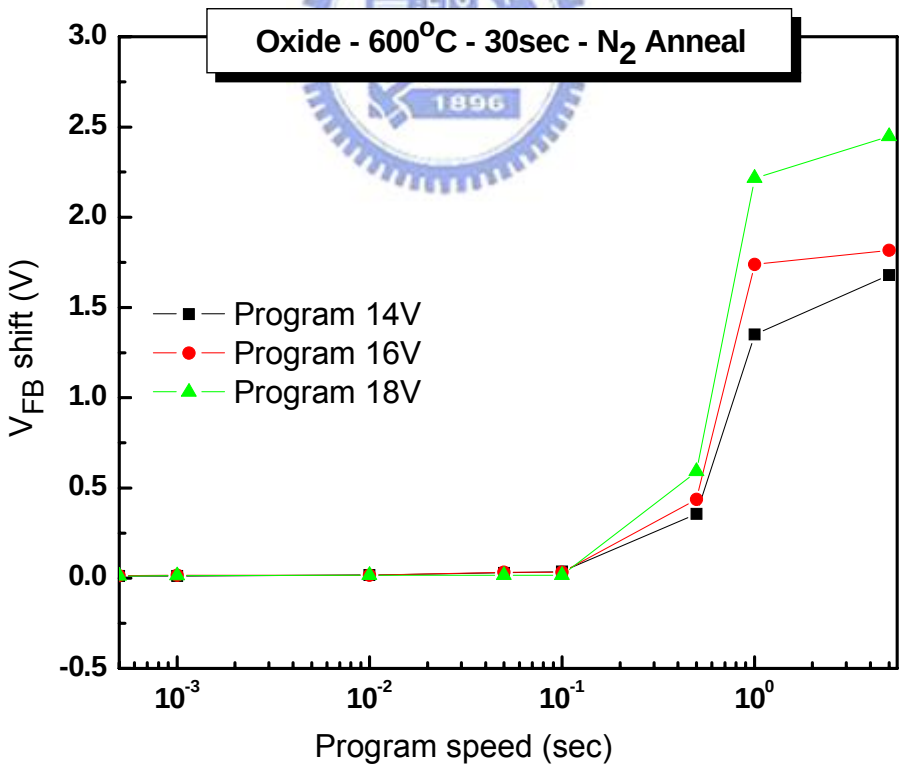


(b)

Fig 3-5: (a) The C-V hysteresis of the Cap-N6 after bidirectional sweeps (b) The C-V hysteresis of the Cap-O6 after bidirectional sweeps.

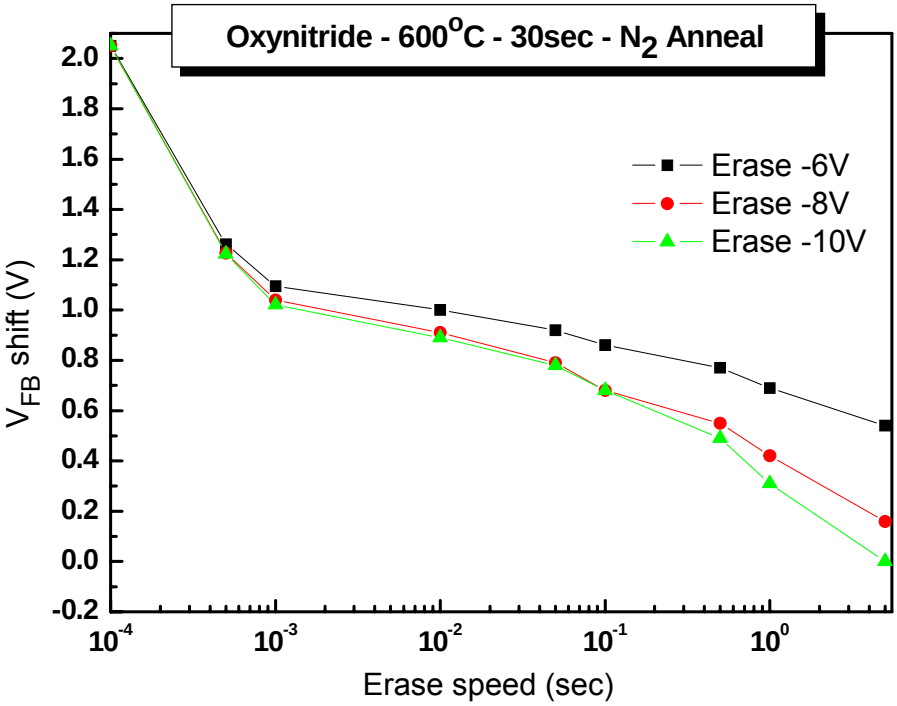


(a)

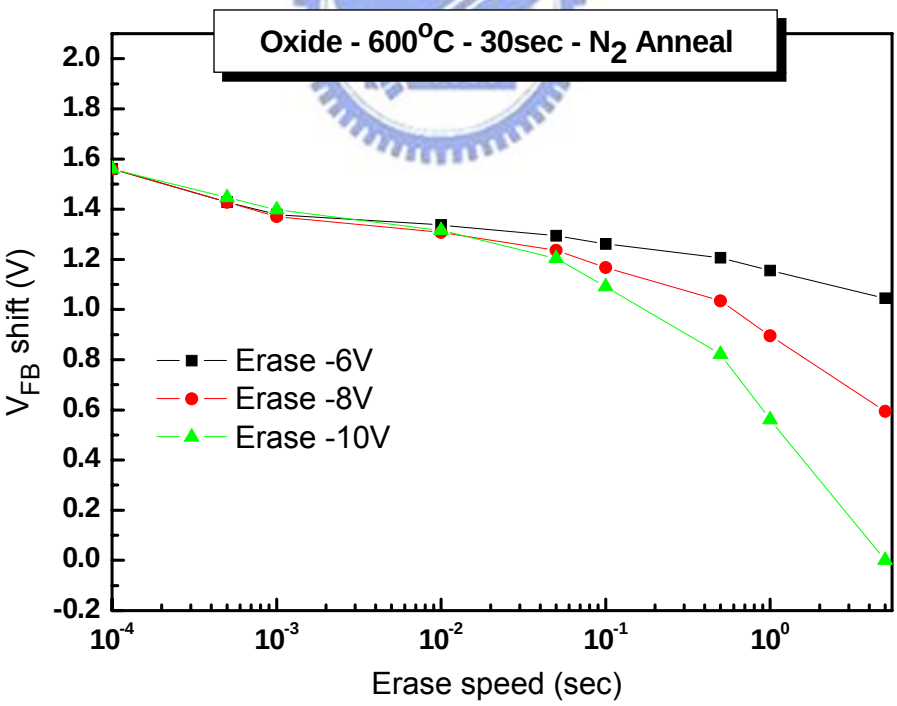


(b)

Fig 3-6: (a)Program characteristics of Cap-N6 with different operating condition (b)Program characteristics of Cap-O6 with different operating condition.

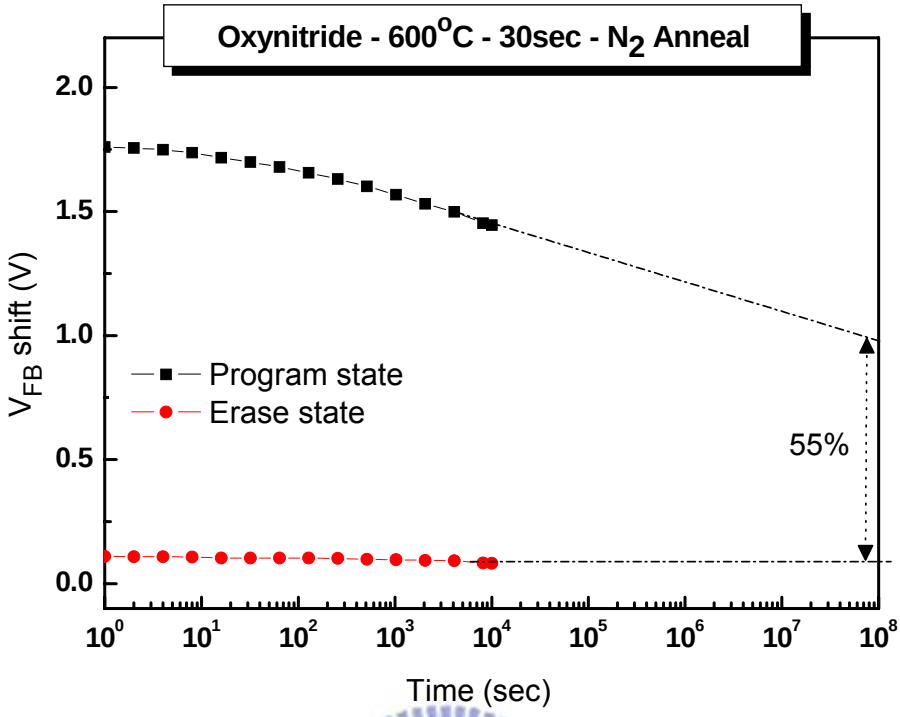


(a)

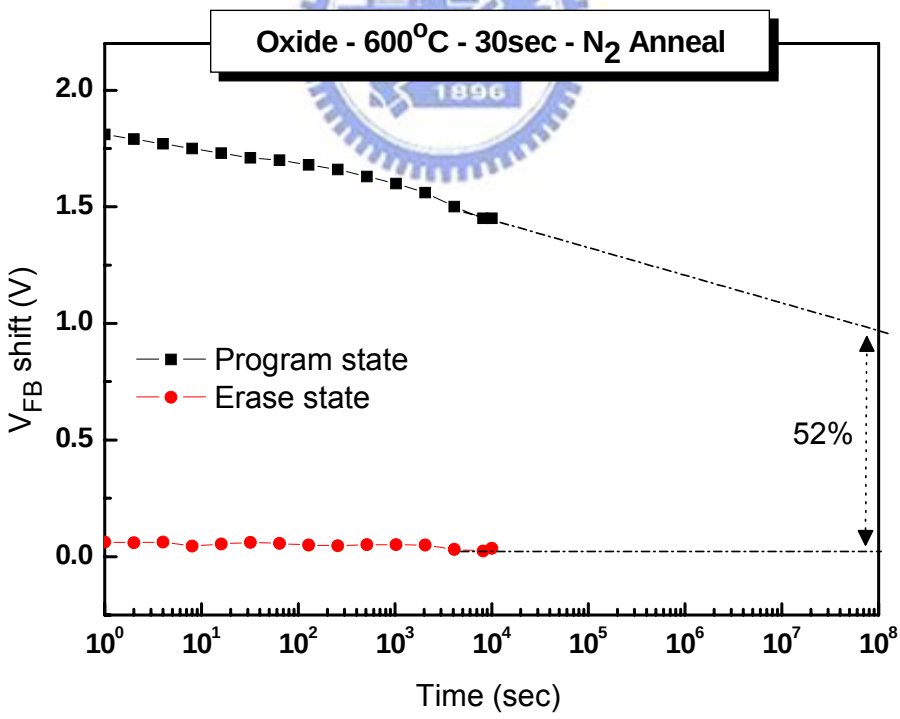


(b)

Fig 3-7: (a)Erase characteristics of Cap-N6 with different operating condition (b)Erase characteristics of Cap-O6 with different operating condition.

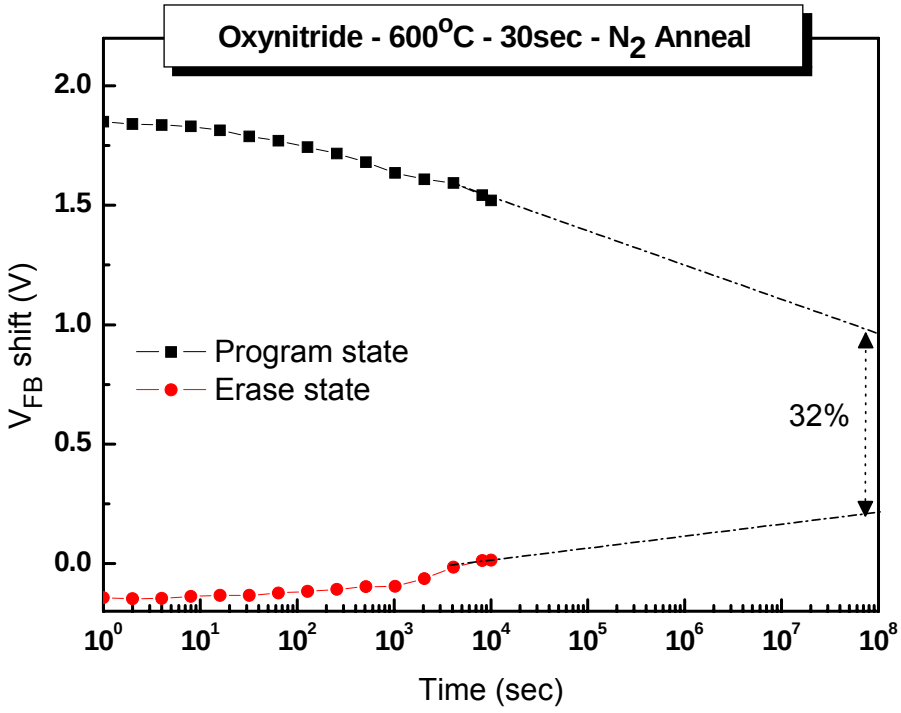


(a)

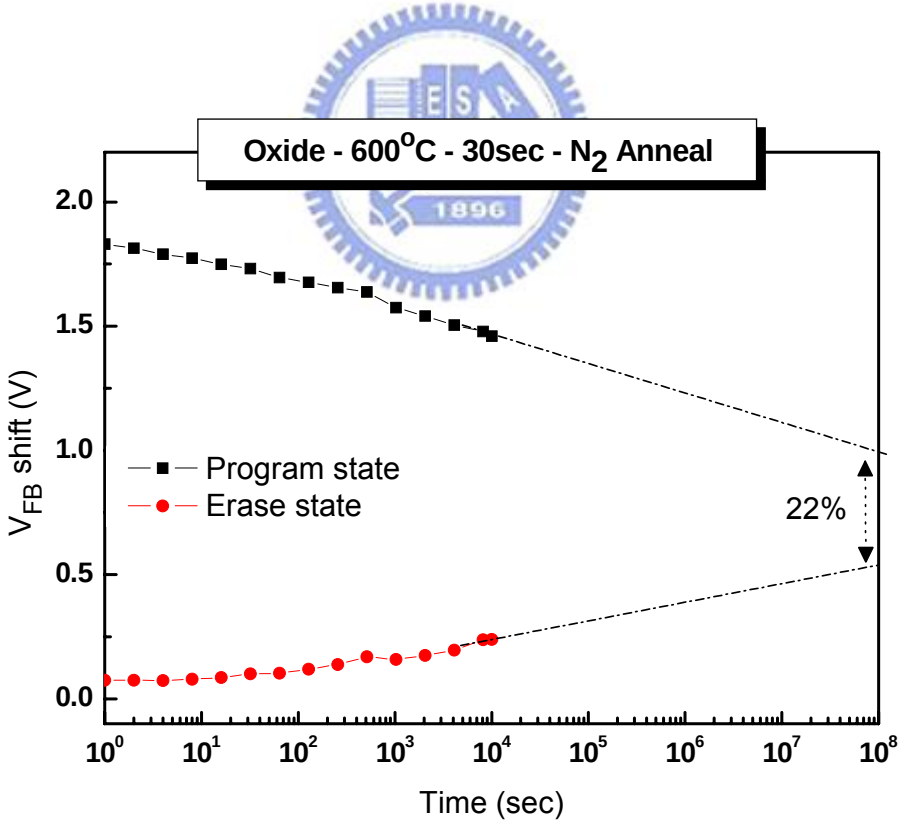


(b)

Fig 3-8: (a) The retention characteristics of Cap-N6 at room temperature
(b) The retention characteristics of Cap-O6 at room temperature.



(a)



(b)

Fig 3-9: (a) The retention characteristics of Cap-N6 after 10^5 cycles
(b) The retention characteristics of Cap-O6 after 10^5 cycles.

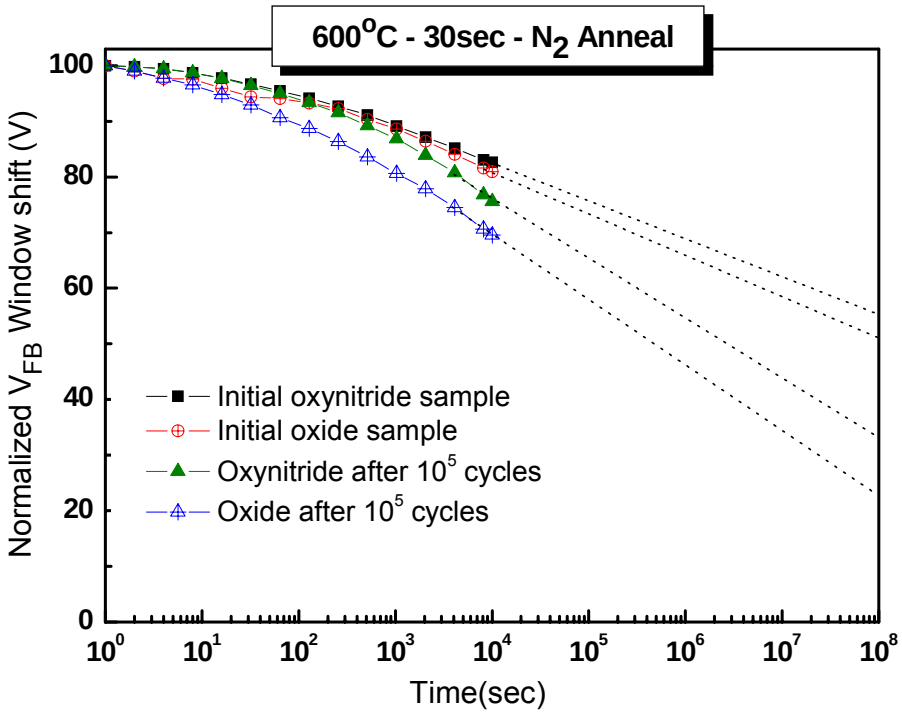


Fig 3-10: The compared retention characteristics of initial Cap-N6, Cap-O6 and after 10^5 cycles.

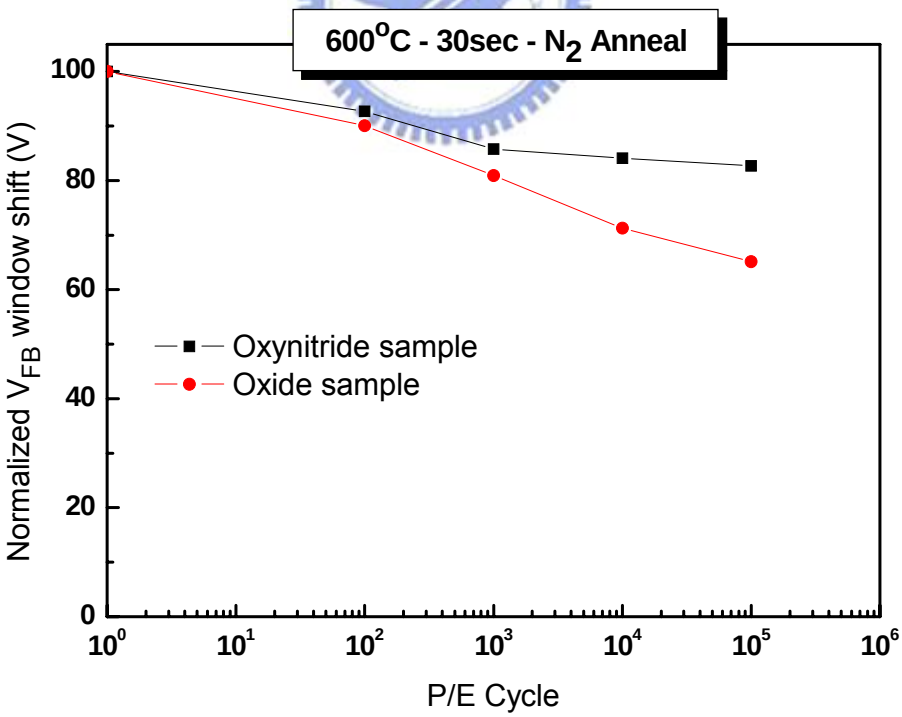
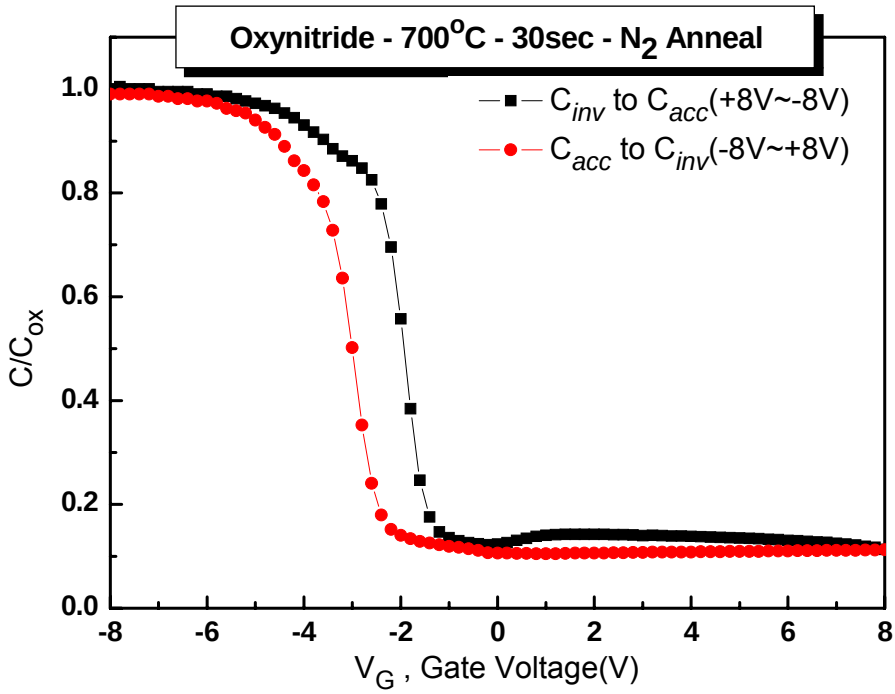
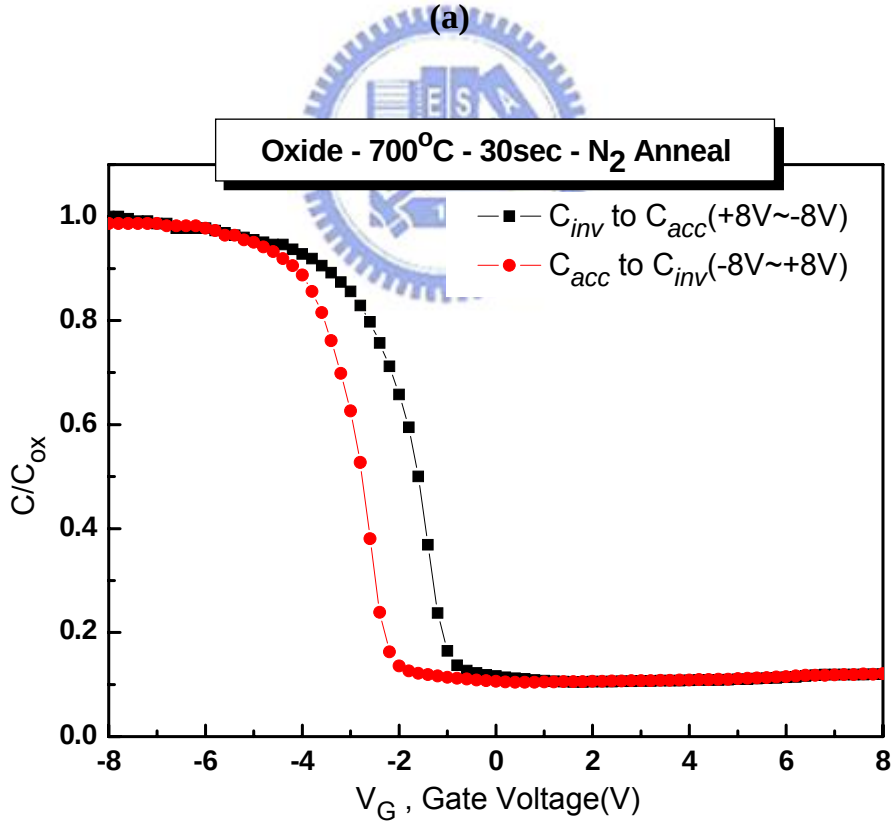


Fig 3-11: The endurance characteristics of Cap-N6 and Cap-O6.

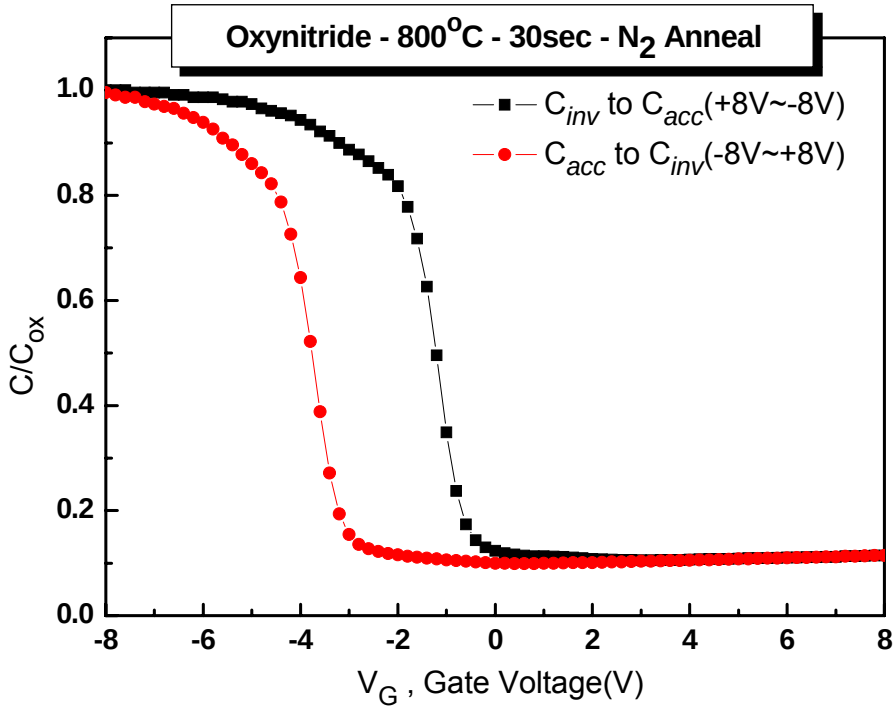


(a)

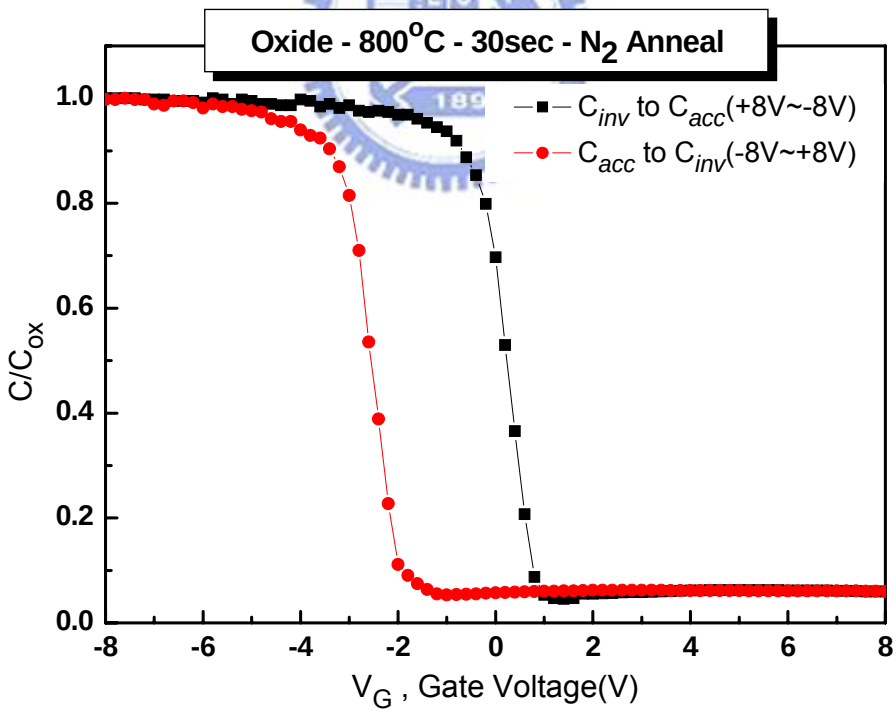


(b)

Fig 3-12: (a) The C-V hysteresis of the Cap-N7 after bidirectional sweeps (b) The C-V hysteresis of the Cap-O7 after bidirectional sweeps.

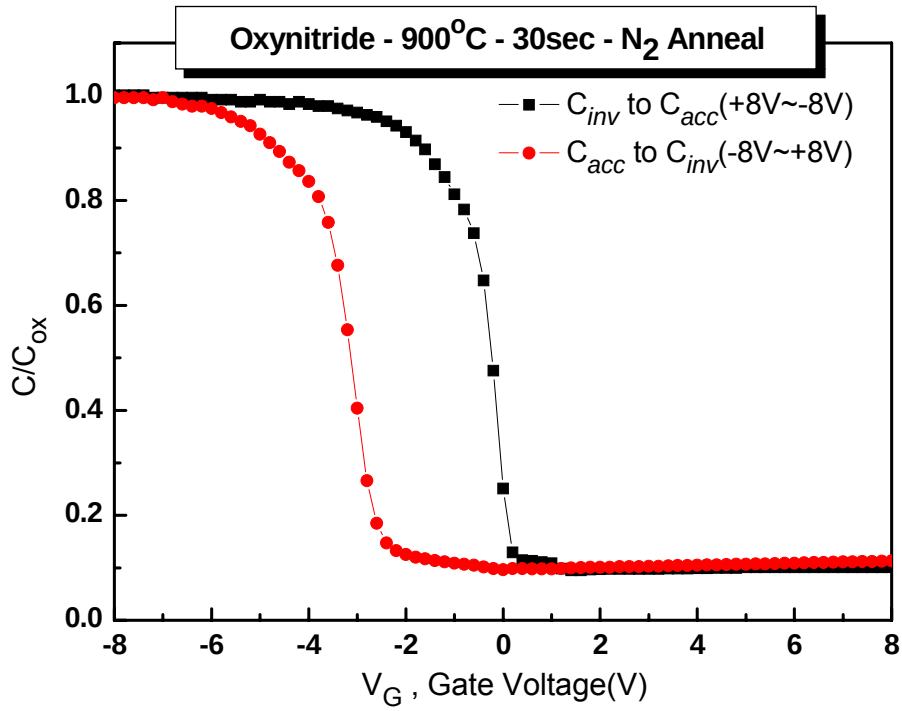


(a)

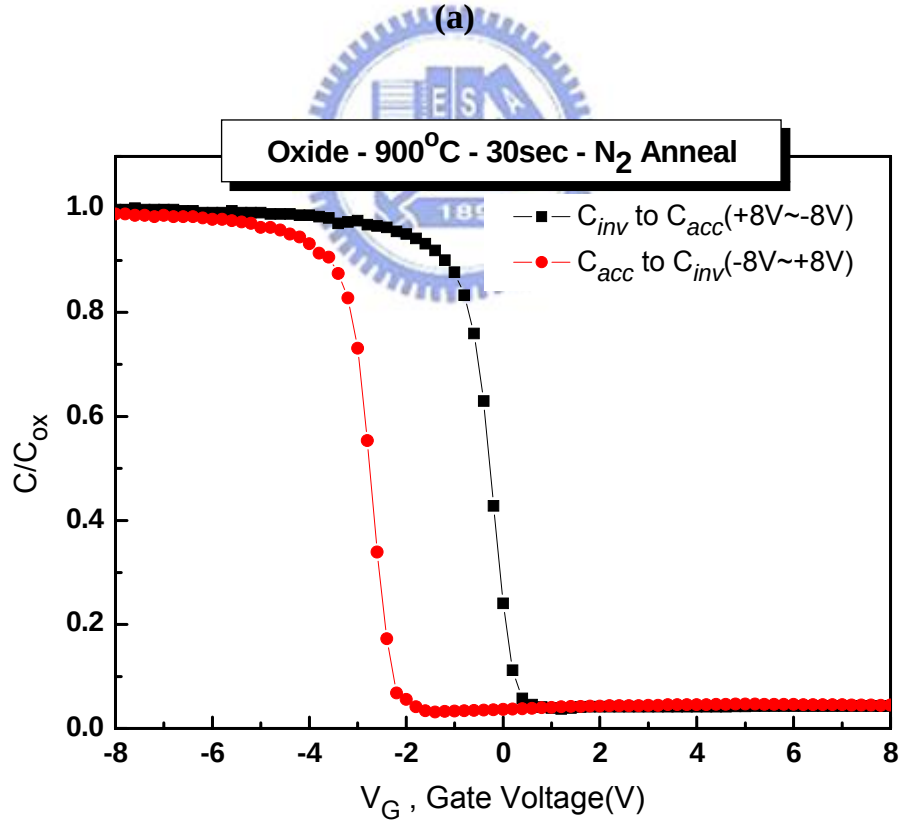


(b)

Fig 3-13: (a) The C-V hysteresis of the Cap-N8 after bidirectional sweeps (b) The C-V hysteresis of the Cap-O8 after bidirectional sweeps.

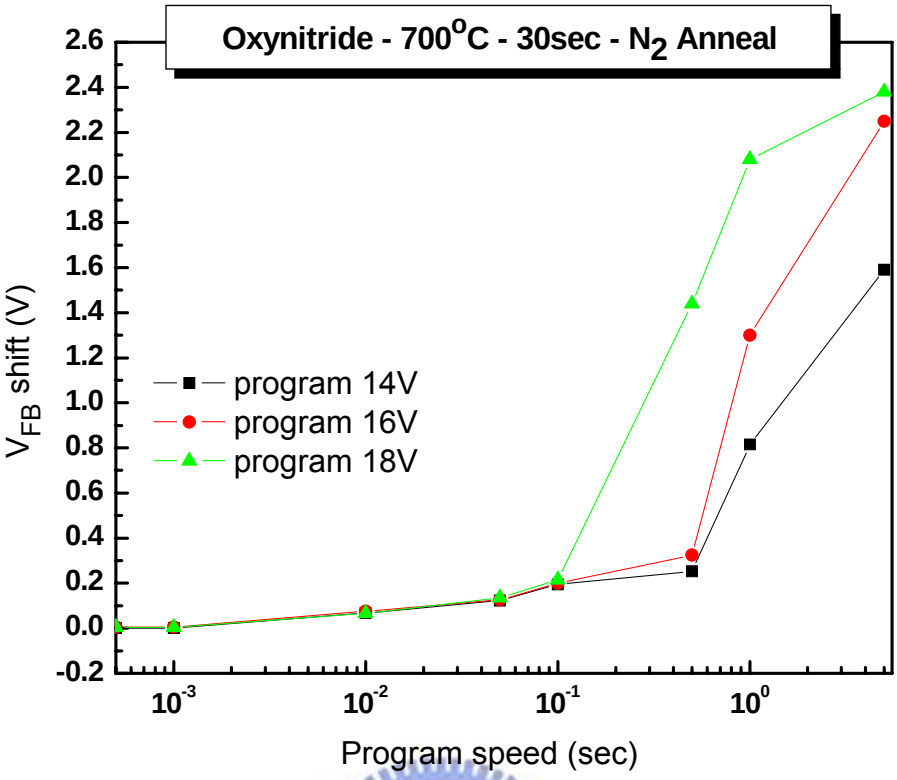


(a)

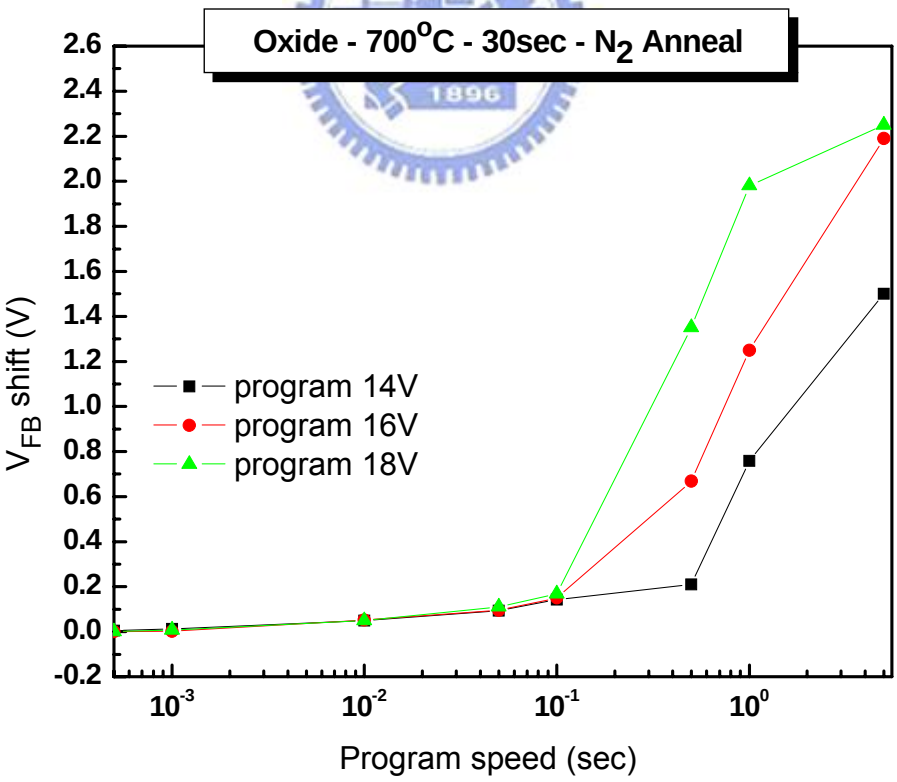


(b)

Fig 3-14: (a) The C-V hysteresis of the Cap-N9 after bidirectional sweeps (b) The C-V hysteresis of the Cap-O9 after bidirectional sweeps.

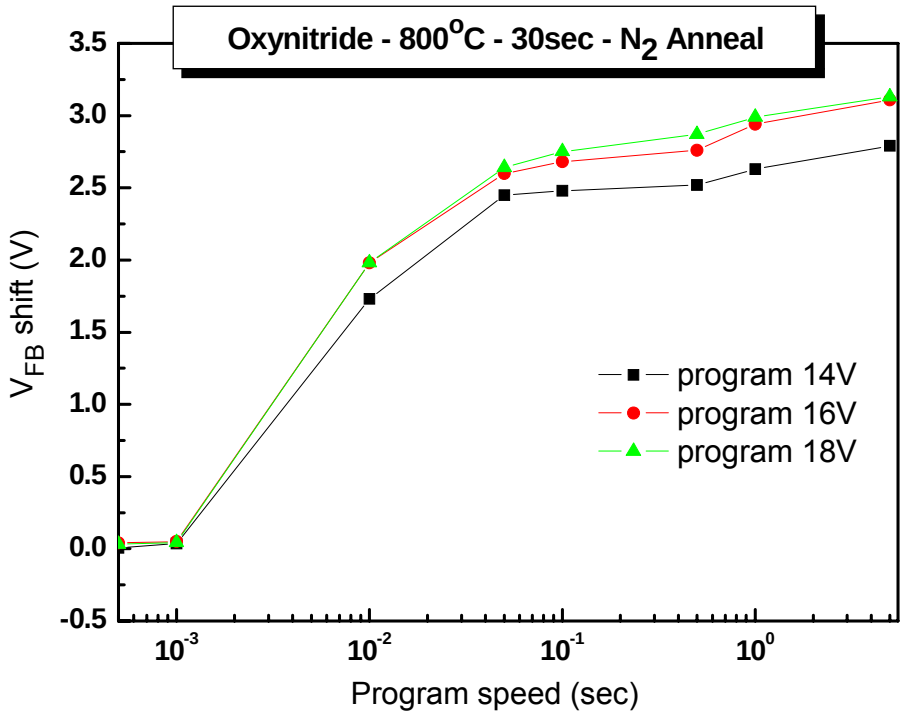


(a)

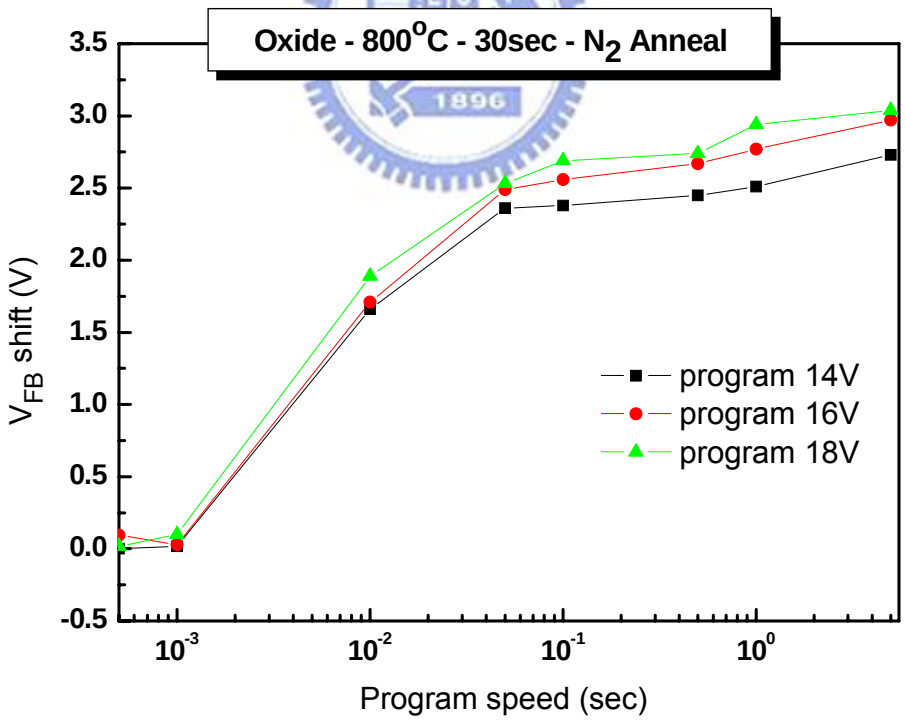


(b)

Fig 3-15: (a)Program characteristics of Cap-N7 with different operating condition (b)Program characteristics of Cap-O7 with different operating condition.

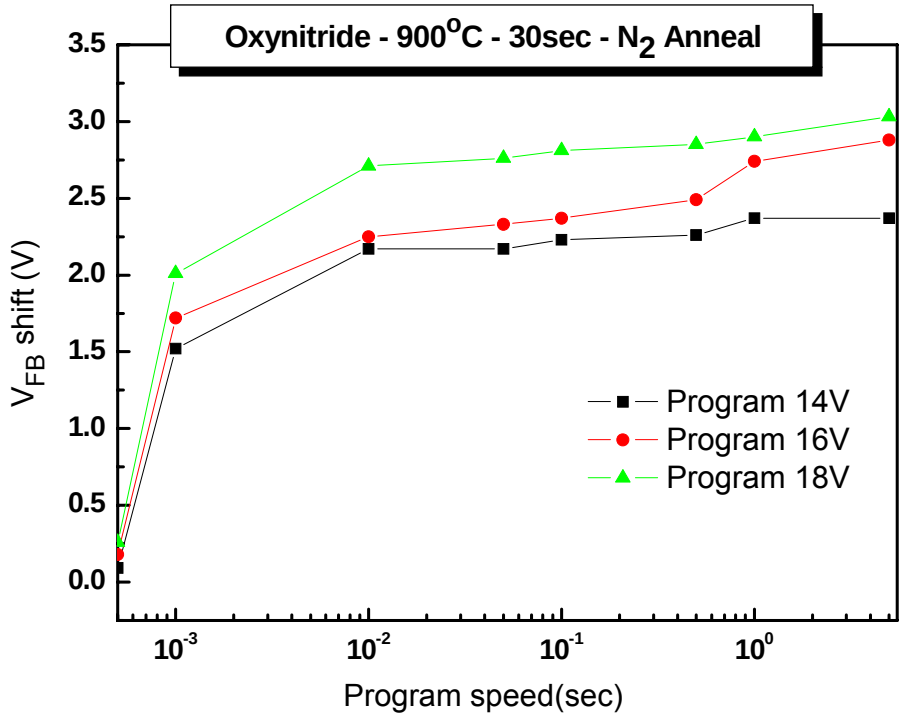


(a)

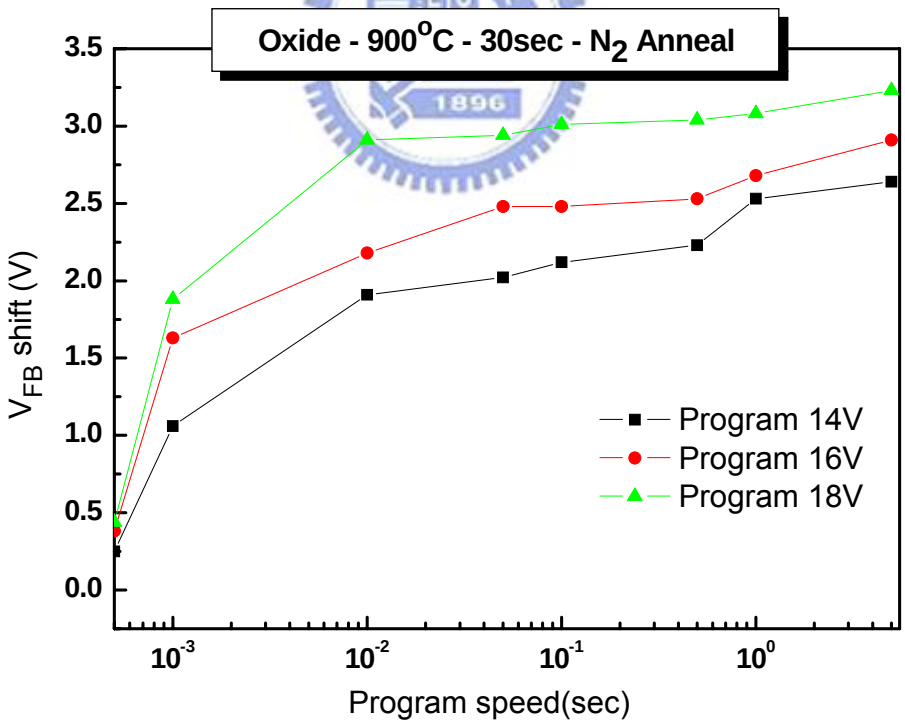


(b)

Fig 3-16: (a)Program characteristics of Cap-N8 with different operating condition (b)Program characteristics of Cap-O8 with different operating condition.

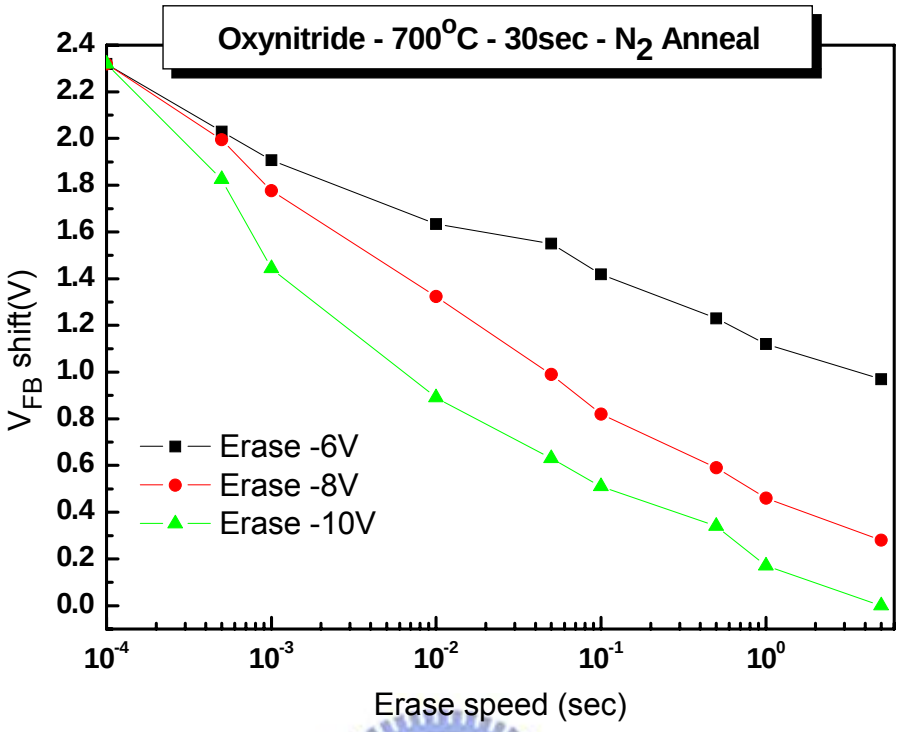


(a)

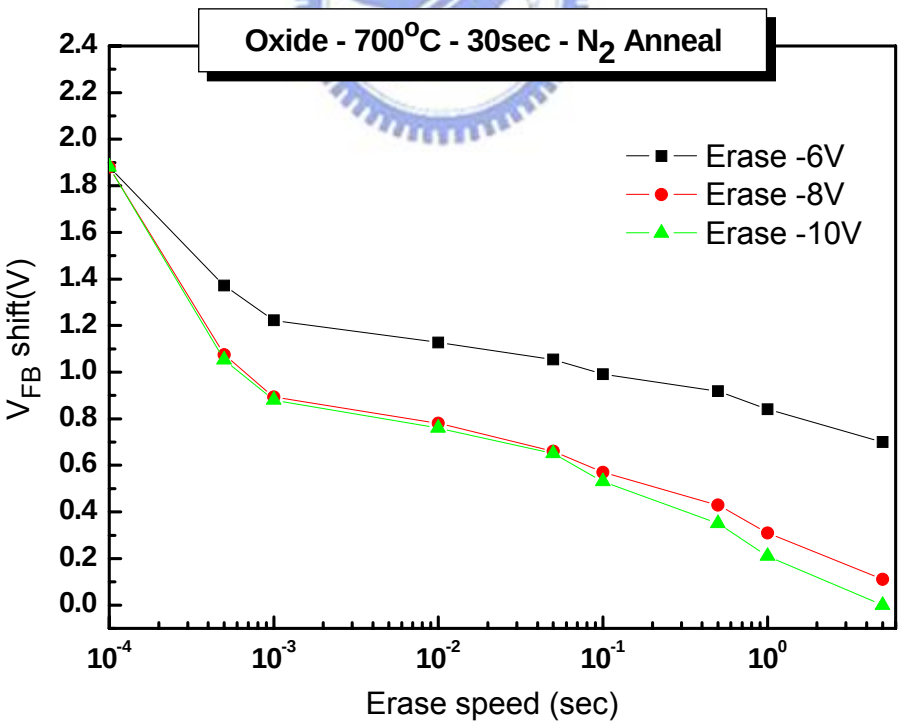


(b)

Fig 3-17: (a)Program characteristics of Cap-N9 with different operating condition (b)Program characteristics of Cap-O9 with different operating condition.

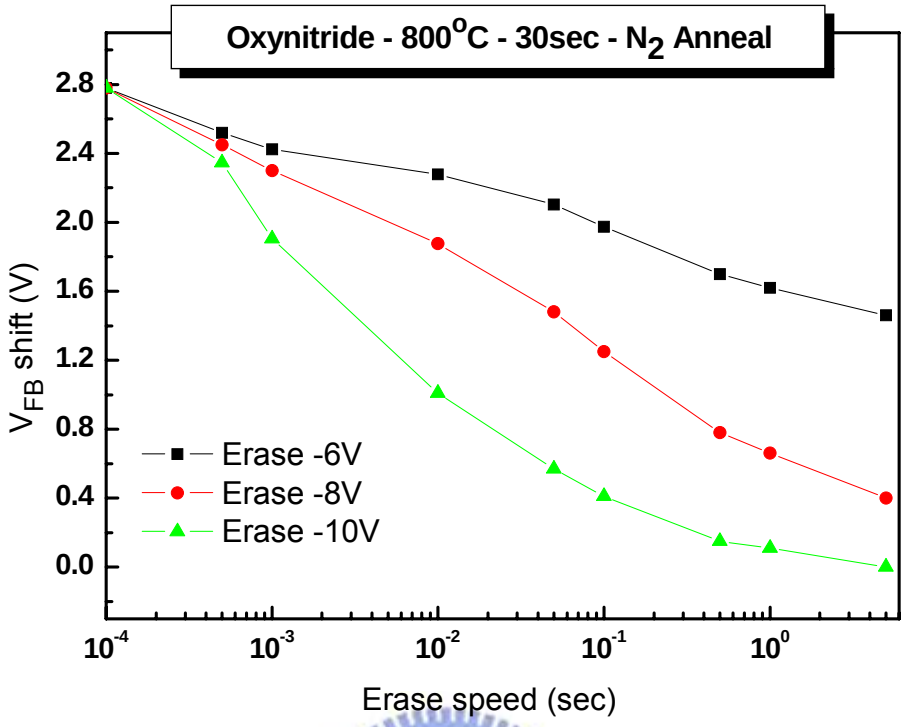


(a)

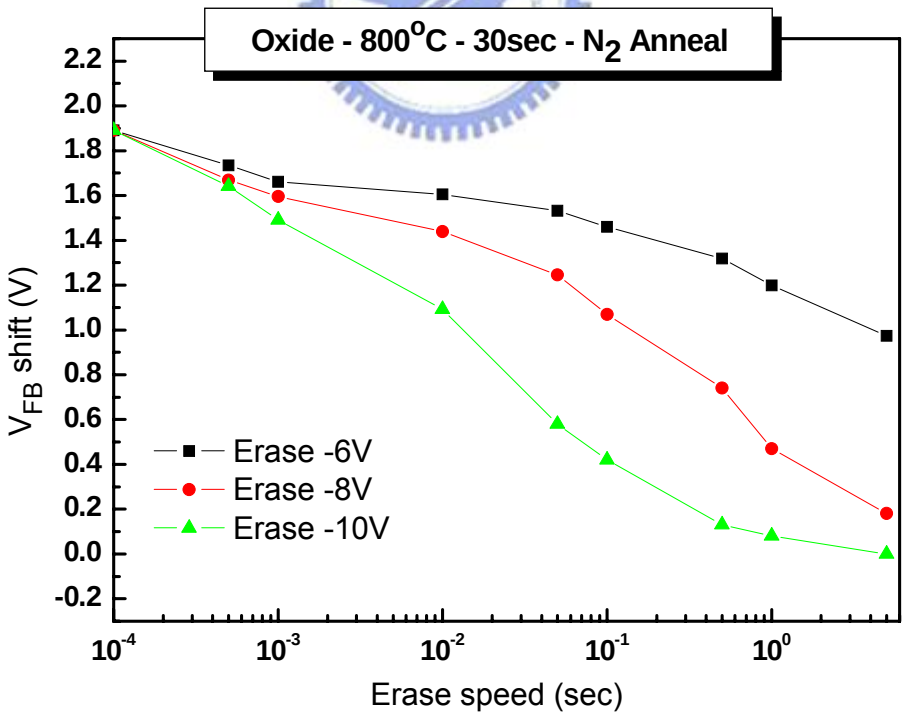


(b)

Fig 3-18: (a)Erase characteristics of Cap-N7 with different operating condition (b)Erase characteristics of Cap-O7 with different operating condition.

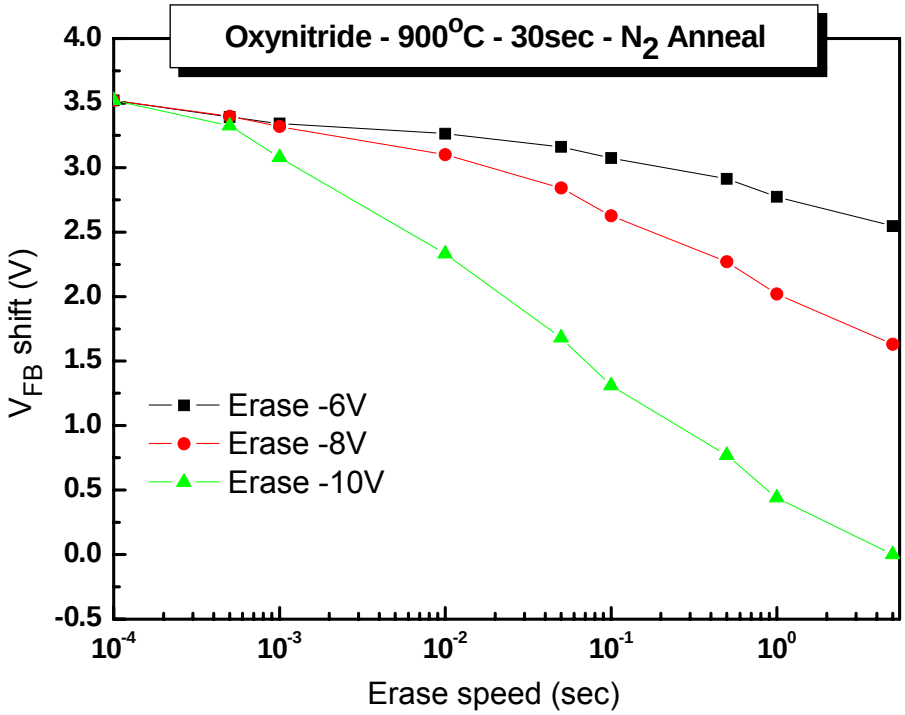


(a)

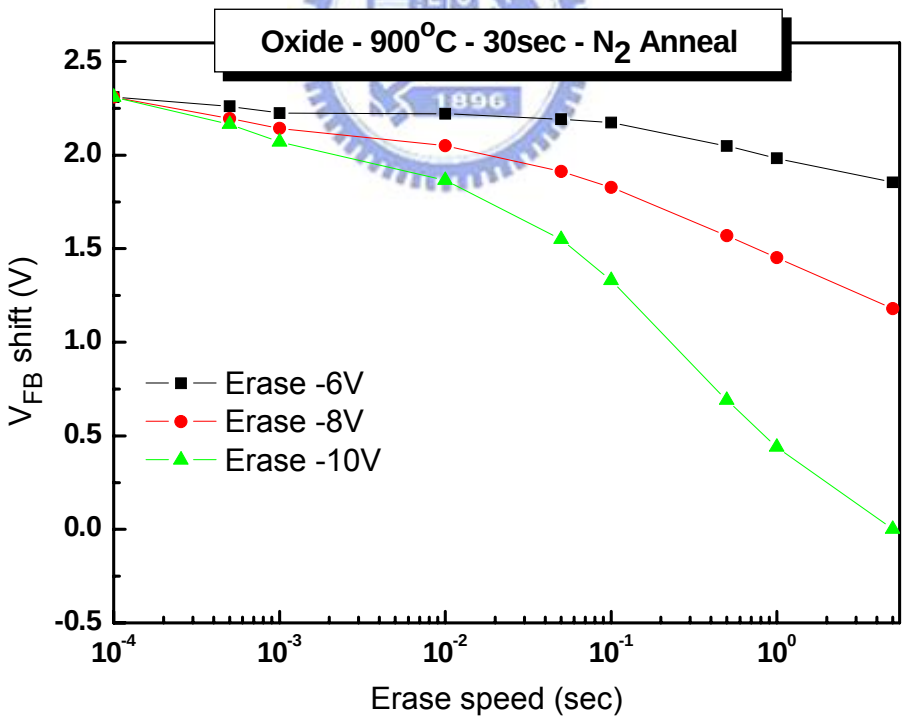


(b)

Fig 3-19: (a)Erase characteristics of Cap-N8 with different operating condition (b)Erase characteristics of Cap-O8 with different operating condition.

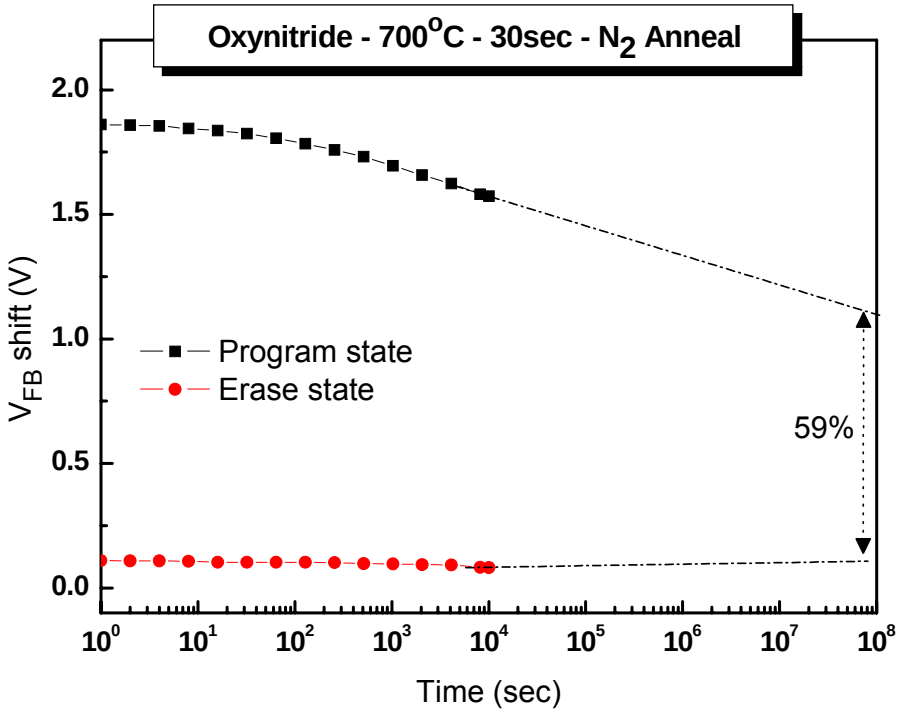


(a)

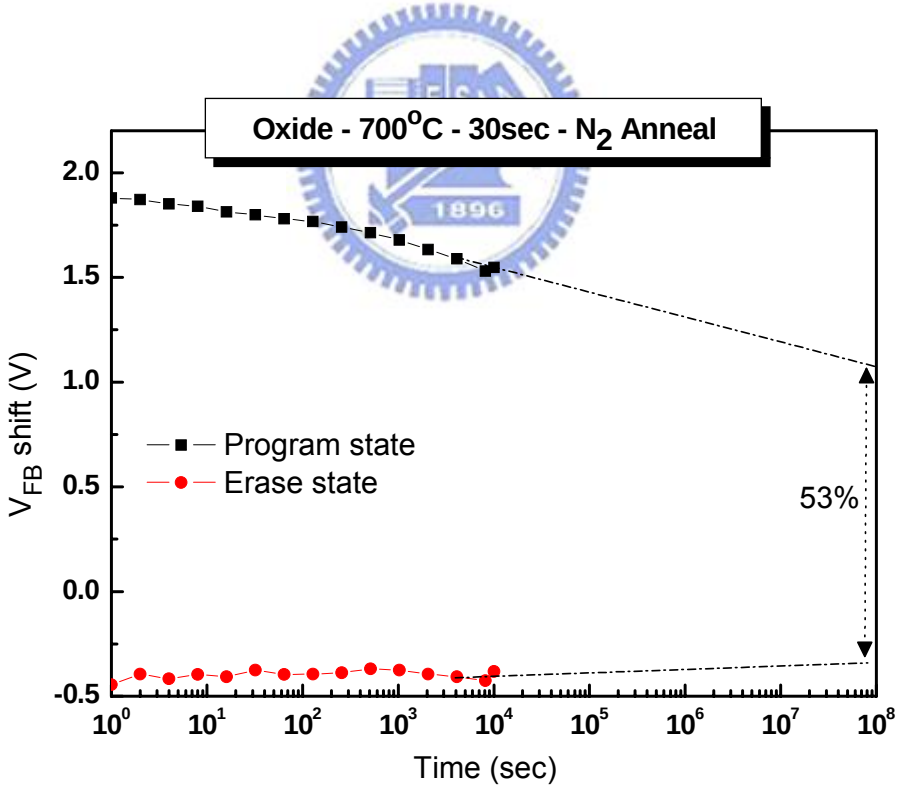


(b)

Fig 3-20: (a)Erase characteristics of Cap-N9 with different operating condition (b)Erase characteristics of Cap-O9 with different operating condition.

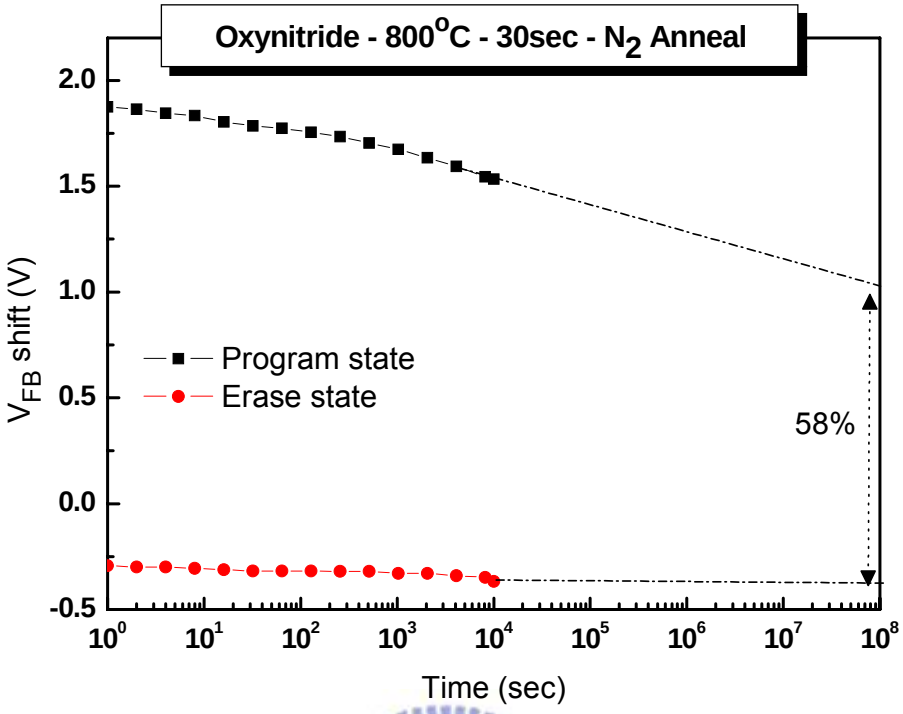


(a)

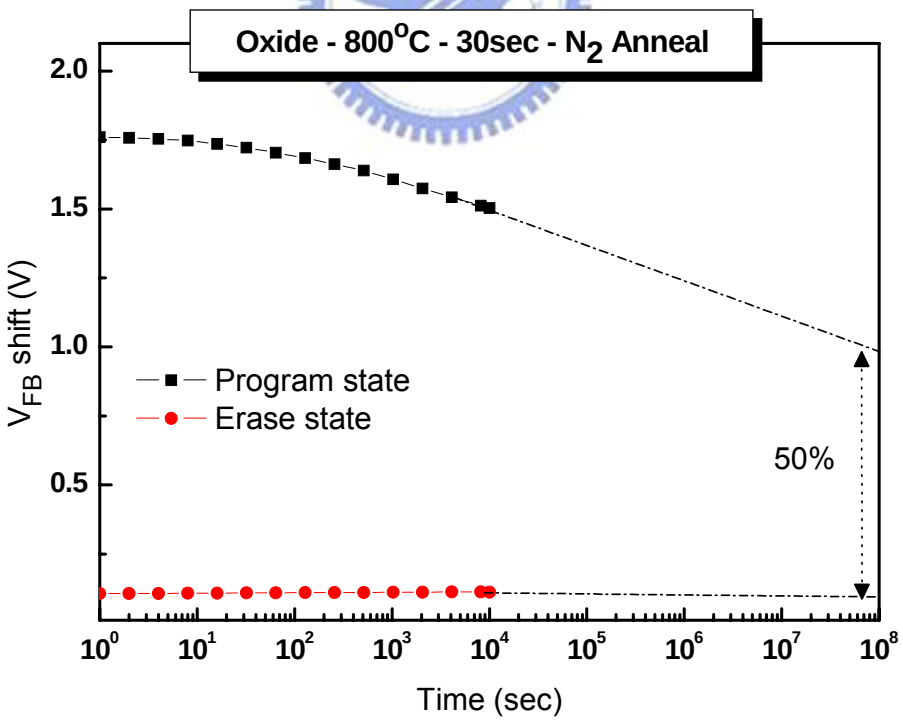


(b)

Fig 3-21: (a) The retention characteristics of Cap-N7 at room temperature (b) The retention characteristics of Cap-O7 at room temperature.

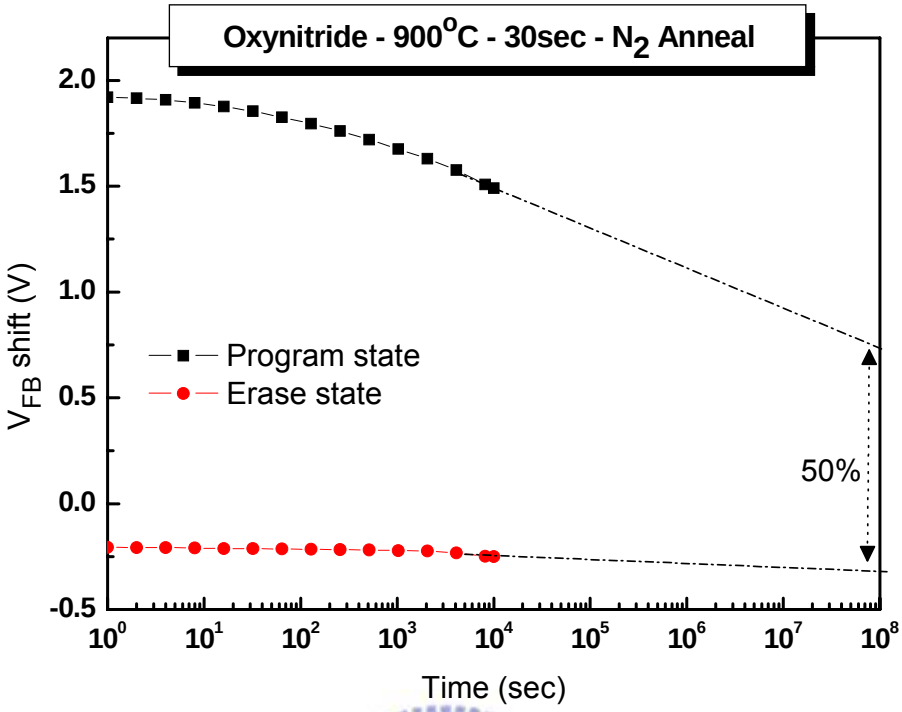


(a)

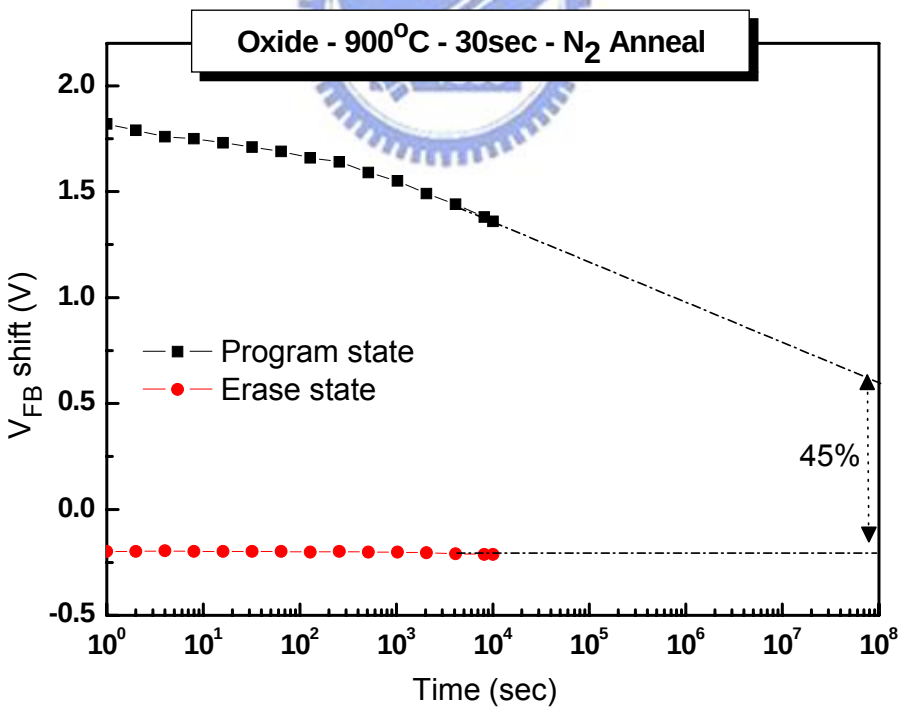


(a)

Fig 3-22: (a) The retention characteristics of Cap-N8 at room temperature
(b) The retention characteristics of Cap-O8 at room temperature.

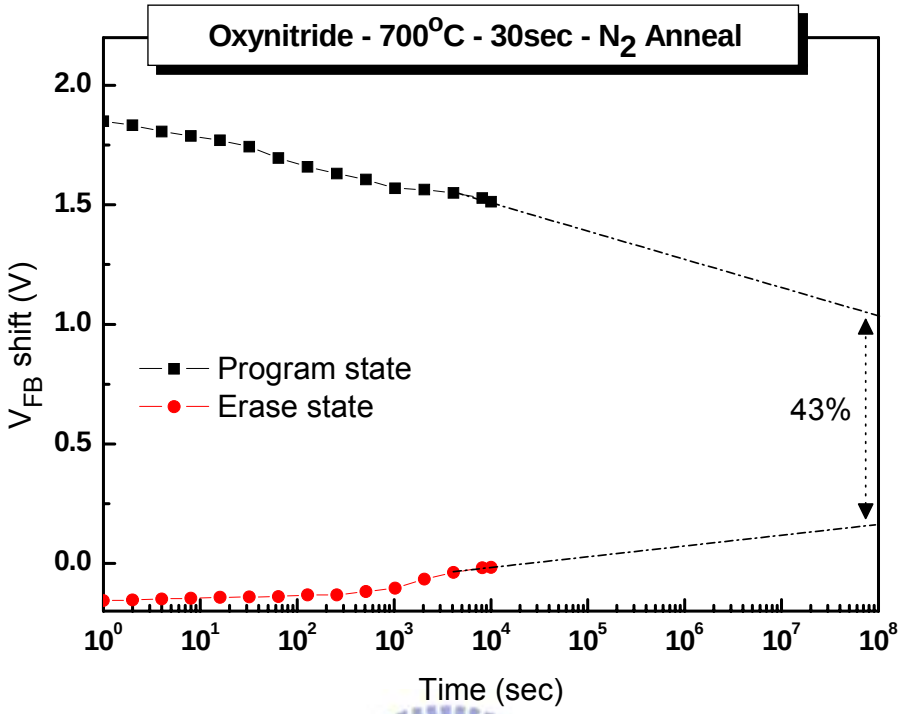


(a)

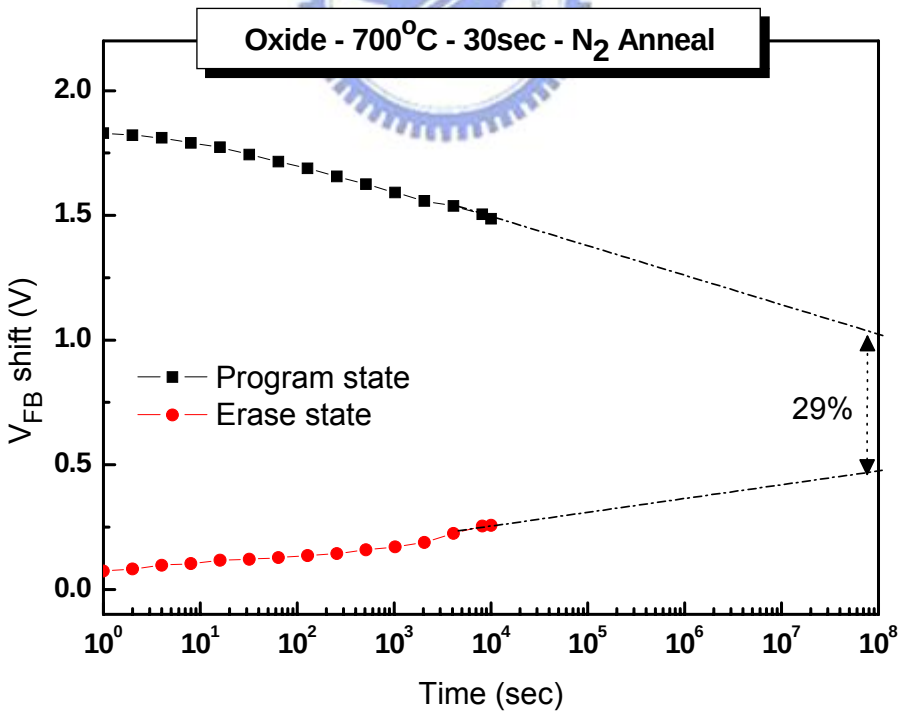


(b)

Fig 3-23: (a) The retention characteristics of Cap-N9 at room temperature
(b) The retention characteristics of Cap-O9 at room temperature.

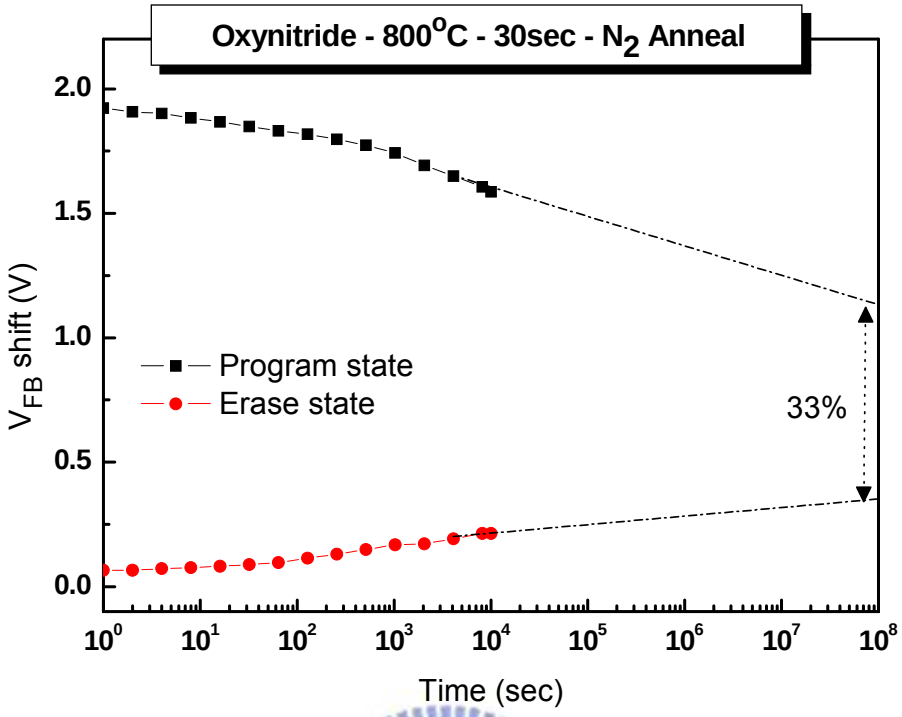


(a)

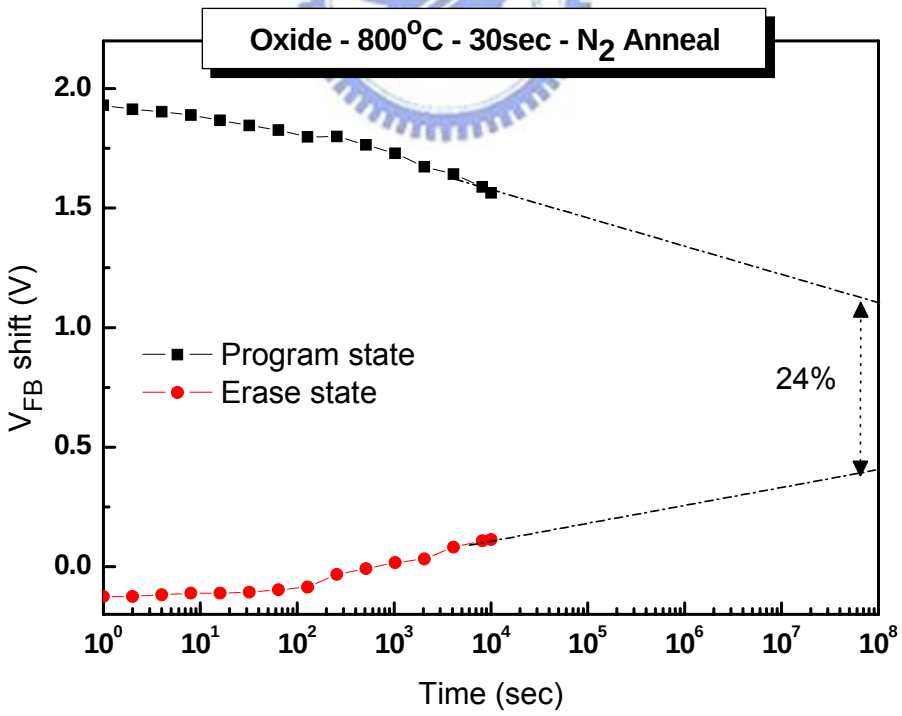


(b)

Fig 3-24: (a) The retention characteristics of Cap-N7 after 10^5 cycles (b) The retention characteristics of Cap-O7 after 10^5 cycles.

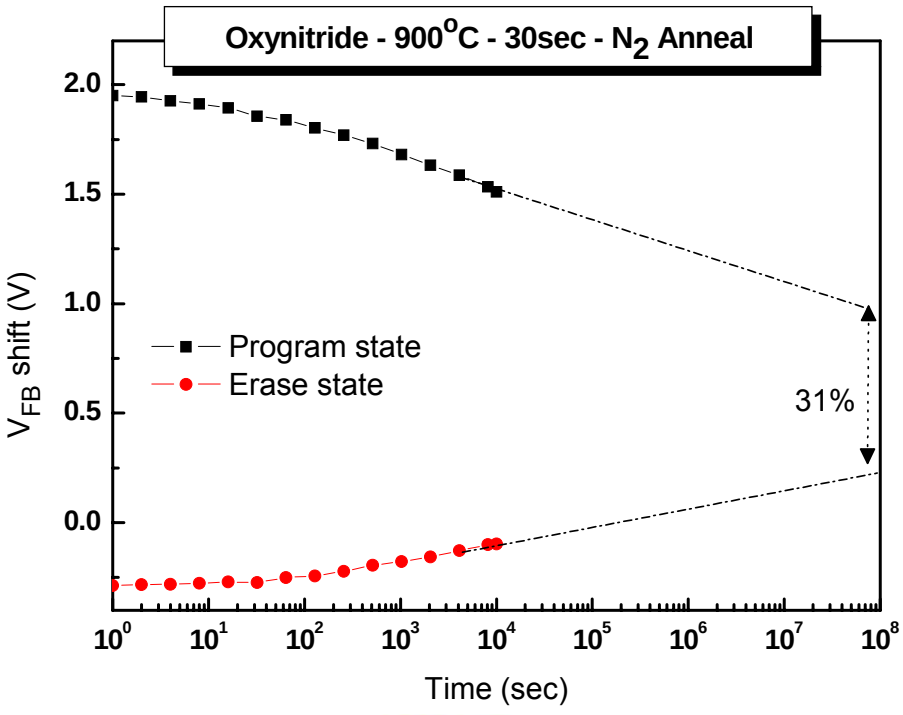


(a)

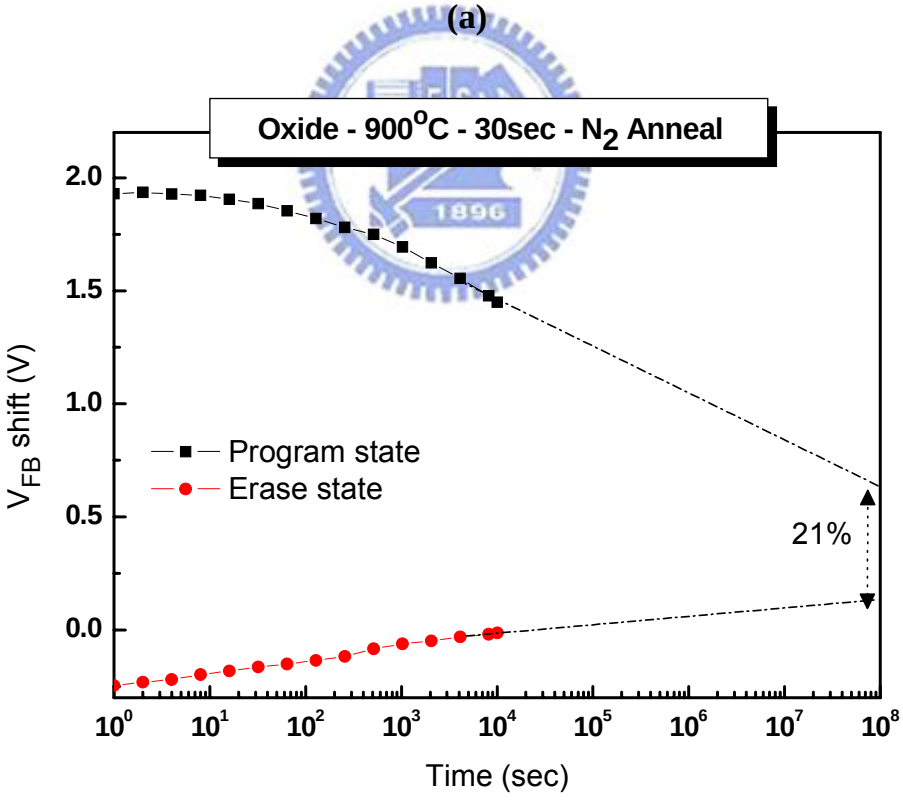


(b)

Fig 3-25: (a) The retention characteristics of Cap-N8 after 10^5 cycles (b) The retention characteristics of Cap-O8 after 10^5 cycles.



(a)



(b)

Fig 3-26: (a) The retention characteristics of Cap-N9 after 10^5 cycles (b) The retention characteristics of Cap-O9 after 10^5 cycles.

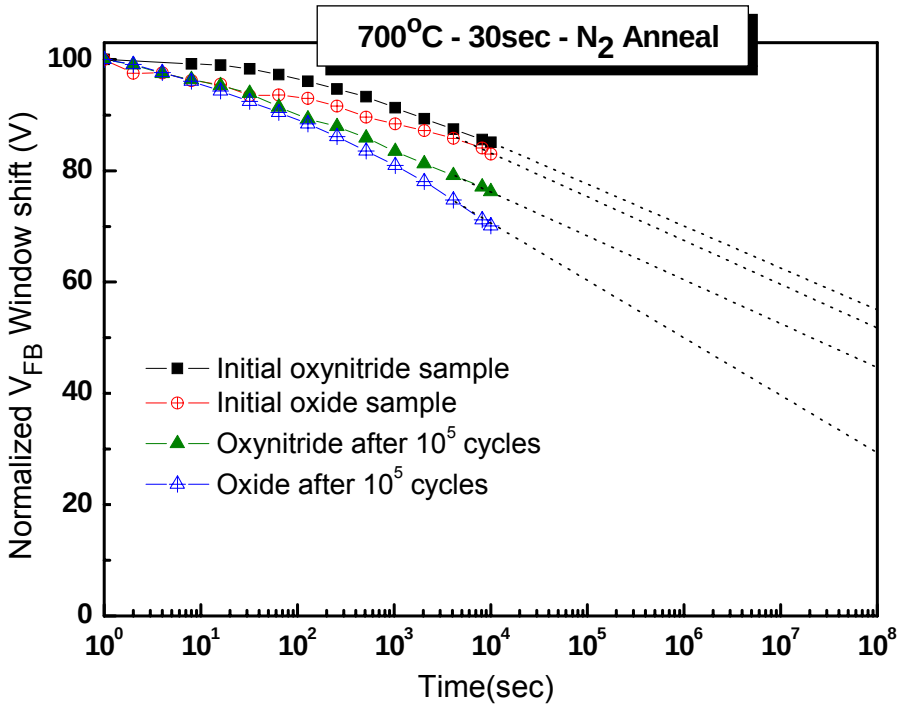


Fig 3-27: The compared retention characteristics of initial Cap-N7, Cap-O7 and after 10^5 cycles.

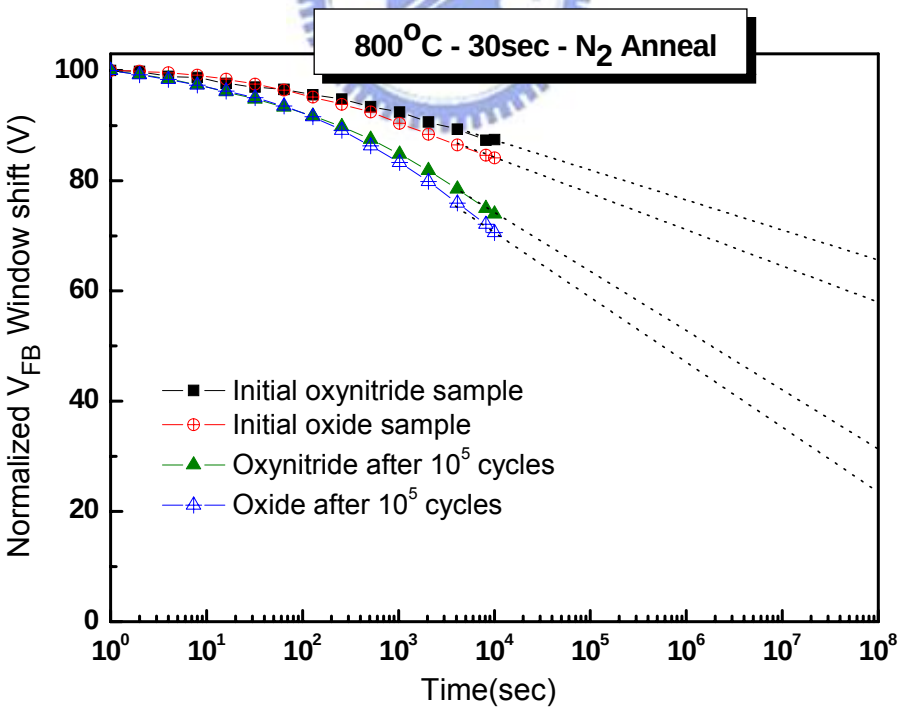


Fig 3-28: The compared retention characteristics of initial Cap-N8, Cap-O8 and after 10^5 cycles.

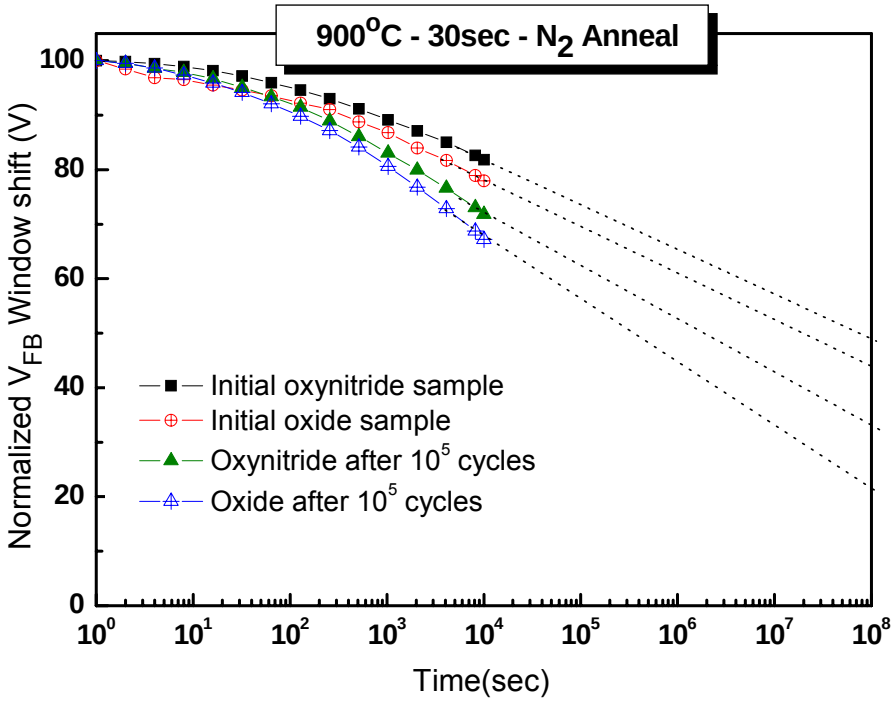


Fig 3-29: The compared retention characteristics of initial Cap-N9, Cap-O9 and after 10^5 cycles.

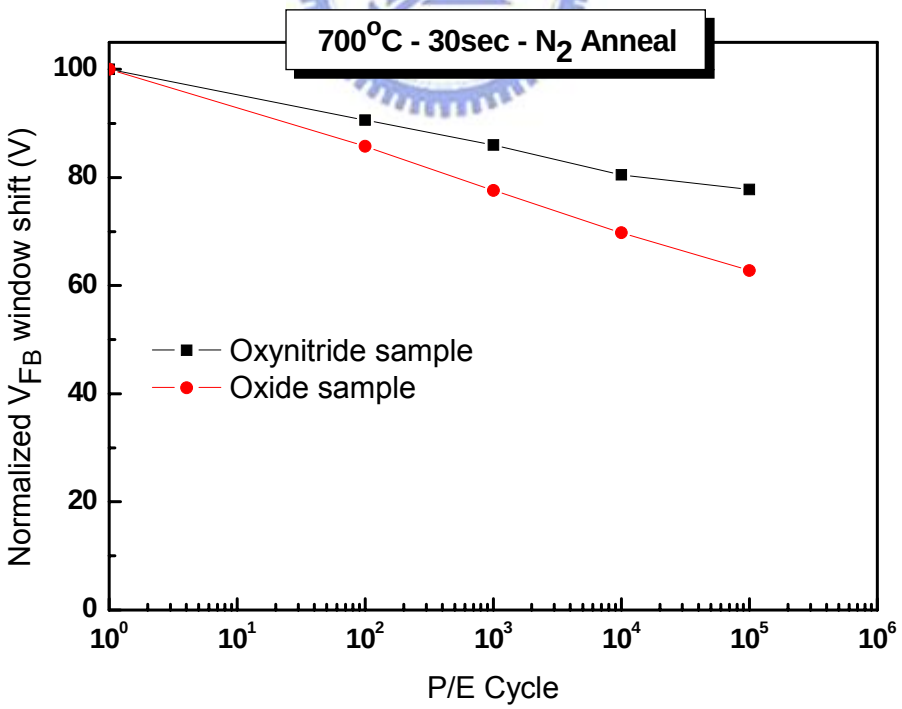


Fig 3-30: The endurance characteristics of Cap-N7 and Cap-O7.

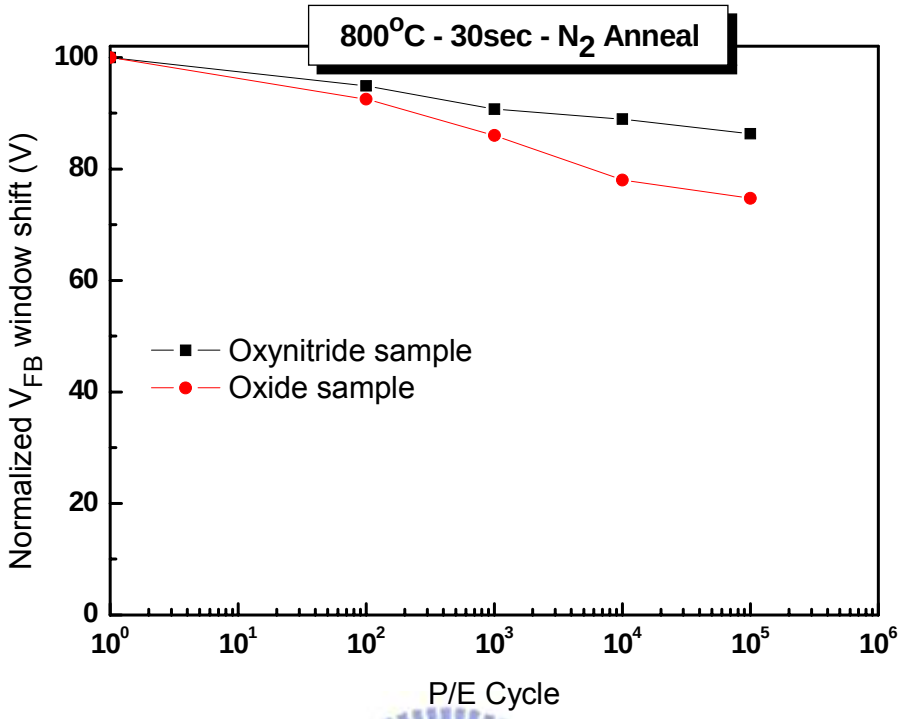


Fig 3-31: The endurance characteristics of Cap-N8 and Cap-O8.

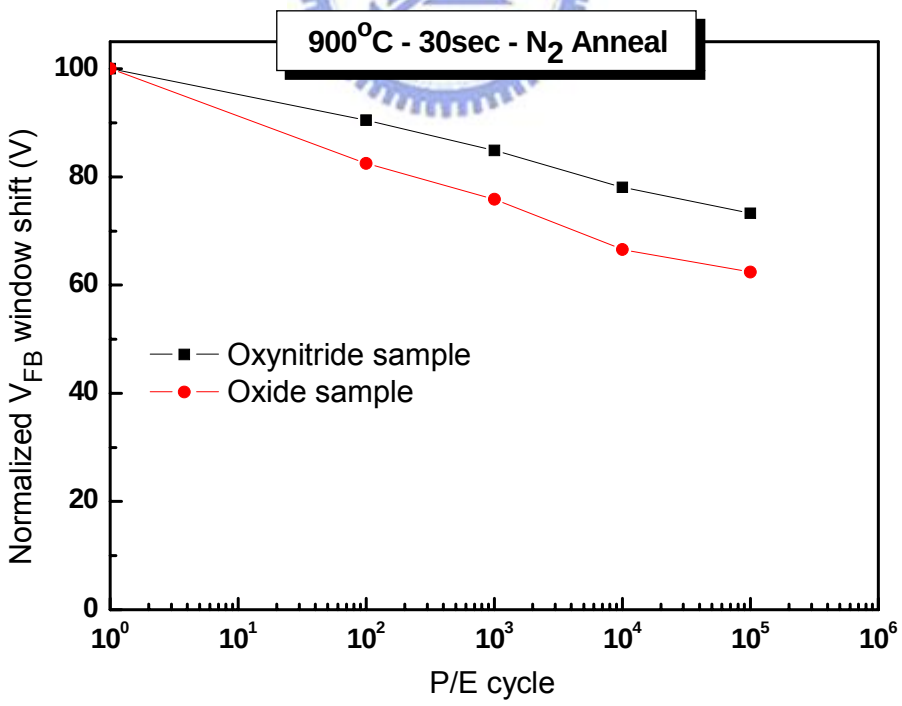
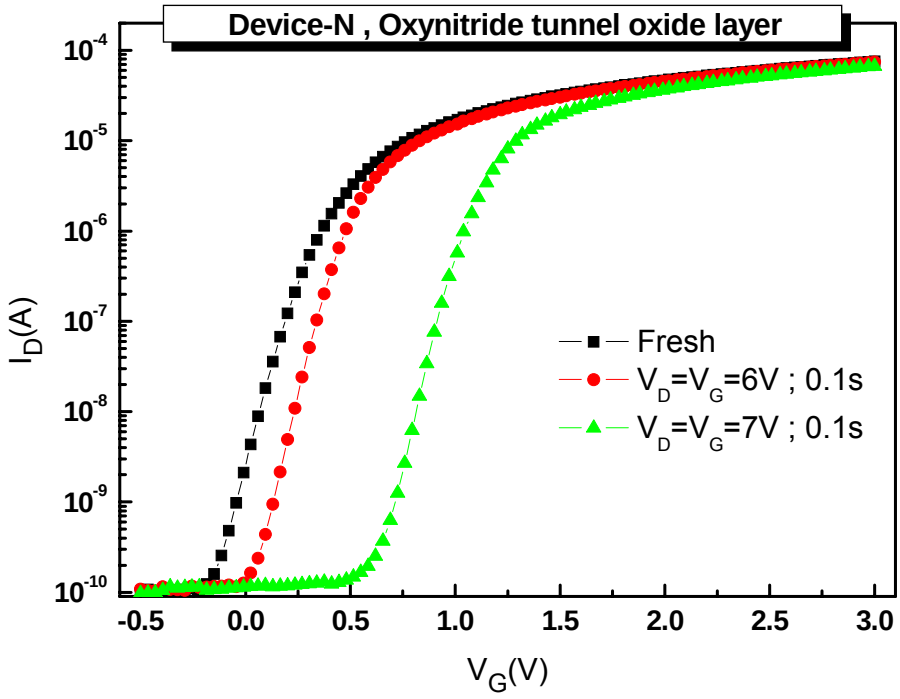
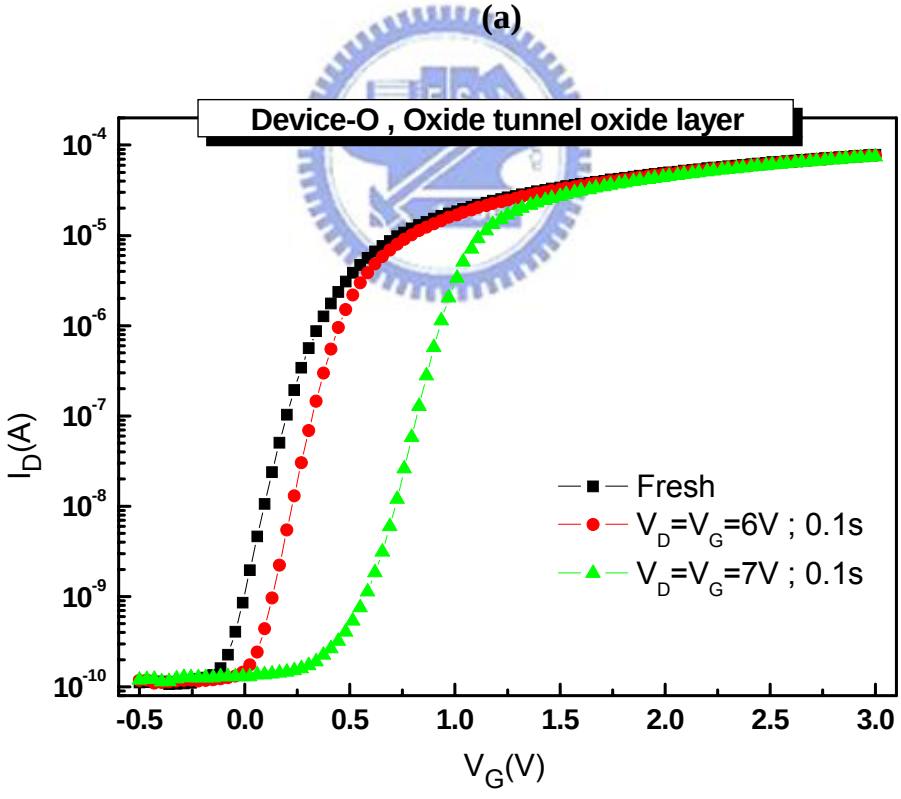


Fig 3-32: The endurance characteristics of Cap-N9 and Cap-O9.

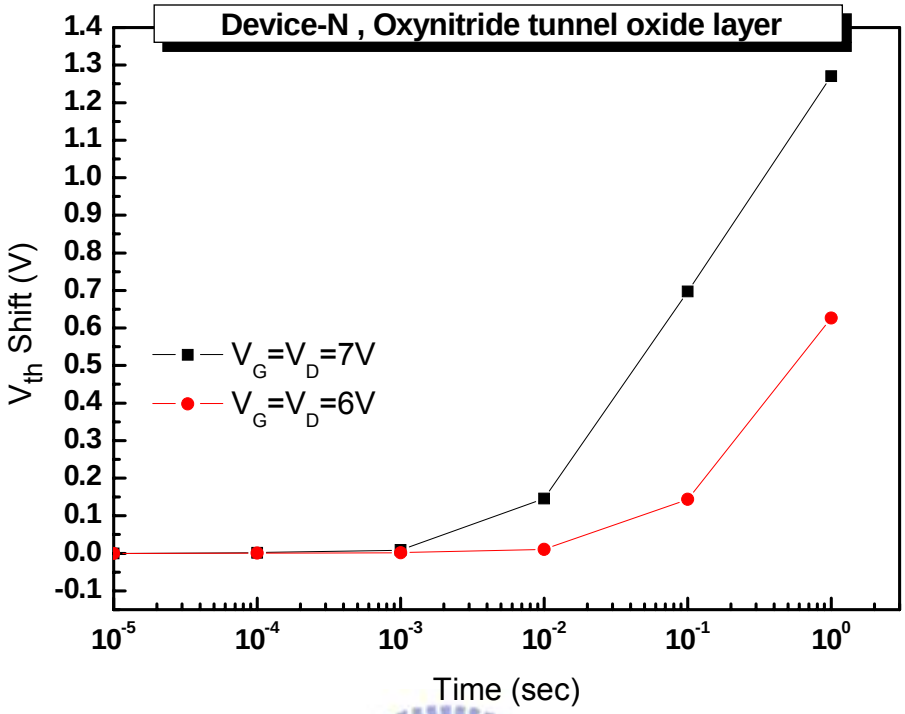


(a)

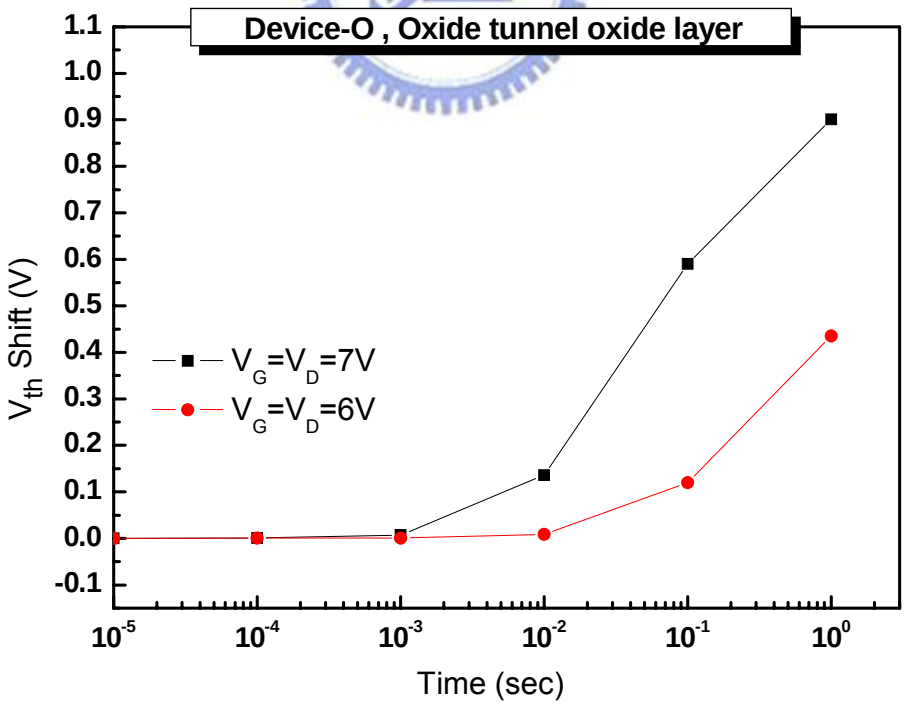


(b)

Fig 3-33: (a) I_D-V_G curve of oxynitride SOHOS memory cell with different programming conditions (b) I_D-V_G curve of oxide SOHOS memory cell with different programming conditions.

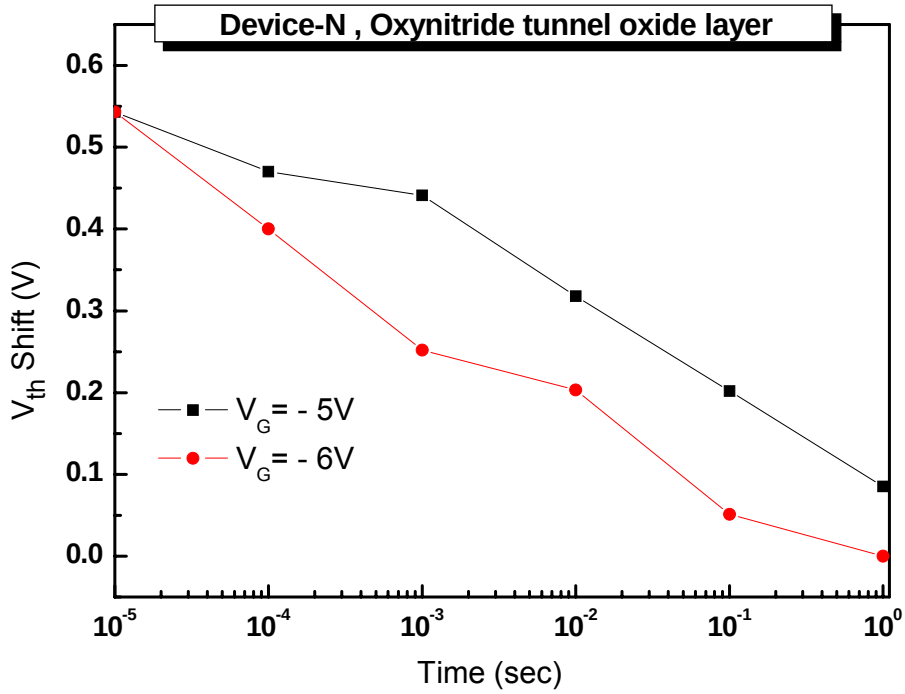


(a)

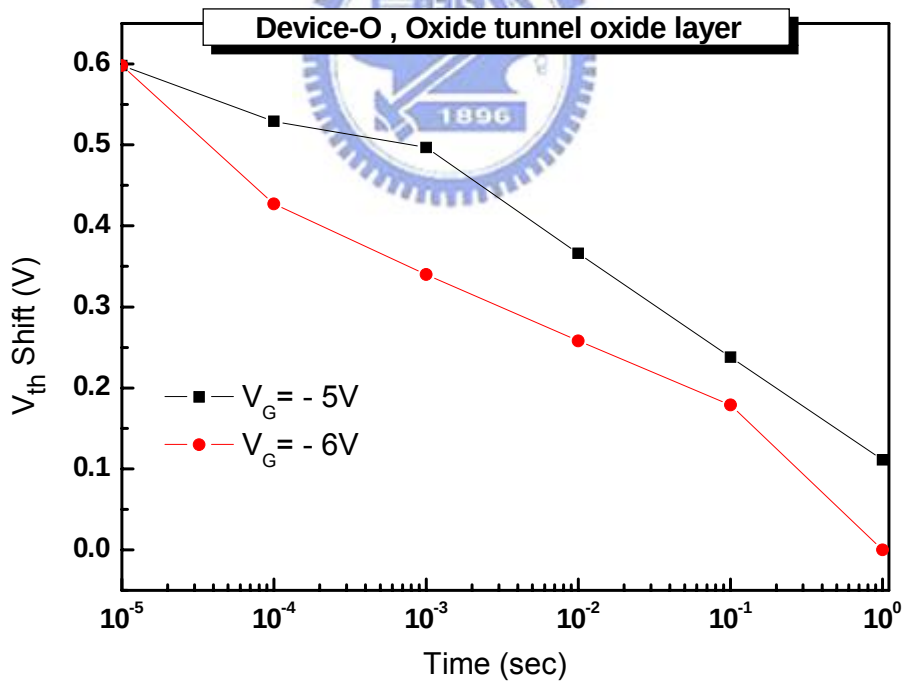


(b)

Fig 3-34: (a)Program characteristics of Device-N with different operating condition (b)Program characteristics of Device-O with different operating condition.



(a)



(b)

Fig 3-35: (a)Erase characteristics of Device-N with different operating condition (b)Erase characteristics of Device-O with different operating condition.

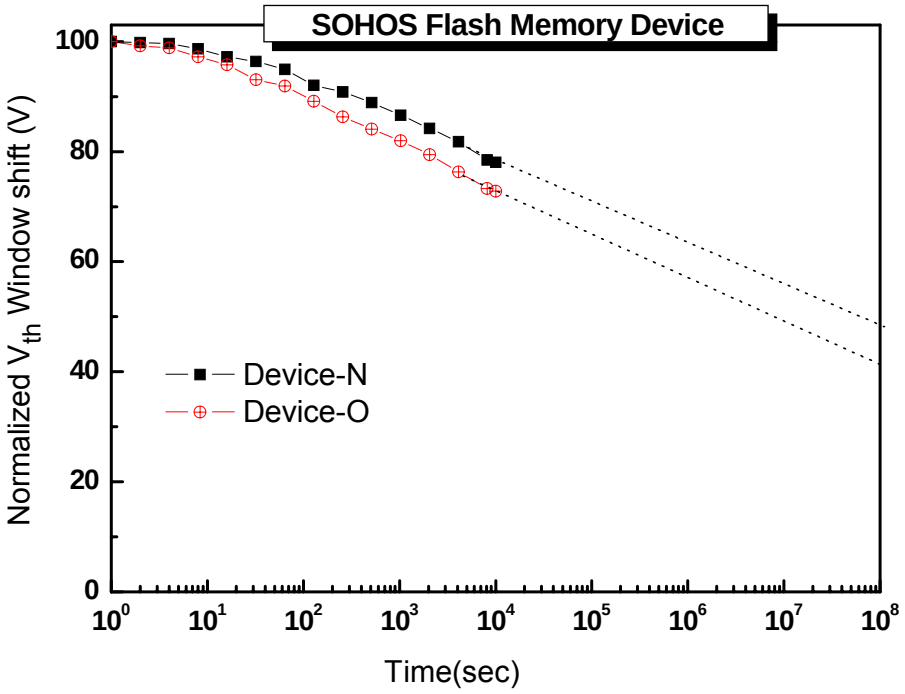


Fig 3-36: The compared retention characteristics of Device-N and Device-O.

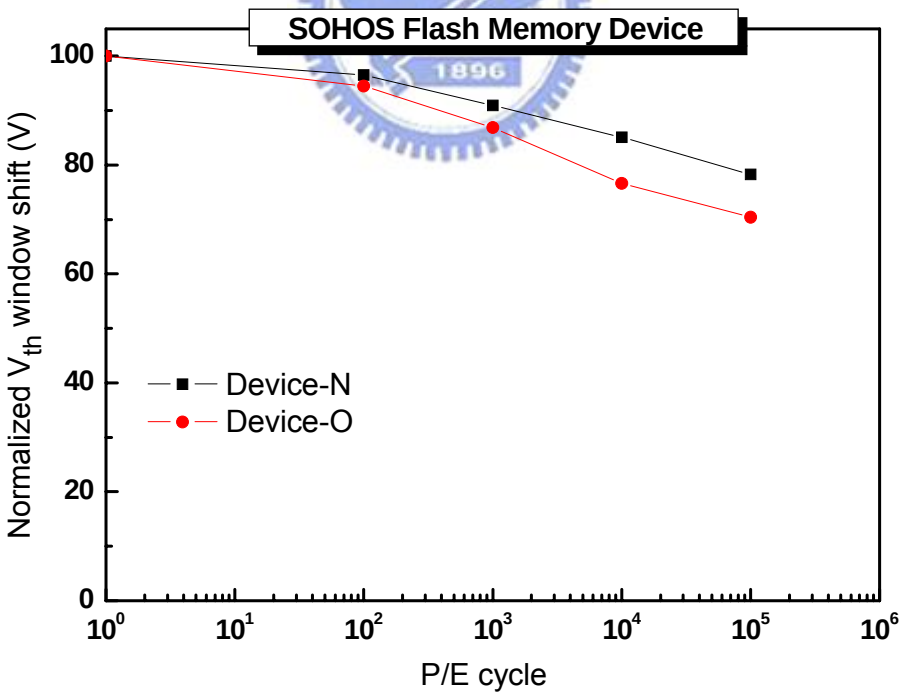


Fig 3-37: The endurance characteristics of Device-N and Device-O.

CHAPTER 4

Conclusion and Suggestion for Future Work

4.1 Conclusion

In this study, we focus on how to improve the reliability of Flash memory. The novel oxynitride process proposed here is simple and fully compatible with current IC industry fabrication technology. It can replace the conventional dry oxide in tunnel oxide of Flash memory and promote the reliability characteristics. From the measurement results of test capacitors and devices, we confirm that the oxynitride process is practicable. The oxynitride can promote not only the data retention but endurance of Flash memory. The better performance attributes to that the novel oxynitride can reduce the interface states and bulk defects of tunnel oxide.

In addition, in order to improve the programming speed and lower the programming voltage of SONOS Flash memory, the nitride trapping layer is replaced by HfO_2 trapping layer and called SOHOS-type Flash memory. In this study, the suitable PDA temperature of HfO_2 layer is investigated through test capacitors and applied in Flash memory cells. Therefore, the oxynitride tunnel oxide and HfO_2 trapping layer is workable in integrated memory cells.

4.2 Suggestions of the Future Work

1. More HRTEM images to evidence the precise thickness of the oxynitride layer .

2. More SIMS measurements to reveal the distribution of the element atoms in the oxynitride layer.

3. More XRD analysis to understand and verify the crystallization of the trapping layer.

4. Looking for a high-quality blocking oxide layer to fabricate stacked-gate Flash memory device and carry variable temperature retention measurements out.

5. Fabricate the thinner oxynitride tunneling layer and blocking oxide layer to promote the program and erase speed.

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碩士論文題目：

新穎含氮氧化層應用於二氧化鉿儲存層快閃記憶體之研究

Study on Novel Oxynitride Layer Applied to Flash Memory using HfO_2 as Charge Trapping Layer