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利用氟摻雜前處理技術應用於高介電常數閘極介電層薄膜電晶體之研究

Study on the Electrical Properties of Fluorine-Incorporated Poly-Si TFTs with High-κ Pr_2O_3 Gate Dielectric

研 究 生：張宏仁

指導教授：羅正忠　博士

邱碧秀　博士

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研 究 生：張宏仁　　Student：Hong-Ren Chang

指導教授：羅正忠　博士　　Advisor：Dr. Jen-Chung Lou

邱碧秀　博士　　Dr. Bi-Shiou Chiou

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學生：張宏仁　　指導教授：羅正忠 博士

邱碧秀 博士

國立交通大學

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摘要

在本論文中，首先，我們在成長複晶矽薄膜電晶體通道之後，運用氟離子佈值在複晶矽通道上，再整合氮化鈦金屬閘極與高介電常數材料三氧化二鐠，以形成低溫複晶矽薄膜電晶體(poly-Si TFTs)。使用三氧化二鐠可達到比目前常見的高介電常數材料還要高的介電常數，且其還有較低的閘極漏電流和卓越的熱穩定性。利用氮化鈦金屬閘極取代傳統複晶矽閘極可降低閘極片電阻。此外，氟離子佈值會鈍化捕陷狀態與消除應力鍵結去產生較強的氟鍵結，進而改善元件的特性。與未離子佈值的複晶矽薄膜電晶體比較之下，適量的離子佈值過後的複晶矽薄膜電晶體可提高導通電流，降低閘極漏電流，與改善可靠度。

另外，取代氟離子佈值，我們導入新穎的技術。即，在成長複晶矽薄膜電晶體通道之後，使用電漿增強化學蒸鍍系統(PECVD)在通道表面上打四氟化碳電漿(CF_4 plasma)，再結合氮化鈦金屬閘極與三氧化二鐠，形成低溫複晶矽薄膜電晶體(poly-Si TFTs)。同理，與未打四氟化碳電漿的傳統複晶矽薄膜電晶體做比較，有打四氟化碳電漿的複晶矽薄膜電晶體擁有較高的導通電流，較低的閘極漏電流與閘極引發汲極漏電(GIDL)，並且改善次臨限擺幅(Subthreshold Swing)與可靠度

的提升等等。然而過強的四氟化碳電漿會造成電漿傷害，進而造成元件劣化。

最後，我們分別對電漿處理與氟離子佈值過後的複晶矽薄膜電晶體進行熱載子應力測試之研究。實驗結果顯示，有經過電漿處理與氟離子佈值過後的複晶矽薄膜電晶體，其可靠度有明顯改善，這是由於氟會取代在複晶矽通道之中和矽與二氧化矽的界面處，較弱的矽氫鍵結，去形成較強的矽氟鍵結，進而提高對應力的免疫力。

Study on the Electrical Properties of Fluorine-Incorporated Poly-Si TFTs with High-κ Pr_2O_3 Gate Dielectric

Student：Hong-Ren Chang　　Advisor：Dr. Jen-Chung Lou

Dr. Bi-Shiou Chiou

Department of Electronics Engineering & Institute of Electronics

National Chiao Tung University

ABSTRACT

In this thesis, first, after being deposited the poly-Si channel of the thin-film transistors, we use fluorine ion implantation on the poly-Si channel incorporated with TiN metal gate and high-κ praseodymium oxide (Pr_2O_3) material to obtain low temperature poly-silicon TFTs. The dielectric constant value of high-κ Pr_2O_3 material is higher than the common high-κ materials and the poly-Si TFT with Pr_2O_3 gate dielectric exhibits lower gate leakage current and perform the superior thermal stability. Instead of conventional poly-silicon gate electrode, TiN metal gate can decrease the gate sheet resistance. In addition, fluorine ion implantation can passivate the trap state and relax the strain bonds to form stronger fluorine bonds, and then improve the performance of thin-film transistors. Comparing with no ion-implanted poly-Si TFTs, the poly-Si TFTs with appropriate dosage of ion implantation can raise the driving current, decrease the gate leakage current, and improve the reliability.

Besides, instead of fluorine ion implantation, the novel technique was

introduced and the processing fabrication is as follows, after being deposited poly-Si channel, utilizing CF_4 plasma treatment on the poly-Si surface of the channel in the plasma-enhanced chemical vapor deposition (PECVE) and incorporating with TiN metal gate electrode and Pr_2O_3 gate dielectric obtain the low temperature poly-silicon thin film transistors. The mechanism for the improvement of performance is the same as fluorine ion implantation, and the poly-Si TFTs with CF_4 plasma treatment own the higher driving current, lower gate leakage current and gate-induced-leakage current (GIDL), improve the subthreshold swing, and raise the reliability compared to the poly-Si TFTs without CF_4 plasma treatment. However, the excess RF power of CF_4 plasma treatment would cause plasma damage, and then create the degradation of device.

Finally, we examine the treated poly-Si TFTs on the hot-carrier stress test. Experimental results have shown that the poly-Si TFTs with CF_4 plasma and fluorine ion-implanted treatment would improve the reliability. This is due to fluorine pile-up in the interface between poly-Si channel and gate dielectric, and it can be in place of the weak Si-H bonds to form a strong Si-F bond. Thereby, it can raise the immunity against the hot carrier stress.

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Chapter 1

Introduction

1.1 Brief Overview of Poly-Si Thin-Film Transistors

A thin-film transistor (TFT) is that a field-effect transistor is deposited on insulating substrate, and it utilizes a semiconductor thin film as its channel. For the channel using Silicon thin films, they are divided into amorphous silicon (α-Si) TFTs and polycrystalline silicon (poly-Si) TFTs.

Amorphous silicon (α-Si) TFTs have some issues. For example, their mobility are extremely low because the low temperature process results in mobile leaking from source to gate or scatters at the interface, and the grain boundaries cause mobile scattering during transport. In recent years poly-Si TFTs are considered that they are better candidates than α-Si TFTs due to their higher mobility (ranging from 10 to 300cm^2/V-s) [1]. Therefore, polycrystalline silicon (poly-Si) thin film transistors (TFTs) have been widely used in a active-matrix liquid crystal displays (AMLCDs)[2]. The major application of poly-Si TFTs in AMLCDs lies in integrating the peripheral driving ICs, and the pixel switching elements on the glass substrate to realize system-on-panel (SOP) purpose[3]. Pixel TFTs need to operate at high voltages with low gate-leakage currents to drive the liquid crystal. In contrast, high-speed display circuits require that TFTs operate at low voltages and high driving currents with a low threshold voltage (V_{th}).

However, trap states of carriers at the poly-Si grain boundary cause the

degradation of electrical performance. In the ON state, the grain boundary traps capture carriers and form potential barriers, resulting in reduction of the carrier mobility. The effect will increase the threshold voltage and degrade the ON current as compared with single-crystalline Si MOSFET. In the OFF state, the grain boundary traps assist the carrier in generating in the depletion layer, and increase the leakage current. Therefore, reduction of trap states density in poly-Si channel is essential for fabricating high performance TFTs.

1.2 The Techniques of Performance Improvements

In order to obtain desirable characteristics of polysilicon TFTs, the major techniques had been employed to improve the device performance by reducing the trap state density or increasing the grain size of the polysilicon.. There are several methods to increase the grain size through SPC (solid phase crystallization)[4], ELA (excimer laser annealing)[5-6] and MILC (metal induced lateral crystallization)[7]. Furthermore, there are also many ways to reduce the trap-state density, such as plasma treatments or ion implantation. Various plasma such as H_2[8], NH_3[9], N_2O[10], O_2[11] and CF_4 plasma[12] have been intensely investigated in recent years. Besides, ion implantation, such as F^+[13], N^+[14], are incorporated into TFT poly-Si channel to terminate the poly-Si defects and then improve the performance.

Moreover, novel structure design is another approach to fabricate high-performance poly-Si TFTs. These techniques focus on reduction of the electrical field near the drain junction, and thus suppress the device's Off-state leakage current. Many structures including multiple channel structures [15], offset drain/source [16-17], lightly doped drain (LDD) [18], gate-overlapped LDD [19-21], field induced drain [22] and vertical channel [23] have been proposed and investigated intensively.

1.3 Incorporating High-κ Gate Dielectric

Generally speaking, using a thin gate oxide can increase the driving current of TFTs. Unfortunately, for a conventional gate dielectric (i.e., SiO_2 or Si_3N_4), a thinner gate dielectric may induce higher gate-leakage current and degrade the TFT characteristics significantly [24]. To preserve the physical gate-dielectric thickness while increasing the gate capacitance density and then improving the mobile carrier density in the channel region, high-κ gate-dielectric materials were suggested, such as Al_2O_3 [25], Ta_2O_5 [26], HfO_2 [27].

The relation between gate capacitance and dielectrics constant and equivalent oxide thickness (EOT) is shown:

$$C_{ox} = \frac{\kappa \varepsilon_0}{t_{high-k}} = \frac{\varepsilon_0}{t_{ox}} \quad \text{.....(Eq.1.1)}$$

where C_{ox} is the gate capacitance/unit area, ε_0 is the permittivity of free space, κ is the relative permittivity of high-κ, t_{ox} is the oxide thickness, $t_{high-\kappa}$ is the high-κ dielectric thickness.

Using the high-κ materials replace conventional oxide gate dielectric, attempts have been made to maintain these material amorphous even after post-deposition high temperature processing, in order to avoid surface roughness and grain boundary induced leakage current. In this thesis, we choose the excellent alternative which is the praseodymium oxide films[28].

1.4 Motivation

We choose the high-κ Pr_2O_3 material as the gate dielectric due to the high gate capacitance density and it can result in improving the mobile carrier density in the

channel region which is discussed in Chapter 2.

The trap states which are in the poly-Si TFT's channel and on the Si/poly-Si interface can trap carriers to form potential barriers, and thuss affect the current transport [29]. Moreover, the Off-current in poly-Si TFTs is associated with the amount of trap states in the drain depletion region. It can be attributed to thermionic emission at a low electric field and the field-enhanced emission (i.e. F-P emission or trap-assisted band-to-band tunneling) at a high electric field [30]. Hence trap states can lead to a poor device performance, such as low field-effect mobility, large leakage current, bad subthreshold slope and high threshold voltage.

Plasma treatments are believed to be the most effective methods to reduce trap states in the poly-Si. Many kinds of plasma such as H_2/N_2 mixture plasma [31], nitrogen implantation with H_2 plasma [32], pre-oxidation NH_3 annealing with H_2 plasma [33], NH_3 plasma [34] and H_2/O_2 plasma [35] have been proposed. Generally, hydrogen-based plasma is mostly adopted, because the hydrogen atoms can easily restore the trap states at the poly-Si/SiO_2 interface and in the grain boundaries. However, it is known that hydrogenated poly-Si TFTs have a troublesome issue in the device reliability [36-37]. The device performance degrades seriously under a long-term electrical stress. It is known that the poor device reliability of the hydrogenated TFTs is due to the weak Si-H and Si-Si bonds, which might be broken easily during the electrical stress and thus cause the creation of trap states in the poly-Si channel [38]. Recently, fluorination and technique has been proposed. It can improve both the device performance and also reliability, because the Si-F bonds are stronger than Si-H bonds [39-44]. So fluorine ion implantation (FII) technique is mostly adopted to introduce fluorine atoms into the poly-Si. Besides, the incorporation of nitrogen into the gate-dielectrics by different process has been widely

investigated to improve reliability [45-50]. The improved reliability is mainly due to the fact that most of the incorporated nitrogen can pile up at the gate-SiO_2/Si interface to make the interface more robust and then to improve the hot-carrier immunity. Moreover, the incorporation of nitrogen can also suppress boron penetration from the p^+-polysilicon gate due to the formation of gate oxynitrides. In Chapter 3, we investigate the improvement by fluorine implantation incorporated Pr_2O_3 high-κ gate dielectric and TiN metal gate.

However, the method of ion implantation may be not suitable for large-area electronics. Moreover, a subsequent high temperature process, required to activate implanted atoms and recover the damage created by implantation, is an issue for the current AMCLD fabrication process. Therefore, effective and process-compatible techniques introduce fluorine atoms into the poly-Si channel are needed to be developed. In Chapter 4, an effective and process-compatible fluorine incorporated technique is proposed by fluorine-based plasma treatment. We have successfully combined TiN gate, Pr_2O_3 high-κ gate dielectric, and CF_4 plasma to fabricate high-performance poly-Si TFTs.

1.5 Method of Device Parameter Extraction

In this thesis, we use HP 4156B-Precision Semiconductor Parameter Analyzer to measure the electrical characteristics of proposed poly-Si TFTs. Furthermore, we utilize FIB and TEM to see the cross-section view. The methods that we extract the characteristic parameters of poly-Si TFTs are described in this section.

1.5.1 Determination of Threshold Voltage

Threshold voltage (Vth) is an important parameter required for channel

length-width and series resistance measurements. However, V_{TH} is not uniquely defined. Various definitions have been proposed and the reason can be found in I_{DS}-V_{GS} curves. In this thesis, we use a simple method to determinate the Vth called constant drain current method. The voltage at a specified threshold drain current is taken as the Vth. This method is adopted in the most studied papers of poly-Si TFTs. It canbe given a threshold voltage close to that obtained by the complex linear extrapolation method. Typically, the threshold current is specified at $I_D=(W/L)\times 100nA$ for $V_{DS}=0.1V$ and $I_{DS}=(W/L)\times 100nA$ for $V_{DS}=5V$, where W and L is channel width and channel length, respectively.

1.5.2 Determination of Subthreshold Swing

Subthreshold swing (S.S) is a typical parameter to describe the control ability of gate toward channel, which reflects the turn on/off speed of a device. It is defined as the amount of gate voltage required to increase/decrease drain current by one order of magnitude.

The S.S. should be independent of drain voltage and gate voltage. However, in reality, the S.S. increase with drain voltage due to channel shortening effect such as charge sharing , avalanche multiplication and punch through effect. The subthreshold swing is also related to gate voltage due to undesirable and inevitable factors such as the serial resistance and interface states.

In this thesis, the S.S is defined as one-third of gate voltage required to decrease the threshold current by two order of magnitude. The threshold current is specified to be the drain current when the gate voltage is equal to threshold voltage.

1.5.3 Determination of Field Effect Mobility

The field-effect mobility is usually extracted from the maximum value of transconductance (Gm) at low drain bias (V_D=0.1V). The drain current in the linear region ($V_{DS} < V_{GS}-V_{TH}$) is expressed as the following equation

$$I_{DS} = \mu_{eff} C_{ox} (\frac{W}{L}) \left[(V_G - V_{th}) V_D - \frac{1}{2} V_{DS}^2 \right] \quad \text{.....(Eq.1.2)}$$

The transconductance Gm is gived by

$$g_m = \frac{\partial I_{DS}}{\partial V_G} = \mu_{FE} C_{ox} \left(\frac{W}{L} \right) V_D \quad \text{.....(Eq.1.3)}$$

Therefore, the field-effect mobility is

$$\mu_{eff} = \frac{L}{WC_{ox} V_{DS}} g_{m(\max)} V_{DS} \quad \text{.....(Eq.1.4)}$$

1.5.4 Determination of ON/OFF Current Ratio

On/off current ratio is one of the most important parameters of poly-Si TFTs since a high-performance device exhibits not only a large on-current but also a small off-current (leakage current). The leakage current mechanism in poly-Si TFTs is not like that in MOSFET. In MOSFET, the channel is composed of single crystalline Si and the leakage current is due to the tunneling of minority carrier from drain region to accumulation layer located in channel region. However, in poly-Si TFTs, the channel is composed of poly-Si. A large amount of trap state densities in grain structure attribute a lot of defect states in energy band gap to enhance the tunneling effect. Therefore, the leakage current is much larger in poly-Si TFTs than in MOSFET. When the voltage drops between gate voltage and drain voltage increases, the band gap width decreases and the tunneling effect becomes much more severe. Normally we can find this effect in typical poly-Si TFTs' I_{DS}-V_{GS} characteristics where the magnitude of leakage current will reach a minimum and then increase as the gate voltage decreases/increases for n/p-channel TFTs.

There are a lot of ways to specify the on and off-current. In this thesis, take n-channel poly-Si TFTs for examples, the on-current is defined as the drain current when gate voltage at the maximum value and drain voltage is 1V. The off-current is specified as the minimum current when drain voltage equals to 1V.

$$\frac{I_{ON}}{I_{OFF}} = \frac{Maximum\ \ Current\ \ of\ \ I_{DS}-V_{GS}\ \ Plot\ \ at\ \ V_{DS}=1V}{Minimum\ \ Current\ \ of\ \ I_{DS}-V_{GS}\ \ Plot\ \ at\ \ V_{DS}=1V} \quad \text{.....(Eq.1.5)}$$

1.5.5 Extraction of Grain Boundary Trap State Density

The Trap State Density (N_t), which can be determined by the theory established by Levinson et al. [51], which is based on Seto's theory [52].

For poly-Si TFTs, the drain current I_{DS} can be given as following:

$$I_{DS} = \mu_{FE} C_{ox} \left(\frac{W}{L}\right) V_{DS} V_{GS} \exp\left(\frac{-q^3 N_t^{\,2} L_c}{8\varepsilon_{Si} kTC_{ox} V_{GS}}\right) \quad \text{.....(Eq.1.6)}$$

Where,

μ_{FE} : field-effect mobility of carriers

q : electron charge

k : Boltzmann's constant

ε_{Si} : dielectric constant of silicon

T : temperature

N_t : trap-state density per unit area

L_c : channel thickness

This expression, first developed by Levinson et al., is a standard MOSFET's equation with an activated mobility, which depends on the grain-boundary barrier height. Levinson et al. assumed that the channel thickness was constant and equal to the thickness of the poly-Si film (t). This simplifying assumption is permissible only

for very thin film (t < 10nm). The trap-state density can be obtained by extracting a straight line on the plot of $\ln(I_{DS}/V_{GS})$ versus $1/V_{GS}$ at low drain voltage and high gate voltage.

Proano et al. [53] thought that a barrier approximation is to calculate the gate induced carrier channel thickness by solving Poisson's equation for an undoped material and to define the channel thickness (L_c) as a thickness in which 80% of the total charges were induced by the gate. Doing so, one obtains

$$L_c = \frac{8kTt_{ox}\sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{SiO_2}}}}{q\left(V_{GS}-V_{fb}\right)} \quad \text{.....(Eq.1.7)}$$

which varies inversely with $(V_{GS}-V_{fb})$. This predicts, by substituting Eq.1.7 into Eq.1.6, that $\ln[IDS/(V_{GS}-V_{fb})]$ versus $1/(V_{GS}-V_{fb})^2$. We use the gate voltage at which minimum leakage current occurs as flat-band voltage (V_{fb}). Effective trap-state density (N_t) can be determined from the square root of the slope.

$$N_t = \frac{C_{ox}}{q}\sqrt{|\ slope\ |} \quad \text{.....(Eq.1.8)}$$

1.5.6 Extraction of interface State Density

The effective interface trap states densities near (N_T) the SiO_2/Poly-Si interface were calculated from S.S. By neglecting the depletion capacitance in the active layer, the Nt can be expressed as [54]:

$$N_T = \left(\frac{S.S}{\ln 10}\frac{q}{KT}-1\right)\left(\frac{C_{ox}}{q}\right) \quad \text{.....(Eq.1.9)}$$

Where the Cox is the capacitance of the gate oxide and the S.S is subthreshold swing. The Nt value reflect both interface states and grain boundary trap states near the SiO_2/poly-Si interface.

1.5.7 Extraction of Active Energy

First, we measure the drain current versus the gate voltage for temperatures varying from 25 to 105℃. Then, we draw a plot of nature logarithm of drain current versus 1/KT at a fixed gate voltage and extract the absolute value of slope, i.e. the active energy E_A. In this case, the thermal dependence of drain current is given by:

$$I_{DS} \propto \exp\left(\frac{-E_A}{kT}\right) \quad \text{.....(Eq.1.10)}$$

Thus, we can plot the variations of E_A versus the gate voltage, for the whole gate-voltage range [55].

1.6 Organization of the Thesis

This thesis is organized as follow:

In Chapter 1, the overview of poly-Si TFTs, the method of device parameter extraction, the reason for high-κ extraction and motivations of this thesis are described.

In Chapter 2, we discuss the advantage of Pr_2O_3 high-κ material and TiN metal gate. Furthermore, Pr_2O_3 high-κ gate dielectric perform significant improvements in the device performance, such as lower threshold voltage, improved subthreshold swing, enhanced field effect mobility, and higher ON/OFF current ratio can be achieved as compared to the TEOS TFT even without other hydrogenation treatment.

In Chapter 3, the fabrication process of poly-Si TFTs combined with Pr_2O_3 gate dielectric, TiN gate and fluorine ion implantation will be proposed. Then, we research into the improvement degree of electrical characteristic and reliability.

In Chapter 4, the electrical characteristics and fabrication process of the

solid-phase-crystallized (SPC) poly-Si TFTs with CF_4 plasma treatment combined with Pr_2O_3 gate dielectric and TiN gate will be proposed. Also we explore its performance and reliability.

In Chapter 5, we will make conclusions and future works.

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Chapter 2

High-Performance Poly-Si TFTs with High-κ Pr_2O_3 Gate Dielectric

2.1 Introduction

Polycrystalline silicon thin-film transistors (poly-Si TFTs) have attracted much attention in active-matrix liquid crystal displays (AMLCDs) for the sake of realizing the integration of driving circuits and pixel elements on glass substrate to accomplish the system-on-panel (SOP) purpose [1]-[3]. For approaching the low power display driving circuits, high-performance poly-Si TFT with low operation voltage, low subthreshold swing, high driving capability, and low gate leakage current are required. A traditional solid-phase crystallized (SPC) poly-Si TFT with continued gate dielectric (i.e., SiO_2 or Si_3N_4) scaling is utilized to increase the gate capacitance density for driving current enhancement to reach the level of display driving circuits. However, employing a thinner gate dielectric would induce higher gate leakage current and degrade the TFT performance significantly [4]. In order to address these issues, integrating metal gate on high-κ gate dielectric with poly-Si TFT is urgently required for maintaining not only a higher gate capacitance density but also a lower gate leakage current with keeping thicker physical gate dielectric thickness [5]. Besides, the trap states at poly-Si grain boundaries also could be filled up quickly to improve the subthreshold swing even without additional hydrogenation treatment [6]. Therefore, several high-κ gate dielectrics including ONO gate stack, Al_2O_3, HfO_2, and

$LaAlO_3$ have been proposed to increase the gate capacitance density and reduce the gate leakage current for better gate controllability with keeping thicker physical gate dielectric thickness [7].

We generalize a summary of the needs for the selection of appropriate materials for gate dielectric applications. First, the suitable k value is about 12~60. In general, those materials with too large k-value almost have poor thermal stability. Second, the high-κ layer must act as an insulator. Higher energy band gap with conduction band offset ($\triangle E_c$ >1eV) or valence band offset ($\triangle E_v$ >1eV) in order to inhibit conduction by the Schottky emission of electrons or holes through the gate dielectric band. Lower energy band gap will lead to unacceptably gate leakage current. Third, the high-κ materials must not react with Si as far as possible during high temperature process. Since most high-κ materials reported that its oxygen would react with Si to form an undesirable interfacial layer in the interface and the high-κ material would react with Si to form the silicide. The formations of interfacial layer and sillicide result in lower k-value and consequently reduce the effective dielectric constant of the gate capacitor. Fourth, we must choose to use a crystalline or an amorphous structure because of the amorphous morphology has smaller leakage current than polycrystalline morphology. Fifth, the high-κ dielectric must have the excellent quality which has low density of intrinsic defect at Si/high-κ interface and in the bulk materials. For this reason, an amorphous gate dielectric could configure its interface bonding to minimize the number of interface defects. Hence, using an amorphous dielectric has many advantages over a polycrystalline dielectric.

According to the conclusion given above, we believe that the praseodymium oxide (Pr_2O_3) [8] is an outstanding gate dielectric because it has a high dielectric constant k about 31 [9], and large band gap equal to 3.9eV [10], the symmetrical band

offset larger 1eV respect to Si [11]. On the other hand, Pr_2O_3 exhibits lower leakage current density below $10^{-8}A/cm^2$ at Vg = ±1V than HfO_2 and ZrO_2 at the same equivalent silicon oxide thickness of 1.4nm [12][13], and it can suffer annealing of up to 1000℃ for 15 seconds with no structural changes and no degradation in electrical properties [14], in other words, Pr_2O_3 perform the superior thermal stability against degradation of crystalline dielectric.

CMOS devices with PVD TiN metal-gate have recently received lots of attention owing to the low resistivity of metal layers, the capability of eliminating the poly depletion effect (PDE) encountered in poly-gate counterparts and low temperature deposition process[15-17]. However, many process-related issues, such as the thermal stability and plasma damage may limit practical applications of metal-gate CMOS [18-19]. Because of the low temperature fabrication processing of poly-Si TFTs, we can reduce the degradation of TiN during high temperature process. Hence, TiN metal gate is an admirable metal gate for poly-Si TFTs.

In this paper, integration of TiN metal gate on high-κ Pr_2O_3 gate dielectric with SPC poly-Si TFT is successfully demonstrated for the first time. The proposed Pr_2O_3 gate dielectric poly-Si TFT show outstanding electrical characteristics as compared to tetraethoxysilane (TEOS) gate dielectric poly-Si TFT; hence, it may satisfy the needs of low power display driving circuit applications.

2.2 Experimental

For a start, in order to know the Pr_2O_3 k-value and its breakdown voltage, we built a capacitor structure and using Pr_2O_3 as its gate dielectric. The process follows: after cleaning the bare silicon, 33.6-nm Pr_2O_3 thin film was deposited by e-gun evaporation system as gate dielectric, followed by a furnace treatment at 600 ^oC for 30

min in N_2 ambient to improve the gate dielectric quality. In the end, a 500-nm aluminum film was deposited and patterned as the gate electrode.

On the other hand, the device of poly-Si TFTs with conventional gate dielectric tetraethoxysilane (TEOS) and high-κ Pr_2O_3 gate dielectric was described as follows. The cross section of the proposed self-aligned TiN gate and Pr_2O_3 gate dielectric TFT is depicted in Figure 2.1. First, a 100-nm undoped amorphous silicon (α-Si) layer was deposited on 500-nm thermally oxidized Si wafers by dissociation of SiH4 gas in a low-pressure chemical vapor deposition (LPCVD) system at 550 ^oC, followed by a solid-phase crystallization (SPC) process at 600 ^oC for 24 h in N_2 ambient for the phase transformation from amorphous to polycrystalline silicon. Individual device active region was patterned and defined. After the clean process, a 33.6-nm Pr_2O_3 thin film was deposited by e-gun evaporation system as gate dielectric, followed by a furnace treatment at 600 ^oC for 30 min in N_2 ambient to improve the gate dielectric quality. Then, a 200-nm TiN film was deposited and a Cl_2 based plasma etching process capable of stopping on the Pr_2O_3 layer was used to pattern the gate electrode. Next, a self-aligned phosphorous ion implantation was performed at the dosage and energy of 5 x 10^{15} cm^{-2} and 90 keV, respectively. The dopant activation was performed at 600℃ furnace annealing at nitrogen ambient for 30 min, followed by deposition of the 300-nm passivation layer in PECVD chamber at 300 ^oC. Next, a two-step wet-etching process is used to open the contact holes. The passivation SiO_2 and Pr_2O_3 film were etched away by buffered oxide etch (BOE) and H_2SO_4/H_2O_2 solution separately. Finally, a 400-nm aluminum film was deposited and patterned as the metal pad and sintered at 400℃ for 30min. For comparison, poly-Si TFTs with a 35-nm tetraethoxysilane (TEOS) as gate dielectric deposited by PECVD was prepared with the same process flow. Note that no hydrogenation treatment was

performed after the Al formation.

2.3 Result and Discussion

The cross-sectional transmission electron microscopy (TEM) image of the proposed TiN gate and Pr_2O_3 gate dielectric TFT structure is depicted in Figure 2.2, which shows a physical thickness of Pr_2O_3 film around 33.6-nm and the interfacial SiO_2 –like layer is about 1.5-nm [20].

A high gate capacitance density of 532 nF/cm^2 is obtained from capacitance-voltage (C-V) measurement of the capacitor structure, as shown in Figure 2.3. Moreover, forward sweeping (-4V to 4V) and reverse sweeping (4V to -4V) on V_g with repeating 100 cycles display the negligible C-V hysteresis characteristics for Pr_2O_3 gate dielectric. Such low charge-trapping phenomenon reveals an excellent gate dielectric property of Pr_2O_3 thin film [21][22]. From the TEM image and the C-V measurement, the equivalent-oxide thickness (EOT) and the effective dielectric constant (ε_r) of Pr_2O_3 gate dielectric are 6.5 nm and 26.2, respectively.

Figure 2.4 shows the J-E characteristic of the capacitor structure with Pr_2O_3 gate dielectric, and the J-E curves can be calculated from I-V curves, where J=I/(area of the capacitors) and E=V/(physical thickness of the high-κ gate dielectric). As can be seen, the Pr_2O_3 high-κ gate dielectric performs a high breakdown field (~7MV/cm) and a low leakage current (~5.9224×10^{-8}A/cm2 at V_G=1V). The breakdown filed of Pr_2O_3 is slightly smaller than TEOS (~10MV/cm). Therefore, this is high enough to drive a liquid crystal display.

To confirm the chemical composition of Pr_2O_3 gate dielectric on poly-Si substrate, x-ray photoelectron spectroscopy (XPS) measurement was performed. As shown in Figure 2.5, the measured XPS spectra of the Pr 3d and O 1s core levels for

Pr_2O_3 are in good agreement with previous experimental and theoretical data [23]. Besides, the binding energy of the Pr $3d^{5/2}$ core level for Pr_2O_3 and the difference between the binding energy of Pr $3d^{5/2}$ and the Pr $3d^{3/2}$ core level was typical to previously reported data on Pr_2O_3.

Figure 2.6 (a) shows the typical transfer characteristics (I_{DS}-V_{GS}) and maximum transconductance for the proposed Pr_2O_3 TFT and TEOS TFT with a dimension of Width/Length (W/L) = 2μm/2μm at V_{DS} = 0.1V and 1V, respectively. The ON/OFF current ratio is defined as that ratio of the maximum on-state current to the minimum off-state current at V_{DS} = 1 V. The threshold voltage (V_{TH}) is defined as the gate voltage required to achieve a normalized drain current of I_{DS} = (W/L)×100 nA at V_{DS} = 0.1 V. The Pr_2O_3 TFT exhibited improved electrical performance, including threshold voltage decreased from 2.28 V to 1.27 V, subthreshold swing improved from 1.08 V/dec. to 0.22 V/dec., and ON/OFF current ratio increased from 3.5×10^6 to 10.6×10^6, as compared to TEOS TFT. However, the undesirable gate-induced drain leakage (GIDL) current of the Pr_2O_3 TFT is higher than that of the TEOS TFT, especially under a continuously decreasing gate bias. This inferior GIDL current may be ascribed to the higher vertical electric field near the drain junction owing to the thin EOT of Pr_2O_3 gate dielectric. The issue could be relaxed by utilizing lightly doped drain (LDD) or field-induced drain (FID) structure [24], [25]. Figure 2.6 (b) shows the mobility for the proposed Pr_2O_3 TFT and TEOS TFT with a dimension of Width/Length (W/L)=2μm/2μm at V_{DS} = 0.1 V. The field-effect mobility (μ_{FE}) enhance from 23 cm^2/V-s to 44 cm^2/V-s under the gate voltage range between 0 to 8 V. Because of the subthreshold of TEOS is more slope than Pr_2O_3 high-κ , the mobility of TEOS is smaller than Pr_2O_3.

Typical output characteristics (I_{DS}-V_{DS}) of the proposed Pr_2O_3 TFT and TEOS

TFT are illustrated in Figure 2.7. The device has a drawn channel length (L) and channel width (W) of 2 μm and 2 μm, respectively. As can be seen, the driving current of Pr_2O_3 TFT (around 97 μA) is approximately six times larger than that of TEOS TFT (around 16 μA) at V_{DS} = 4 V and common gate drive of $V_{GS} - V_{TH}$ = 4 V, respectively. This driving current enhancement results from the high capacitance density induced higher mobility and smaller threshold voltage for the Pr_2O_3 TFT compared with the TEOS TFT. Hence, this large driving capability is attractive for high-speed peripheral driving IC's application. Note that obvious improvements in device characteristics were achieved even without the implementation of NH_3 plasma passivation [26] or advanced phase crystallization technique such as excimer-larser annealing (ELA).

The measured and extracted device parameters are summarized in Table 2.1, where the data value from TFT devices with other gate dielectrics, such as HfO_2, $LaAlO_3$, and PECVD TEOS oxide from this work are also shown for comparison. It was found that the electrical characteristics of the poly-Si TFT with the implementation of TiN metal gate on high-κ Pr_2O_3 gate dielectric were comparable to other reported data [5], [6]. Besides, we summarized the improved degree of this experimental result in Table 2.2. The enhancement of substhreshold is 86%, mobility is 91% and ON/OFF current ratio is 2 twice.

To examine the short-channel effect of TFTs with different gate dielectrics, the threshold-voltages (V_{TH}) rolloff of Pr_2O_3 and TEOS ploy-Si TFTs are compared in Figure 2.8. For poly-Si TFTs, the threshold-voltage rolloff is dominated by the decreasing of number of grain boundary as the devices scale down [27]. For the long-channel poly-Si TFTs, the large number of grain boundaries in the channel raises the threshold voltage and degrades the effective mobility [28]. The Pr_2O_3 TFTs with ultrathin EOT and large gate capacitance density can speedily fill the trap states at

grain boundary and turn on the devices fast; therefore, not only release the grain-boundary effect but also lower the threshold voltage effectively.

2.4 Summary

High performance SPC poly-Si TFT integrated with Pr_2O_3 gate dielectric and TiN metal gate has been successfully demonstrated for the first time. This work provides the thinnest EOT of 6.5-nm from the high gate capacitance density of Pr_2O_3 film. The electrical characteristics of Pr_2O_3 TFT can be effectively improved compared to those of TEOS TFT, including lower threshold voltage, steeper subthreshold swing, higher field-effect mobility, and higher driving current capability, even without additional hydrogenation treatment or advanced phase crystallization techniques. Therefore, the proposed Pr_2O_3 TFT is a good candidate for high performance TFT with low operation voltage.

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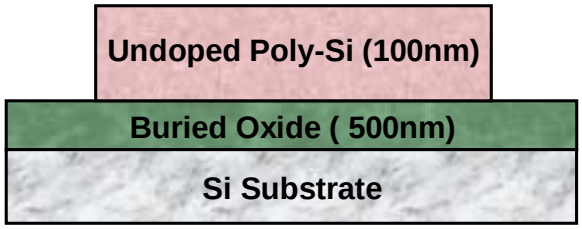
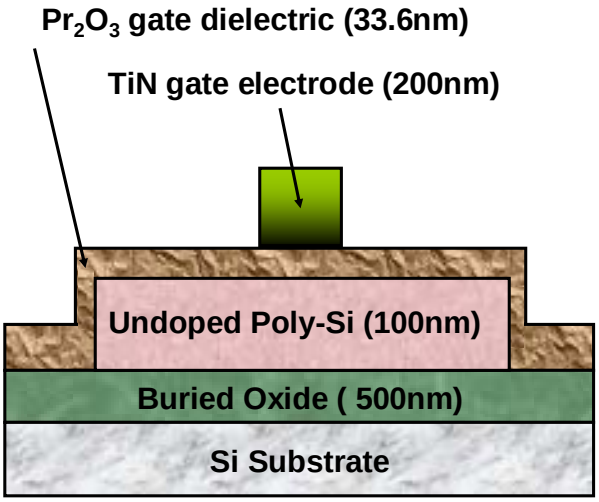
High-k process

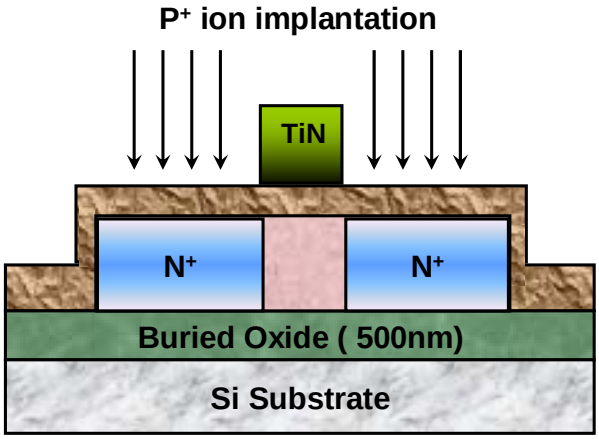
- 500-nm thermal oxidation at 980°C
- 100-nm α-si deposition at 550°C by LPCVD
- SPC at 600°C for 24h in N_2 ambient (α-Si ➔ poly-Si)
- Define active region



- 33.6-nm Pr_2O_3 film deposition by e-gun evaporation system
- Furnace annealing at 600°C for 30 min in N_2 ambient
- 200-nm TiN film by PVD
- Define gate electrode



- **Self-aligned source/drain implantation (P^+ $5x10^{15}$ 90keV)**
- **Dopant activation at 600°C for 30min in N_2 ambient**



- **300-nm passivation oxide SiO_2 by PECVD**
- **Define contact hole, two-step wet-etching process**
- **400-nm Al pads**
- **N_2/H_2 sintering at 400°C for 30min**

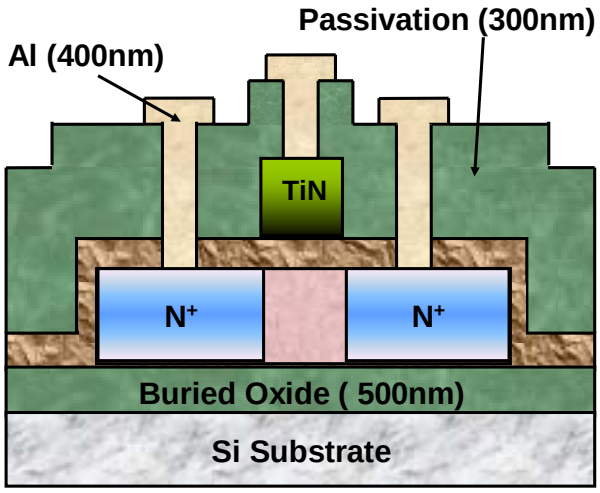


Fig. 2.1 Schematic diagram of the combined TiN gate and Pr_2O_3 gate dielectric TFT.

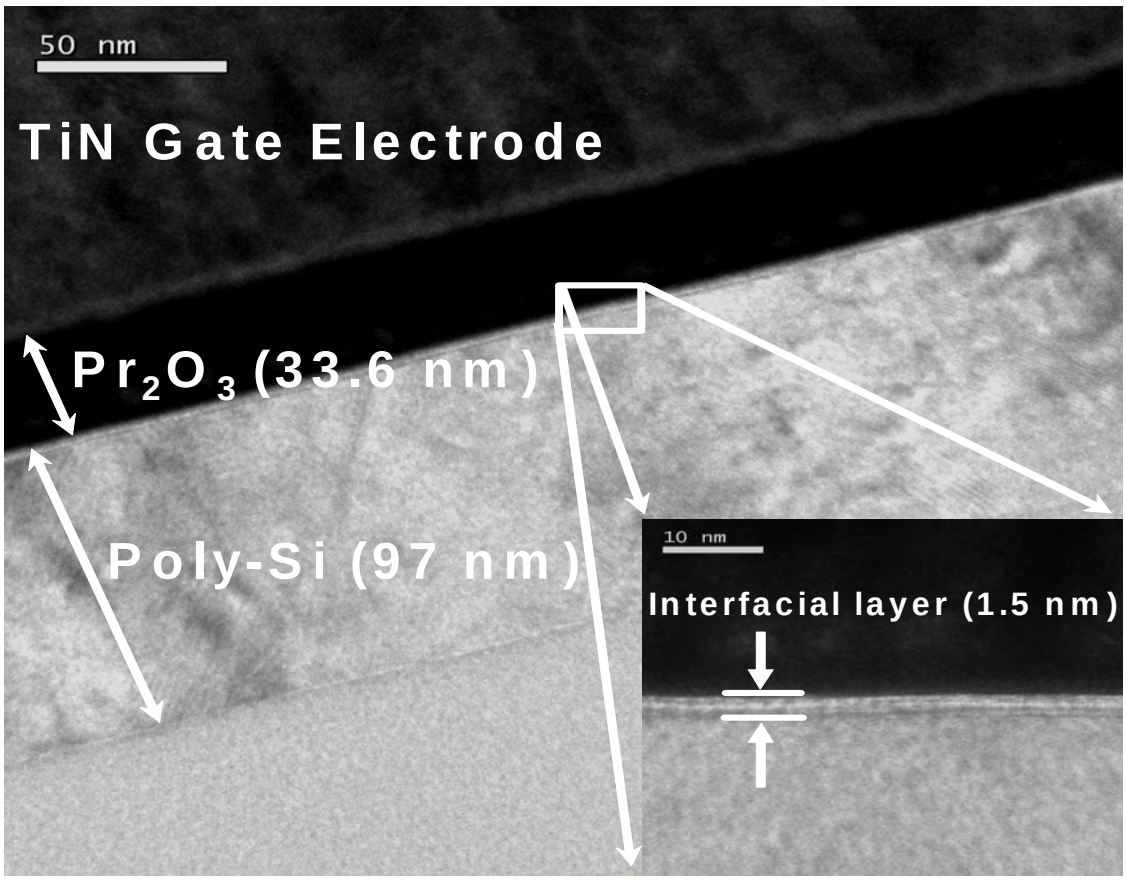


Fig. 2.2 TEM image of the proposed gate stack structure.

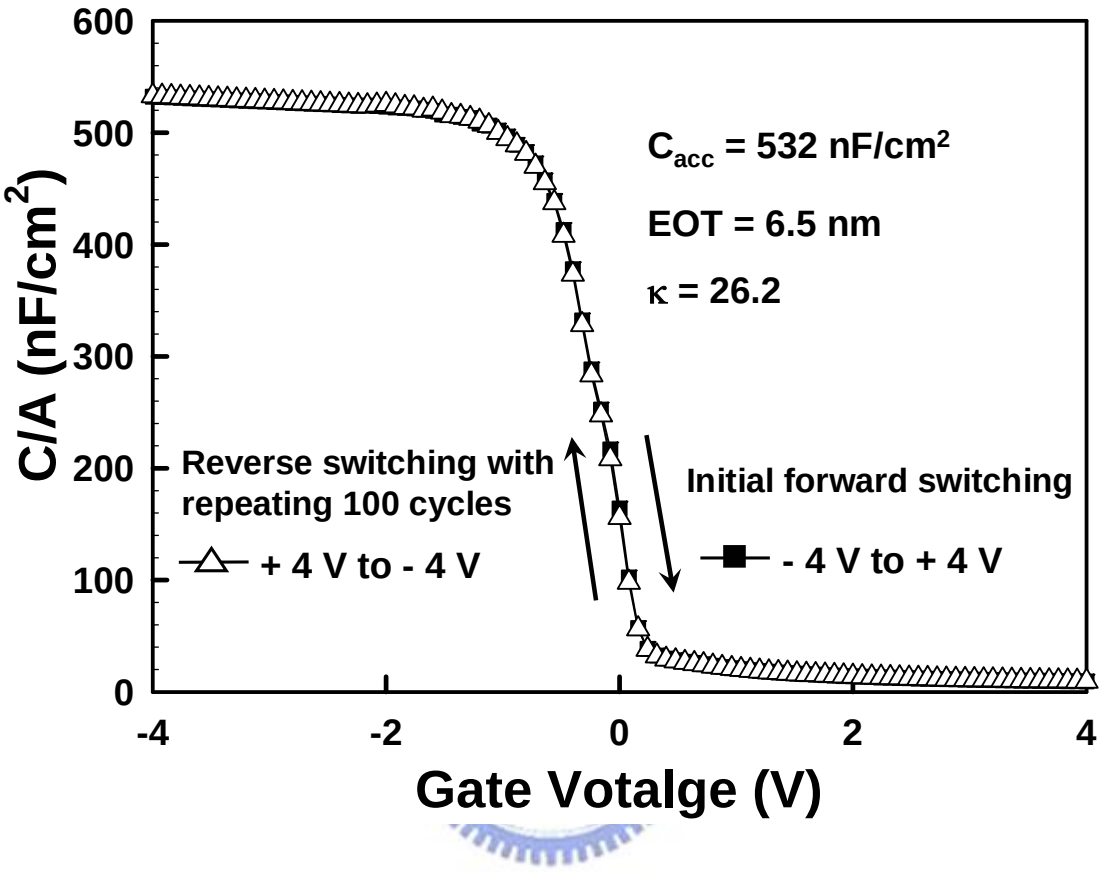


Fig. 2.3 Typical C–V characteristics of the Pr_2O_3 gate dielectric demonstrating the negligible hysteresis characteristics after repeating 100 forward and reverse cycles.

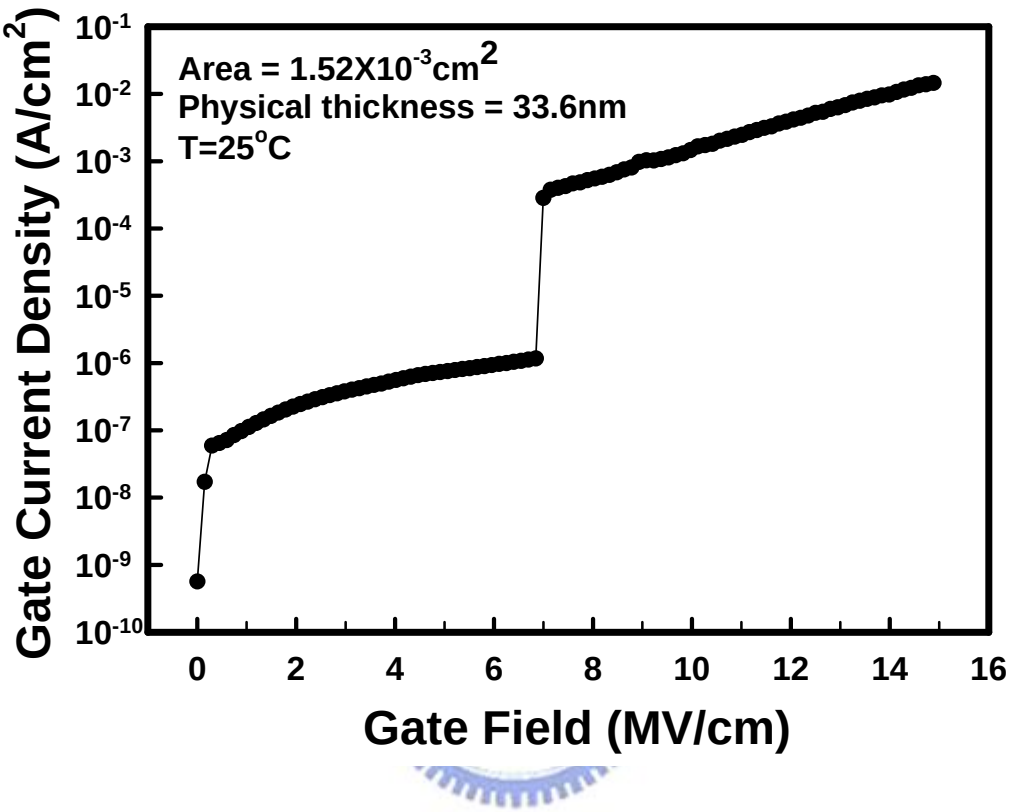


Fig. 2.4 J-E characteristic of the capacitors with Pr_2O_3 gate dielectric.

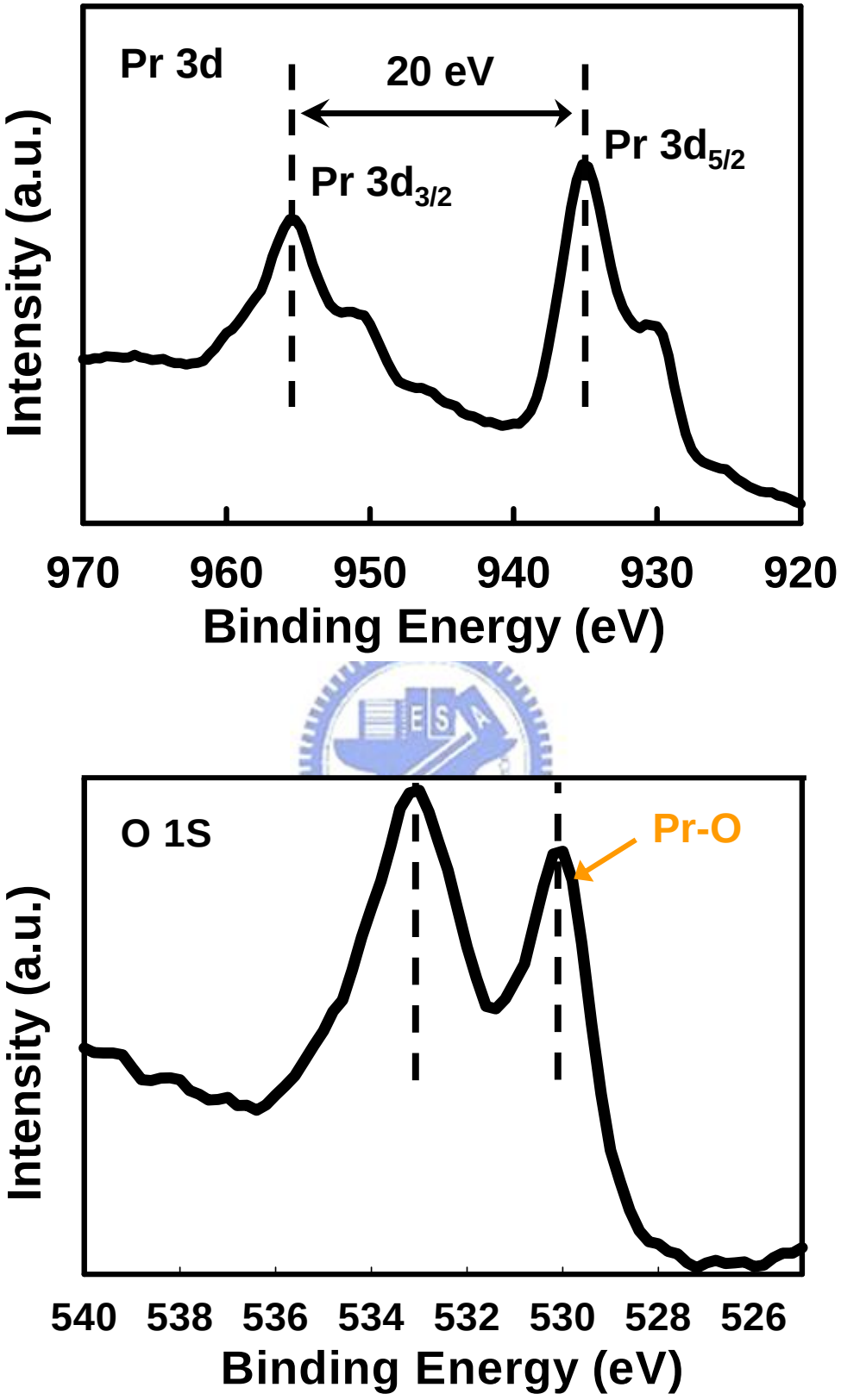
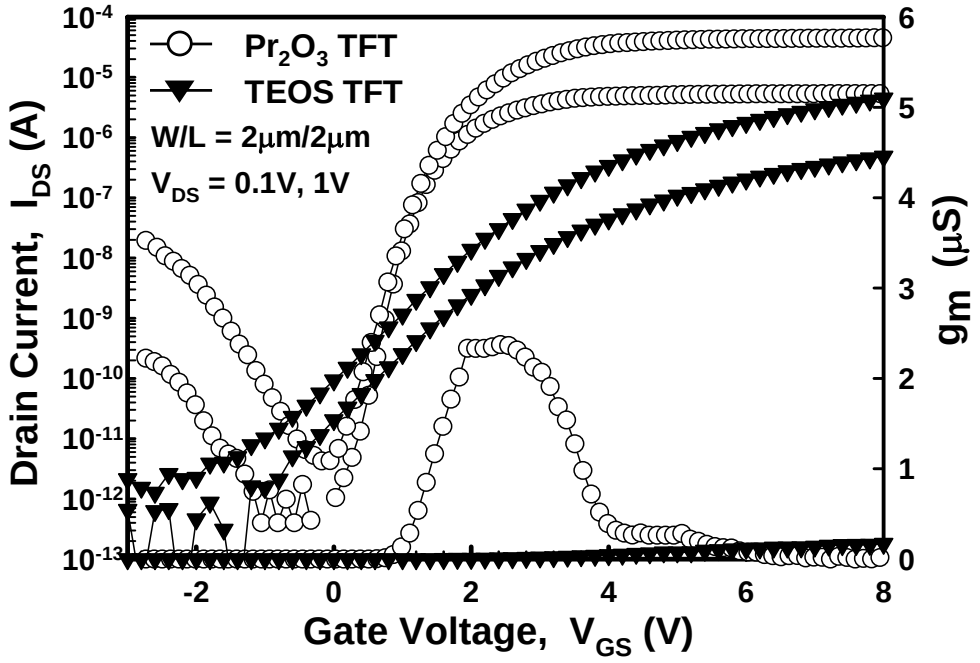
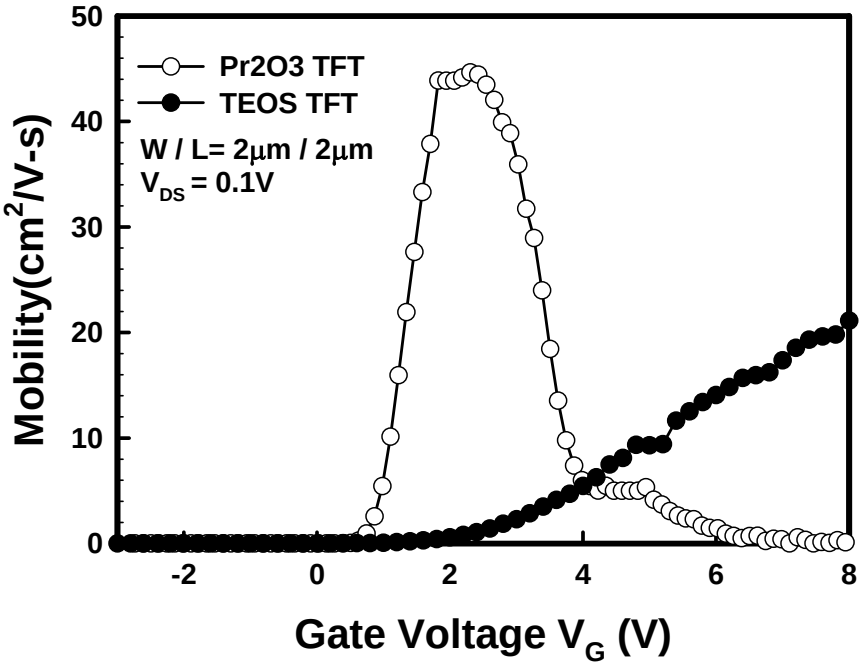


Fig. 2.5. Pr 3*d* photoelectron spectrum for Pr_2O_3.The inset also shows the O 1s photoelectron Spectrum which clearly indicates the presence of Pr_2O_3.



(a)



(b)

Fig. 2.6 (a) Typical transfer characteristics (I_{DS}-V_{GS}) and (b) mobilityof the proposed TiN metal gate and high-κ Pr_2O_3 gate dielectric poly-Si TFT. (W/L=2μm/2μm)

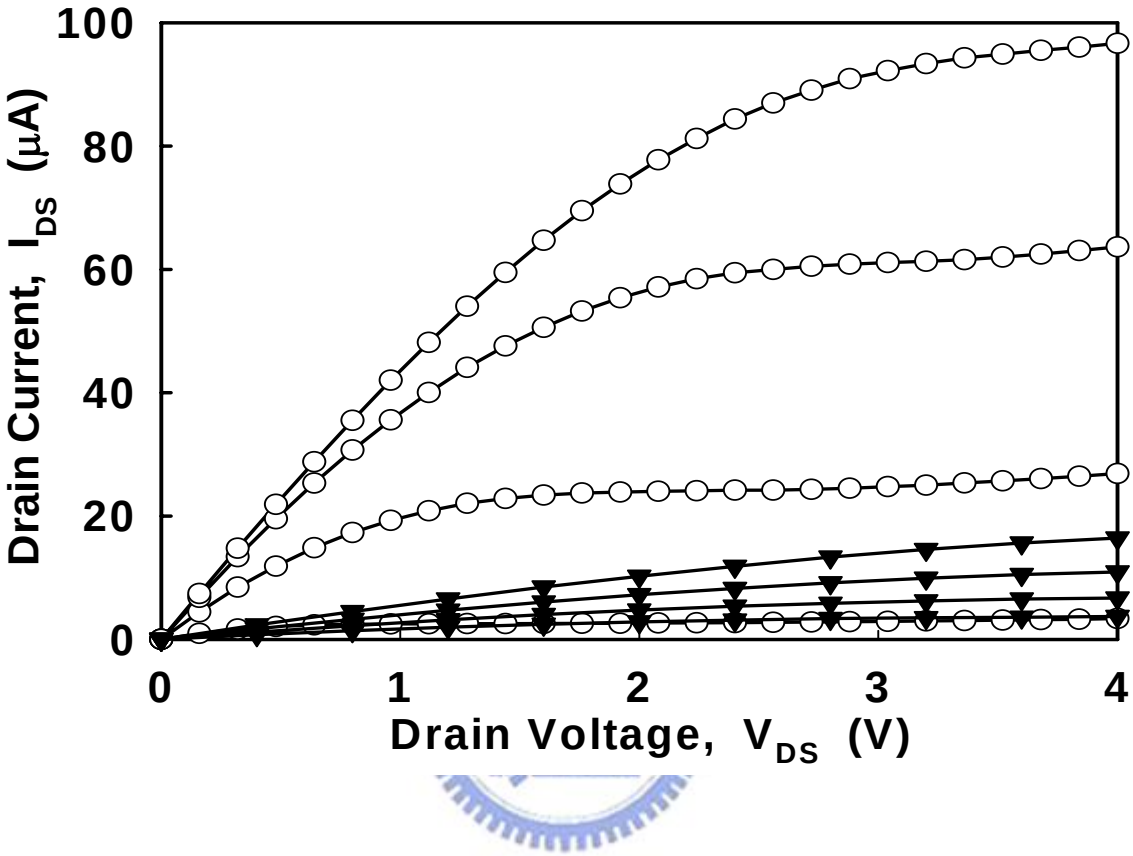


Fig. 2.7 Typical output characteristics (I_{DS}-V_{DS}) of the proposed TiN metal gate and high-κ Pr_2O_3 gate dielectric poly-Si TFT. (W/L=2μm/2μm)

SPC poly-Si TFT with various gate dielectrics	Pr_2O_3 [This work]	HfO_2 [5]	$LaAlO_3$ [6]	PECVD TEOS [This work]
$T_{Physical}$/ EOT	33.6 nm/ 6.5 nm	27.7 nm/ 7.3 nm	50 nm/ 8.7 nm	35 nm/ 42.6 nm
W/L (μm)	2/2	0.1/1	100/4	2/2
V_{TH} (V)	1.27	0.3	1.2	2.28
S.S. (V/decade)	0.22	0.28	0.31	1.08
μ_{EF} (cm^2/V-s)	44	39	40	23
I_{ON}/I_{OFF} ratio (10^6) (max I_{ON}@V_{DS}=1V)	10.6	9.7	1.5	3.5

Table 2.1 Comparison of device characteristics of the HfO_2, $LaAlO_3$, TEOS and Pr_2O_3 gate dielectric SPC poly-Si TFTs.

SPC poly-Si TFT with various gate dielectrics	Pr_2O_3 [This work]	PECVD TEOS [This work]	Enhancement
$T_{Physical}$/ EOT	33.6 nm/ 6.5 nm	35 nm/ 42.6 nm	X
W/L (μm)	2/2	2/2	X
V_{TH} (V)	1.27	2.28	1.01
S.S. (V/decade)	0.22	1.08	86%
μ_{EF} (cm^2/V-s)	44	23	91%
I_{ON}/I_{OFF} ratio (10^6) (max I_{ON}@V_{DS}=1V)	10.6	3.5	203%

Table 2.2 Improvement of device characteristics of the TEOS and Pr_2O_3 gate dielectric SPC poly-Si TFTs.

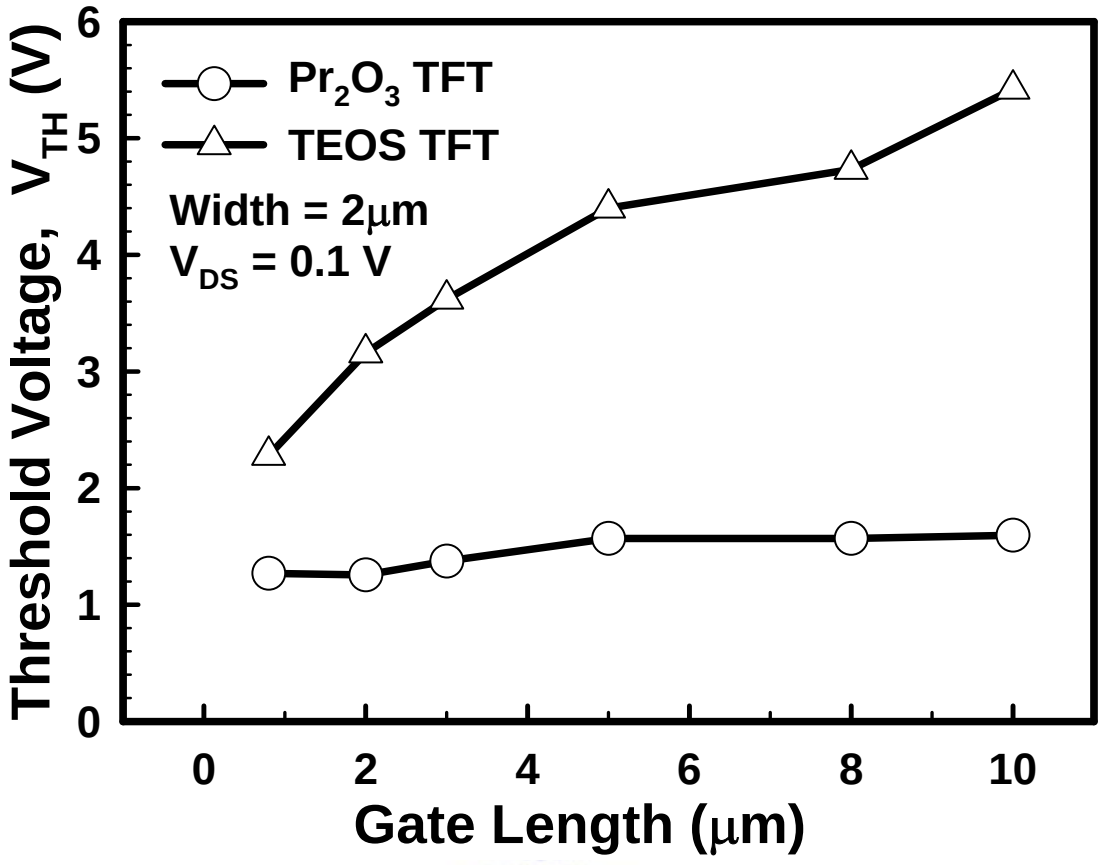


Fig. 2.8 Threshold-voltage rolloff of poly-Si TFTs with Pr_2O_3 and TEOS at V_{DS}=0.1V

Chapter 3

Fluorine-Ion Implanted Poly-Si TFTs with High-κ Pr_2O_3 Gate Dielectric

3.1 Introduction

The peripheral driving ICs of AMLCDs which is one of the major applications of poly-Si TFTs have the electrical characteristics requirement of low operation voltage, low threshold voltage, and high driving current. However, conventional solid-phase crystallization (SPC) poly-Si TFT with SiO_2 as gate dielectric can not satisfy the needs. In order to address this issue, several high-κ gate dielectrics including HfO_2 and $LaAlO_3$ were proposed to increase the gate capacitance density for better gate controllability with keeping the thickness of physical gate dielectric [1-2]. In this thesis, we choose Praseodymium oxide (Pr_2O_3) high-κ material as the gate dielectric and its excellent performance was discussed in Chapter 2.

On the other hand, the detrimental GIDL current from the grain boundaries trap states was observed in the unhydrogenated poly-Si TFT [3]. Hence, in order to obtain desirable characteristics of polysilicon TFTs, many techniques had been employed to improve the device performance by reducing the trap-state density or increasing the grain size of the polysilicon. Hydrogenation is a popular method to improve the TFT performance[4-6]. However, H_2-plasma treatment will loss their the passivation effect when the passivated samples are subjected to high temperature (> 500℃) annealing. Also, it had been found that the H_2-plasma applied on a MOS

capacitor creates positive charges in the oxide, hence, causing an undesirable flat band voltage shift of the device [7-8]. Furthermore, it was reported that [9-10] TFTs suffer a low hot carrier endurance after the H2-plasma passivation. For the H_2-plasma passivation, it is easy to passivate dangling bonds in grain boundaries to reduce the midgap deep states, while it needs a very long hydrogenation time (> 4 h) to passivate the strain-bond-related tail states [6]. However, it has been reported that the fluorine can break strained bonds, likely the strained Si-0-Si bonds and the Si-Si bonds to cause local strain relaxation [11-13] and to reduce the interface states [12]. Also, it was reported that fluorine may break a weak Si-H bond or a weak Si-OH bond to form a strong Si-F bond in its place at the Si/SiO_2 interface. With the fluorine implantation in the Si/SiO_2 interface, an MOS has a better irradiation and hot-carrier resistance . Recently, H. Kitajima *et al.* had found that F^+ implantation is effective to increase the ON-current of polysilicon TFTs by improving their subthreshold swings [14]. In this chapter, we examine the effect of fluorine implantation incorporated Pr_2O_3 gate dielectic and TiN metal gate on the performance of TFTs, in particular Vth, On-current, driving current, mobility, active energy and trap state density. Finally, the reliability of TFT such as hot carrier stress will be measured to proof that fluorine implantation on high-κ material will be improved effectively

3.2 Experimental

The cross-section fabrication process of the proposed TFT device is shown in Figure 3.1 and the self-aligned TiN gate and high-κ Pr_2O_3 gate dielectric poly-TFTs with fluorine ions implantation were describe as follows. Undoped amorphous silicon (α-Si) films of 50 nm thickness were initially deposited on thermally oxidized silicon wafers by an low-pressure chemical vapor deposition (LPCVD) system at 550^{o}C

followed by fluorine ions implantation into the α-Si film. The projected range of fluorine ions were set at the middle of a-Si layer and the implantation was performed without any pad oxide on a-Si. The dosage and ion accelerating energy was 5×10^{12} cm^{-2} and 11 keV, respectively. The F-implanted α-Si layer was subsequently recrystallized by a solid-phase crystallization (SPC) annealing at 600 °C for 24 h in N_2 ambient, and then patterned into the device active region. Next, a 40-nm Pr_2O_3 film was deposited by e-gun evaporation system as gate dielectric, followed by a furnace treatment at 600 °C for 30 min in N_2 ambient to improve the gate dielectric quality. A 200-nm TiN film was sequentially deposited by physical vapor deposition (PVD) and patterned to form the gate electrode. A self-aligned phosphorous ion implantation was applied at the dosage and energy of 5×10^{15} cm^{-2} and 80 keV, respectively, followed by dopant activation annealing at 600°C for 30min in N_2 ambient and a deposition of 300-nm plasma-enhanced CVD (PECVD) passivation layer. Subsequently, a two-step wet-etching process is used to open the contact holes. The passivation SiO_2 and Pr_2O_3 film were etched away by buffered oxide etch (BOE) and H_2SO_4/H_2O solution separately, which has rather high selectivity of Pr_2O_3/SiO_2. Finally, a 400-nm Al film was deposited and patterned as the metal pad. Finally, the devices were sintered at 400 °C for 30 min in N_2 ambient. For comparison, the control TFTs without fluorine ion implantation were prepared with the same process flow. No deliberate hydrogenation was performed, so that the "intrinsic" performance of the TFTs can be measured. For comparison, the control TFTs without the Nitrogen ion implantation were prepared with the same process flow. The electrical and reliability characteristics were performed by using HP 4156B.

3.3 Result and Discussion

The proposed TiN metal gate and Pr_2O_3 gate dielectric TFT structure is confirmed by transmission electron microscopy (TEM), as shown in Figure 3.2 which shows a physical thickness of Pr_2O_3 film around 40-nm. A high gate capacitance density of 463 nF/cm^2 is obtained from capacitance-voltage (Cg-Vg) measurement, as shown in Figure 3.3. Therefore, a thin equivalent-oxide thickness (EOT) of 6-nm was extracted from the Pr_2O_3 thin film.

Many references show the SIMS (secondary ion mass spectroscopy) profiles of the fluorinated poly-Si films. The SIMS profile exhibit the substantial amount of fluorine were introduced into the poly-Si layer by Fluorine ion implantation. The SIMS analysis also shows a notably high concentration of fluorine atoms piling up near the SiO_2/poly-Si interface, instead of in the deep poly-Si layer. Those results indicated that by employing this Fluorine implanted-treatment technique not only the fluorine atoms were introduced into the poly-Si but also the Si-F bonds were formed in the SiO_2/poly-Si interface.

Therefore, these results figure that trap states in both grain boundaries and the SiO_2/poly-Si interface were reduced by using Fluorine implanted treatment, which resulting the great improvement in the device performance. Based on these results, a schematic cross section view of the SiO_2/poly-Si interface is illustrated in Figure 3.4. It is suggested that strong Si-F bonds replace the dangling and strain bonds for the fluorinated poly-Si films, and thus improve the device performance.

Typical transfer characteristics I_{DS}-V_{GS} of the integrated TiN gate and high-κ Pr_2O_3 TFTs with and without Fluorine implanted treatment are shown in Figure 3.5. The drawn channel length (L) and channel width (W) are 5μm and 10μm, respectively. The measurements were performed at two different drain voltage of V_{DS}=0.1 and 1V. According to the method of parameter extraction in Chapter 1, the Vth and S.S. of the

fluorinated poly-Si TFT were found to be 0.735V and 200mV/dec. extracted from Figure 3.5, which are superior to those of the control one (1.54V and 278mV/dec.). It's know that the Vth and S.S. are strongly influenced by the deep trap states, associated with dangling bonds in the channel, which have energy states near the middle of the silicon band gap. Therefore, one can infer that Fluorine implanted treatment can terminate the dangling bonds in the poly-Si and SiO_2/poly-Si interface. Additionally, the I_{ON} , I_{OFF} and ON/OFF current ratio of the fluorinated TFT are also better than those of the control TFT, because Fluorine implantation can cause the decrease of trap states which can assist the carrier generation in the depletion layer and increase the leakage current in the OFF state and capture carriers and form potential barriers, resulting in reduction of the carrier mobility and degradation of the ON current in the ON state.

Besides, while the applied gate voltage was toward negative, the fluorinated poly-Si TFT show smaller leakage current compared with that of the control TFT, i.e. GIDL effect is suppressed. It is know that under a high electric field leakage current of the poly-Si TFT mainly comes from the trap-assisted band to band tunneling near the drain edge [15]. This observation suggest that there must be fewer trap states existed in the fluorinated poly-Si TFT, and thus the leakage current under a high electric field is reduced.

Figure 3.6 shows field-effect mobility versus the gate voltage of control and fluorinated poly-Si TFTs. The field-effect mobility was calculated from the value of transconductance at V_{DS}=0.1V. The Fluorinated poly-Si TFT shows approximately 41% enhancement in the maximum field-effect mobility. Note that the filed-effect mobility is significantly affected by the tail states near the band edge, which is resulted from the strain bond in the poly-Si and SiO_2/poly-Si interface [16]. These

results imply that Fluorine implanted treatment may not only terminate the dangling bonds, but also relieve the strain bonds.

Figure 3.7 shows the typical I_{DS}-V_{DS} output characteristics for the integrated TiN gate and Pr_2O_3 gate dielectric with Fluorine implanted -treated TFTs and control TFTs. The devices have a drawn channel length (L) of 5 μm and a channel width (W) of 10 μm, respectively. Clearly, the driving current of Fluorine implanted-treated TFT (about 150 μA/μm) is larger than that of control TFTs (about 95 μA/μm) at V_{DS} = 4 V and V_{GS} = 4 V. This is due to the higher mobility and smaller threshold voltage of the fluorinated poly-Si TFT. This large driving capability is desirable for high-speed display IC's application resulted from the high gate capacitance density.

Figure 3.8 shows that the kink-point voltage (i.e. the voltage of kink-effect (also named "floating-body effect) occurred) versus different gate voltage extracted from Figure 3.7, and its mechanism is explained as follows [17-18]. For short gate length and high drain bias, the lateral electric field causes impact ionization near the drain, generating electron-hole pairs. These electrons contribute to the drain current, whereas the holes drift from the drain and gate regions toward the source and polysilicon-SiO_2 interface regions. The presence of these holes raises the body potential, which may become large enough to forward bias the body-source diode. When this occurs, the hole current flowing into the source results in injection of electrons into the body. These electrons flow along the field into the drain region, and the entire process repeats. This causes an increase in the drain current and a decrease in threshold voltage, as observed. By Fluorine ion implantation, the kink-effect can be reduced owing to the decrease of the trap state which is the location usually occurred impact ionization in the poly-Si bulk, and then the kink-point voltage will be raised as shown in the Figure 3.8.

The grain boundary trap state densities (N_T) of the conventional and fluorinated high-κ gate dielectric poly-Si TFTs were estimated by Levison and Proano method [19-20] and we have demonstrated in Chapter 1. Figure 3.9 exhibits the plots of the $\ln[I_D/(V_{GS}-V_{FB})]$ versus $1/(V_{GS}-V_{FB})^2$ curves at low V_{DS} and high V_{GS}. The fluorinated Pr_2O_3 high-κ gate dielectric poly-Si TFT exhibits a Nt of 4.58×10^{12} cm-2, whereas the control TFT has 14.4×10^{12} cm-2. This result implies that the Fluorine implantation treatment can terminate the grain boundary trap state in the poly-Si film. To further study the fluorine passivation effect near the interface, the effective interface trap states densities (N_{IT}) near the SiO_2/poly-Si interface were also calculated. Form Chapter 1, we have known the effective interface trap states density equation which can be expressed as: $N_{IT}=[(S.S./\ln10)(q/KT)-1](Cox/q)$. The N_{IT} of the control TFT and the fluorinated high-κ gate dielectric TFT are 10.6×10^{12} cm-2 and 6.81×10^{12} cm-2, respectively. The value of grain boundary trap state densities (N_{IT}) reflects trap states near the SiO_2/poly-Si interface.

The key parameters were summarized in the Table. 3.1. Comparing with conventional TFTs, the TFT by utilizing Fluorine implanted treatment is performed prior high-κ deposition, Vth decreased from 1.54V to 0.735V, S.S. decreased from 278 mV/dec to 200 mV/dec, Ion/Ioff increased from 1.98×10^6 to 9.27×10^6 while VDS=1V grain boundary traps densities decreased from $14.4\times10^{12}cm^{-2}$ to $4.58\times10^{12}cm^{-2}$, and interface trap states decreased from 10.6×10^{12} cm^{-2} to 6.81×10^{12} cm^{-2}.

Figure 3.10 exhibits the activation energy (Ea) versus the gate voltage for the control and fluorinated poly-Si TFTs at V_{DS}=0.1V. In Off-region (low V_{GS}), the value of Ea reflects the required energy for carriers to leak by means of traps, whereas in On-region (high V_{GS}), the value of Ea reflects the carriers transport barrier caused by

the trap states within the poly-Si channel [21]. Compared with the control TFT, the extracted activation energy (Ea) of the fluorinated poly-Si TFT decreases in On-region and increases in Off-region. That is to say, for fluorinated poly-Si TFT, fluorine atoms can passivate the trap states and hence reduce the barrier height for carrier transport when device is turned on. On the other hand, in Off-region fewer trap states after fluorinating process resulting in the increasing of Ea and thus the trap-assisted leakage current is suppressed. Moreover, in the subthreshold region, a steeper profile can be found for the fluorinated TFT, which proves that the interface quality of the fluorinated TFT is much better than that of the control TFT.

Additionally, the hot carrier stress was carried out to examine the reliability pf the device. The drawn channel length (L) and channel width (W) are 10μm and 10μm, respectively. The device degradation under hot carrier stress can be attributed to two mechanisms: oxide trap charges and the creation of trap states in the poly-Si. This can be attributed to channel-hot-electron (CHE) and self-heating (SH) phenomenon. For CHE, electrons were injected and trapped in the gate oxide; then, the carrier flow in the channel is disturbed, therefore reduced the On-current. SH-induced damage is due to the large Joule heat, resulted from a high drain current [22-23]. Because TFTs are fabricated on a poor thermal-conducting substrate, device can reach a very high temperature during operation. Such high temperature enhances the breaking of Si-H bonds at grain boundaries to generate trap states in the poly-Si channel and the generation of Si/SiO_2 interface states [9-10], and degrade the TFT performance.

The stress condition is applied at $V_D = V_G = 4$ V for 1000 s to examine the electrical reliability. The threshold voltage variations and the on-current degradation are shown in Figure 3.11 and Figure 3.12. The variation of I_{ON} and V_{TH} were defined as (V_{TH},stressed-V_{TH},initial) and (I_{ON},stressed - I_{ON},initial)/ I_{ON},initial×100 (%),

respectively, where V_{TH},initial, I_{ON},initial and V_{TH},stressed, I_{ON},stressed represent the measured values before and after stress. As can be seeen, the CF_4 plasma treated TFTs have high immunity against the hot carrier stress as compared to control TFTs. We deduce that the significant improvement in the electrical reliability is attributed to the formation of stronger Si–F bonds in place of weaker Si–Si and Si–H bonds in the poly-Si channel and at the Si/SiO_2 interface.

3.4 Summary

Integration of TiN metal gate with high-κ Pr_2O_3 gate dielectric on fluorine-implanted poly-Si TFT has been successfully demonstrated for the first time. Significant improvements in the device performance, including lower threshold voltage, steeper subthreshold swing, improved field effect mobility, and enhanced I_{ON}/I_{OFF} ratio are achieved with fluorine incorporation within the poly-Si layer. In addition, the fluorine-incorporated poly-Si TFT can improve the hot-carrier immunity due to the formation of stronger Si-F bonds instead of the weak Si-Si and Si-H bonds within the poly-Si channel. Therefore, combining this simple and effective fluorine-incorporation technique with high-κ Pr_2O_3 gate dielectric on poly-Si TFT is a good candidate to further improve the device performance and reliability.

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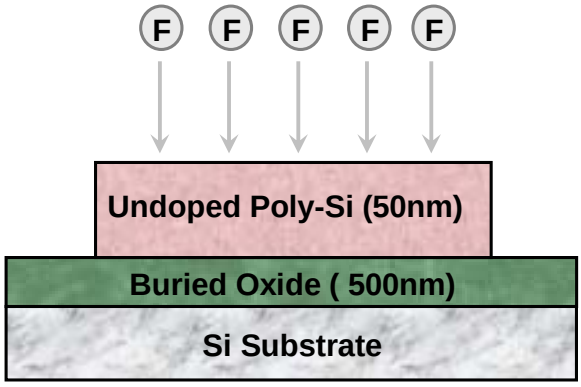
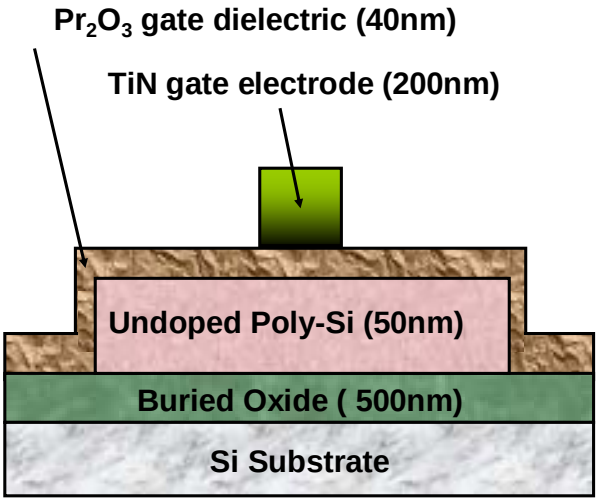
Fluorine implant process

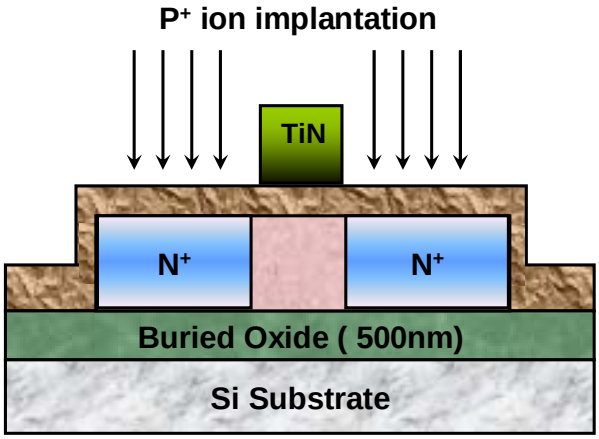
- 500-nm thermal oxidation at 980°C
- 50-nm α-si deposition at 550°C by LPCVD
- Fluorine implantation: 5E12, 11KeV
- SPC at 600°C for 24h in N_2 ambient (α-Si ➔ poly-Si)
- Define active region



- 40-nm Pr2O3 film deposition by e-gun evaporation system
- Furnace annealing at 600°C for 30 min in N2 ambient
- 200-nm TiN film by PVD
- Define gate electrode



- **Self-aligned source/drain implantation (P^+ $5x10^{15}$ 80keV)**
- **Dopant activation at 600°C for 30min in N_2 ambient**



- **300-nm passivation oxide SiO_2 by PECVD**
- **Define contact hole, two-step wet-etching process**
- **400-nm Al pads**
- **N_2/H_2 sintering at 400°C for 30min**

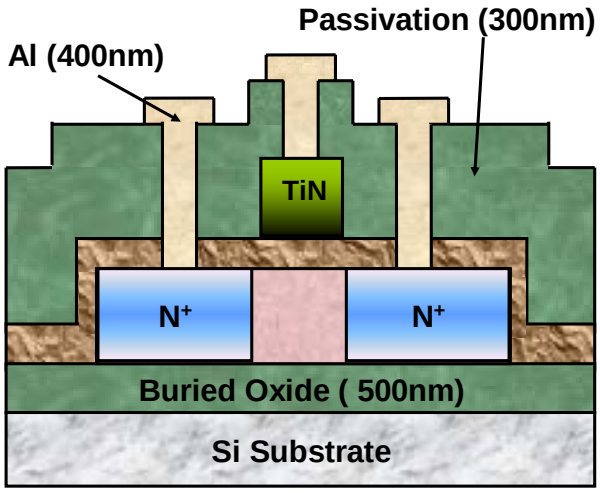


Fig. 3.1 Fabrication process of the combined TiN gate and Pr_2O_3 gate dielectric TFT with Fluorine ion implantation.

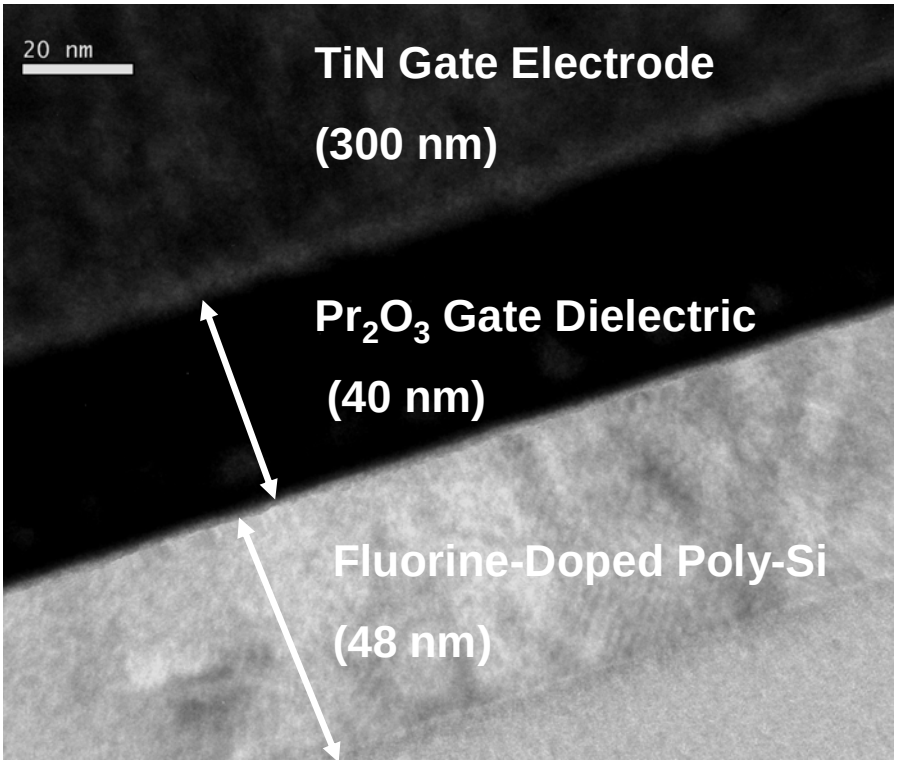


Fig. 3.2 Cross-section TEM image of the proposed high-κ Pr_2O_3 gate dielectric TFT structure.

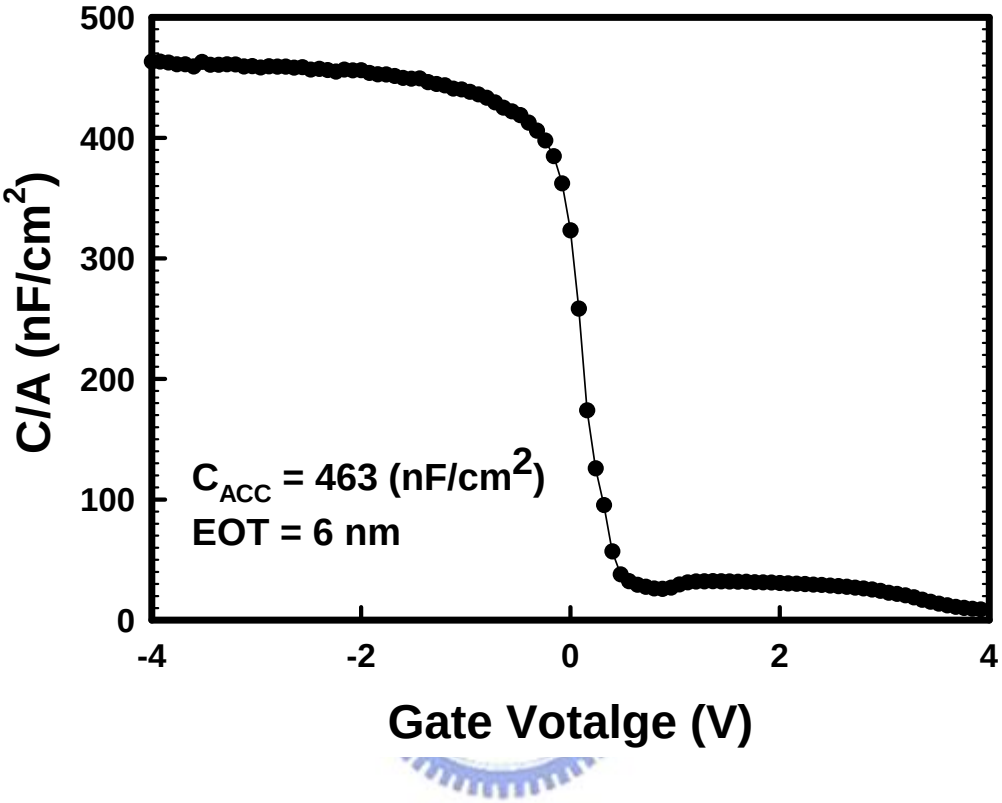


Fig. 3.3 C-V measurement of Pr_2O_3 capacitor

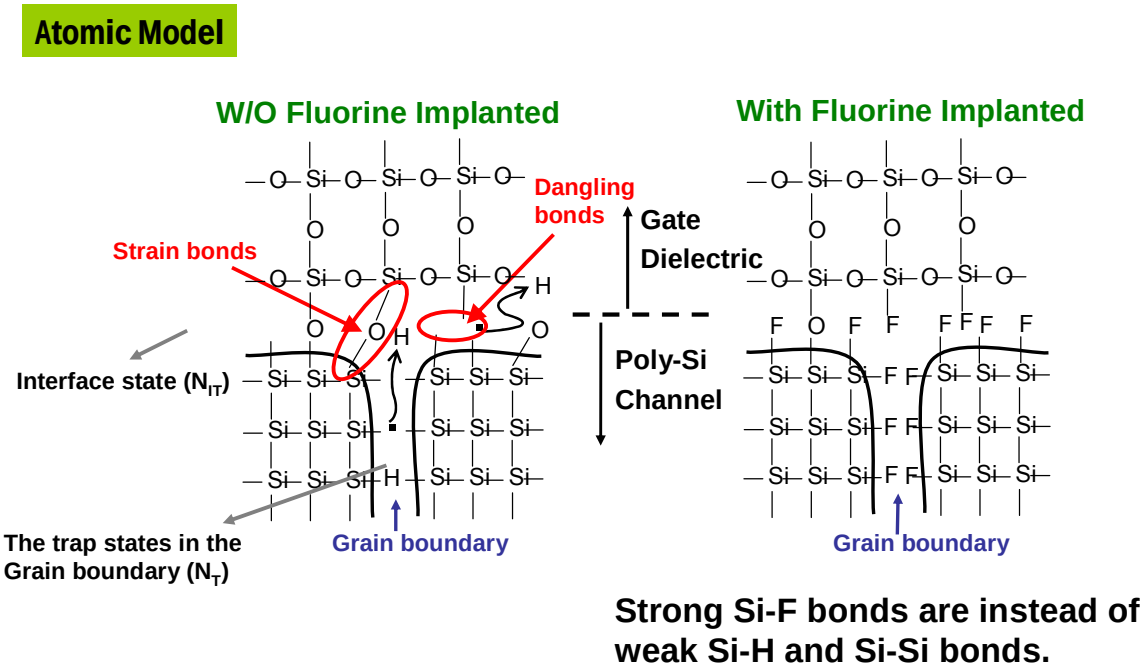


Fig. 3.4 Schematic cross-sectional view of SiO_2/poly-Si interface without Fluorine implanted and with Fluorine implanted treatment.

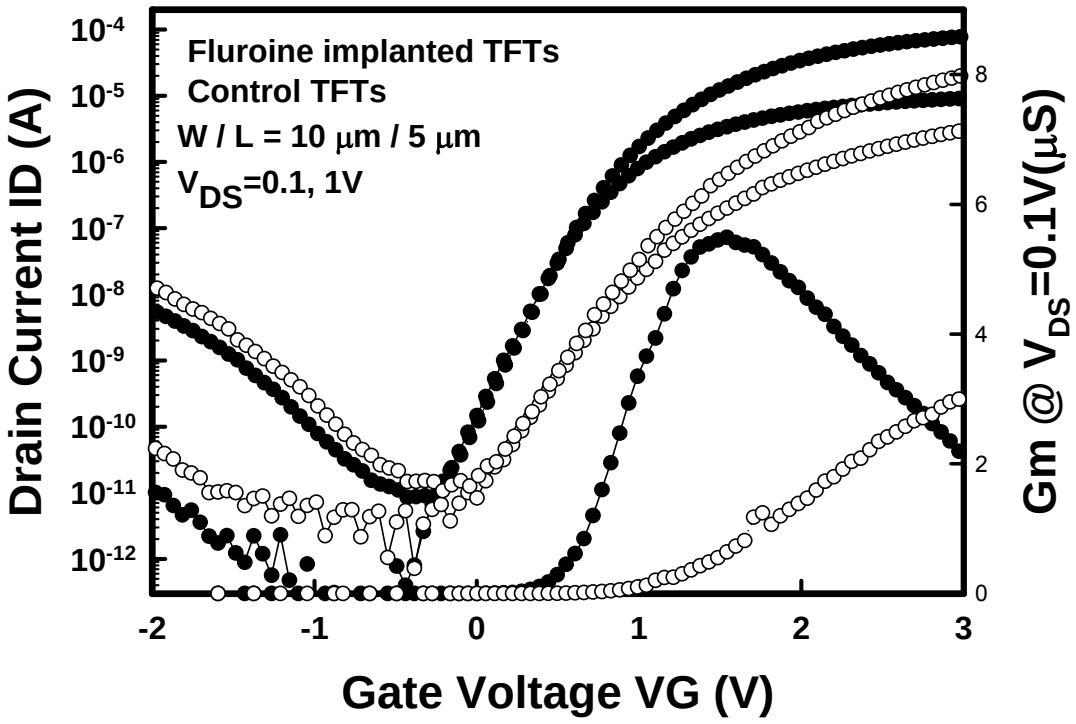


Fig. 3.5 Comparison of ID−VG characteristics for control TFTs and Fluorine implanted treated TFTs (W/L=10μm/5μm).

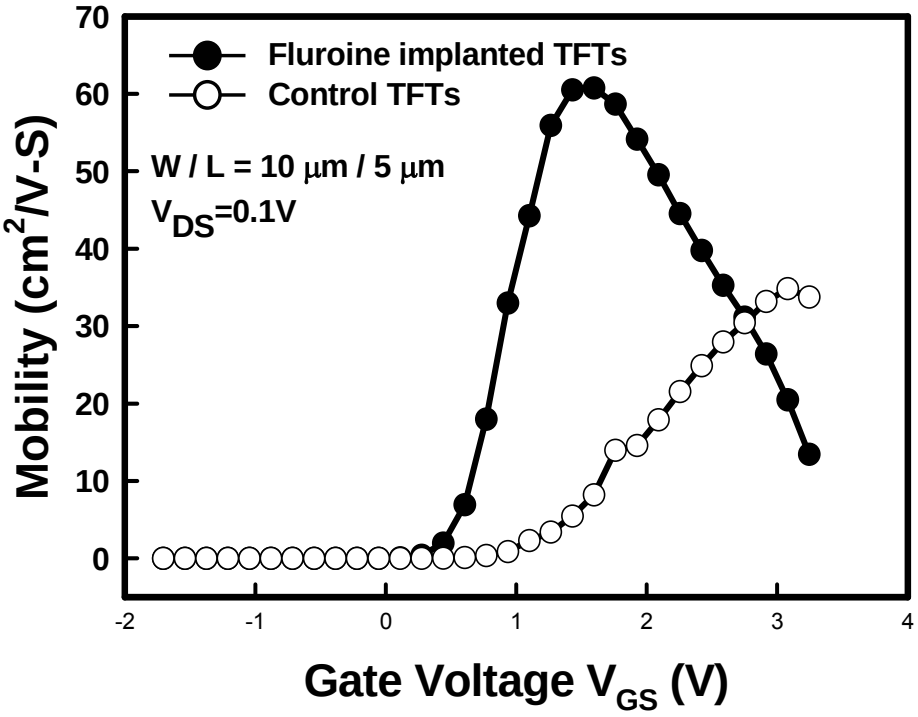


Fig. 3.6 Field-effect mobility of the control and fluorinated SPC poly-Si TFTs with V_{DS}=0.1

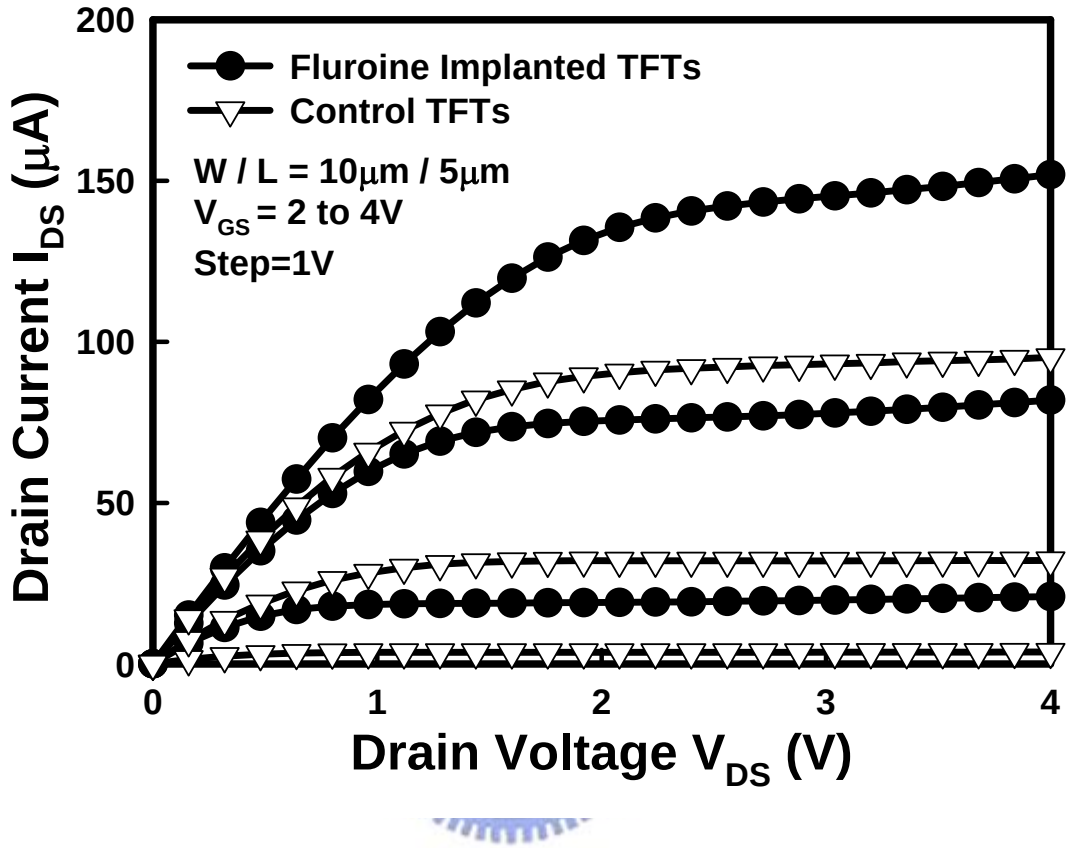
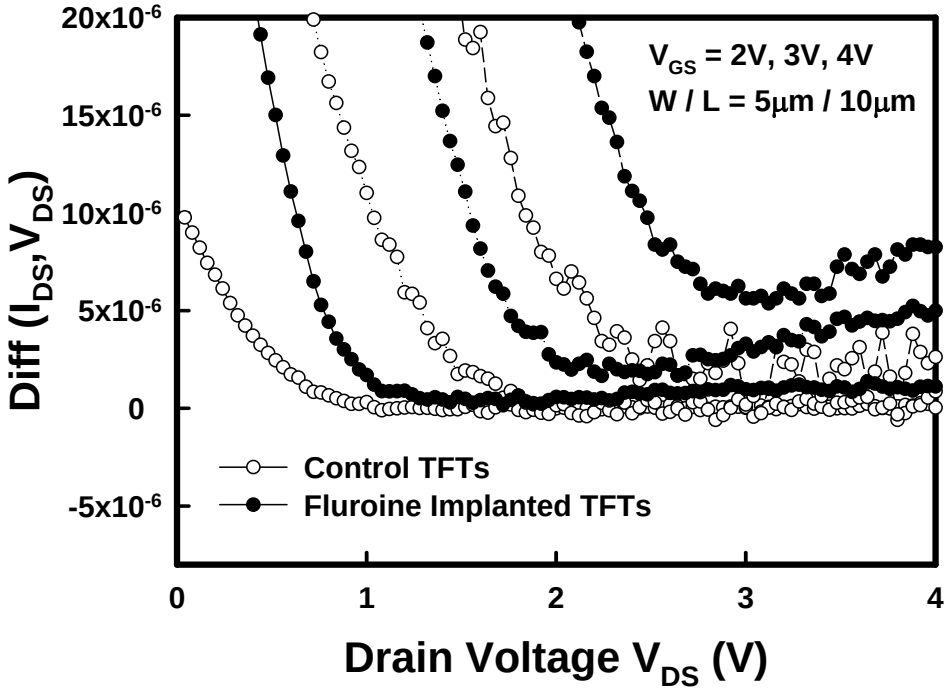
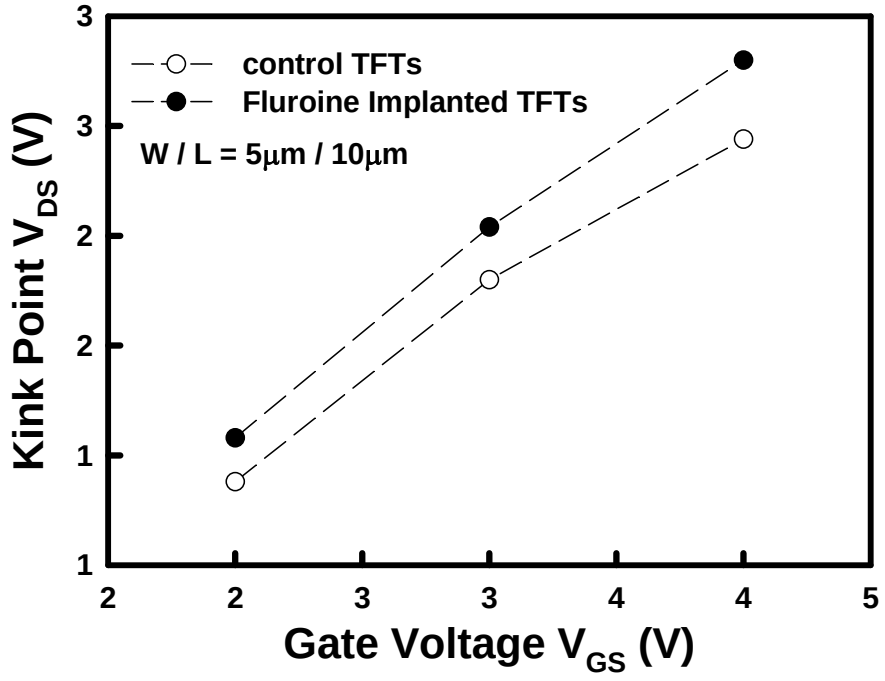


Fig. 3.7 Comparison of I_D−V_D characteristics for control TFTs and Fluorine implanted treated TFTs (W/L=10μm/5μm).



(a)



(b)

Fig. 3.8 (a) Differential (I_{DS},V_{DS}) versus Drain voltage (b) Kink-point of the control and fluorinated SPC poly-Si TFTs extracted from Fig. 3.9.

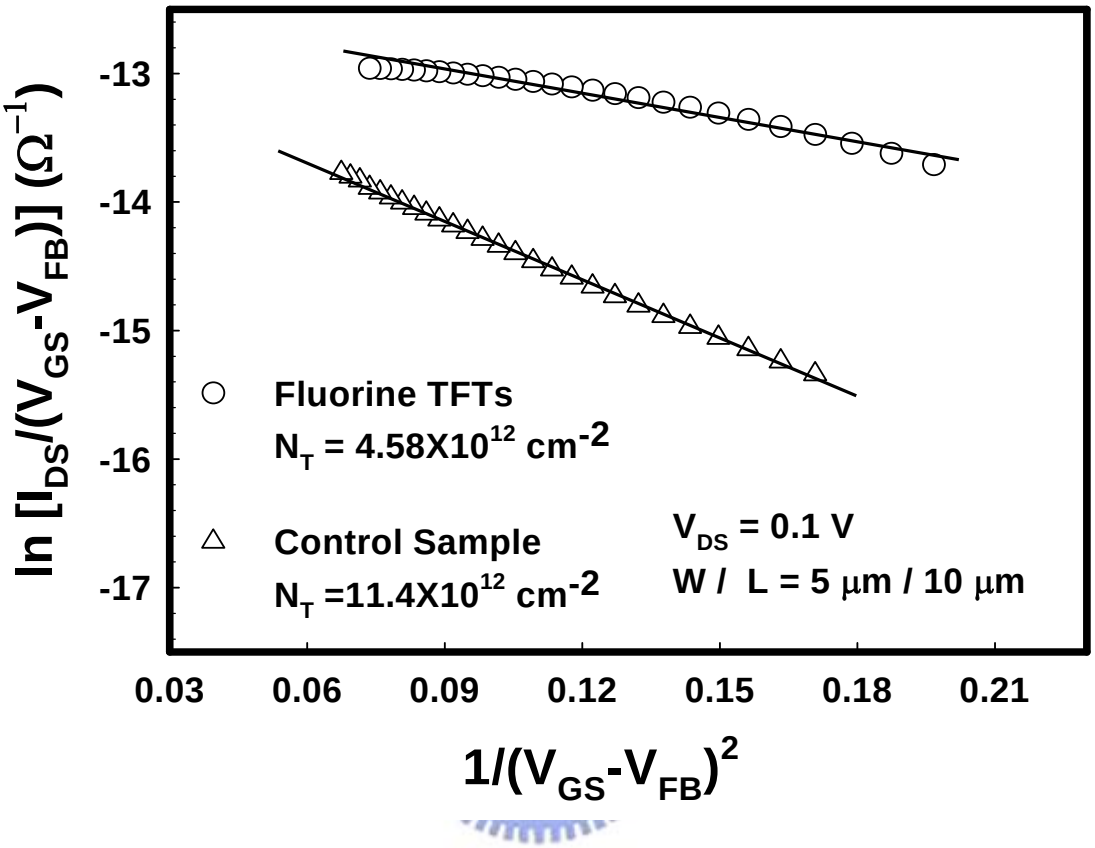


Fig. 3.9 $\ln[I_D/(V_{GS}-V_{FB})]$ versus $1/(V_{GS}-V_{FB})^2$ curves at V_{DS}=0.1V and high V_{GS} for control and fluorinated SPC poly-Si TFTs.

Key Parameters	Fluorine-implanted TFT	Control TFT	Enhancement
V_{TH} (V)	0.735	1.54	0.805
S.S. (mV/dec)	200	278	28%
μ_{FE} (cm^2/V-s)	61.6	43.6	41%
N_T (10^{12} cm^{-2})	4.58	14.4	68%
N_{IT} (10^{12} cm^{-2})	6.81	10.6	56%
I_{ON} / I_{OFF} ratio (10^6) (V_{DS}= 1V)	9.27	1.98	368%

Table. 3.1 Key device characteristics of the CF_4 plasma treated TFTs and control TFTs

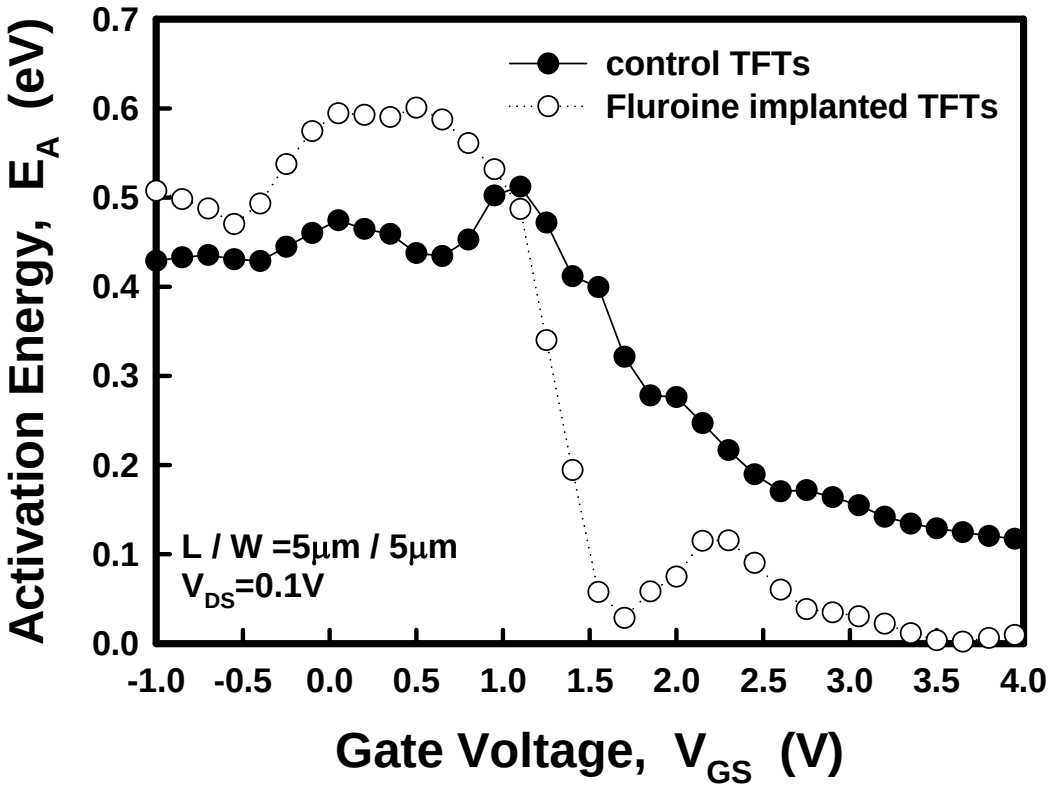


Fig. 3.10 Activation energy versus gate voltage of the control and fluorinated SPC poly-Si TFTs

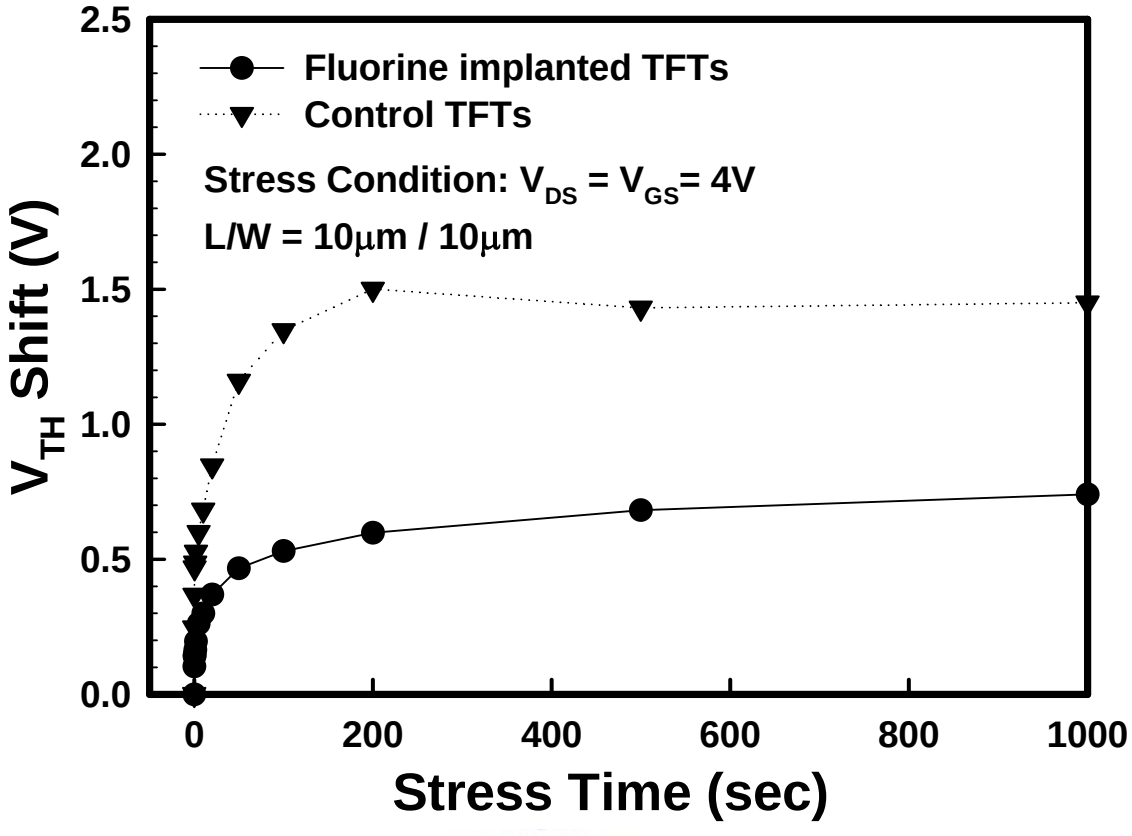


Fig. 3.11 Threshold voltage variation versus stress time for the control and Fluorine implanted treated TFTs.

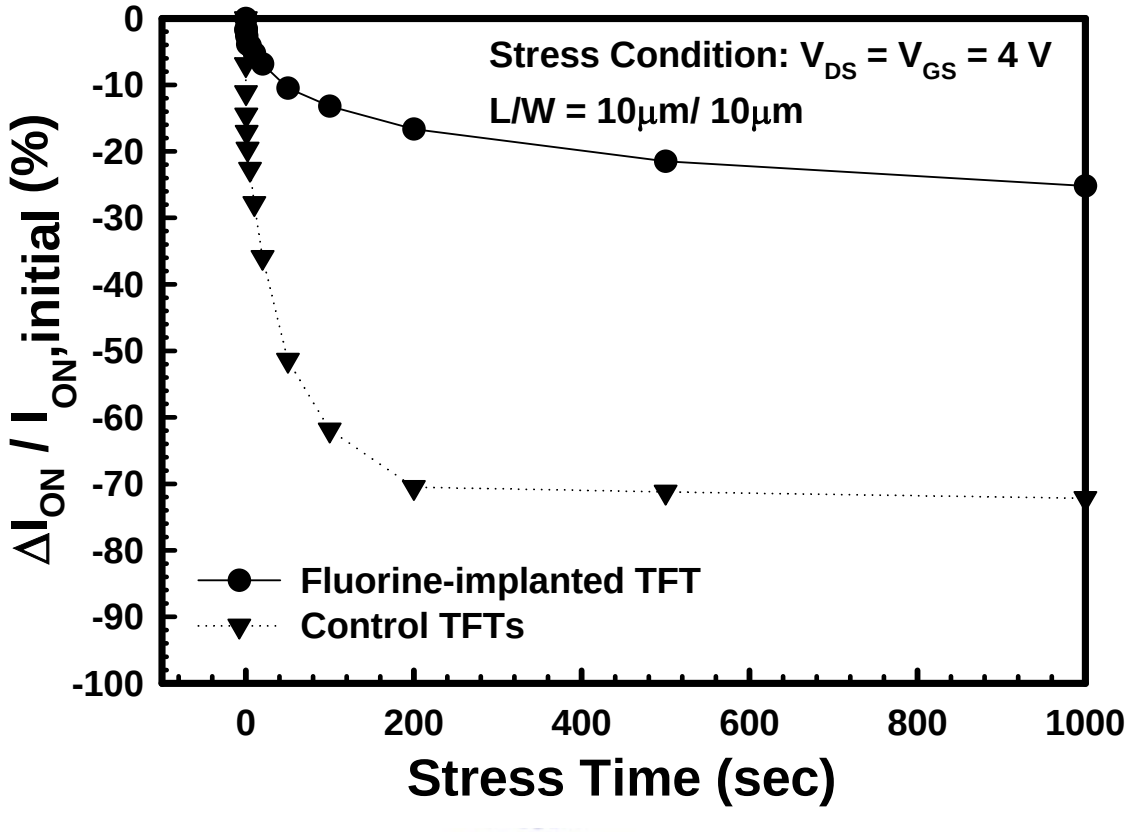


Fig. 3.12 On-current degradation versus stress time for the control and Fluorine implanted treated TFTs.

Chapter 4

Poly-Si TFTs with High-κ Pr_2O_3 Gate Dielectric under CF_4 Plasma Treatment

4.1 Introduction

In this thesis, we have performed the improvement of Fluorine implantation in chapter 3. Nevertheless, conventional ion implantation technique might be not suitable for large-sized glass substrate application, because of some complex process needed to perform such as an additional pad oxide deposition, and subsequent high temperature annealing that is required to activate the implanted atoms and recover the defect created by ion implantation. Furthermore, high-temperature process is not compatible with current production due to the low-melting point of low-cost glass substrate. Kim et al. demonstrated the use of fluorinated oxide (SiO_xF_y) to serve as a diffusion source [1-2]. However, an extra film deposition and etching are required.

To date, although hydrogen-based plasma treatments have been widely investigated in poly-Si TFTs, there is still a lack of a process-compatible technique to effectively introduce fluorine atoms into poly-Si films. In this chapter, we proposed a novel fluorine passivation technique by employing CF_4 plasma treatment, which is a simply and efficient process. To obtain which one condition is the optimal effect and avoid an unwanted etching effect, we controlled the RF to apply various powers from 10 to 20 Watts and very short time (15 seconds) to dissociate fluorine atoms, which were used to fluorinate the poly-Si film. Using this technique, an effective, low-cost, and process compatible fluorine-based plasma treatment on poly-Si was proposed. We

integrated a TiN metal gate and high-κ Pr_2O_3 gate dielectric TFTs with CF_4 plasma treatment to further improve the device characteristics for the first time and showed a negligible gate-dielectric hysteresis characteristics, a low Vth of 1.62 V, a low subthreshold swing of 241.4 mV/dec., a high field-effect mobility of 39.6 cm^2/Vs, a large ON/OFF current ratio of 9.76 x 10^6.

4.2 Experimental

The schematic diagram of the fabrication process are shown in Figure 4.1. The fabrication begins by depositing a 100-nm undoped amorphous silicon (α-Si) layer on a thermally oxidized Si wafer in a low-pressure chemical vapor deposition (LPCVD) at 550℃. Subsequently, solid phase crystallization (SPC) was performed at 600℃ for 24 hours in nitrogen ambient for the phase transformation from a-Si to poly-Si. Then active region were patterned and defined. Following a standard cleaning process, a CF_4 plasma treatment was performed at 350 °C for 15 seconds with pressure of 200 mtorr and power of 10 Watts and 20 Watts in plasma-enhanced chemical vapor deposition (PECVD) chamber. Next, a 35-nm Pr_2O_3 gate dielectric film was deposited by e-gun evaporation system, followed by a furnace annealing at 600 °C for 30 min in N_2 ambient to densify the gate dielectric quality. A 200-nm TiN film was sequentially deposited by physical vapor deposition (PVD), and then patterned to form gate electrode. A self-aligned phosphorous source/drain implantation was performed with the dosage and energy of 5E15 cm^{-2} and 70 keV, respectively. The dopant activation was performed at 600℃ furnace annealing at nitrogen ambient for 30min, followed by deposition of the 300nm passivation layer in PECVD chamber at 300 °C. Subsequently, the contact holes were opened by a two-step wet-etching process. First, the 300-nm

SiO_2 layer was etched away by buffered oxide etch (BOE) solution and then the Pr_2O_3 film was etched away by a H_2SO_4/H_2O solution, which has rather high selectivity of Pr_2O_3/SiO_2. Next, a 400nm-thick Aluminum electrode was deposited and patterned. Finally, N_2/H_2 sintering at 400℃ for 30 minutes were successively performed and no deliberate hydrogenation was performed, so that the "intrinsic" performance of the TFTs can be measured. For comparison, the control TFT without the CF_4 plasma treatment was prepared with the same process flow. The electrical and reliability characteristics were performed by using HP 4156B.

4.3 Result and Discussion

The proposed TiN metal gate and Pr_2O_3 gate dielectric TFT structure is confirmed by transmission electron microscopy (TEM), as shown in Figure 4.2 and the physical thickness of Pr_2O_3 is.34 nm. A thin equivalent-oxide thickness (EOT) of 6.6-nm is derived from the high gate capacitance density of 526 nF/cm^2 from capacitance-voltage (C-V) measurements, as shown in the Figure 4.3.

From the SIMS(secondary ion mass spectroscopy) of S-D Wang's paper [8],it exhibit the substantial amount of fluorine were introduced into the poly-Si layer by CF_4 plasma treatment, not carbon atoms and shows a notably high concentration of fluorine atoms piling up near the SiO_2/poly-Si interface, instead of in the deep poly-Si layer. These piled-up fluorine atoms is believed that they can provide more effective passivation of trap states, because the quality of SiO_2/poly-Si interface are the main issue for carrier transport. A strong signal of F bonds is detected in the CF_4 plasma treated sample. Also, Fourier Transform Infrared Spectroscopy (FTIR) spectra of the conventional and CF_4 plasma-treated poly-Si films are also shown in Figure 4.4. The spectra exhibit absorption peak corresponding to Si-F bonds and Si-O bonds centered

at round 930 and 1100cm^{-1}. The strong peak of Si-O bond is related to the SiO_2 substrate. These results indicated that by employing this CF_4 plasma treatment technique not only the fluorine atoms were introduced into the poly-Si but also the Si-F bonds were formed in the SiO_2/poly-Si interface.

According to Figure 3.6 in Chapter 3, trap states in both grain boundaries and the SiO_2/poly-Si interface were also reduced by using CF_4 plasma treatment, which resulting the great improvement in the device performance. It is suggested that strong Si-F bonds replace the dangling and strain bonds for the fluorinated poly-Si films, and thus improve the device performance.

Figure 4.5 shows the typical I_{DS}-V_{GS} transfer characteristics for the proposed CF_4 plasma-treated TFT and control TFT. The measurements were performed at two different drain voltage of V_{DS}=0.1 and 2V. The devices have a drawn channel length (L) of 5 μm and a channel width (W) of 10 μm, respectively. According to the method of parameter extraction in Chapter 1, the Vth and S.S. of the fluorinated poly-Si TFT were found to be 1.62V and 241mV/dec. extracted from Figure 4.5, which are superior to those of the control one(1.94V and 335mV/dec.). Moreover, the extracted field effect mobility calculated from the value of transconductance at V_{DS} = 0.1 V is also shown. As can be seen, the CF_4 plasma-treated sample shows approximately 46% enhancement in the field effect mobility. The major reason for the superior device performance in CF_4 plasma-treated sample is that the deep trap states near midgap associated with the Si dangling bonds and the tail states near the band edge caused by the strain bonds in poly-Si and SiO_2/poly-Si interface are well-passivated by the incorporation of fluorine ions. Also, the leakage current of the CF_4 plasma-treated TFT is lower than that of the control TFT, especially at the more negative gate bias. It has been reported that the deep trap states can be eliminated effectively by using

fluorine passivation, leading to a reduced gate-induced drain leakage (GIDL) from the field-enhance-emission via trap states under a high electric field [3]. The mechanism is discussed in Chapter 3. Additionally, the ON/OFF current ratio of the CF_4 plasma-treated TFT ($9.76x10^6$) is approximately two times larger than that of the control TFT ($4.06x10^6$).

Figure 4.6 shows the typical I_{DS}-V_{DS} output characteristics for the integrated TiN gate and Pr_2O_3 gate dielectric with CF_4 plasma-treated TFTs and control TFTs. The devices have a drawn channel length (L) of 5 μm and a channel width (W) of 10 μm, respectively. Clearly, the driving current of CF_4 plasma-treated TFT is larger than that of control TFTs at V_{DS} = 4V and V_{GS}=5V. This is due to the higher mobility and smaller threshold voltage of the fluorinated poly-Si TFT. This large driving capability is desirable for high-speed display IC's application resulted from the high gate capacitance density.

Figure 4.7 shows that the kink-point voltage (i.e. the voltage of kink-effect (also named "floating-body effect) occurred) versus different gate voltage extracted from Figure 4.6, and the phenomenon is the same as in Chapter 3. By CF_4 plasma treatment, the kink-effect can be reduced owing to the decrease of the trap state which is the location usually occurred impact ionization in the poly-Si bulk, and then the kink-point voltage will be raise as shown in the Figure 4.7.

The grain boundary trap state densities (N_T) of the conventional and fluorinated high-κ gate dielectric poly-Si TFTs were estimated by Levison and Proano method [4-5] and we have demonstrated in Chapter 1. Figure 4.8 exhibits the plots of the $\ln[I_D/(V_{GS}-V_{FB})]$ versus $1/(V_{GS}-V_{FB})^2$ curves at low V_{DS} and high V_{GS}. The fluorinated Pr_2O_3 high-κ gate dielectric poly-Si TFT exhibits a Nt of 9.44×10^{12} cm-2, whereas the control TFT has 13.5×10^{12} cm-2. This result implies that the CF_4 plasma

treatment can terminate the grain boundary trap state in the poly-Si film. To further study the fluorine passivation effect near the interface, the effective interface trap states densities (N_{IT}) near the SiO_2/poly-Si interface were also calculated. Form Chapter 1, we have known the effective interface trap states density equation which can be expressed as: $N_{IT}=[(S.S./ln10)(q/KT)-1](Cox/q)$. The N_{IT} of the W/O CF_4 plasma TFT and the 10W CF_4 plasma TFT are 15.2×10^{12} cm-2 and 10×10^{12} cm-2, respectively. The value of grain boundary trap state densities (N_{IT}) reflects trap states near the SiO_2/poly-Si interface.

The key parameters were summarized in Table 4.1. From Table 4.1(a), comparing with conventional TFTs, the TFT by utilizing CF_4 plasmas with RF power of 10 Watts is performed prior high-κ deposition, Vth decreased from 1.94V to 1.62V, S.S. decreased from 335 mV/dec to 241 mV/dec, Ion/Ioff at V_{DS}=2V increased from. 4.06×10^6 to 9.76×10^6, grain boundary traps densities decreased from 13.5×10^{12} cm^{-2} to 9.44×10^{12} cm^{-2}, and interface trap states decreased from 15.2×10^{12} cm^{-2} to 10×10^{12} cm^{-2}. However, as can be seen from Table 4.1(b), the electrical performance including threshold voltage, subthreshold swing, and field-effect mobility would degrade as the RF power increased to 20 Watts. These parameters are extracted from Figure 4.9 which performs the typical I_{DS}-V_{GS} transfer characteristics for the 10 Watts, 20Watts CF_4 plasma-treated TFT and control TFT. These measurements were performed at drain voltage V_{DS}=0.1 and the devices have a drawn channel length (L) of 1μm and a channel width (W) of 1μm, respectively. The degradation may be attributed to the moisture absorption and CF_4 plasma-induced etching damage. According to previous report, the plasma-induced degradation and absorbed moisture would easily form OH and then react with fluorine to form HF, which in turn deteriorate the poly-Si channel [6] Therefore, the segregated fluorine ions within the poly-Si channel will not

passivate the trap states but generate additional defect states to degrade the devices performance and reliability as the RF power reaches to 20W.

Measurements of the I_{DS}–V_{GS} characteristics are performed on all the devices for temperatures varying from 25 to 105 °C in order to extract the variations of the activation energy of the drain current as shown in Figure 4.10. Activation energy expresses the index of carrier transport capability, which associates with the barrier height of carrier flow in fthe poly-Si channel [7]. The activation energy of the drain current in CF_4 plasma treated-TFT is found to be higher under the off-state and lower under the on-state as compared to control TFT, implying that CF_4 plasma treatment alters the trap state density. That is to say, for fluorinated poly-Si TFT, fluorine atoms can passivate the trap states and hence reduce the barrier height for carrier transport when device is turned on. On the other hand, in Off-region fewer trap states after fluorinating process resulting in the increasing of Ea and thus the trap-assisted leakage current is suppressed. Moreover, in the subthreshold region, a steeper profile can be found for the fluorinated TFT, which proves that the interface quality of the fluorinated TFT is much better than that of the control TFT.

Additionally, the hot carrier stress was carried out to examine the reliability pf the device. The mechanism of the reliability degradation is also discussed in Chapter 2. The stress condition is applied at $V_D = V_G = 4$ V for 1000 s to examine the electrical reliability. The threshold voltage variations and the on-current degradation are shown in Figure 4.11 and Figure 4.12. The variation of I_{ON} and V_{TH} were defined as (V_{TH},stressed-V_{TH},initial) and (I_{ON},stressed - I_{ON},initial)/ I_{ON},initial×100 (%), respectively, where V_{TH},initial, I_{ON},initial and V_{TH},stressed, I_{ON},stressed represent the measured values before and after stress. As can be seeen, the CF_4 plasma treated TFTs have high immunity against the hot carrier stress as compared to control TFTs. We

deduce that the significant improvement in the electrical reliability is attributed to the formation of stronger Si–F bonds in place of weaker Si–Si and Si–H bonds in the poly-Si channel and at the Si/SiO_2 interface, and the result is the same as the Chapter 3. Hence, CF_4 plasma treatment can obtain an excellent electrical characteristic and reliability as wonderful as Fluorine implanted treatment.

4.4 Summary

Integrating poly-Si TFTs with TiN and Pr_2O_3 as gate electrode and gate dielectric, respectively, which yield thin EOT and high gate capacitance density are demonstrated for the first time. Moreover, a simple, low cost and effective CF_4 plasma treatment technique with an optimum RF power of 10 Watts is proposed to improve extremely the electrical characteristics. Significant improvements in devices performance and reliability are obtained, speculatively thanks to the terminated Si dangling bonds by CF_4 plasma passivation and the formation of Si-F bonds in place of the weaker Si-Si and Si-H bonds within the poly-Si film. We have successfully combined a CF_4 plasma pretreatment, TiN metal gate, and Pr_2O_3 gate dielectric to fabricate high-performance poly-Si TFTs, potentially suitable for AMLCD application.

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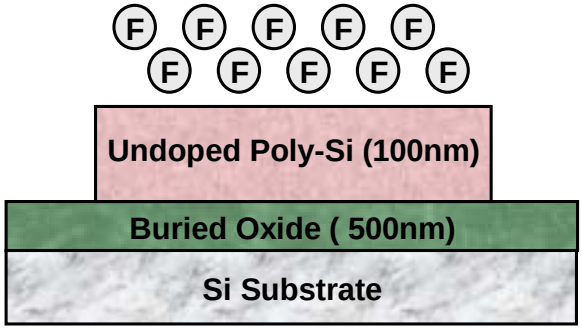
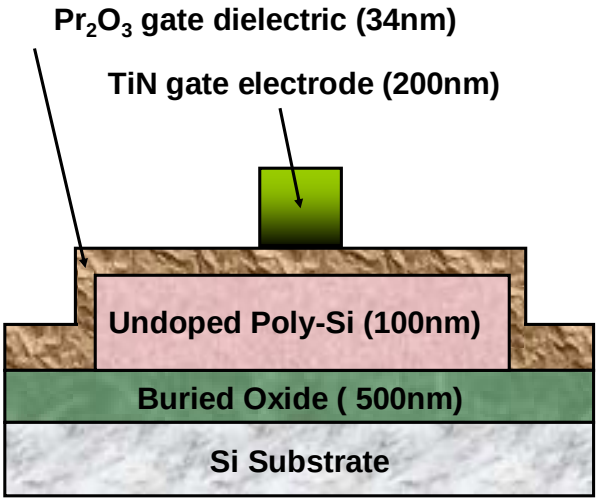
CF4 plasma process

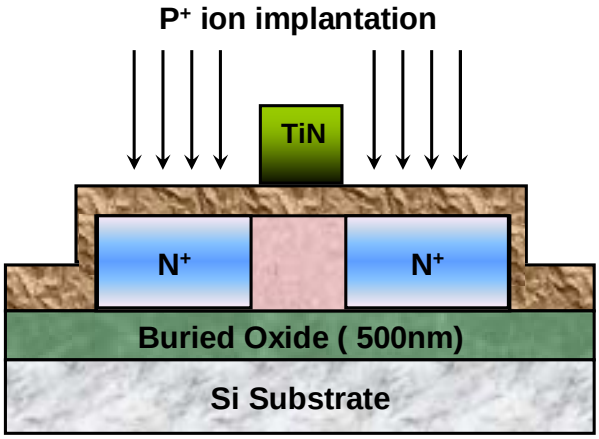
- 500-nm thermal oxidation at 980°C
- 100-nm α-si deposition at 550°C by LPCVD
- SPC at 600°C for 24h in N_2 ambient (α-Si ➔ poly-Si)
- Define active region
- CF4 plasma at 350 °C for 15 sec 200 mtorr with 10W、20W



- 34-nm Pr2O3 film deposition by e-gun evaporation system
- Furnace annealing at 600°C for 30 min in N2 ambient
- 200-nm TiN film by PVD
- Define gate electrode



- **Self-aligned source/drain implantation (P^+ $5x10^{15}$ 90keV)**
- **Dopant activation at 600°C for 30min in N_2 ambient**



- **300-nm passivation oxide SiO_2 by PECVD**
- **Define contact hole, two-step wet-etching process**
- **400-nm Al pads**
- **N_2/H_2 sintering at 400°C for 30min**

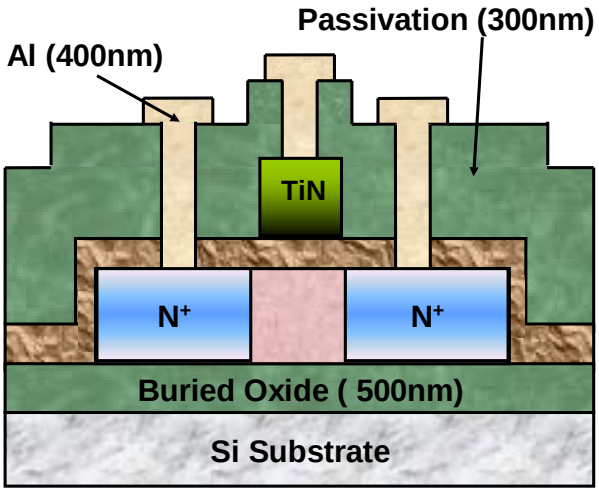


Fig. 4.1 Schematic diagram of the combined TiN gate and Pr_2O_3 gate dielectric TFT with CF_4 plasma treatment.

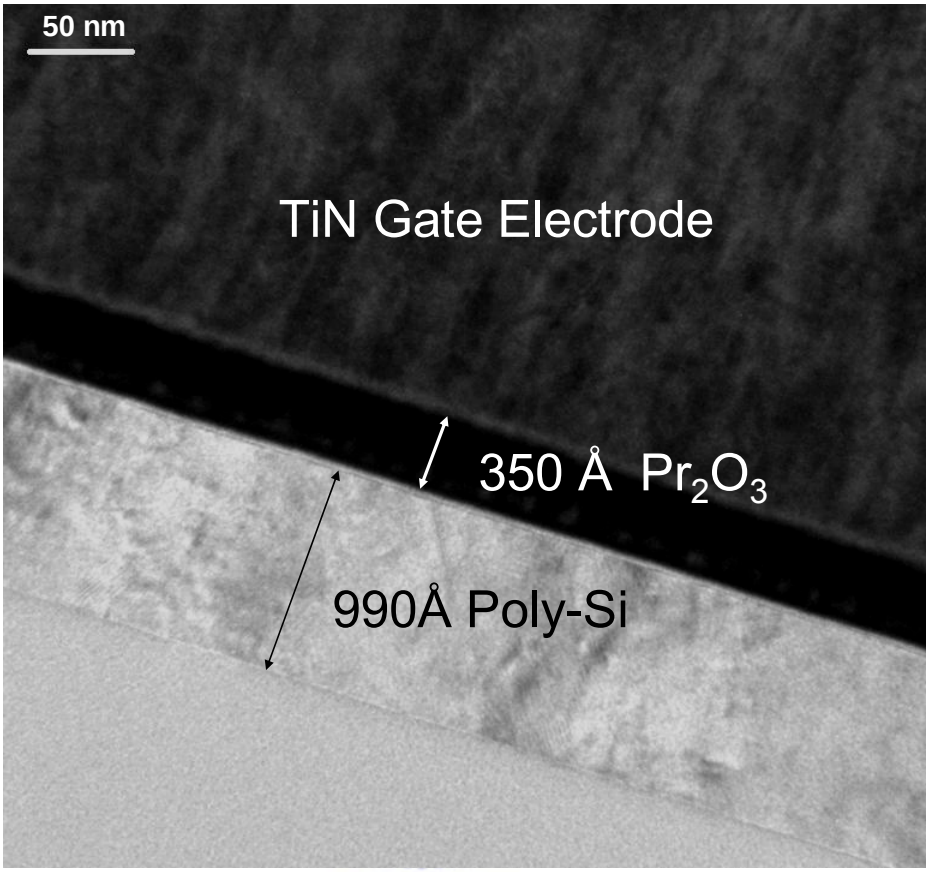


Fig. 4.2 Cross-section TEM image of the proposed high-κ Pr_2O_3 gate dielectric TFT structure.

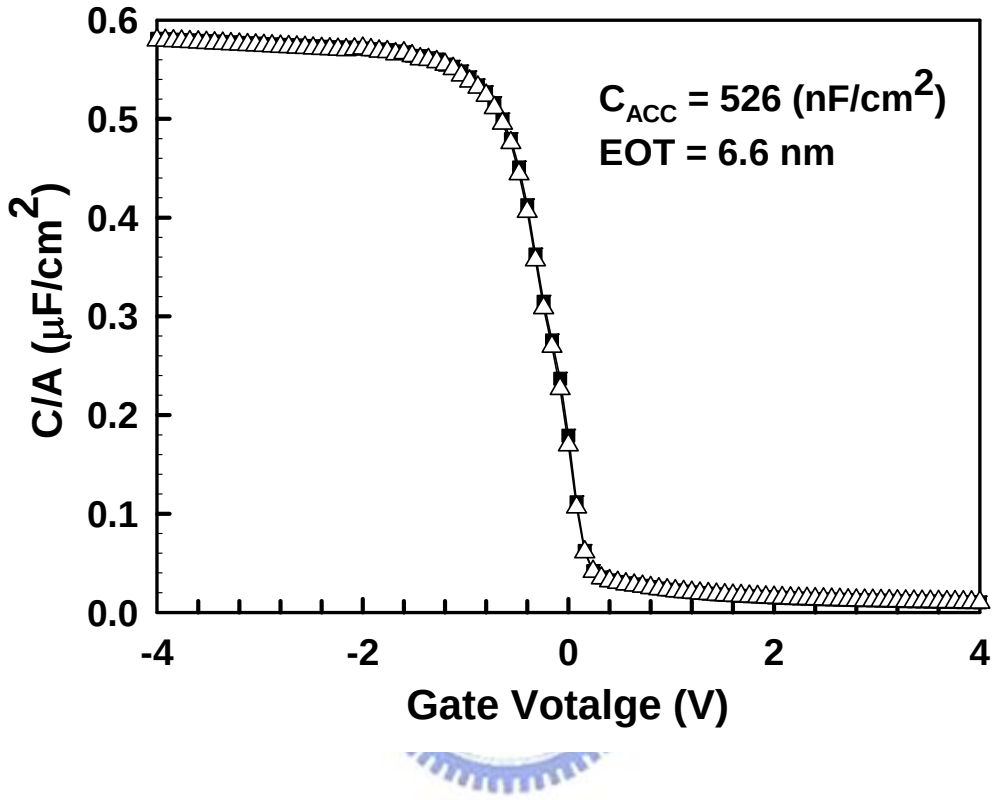


Fig. 4.3 C-V measurement of Pr_2O_3 dielectric capacitor.

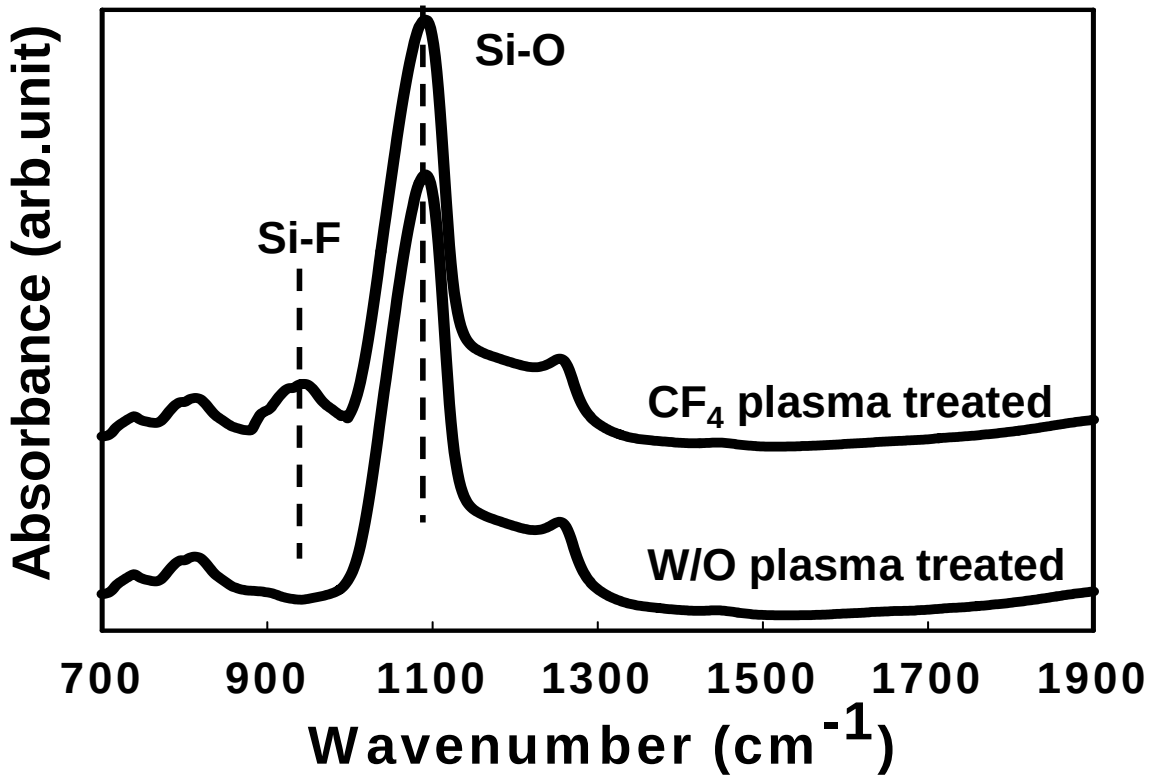


Fig. 4.4 FTIR spectra of the conventional and the CF_4 plasma-treated high-κ gate dielectric poly-Si films.

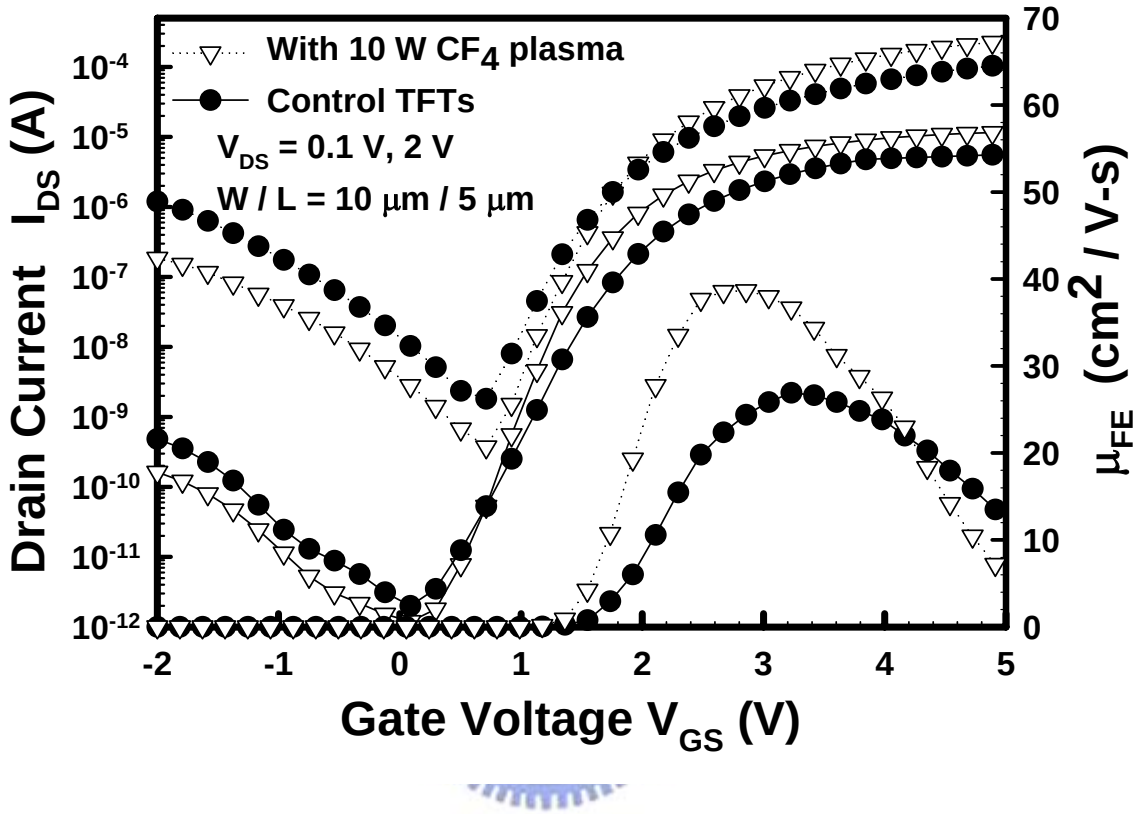


Fig. 4.5 Comparison of I_{DS}−V_{GS} characteristics and mobility for control TFTs and CF_4 plasma treated TFTs (W/L=10μm /5μm).

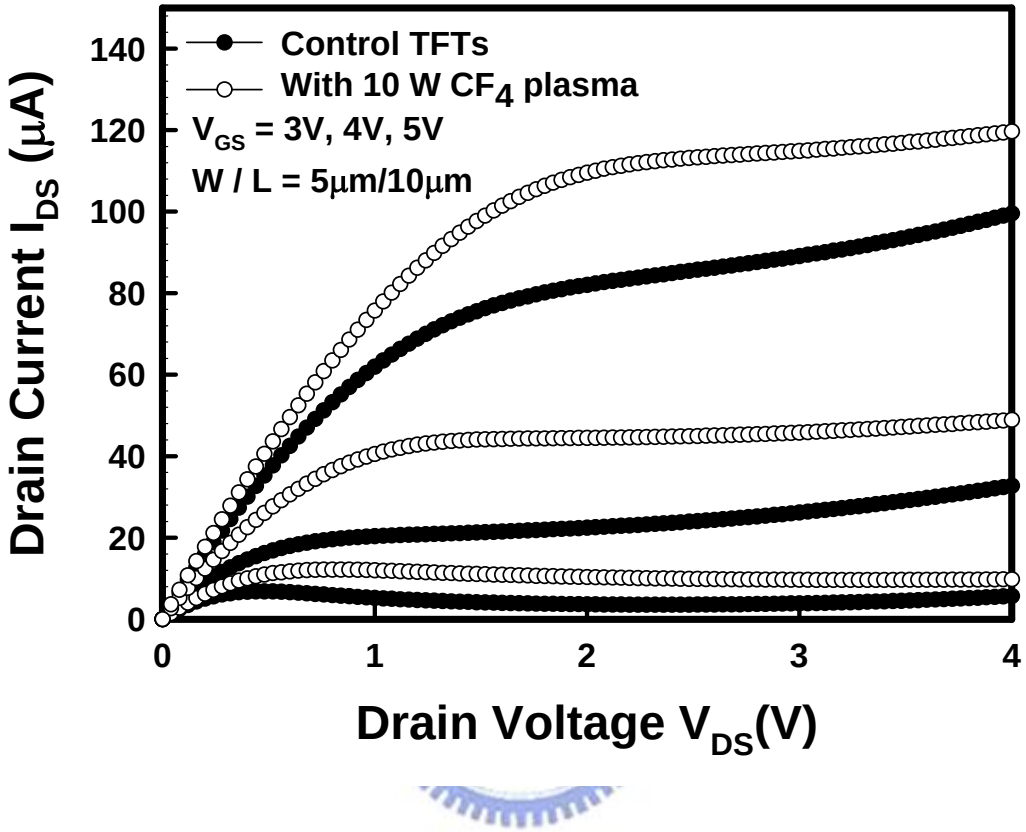
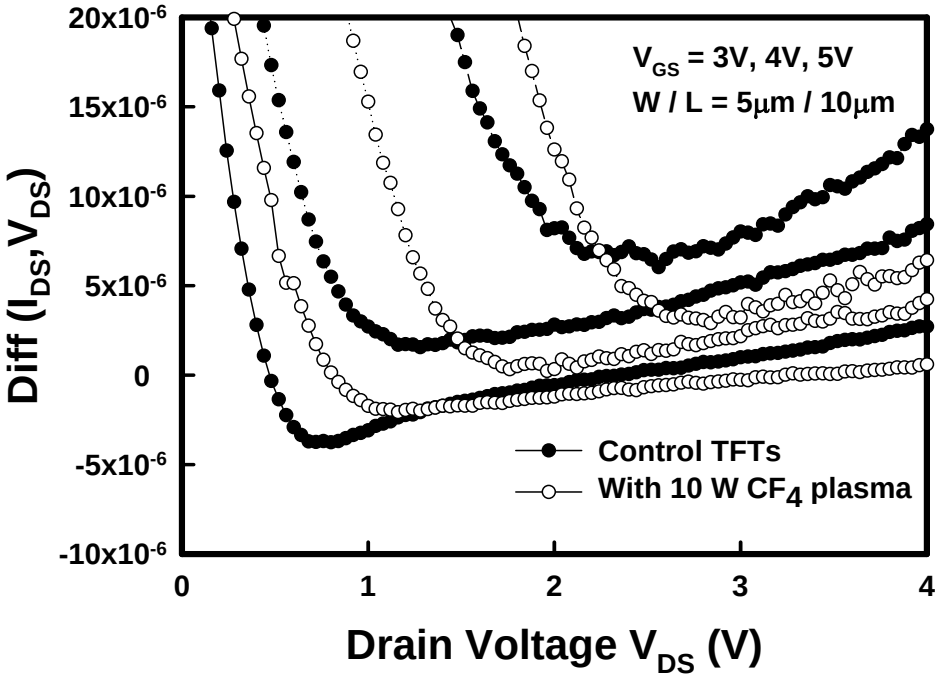
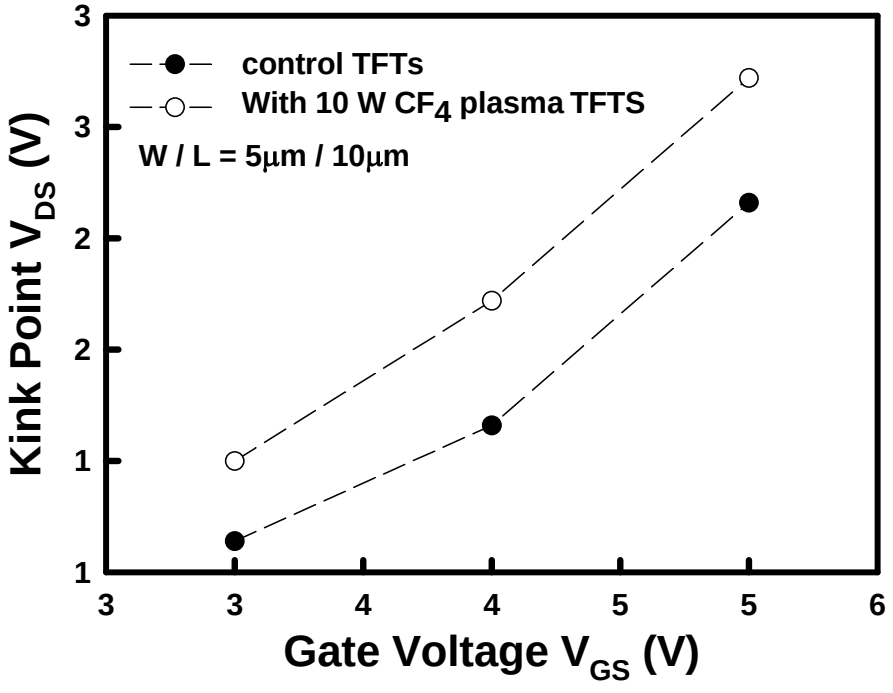


Fig. 4.6 Comparison of I_D−V_D characteristics for control TFTs and CF_4 plasma treated TFTs (W/L=1μm/1μm).



(a)



(b)

Fig. 4.7 (a) Differential (I_{DS},V_{DS}) versus Drain voltage (b) Kink-point of the control and fluorinated SPC poly-Si TFTs extracted from Fig. 4.7

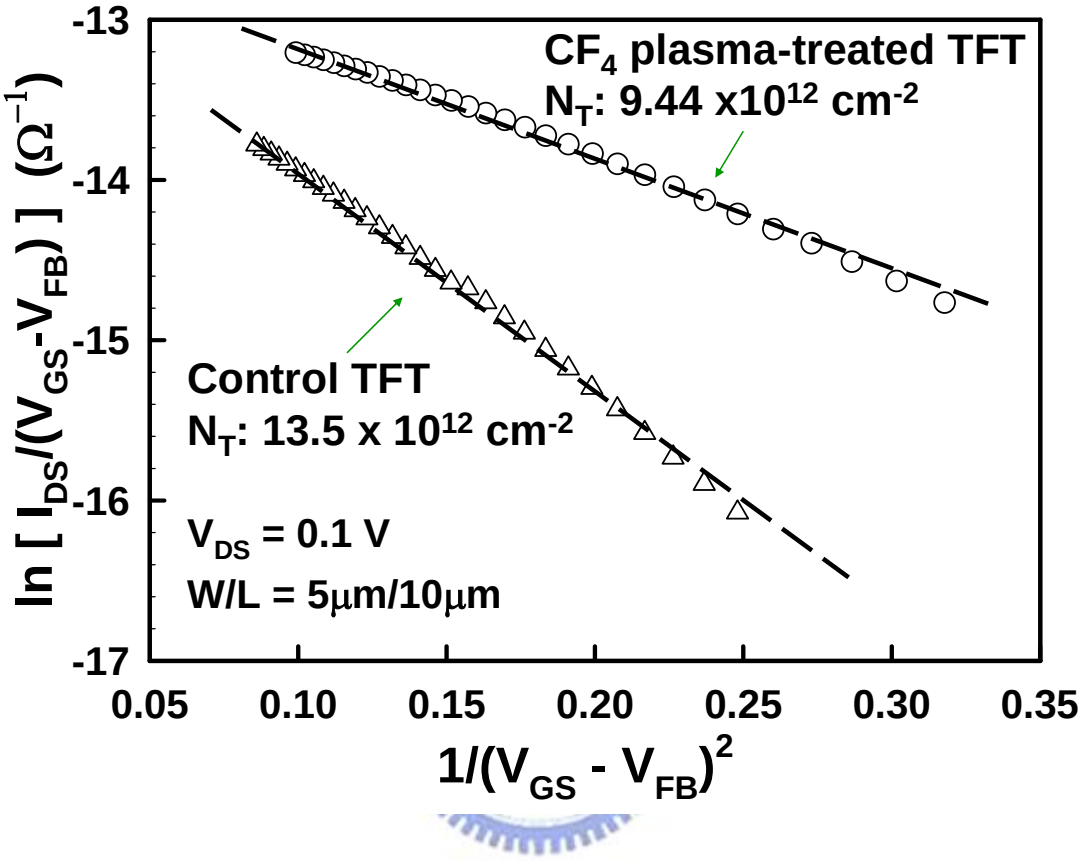


Fig. 4.8 $\ln[I_D/(V_{GS}-V_{FB})]$ versus $1/(V_{GS}-V_{FB})^2$ curves at V_{DS}=0.1V and high V_{GS} for control and fluorinated SPC poly-Si TFTs.

Key Parameters	10W CF_4 plasma	W/O CF_4 plasma	Enhancement
W/L (μm)	10/5	10/5	X
V_{TH} (V)	1.62	1.94	0.32
S.S. (mV/dec)	241	335	28%
μ_{FE} (cm^2/V-s)	39.6	27.1	46%
N_T (10^{12} cm^{-2})	9.44	13.5	30%
N_{IT} (10^{12} cm^{-2})	10	15.2	34%
I_{ON} / I_{OFF} ratio (10^6) (V_{DS}= 2V)	9.76	4.06	140%

(a)

Key Parameters	10W CF_4 plasma	20W CF_4 plasma	W/O CF4 plasma
W/L (μm)	1/1	1/1	1/1
V_{TH} (V)	1.59	2.23	1.92
S.S. (mV/dec)	213	335	283
μ_{FE} (cm^2/V-s)	42.13	18.82	28. 33
N_T (10^{12} cm^{-2})	9.3	25.3	13.8
N_{IT} (10^{12} cm^{-2})	8.54	15.2	12.3
I_{ON} / I_{OFF} ratio (10^6) (V_{DS}= 1V)	6.5	2.21	4.63

(b)

Table. 4.1. (a) Key device characteristics of the CF_4 plasma treated TFTs with 10W and control TFTs (W/L=10μm/5μm) (b) Comparison of 10W, 20W and control sample (W/L=1μm/1μm)

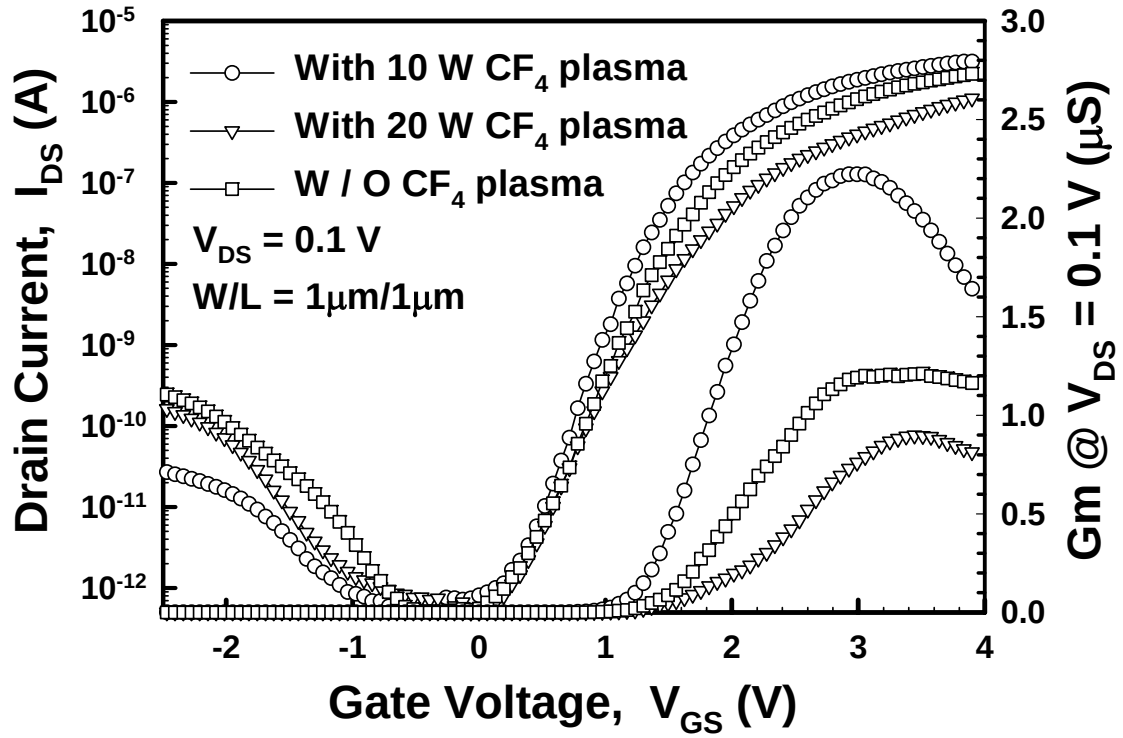


Fig. 4.9 Comparison of I_{DS}−V_{GS} characteristics for control TFTs and CF_4 plasma treated TFTs at V_{DS}=0.1V with 10 Watts and 20 Watts (W/L=1μm /1μm).

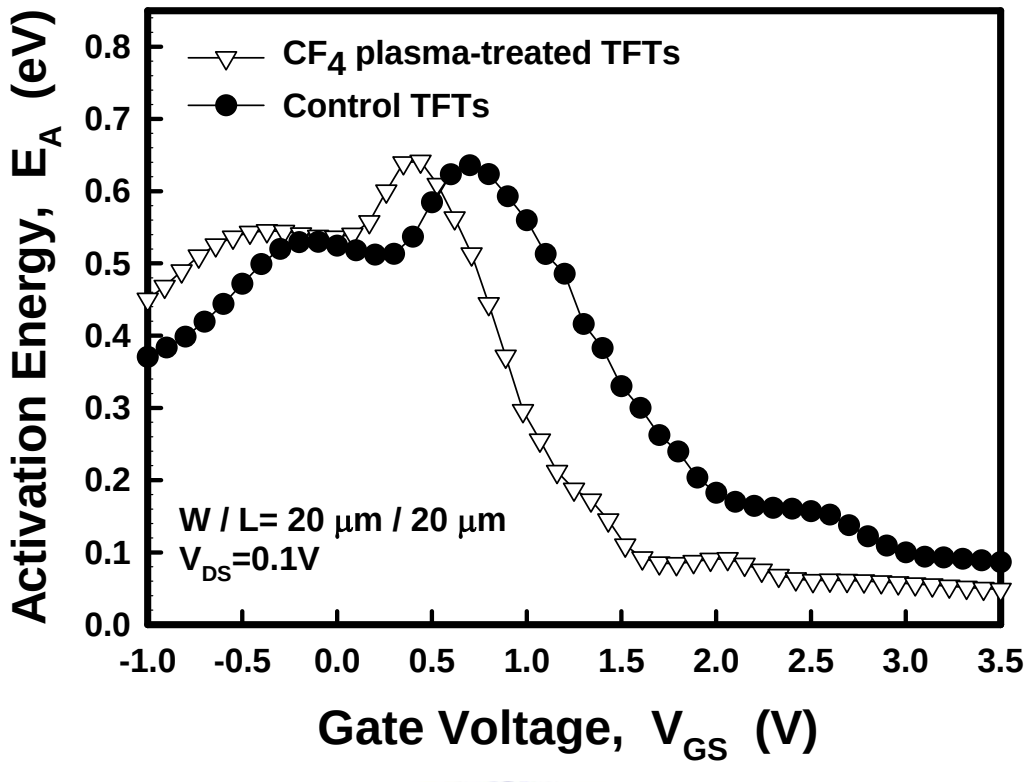


Fig. 4.10 Activation energy versus gate voltage of the control and fluorinated SPC poly-Si TFTs

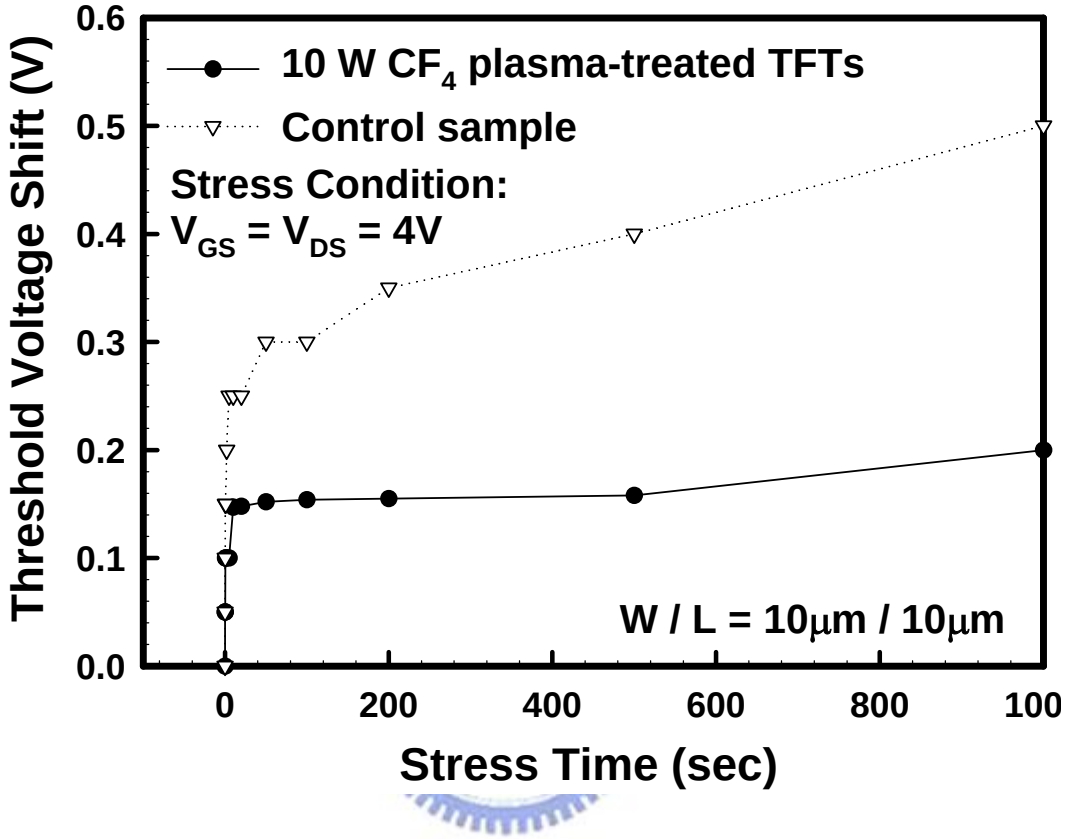


Fig. 4.11. Threshold voltage variation versus stress time for the control and CF_4 plasma treated TFTs.

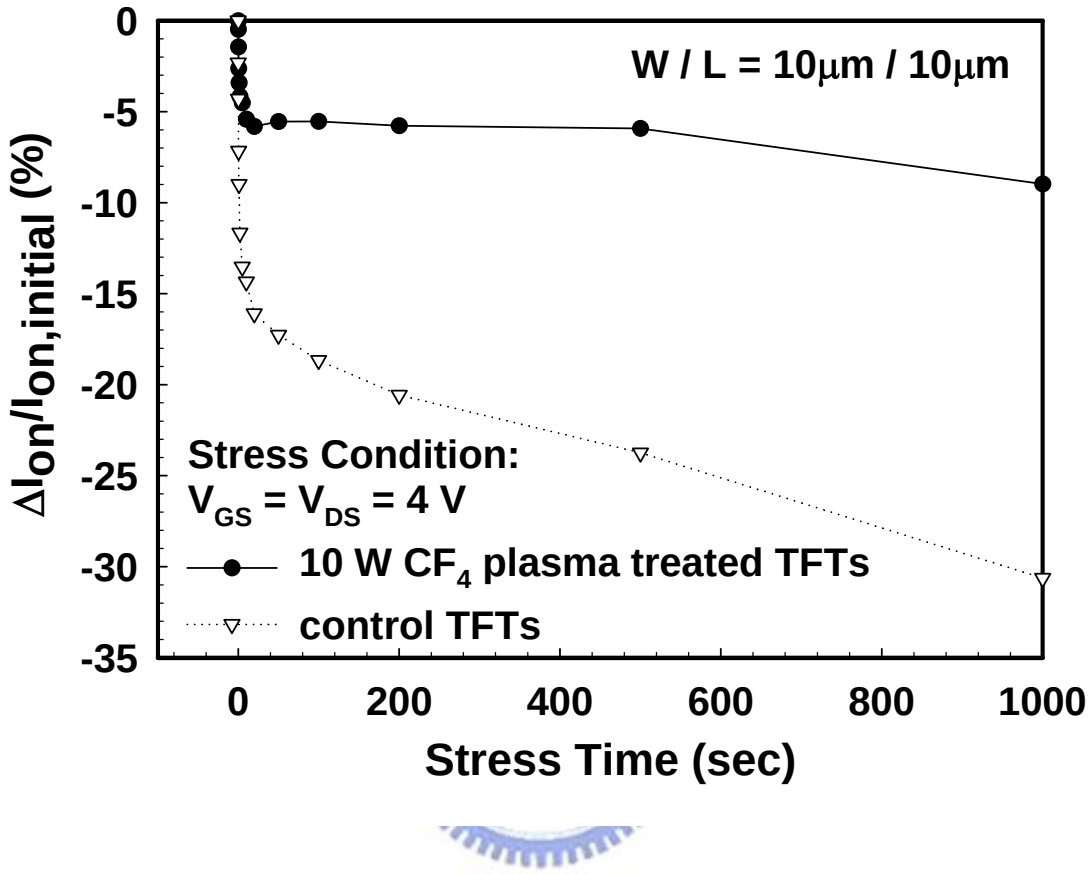


Fig. 4.12 On-current degradation versus stress time for the control and CF_4 plasma treated TFTs.

Chapter 5

Conclusions and Future Works of the Thesis

5.1 Conclusions

In this thesis, we compare the high-κ Pr_2O_3 material with conventional TEOS, and perform the advantage of the high-κ Pr_2O_3 material. Then, Fluorine implantation were utilized to improve the electrical characteristic and reliability of SPC poly-Si TFTs. Finally, using the novel CF_4 plasma treatment technique, significant improvements in the performance of fluorinated SPC poly-Si TFTs are presented. The main results of these studies are summarized as below:

In Chapter 2, utilizing the high-κ Pr_2O_3 as gate dielectric performs significant improvements in the device performance, including lower threshold voltage, improved subthreshold swing, higher field effect mobility, and enhanced ON/OFF current ratio are realized as compared to the TEOS poly-Si TFTs, owing to the high gate capacitance density and its good gate dielectric property of lower leakage current density.

In Chpater 3, utilizing fluorine ion implantation to passivate the dangling bonds in the grain boundaries and relax the strain bonds in the interface state, we can obtain the significant improvements in the device performance. Furthermore, the fluorine-doped poly-Si TFTs also improves the hot-carrier immunity due to the stronger Si-F bond than Si-Si bond and Si-H bond. Therefore, Fluorine-implanted technique with high-κ Pr_2O_3 gate dielectric is a good candidate to improve the device

performance and reliability of poly-Si TFTs.

In Chapter 4, utilizing an novel CF_4 plasma treatment to passivate the trap states is also the other way to improve the performance and reliability. The principle of improvement is the same as Fluorine-implanted technique in Chapter 3. However, ion implantation may not be suitable for large-size glass substrate due to high temperature annealing to active the implanted atoms. Therefore, a simple, low cost and effective CF_4 plasma treatment technique with an optimum RF power of 10 Watts is proposed to improve extremely the electrical characteristics such as threshold voltage, subthreshold swing, field effect mobility, and ON/OFF current ratio and so on. We have successfully combined a CF_4 plasma pretreatment, TiN metal gate, and Pr_2O_3 gate dielectric to fabricate high-performance poly-Si TFTs, potentially suitable for AMLCD application.

5.2 Future Works

5.2.1 Integrate Various Device Structures in Pr_2O_3 TFT

In Chapter 2, we found that the Pr_2O_3 TFTs exhibit undesirable gate-induced drain leakage (GIDL) current, especially under a continuously decreasing gate bias. The issue could be relaxed by using lightly doped drain (LDD) or field-induced drain (FID) structure. Those structures can effectively reduce the vertical electric field near the drain edge, and therefore decrease the gate-induced drain leakage current.

Therefore, integrating various device structures with excellent Pr_2O_3 gate dielectric will obtain further improvements.

5.2.2 Integrate Pr_2O_3 Gate Dielectric on ELA Poly-Si TFTs

The main advantage of the ELA is that it can obtain bigger grain size than other techniques of grain growth. Hence the improvements of electrical characteristic will be the best one probably. Utilizing the good technique of ELA with excellent Pr_2O_3 gate dielectric, we confirmed that it will obtain further excellent performance. However, the surface roughness of poly-Si channel by ELA method is so serious that we can not deposited a thin Pr_2O_3 gate dielectric. Therefore, optimum thickness of gate dielectric is needed to consider.

簡歷

姓　　名：　張宏仁

性　　別：　男

出生日期：　中華民國七十一年二月十一日

籍　　貫：　浙江省

地　　址：　高雄市前鎮區忠誠里中華五路 949 號十樓之三

學　　歷：　私立中華大學　　電機工程學系

（民國 92 年 6 月）

國立交通大學　　電子研究所固態組　碩士班

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Study on the Electrical Properties of Fluorine-Incorporated Poly-Si TFTs with High-κ Pr_2O_3 Gate Dielectric

電子郵件：　kuroma0211@msn.com