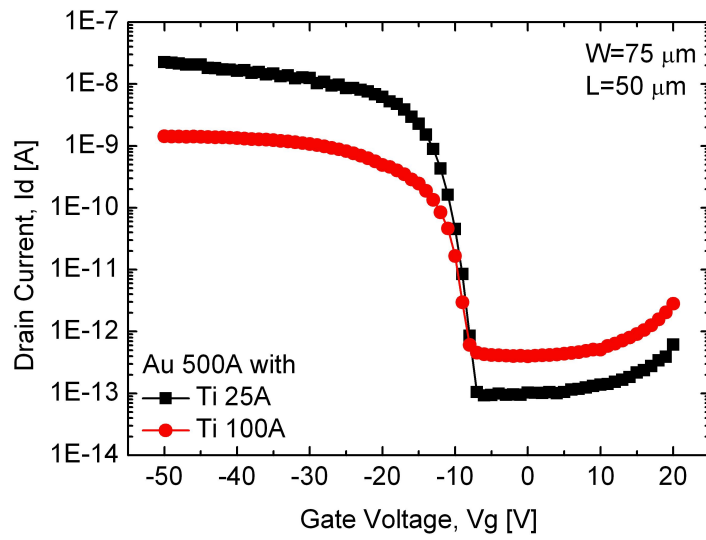
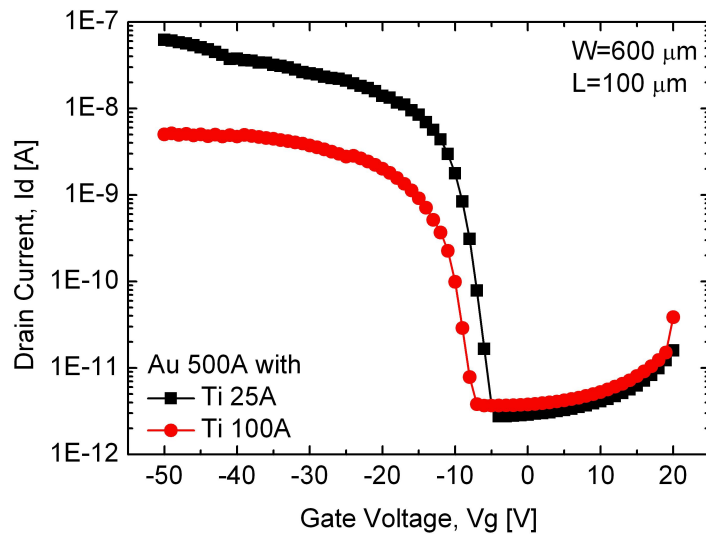


Figure 3.3-1 The Fabrication Procedures of Pentacene TFTs with different contact materials and thicknesses of adhesion layer.



(a)



(b)

Figure 3.3.1-1 The I_d - V_g electrical characteristics of pentacene TFTs with different thicknesses of adhesion layer, and the contact material is Au. The channel width/length of devices are (a) 75/50 $\mu\text{m}/\mu\text{m}$ and (b) 600/100 $\mu\text{m}/\mu\text{m}$.

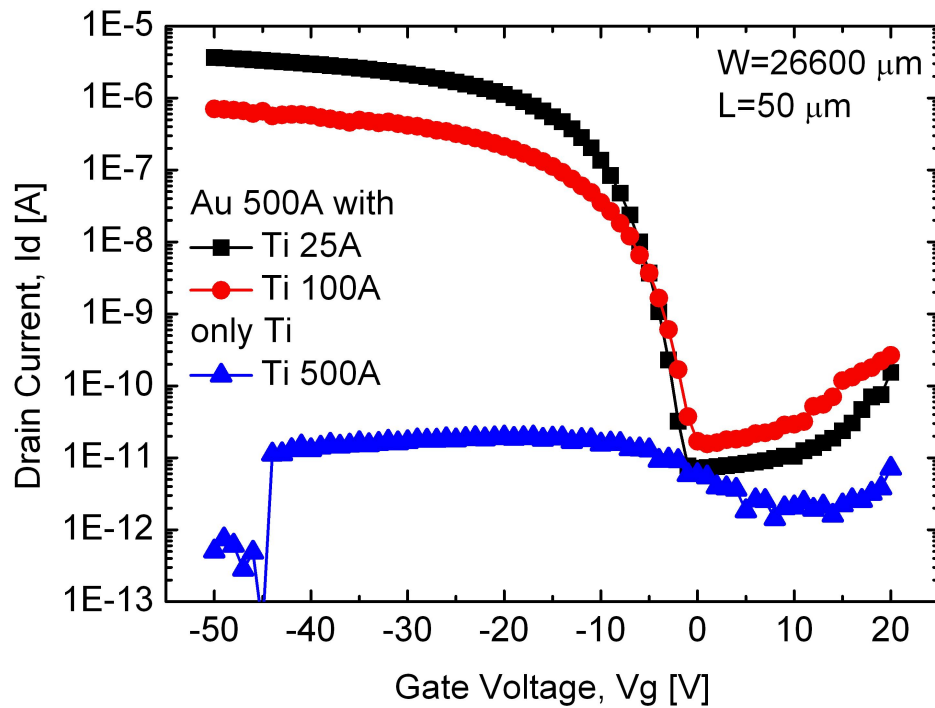
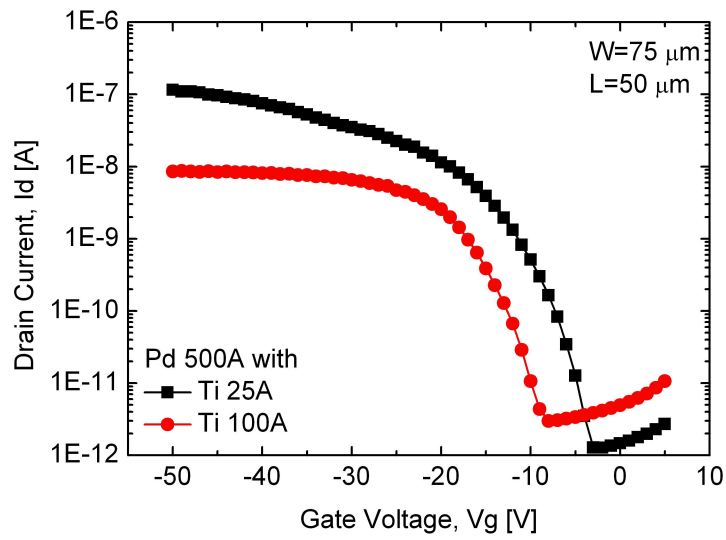
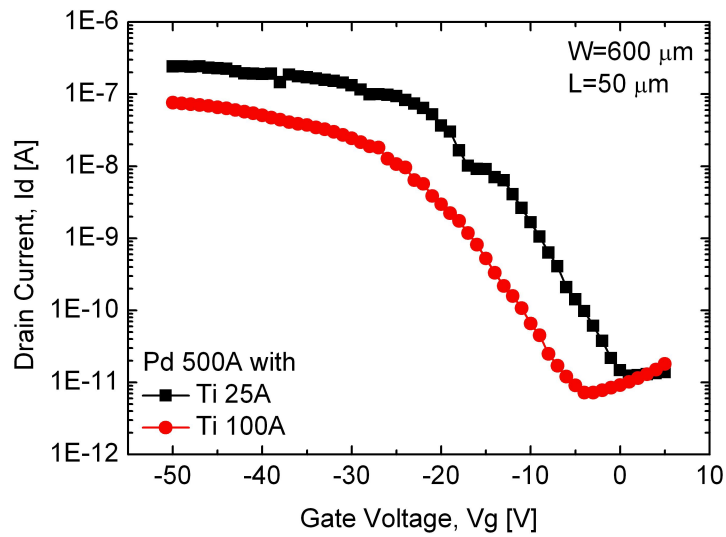


Figure 3.3.1-2 The I_d - V_g electrical characteristics of pentacene TFTs with different thicknesses of adhesion layer, and the contact material is Au. The channel width/length of devices are 26600/50 $\mu\text{m}/\mu\text{m}$.



(a)



(b)

Figure 3.3.1-3 The I_d - V_g electrical characteristics of pentacene TFTs with different thicknesses of adhesion layer, and the contact material is Pd. The channel width/length of devices are (a) 75/50 $\mu\text{m}/\mu\text{m}$ and (b) 600/50 $\mu\text{m}/\mu\text{m}$.

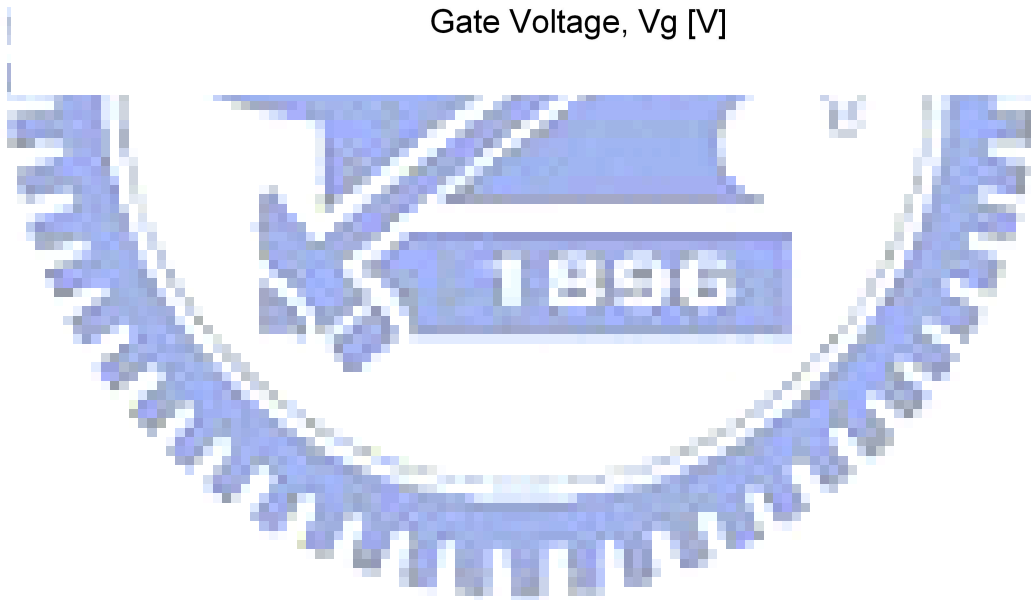
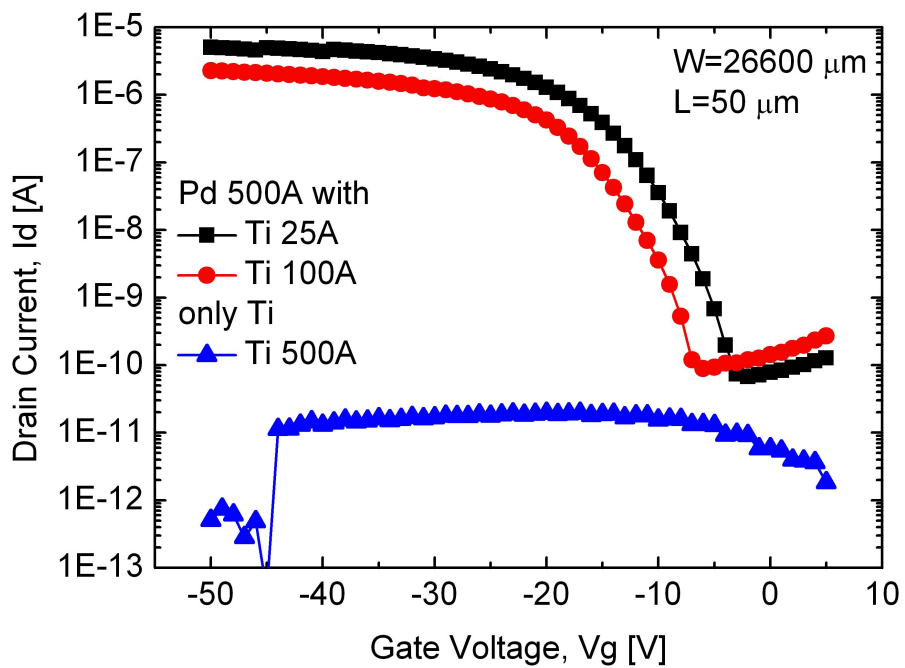


Figure 3.3.1-4 The I_d - V_g electrical characteristics of pentacene TFTs with different thicknesses of adhesion layer, and the contact material is Pd. The channel width/length of devices are 26600/50 $\mu\text{m}/\mu\text{m}$.

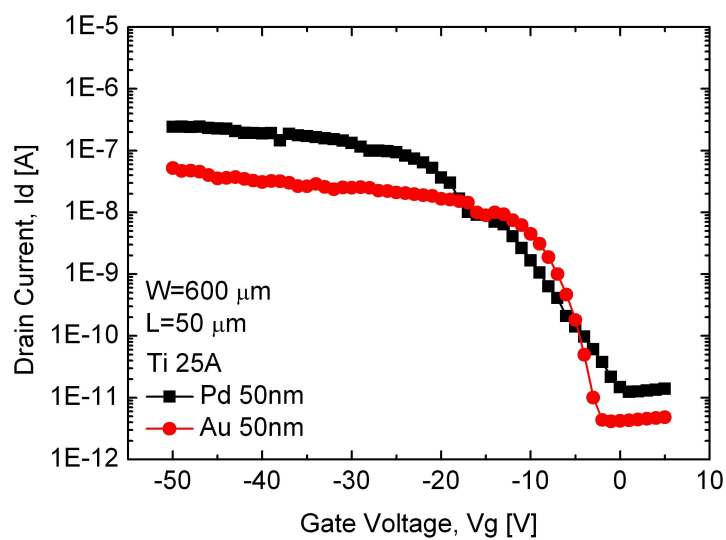
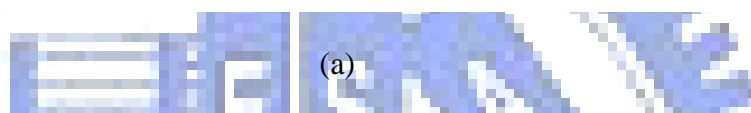
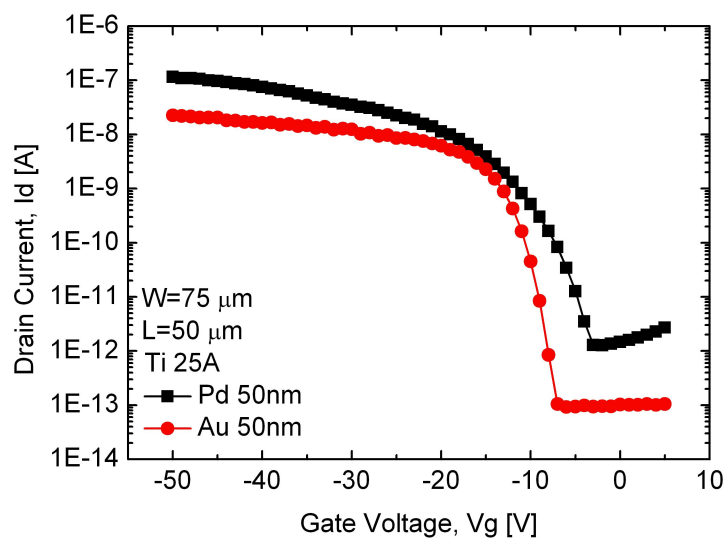


Figure 3.3.2-1 The I_d - V_g electrical characteristics of pentacene TFTs with different contact materials, and the thickness of adhesion layer is 2.5 nm. The channel width/length of devices are (a) 75/50 $\mu\text{m}/\mu\text{m}$ and (b) 600/50 $\mu\text{m}/\mu\text{m}$.

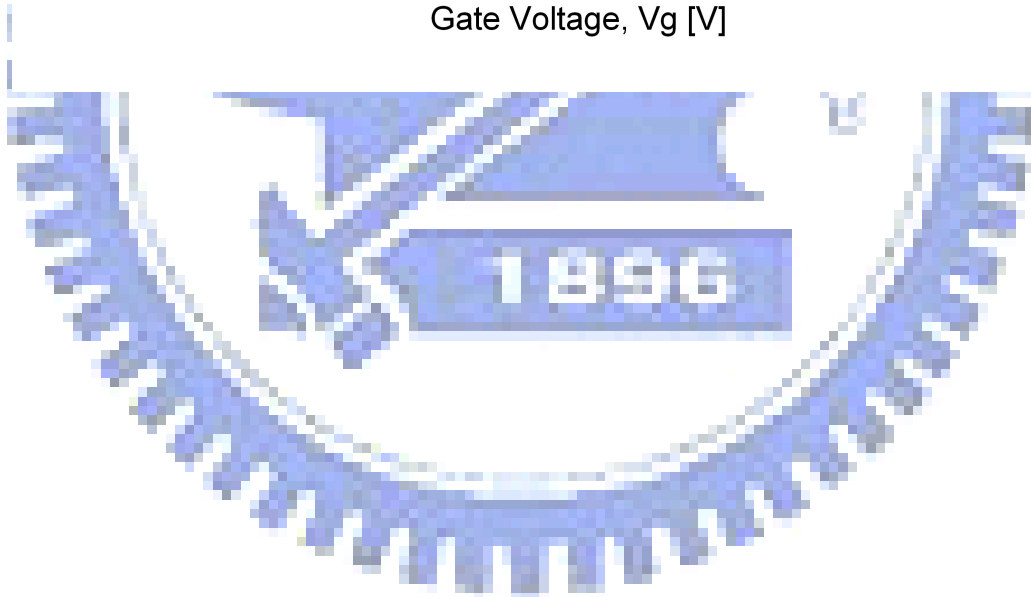
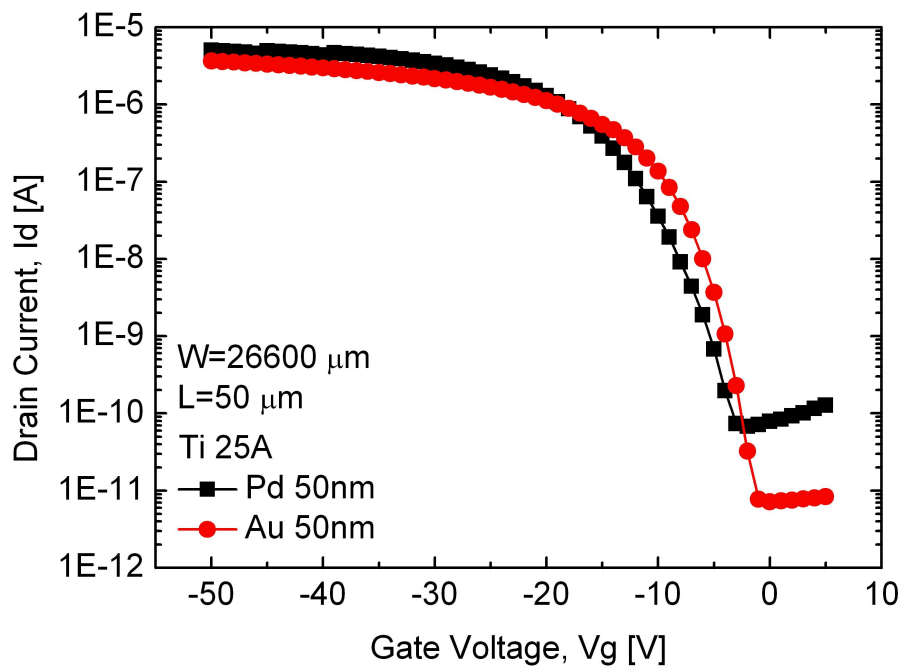


Figure 3.3.2-2 The I_d - V_g electrical characteristics of pentacene TFTs with different contact materials, and the thickness of adhesion layer is 2.5 nm. The channel width/length of devices are 26600/50 $\mu\text{m}/\mu\text{m}$.

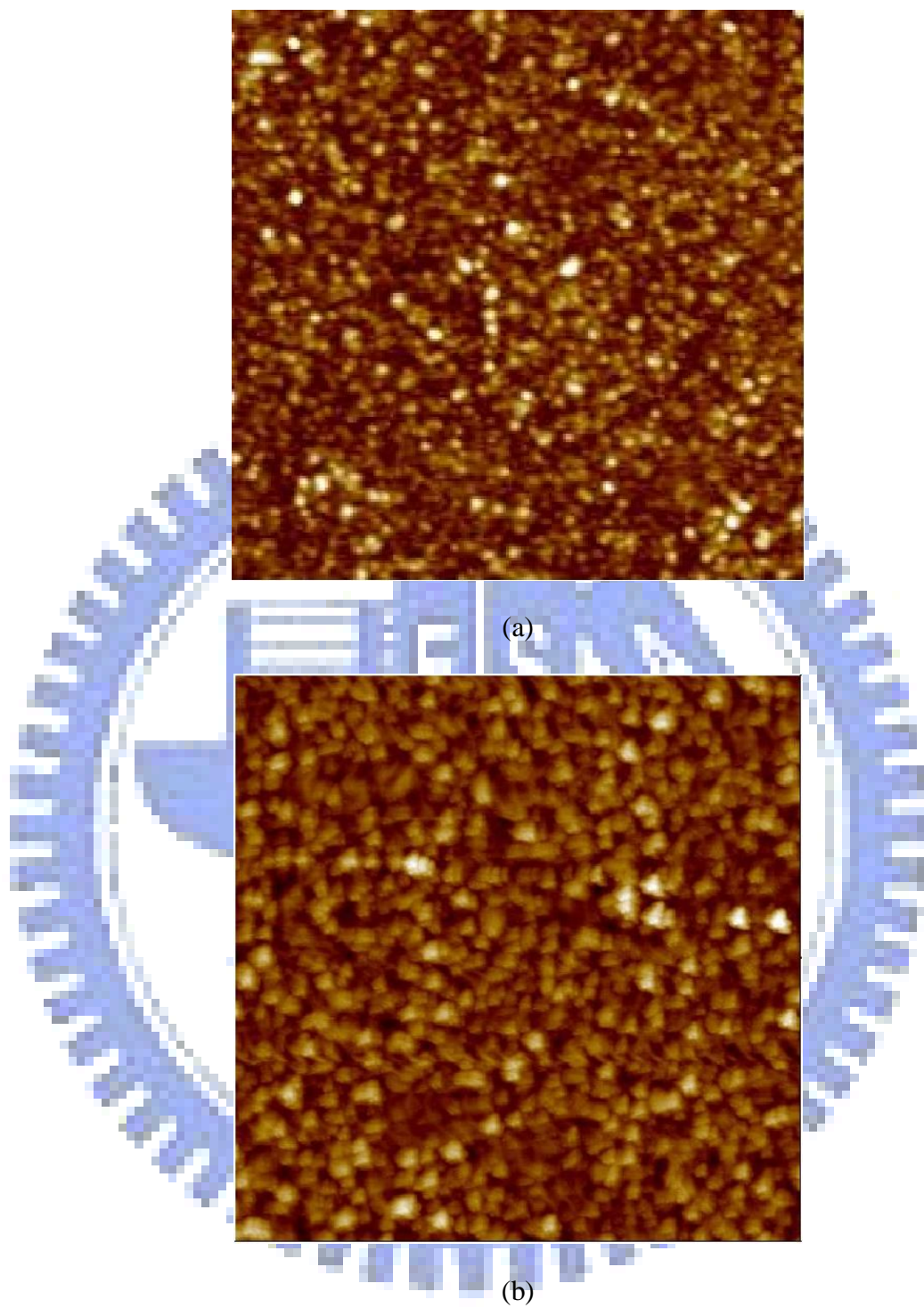


Figure 3.3.2-3 The AFM images of surface morphologies of (a) Pd and (b) Au.



Figure 3.3.2-4 The AFM images of surface morphologies of pentacene active layer deposited on (a) Pd and (b) Au.

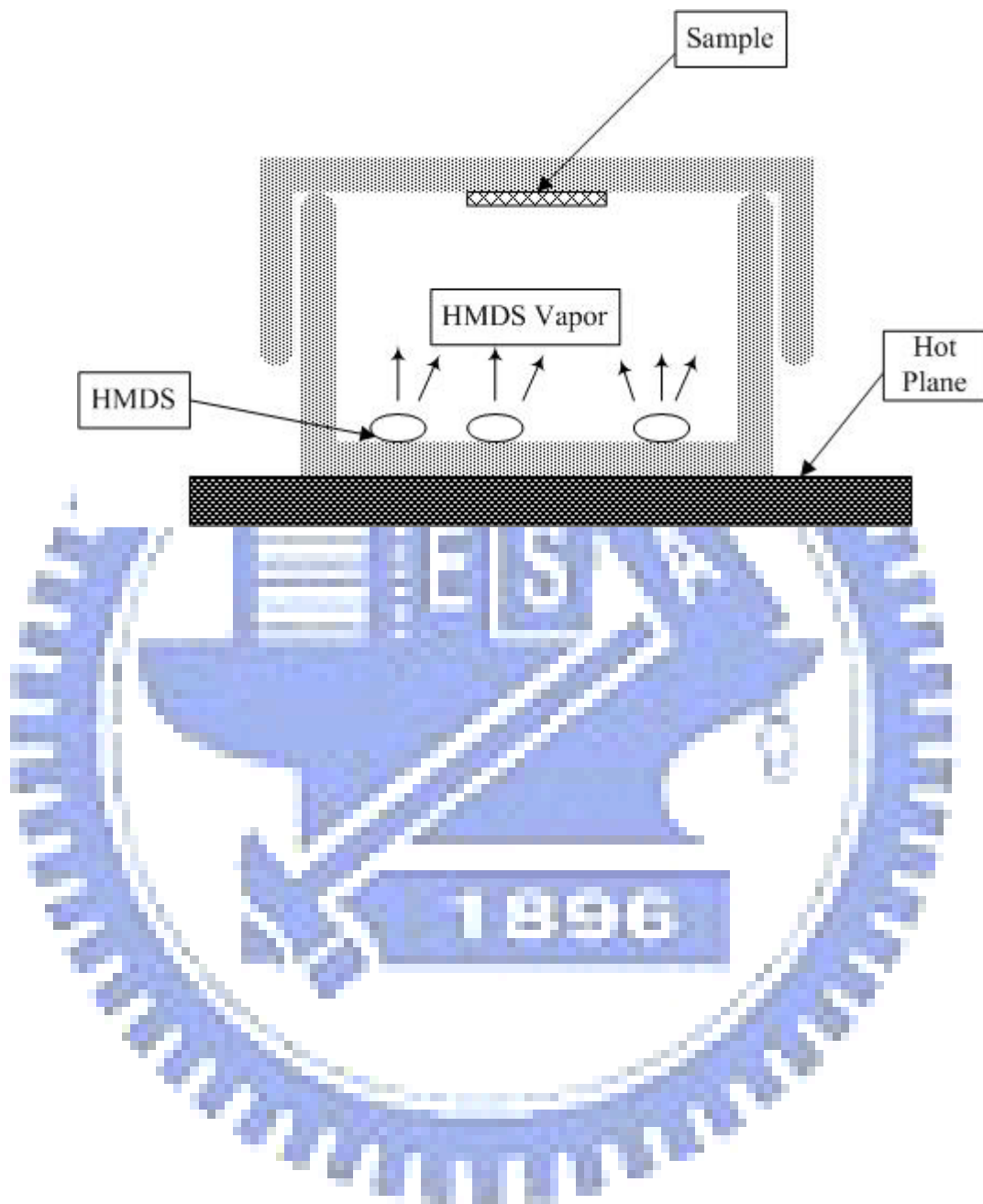


Figure 3.3.3-1 The schema of cross section of HMDS surface treatment process, pentacene TFTs is fixed on top of the cover of vitric container.

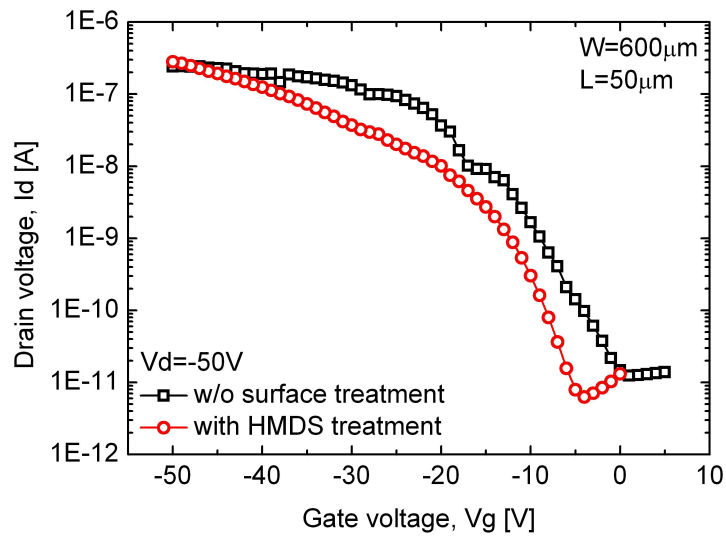
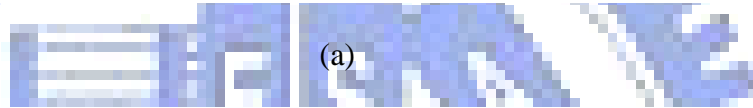
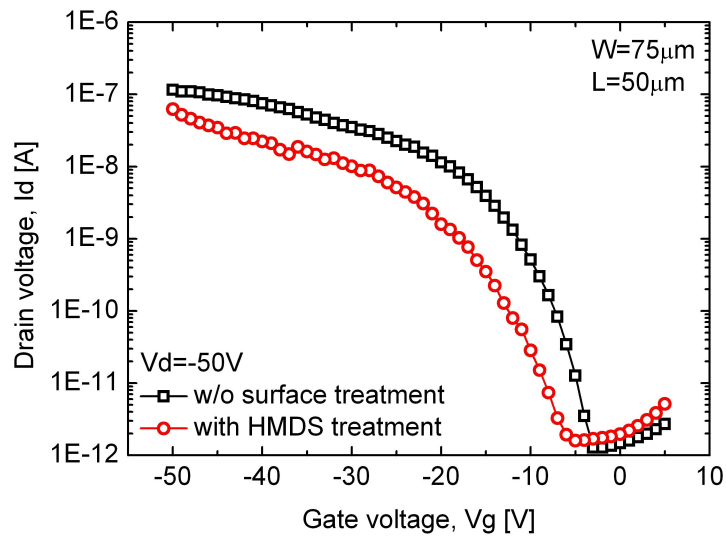


Figure 3.3.3-2 The I_d - V_g electrical characteristics of pentacene TFTs with and without HMDS surface treatment. The channel width/length of devices are (a) 75/50 $\mu\text{m}/\mu\text{m}$ and (b) 600/50 $\mu\text{m}/\mu\text{m}$.

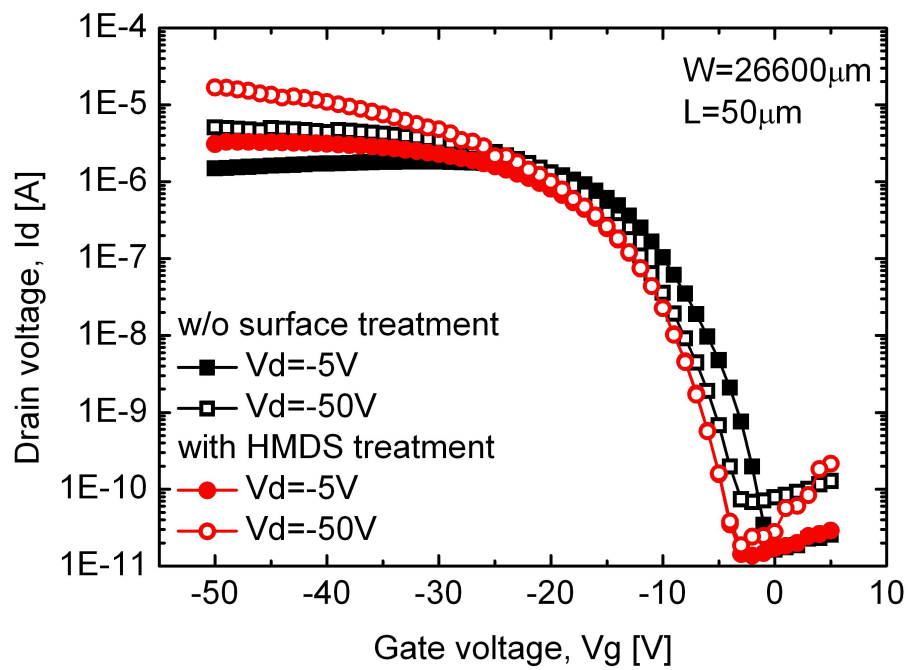


Figure 3.3.3-3 The I_d - V_g electrical characteristics of pentacene TFTs with and without HMDS surface treatment. The channel width/length of devices are 26600/50 $\mu\text{m}/\mu\text{m}$.

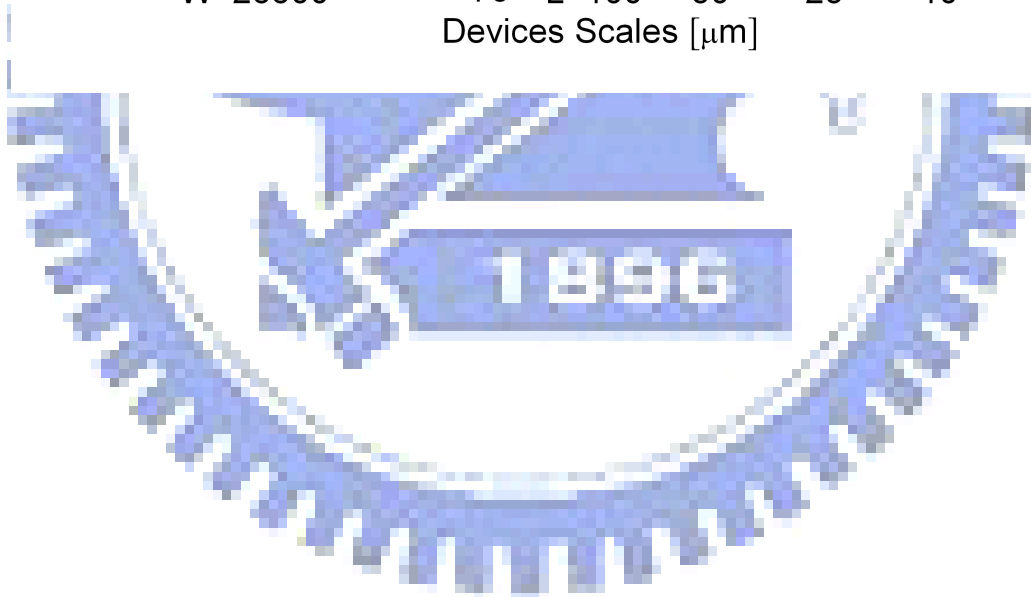
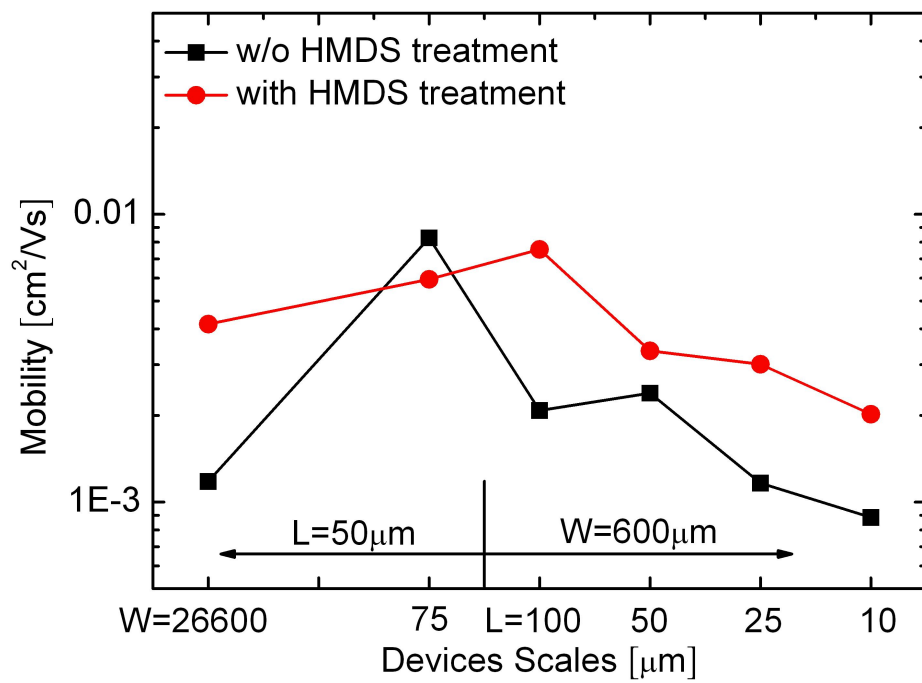


Figure 3.3.3-4 The extractions of mobility of pentacene TFTs with different device scales and HMDS surface treatment or not.