Chapter 1

Introduction

1.1 Overview of Organic Semiconductor

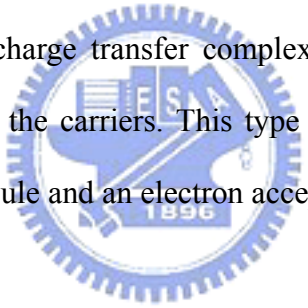
1.1.1 Introduction

A semiconductor is any compound whose electrical conductivity is in between that of typical metals and that of insulating compounds, and an organic semiconductor is any organic material that has semiconductor properties. In general, the organic semiconductors could divide into two catalogs. As shown in **Table 1.1.1 [1.1]**, both oligomers (short chain) and conjugated polymers (long chain) organic semiconductors are known. For examples, semiconducting oligomers are pentacene, perylene and C_{60}, and conjugated polymers are: poly(3-hexylthiophene), poly(p-phenylene vinylene), F8BT, as well as polyaectylene and its derivatives.

Organic semiconductors can be doped like inorganic semiconductors. Highly doped organic semiconductors, for example, Polyaniline and PEDOT: PSS, are also known as organic metals.

The organic semiconductor films can be deposited by using the four methods including solution-processed deposition, vacuum evaporation, electro-polymerization, and Langmuir-Blodgett technique. Solution-processed deposition and vacuum evaporation to fabricate organic semiconductor films have been extensively used in many works. For solution-deposited organic semiconductor films, such as polymers and pentacene are dissolved in solvents. And then these materials are deposited onto the substrate using spin-coating, dip-coating, or ink jet printing methods. Generally speaking, the oligomers are processed by vacuum evaporation.

There are two major classes of organic semiconductors, which overlap significantly: organic charge-transfer complexes, and various “linear backbone” polymers derived from polyacetylene, such as polyacetylene itself, polypyrrole, and polyaniline. Charge-transfer complexes often exhibit similar conduction mechanisms to inorganic semiconductors, at least locally. This includes the presence of a hole and electron conduction layer and a band gap. As inorganic amorphous semiconductors, tunneling, localized states, mobility gaps, and phonon-assisted hopping also contribute to conduction, particularly in polyacetylenes. Several kinds of carriers mediate conductivity in organic semiconductors. These include π-electrons and unpaired electrons. Almost all organic solids are insulators. But when their constituent molecules have π-conjugate systems, electrons can move via π-electron cloud overlaps. Polycyclic aromatic hydrocarbons and phthalocyanine salt crystals are examples of this type of organic semiconductor. In charge transfer complexes, even unpaired electrons can stay stable for a long time, and are the carriers. This type of semiconductor is also obtained by pairing an electron donor molecule and an electron acceptor molecule



1.1.2 Carrier Transport model of Organic Semiconductors

The organic semiconductor molecules are joined together by van der Waals force with energy smaller than 10 kcal/mol. This weak interaction energy of molecules may take responsibility for the low upper limit of carrier mobility, falls between 1-10 cm^2/Vs by time-of-flight measurement **[1.2]**, due to its value close to the vibration energy of molecules. Contrary to inorganic semiconductors that are joined by covalent bonds, the intermolecular bonding energy is strong such as 76 kcal/mol in silicon. Thus the carriers move as highly delocalized plane waves in wide band with high mobility.

The conjugated organic materials contain the specific π electron orbital that makes the carriers possible to move intra-molecular. In well-order organic semiconductors, the energy of

extraction state and the steady states of π electron would extend and split to form a band-like energy scheme. The energy scheme is similar to that in inorganic semiconductor, LUMO (Lowest Unoccupied Molecular Orbital) like the conduction band and HOMO (Highest Occupied Molecular Orbital) as the valence band. The energy band structure make the carrier transport demonstrate band-like behavior in some case.

However, band structure may not suit for disordered organic semiconductors, in which carrier transport is govern by hopping between localized states. It is thermal activated process and assisted by phonons. The mobility increases with temperature, although the overall mobility remains comparative low, usually much lower than 1 cm^2/Vs. The discrimination between hopping and band transport is the organic semiconductor film of mobility around 1 cm^2/Vs at room temperature. Many kinds of polycrystalline organic semiconductors like acene series, pentacene, rubrene, have mobility falling in the range. Sometimes, a temperature-independent mobility was found in some polycrystalline pentacene film **[1.3]**. This observation argued that the simply thermal activated hopping process governed the whole carrier transport behaviors in high quality polycrystalline pentacene film, despite that the defects rich film quality may cause mobility increase with temperature in some cases.

The understandings of carrier transport in a single crystalline organic semiconductor help us to understand the transport mechanism in a polycrystalline organic semiconductor film. It was believed that the carrier transport mechanism in single crystal is coherent band-like transport of delocalized states at low temperature. A high mobility for holes, 400 cm^2/Vs, measured by time-of-flight in single crystal naphthalene at 4.2 K was observed **[1.4-5]**. The hole mobility increases from 1 cm^2/Vs at room temperature to almost 400 cm^2/Vs at 10 K following a power law of T^{-n}, n=2.79. This is a clear evidence of band transport in single crystalline organic semiconductor. On the other hand, the electron mobility was also found temperature-dependent below 100 K and following a power law of T^{-n}, n~1.5-1.7, in single crystal naphthalene **[1.4, 1.6-7]**. However, between 100 K and 300 K, the electron mobility

revealed a constant value **[1.7-8]**, that has been treated as the superposition of two independent carrier transport mechanisms. The first mechanism was thought as the tunneling of small molecular polaron (MP), that the carriers were treated as heavy polaron type quasi-particles formed by the interaction between carriers with intramolecular vibrations of the local lattice environment. In this model, the mobility followed the power law of $\mu_{MP} \sim aT^{-n}$. Another mechanism is the moving of small lattice polaron (LP) by thermal activated hopping, which followed an exponential dependence on temperature of $\mu_{LP} \sim \exp[-E_a/kT]$. The superposition of these two mechanisms could get good consistence with experiment data from room temperature to a few Kelvin degrees **[1.7]**.

The basic understanding of carrier transport mechanism is very important in organic semiconductor. Although the ultra-pure organic semiconductor demonstrated a coherent band-like transportation, the most real organic semiconductor films were polycrystalline which contained many structure defects, such as in grain boundaries. Those defects dominated the carrier transport though affecting the energy barrier height in grain boundaries.

In summary, from above inference, the ways to enhance the carrier transport, or mobility, in organic semiconductors have two. One is to strengthen the intermolecular force of organic semiconductor to form a more rigid structure that would enhance the transport of delocalized carriers by lattice vibrations (phonons). Another is to build a structure that carrier transport only through intermolecular. That could be realized by long chain polymers or by very short channel length. Both them are not easy to mass production.

1.1.3 The Crystal Structures of Pentacene Thin Film

Pentacene ($C_{22}H_{14}$), a polycyclic aromatic hydrocarbon molecule, is one of promising candidates of organic semiconductors consisting of 5 linearly-fused benzene rings. Its schematic plot is shown in **Figure 1.1.3**. It has the appearance of a dark-blue powder, and it is

sensitive to light and oxygen. Its oxidation product is greenish, and most commercial samples of pentacene are greenish due to oxidized outer layer. Vacuum sublimation is used to purify pentacene.

There are several ways to fabricate it as a continuous film such as the solution process, vapor phase deposition and thermal evaporation. Previous studies on the growth of single crystalline pentacene have shown that the pentacene molecular crystallized in a layer-by-layer structure with herringbone arrangement, and giving a well defined "layer periodicity": d(001) value of 1.44 nm. The single crystal pentacene is triclinic structure with a unit cell parameters of a=7.9 Å, b=6.06 Å, c=16.01 Å, α=101.9^{o}, β=112.6^{o}, γ=85.8^{o} **[1.9-10]**. In 1991, Minakata et al. reported the pentacene as a film with a observed d(001) values of 1.54 nm **[1.11-13]** and 1.5 nm **[1.14-15]** different from the single crystal result. This was first mentioned by Dimitrikopoulos et al., who noted that the d(001) value of 1.54 nm should be attributed to another crystalline phase **[1.16]**. It was also the first time to observe the coexistence of two phases of pentacene, with d(001) values of 1.54 nm and 1.44 nm. The 1.54 nm and 1.44 nm polymorphs are commonly referred to as "thin film phase" and "single crystal phase". However, the Mattheus et al. thus studied and observed that the polymorphs of pentacene would result four crystalline phase of d(001) values of 1.54 nm, 1.5 nm, 1.44 nm, 1.41 nm **[1.17-20]** which strongly depended on the fabrication temperature, surface energy, thickness, and so on. Some of these phases could be transformed each other by solvent or heat **[1.21]**. Different crystalline phases of pentacene would perform different electrical properties. In general, a single type crystalline phase is preferred rather the coexistence of multi crystalline phases in pentacene, the former denoting better electrical properties.

Except the crystal structure properties of pentacene, the electrical properties of pentacene are also concerned. The ionization potential of pentacene is reported between 5.1 eV to 5.3 eV. And the band gap dependent on the crystal structure varied from 2.2 eV to 1.96 eV. The data of dielectric constant of pentacene is quite different determined by different research groups,

and it was reported as 2, or 4.

1.1.4 Applications of Organic Semiconductor to Organic Field Effect Transistors

An organic thin film transistor (OTFT) is a class of Field-Effect Transistor (FET) based on organic semiconductors. OTFTs are composed of three basic elements: (1) a thin semiconductor film; and (2) an insulating layer; and (3) three electrodes. Two of them, the source and the drain, are in contact with the semiconductor film at a short distance from one another. The third electrode, the gate, is separated from the semiconductor film by the insulating layer(s) which called gate dielectric(s). As shown in **Figure 1.1.4-1**, we can illustrate the widely used configurations of these elements. Usually, the former was also called the top contact (TC) and the latter was called the bottom contact (BC) TFTs.

OTFTs have attracted lots of attentions over the last decade due to its low fabrication cost, low temperature process and compatibility with plastic substrate. The field effect of organic semiconductor was reported in 1970s. Recently, OTFTs has been improved dramatically, for instance, mobility, the most important index of properties of TFTs has raised several orders even over the level of amorphous silicon TFTs to 1-5 cm^2/Vs as shown in the **Figure 1.1.4-2**.**[1.22] Table 1.1.4** show the chemical and comparison of mobilities of classes of organic and inorganic semiconductors.**[1.22]** They could be widely used in electronics applications, such as radio frequency identification tags **[1.23]**, smart cards, microelectronics **[1.24-28]** or sensors **[1.29]**. Additionally, the large area display is recognized as another key application. They are also the promising candidates to realize the flexible display technology.

Consequently, the processing characteristics and demonstrated performance of OTFTs suggest that they can be competitive for existing or novel thin film transistor applications requiring large area coverage, structural flexibility, low temperature processing, and

especially low cost. Such applications include switching devices for active-matrix flat-panel displays (AMFPDs) based on either liquid crystal pixels (AMLCDs) or organic light-emitting diodes (AMOLEDs).

1.2 Electrical Characteristics Analyses of OTFTs

1.2.1 The Basic Operation Mode and Principles of OTFTs

The Operation principle of organic TFTs are similar to amorphous or polycrystalline silicon TFTs. The current-voltage relation follows the charge sheet model. In general, the carrier transport in organic semiconductors could roughly divide into two possible ways, the intra-molecular and inter-molecular. The intra-molecular carrier transport is mainly governed by the band-like energy distribution that is constructed by the specific π electron orbital of organic semiconductors. And the carrier transport behaviors of inter-molecules of pentacene are governed by thermal hopping. That deduces the low field effect mobility. Organic semiconductors usually have high band gap and high ionic potential, for instance, pentacene has a nearly 2.5 eV band gap and 5 eV of ionic potential. Those make the pentacene TFTs operation at high voltage and hard to form an ohmic contact with source/drain electrodes.

The Fermi level of electrodes and HOMO-LUMO levels of pentacene are shown in **Figure 1.2.1-1 (a)**, when a positive voltage applied to the gate, negative charges are induced at the source electrode. The high work function materials, such as gold (Au) and palladium (Pd) with work functions of 5.1 eV and 5.0 eV are far away from the LUMO level, so that electron injection is very unlikely. Accordingly, no current passes through the pentacene layer, and small measured current essentially comes from leaks through the insulating layer. When the gate voltage is reversed, holes can be injected from the source to the semiconductor, because the Fermi level of Au or Pd is close to the HOMO level of pentacene. Accordingly, a conducting channel forms at the insulator-semiconductor interface, and charge can be driven from source to drain by applying a second voltage to drain. For this reason, pentacene is said

to be a p-type semiconductor. It should be pointed out that this concept differs from that of doping in conventional semiconductors, which can be made either n-type or p-type by introducing tiny amounts of an electron donating or electron withdrawing element. Symmetrically, an organic semiconductor will be said n-type when the source and drain electrodes can inject electrons in its LUMO level, provided electron transport dose occur, i.e., electron mobility is not too low.

Basically, the thin-film transistor operates like a capacitor. If the insulator has a capacitance per area C_i, and then the accumulated charge per-unit area is simply $(V_{gs}-V_{th}) \times C_i$, assuming that the V_{gs} must overcome the built in voltage, presenting as threshold voltage V_{th} caused by unintentional charge in gate insulator and the voltage dropped across the semiconductor is negligible. The semiconductor now contains positive charges both from doping and from the field effect which created the accumulation layer.

When a voltage is applied between source and gate, a charge is induced at the insulator/semiconductor interface. The gate voltage is dropped over the insulator and over the semiconductor near the insulator/semiconductor interface, giving rise to band bending in the semiconductor, the accumulation region. The additional positive charge accumulated in the region is supplied by the ohmic source and drain contact. This charge forms a conducting channel as shown in **Figure 1.2.1-1 (b)**, the conductance of which is proportional to the gate voltage.

At low drain voltages, the current increases linearly with the drain voltage, following Ohm's law. When the drain voltage is compared to gate voltage, the voltage drop at drain contact falls to zero and the conducting channel is pinched off. This corresponds to the so-called saturation regime where the current becomes independent of the drain voltage. Below a given threshold, the current increases exponentially. This corresponds to the below-threshold regime. In the above threshold regime, the current becomes proportional to the gate bias, as expected from the above description of the operating mode of the transistor.

Accordingly, the relation between current-voltage could be deduced from charge sheet model in linear regime and present as following:

$I_{ds}= \mu C_i(W/L)(V_{gs}-V_{th}-V_{ds}/2)\ V_{ds}$ if $0 > V_d \geqq (V_{gs}-V_{th})$

Where I_{ds} is source-drain current, V_{ds} is the drain-to-source bias, and W/L is the channel width-to-length ratio. For higher V_{ds}, exceed Vth , the channel pinch-off that means the channel depletes at the drain region, the saturation occurs and the current-voltage relation present as:

$I_{ds}= (1/2)\mu C_i(W/L)(V_{gs}-V_{th})^2$ if $0 > (V_{gs}-V_{th}) \geqq V_d$

1.2.2 Threshold Voltage and Constant Current Method

The definition of Vth deduced from MOSFET is not suitable for OTFTs since most organic semiconductors are only proposed uni-polar operation and biased in accumulation mode. The physical meaning of threshold voltage in OTFTs are questionable and difficulty to define.

OTFTs were turned on in the accumulation mode ($V_{gs} < 0$) and were turned off in the depletion mode ($V_{gs} >0$). We define a so-called ON current when the current is higher than a certain value, and the gate voltage (V_{gs}) corresponding to this current is called threshold voltage (V_{th}). We defined the normalized ON current is $10^{-9}/6$ Amp and thus the ON current of specified transistor is $10^{-9}/6 \times$ (W/L). The magnitude of ON current of pentacene TFTs with different channel length and width are listed at **Table 1.2.2**.

1.2.3 Extraction Method of Mobility and Subthreshold Swing

An important parameter, mobility μ, is identified as govern the moving ability of accumulated charges under the influence of field effect. The field effect mobility of saturation region can be obtained by the calculation described below.

$\mu= I_{ds}/[(1/2)\ C_i(W/L)(V_{gs}-V_{th})^2]$

With $|V_{ds}| \geqq |V_{gs}-V_{th}|$, the mobility can be calculated in the equation in this thesis when extract V_{th} by using ON current definition method.

When the gate bias is below the threshold voltage, and the semiconductor surface is in weak inversion or depletion, the corresponding drain current is called as the subthreshold current. The subthreshold region tells how sharply the current drops with gate bias and is particularly important for low-voltage, low power applications. The subthreshold swing (SS) can now be calculated.

$SS = (\ln 10)\partial V_{gs}/\partial(\ln I_{ds})$

1.2.4 Contact Resistances

Ongoing effects on the performance improvement of OTFTs focus on the identification of the relationships between the device structure, film morphology, and charge transport properties. It has been shown that, depending on the device geometry, contact resistances at the source and drain terminals in the OTFTs can be a significant bottleneck to current flow.

Rather than a simple Schottky barrier, contact resistances in OTFTs are typically treated as a combination of thermionic emission from the metal into the organic followed by carrier diffusion through a depletion region of the organic semiconductor, with the relative magnitudes of the two contributions determined by device geometry (TC or BC), carrier mobility, the energetic offset between the metal work function and the HOMO (p channel) or LUMO (n channel) level of the organic semiconductor, and the gate voltage.

In the last years, works by a number of research groups have shown that the properties of the source and drain contacts in OTFTs can important effect on the overall devices performance. For example, Jackson has published a transmission line study of contact resistance in pentacene TFTs **[1.30]** showing significant differences in the contact properties for top versus bottom contact devices. In an earlier study, Dimitrakopoulos and co-workers demonstrated that for bottom contact TFTs there is a region of disorder in the pentacene thin

film near the contact interface, through the disorder can be mitigated by thiolating the contacts**[1.31]**.

A powerful alternative to the transmission line method is to map the potential profile across operating OTFTs, as can be done using Kelvin probe force microscopy (KFM)**[1.32-34]**. Sharp voltage drops, which are observed in the profiles, highlight the resistive bottlenecks to current flow. For example, large contact resistances lead to large voltage drops at the contact-semiconductor interfaces. Dividing the voltage drop by the current yields the contact resistance. Recently Nichols et al. and Puntambekar et al. have reported potential profiling of pentacene TFTs by KFM.**[1.32-33]** In addition, Burgi et al. have demonstrated potential mapping of polythiophene TFTs as a function of temperature, which allows a better assessment of the carrier transport mechanisms at the contacts and in the film. **[1.34]**

Another contact resistance measurement for OTFTs is using the gated four-probe technique, in which the channel potential is sensed at two points between the source and the drain. While this approach dose not provide the exquisite detail of a full potential mapping by KFM, it is relatively easy to implement and allows variable-temperature resistance measurements without the need for a UHV-AFM. Four- terminal measurements on a-Si:H TFTs have been extensively reported,**[1.35]** and recent studies of field-effect transistors bbased on organic single crystals have also exploited four-probe geometries**[1.36-37]**, but so far there have been very few four-terminal measurement on OTFTs. Recently, Yagi et al. reported an initial study of four-terminal pentacene TFTs **[1.38]**.

1.3 Surface Treatment

The surface properties such as frictional or abrasion, permeability, insulating properties, wettability, and chemical reactivity are strongly dependent on a molecular aggregation state of the surface. **[1.39]** Therefore, the control of a molecular aggregation state on the film is

important to construct a highly functionalized surface. One of the most effective ways of studying on surface properties is contact angle measurement. The contact angle is the angle between the tangent to the drop's profile and the tangent to the surface at the intersection of the vapor, the liquid, and the solid. The contact angle is an index of the wettability of the solid surface. A low contact angle between solid surface water-drop indicates that the surface is hydrophilic and has a high surface energy. On the contrary, a high contact angle means that the surface is hydrophobic and has a low surface energy. The surface free energy was traditionally quantified by contact angle measurements.**[1.40]**

In this work, we fabricated the electrical properties of the OTFTs using pentacene fabricated by thermal evaporation in high vacuum with the two kinds of dielectric surface treatments: as-prepared (wet cleaning only), hexamethyldisilazane ($(CH_3)_3$-Si-O-Si-$(CH_3)_3$, HMDS). Oxide surface were treated with HMDS to improve the adhesion between pentacene and oxide surfaces. Modification of the substrate surface prior to deposition of pentacene has also been found to influence the film morphology.**[1.41]** For example, treatment of SiO2 with HMDS replaces the hydroxyl groups at the SiO2 surface with methyl or alkyl groups.

1.4 Motivation of thesis

From the inferences mentioned above, many unclear and unidentified mechanisms need to be studied for pentacene TFTs. Such as the definition of threshold voltage, field effect mobility behaviors, and environment influence, all were further considered. Organic films are very sensitive to the environment and unstable in air. Atmospheric moisture causes pentacene TFTs degradation and exhibit stronger hysteresis than those in a vacuum. OTFTs in air have higher off currents because the oxygen dopant and/or moisture interact with organic films. As a result, the influences of different deposition conditions on the pentacene thin film were discussed in this thesis, such as deposition temperatures, deposition rates, and thicknesses of pentacene thin film. The degradation of pentacene TFTs after stored and exposed in air for a

long time was also discussed.

As shown in the precious sections, large contact resistances are the bottleneck to improve the performances of OTFTs. The contact resistances of pentacene TFTs are proposed to discuss the influences on the work functions of the contact metal and the other contact properties when using different metal contact materials which have the equal work function value. Surface treatment of gate dielectric to improve the performance of pentacene TFTs is practiced by using HMDS.

In order to reduce the contact resistance, a novel material, multi-walled carbon nanotubes (MWCNTs) is introduced to be the contact material of pentacene TFTs. Carbon nanotubes (CNTs) are widely studied in different regions, such as field emission, field effect transistor, interconnection and else.

1.5 Thesis Organization

In chapter 1, the overview of organic semiconductor, OTFTs, basic principles of organic semiconductor and operation of OTFTs are described.

In chapter 2, the basics of pentacene grain growth were studied. The growths of pentacene with different deposition rate and substrate temperatures were studied in the first section. Additionally, the performance would be improved by using a specific thickness of pentacene thin films, and was proposed in the second section. In the final section, we studied the degradations of OTFTs performance exposed in the air for a long time.

In chapter 3, the contact resistance and surface treatment of pentacene TFTs were discussed by using different work function materials and HMDS. For the study on the injection barrier with adhesion layer, different thicknesses of adhesion layer were proposed in the first section. Furthermore, the metals with the equal work function (~ 5.1 eV) were used to be the contact materials of pentacene TFTs. By comparing the performances of pentacene TFTs with different contact metals, we confirmed that work function of the contact was not

the only one feature which was needed to consider when we tried to improve the performance of pentacene TFTs. Contact property between different contact materials and pentacene thin film are also a key point, and these contents are performed in the second section. After studying the influences of performance on contact resistance, the structures with the optimal performance of pentacene TFTs were taken to suffer surface treatment by HMDS for the performance improvement. The details of surface treatment to gate dielectric are shown in the third section in this chapter.

According to the results of previous sections, we introduced a novel material, i.e., MWCNTs to be the source/drain contact materials of pentacene TFTs. Because of the work function of MWCNTs was around 5.0 eV, we also supposed that there were good contact properties between pentacene film and MWCNTs. The influences of different length of MWCNTs, and we confirmed the superior performance was from using MWCNTs by making a comparison of MWCNTs and only treatment source/drain. The results of pentacene TFTs with MWCNTs source/drain were perform in the first and second sections in chapter 4. In the third section, we compared the performances of pentacene TFTs with MWCNTs and Pd/Ti source/drain.

Finally, the conclusions and recommendations for future researches are provided in chapter 5.

Chapter 2

The Effects on the Performance of Pentacene Active Layer

2.1 Introduction

The performances of pentacene TFTs will be affected by varying deposition conditions of pentacene active layer, and many researches have studied the effects of pentacene deposition rate and temperature.**[2.1]** Because different deposition conditions will lead to different surface morphology and crystalline structures of pentacene thin film.**[2.2]** Moreover, the effects of different thicknesses of pentacene thin film are also discussed, and a proper thickness will exhibit the optimum performance.**[2.2-3]**

In addition, OTFTs are very sensitive to moisture in air, and the degradations of electrical characteristics are obviously observed after exposed in air atmosphere. The F. De Angelis and et al. and S. H. Han and et al. had observed the degradations on performance after some periods of exposures in the air. **[2.4-7]**

2.2 Motivation

As the descriptions in section 2.1, the deposition conditions of pentacene thin film will significantly affect the performance. Therefore, the effects of pentacene active layer shall be studied before our further researches. In the first two sections, we attempt to obtain the optimum recipes of deposition of pentacene active layer, which result in superior performance, by varying deposition conditions and thicknesses. Additionally, the pentacene TFTs exposed in air for a long duration are discussed to observe the degradations in the final section.

2.3 Experimental Procedures

The fabrication Procedures of pentacene TFTs are showed schematically in **Figure**

2.3-1(a) ~ 2.3-1(d). As shown in **Figure 2.3-1(a)**, n-type heavy doping silicon substrate (N^{++} Si) was used to be the gate of pentacene TFTs. The resistivity of N^{++} silicon substrate is around 0.002 ~ 0.004 (Ω-cm), and the dopant in the substrate is Arsenic. After standard clean process, silicon dioxide (SiO_2) was prepared to be the gate dielectric of pentacene TFTs by dry oxidation about 200-nm-thick as shown in the **Figure 2.3-1(b)**. After the formation of gate dielectric, FH6400, the S/D was defined on the photoresist-coated dielectric by lithography. Subsequently, 50-nm-thick palladium (Pd) and 2.5-nm-thick titanium (Ti) were deposited by electron beam evaporator, and the Ti was used to be the adhesion layer for firmly sticking Pd and dielectric. After deposition, the P.R. was removed by lift-off process in acetone with vibrations in supersonic oscillator for 5 minutes, and then the S/D was patterned as shown in **Figure 2.3-1(c)**. Finally, pentacene was deposited fully on substrate by thermal evaporator as sown in **Figure 2.3-1 (d)**. Before deposition of pentacene active layer, the samples were cleaned by soaking in acetone with vibrations in supersonic oscillator for 5 minutes to remove the residual organic and particle contaminants on the channel region. Additionally, **Figure 2.3-2** shows the schema of chamber of thermal evaporator which was employed in our experiments and the substrate can be heated by a luminant heater.

There are two kinds of layout in fabrication of pentacene TFTs, i.e., linear like and finger type as shown in **Figure 2.3-3**. The channel lengths and widths of linear-like layout are in a range of 10 ~ 100 μm and 75 ~ 3700 μm. The channel length and width of finger-type layout is fixed at 50 μm and 26600 μm, because the device area of finger type can be minimized. Constant current and saturation mobility methods are used for the definitions of threshold voltage and extractions of mobility as mentioned in chapter one. All the electrical characteristics of pentacene TFTs were measured by using the probe station and Keithley 4200. The morphology of pentacene surfaces were observed by atomic force microscope (AFM) and scanning electron microscopy (SEM).

2.3.1 The Effects of Deposition Conditions of Pentacene Active Layer

2.3.1.1 Experiments

The detailed fabrication processes of pentacene TFTs are similar to section 2.3. However, different deposition rates and temperatures of pentacene are investigated to observe the influences on performances in this section. The deposition rates are 0.03 nm/s and 0.1 nm/s, when the deposition temperature is controlled at room temperature (RT) for comparisons. Moreover, the deposition temperatures of pentacene active layer are varied of RT, 70 ℃, and 90 ℃, when the deposition rate is fixed at 0.03 nm/s to observe.

2.3.1.2 Results and Discussion

The electrical characteristics of pentacene TFTs with different deposition rates are depicted in **Figure 2.3.1-1 (a)**, **(b)** and **2.3.1-2**, and the channel width/length in the figures are 75/50, 600/50, and 26600/50 μm/μm, respectively. From the results, the performances of pentacene TFTs with deposition rate of 0.03 nm/s would be better than those with deposition rate of 0.1 nm/s. Accordingly, we supposed that the reason of the improved performances were attributed to there had better crystalline order of pentacene molecular with slow deposition rate than that with fast one. Sequentially, the defects, which will induce scattering effect to carriers transport, would be reduced by using slow deposition rate. According to this reason, the largest mobility extractions of pentacene TFTs with fast and slow deposition rate could be improved from 0.006 to 0.009 cm^2/Vs as shown in **Figure 2.3.1-1 (a)**.

Furthermore, the Id-Vg diagrams of pentacene TFTs with different deposition temperatures are depicted in **Figure 2.3.1-3 (a)**, **(b)**and **2.3.1-4**, and the channel width/length of them are 75/50, 600/50, and 26600/50 μm/μm, respectively. From the results, we found that pentacene TFTs with high deposition temperature displayed better performances than that with deposition temperature of RT, and we found that the off current and mobility could be improved by raising deposition temperature. The mobility of pentacene TFTs with channel

width and length of 75 μm and 50 μm could be improved from 0.009 cm^2/Vs to 0.013 cm^2/Vs, when raised the deposition temperature from RT to 90 ^oC. By extensively observing the results, we found that pentacene TFTs with channel width and length of 75 μm and 50 μm would almost exhibited optimum performances. The on/off current ratio was improved by the reduced defects in pentacene active layer which lead to low off current. Moreover, the extractions of saturation mobility of pentacene TFTs with different deposition temperatures and device scales are shown in the **Figure 2.3.1-5**.

Additionally, by observing the performances of different channel width, the inferior mobility and on/off current ratio of lager channel width can be attributed to the existent transition region of pentacene active layer. The transition region is formed near the S/D, because the deposition properties of pentacene onto SiO2 and metal were quite different. Moreover, different grain size of pentacene thin film in transition region can also be observed by scanning electronic microscopy (SEM). **Figure 2.3.1-6** is the SEM images of transition region, and non-uniform grain size can be observed near the S/D. Some groups also proposed the observations of transition region, and indicate that the performances of pentacene might be restricted by the extra large grain boundary in transition region.**[2.8]**

2.3.2 The Effects of the Thicknesses of Pentacene Active Layer

2.3.2.1 Experiments

After investigated the effects of pentacene deposition conditions, further studies on effects of pentacene are needed. In this section, the fabrication procedures are also similar to the descriptions of section 2.3, but the effects of pentacene thicknesses will be studied. Three different thicknesses of pentacene thin film, which are 20 nm, 40 nm, and 60 nm, are employed in this section. According to the results of the section 2.3.1, the deposition temperature and rate of pentacene are controlled at 90 ℃ and 0.03 nm/s.

2.3.2.2 Results and Discussion

The Id-Vg characteristics of pentacene TFTs with varied thicknesses are depicted in the **Figure 2.3.2-1 (a)**, **(b)** and **2.3.2-2**, and the channel width/length of them are 75/50, 600/50, and 26600/50 μm/μm, respectively. From the results, pentacene TFTs with pentacene thickness of 40 nm displayed better performances than that with the other thickness. The extractions of mobility of pentacene TFTs with 20, 40, and 60-nm-thick pentacene were 0.001, 0.008, and 0.003 cm^2/Vs, respectively. The reasons for the results of different pentacene thicknesses are still uncertain and needed further studies. Therefore, we suspected that the optimum thickness might be obtained from the compromises of two factors. They were (1) the increasing thickness of pentacene active layer would contain more defects, which could be attributed to the increase of grain boundary and lead to inferior performances, and (2) the bulk phase of crystalline phase in pentacene thin film would increase as increasing pentacene thickness.**[2.2]** Consequently, the effect of (1) might be more serious than that of (2) as increasing thickness of pentacene film, and that resulted in the existent optimum thickness of pentacene film of 40 nm.

The mobility extractions of pentacene TFTs with different device scales and thicknesses of pentacene film are shown in **Figure 2.3.2-3**. The maximum mobility is about 0.02 cm^2/Vs when the thickness of pentacene thin film is 40 nm and channel width/length is 75/50 μm/μm.

2.3.3 The Degradation effect of Pentacene TFTs

2.3.3.1 Experiments

The devices employ in the section are the samples which have measured in the section 2.3.1. Thus, pentacene TFTs with deposition rate of 0.03 nm/s, and the deposition temperature are RT and 90 ℃. The pentacene active layer is 60-nm-thick. These samples are stored in the sample carrier for three months after the measurements of section 2.3.1.

2.3.3.2 Results and Discussion

Figures 2.3.3-1 and **2.3.3-2** are the Id-Vg diagram and the mobility extractions of different device scales with stored for three months. The degradation on performances can be obviously observed, and the threshold voltage exhibit serious shift about -30 V. We suspected that the reasons to induce degradations on electrical characteristic resulted from more accept-like trap states which were induced by the oxidation of moisture, which formed the –OH bonding, on surface and grain boundaries of pentacene thin film. There are some groups has also proposed the supposition, and had extensively studies to demonstrate this phenomenon.**[2.4-7]**

2.4 Summary

From the results in the section 2.3.1, slow deposition rate and raised deposition temperature of pentacene thin film contributed to improve the quality of pentacene active layer. We found pentacene TFTs with deposition rate and temperature of 0.03 nm/s and 90 ^{o}C could result in better performance than that with other conditions in our works. Moreover, pentacene thin film exist an appropriate thickness which lead to obtain the optimum performance. From the results in the section 2.3.2, pentacene TFTs with 40-nm-thick of pentacene active layer exhibited more superior electrical characteristics than the other thicknesses. Additionally, the degradation on electrical characteristics which might be attributed to accept like trap states could be observed obviously, and displayed serious threshold voltage shifts about -30 V.

Chapter 3

The Effects on Metal Contact and Surface Treatment

3.1 Introduction

After studying on the effects of fabrication conditions of pentacene active layer in the chapter 2, the performances of pentacene TFTs will also be significantly affected by the identities of S/D. Consequently, different thicknesses of adhesion layer and contact materials of S/D have been extensively investigated.**[3.1-2]** Because of the differences of the work function differences and contact properties between pentacene and different metal will lead to different pentacene grain size, contact resistance, and injection barriers.

The work function difference between contact metals and Fermi level of pentacene active layer result in large injection barrier, which can call Schottky barrier, will restrict the performances of pentacene TFTs, because the carriers will be difficult to inject from pentacene to metal contact.**[3.2]**

Furthermore, contact properties between pentacene and metals also exhibit seriously influences on performances of pentacene TFTs. By comparing with the performances of pentacene TFTs with different materials of S/D, the influences of contact properties can be observed.**[3.1]**

Additionally, surface treatments are extensively adopted to modify surface properties of gate dielectric and to improve the crystalline order of pentacene thin film. Hexamethyldisilazane (HMDS) and octadecyltrichlorosilane (OTS) were extensively used in surface treatment. **[3.3-7]** Generally speaking, the mechanisms of surface treatments were to replace the properties of gate dielectric surface from hydrophilic to hydrophobic which were replacing the “–OH” bonds forming on the gate dielectric surface by the organic terminal

groups, i.e., "–CH_3" or "–$(CH_2)_n$–CH_3" bonds.**[3.6-3.7]** Thus, the organic terminal groups induced superior contact properties for pentacene thin film, and the mobility could be improved because of the improvement of crystalline order of pentacene active layer.

3.2 Motivation

The appropriate deposition conditions of pentacene active layer are already obtained in chapter two. In this chapter, the influences on performances of different contact materials and thickness of adhesion layer are investigated which are necessary to further obtain the fabricated conditions can display superior performances. Additionally, surface treatment which employed HMDS to improve performance is discussed in this chapter.

3.3 Experimental Procedures

The fabrication procedures are depicted in the **Figure 3.3-1 (a) ~ 3.3-1 (d)**, n type heavy doping silicon substrate (N^{++} Si) was used to be the gate of pentacene TFTs. The resistivity of it is 0.002 ~ 0.004 (Ω-cm), and the dopant of the substrate is Arsenic. After standard clean process, silicon dioxide (SiO_2) was prepared to be the gate dielectric of pentacene TFTs by wet oxidation about 320 nm-thick as shown in the **Figure 3.3-1 (b)**. After the formation of gate dielectric, FH6400, the S/D was defined on the photoresist-coated dielectric by lithography. Subsequently, 50-nm-thick contact metal and titanium (Ti) were deposited by electron beam evaporator, and the Ti was used to be the adhesion layer for firmly sticking contact metal and dielectric. After deposition, the P.R. was removed by lift-off process in acetone with vibrations in supersonic oscillator for 5 minutes, and then the S/D was patterned as shown in **Figure 3.3-1(c)**. Finally, pentacene was deposited fully on substrate by thermal evaporator as shown in **Figure 3.3-1 (d)**. Before deposition of pentacene active layer, the samples were cleaned by soaking in acetone with vibrations in supersonic oscillator for 5 minutes to remove the residual organic and particle contaminants on the channel region.

Pentacene was deposited by thermal evaporator, and the thickness, deposition rate and temperature of pentacene active layer was fixed at 40 nm, 0.03 nm/s, and at RT.

There are two kinds of layout in fabrication of pentacene TFTs, i.e., linear like and finger type as shown in **Figure 2.3-3**. The channel lengths and widths of linear-like layout are in a range of 10 ~ 100 μm and 75 ~ 3700 μm. The channel length and width of finger-type layout is fixed at 50 μm and 26600 μm, because the device area of finger type can be minimized. Constant current and saturation mobility methods are used for the definitions of threshold voltage and extractions of mobility as mentioned in chapter one. All the electrical characteristics of pentacene TFTs were measured by using the probe station and Keithley 4200. The morphology of pentacene surfaces were observed by atomic force microscope (AFM) and scanning electron microscopy (SEM).

3.3.1 The Influences of Thicknesses of Ti Adhesion Layer

3.3.1.1 Experiments

The details of fabrication procedures are similar to section 3.3. However, the influences on performances of thickness of Ti adhesion layer with different contact metal materials, which are Au and Pd, are discussed in the section. For comparisons, the thicknesses of Ti adhesion layer are varied of 2.5 nm and 10nm with contact metal, and 50nm without contact metal.

3.3.1.2 Results and Discussion

The Id-Vg diagrams of pentacene TFTs with Au/Ti S/D and the channel width/length of them are 75/50, 600/100, and 26600/50 μm/μm, are shown in the **Figure 3.3.1-1 (a)**, **(b)**, and **Figure 3.3.1-2**, respectively. From the results in **Figure 3.3.1-1** and **Figure 3.3.1-2**, we found that the injection barrier was proportional to the thickness of Ti adhesion layer. Furthermore, pentacene TFTs with Ti S/D, which was only 50-nm-thick of Ti, displayed poor performances.

By observing the results, large injection barrier was induced by the work function difference between Ti and pentacene active layer.

From the results, pentacene TFTs with Au/Ti S/D with 50 nm/2.5 nm would exhibit better performance than other thicknesses of Ti. The drive current of it was one order larger than that with 10-nm-thick of Ti. The extractions on maximum mobility of pentacene TFTs with Au/Ti S/D with 50 nm/ 2.5nm were 0.0018 cm^2/Vs. On the opposite, Pentacene TFTs with Ti (50 nm) S/D showed inferior performance which were nearly not "turn-on", and the mobility of them were 2×10^{-9} cm^2/Vs with channel width/length was 26600/50 μm/μm.

Furthermore, by observations of different contact material which has approximate work function value as Au, we could observe the tendence of influences on performances of Ti adhesion layer. **Figure 3.3.1-3 (a)**, **(b)** and **Figure 3.3.1-4** are the Id-Vg diagrams of pentacene TFTs with Pd/Ti S/D, and channel width/length of them are 75/50, 600/50, and 26600/50 μm/μm, respectively. From the results, the phenomenon which was similar to pentacene TFTs with Au/Ti S/D was observed.

From all the results in this section, no matter what kinds of contact material, large injection barrier would exist between Ti and pentacene.

3.3.2 The Influences of contact materials

3.3.2.1 Experiments

The fabrication procedures in the section are similar to the procedure has mentioned in section 3.3. However, the influences on performance of pentacene TFTs with different contact materials are discussed, and they are Au and Pd which are in order to observe the contact properties between pentacene and them which have the approximate work function value. From the results in section 3.3.1, for comparisons, the thickness of adhesion layer is fixed at 2.5 nm.

3.3.2.2 Results and Discussion

Figures 3.3.2-1 (a), **(b)** and **3.3.2-2** depict the Id-Vg characteristics of pentacene TFTs with different S/D contact materials, and the channel width/length of them are 75/50, 600/50, and 26600/50 μm/μm, respectively. From the results, the pentacene TFTs with Pd/Ti S/D displayed better performance than that with Au/Ti. Because the work function of Au and Pd are approximative which are around 5.1 eV, we supposed that there existed better contact properties between pentacene and Pd than that between pentacene and Au. Therefore, it contributed to superior performance.

Furthermore, the results as shown in **Figures 3.3.2-1** and **3.3.2-2** might also attribute to the morphology of pentacene active layer on Pd and Au**.** Because different surface roughness would seriously affect the grain size of pentacene.**[3.1,3.8-9]** For comparison, the deposition rate of these contact materials was fixed at 0.03 nm/s which meant that the contact metals might exist approximative surface roughness. **Figure 3.3.2-3 (a)** and **(b)** showed the surface morphology of Pd and Au, respectively. **Figure 3.3.2-4 (a)** and **(b)** showed the surface morphology of pentacene on Pd and Au, respectively. Some researches had observed that there existed different morphologies of pentacene on Pd and Au.**[3.1]** However, by observing the images of AFM in our works, there were not obvious difference of them.

Consequently, from all the results in our work, we found the superior performances of pentacene TFTs with Pd/Ti S/D might contribute to the superior properties between pentacene and Pd.

3.3.3 Surface Treatment of Gate Dielectric

3.3.3.1 Experiments

The fabrication procedures in this section are also similar to that described in the section 3.3. In order to further improve the performances of pentacene TFTs, a surface treatment on gate dielectric which was administered by vapor of HMDS were employed before pentacene

deposited. According to the results in the front two sections, the material of S/D were Pd/Ti and the thicknesses were fixed at 50/2.5 nm/nm. For comparison, the deposition conditions of pentacene were controlled at RT of temperature and 0.03 nm/s of rate, and it was fixed at 40-nm-thick. **Figure 3.3.3-1** depicts the schema of HMDS surface treatment with substrate temperature of 150 ℃ and treatment time in air atmosphere of 15 minutes.

3.3.3.2 Results and Discussion

The improvement on performances of surface treatment for pentacene TFTs with Pd/Ti S/D are studied in this section. HMDS is employed to modify surface properties of gate dielectric from hydrophilic to hydrophobic, and improved the crystalline order of pentacene active layer as mentioned in section 3.1.

Figures 3.3.3-2 (a), (b), and **3.3.3-3** are the Id-Vg diagrams of pentacene TFTs with surface treatment, and the channel width/length of them are 75/50, 600/50, and 26600/50 μm/μm, respectively. **Figure 3.3.3-4** is the extractions of mobility with different device scales. As shown in these figure, the improvement on performances of pentacene with HMDS treatment were near three times better than that without treatment. This phenomenon were also observed by other research groups.**[3.6-7]**

There were two reasons which we supposed to contribute to the improvement of performances: (1) The contact properties between pentacene and gate dielectric might be improved by the chemical bonding of pentacene and organic terminal groups. (2) After surface treatment, the crystalline order of pentacene thin film was improved, and fewer defects existed in it. Both these two factors contributed to reduce carrier scattering, which were interface scattering and impurity scattering, and to improve the performance.

The mobility extractions of pentacene TFTs with and without surface treatment were around 0.007 cm^2/Vs and 0.002 cm^2/Vs, respectively, and the channel width/length of them were 600/100 μm/μm. there was needed to explain that the mobility of pentacene TFTs

without surface treatment were inferior to the results in chapter 2. It was attributed to thicker gate dielectric (320 nm) and the growth rate of wet oxidation was much faster than dry oxidation, and both of them would induce larger surface roughness.

3.4 Summary

From the results in section 3.3.1, the work function difference between Ti adhesion layer and pentacene resulted in large injection barrier. Accordingly, pentacene TFTs with thinner adhesion layer exhibited superior performance. When the thickness of Ti adhesion layer is 2.5 nm, optimum performances were obtained in our work.

In section 3.3.2, the impacts of contact properties on performances were studied by employing different contact materials with approximative work function which are Au and Pd. From the results, the performance of pentacene TFTs with Pd/Ti S/D were better than Au/Ti S/D, because of the better contact properties between pentacene and Pd than Au.

Finally, from the results in section 3.3.3, HMDS surface treatment for pentacene TFTs with Pd/Ti S/D could improve the performances about several times.

Chapter 4

Pentacene TFTs with Novel Material Source and Drain

4.1 Introduction

Pentacene-based organic thin-film transistors (OTFTs) have been attracting much attention because of their relatively low cost and the feasibility of fabricating them on flexible organic substrates at low temperature. Currently, two typical device structures are employed for the fabrication of OTFTs, i.e., bottom-contact (BC) and top-contact (TC) OTFTs. When pursuing denser electrical circuits, BC-OTFTs have an advantage over TC-OTFTs because exposure of the active organic material to solvents and chemicals can be avoided during the lithography process.**[4.1]** Nevertheless, the performance of BC-OTFTs is usually inferior to that of TC-OTFTs because of higher contact resistance (R_c) at the source/drain (S/D) electrodes; this phenomenon has been investigated extensively.**[4.2-4.3]**

Carbon nanotubes (CNTs) have been the focus of much recent research because of their unique electronic properties and extraordinary mechanical properties.**[4.4-4.5]** Single-walled carbon nanotubes (SWCNTs) have been demonstrated as highly useful materials in nanoscale devices, while multi-walled carbon nanotubes (MWCNTs) have great potential for the field emission applications and as interconnects.**[4.6-4.7]**.

4.2 Motivation

In order to reduce the contact resistance of pentacene TFTs, we introduce a novel material, multi-walled carbon nanotubes (MWCNTs), to be the S/D contact material. We supposed that MWCNTs would exhibit good contact properties, large contact area, and small work function difference between pentacene active layer and MWCNTs. Therefore, contact resistances of pentacene TFTs could be reduced by using MWCNT S/D.

4.3 Experimental Procedures

In this chapter, we propose a technique—employing thermal chemical vapor deposition (T-CVD) to deposit MWCNTs directly onto patterned S/D electrodes—for reducing the value of R_c of pentacene-based BC-OTFTs; this approach appears to be more practical and reliable than that proposed in a previous study.**[4.8]**

Figure 4.3-1 and **Figure 4.3-2** illustrate a schematic cross-section of a BC pentacene TFT possessing an MWCNT S/D and the recipe for growth of the MWCNTs. An n^{++}-Si substrate was used as the gate electrode. After standard cleaning, a 320-nm-thick SiO_2 layer was grown thermally as the gate insulator. For S/D formation, a Fe/Ti catalytic layer was then deposited through electron beam thermal evaporation and patterned using the lift-off technique. For comparison, the thickness of the Fe layer was fixed at 5 nm.

All samples were cleaned by soak in acetone with vibrations in supersonic oscillator for 5 minutes. Subsequently, the MWCNTs were grown through T-CVD; the procedure was performed as follows: The samples were heated to 700°C under a nitrogen gas (N_2) atmosphere. After pretreatment of the Fe/Ti catalytic layer in a mixed hydrogen (H_2) and N_2 atmosphere, MWCNTs were grown on the S/D region through pyrolysis of ethylene (C_2H_4), as the carbon source. After MWCNT growth, a pentacene layer (ca. 40 nm) was finally deposited using thermal evaporation in a high vacuum chamber operated at a base pressure of 10^{-6} torr at room temperature.

There are two kinds of layout in fabrication of pentacene TFTs, i.e., linear like and finger type as shown in **Figure 2.3-3**. The channel lengths and widths of linear-like layout are in a range of 10 ~ 100 μm and 75 ~ 3700 μm. The channel length and width of finger-type layout is fixed at 50 μm and 26600 μm, because the device area of finger type can be minimized. Constant current and saturation mobility methods are used for the definitions of threshold voltage and extractions of mobility as mentioned in chapter one.

Additionally, the surface morphology of pentacene was observed by scanning electron

microscope (SEM) and atomic force microscope (AFM). The electrical properties of the fabricated OTFTs were characterized using a Kiethley 4200 parameter analyzer in air.

Moreover, the contact resistances are extracted by transmission line method which is introduced in the chapter 1. The channel lengths are 10, 25, 50,and 100 μm, channel width is 600 μm. Pentacene TFTs were operated at linear region which the drain voltage was biased at -5 V for the extractions of contact resistance.

4.3.1 MWCNT Deposition Times and Thicknesses of Buffer Layer

4.3.1.1 Experiments

The detailed procedures of pentacene TFTs with MWCNT S/D in this section are similar to that in section 4.3. However, the deposition time and buffer layer thickness are varied in this section. The deposition times of MWCNTs are 3 and 5 minutes to observe the impacts on performance of pentacene TFTs with different MWCNT lengths. The lengths of the MWCNTs deposited for 3 and 5 min were confirmed through scanning electron microscopy (SEM). For the investigations of the influences on performance of MWCNTs with different growth times, Ti buffer layer is fixed at 10nm-thick.

Two kinds of Ti buffer layer thickness, which are 10 nm and 50 nm, are employed in this section. It is mentionable that the further influences of Ti buffer layer thickness on particle size of Fe catalytic layer during pretreatment are ignored**,** because different particle size of Fe catalytic layer might affect growth of MWCNTs.**[4.9-10]** For the investigations to the influences on performance of the buffer layer thicknesses, the MWCNT growth time was fixed at 5 minutes. After MWCNT growth, pentacene deposited at room temperature in this section.

4.3.1.2 Results and Discussion

Figure 4.3.1-1 (a), (b), and **4.3.1-2** depict the Id-Vg diagrams of pentacene TFTs with

MWCNT S/D with varied MWCNT growth times. These devices were operated at saturation region which drain voltage biased at -50 V, and the channel width/length of them are 75/50, 600/50, and 26600/50 μm/μm in the **Figure 4.3.1-1 (a)**, **Figure 4.3.1-1 (b)**, and **Figure 4.3.1-2**, respectively. From the results, the performances of pentacene TFTs with MWCNT growth time as 5 minutes display better performances than 3minutes. We supposed the reason of the phenomenon might be attributed to the increase of contact area, because the longer deposition time lead to longer MWCNTs contributed to the larger contact area.

The threshold voltage and mobility of these devices are extracted by constant current method which had introduced in chapter 1. The highest saturation mobility extracted from the devices with channel width/length was 75/50 μm/μm was about 0.14 cm^2/Vs, and threshold voltage was -6.5 V. The highest on/off current ratio is about 5.56×10^6 extracted form devices with channel width/length was 26600/50 μm/μm.

In **Figure 4.3.1-3 (a)** and **(b),** the lengths of grown MWCNTs were confirmed by SEM to be around 300nm and 1μm for 3-minute and 5-minute depositions, respectively. **Figure 4.3.1-4 (a)** and **(b)** show the images are observed through SEM of top view of MWCNTs S/D which is at junction of S/D and gate dielectric. The SEM images of the two different MWCNT growth times after deposited pentacene are shown in **Figure 4.3.1-5 (a)** and **(b)**. The transition region of pentacene active layer could also be observed near the MWCNT S/D. **Figure 4.3.1-6 (a)** and **(b)** depict cross section view of MWCNT S/D after deposited pentacene.

Figure 4.3.1-7 (a), (b), and **4.3.1-8** are the Id-Vg diagrams of pentacene TFTs with MWCNT S/D with varied thicknesses of Ti buffer layer, and these devices were operated at saturation region which drain voltage biased at -50 V. The channel width/length are 75/50, 600/50, and 26600/50 μm/μm in **Figure 4.3.1-7 (a)**, **Figure 4.3.1-7 (b)**, and **Figure 4.3.1-8**, respectively. From the results, the Ti buffer layer thickness with 10 nm displayed better performances than 50 nm. The reason for this phenomenon could attribute to lager barrier for

the carrier inject from pentacene to S/D when the thickness of Ti buffer layer became thicker.**[4.11]**

Figure 4.3.1-9 illustrates the R_{tot}-L diagram of pentacene TFTs with MWCNT S/D, which the MWCNT growth times are 3 and 5 minutes with thickness of Ti buffer layer is 10 nm. When the channel length was approached to 0 μm, the value of R_{tot} was around 3×10^8 Ω μm or 30 kΩ cm.

4.3.2 Pentacene TFTs with MWCNT and Only Pre-Treatment S/D

4.3.2.1 Experiments

From the results of section 4.3.1, we found pentacene TFTs with MWCNT S/D exhibited superior performances. However, additional evidences to demonstrate the superior performances were contributed by MWCNTs S/D are necessary. Because there are still uncertain to confirm that the superior performances were not contributed by catalytic layer. Therefore, by comparing the electrical characteristics of pentacene TFTs with MWCNT S/D and only pre-treatment S/D, i.e., no MWCNT growth time, we could analysis and demonstrate that. The other fabrication procedures of pentacene TFTs with or without MWCNT S/D are similar to that in section 4.3.

4.3.2.2 Results and Discussion

Figure 4.3.2-1 (a), **(b)**, and **4.3.2-2** illustrate the I_d–V_g characteristics of the OTFTs prepared with and without MWCNT coverage on the S/D region. The channel width/length in **Figure 4.3.2-1 (a)**, **(b)**, and **4.3.2-2** are 600/100, 600/10, and 26600/ 50 μm/μm. It is clear that the performance of the OTFTs was improved significantly after incorporating the MWCNTs. We believe that this behavior is related to three factors: (1) the difference between the work functions of Fe (ca. 4.5 eV) and pentacene is larger than that between MWCNT (4.7 ± 0.4 eV) and pentacene;**[4.7]** (2) the MWCNT/pentacene system probably possesses better contact

properties than the metal/pentacene system, as might be expected from a previous finding that pentacene molecules, when deposited onto SWCNT electrodes, stack on the surface of the SWCNTs in a commensurate configuration as a result of favorable π–π interactions;**[4.8]** (3) the contact area induced by the presence of MWCNTs was increased tremendously. All of these factors would contribute to the smaller contact resistance and, in turn, improve the device performance.

Figure 4.3.2-3 (a) and **(b)** were the AFM images, the morphology of pentacene active layer deposited on only pretreatment S/D and junction of only pretreatment S/D and gate dielectric can be observed from them.

4.3.3 Pentacene TFTs with MWCNT and Pd/Ti S/D

4.3.3.1 Experiments

From the results in the front two sections, pentacene TFTs with MWCNT S/D exhibited superior performance. Furthermore, the comparisons of pentacene TFTs with MWCNTs and Pd/Ti S/D are presented in this section.

The fabrication procedures in this section are similar to that in section 4.3, but the thickness of gate dielectric, which is silicon dioxide prepared by thermally dry oxidation, is changed to 200 nm. For the S/D of pentacene TFTs, the growth time of MWCNTs is 5 minutes, and the thickness of Pd/Ti which prepared by E beam thermal evaporation is 50 nm/ 2.5 nm with the deposition rate of 0.03 nm/s. After preparations of S/D, pentacene active layer was deposited by thermal evaporator with two kinds of deposition temperatures which are room temperature and 90 ^{o}C. Both pentacene TFTs with MWCNT or Pd/Ti S/D were deposited pentacene thin film in the same run in order to reduce variability.

4.3.3.2 Results and Discussion

Figure 4.3.3-1 (a), **(b)**, and **Figure 4.3.3-2** are the Id-Vg electrical characteristics of

pentacene TFTs with MWCNT and Pd/Ti S/D and with different device scales and pentacene deposition temperature. All the channel length employed in **Figure 4.3.3-1 ~ 2** is 50 μm, but channel width are 75, 600, and 26600 μm in **Figure 4.3.3-1 (a)**, **(b)**, and **Figure 4.3.3-2**, respectively. As shown in these figures, the drive current of pentacene TFTs with MWCNT S/D are one order larger than Pd/Ti S/D.

The extractions of optimum mobility, threshold voltage, subthreshold swing and on/off current ratio of pentacene TFTs with MWCNT (and Pd/Ti) S/D were nearly 0.16 (0.019) cm^2/Vs, -3.5 (-3.5) V as shown in **Figure 4.3.3-1 (a)**, and nearly 0.61 (0.62) V/decade, 10^7 (10^6) V/V as shown in **Figure 4.3.3-2**.

Figure 4.3.3-3 (a) and **(b)** illustrate the R_{tot}-L diagrams of pentacene TFTs with MWCNT and Pd/Ti S/D with pentacene deposition temperature of 90 ^oC. When channel length was approached to 0 μm, the value of R_{tot} was around 3×10^8 Ω μm or 30 kΩ cm for MWCNT S/D and 10^{10} Ω μm or 1000 kΩ cm for Pd/Ti S/D. **Figure 4.3.3-4** is the extractions on mobility of pentacene TFTs with different device scales and pentacene deposition temperatures.

4.4 Summary

From the results in section 4.3.1, MWCNTs could increase contact area and reduce contact resistance. Moreover, thin Ti buffer layer reduced carrier injection barrier. Pentacene TFTs with MWCNT S/D exhibited high carrier mobility, on/off current ratio, and low contact resistance. In our work, pentacene TFTs with MWCNT S/D with 10-nm-thick of Ti buffer layer and 5 mins of MWCNT growth time had the optimum performance.

Furthermore, by comparing the performances of pentacene with MWCNT S/D and only pre-treatment S/D as show in section 4.3.2, superior performances could attribute to the employment of MWCNTs. MWCNT S/D possessed good contact properties and small work function difference between pentacene and MWCNTs, and increasing contact area. All these

contributed to the small contact resistance which improved the performance.

Finally, by comparing electrical characteristics of pentacene TFTs with MWCNT and Pd/Ti S/D in section 4.3.3, the drive current of that with MWCNT S/D were one order larger than Pd/Ti S/D. The improvement could be attributed to the reduced contact resistance of pentacene TFTs with MWCNT S/D.

Chapter 5

Conclusions

5.1 Conclusions

In chapter one, we found the performances of pentacene TFTs would be influenced by the deposition conditions and thickness of pentacene active layer. From the results, high deposition temperature and low deposition rate of pentacene might improve film-quality and reducing defects. By using low deposition rate which is 0.03 nm/s, the highest mobility could be improved from 0.005 to 0.01 cm^2/Vs. Furthermore, by using high deposition temperature which is 90 ^oC, the highest mobility could be improved from 0.01 to 0.013 cm^2/Vs. Besides, we found that pentacene TFTs with appropriate thickness of pentacene active layer, which was 40 nm, exhibited highest performance. The highest mobility of devices with 40-nm-thick of pentacene and 90 ^oC of deposition temperature was improved from 0.013 to 0.019 cm^2/Vs when compared to that with 60-nm-thick of pentacene and 90 ^oC of deposition temperature. Additionally, the degradation on performance of pentacene TFTs were also observed. The degradation on performance might be attributed to the existence of accept-like trap states in pentacene active layer which might result from the oxidation of moisture on pentacene which formed the –OH bonding on pentacene surface and grain boundaries. The highest mobility was reduced from 0.013 to 0.0015 cm^2/Vs, and the threshold voltage exhibited serious voltage shift which were about -30 V.

After the discussions of impacts on performance of pentacene active layer, the influences on performances of pentacene TFTs of the contact properties between pentacene and contact metal and the injection barrier which were induced by the work function difference were investigated in chapter two. From the result, we found that pentacene TFTs with thin (2.5 nm)

Ti adhesion layer exhibited several times of improvement which compared to that with thick Ti adhesion layer (10nm). This tendence could be observed when different contact materials were employed. The highest mobility of pentacene TFTs with Pd/Ti and Au/Ti S/D with 2.5-nm-thick of Ti adhesion layer were 0.002 and 0.0018 cm^2/Vs. Accordingly, we also found that different contact materials had significant difference of contact properties which would impact the performance. It seems that pentacene TFTs with Pd/Ti S/D would have better performance than that with Au/Ti S/D. Additionally, HMDS surface treatment on surface of gate dielectric to improve performance were also studied in the last section of this chapter. The pentacene TFTs with HMDS surface treatment had obvious improvement. The highest mobility of pentacene TFTs with and without HMDS surface treatment were 0.007 and 0.002 cm^2/Vs.

In chapter four, we introduce MWCNTs to be the contact material of pentacene TFTs. From the results, we found that superior performances could be obtained by using MWCNTs to be the S/D of pentacene, because of reduced contact resistance and improved contact properties. By the employments of long deposition times (5 minutes) of MWCNTs and thin (10 nm) buffer layer, superior performance could be obtained. Because large length of MWCNTs could reduce contact resistance, and large injection barrier which was induced by Ti buffer layer could be avoided when reducing the thickness of Ti buffer layer as the results in chapter three. The highest mobility of pentacene TFTs with MWCNT S/D was 0.14 cm^2/Vs, while the deposition time and thickness of buffer layer was 5 minutes and 10 nm. Furthermore, the contributions of superior performances of pentacene TFTs which resulted from employment of MWCNTs were confirmed by comparing to the performance of that with only pretreatment S/D. Moreover, we found the performances of pentacene TFTs with MWCNT S/D were better than that with Pd/Ti S/D, which could attribute to the effective reduction of contact resistance.

For conclusions, high performances of pentacene TFTs could be realized by controlling

deposition conditions of pentacene active layer, reducing the thickness of Ti adhesion layer, and incorporating MWCNTs to be the contact materials.