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碩 士 論 文

奈米應變矽CMOS元件之通道背向散射特性與可靠度之相關性研究

The Channel Backscattering Characteristics of Nanoscale Strained-CMOS and Its Correlation to the Reliability

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摘要

近幾年，由於應變矽元件有較大的電子漂移率，所以被視為是高速和低功率邏輯CMOS有潛力的元件之一。且應變矽在不同的方向上會有不同的特性曲線，利用最佳的方向組合來達到最佳的元件特性將會是未來應變矽元件的一個方法。

本論文中，將在此探討藉由應變工程而造成驅動電流提升的彈射範圍內的CMOS元件。這會由兩個重要的參數來決定：入射速度(V_{inj})以及通道散射係數(r_c)不同的應變方向以及在最大的電流移動率提升的通道/基板方向做實驗的驗證。對於NMOS 而言，結果顯示出利用CESL單軸方向的張力型應變比利用矽鍺當作基板之雙軸方向的張力型應變在驅動電流的提升上較有效率。對於PMOS而言，評估在不同結構的擠壓型應變用於單軸與雙軸的結構，不同於PMOS在應變工程上通道散射係數(r_c)無法有效的提升，我們首次發現，利用單軸擠壓應變與雙軸擠壓應變矽元件上，在入射速度以及反射係數兩者都有增加的效果。這些結果用在設計高性能應變矽元件上，可以提供一個設

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計指標。

我們將此理論應用於可靠度上，藉由分析載子的入射速度與所遭遇的位元障高低來做判斷。結果顯示：擁有越大速度且遭遇較小位能的載子，會有較多的機會在行經汲極區域時發生與晶格的碰撞，進而產生「衝擊離子化」，形成電子電洞對，進而造成元件氧化層的傷害。實驗結果發現擁有越好特性的元件其可靠度也較差。

The Channel Backscattering Characteristics of Nanoscale Strained-CMOS and Its Correlation to the Reliability

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ABSTRACT

In more recent years, strained-Si device has been evolved as a potential candidate for high speed and low power logic CMOS technologies as a result of the mobility enhancement in devices. Also, there will be different performance using strained-Si on different orientation. The combination of strained technique with orientation is the best approach so far for the 65nm CMOS Technology and beyond.

In this thesis, the strain engineering and its correlation to the drive current enhancement of CMOS devices in the ballistic regime has been examined. It was characterized by two parameters, the reflection coefficient and the injection velocity. Experimental verification on very high mobility n-and p-MOSFET on channel/substrate orientations with various strain have been made. For nMOSFETs, it shows that uniaxial tensile-stress using CESL is more efficient in current enhancement than the biaxial stress with bulk strained-SiGe technique. In terms of the reliability, by examining the injection velocity of the carriers and the barrier height, it was found that while carriers with larger injection velocity and lower barrier shows

worse reliability.

For the pMOSFETs, backscattering coefficient can not be improved, on the contrary. Experimentally, compressive stress using uniaxial or biaxial has been evaluated for various structures. It was found for the first time that both reflection coefficient and the injection velocity can be enhanced with a specific structure of the device.

Subsequently, we apply this theory to investigate the device reliability, by examining the injection velocity of the carriers and the potential barrier of the carrier. It shows that the carriers posse higher injection velocity and encounter lower potential barrier will have higher probability to collide the lattice when transporting to the drain region. As a consequence, the aforementioned collision causes the “impact ionization” to generate the electron-hole pairs, which then makes worse the gate oxide damage. Results show that the device with better current enhancement exhibits much worse reliability.

誌　謝

兩年的實驗室生活是精采豐富的，但同時也充滿艱辛與汗水。首先要感謝的是我的指導教授：莊紹勳教授，老師給予的生活上與專業上的指導與建議，讓我在學業上與研究上獲益良多並學習到對事物應有的嚴謹態度以及處理方法。除此之外，對於課業外的生活技能、觀念的督促，讓我必須在此表達感謝之意。

感謝已畢業的冠德、又仁學長當我在實驗遇到瓶頸和挫折時，總是能在電話那端指導，並給予支持與鼓勵。也感謝在兩年研究生涯中，與我起嚐遍酸甜苦辣的同學，包括耀賢、大正與元亨，我們一起經歷困苦的研究過程，相信數年後再聚首，一定倍感溫馨。對於汪老師研究群的同學，即使我們身在不同的研究群，但我們的感情就像是一家人一樣，希望以後在業界相遇時還能保有我們現在的真誠，也祝福達達、志昌小馬能夠順利取得博士學位，此外也感謝家銘、小郭、友良、文彥與易叡，感謝有你們這群學弟平日對於實驗室的付出，使學長們能夠專心於研究上，在此，輕遞一份真摯的祝福，希望明年亦能看見你們順順利利的畢業。

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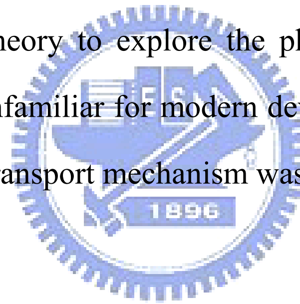
Fig. 5.2 The roadmap of reported injection velocity versus channel lengths. To achieve thermal velocity limit, lots of work still need to be studied.

Chapter 1
Introduction

1.1 The Motivation of This Work

The device scaling to the physical limit has become a major challenge faced by device engineers. Recently the backscattering model [1] was outlined to explore the mesoscopic carrier transport in nanoscale MOSFET. And the effective mobility of inversion carriers is an important parameter in traditional theories of MOSFET but its significance in MOSFET of nanoscale dimensions, where off-equilibrium (velocities overshoot) and quasi-ballistic transport dominate and are less clear. So, we need to use channel backscattering theory to explore the physics of the nanoscale MOSFET. This simple conceptual model may seem unfamiliar for modern device engineers but it is not a new one. In fact, the conventional semiconductor transport mechanism was built in the 1960 and 1961 by Mckelvey [2] and Schockley [3].



In the past several years, various strain techniques are actively pursued to give the device performance a booster in the 90nm node and beyond [4] [5] [6]. Mobility enhancement induced by the strain in the channel has been widely characterized, however, only half of the mobility enhancement is needed to account for the observed saturation drain current increase.

So far, many research groups have paid much attention to the theories, such as velocity overshoot, thermal or ballistic limit, and mobility dependencies [7] [8] [9]. In particular, recent efforts have been paid on the strain engineering and hybrid substrate technology and process induced stress. This technique should therefore be more appropriate for evaluating how close to modern MOSFET when operates to the thermal limit.

The enhancement of the drive current fully relies on the mobility enhancing schemes. It also aroused much interest on which scheme or strain is most useful. So far, only a few studies have been paid on the study of one kind of devices, such as either n-MOSFET or p-MOSFET only. With focus on these two important parameters .To understand the correlation between carrier transport and the strain engineering, much effort still needs to be done for a general design of high performance strained CMOS devices.

1.2 Organization of This Thesis

This thesis has been divided into five chapters. Chapter 2 describes the devices used in this work and experimental setup. The channel backscattering experimental flow chart in Fig. 1.1 is used to extract the two parameters. Also the model description will be illustrated in chapter 2.

In Chapter 3, we will report the impacts on device characteristics, as a result of uniaxial and biaxial strain for nMOSFET. Also, we will examine the pMOSFET with various combination of uniaxial and biaxial strained techniques.

In chapter 4, we observe the relationships of those two important parameters with the reliability. In general, the carriers have higher energy which will cause the oxide damage serious. Combining B_{sat} and V_{inj}, we can use it to predict how the reliability of the test devices shows.

Finally, a summary and conclusion are given in Chapter 5.

Chapter 2
Device Fabrication and Experimental Measurements

2.1 Introduction

As CMOS devices scale down, new materials or devices structures are required to overcome the scaling barriers and enhance device performance. The SiGe or Ge has been considered to be a potential option due to their high intrinsic mobility. 6-25X hole mobility enhancement over Si have been reported using strained-Ge channels [10] [11] [12] [13]. Moreover, it is well known that hole mobility is more than double at <110> channel direction on (110) surface [14]. In addition, electron shows higher performance on <110>/(100) direction. Hence, the hybrid substrate is a popular technique for high performance logic applications [14]. In Fig. 2.1, the structure of this technique is pMOSFET made on (110) substrate while nMOSFET on (100) substrate.

Therefore, to further enhance the pMOSFET performance for modern VLSI applications, strain technique on (110) substrate will be a compromising choice as shown in Fig 2.2, which is the devices we measured in this work.

As for nMOSFET, uniaxial and biaxial strained devices have been used in this work For uniaxial strained sample is made by silicon nitride capping layer as a stressor to tensile the channel and biaxial strain is generally grown on thick relaxed/graded $Si_{1-x}Ge_x$ buffer virtual substrate. The schematic cross section of the strained-Si nMOSFET used in this chapter is shown in Fig. 2.4

In this chapter, first, we will describe the manufacturing process for strained devices. Then, we will illustrate the experimental setups to characterize the test device, which include the instrumental scheme, various experimental skills, and temperature dependent experiment.

pFET on (100) SOI, nFET on (100) epi-layer
nFET on (100) SOI, pFET on (110) epi-layer

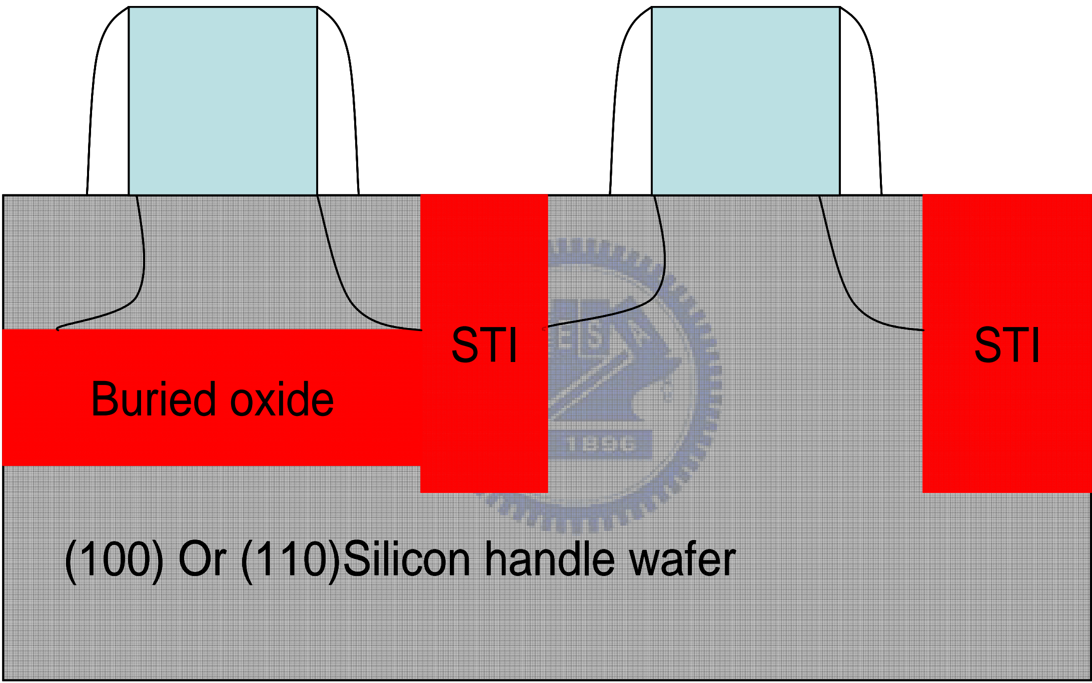


Fig. 2.1 The Schematic cross-section of CMOS on a hybrid-substrate with pFET on (110) substrate orientation and nFET on (100) substrate orientation.

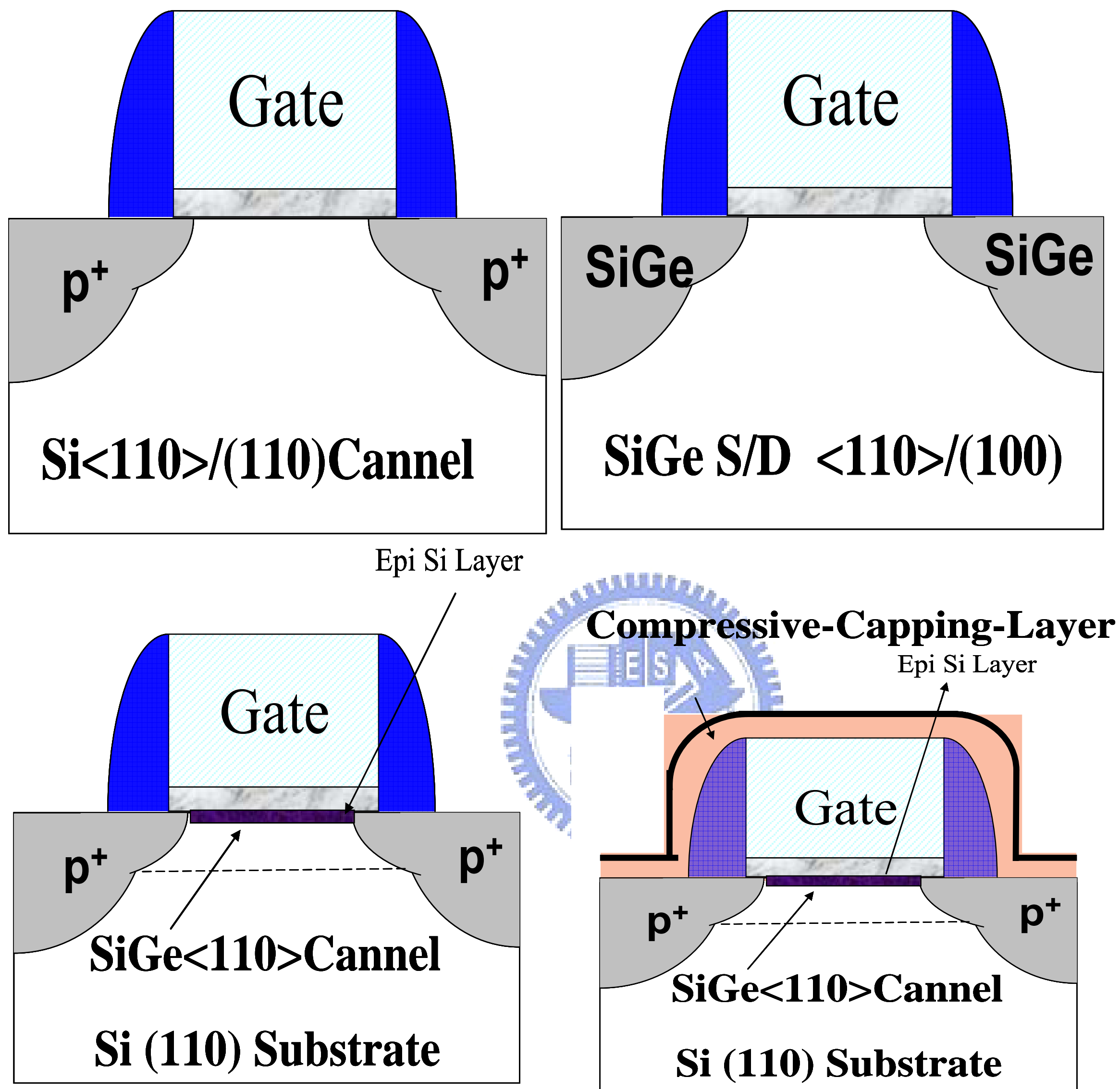


Fig. 2.2 The device cross session view of pMOSFET, (a) the control device, (b) SiGe in S/D region, (c) SiGe channel , and (d) SiGe channel + CESL.

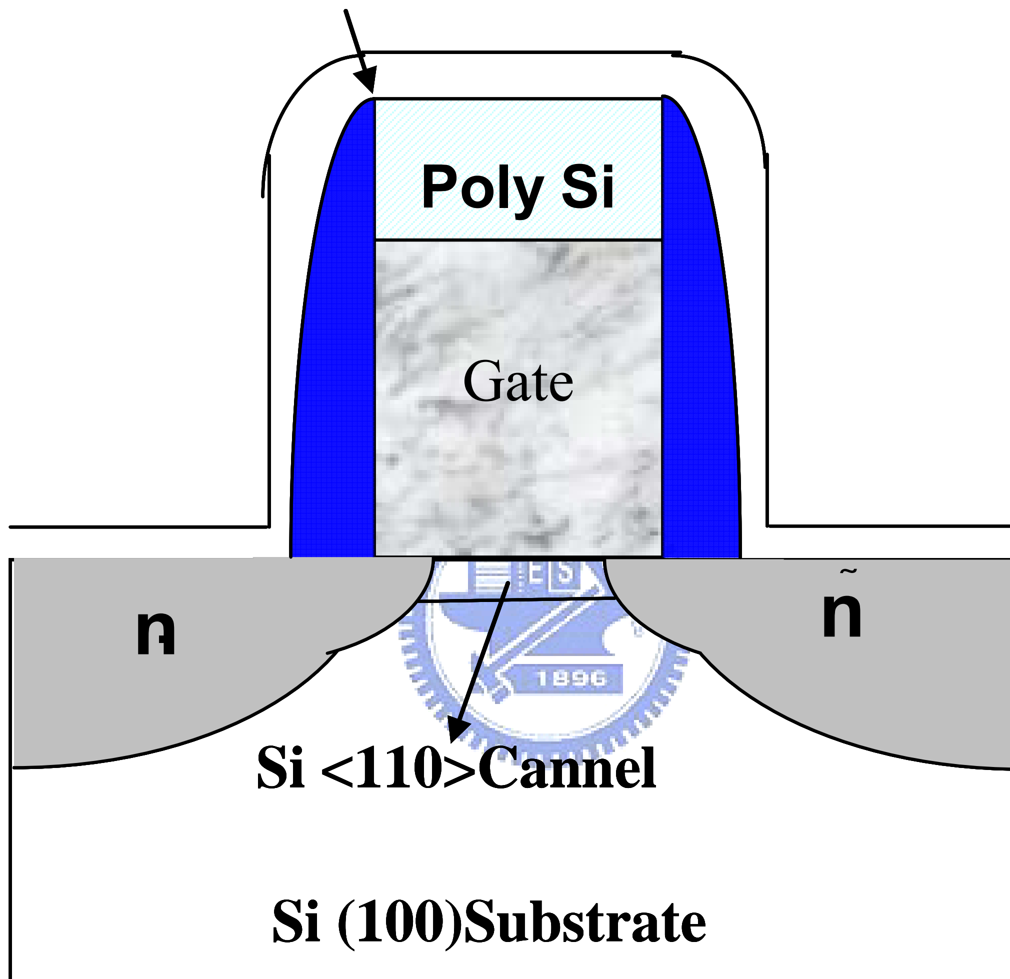


Fig. 2.3 The cross section view of uniaxial strained nMOSFET.

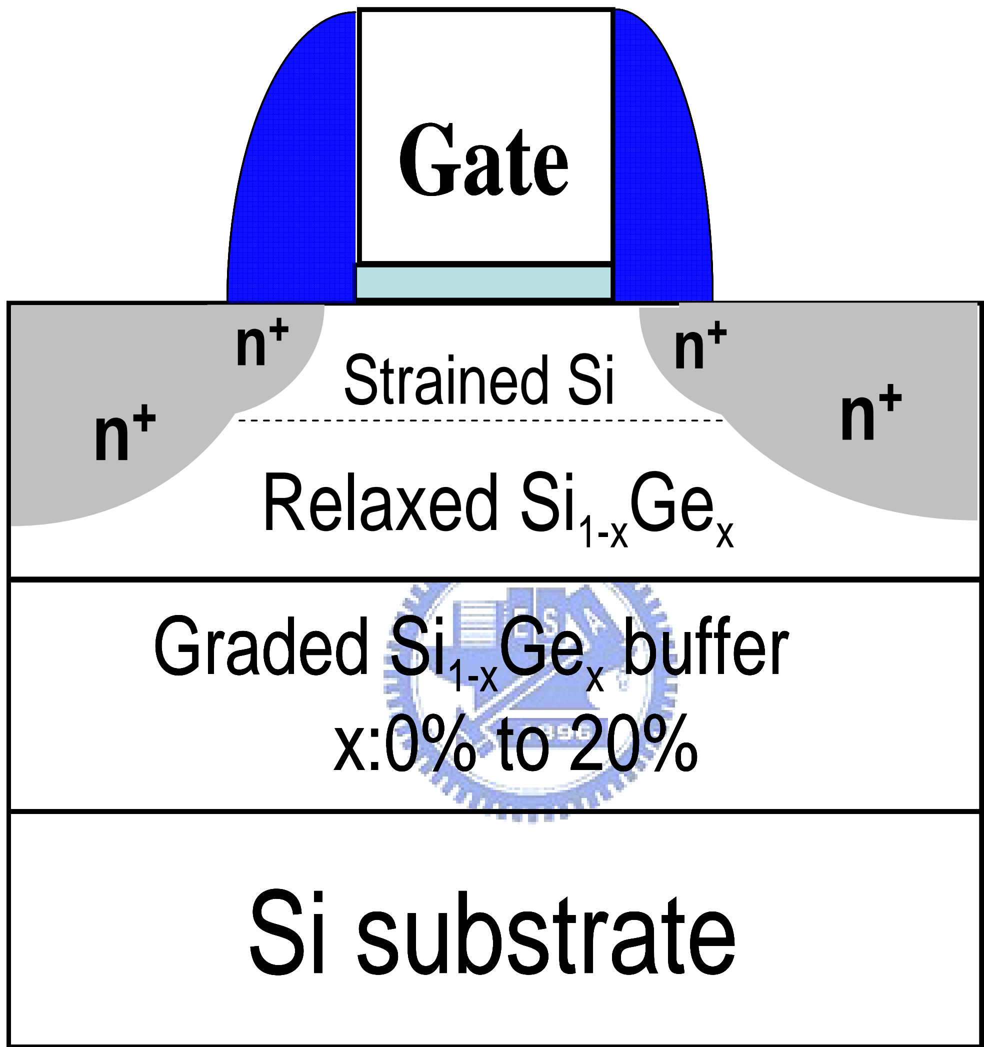


Fig. 2.4 The schematic cross section of the biaxial strained-Si nMOSFETs.

2.1 Device Fabrication

The testing devices in this experiment are the best channel/substrate orientations of CMOS. In nMOSFET, <110>/(100) uniaxial tensile strained-Si and biaxial tensile strained-Si channel were fabricated in state-of-art process. On the other hand, for pMOSFET is on <110>/(110) orientation [14]. Table 2.1 shows the summary of the best orientations of n- and p-MOSFET.

2.1.1 Fabrication of nMOSFET

The biaxial strained nMOSFET devices were fabricated on bulk Si substrate and relaxed SiGe virtual substrate with a tensile strained Si capping layer. The V_T shift due to enhanced arsenic diffusion in the SiGe buffer was controlled by a modified halo implant and an optimized dopant anneal process. A nickel silicide process was adopted to avoid the problem of Ge segregation during silicide formation on SiGe. These test devices were made with the same physical thickness (16Å) of nitrided gate oxide and with different channel lengths. The relaxed Si_{1-x}/Ge_x is at x=20% and with Si cap layer thickness 100Å. Both technologies used the same processes except for the channel engineering to match the V_T shift.

Uniaxial tensile strain in nMOSFET is using nitrided capping layer which was deposited upon the gate region to introduce tensile strain to the channel. The process flow is the same with the standard nMOSFET, bur the difference is that after gate silicidation we deposit the SiN capping layer on gate.

2.1.2 Fabrication of pMOSFET

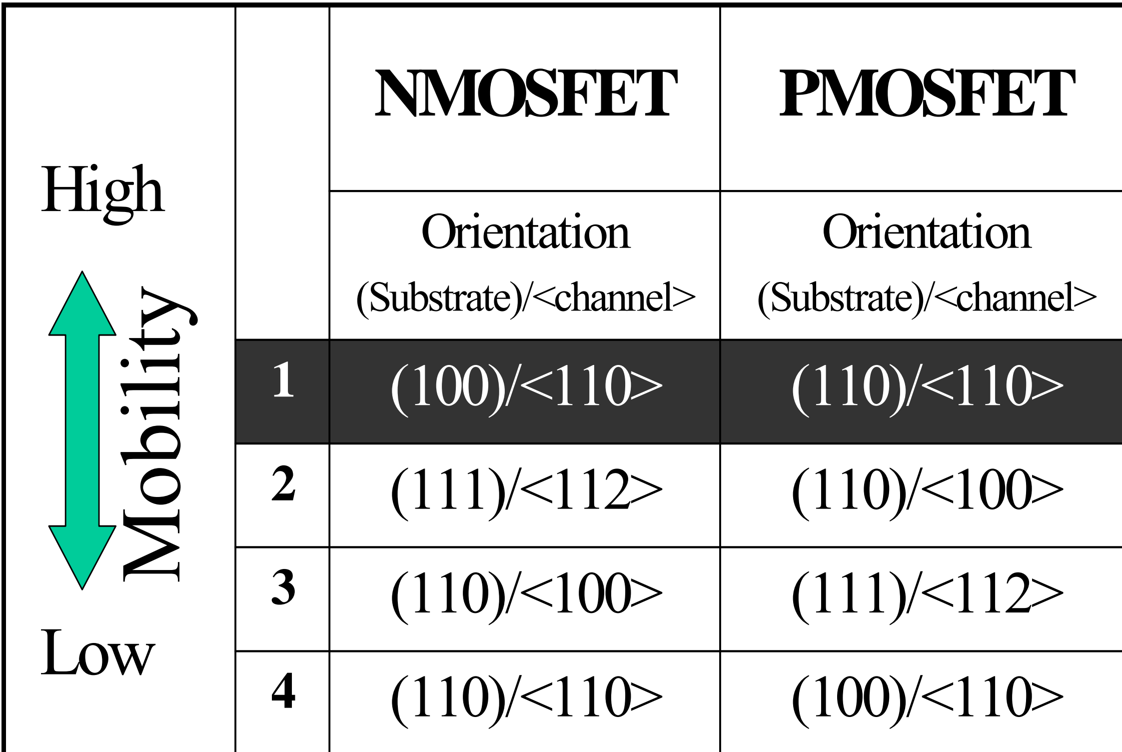
For pMOSFET, starting form (110) Si substrate, the 8nm $Si_{0.7}Ge_{0.3}$ channel with 5nm Si cap were

selectively grown on the active region after isolation and well implant process. The Si cap was used to form high quality nitridated oxide layer. The <110> channel direction was adopted for fabricated devices. After nickel salicidation, 1000A compressive (-2Gpa) or tensile (+1.1Gpa) capping layer was deposited to server as the contact etch stop layer (CESL). That is the process flow of SiGe and SiGe+CESL device.

As for SiGe refill at source and drain region device, also it was fabricated in the state-of-the art process, by inserting a Si recess etch and selective epitaixial $Si_x Ge_{1-x}$(x=0.17) deposition post-spacer formation into a standard logic technology process flow. The mismatch in the $Si_x Ge_{1-x}$ to Si lattice causes the p-type MOSFET to be under compressive strain.

2.2 Fundamental Experimental Setup

The experimental setup for the Current-Voltage measurement of n- and p-MOS devices is illustrated in Fig. 2.5. Based on the computer controlled instrument environment, the complicated and long-term characterization procedures for analyzing the intrinsic and degradation behavior in MOSFET can be easily achieved. As shown in Fig. 2.5, the characterization equipments that connected by Co-axial and Tri-axial cable, including the semiconductor parameter analyzer (HP 4156C), the low leakage switch mainframe (HP E5250A), the cascade guarded thermal probe station, and thermal controller, provide an adequate capability for measuring the low leakage device I-V characteristics.



Mobility (High → Low)		NMOSFET	PMOSFET
		Orientation (Substrate)/<channel>	Orientation (Substrate)/<channel>
High	1	(100)/<110>	(110)/<110>
	2	(111)/<112>	(110)/<100>
	3	(110)/<100>	(111)/<112>
Low	4	(110)/<110>	(100)/<110>

Tab. 2.1 The combination of mobility for hybrid CMOS technology. Group one has the highest mobility and Ion enhancement.

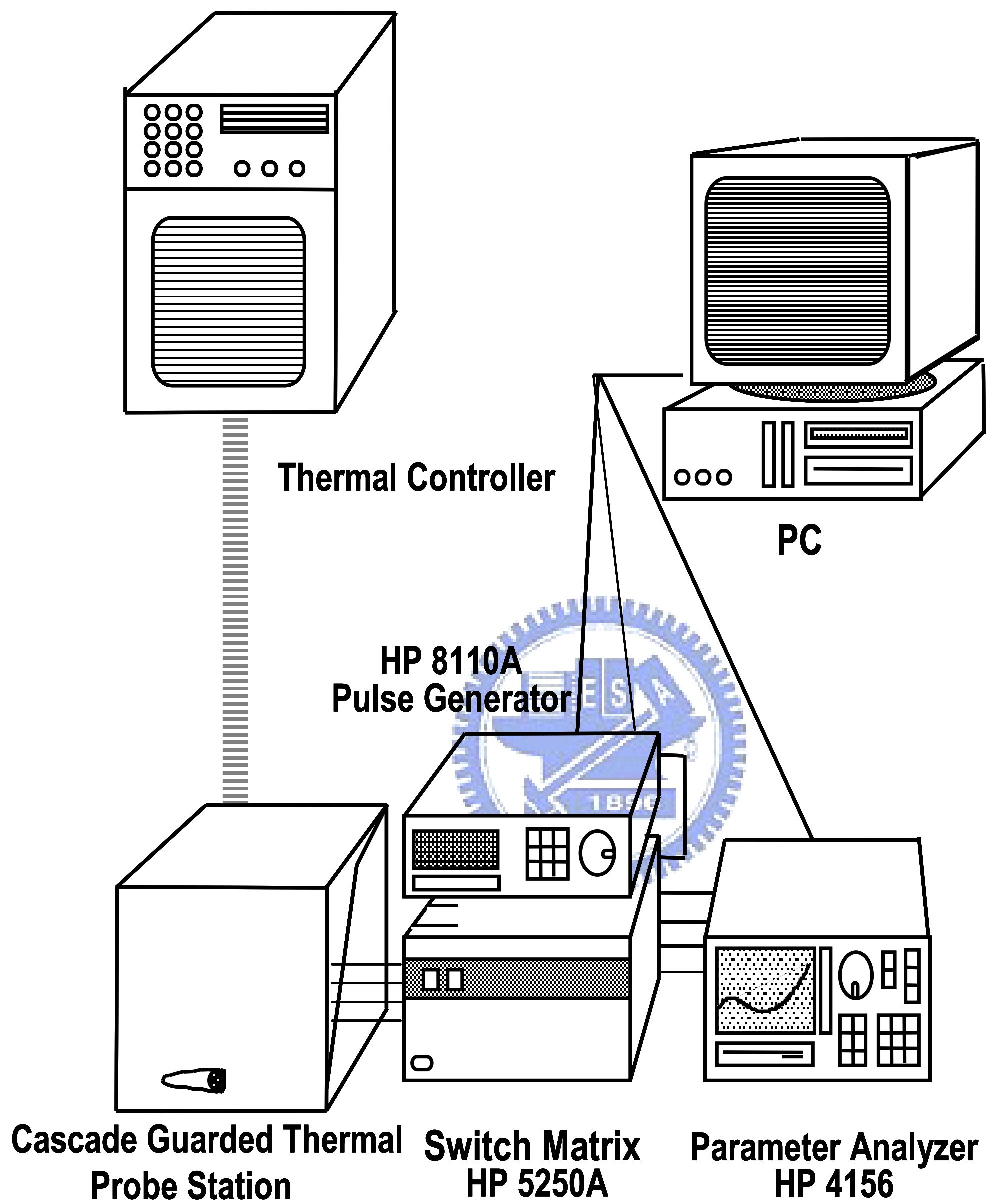


Fig. 2.5 The experimental setup for the current-voltage measurement of n- and p-MOSFET.

2.3 Charge Pumping Measurement

2.3.1 Basic Experimental Setup

The basic setup of charge pumping measurement is shown in Fig. 2.6. The source, drain and bulk electrodes of tested devices are grounded. A 1MHz (the frequency can be modulated for different devices) square pulse waveform provided by HP8110A with fixed base level (V_{gl}) is applied to the NMOS gate, or with fixed top level (V_{gh}) is applied to the PMOS gate. We keep V_{gl} at –1.0V while increase V_{gh} from –1.0V to 1.0V by step 0.1V, or keep V_{gh} at 1.0V while decrease V_{gl} from 1.0V to –1.0V by step –0.1V. With a smaller voltage step, we get a higher profiling resolution. The parameter analyzer HP4156C is used to measure the charge pumping current (I_{CP}).

2.3.2 Basic Theory

The charging pumping principle for MOSFET has been applied to characterize the fast interface traps in MOSFET. The original charge pumping method was introduced by Brugler and Jespers, and the technique was developed by Heremans [2]. This technique is based on a recombination process at the Si/SiO_2 interface involving the surface traps. It consists of applying a constant reverse bias at the source and

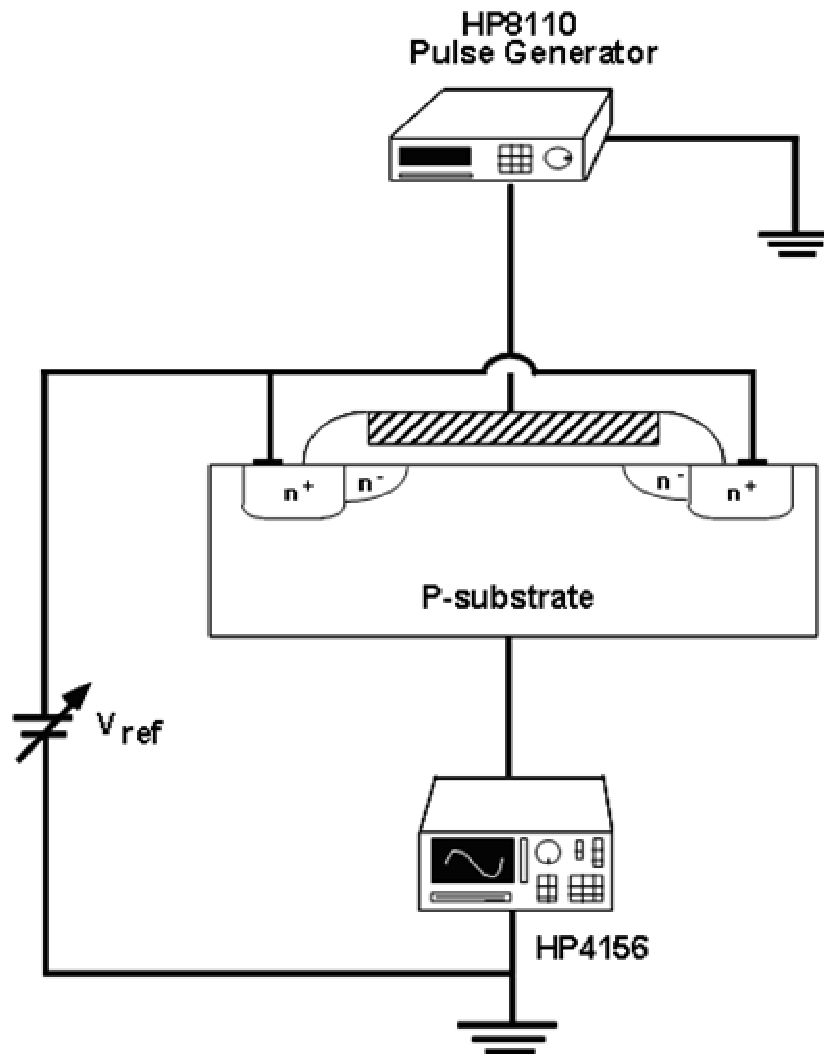


Fig. 2.6 The experimental setup and environmental for basic I-V measurement of MOSFET.

drain, while sweeping the base level of the gate pulse train from a low accumulation level to a high inversion level. The frequency and the rise/fall time are kept constant. When the base level is lower than that flat-band voltage while the top level of the pulse is higher than the threshold voltage, the maximum charge pumping current occurs. This means that a net amount of charge is transferred from the source and drain to the substrate via the fast interface traps each time the device is pulsed from inversion toward accumulation. The charge pumping current is caused by the repetitive recombination at interface traps. As a result, the recombination current measured from the bottom (substrate) is the so-called charge pumping current [3]. The CP current can be given by:

$$I_{CP} = q \cdot f \cdot W \cdot L \cdot N_{IT}. \tag{2.1}$$

According to this equation, the current is directly proportional to the interface trap density in the channel, the frequency, and the area of the device. However, when the top level of the pulse is lower than the flat-band voltage or the base level is higher than the threshold voltage, the fast interface traps are permanently filled with holes in accumulation or the electrons in inversion in n-MOSFET, which no holes reach the surface at the time, respectively. As a result, there is no recombination current and then the charge pumping current cannot be discovered.

Charge pumping measurements can be performed with several different ways. For our experimental requirement, we perform the charge pumping measurement by applying a gate pulse with the fixed base voltage (V_{gl}) and increasing the pulse amplitude. While the channel operates between accumulation and inversion as the fixed base voltage lower than flat-band voltage and high voltage above the threshold voltage respectively; this gives rise to the charge pumping current (I_{CP}) from the bulk and reaches saturation situation. If we use another method which changes base voltage with fixed pulse amplitude, the current saturation region is not extensive enough for research because of the limit

that the saturation current happens only when the gate pulse train from a low accumulation level to a high inversion level.

2.3.3 Principle of the Low Leakage IFCP Method

Figures 2.7 (a) and (b) show the schematic of a low leakage IFCP measurement for CMOS developed by our group in [4]. With both S/D grounded and by applying a gate pulse with a fixed base level (V_{gl}) and a varying high-level voltage (V_{gh}) for NMOS, the channel will be switched between the accumulation and inversion. This gives rise to the charge pumping current I_{CP} (=I_B) measured from the bulk. From Fig. 2.3, when t_{ox} >30Å, the leakage current I_G of I_{CP} is very small. However, when t_{ox} is slow down than 20Å, the leakage current I_G is unavoidable. The unexpected leakage current will influence our research. From the measured I_{CP} at two frequencies, f_1 and f_2, can be expressed as

$$I_{CP,\ f1\ with\text{-}leakage} = I_{CP,\ f1\ correct} + I_{CP,\ leakage@f1} \quad (2.1)$$

and

$$I_{CP,\ f2\ with\text{-}leakage} = I_{CP,\ f2\ correct} + I_{CP,\ leakage@f2}. \quad (2.2)$$

When the frequency is sufficiently high, the leakage components in these two frequencies are almost the same ($I_{CP,\ leakage@f1} \approx I_{CP,\ leakage@f2}$). We then take the difference of I_{CP} ($\Delta I_{CP,\ f1-f2}$) between two frequencies. From equations (2.1) and (2.2), the difference of these two CP curves gives

$$\Delta I_{CP,\ f1-f2} = I_{CP,\ f1\ with\text{-}leakage} - I_{CP,\ f2\ with\text{-}leakage}. \quad (2.3)$$

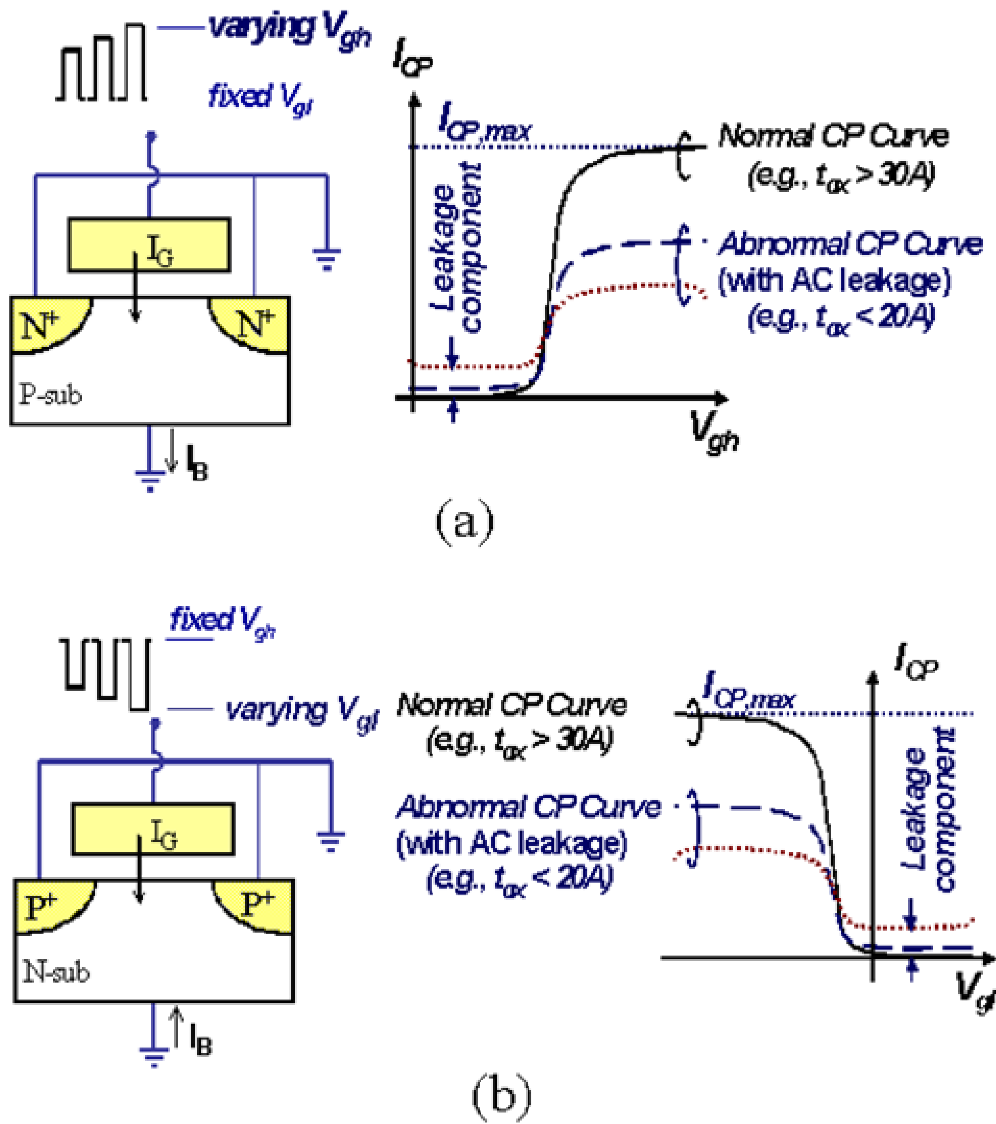


Fig. 2.7 The schematic diagram of charge pumping for

(a) nMOSFET measurement

(b) pMOSFET measurement ,

Induced leakage current (I_G) occurs when t_{ox}<20A

Since the correct CP curve is directly proportional to the frequency, it will be equal to the difference of two CP curves. Therefore, in the IFCP method, the correct CP curve at frequency ($f1- f2$) can be given by

$$I_{CP,\ f1-f2} = \Delta I_{CP,\ f1-f2}. \qquad (2.4)$$

For example, $I_{CP(2MHz)} - I_{CP(1MHz)}$ is regarded as the I_{CP} at their difference frequency, 1MHz. The result of the charge pumping measurement for the strained-Si device is shown in Fig. 2.4 curve (1) and curves (2). From this figure, we can find a huge gate leakage current appears in the charge pumping cure when the voltage of gate pulse is higher than 1V. Because the correct charge pumping current is directly proportional to the frequency of gate pulse and the leakage of current is irrelevant to the frequency, so we can receive the correct charge pumping current by taking the difference of the measured I_{CP} between two frequencies theoretically. To see the result, we finally get a correct curve with commonly known saturation charge pumping current, curve (3), in Fig. 2.4.

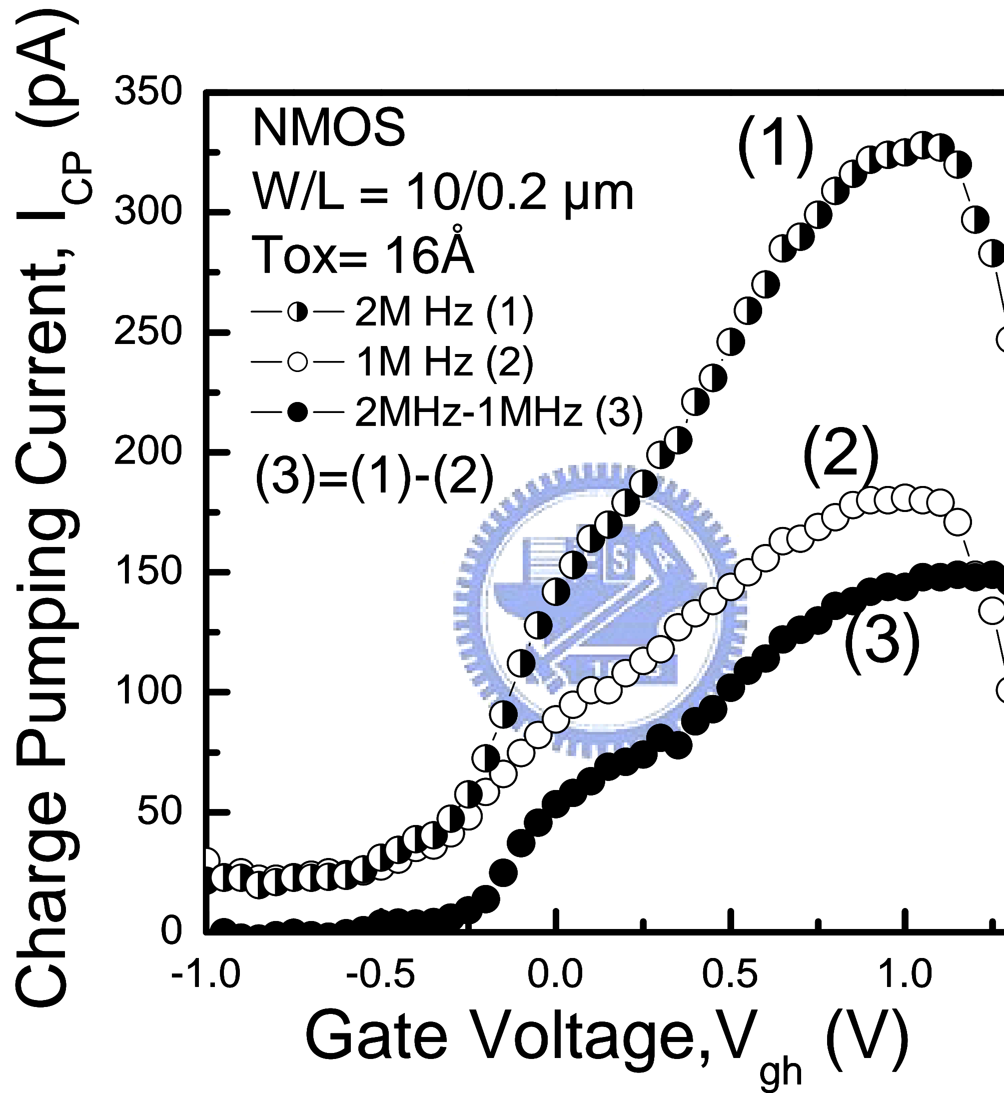


Fig. 2.8 Measurment of I_{cp} at two different frequencies. The two leakage IFCP method is achieved by subtracting their respective I_{cp}'s at two successive frequencies

2.4 Model Description and Derivation

2.4.1 Essential Physics of Channel Backscattering

Fig. 2.9 is the schematic diagram of channel backscattering theory in saturation region. Carriers are injected from the thermal source side, across the potential barrier whose height is modulate by the gate voltage and the drain voltage called K_bT-layer, into the channel which is populated by carriers injection from thermal equilibrium source. Because of the high electrical field and velocity overshoot near the drain side, carriers transport rapidly through the channel into the drain.

Therefore the device current is controlled by the low field region near the beginning of the channel instead of the drain side. Where l_0 is the length of potential barrier. According to [elementary scattering theory of Si MOSFET], real device operate below ballistic limit because of carrier back-scattering, which leads to:

$$I_{D,sat} = W \bullet V_{inj} \bullet C_{eff} \bullet B_{sat} \bullet (V_G - V_{T,sat}) \quad \text{Where} \quad B_{sat} = \frac{1-r_c}{1+r_c}$$

Fig 2.10 shows the experimental flow chart of this thesis. All of these symbols have their physical meanings: V_{inj} is the thermal velocity from the source side, r_c is the backscattering coefficient and B_{sat} is the ballistic efficiency. The symbol $C_{eff} \bullet (Vg - V_{T,sat})$ equals to the inversion charge density which is usually assumed to be proportional to the amount of the gate voltage overdrive between the gate voltage and threshold voltage. In state-of-the-art manufacturing process, the length of potential barrier is comparable to one mean-free-path, which means the transport across this layer is

quasi-ballistic. Note that the above deviations ignore some effect such as quantum confinement and carrier degeneracy.

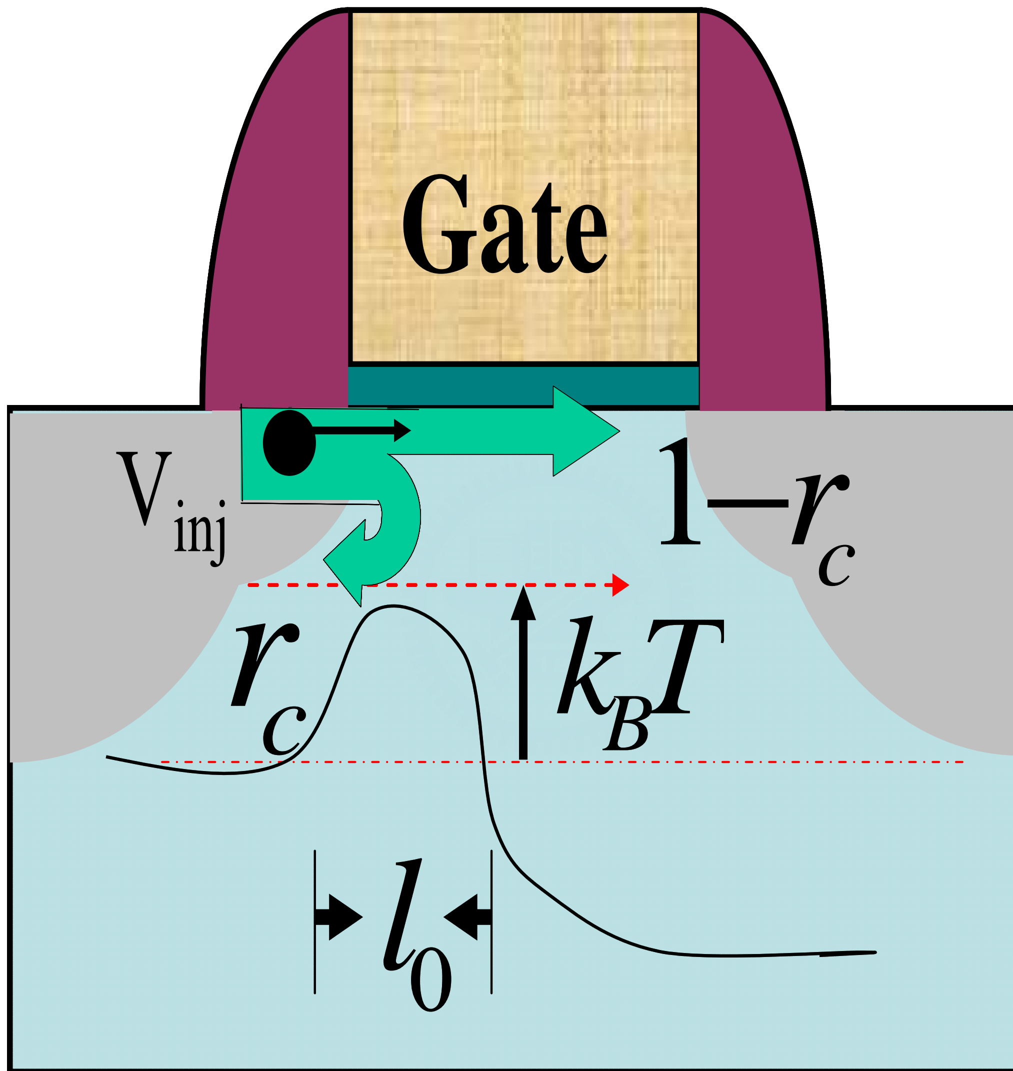


Fig. 2.9 The schematic diagram of channel backscattering in the saturation region of a device.

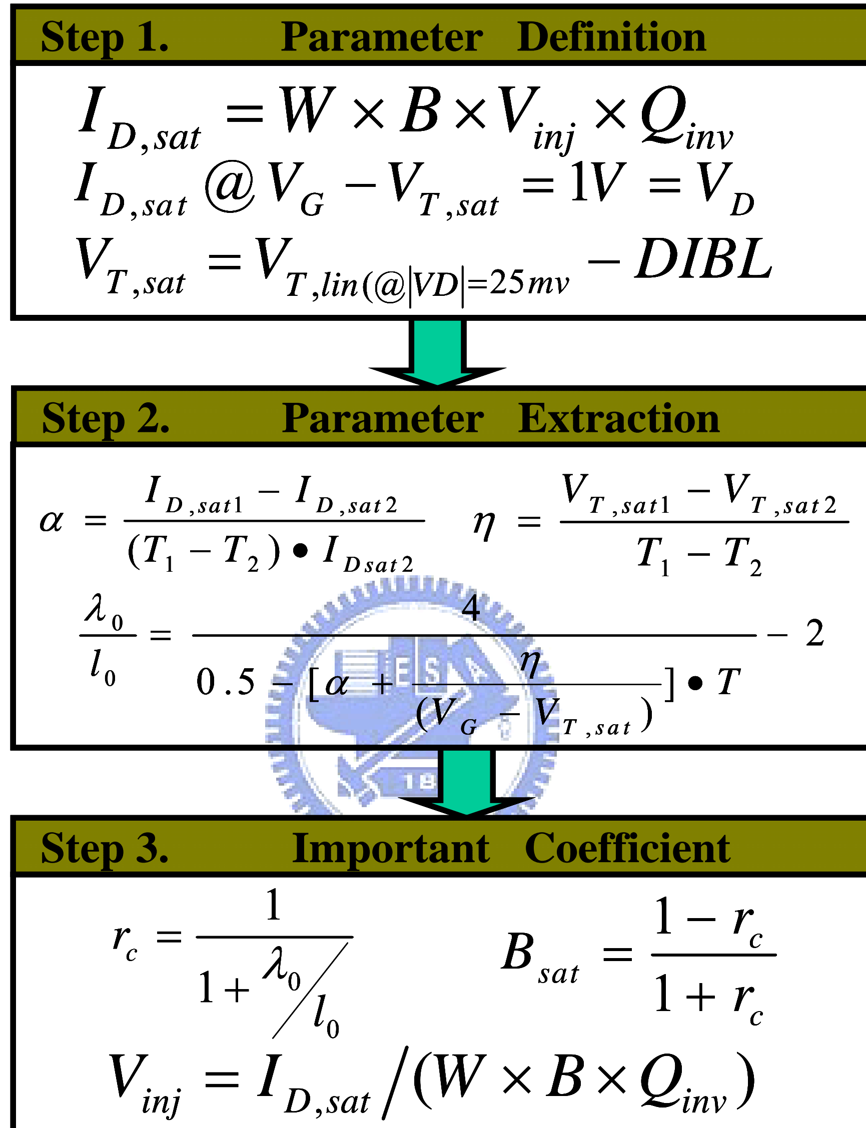


Fig. 2.10 The experimental flow chart of this thesis.

2.4.2 Principle of the Measurement

First of all, as shown in Fig 2.6 we use temperature dependent method to achieve the experiment, which the temperature is ranged from $25^0 C$ to $75^0 C$. Determining the threshold in short channel is difficult because of potential uncertainties caused by short channel effect i.e., DIBL (Drain Induced Barrier Lowering). In order to minimize this effect, we need to diminish the extra threshold drop. Device operates at saturation region where the threshold voltage is not exactly defined by G_m method. It's only precisely when drain voltage is very small about 25mv. Thus threshold voltage at saturation region $V_{T,sat}$ equals the threshold voltage at linear region $V_{T,lin}$ minus the DIBL effect:

$V_{T,sat} = V_{T,lin(@|VD|=25mv} - DIBL$. Fig. 2.8 is the DIBL effect of the test device. We can see that at high drain voltage, threshold is easily attained [15].So it is necessary to consider. Because of drain voltage and threshold voltage is temperature dependent; there will be some deviation at different temperature. Then, a temperature-dependent analytic is employed to extract the λ_0 / ι_0 ration by using following analytic expression:

$$\frac{\partial I_{dsat}}{\partial T} = I_{dsat}[\frac{1}{V_{inj}}\frac{\partial V_{inj}}{\partial T} + \frac{1+r_c}{1-r_c}\frac{\partial}{\partial T}(\frac{1-r_c}{1+r_c}) + \frac{1}{V_g - V_{T,sat}}\frac{\partial(V_g - V_{T,sat})}{\partial T}$$

$$= I_{dsat}[\frac{1}{2T} - (\frac{1}{1-r_c} + \frac{1}{1+r_c})\frac{\partial r_c}{\partial T} - \frac{\eta}{V_g - V_{T,sat}}]$$

$$= I_{dsat} \bullet \alpha$$

Where $$\frac{\partial r_c}{\partial T} = [2r_c(1-r_c)]/T$$

So can be derived as follows: $\alpha = \frac{1}{T}[\frac{1}{2} - \frac{4}{2+\lambda_0/l_0}] - \frac{\eta}{V_g - V_{T,sat}}$

For $r_c = \frac{1}{1+(\lambda_0/l_0)}$ we need to extract λ_0/l_0 first. λ_0/l_0 equals $\frac{4}{0.5-[\alpha+\frac{\eta}{(V_G - V_{T,sat})}]\bullet T} - 2$,

α and η is the important parameter above this experimental. We can estimate that $\alpha = \frac{I_{D,sat1} - I_{D,sat2}}{(T_1 - T_2)\bullet I_{Dsat2}}$

and $\eta = \frac{V_{T,sat1} - V_{T,sat2}}{T_1 - T_2}$. α and η are extracted from the best-fitted slope of

ΔI_{dsat} and $\Delta V_{T,sat}$. Lastly, backscattering coefficient r_c, ballistic efficiency B_{sat} and injection velocity V_{inj} can be deduced. Notice that the capacitance we measured is long channel, big area device.

However the devices we tested are short channel devices, the inversion charge will be underestimated. So we need to correct this mismatch. In [16], we can use the difference of the threshold voltage of long and short channel devices to compensate the inversion charge. Thus the backscattering coefficient r_c is easily extracted by this temperature dependent method.

2.5 Summary

In this chapter, we present a simple theory of the MOSFET to explore the physics of the Nano-scaled devices. It emphasizes on the critical importance of the source to channel transition region in these small devices and the need to realize the efficient carrier injectors at the source. The experimental setup and analytical method are described simply. We will use these experimental techniques to discuss control Si and Strained-Si samples transport issues.

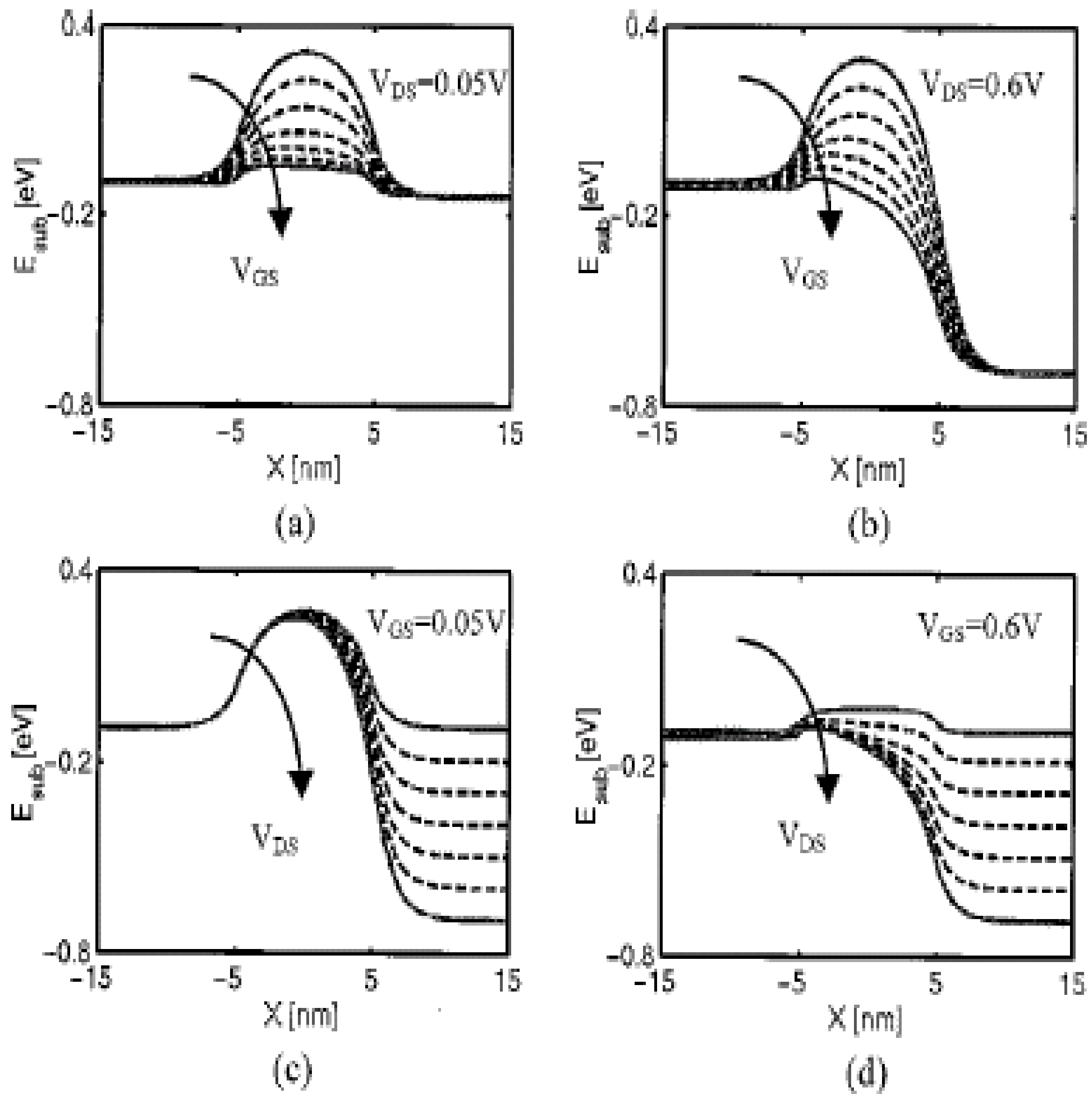
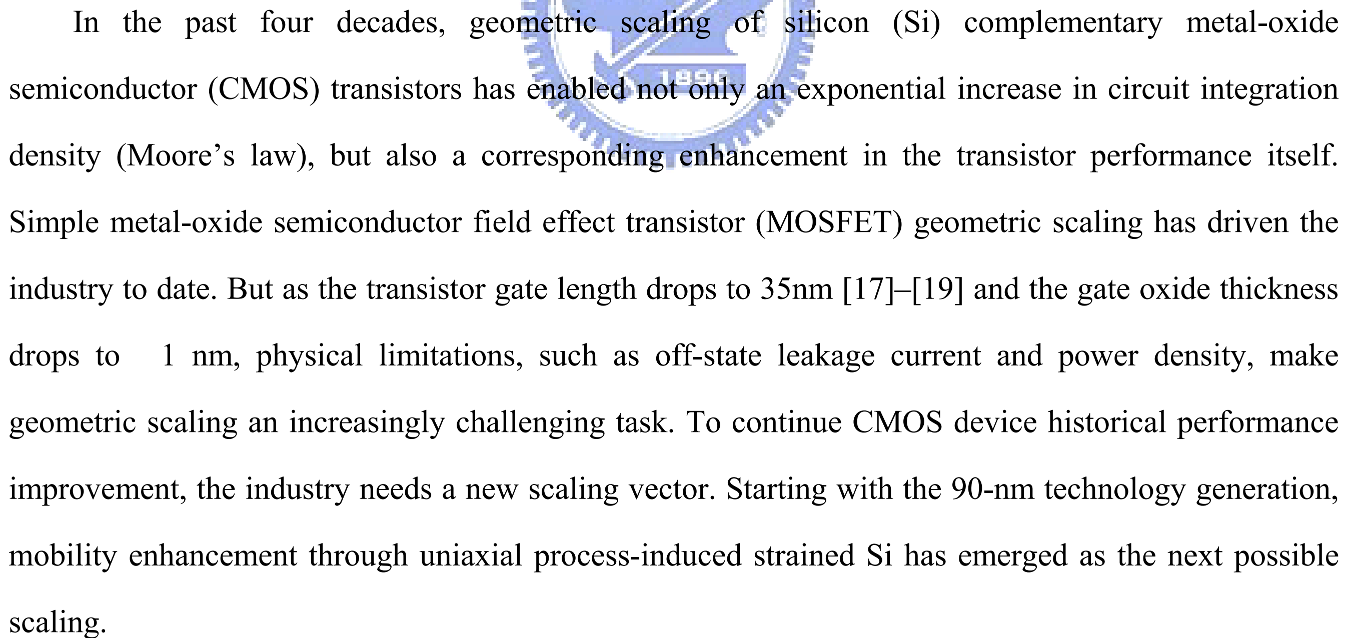


Fig. 2.11 The DIBL effect at different drain voltages. We can see that threshold voltage can be easily attained due to DIBL effect.

Chapter 3
Performance and Backscattering Transport of CMOS with Various Strain techniques

3.1 Introduction

With the scaling of the device size, performance improvement of CMOS devices faces a number of obstacles. Mobility enhancement technology is the way to offer dramatic advances of CMOS devices. In order to realize high-speed scaled CMOS devices, it is necessary to increase the carrier mobility for device gate length down to the sub-100-nm and beyond. Recently, a number of groups have shown that short channel nMOSFET devices incorporating thin strained-Si surface channels can achieve significant drive current enhancement.



In the past four decades, geometric scaling of silicon (Si) complementary metal-oxide semiconductor (CMOS) transistors has enabled not only an exponential increase in circuit integration density (Moore's law), but also a corresponding enhancement in the transistor performance itself. Simple metal-oxide semiconductor field effect transistor (MOSFET) geometric scaling has driven the industry to date. But as the transistor gate length drops to 35nm [17]–[19] and the gate oxide thickness drops to 1 nm, physical limitations, such as off-state leakage current and power density, make geometric scaling an increasingly challenging task. To continue CMOS device historical performance improvement, the industry needs a new scaling vector. Starting with the 90-nm technology generation, mobility enhancement through uniaxial process-induced strained Si has emerged as the next possible scaling.

Electron/hole mobility enhanced by uniaxial stress and biaxial stress in tensile/ compressive strain is efficiency. In nMOSFET uniaxial strain, we can use SiN (Thermal CVD) as a contact etch stop

layer (CESL) to tensile the channel. For biaxial strain in nMOSFET, Si on relaxed SiGe virtual substrate is the popular technique. On the other hand, there are two approaches to achieve uniaxial strain in pMOSFET, one is to deposit SiN (PE CVD) on the gate, and the other way is to refill S/D with SiGe, which will cause compressive strain to the channel. The biaxial compressive strain utilizes SiGe on Si substrate. In this chapter, the devices performance and backscattering characteristic of strained-Si MOSFET will be demonstrated.

3.2 The Backscattering Characteristics of Uniaxial and Biaxial Strained-nMOSFET

3.2.1 Device Performance of Uniaxial nMOSFET

Fig. 3.1 shows the I_{on}/I_{off} characteristic of uniaxial strain nMOSFET, which is enhanced about 34% than control sample. Piezoresistance coefficients can be as a guide as to which strain maximizes the mobility enhancement in uniaxial stress. Since uniaxial process-induced strain is generally parallel (longitudinal) or perpendicular to the direction of the MOSFET current flow. The effect of mechanical stress on the mobility can then be expressed as follows: $\frac{\Delta\mu}{\mu} \approx \left|\pi_{||}\sigma_{||} + \pi_{\perp}\sigma_{\perp}\right|$ where $_{||}$ and $_{\perp}$ refers to the directions parallel and traverse to the current flow in the plane of the MOSFET, $\frac{\Delta\mu}{\mu}$ is the fraction change in mobility. $\sigma_{||}$ and $\sigma_{\perp}$ are the longitudinal and transverse stresses, and $\pi_{||}$ and $\pi_{\perp}$ are the piezoresisitance coefficient express in Pa^{-1}. The longitudinal and transverse piezoresisitance coefficients for the standard layouts are given in Table 3.1. From the table that nMOSFET uniaxial strain on <100> channel direction is efficiency for it has higher $\pi_{||}$ [20], which results on the high strain reduced to high performance.

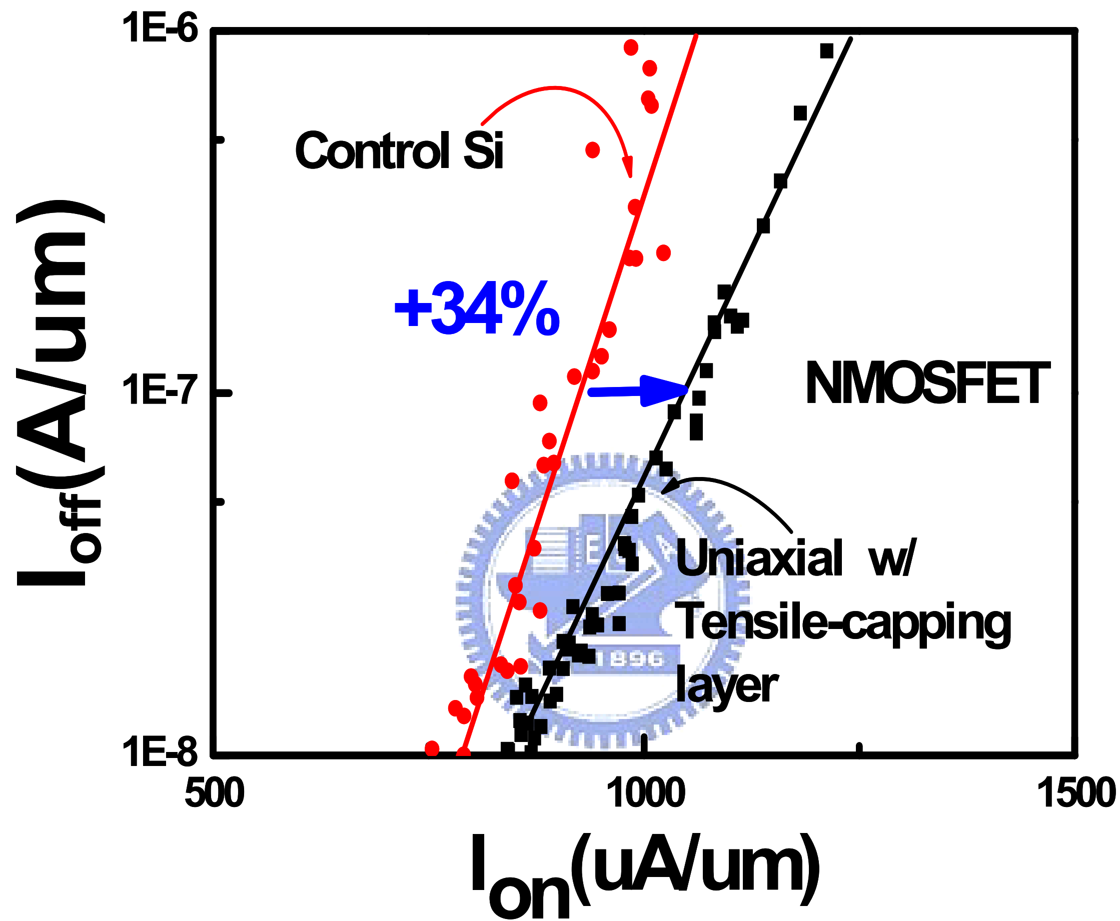


Fig. 3.1 The I_{on}/I_{off} characteristic of uniaxial strain nMOSFET, enhanced about 34% than the control sample.

	<100>		<110>	
polarity	$\pi_{\parallel}$	$\pi_{\parallel}$	$\pi_{\perp}$	$\pi_{\parallel}$
N or P	π_{12}	$\pi_{\perp}$	$(\pi_{11}+\pi_{12}+\pi_{44})/2$	$(\pi_{11}+\pi_{12}+\pi_{44})/2$
N-type	-102	53.4	-31.6	-17.6
P-type	6.6	-1.1	71.8	-66.3

Tab. 3.1 The longitudinal and transverse piezoresistance coefficient evaluated for standard layout and wafer orientation

3.2.2 Backscattering Characteristic of Uniaxial nMOSFET

Fig. 3.2 shows the λ_o / l_o versus channel lengths, which was extracted form the measured temperature dependent parameters. Fig. 3.3 shows the r_c versus channel lengths, is calculated from the α, η, and V_T as defined in fig. 2.6. Based on extracted $\frac{\lambda_o}{l_o}$ ratio, ballistic efficiency B_{sat} under saturation operation are calculated and plotted in Fig. 3.4.

As gate length shrinks, the departure of r_c between control and uniaxial strained-MOSFET becomes more evident. Uniaxial strained-nMOSFET exhibits a smaller r_c while control sample exhibits a larger r_c. This observation indicates that carriers are injected from source into the channel, the injected electrons suffered less backscattering under uniaxial tensile strain. After extracting the backscattering coefficient, the other parameter: injection velocity also needs to be extracted. In Fig. 3.5 shows the V_{inj} versus channel lengths: Uniaxial strained sample has higher velocity about 2 times than control sample. From the above results, uniaxial strained nMOSFET has higher transport mechanism than control sample.

3.2.3 Device Performance of Biaxial Strained-nMOSFET

Fig.3.6 shows the I_{on}/I_{off} characteristic of biaxial strained-nMOSFET, which is enhanced about 30% than control sample. Fig. 3.7 is the current enhancement scheme and its cross-section view of the strain structure. It was found that silicon under biaxial tensile strain features splits the six-fold degenerate conduction band minimum into a two-fold (△2) and a four-fold (△4) degenerate band. Since electrons preferentially popular the △2 band, which is lower in energy, the increasing in energy splitting reflects the reduction in the inter-valley phonon scattering and lower in-plane electron

effective mass [21] .That the reason why under biaxial strain will cause performance enhancement about 30% than control sample.

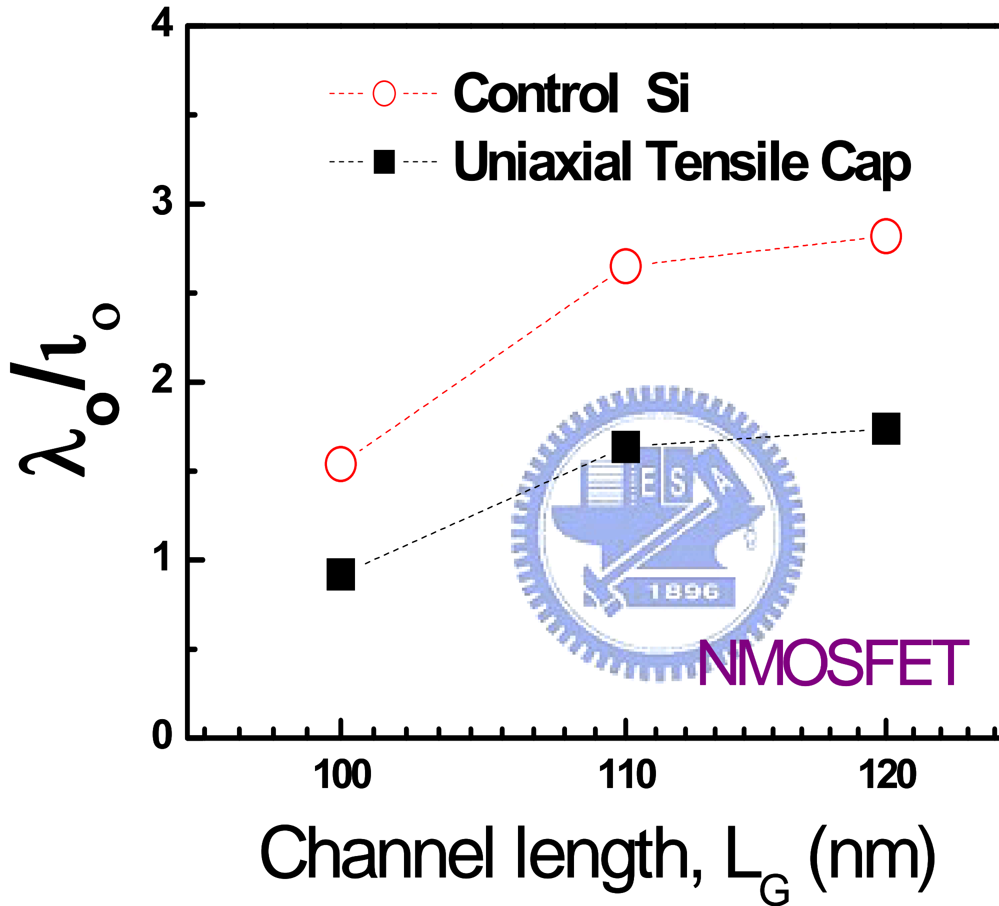


Fig. 3.2 The measured λ_o / l_o characteristics of uniaxial strained-nMOSFET.

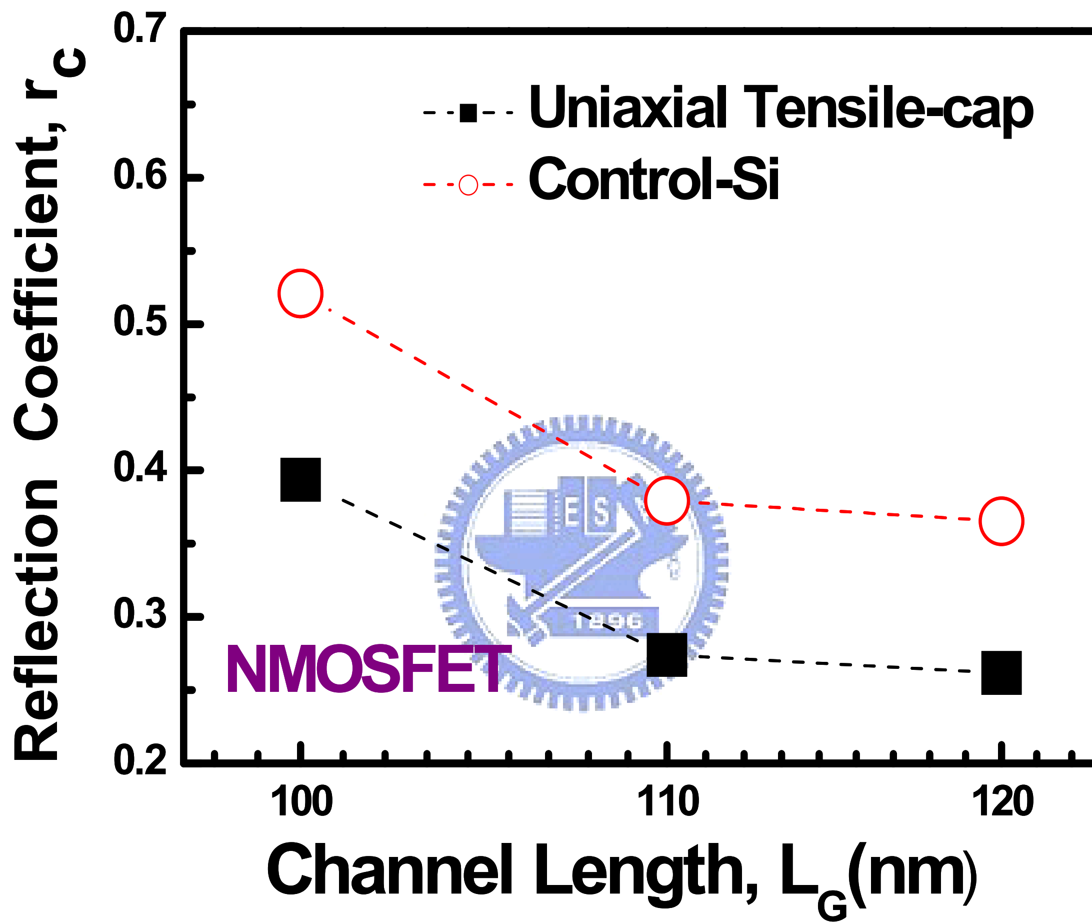


Fig 3.3 The calculated r_c, which was plotted as a function of channel lengths from the V_T defined in Fig. 2.10.

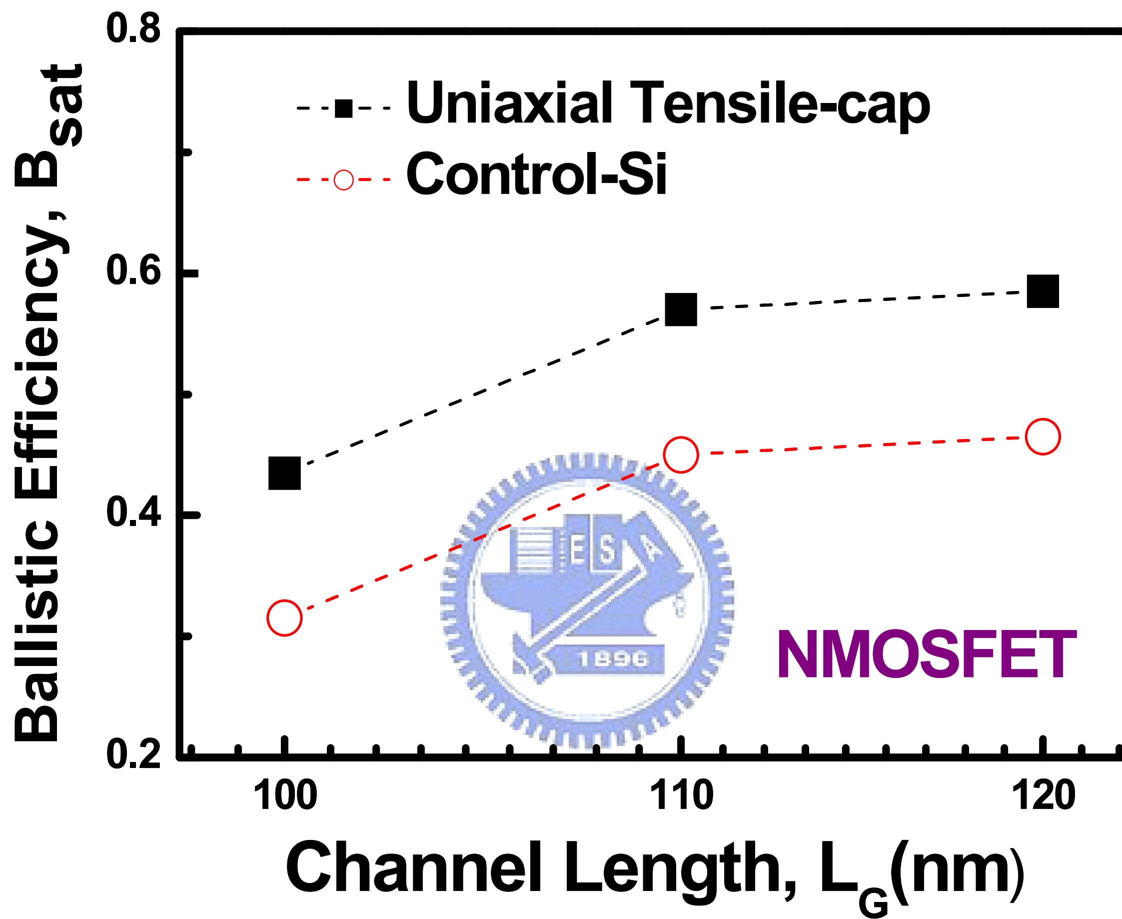


Fig. 3.4 The ballistic efficiency B_{sat} under saturation operation of uniaxial strained-nMOSFET.

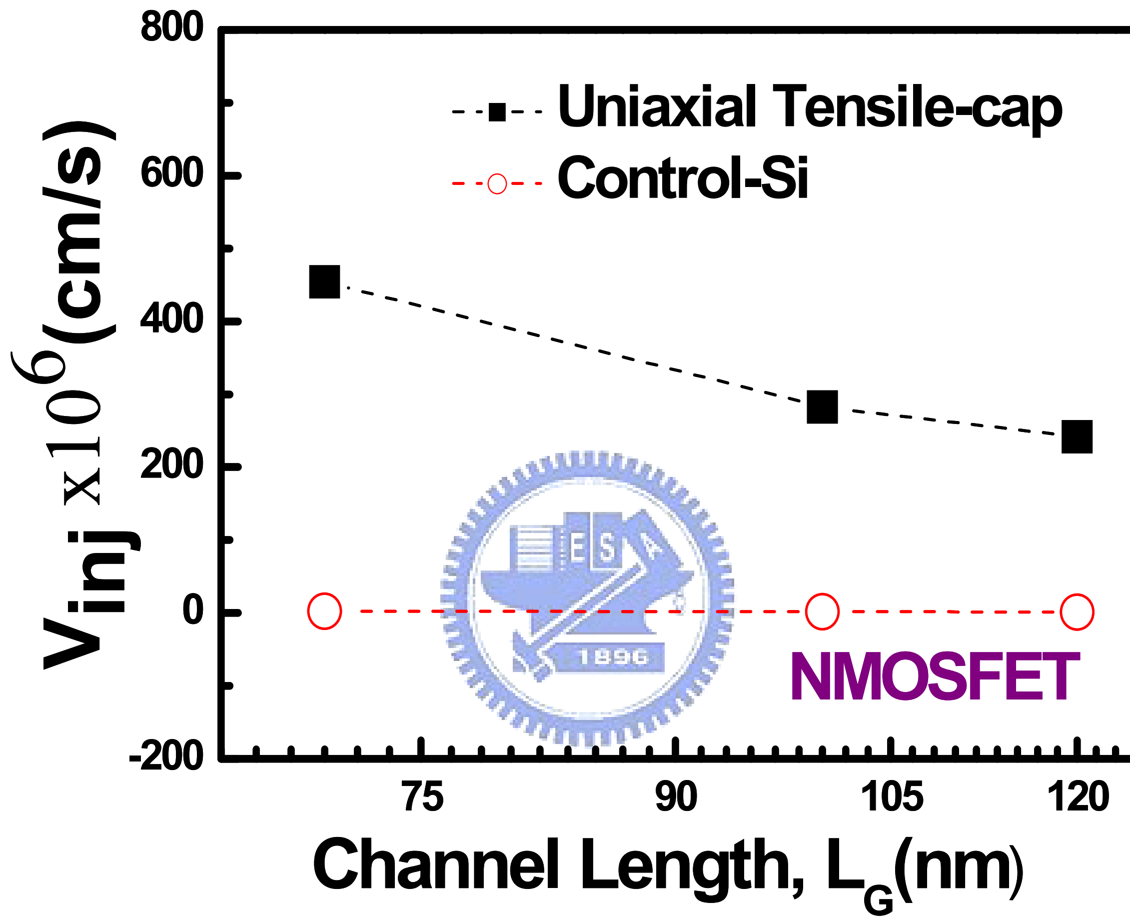


Fig. 3.5 The calculated V_{inj} versus channel lengths. The uniaxial strained sample has higher velocity with about 2 times more than the control sample.

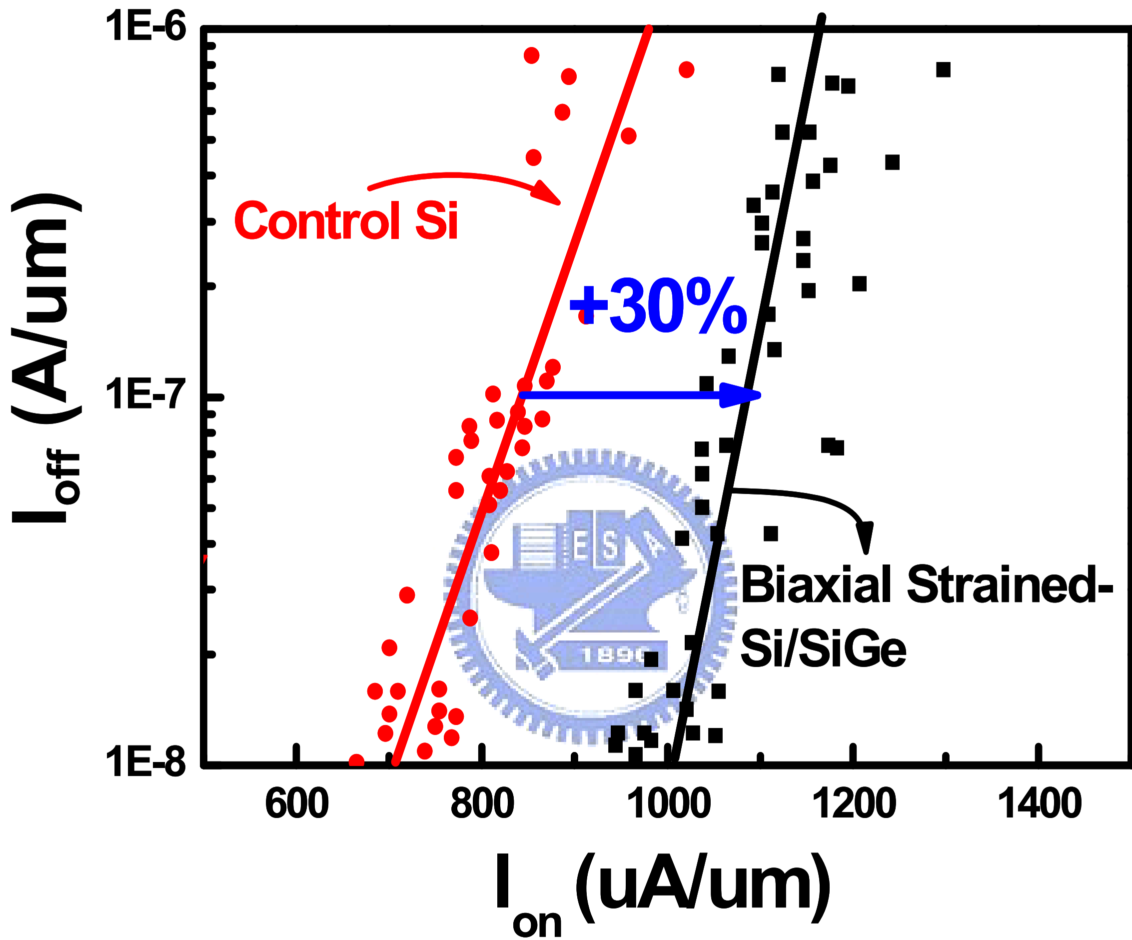


Fig. 3.6 The I_{on}/I_{off} characteristic of biaxial strained-nMOSFET, which is enhanced about 30% than the control sample.

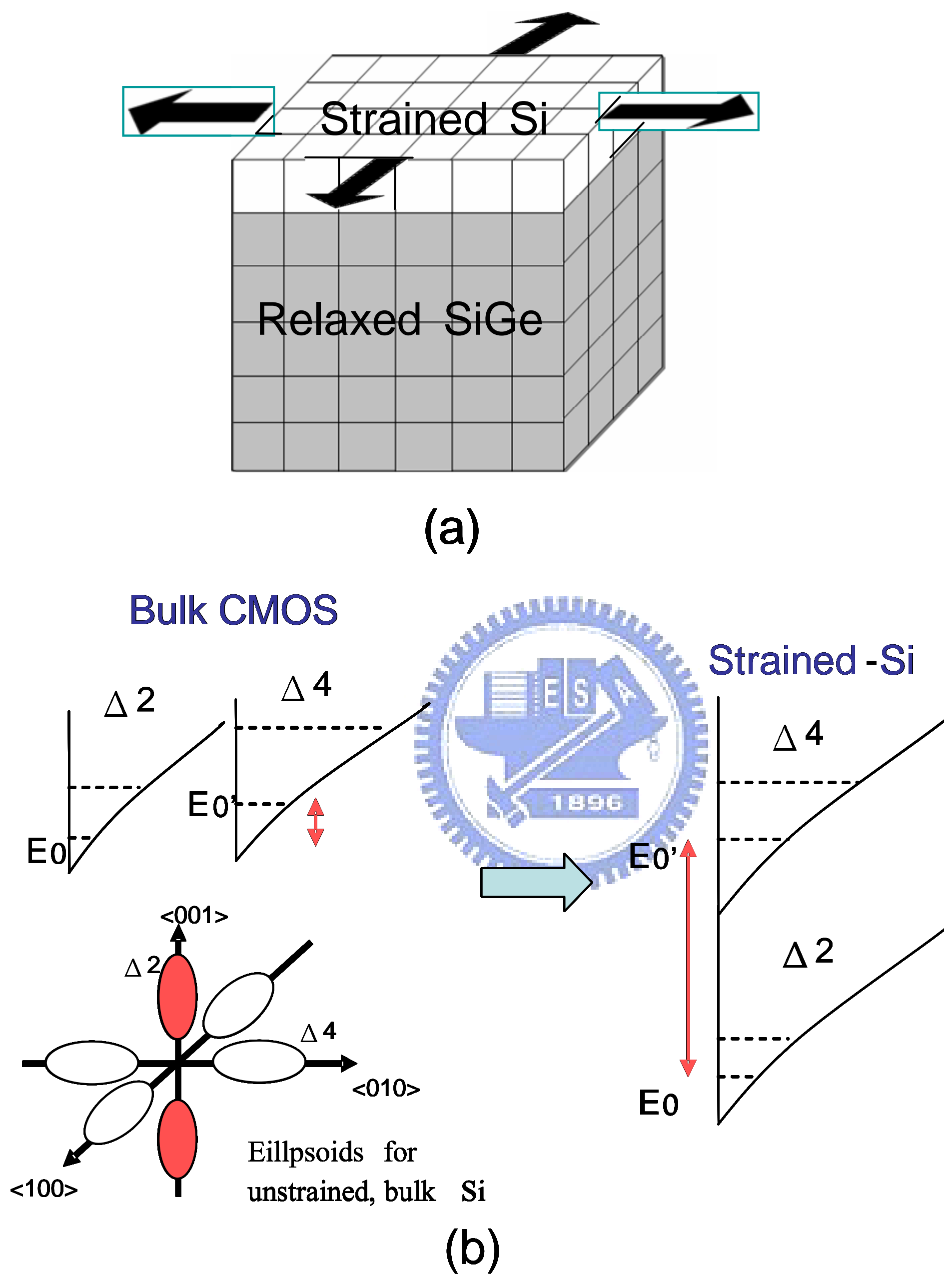
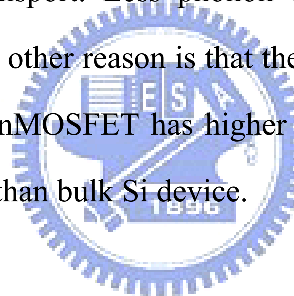


Fig. 3.7 (a) Pseudomorphic, strained-Si on relaxed SiGe (b) Energy splitting between theΔ_2 (2-fold degenerate) and Δ_4 (4-fold degenerate) conduction bands for strained-Si device and bulk device.

3.2.4 Backscattering Characteristic of Biaxial Strained-nMOSFET

Fig. 3.8 shows the λ_o / l_o versus channel lengths, which was extracted form the measured temperature dependent parameters In Fig. 3.9 is the backscattering coefficient r_c , Fig. 3.10 is the ballistic efficiency B_{sat}. And in Fig 3.11 is the injection velocity (V_{inj}) as a function of channel lengths. As the channel length reduced, the B_{sat} si increased. For injection velocity is higher than control and reached about $1*10^7$ value, which is little lower than velocity overshoot ($2*10^7$).

From the result above, strained sample also has better transport behavior than control sample. First reason may due to the mismatch of the Si/SiGe lattice tensile strain on the channel which will reduce the carriers scattering during the transport. Less phonon collision with carriers will enhance the velocity of carriers in the channel. The other reason is that the biaxial strain changes the effective mass of carriers. Thus, the biaxial strained-nMOSFET has higher injection velocity which is proportion to the inverse of "effective mass" square than bulk Si device.



3.3 The Backscattering Characteristic of Strained-pMOSFET

3.3.1 Device Performance of Strained-pMOSFET

The promising (110) SiGe channel technique as next generation high performance pMOSFET is used in this thesis. Fig. 3.12 shows the pMOSFET I_{on}/I_{off} characteristic of (110) SiGe channel and (110) Si channel devices. A high current gain of 48% is achieved for (110) SiGe channel pMOSFET. Extreme I_{dsat} enhancement of 81% can be realized by applying additional compressive capping layers on (110) SiGe channel pMOSFET. The (110) SiGe channel devices with compressive capping layer exhibit a remarkably high I_{dsat} of 850 uA/um at I_{off} =100nA.

The longitudinal piezoresistance coefficient $\pi_{\perp}$ of SiGe is 32% larger than Si. Therefore by applying the same longitudinal compressive stress, the current enhancements in SiGe channel pMOSFET should be larger compared to Si channel pMOSFET. Here shows the superposition effect in the strain enhance device performance.

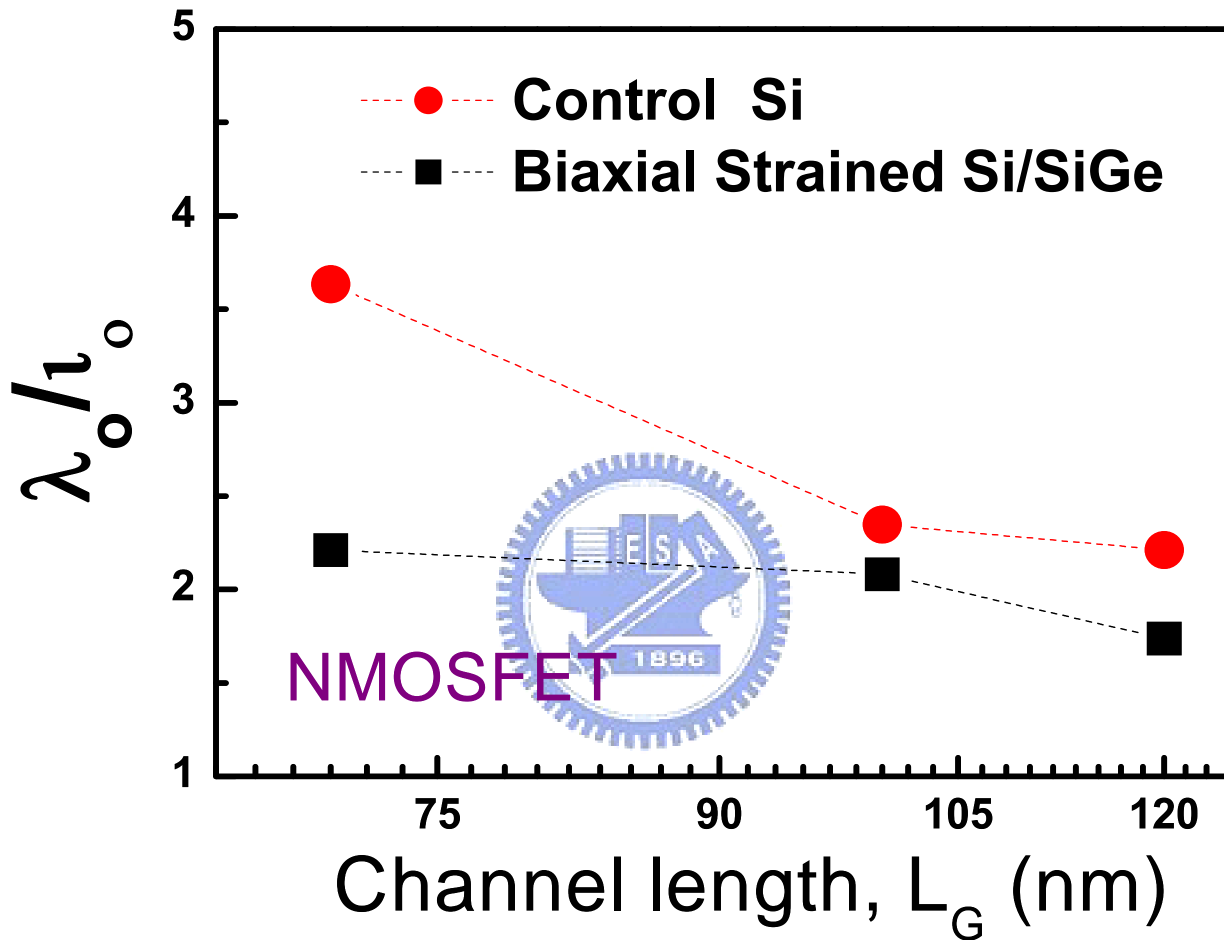


Fig 3.8 The measured λ_o / l_o characteristics of biaxial strained-nMOSFET.

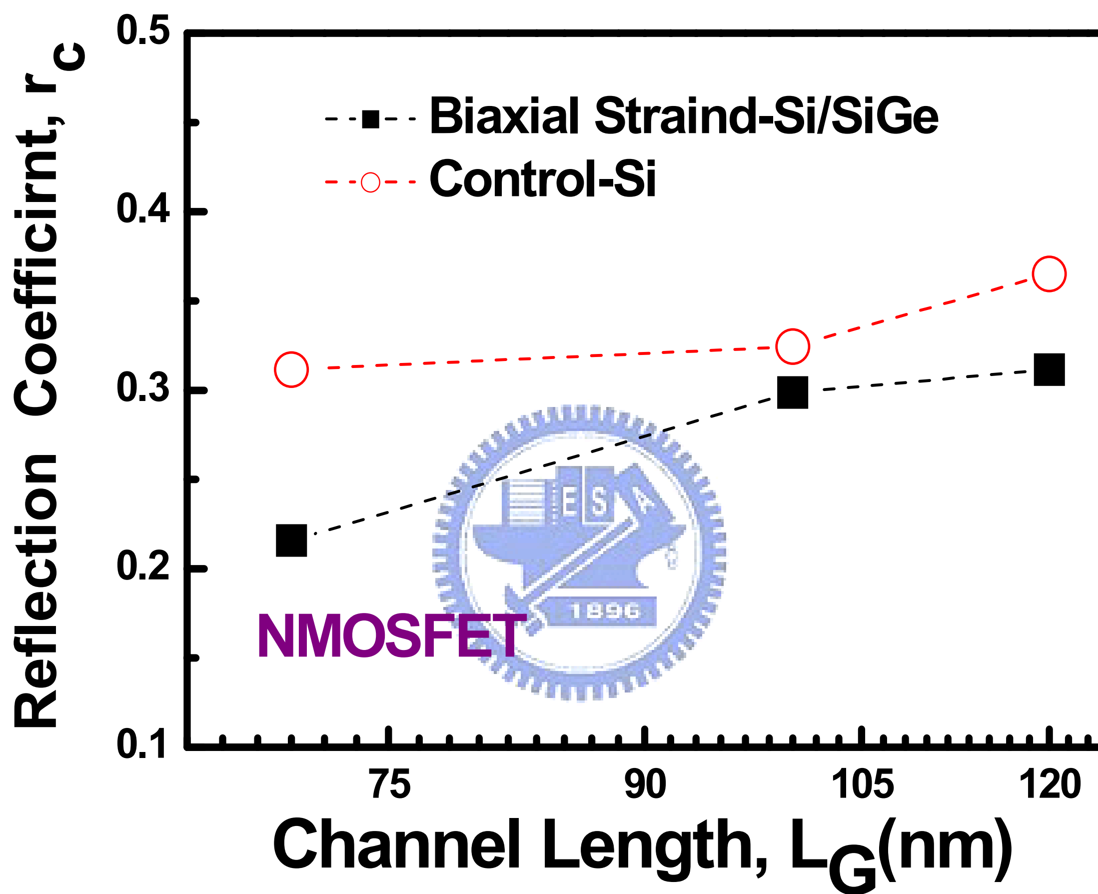


Fig. 3.9 The values of r_c versus channel lengths for biaxial strained-nMOSFET

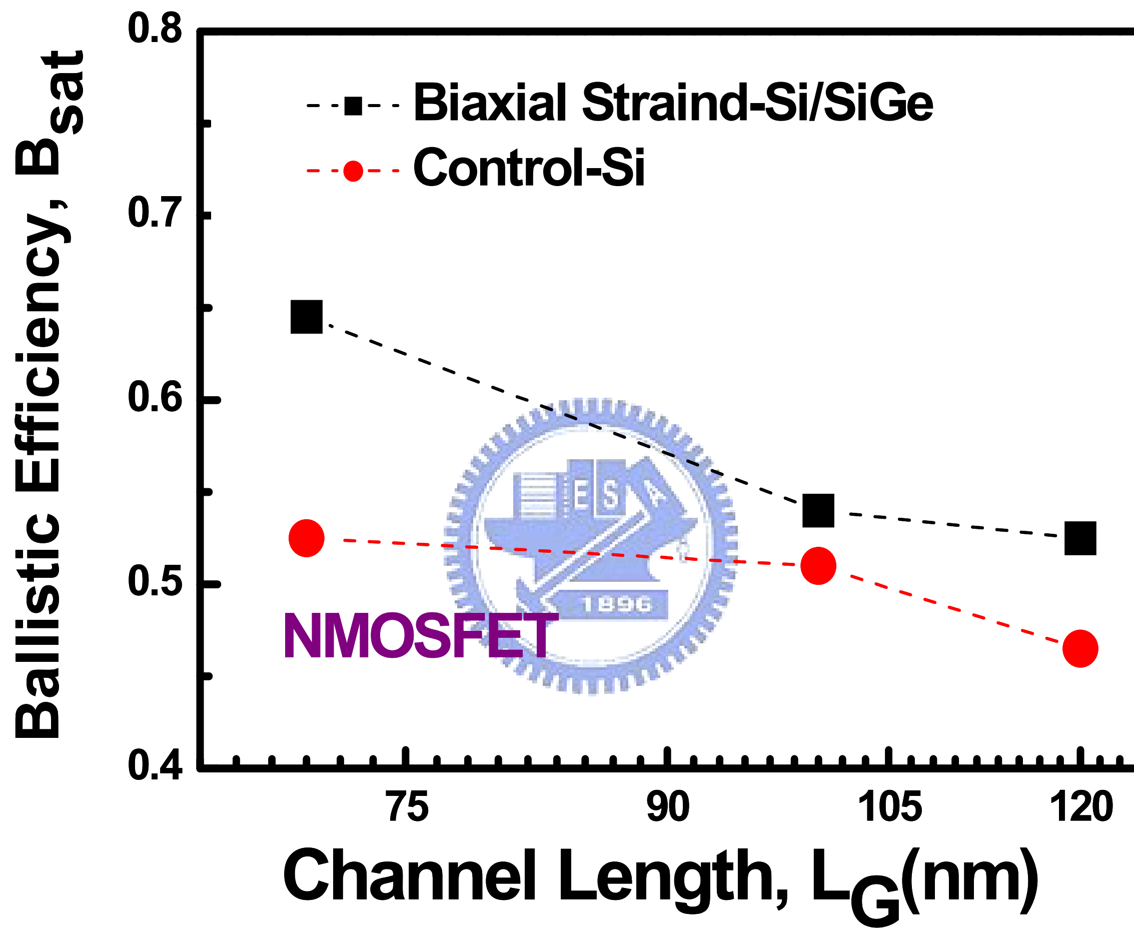


Fig. 3.10 The ballistic efficiency B_{sat} under saturation operation of biaxial strained-nMOSFET, biaxial strain has larger value than the control ones.

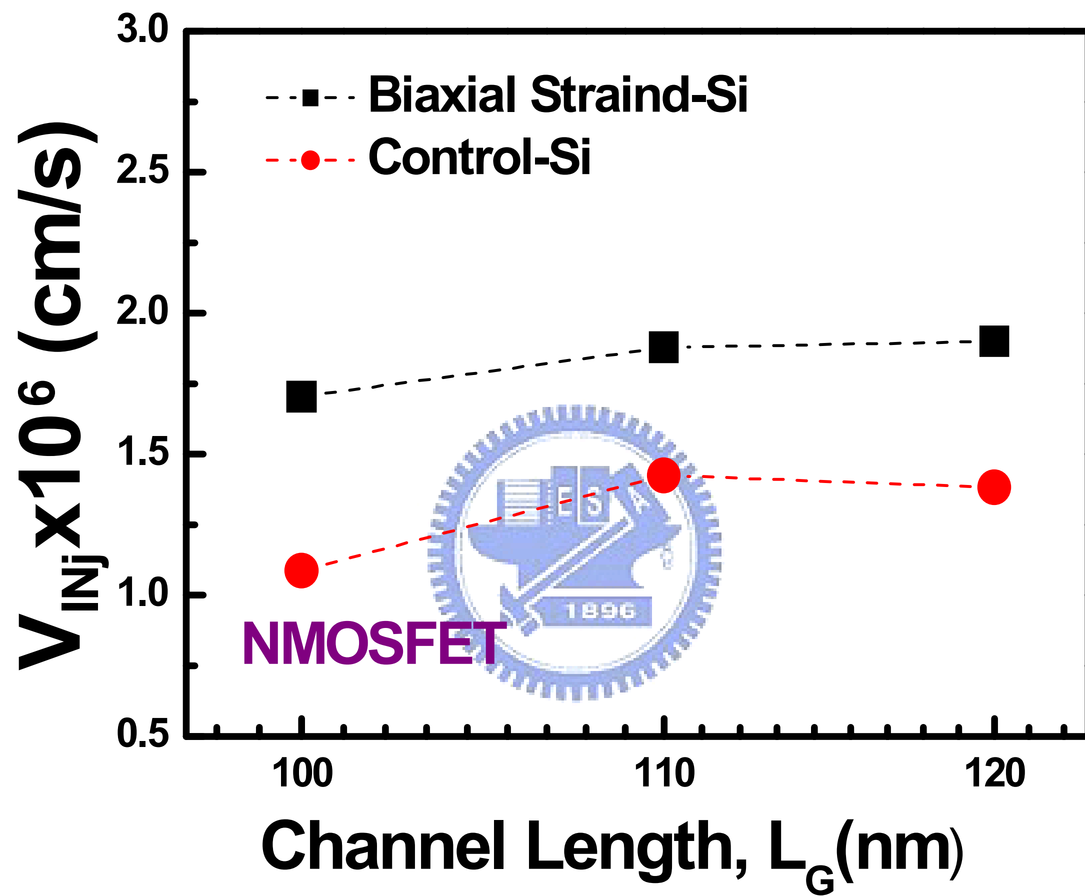


Fig. 3.11 The injection velocity (V_{inj}) as a function of channel lengths. Biaxial strained device exhibits larger value than the control ones.

3.3.3 Backscattering Characteristics of Strained-pMOSFET

Fig. 3.13 shows the λ_o / l_o versus channel lengths, which was extracted form the measured temperature dependent parameters Fig. 3.14 shows the r_c versus channel length, four samples are discussed here: control sample, SiGe channel , SiGe at source drain region ,and SiGe channel with compressive capping layer. And in the Fig. 3.15 is the B_{sat} as a function of channel lengths. From the figure we can see that SiGe channel device has highest B_{sat} while SiGe at S/D is lowest. But with compressive capping layer was deposited onto the SiGe channel, the r_c is increased. In [22] referring to that, compressive strained-pMOSFET will degrade the transport behavior. As the lattice constant is decreased by compressive strain, the phonon distribution is affected, which may account for more phonon scattering and therefore higher channel backscattering is obtained. So, when uniaxial strain plus biaxial strain, there should be has the superposition effect in transport behavior. Biaxial strain will enhance transport behavior, while uniaxial strain degrades it in pMOSFET. So we can see that in fig. 3.12 SiGe channel device has highest B_{sat} than the others, and SiGe + CESL is the second rank amount the three devices.

In Fig. 3.16 shows the injection of the pMOSFET, SiGe + CESL is the highest velocity at about $5.5*10^6$, then is the SiGe at S/D region , and then is the SiGe channel and lowest value is the control sample. As noticed that at shorter length the injection velocity shows higher value in pMOSFET.

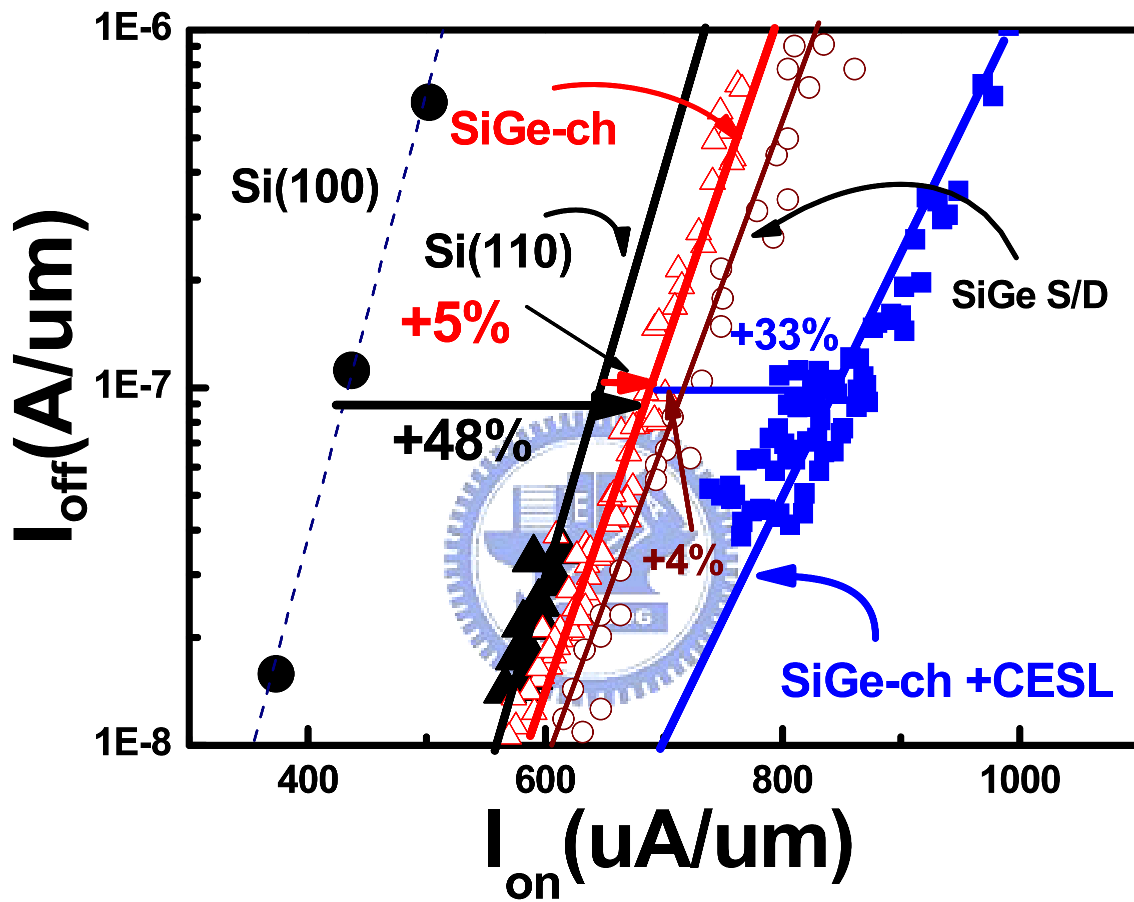


Fig. 3.12 The I_{on}/I_{off} characteristic of strained- pMOSFET devices, where SiGe+CESL has the largest current enhancement among the strained devices.

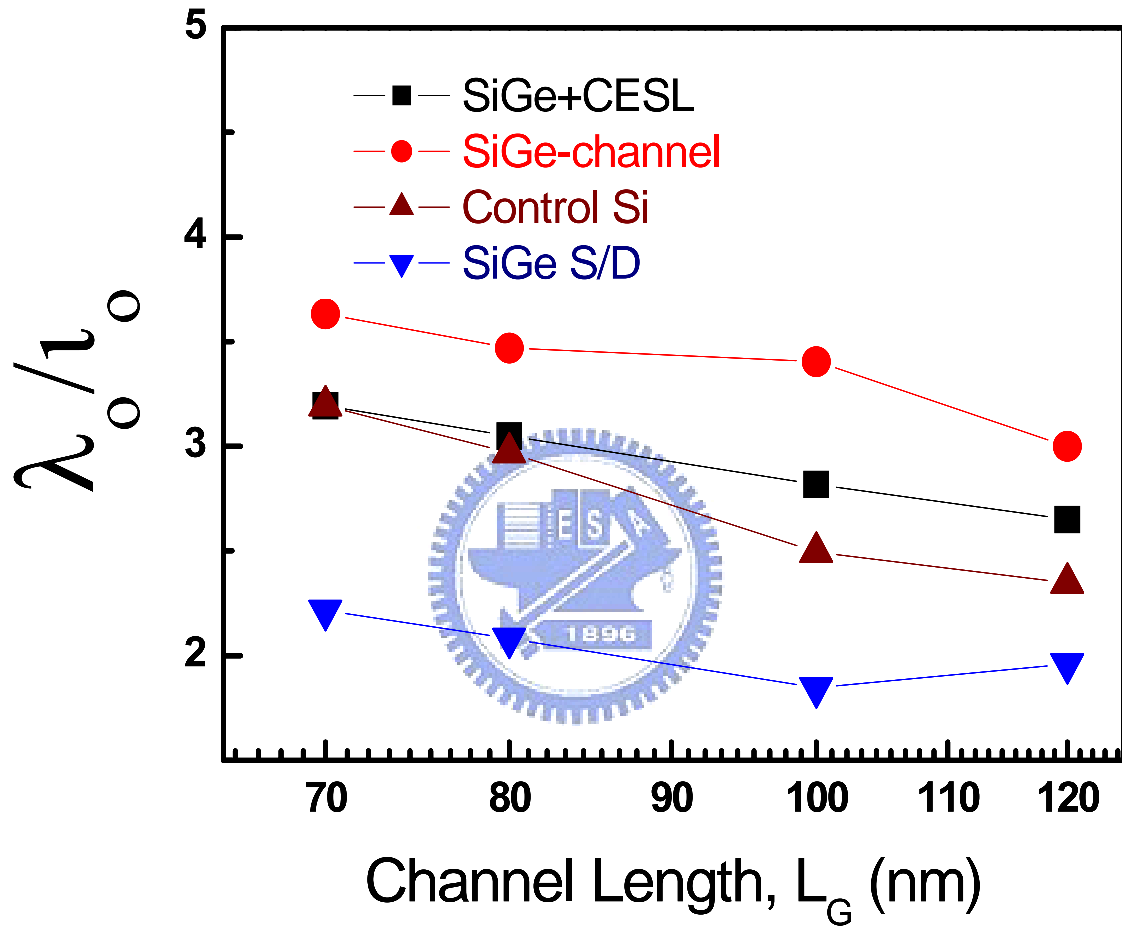


Fig .3.13 The measured λ_o / l_o characteristics of strained-pMOSFET devices.

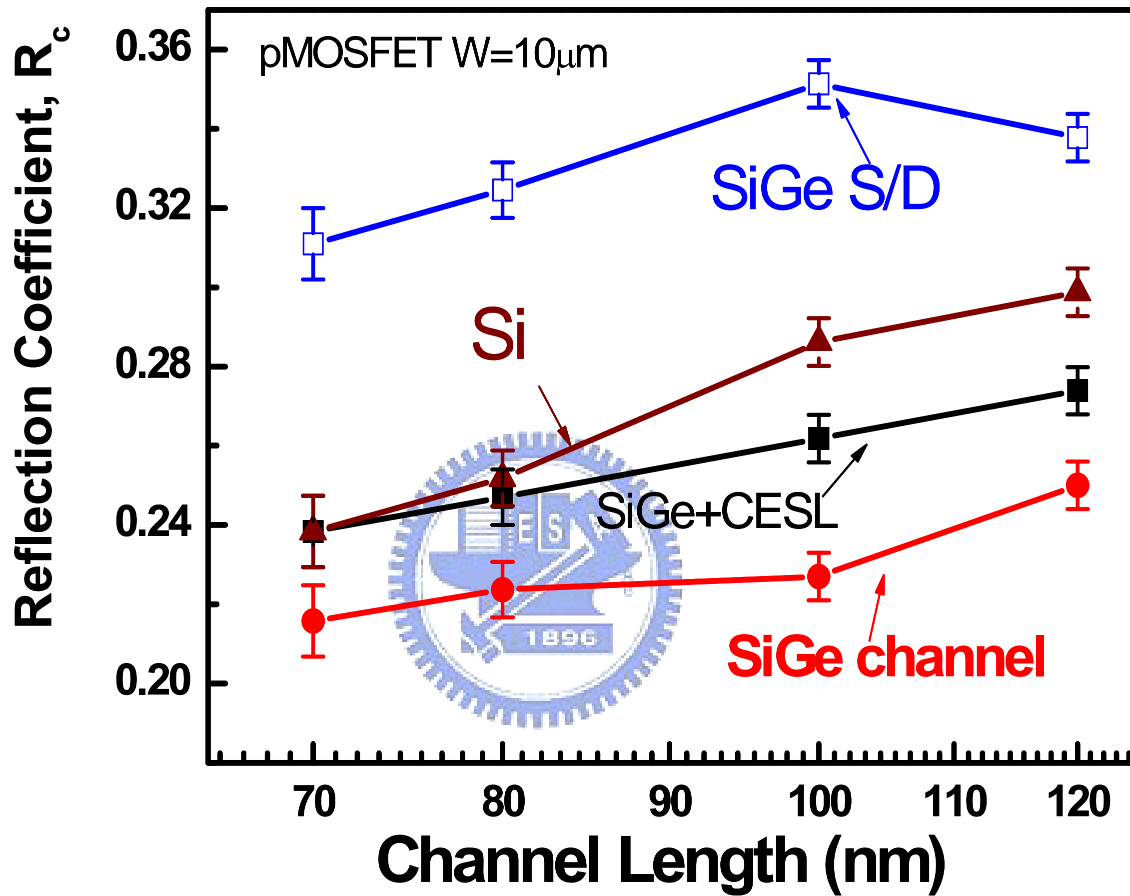


Fig. 3.14 The plotted r_c versus channel length of pMOSFET, where uniaxial strained device using SiGe S/D has the largest reflection than the others, and biaxial strained using SiGe channel has the lowest value.

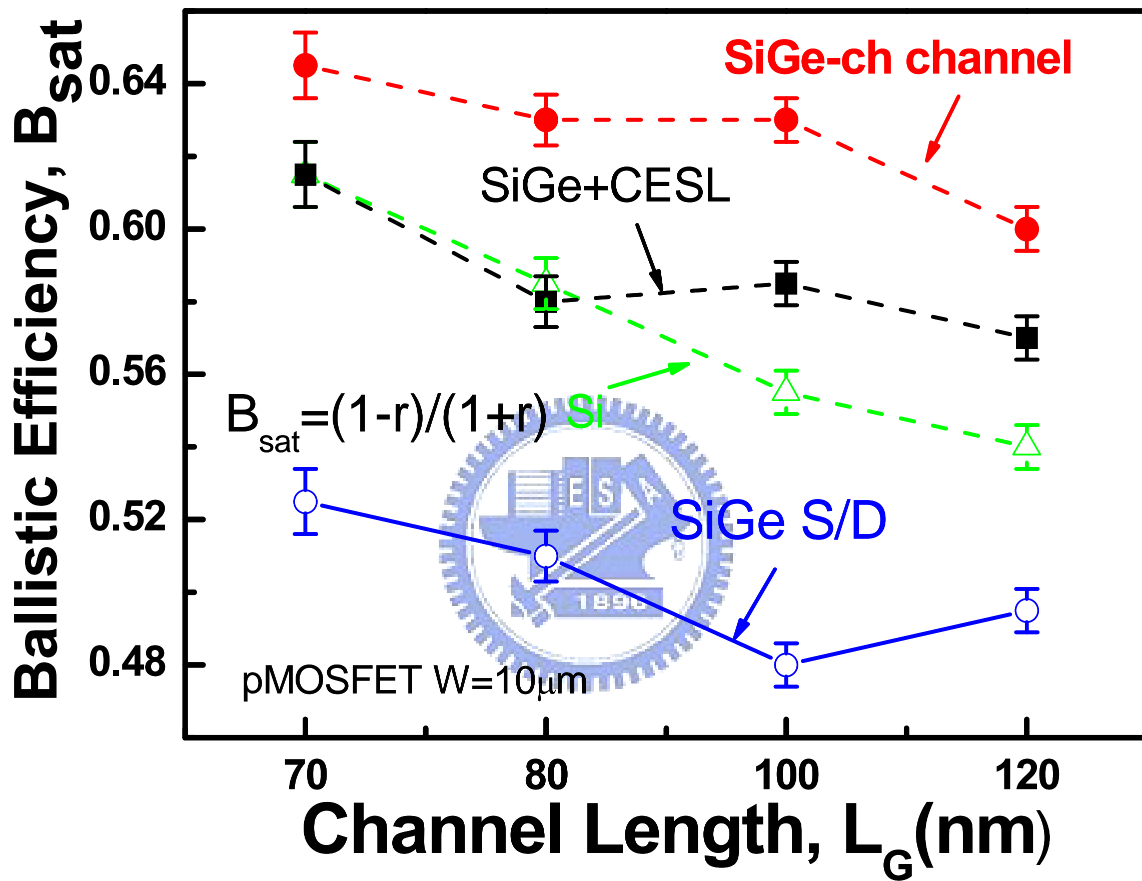


Fig. 3.15 The B_{sat} as a function of channel lengths. It was noted that SiGe channel device has highest B_{sat} while SiGe at S/D is lowest. But with compressive capping layer on the SiGe channel, r_c is increased.

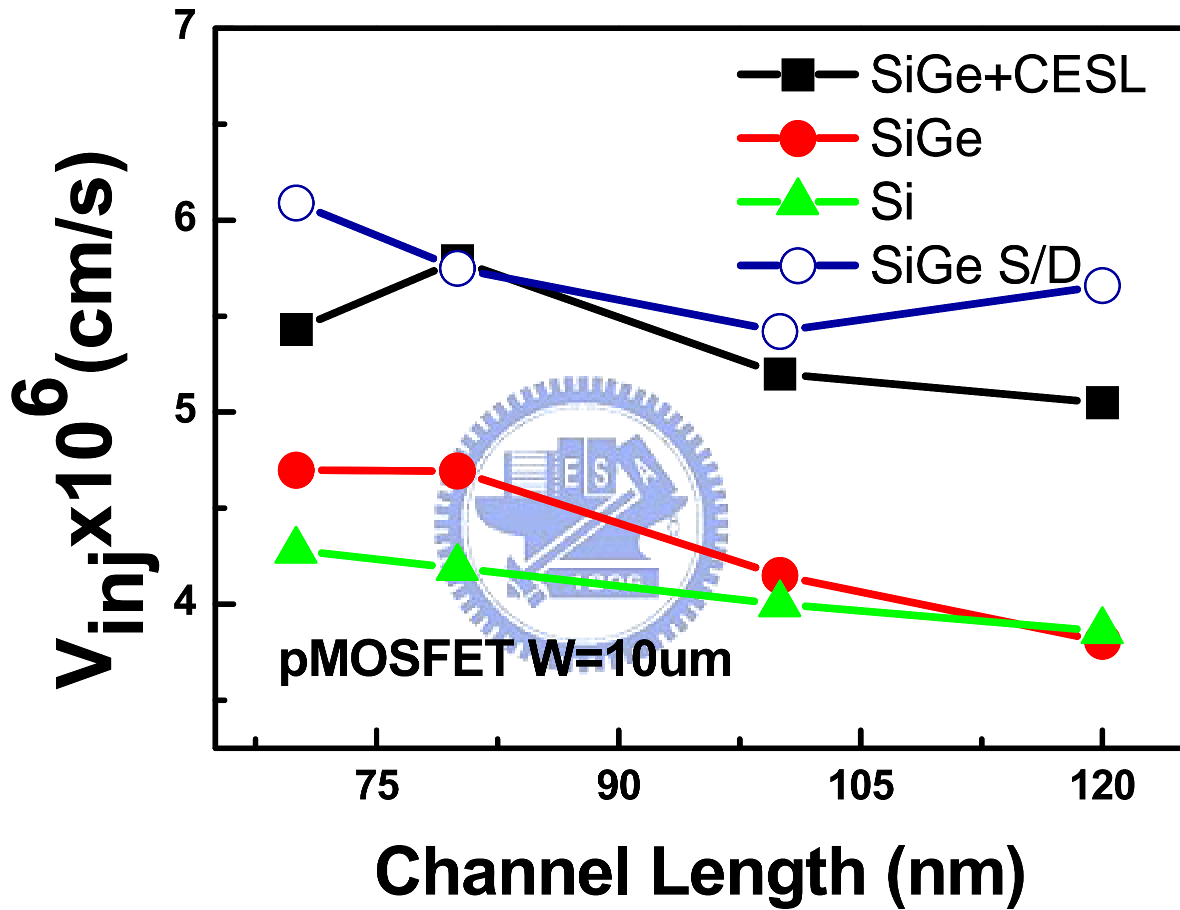
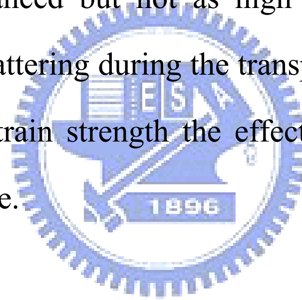


Fig. 3.16 The calculated V_{inj} of the pMOSFET, where SiGe+CESL is the highest velocity at about $5.5*10^6$, and lowest value is the control sample.

3.4 Summary

The impact of channel backscattering on strained-MOSFET in nanoscale device is demonstrated. Source-side injection velocity and backscattering ratio are both dominant factors in determining the drain current. The uniaxial and biaxial tensile strained-nMOSFET is enhanced in both B_{sat} and V_{inj}. Especially, in uniaxial strained SiGe S/D shows higher injection velocity than biaxial. However, biaxial strained device has higher ballistic efficiency than uniaxial strained ones.

For strained-pMOSFET, biaxial compressive strain shows the enhanced B_{sat} and V_{inj}. In SiGe+CESL device, B_{sat} is also enhanced but not as high as in biaxial strained device. Uniaxial compressive strain will cause much scattering during the transport due to the lattice constant decreases. Since both the uniaxial and biaxial strain strength the effects, the injection velocity, shows highest value in SiGe+CESL pMOSFET device.



In the next chapter, the relationships between enhancement of current and backscattering parameters will be demonstrated. From the reliability point of view, the bulk current will be a guide to present the impact ionization, which is the main current to reflect the hot carrier degradation.

Chapter 4
The Relationships Between Reliability and Current Enhancement

4.1 Introduction

Strained technique enhances device performance, by reducing scattering probability and increasing carrier population. And with the channel backscattering theory, there are two parameters to determine the drive current: V_{inj} and B_{sat}. We will show the current enhancement and its relationship with the two parameters. Which parameters of channel backscattering theory is the dominant factor to influence the device performance will also be demonstrated in this chapter.

Hot carrier degradation of MOSFET is an important reliability issue in deep-submicron technology [23]. Strained-Si device is a promising candidate for enhancement of CMOS performance. However, little research has been done on its reliability issues. To exploit the advantage or the shortcoming of the strained-Si device and investigate the reliability issue of the device, in later discussion, we use hot carrier measurement to study that. Bulk current is a good guide to detect after the impact ionization effect, how much carrier will be injected into the gate oxide to cause damage.

4.2 Current Enhancement Relates to Channel Backscattering Parameters

4.2.1 Enhancement Correlation in Tensile-Strained-nMOSFET

As shown in Fig. 4.1 is the current enhancement relates to channel backscattering parameters of uniaxial strained-nMOSFET. In the left scale is the enhancement of injection velocity (ΔV_{inj}), In the right is the ballistic efficiency enhancement (ΔB_{sat}) and X-axis is the current enhancement (ΔID). From the figure we can see that ΔV_{inj} enhances about 50% over in control sample while ΔB_{sat} enhances a little about less 20%. Fig. 4.2 is in biaxial strained-nMOSFET. Also ΔV_{inj} is enhanced larger than ΔB_{sat}, ΔV_{inj} enhances less than 60% while ΔB_{sat} enhances larger than 20%. Thus, in the tensile-stained-nMOSFET, both ΔV_{inj} and ΔB_{sat} is enhanced. Especially injection velocity is the dominant factor to promote the nMOSFET devices performance.

4.2.2 Enhancement Correlation in Compressive-Strained-pMOSFET

Fig. 4.3 shows the current enhancement relates to channel backscattering parameters of uniaxial strained-nMOSFET in SiGe S/D uniaxial compressive-pMOSFET. The ΔV_{inj} is enhanced about 20% but ΔB_{sat} is degraded among 14%. Fig 4.4 shows the enhancement correlation in SiGe pMOSFET. In which both ΔV_{inj} and ΔB_{sat} is enhanced. ΔV_{inj} is enhanced about 40% and ΔB_{sat} enhanced about 9.8% in average. Fig. 4.5 is shown the enhancement correlation in SiGe+CESL pMOSFET. In biaxial strain plus uniaxial strain, both ΔV_{inj} and ΔB_{sat} is enhanced. Enhancement of ΔV_{inj} is largest of the pMOSFET, but Enhancement of ΔB_{sat} is the second. There has the superposition effect of the result strain promote the injection velocity and biaxial increases the B_{sat}, while uniaxial strain lowers the B_{sat}.

4.3 The Reliability of Strained Device Relates to Channel Backscattering Parameters

In the following, we compared the substrate current after impact ionization effect of both devices. When carrier has great transverse electric field, it will be accelerated and possesses huge energy to collision the lattice to generate the electron-hole pairs. When gate is applied to positive voltage, the

electron will transport to the bulk for coulomb repulsion, and holes will be attracted to the gate oxide to hit the Si/SiO_2 interface. So we can measure bulk current to detect how sever the damage is.

Fig. 4.6 exhibits impact ionization current of the strained-Si device of nMOSFET which is operated at Vd= 2V and sweep Vg. It puts the four devices to compare the impact ionization current. In the figure we can see that biaxial strain has higher value than uniaxial strain. Hence, biaxial strained device is severed more degradation than using capping layer uniaxial strained device. In Fig. 4.7 (a) is measured charge pumping current of biaxial strained-nMOSFET, (b) is the measured charge pumping current of uniaxial strained-nMOSFET. In which we can see that strained device exhibits the larger value than control. This implies that strained devices of nMOSFET show larger interface traps. After hot carrier stress under Vg=Vd=2V, we extract the delta charge pumping current of the strained-nMOSFET is shown in the Fig 4.8

In Fig. 4.9 is the impact ionization current of the strained-Si device of pMOSFET which is operated at Vd= -2V and sweep Vg. As shown in the figure, SiGe + CESL has largest bulk current while control device shows the lowest. Then the second rank is the SiGe channel, third is SiGe S/D. In [23] exhibits that SiGe S/D uniaxial compressive strain has better reliability than SiGe channel biaxial compressive strain. So when consider the effect of the plus with uniaxial and biaxial strain, the result shows the worse reliability. The larger bulk current means that the gate is suffering serious damage. In Fig. 4.10 is measured charge pumping current of strained-pMOSFET, also the strained-devices show worse interface quality. Then the measured charge pumping current after the hot carrier stress to the pMOSFET is shown in the Fig. 4.11. Whatever for nMOSFET or pMOSFET, it shows the same result with the impact ionization rate, larger bulk current cause server interface traps.

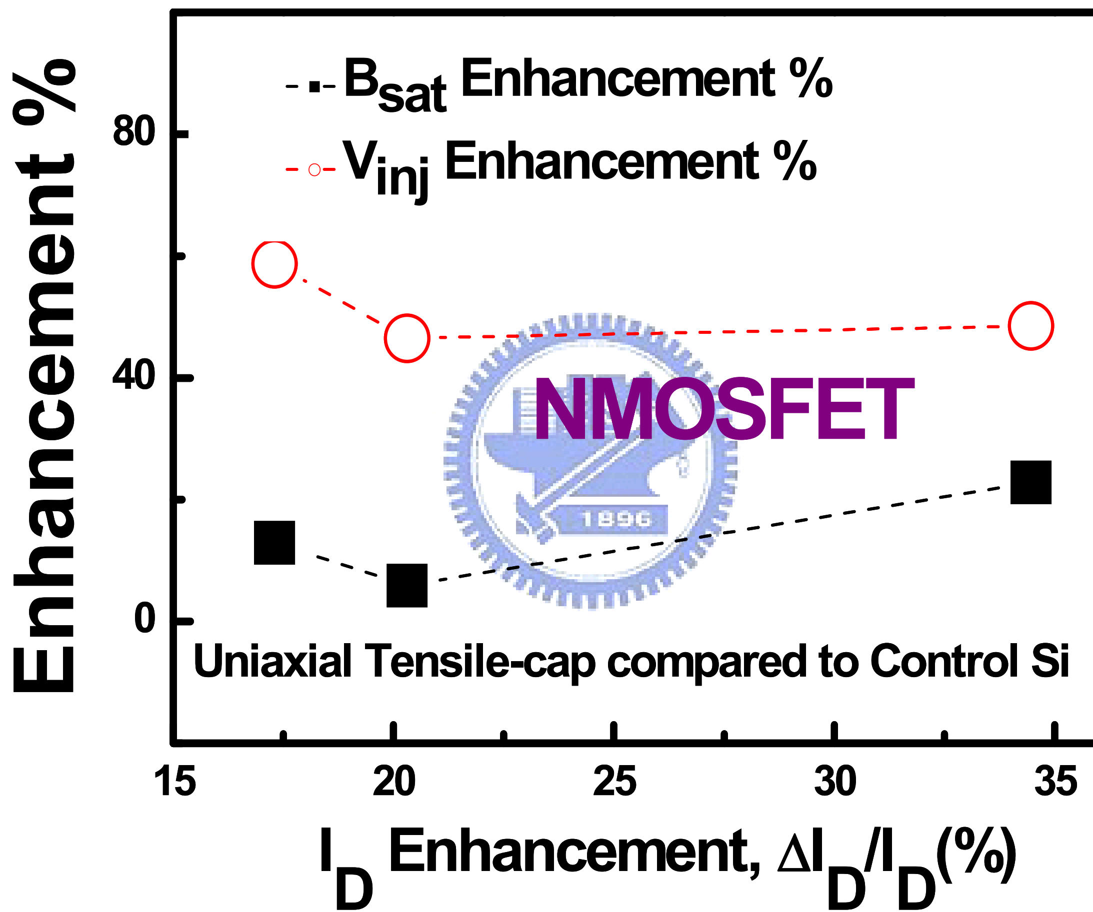


Fig. 4.1 The current enhancement relates to channel backscattering parameters of uniaxial strained-nMOSFET. Both B_{sat} and V_{inj} are enhanced while V_{inj} is enhanced about 50% than the control sample.

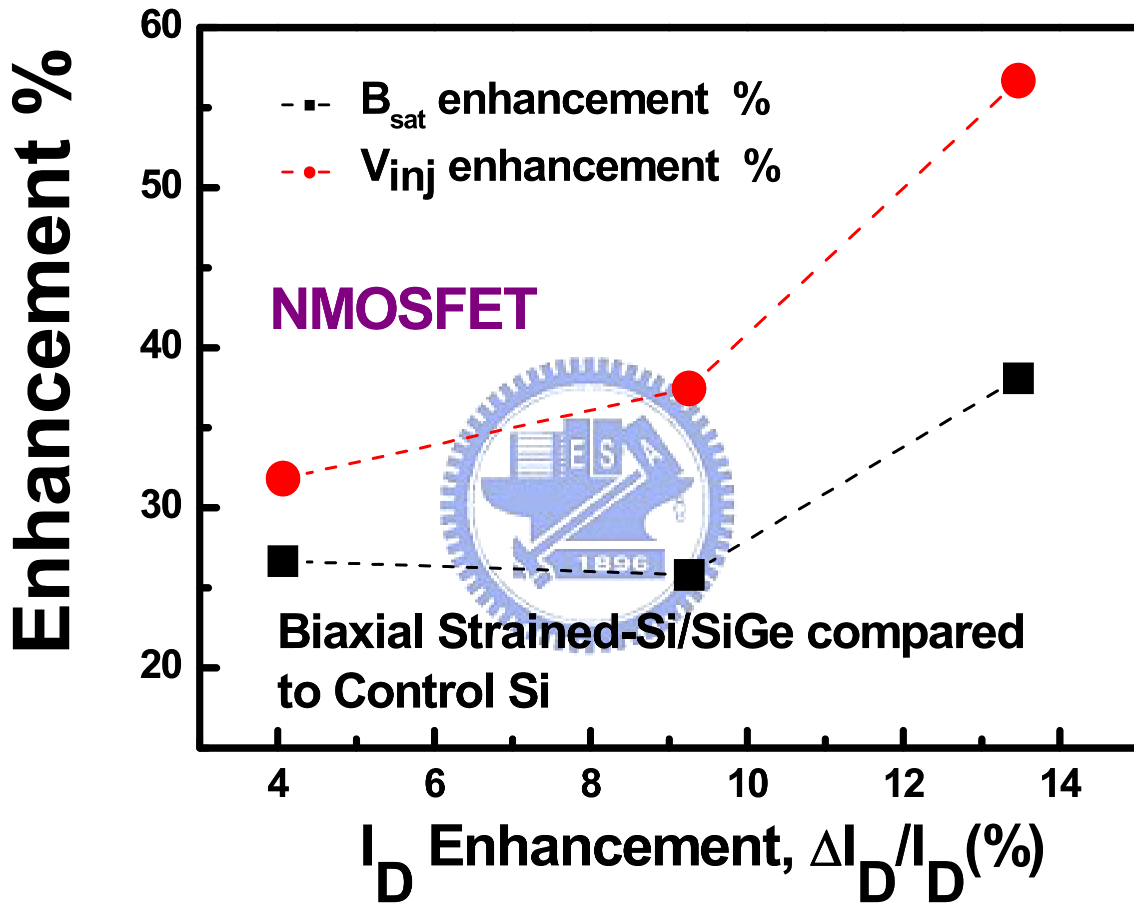


Fig. 4.2 The current enhancement relates to channel backscattering parameters of Biaxial strained-nMOSFET. Both B_{sat} and V_{inj} are enhanced, *and* V_{inj} is enhanced much larger than B_{sat}.

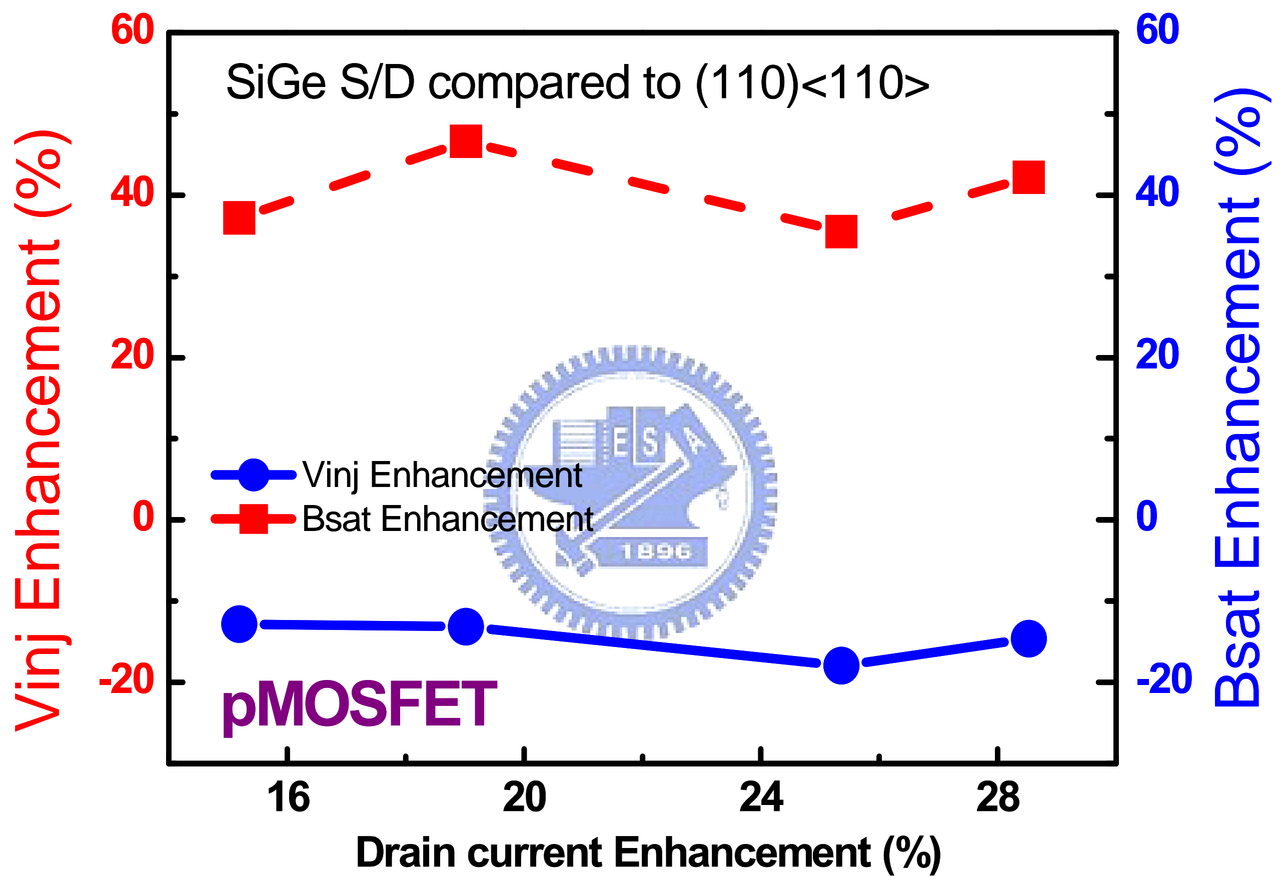


Fig. 4 .3 The current enhancement relates to channel backscattering parameters of uniaxial strained-pMOSFET. B_{sat} is degraded, while V_{inj} is enhanced.

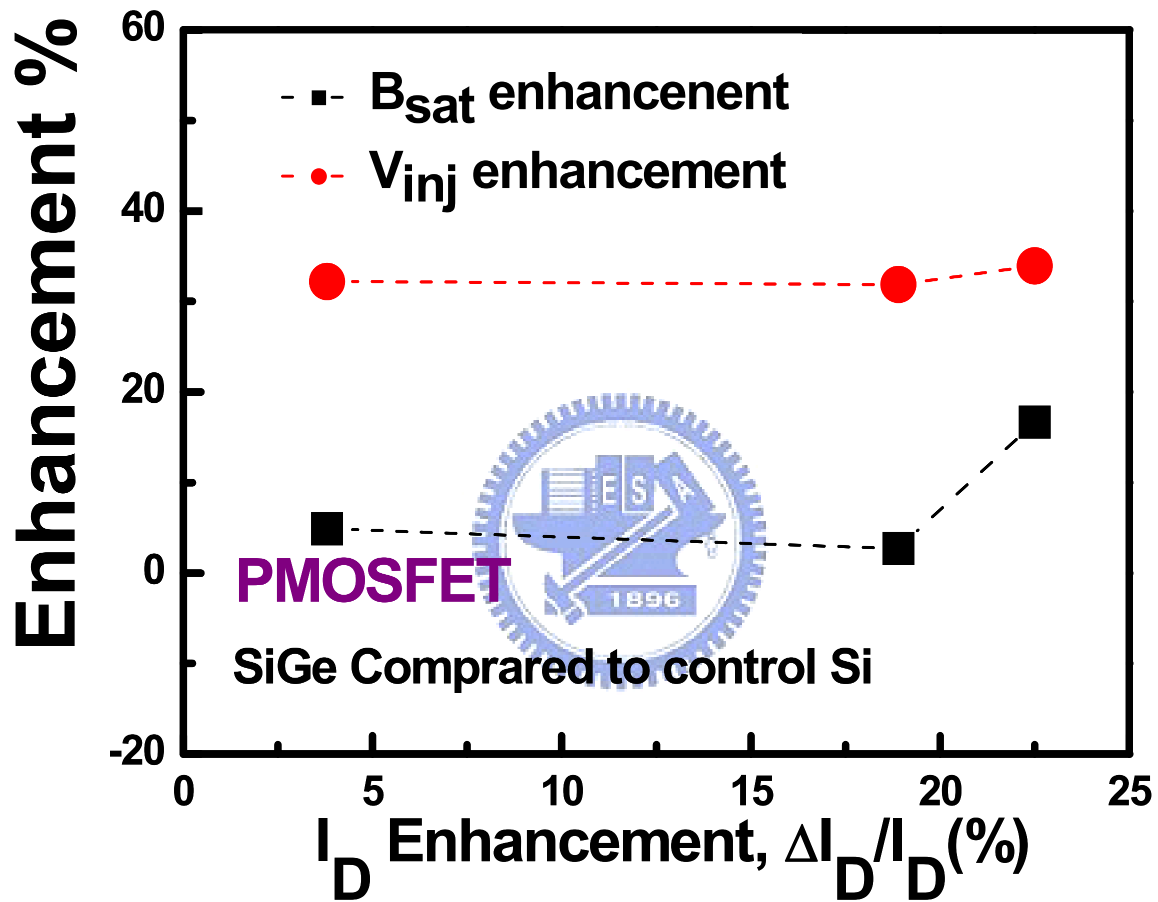


Fig. 4 .4 The current enhancement relates to channel backscattering parameters of biaxial strained-pMOSFET. Both parameters are enhanced. V_{inj} is enhanced about 40% and B_{sat} is enhanced about 9.8% in average.

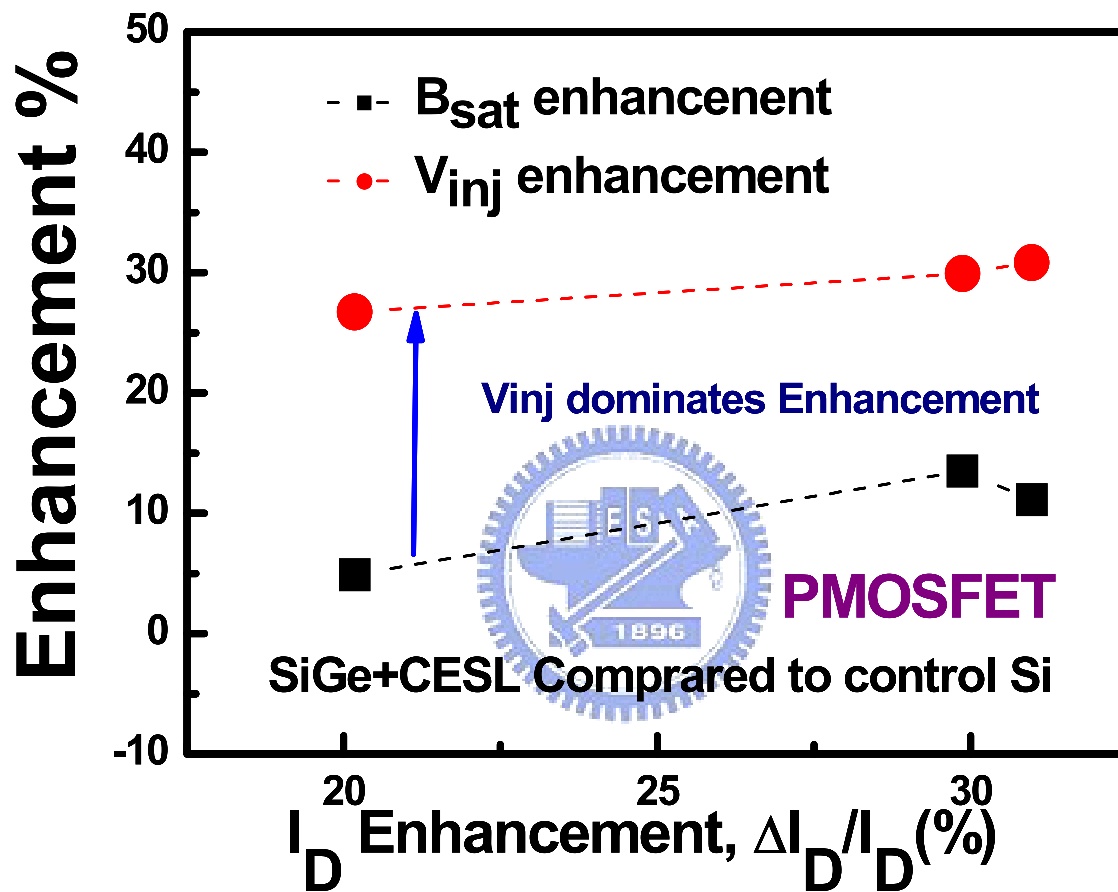


Fig. 4.5 The current enhancement relates to channel backscattering parameters of biaxial plus uniaxial (SiGe+CESL) strained-pMOSFET. Both V_{inj} and B_{sat} are enhanced.

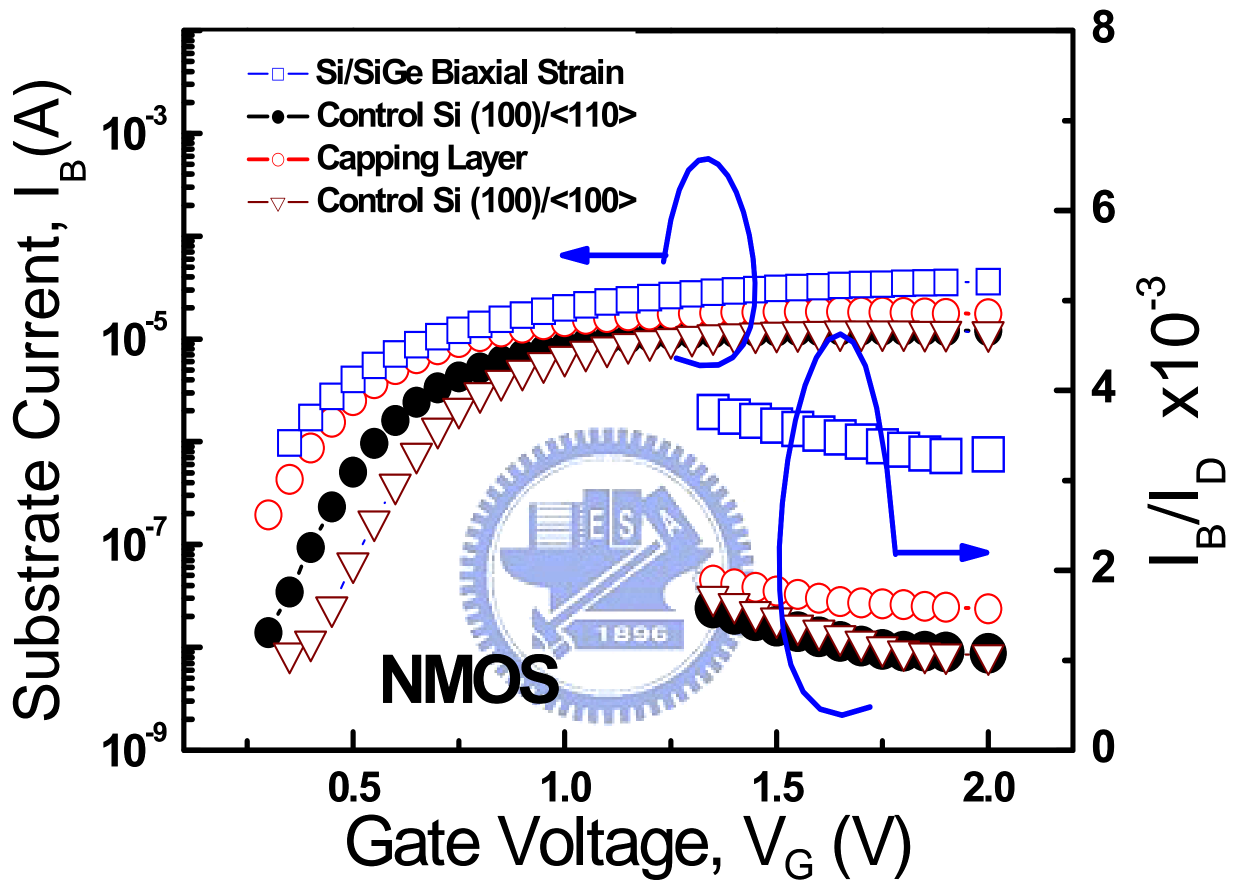
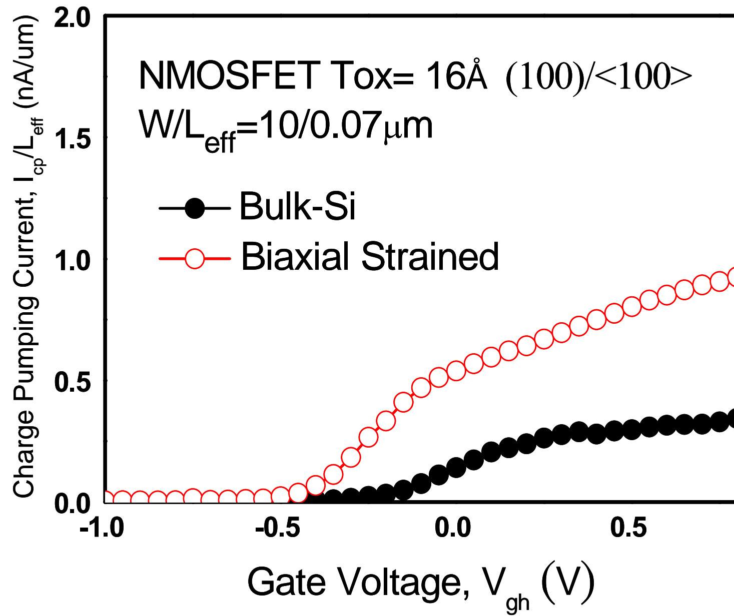
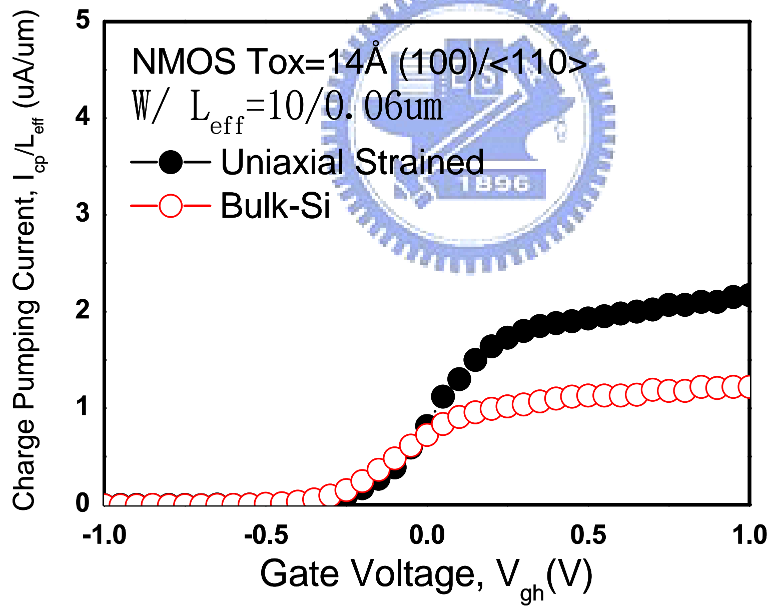


Fig. 4.6 The measured impact ionization current of the strained-Si device of pMOSFET. Biaxial strain has largest value while control<100>/(100) is the lowest.

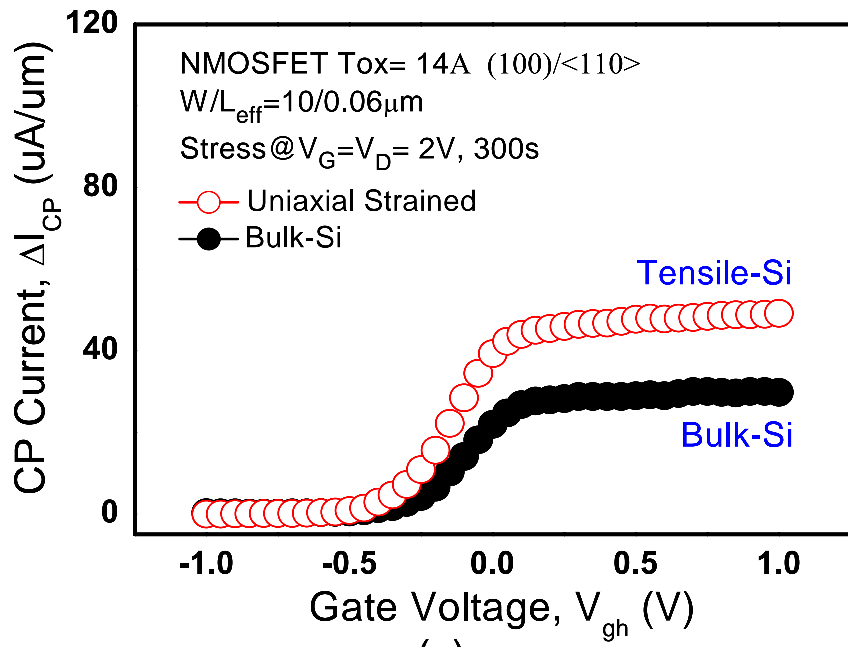


(a)

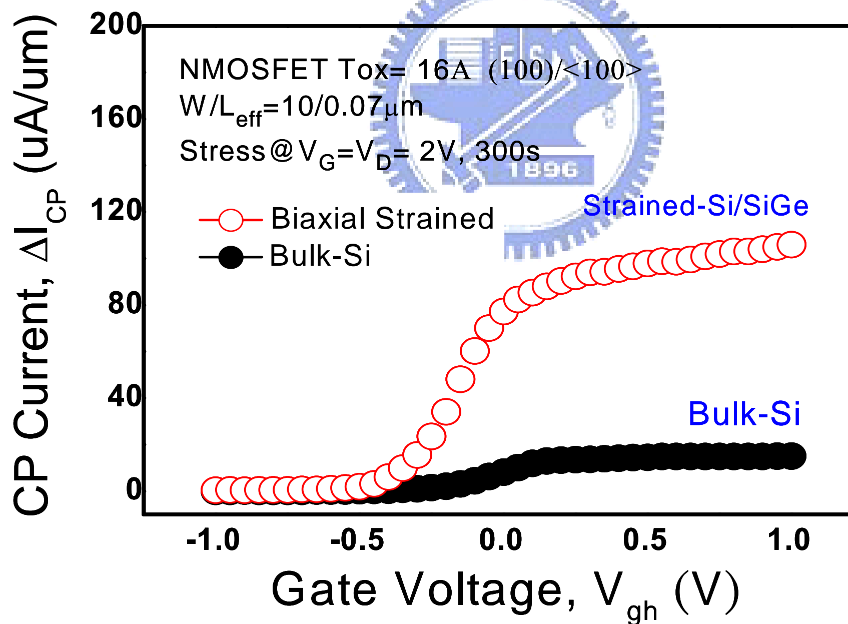


(b)

Fig. 4.7 The comparison of charge pumping currents in nMOSFET devices, including (a) bulk-Si and biaxial strained-Si/SiGe devices and (b) bulk-Si device and bulk-Si channel with tensile-cap layer.



(a)



(b)

Fig. 4.8 The comparison of charge pumping currents in nMOSFET devices after HC stress at 300s including (a) bulk-Si and biaxial strained-Si/SiGe devices and (b) bulk-Si device and bulk-Si channel with tensile-cap layer.

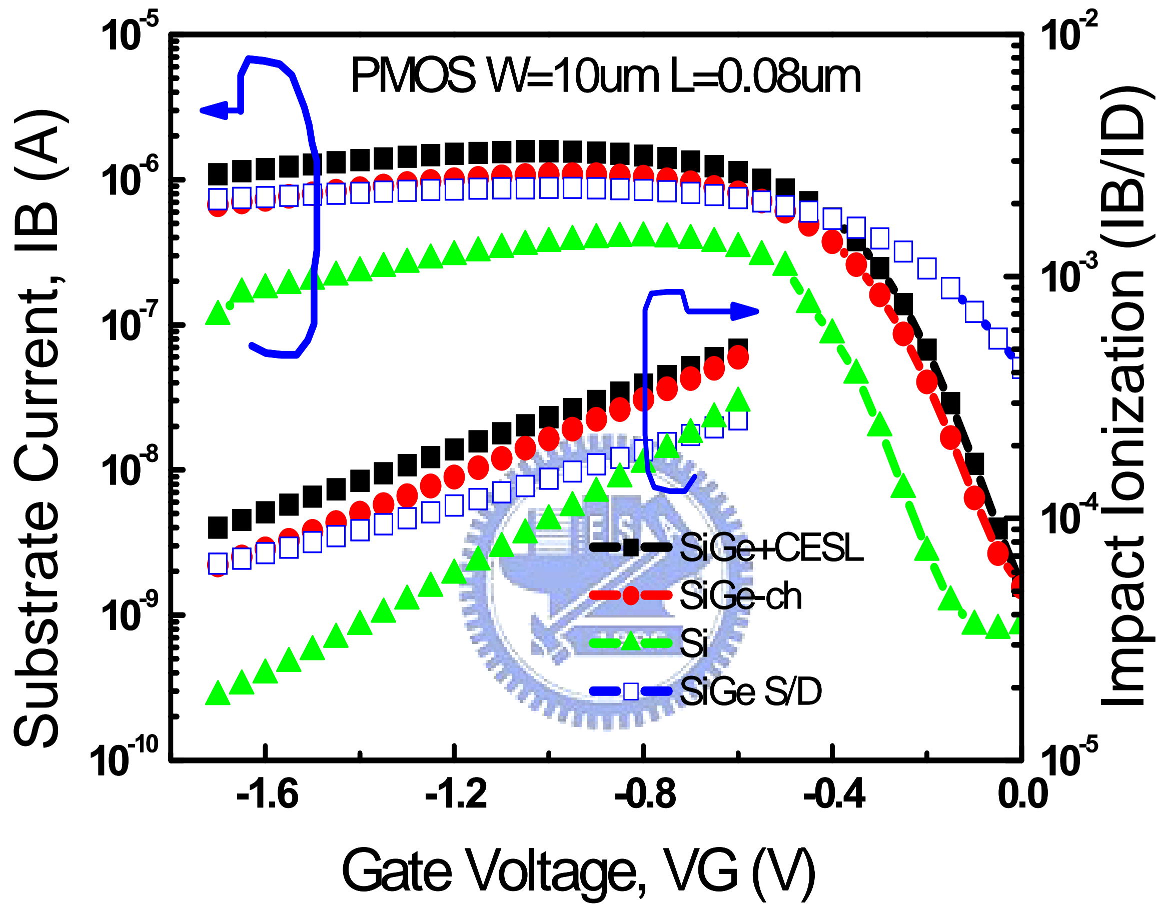


Fig. 4.9 The measured impact ionization current of the strained-Si device of pMOSFET, in which SiGe+CSEL has the largest impact ionization rate, next is SiGe channel. The lowest is the control sample.

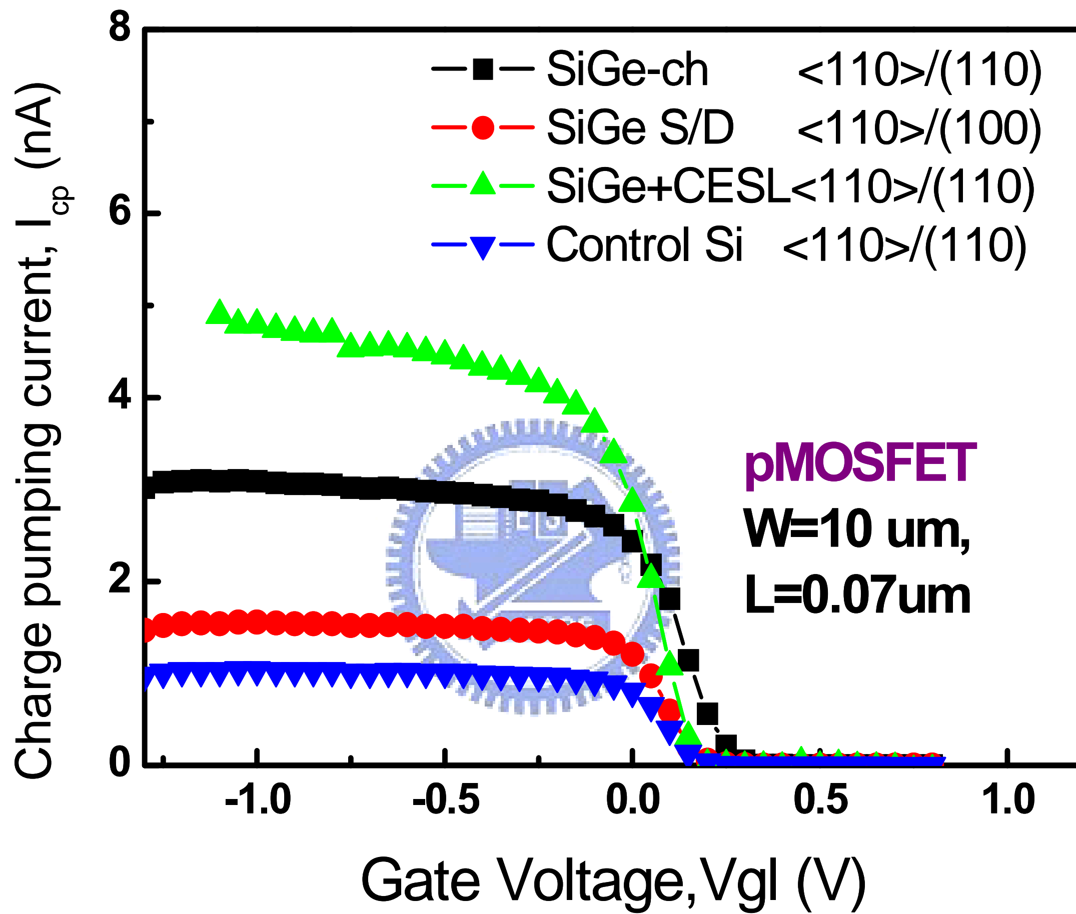


Fig. 4.10 The comparison of charge pumping currents in pMOSFET devices, in which control shows lowest value while SiGe+CESL is the largest.

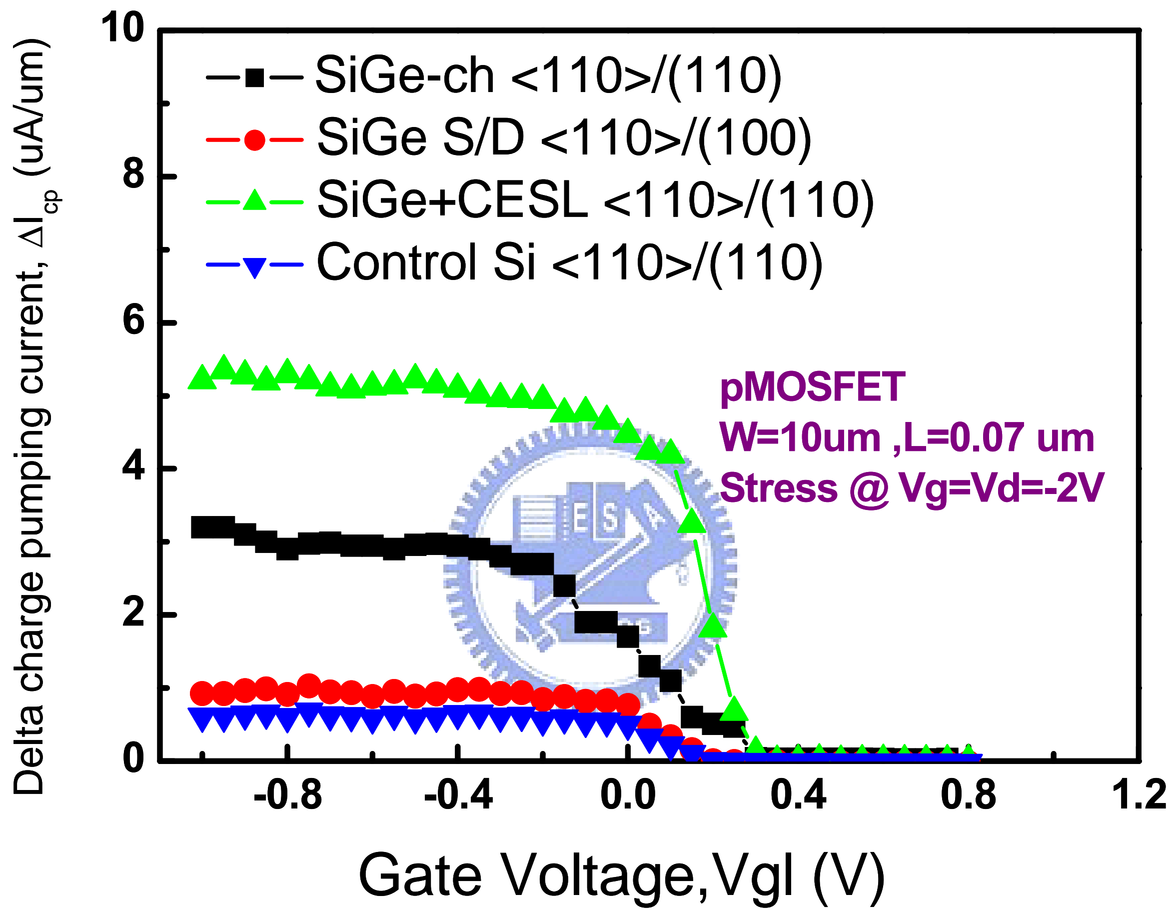


Fig. 4.11 The comparison of charge pumping currents in pMOSFET devices after HC stress at 300s. The severe degradation is shown in SiGe+CESL device.]

4.4 Summary

In this chapter exhibits the relationships with reliability and current enhancement of CMOS. Form the backscattering theory, V_{inj} and B_{sat} are the two important factors to determine the drive current. Also in the experimental above, we can conclude that injection velocity is the most important parameter to cause the device performance enhance. In every device we measured, we find that ΔV_{inj} is always occupied a huge portion to influence the performance.

The reliability of strained-devices is inevitable an important issue of the practice application. And we can use this simple theory to predict the essential effect of reliability (impact ionization rate). The lower barrier is the more carriers will transport to the drain region, and the larger the injection velocity is the higher the energy the carriers have. Fig. 4.12 illustrates the mechanism, in which the carriers possess higher Vinj and pass through the lower barrier will have more probability to collide the lattice and hence to produce electron-hole pairs.

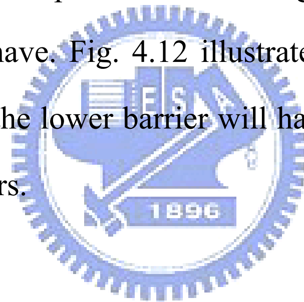


Table 4.1 is the summary of this thesis, including the average of ΔV_{inj} , ΔB_{sat} and the superposition of these two parameters. The value of superposition of ΔV_{inj} and ΔB_{sat} is proportional to the impaction ionization rate. Hence form the table 4.1, we can see that in nMOSFET biaxial tensile strain will has the reliability issue than uniaxial strainecd-nMOSFET for for its value of $\Delta V_{inj} + \Delta B_{sat}$. In pMOSFET, uniaxial strain strained-pMOSFET with SiGe S/D exhibits lowest value of $\Delta V_{inj} + \Delta B_{sat}$, hence it will has better reliability than the other strain technique. Although twice-strain technology is applied to the channel to promote the performance to 56% than control (100) device, but also due to the effect to cause the interface face un-uniform. The SiGe+CESL device shows the worst reliability of the testing device. From the result above, we can back to the Fig. 4.5: the rank of impact ionization rate, which demonstrates the same rank of the n-pMOSFET. The value of superposition of ΔV_{inj} and ΔB_{sat} is a good guide to predict the device reliability.

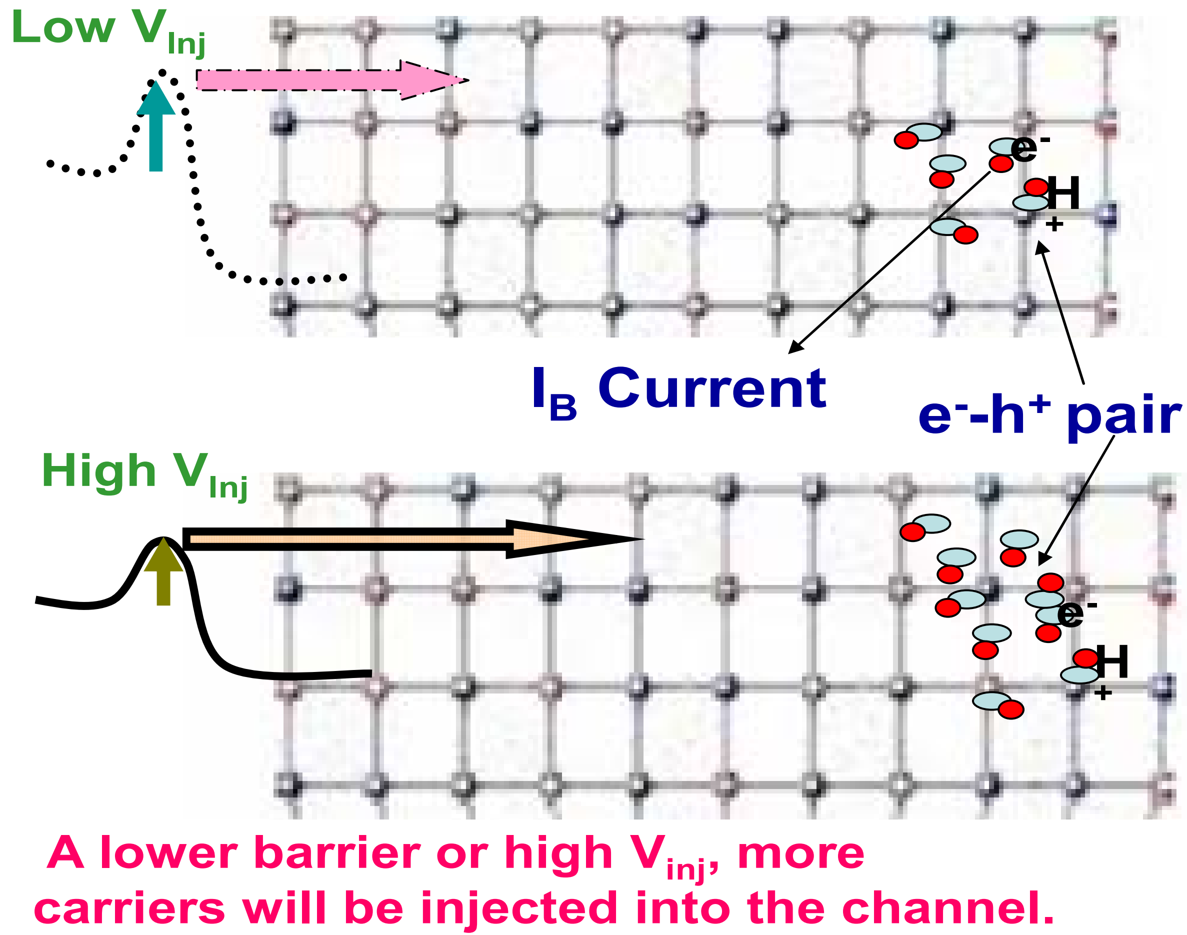


Fig. 4.12 The schematic diagram of bulk current which is related to the barrier and injection velocity of the carriers. Carriers which exhibit higher V_{inj} and a lower barrier will have more probability to collide with the lattice and hence produce electron-hole pairs

nMOSFET Tensile -Strain			pMOSFET Compressive -Strain		
	Biaxial – strain (SiGe-ch)	Uniaxial - Strain (CESL)	Uniaxial – Strain (SiGe S/D)	Biaxial-Strain (SiGe-ch)	Biaxial-Strain + CESL
< B_{sat} >	+ 30%	+13.8%	- 14.6%	+ 9.8%	+ 3.6%
< V_{inj} >	+ 41.9%	+51.3%	+ 21.1%	+ 4 %	+ 29%
< B_{sat} >+ < V_{inj} >	+ 71.9%	+65.1%	+ 6.5%	+ 13.8%	+ 22.6%
compared to control Si					

Tab. 4.1 The summary of this thesis, including the average of, and the superposition effect of the two parameters. For nMOSFET, uniaxial shows better reliability than biaxial strain. For pMOSFET, SiGe S/D device demonstrates the best reliability among the strained sample.

Chapter 5
Summary and Conclusion

In order to realize high-speed scaled CMOS devices for logic applications, short channel CMOS devices incorporating thin strained-Si surface channels, which can enhance mobility, have evolved as a potential candidate for high speed and low power logic CMOS technologies.

First we show the backscattering characteristics of n-pMOSFET, in the transport point of view we exam the device performance. For nMOSFET is better made by uniaxial strain using tensile capping layer. Since its high performance and better transport behavior, it is better made pMOSFET by SiGe+CESL technique than uniaxial strain. In Fig. 5.1 shows the ballistic efficiency as a function of channel lengths. In ballistic limited, it should equal to 1. There are three dash lines in the Fig. 5.1, blue line is the projection line of the measurement of Dr. Lin [22] [25], red dash line is the projection line of the measurement of other bulk Si devices [26]. And in brown dash line is the projection line of this work. Comparing with three lines, we can see that brown line has better transport behavior in longer length to achieve ballistic limited. In Fig. 5.2 is shown the injection velocity versus channel lengths, the value also extracted from the group's research. To achieve thermal velocity limited, there are still lots of work to be studied.

In real devices, which are usually operated below ballistic and thermal velocity limit, there are constraints for their performance. So, to increase the device V_{inj} and B_{sat} characteristic is one way to enhance the performance. Especially V_{inj} is the dominant factor to determine the drain current, and it still has a huge gap to achieve thermal limit. We can start from here to enhance the device performance.

Also this theory is suitable to predict the device reliability, by detecting the height of the barrier and the injection velocity of the carriers.

In summary, comprehensive studies on the uniaxial and biaxial effects on the current enhancement have been provided for the first time. Two major design criteria for strained nMOSFET and pMOSFET technology for extreme high current enhancement have been provided. For nMOSFET, on <110>/(100), the uniaxial strain is more efficiency by comparing to the biaxial strain. For pMOSFET, a specific strain technique with the combination of SiGe-channel plus CESL on <110>/(110) provides an extremely high current gain. This observation has been the first reported to date. Moreover, a roadmap has also been established for both injection velocity and ballistic efficiency.

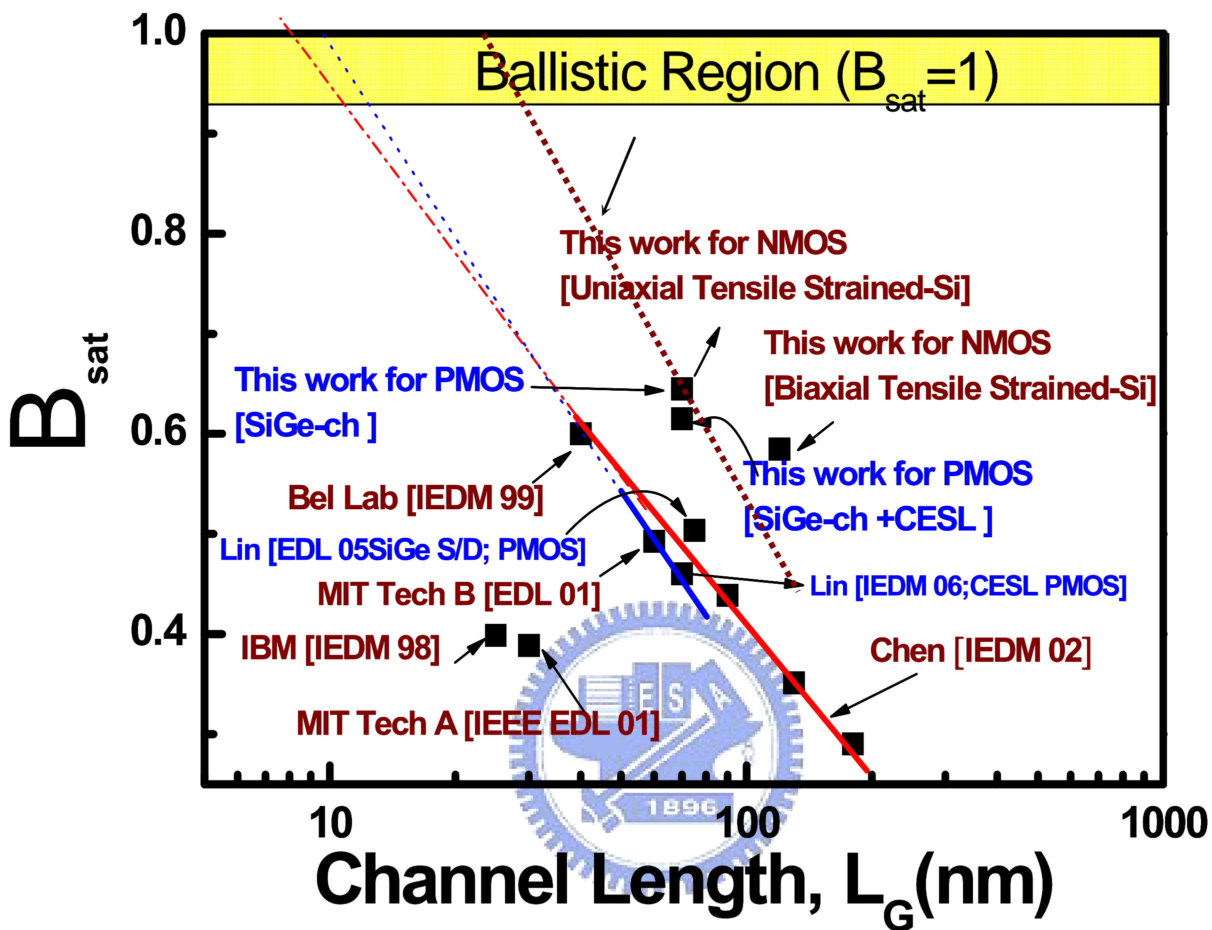


Fig. 5.1 The ballistic efficiency roadmap. There are three dashed lines in the Fig. 5.1, blue line is the projection line of the measurement of Dr. Lin [22] [25], red dash line is the projection line of the measurement of other bulk Si devices [26]. And, brown dash line is the projection line of this work

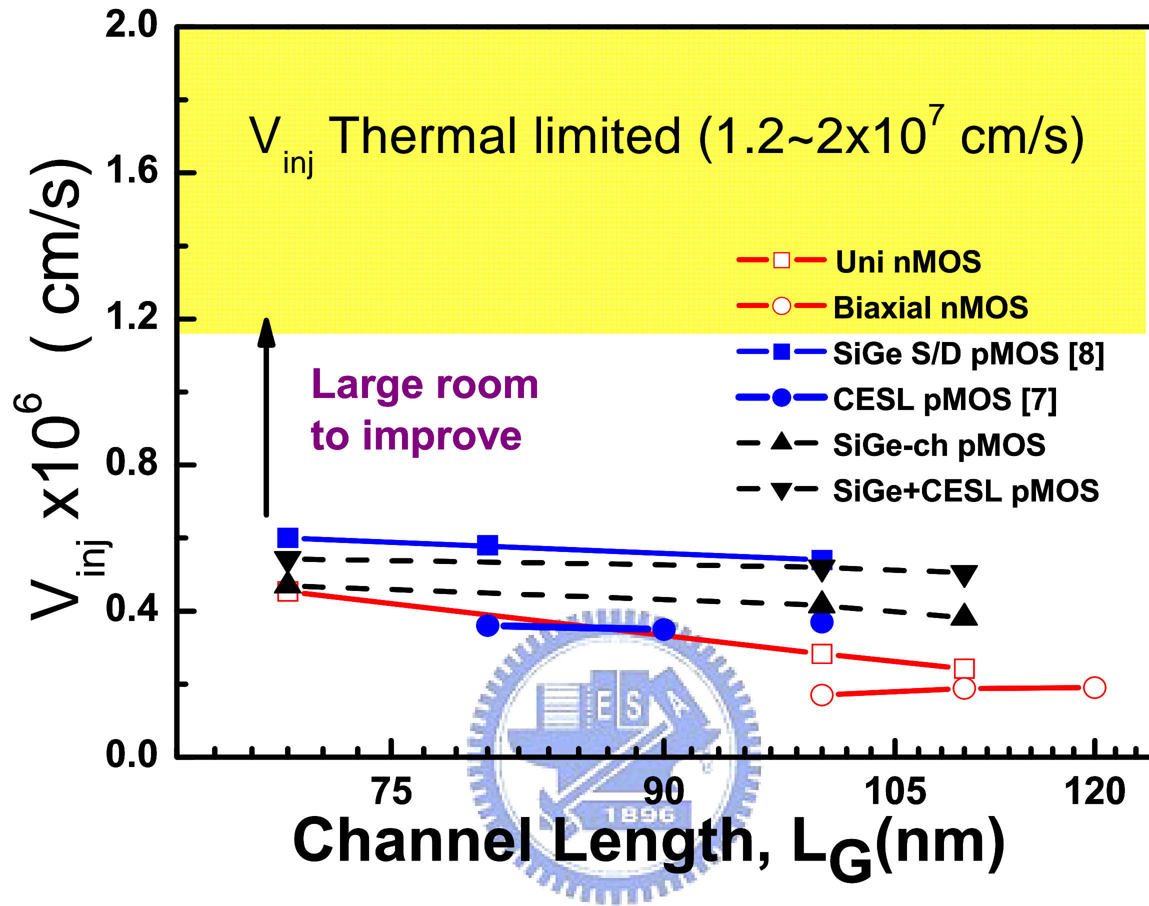


Fig. 5.2 The roadmap of reported injection velocity versus channel lengths. To achieve thermal velocity limit, lots of work still need to be studied.

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