國 立 交 通 大 學

電子工程學系　電子研究所碩士班

碩 士 論 文

電漿氣相輔助沉積氮化矽覆蓋層之形變 N 型金氧半場效電晶體之電流增強方法與可靠度之研究

A Study of Drive Current Enhancement Methods and Relability Issues of Strained NMOSFETS with PECVD SiN Capping Layer

研 究 生：詹凱翔

指導教授：林鴻志　博士

黃調元　博士

中 華 民 國 九 十 六 年 六 月

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研 究 生 ： 詹凱翔　　Student ：Kai-Hsiang Chan

指導教授 ： 黃調元　博士　　Advisors ：Dr. Tiao-Yuan Huang

林鴻志　博士　　Dr. Horng-Chih Lin

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碩 士 論 文

A Thesis

Submitted to Department of Electronics Engineering & Institute of Electronics

College of Electrical and Computer Engineering

National Chiao-Tung University

in Partial Fulfillment of the Requirements

for the Degree of

Master of Science

in

Electronic Engineering

June 2007

Hsinchu, Taiwan, Republic of China

中 華 民 國 九 十 六 年 六 月

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摘要

在本論文中，我們主要探討在 N 型金氧半場效電晶體中，利用電漿氣相輔助沉積(PECVD)氮化矽覆蓋層及其相關沉積製程參數對元件特性與熱載子退化效應的影響。我們在沉積氮化矽覆蓋層時，固定矽甲烷(SiH_4)與氨(NH_3)的流量，而調整氮(N_2)流量，使所沉積的氮化矽覆蓋層舒張應力增加，來造成元件通道的形變，進而增進元件載子遷移率。在實驗中，我們也利用一不同特性的電漿氣相輔助沉積系統，來沉積具壓縮應力的氮化矽覆蓋層，並證實了元件在舒張的應力下可得到較大電子遷移率，而在壓縮應力下則呈現相反的效果。另外，我們也證實在電漿氣相輔助沉積氮化矽的過程中，因為所施與的熱預算(thermal budget)並不算大，因此並未引起多晶矽空乏現象（poly-depletion）。除此之外，我們也發現氮化矽覆蓋會使元件熱載子退化效應更嚴重，但可藉由增加氮(N_2)流量使其退化效應下降。

因此在以電漿氣相輔助沉積系統沉積氮化矽覆蓋層時，我們可以藉由增加氮(N_2)流量使 N 型金氧半場效電晶體電性變好，而避免熱載子退化效應，達到雙贏的效果。

A Study of Drive Current Enhancement Methods and Relability Issues of Strained NMOSFETS with PECVD SiN Capping Layer

Student : Kai-Hsiang Chan Advisors : Dr. Horng-Chih Lin

Dr. Tiao-Yuan Huang

Department of Electronics Engineering and Institute of Electronics

National Chiao Tung University, Hsinchu, Taiwan

Abstract

Recently locally strained devices have emerged as the main technique for carrier mobility enhancement (e.g., SiN-capped devices). In this thesis, we investigated the impact of silicon nitride (SiN) capping layer and the associated deposition process parameters on the device characteristics and hot-electron degradation of strained NMOSFETs. The SiN layer used to induce channel strain for mobility enhancement was deposited by plasma-enhanced chemical vapor deposition (PECVD) by varying the flow rate of N_2, while fixing the flow rate of SiH_4 and NH_3, to adjust the tensile stress of SiN film. For comparison, we also fabricated devices with compressive SiN capping layer using another PECVD system. We confirmed that the electrical characteristics of devices with tensile SiN capping layer will be improved. In contrast, the compressive

SiN capping layer will degrade the device performance. We also found that the deposition of the SiN does not worsen the poly-depletion effect due to the light thermal budget. Furthermore, although the device hot-electron degradation is aggravated by the SiN capping layer, the degradation can be alleviated by increasing the flow rate of N_2. We thus conclude that the electrical performance and reliability can both be improved by increasing N_2 flow rate for NMOSFET with tensile SiN capping.

致謝

時光荏苒，歲月如梭，兩年的碩士生涯如此的結束了。一段旅程的結束，也代表著另一趟旅程的開始，而在期間，也遇到了許多貴人，對我的影響是深遠且巨大的。首先誠摯的感謝指導教授林鴻志老師與黃調元老師這兩年來的細心指導，黃老師豐富的經驗以及對實驗嚴謹的態度讓學生感到印象深刻，讓我們對研究的態度有著更深的認知。而林老師悉心的教導使我得以一窺電子領域的深奧，不時的討論並指點我正確的方向，使我在這些年中獲益匪淺。老師對學問追求的熱忱及其專業的知識也如同一盞明燈，讓我能夠在研究的過程中能夠追尋老師的方向前進。

本論文的完成另外亦得感謝國家奈米元件實驗室的研究員李耀仁博士的大力協助。因為有你的幫忙，讓一些奇怪的現象能有所解答，使得本論文能夠更完整而嚴謹。

兩年裡的日子，實驗室裡共同的生活點滴，學術上的討論、趕作業的革命情感、在 NDL 作實驗做到三更半夜.....，感謝眾位學長姐、同學、學弟妹的共同砥礪，你們的陪伴讓兩年的研究生活變得絢麗多彩。

感謝呂嘉裕學長、李明賢學長、蘇俊榮學長、盧景森學長、張凱翔學長、徐行徽學長，感謝你們能不厭其煩的指出我研究中的缺失，且總能在我迷惘時為我解惑，也感謝子儀的幫忙，恭喜我們順利走過這兩年，也祝你在未來邁向博士的求學生涯中能夠順遂。還有要感謝先進元件技術實驗室的其他成員朱馥鈺、陳瀅弘、林欣逸、王偉銘、黃育峯、李克慧、黃建富、王子銘、劉大偉、陳威臣、陳玲、江忠祐、洪政雄、李冠樟、林漢仲、洪文強，因為你們，得以讓我的碩士生涯能夠多采多姿。

最後，謹以此文獻給我摯愛的雙親詹閔樺先生與蕭麗慎女士，感謝你們這二十幾年來的養育之恩，總是默默的關心我照顧我，讓我能夠順利的完成求學的過程，在未來的日子裡我將會好好努力，以不辜負你們對我的期望。最後，僅將此論文獻給曾經幫助過我的人，在此表達最誠致的謝意。

2007.6.27 詹凱翔誌於風城交大

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Chapter 1
Introduction

1-1 General Background and Motivation

1-1.1 Strained Channel Technology

The “Moore’s Law” was proposed in 1964 by Gordon Moore who was a co-founder of Intel. The law states that the number of transistors integrated in a chip will be doubled every two years. Although the period for one-fold increase in transistor number is not precisely two years, for the past four decades the power-dependence on time implicated by the law has been successfully applied to the evolution trends of semiconductor industry. It can be said that the Moore’s Law has been playing the role of driver to propel and advance the performance of the integrated circuit (IC) performance. Furthermore, the Law may continue in the next two decades as indicated by Morris Chang, the president of Taiwan Semiconductor Manufacturing Company (TSMC).

The continuous shrinkage of device dimensions is the name of the game adopted by the main-stream companies in the industry to follow and push the “Moore’s Law”. The geometric scaling of Complementary Metal-Oxide- Semiconductor(CMOS) not only increases the circuit integration density, but also enhances the transistor performance. To address the short-channel effects, the device shrinkage has to be three dimensional in nature. In other words, in addition to channel length and width

scaling, thinner gate oxide and shallower junction depth are also essential to the development of a new generation of technology.

As evolving into the nano-scale era, severe short channel effects pose a big barrier ahead. Lowering in power supply voltage and ultra-shallow doping profile for source and drain junctions could help, but these measures are often accompanied with a penalty of drive current degradation. In addition, the increase in substrate doping concentration in order to reduce short channel effects causes mobility degradation. Recently strain channel engineering has demonstrated its capability to address these issues, and thus becomes more and more popular for practical manufacturing [1-4]. To this date at least two major strain channel technologies can be categorized. One is accomplished by applying a high bi-axial tensile strain to the channel region with a SiGe virtual substrate [1]. Another approach is to apply certain unique techniques to induce uni-axial strain in the channel [2-5]. The latter approach is more attractive because it can be easily implemented in modern Si CMOS processes. Uni-axial stress usually exhibits better performance enhancement when channel length becomes shorter [10-12]

Bi-axial tensile strain improves both NMOSFET and PMOSFET drive current by altering the band structure of the channel and can therefore enhance performance even at aggressively scaled channel length. The biaxial tensile channel stress by growing a

Si channel layer on a relaxed SiGe substrate has been demonstrated. Drive current of both NMOSFET and PMOSFET is enhanced by biaxial tensile stress when Ge is incorporated by more than 20% in the relaxed SiGe layer. However, the yield issue associated with high threading dislocation density (typically > 10^4 cm^{-2}) of the virtual SiGe substrates represents a major obstacle for practical applications. In addition, others concerns, such as high Ge content and up-diffusion, fast diffusion of n-type dopants, and high wafer cost, further blight the situation.

In order to find out a solution to eliminate the problems of the biaxial strain channel techniques, a number of uniaxial strain channel techniques have been proposed. In this aspect, channel strain can be engineered and optimized by modifying the device processing and/or structure, including those steps involving contact-etch-stop-layer (CESL)[13], shallow trench isolation (STI)[14], source/drain material[15], silicicidation [16], packing process[17], and so on. Furthermore, the behaviors of carrier mobility under uniaxial strain depend on the strength of the strain and orientation. Electron and hole mobilities respond to the complex three-dimensional mechanical stress in different and opposite ways. The channel tensile and compressive stress can be applied separately to NMOS and PMOS devices to enhance performance, respectively. It has been shown that the mechanical stress from a contact etch-stop SiN layer (CESL) over the gate electrode can significantly

affect the drive current. Depending on the deposition conditions, the SiN capping layer can generate either tensile or compressive stress [18]. It thus can be applied to the NMOS devices that benefit from tensile stress, as well as PMOS devices that benefit from compressive stress. (Fig. 1.1)

The carrier distribution in energy valley, scattering rate, and effective mass are the most significantly impact factors for mobility enhancement in strained-Si devices ($\mu = \frac{q\tau}{m^*}$, where $1/\tau$ is the scattering rate and m^* is the conductivity effective mass). Strain enhances the mobility by reducing the effective mass and/or the scattering rate. Both are important for mobility enhancement in electrons [19]. However, only effective mass change due to band warping and repopulation [20] plays a significant role in holes. For electron transports in bulk Si, the conduction band is composed of six degenerate valleys (Δ6) of the same energy, as illustrated in Figure 1.2 [21]. Strain removes the degeneracy between the four in-plane valleys (Δ4) and the two out-of-plane valleys (Δ2) by splitting them in energy. (Fig. 1.3) The energy difference (ΔE) between Δ2 and Δ4 sub-bands determines the total population in each sub-band. The enhancement caused by the splitting of conduction band can suppress inter-valley phonon scattering [22]. The lower energy of the Δ2 valleys indicates that they are preferentially occupied by electrons. The electron mobility is improved partly by reducing in-plane and increasing out-of-plane effective mass due to the favorable

mass of the Δ2 valleys, which results in more electrons with an in-plane transverse effective mass and out-of-plane longitudinal mass.

For holes, the valance-band structure of Si is more complex than the conduction-band structure. The complex band structure as well as valence-band warping under strain results in a much larger mobility enhancement of holes than electrons. This is why strained-channel PMOSFETs is a key focus in advanced logic technologies. Holes occupy the top two (the heavy- and light- hole) bands for unstrained Si. With the application of strain, the hole effective mass becomes highly anisotropic due to band warping, and the energy levels become mixtures of the pure heavy, light, and split-off bands. Thus, the light and heavy hole bands lose their meaning, and holes increasingly occupy the top band at higher strain due to the energy splitting. To quantify the mobility enhancement of holes, changes of scattering and effective mass depend on the altered valance band caused by the strain. From full band Monte Carlo simulation [23], PMOSFETs with uni-axial compressive stress may have lighter in-plane effective mass and thus show improved hole mobility. But, for biaxial tensile stress, the effective mass is heavier than that in the unstrained case. Thus the hole mobility enhancement is only possible through the reduction of inter-valley scattering [24]. This effect becomes significant only when the strain level is high enough (e.g.,Ge>20%). Reducing the intra-band acoustic scattering by altering

the density- of-states of the light- and heavy-hole bands is negligible for uni-axial strain in Si, even at several hundreds of mega-pascal.

The mobility enhancement of uni-axial strain at high vertical electric field is higher than that of the bi-axial case. This represents another advantage of uni-axial strain over the bi-axial strain. Hole mobility at high vertical field would have different behaviors between uni-axial compressive and biaxial tensile stress. The splitting of light- to heavy-hole band caused by uni-axial and biaxial stresses has no significant difference without considering surface quantization confinement. However, the splitting of light- and heavy-hole bands caused by bi-axial tensile stress would be annulled at high electric field due to surface confinement [11]. In contrast, hole mobility enhancement under uni-axial compressive strain is not annulled by surface confinement, which represents a major advantage for MOSFETs operating at high electric fields. The splitting magnitude of the surface confinement depends on the relative magnitude of the stress altered light and heavy hole out-of-plane effective masses. A recent report [11] showed the interesting result that the out-of-plane effective mass of light hole is heavier than heavy hole for uni-axial stress and causes the light to heavy hole band splitting to increase. On the contrary, for bi-axial stress the previously-reported out-of-plane effective mass of light hole is lighter than heavy hole and causes the band splitting to be reduced. This is why the bi-axial stress

degrades hole mobility enhancement at high vertical electric fields.

In strained-Si NMOSFETs, the strain will induce valence band offset. The negative valence band offset makes the Fermi level closer to the conduction band, thus, the band offset lowers the threshold energy and makes the channel depletion shallower. The fact that the threshold voltage shift caused by bi-axial tensile stress is larger than the case with uni-axial tensile strain has been reported for NMOSFETs [25]. This is because the bi-axial tensile stress induces more band gap narrowing than uni-axial tensile strain case. Similarly for PMOSFETs, larger shift of light-hole band edge under bi-axial tensile strain leads to larger shift in Vth than the case with uni-axial compressive strain [26].

1-1.2 Hot Carrier Effects

The knowledge of mobility enhancement in strain-Si is well known. It is found that it can effectively boost the driving current, but the issue of reliability remains a concern. In this aspect, device degradation induced by hot electrons represents one of the most critical reliability issues in deep sub-micron NMOSFETs [5-6], and have been widely investigated [7-8] previously. The degradations in terms of threshold voltage shift (ΔV_{th}), drain current degradation (ΔI_{DS}), and transconductance degradation (ΔG_m), are observed in the accelerated stress test.

If device dimensions are reduced while keeping the supply voltage relatively

unchanged, the lateral electric field in the channel increases significantly. The inversion layer charges will be accelerated more significantly, resulting in the generation of hot carriers, which may lead to undesired defect formation when they release energy at the channel/oxide interface or in the oxide. The mechanisms mentioned above are called hot-carrier degradation. It causes a time-dependent degradation of various MOSFET parameters, for example, threshold voltage, linear transconductance, subthreshold slope, and saturation slope, and saturation current.

The locations of damage region due to hot-carrier stressing were found to be adjacent to the drain of the device. The lifetime of the device is impacted by the spatial non-uniformity of this damage. The damaged locations and extent depend on a number of factors like device geometry, the duration and conditions of stress, oxide thickness, and drain extension structure. It was reported that the length of damaged region is more or less independent of channel length [27], its influence on device performance becomes more significant as the device is shrunk. This causes a dramatic increase in the percentage of drive current degradation as channel length becomes shorter under the same stress conditions.

1-2 Motivation

As mentioned above, the SiN layer can be used to induce channel strain for mobility enhancement [3][20]. However, in typical SiN capping processes abundant

hydrogen spicies will be incroporated into the channel which may significantly affect device reliability. In particular for NMOSFETs, despite the dramatic improvement in device performance with tensile SiN capping, their hot-carrier relability is, however, compromised. In one of our group's previous studies, we characterized the NMOS devices capped with a highly tensile SiN stressor layer. Although the stressor indeed showed improvement in carrier mobility and device drive current, we found that the extra hydrogen species incorporated during SiN deposition has undesirable influence on hot carrier reliability [9]. To reduce the impact of hydrogen without compromising the induced strain remains an important task. This motivates us to carry out this study intended to develop optimized SiN deposition conditions using plasma enhanced chemical vapor deposition (PECVD) system. The desirable SiN capping layers should have the ability to induce suitable stress in the channel but have reduced hydrogen content to avoid significantly degrading the hot-carrier reliability.

1-3 Organization of This Thesis

In addition to this brief introductory chapter, this thesis contains the following three chapters and their contents are described below:

In Chapter 2, we briefly describe the process flow for fabricating the NMOS devices with the SiN capping layer. We also present the characterization methods, measurement setups and the stress conditions.

In Chapter 3, we show and discuss the improvement on device performance with SiN capping layer by PECVD. The results on evaluating the hot carrier characteristics of the locally strained devices are presented. Effects of strain on the hot carrier effects are also discussed.

Finally, important conclusions generated from our experimental results are summarized. Certain recommendations and suggestions for future work are also given in this chapter.

Chapter 2
Device Fabrication and Measurement Setup

2-1 Device Fabrication and Process Flow

NMOSFETs used in this study were fabricated on 6-inch p-type (100) Si wafers with resistivity of 15~25Ω-cm and the wafer thickness is 655~695 μm. The p-type well was formed first by BF_2^+ implantation at 100 keV and 1×10^{-13} cm^{-2}. Standard local oxidation of silicon (LOCOS) process with channel stop implant (by BF_2^+ implantation at 120 keV and 4×10^{-13} cm^{-2}) was used for device isolation. Threshold voltage adjustment and anti-punch through implantation steps were done by implanting 40 keV BF_2^+ and 35 KeV B^+, respectively. After the growth of 3 nm-thick thermal gate oxide, a 150nm undoped poly-Si layer was deposited by low-pressure chemical vapor deposition (LPCVD), followed by gate etch process to pattern the film. The source/drain (S/D) extension regions were then formed by As^+ implantation at 10 keV and 5×10^{-14} cm^{-2}. After a TEOS spacer formation, S/D regions were formed by P^+ implantation at 15 keV and 5×10^{-15} cm^{-2}. Then the substrate electrode patterning was performed through lithography and etching processes, and the substrate junction was formed by BF_2^+ implantation at 40 keV and 5×10^{-15} cm^{-2}. Rapid thermal anneal (RTA) was then carried out in a nitrogen ambient at 900°C for 30 sec to activate dopants in

the gate, S/D, and substrate regions.

Afterwards, most samples were capped with a SiN capping layer (passivation layer,) under different flow rate ratio of N_2/SiH_4 (1, 2 and 20), with a thickness of 300nm, by using a plasma-enhanced chemical vapor deposition (PECVD) system. While some wafers were deliberately skipped of the SiN capping layer to serve as the controls. The SiN deposition was performed at 300 ℃ with SiH_4, N_2, and NH_3 as the reaction precursors. Then a 300nm TEOS was deposited for passivation by the same PECVD system.

The SiN layers used in the above fabrications exert tensile stress on the Si wafer it capped. To confirm the effects of different stress types on electrical characteristics of the fabricated devices, we also fabricate some devices capped with a compressive 300nm-thick SiN layer. The layer was deposited using another PECVD system.

After contact hole etching, normal metallization scheme was carried out. The final step was a forming gas anneal performed at 400°C for 30 min to mend dangling bonds and reduce interface state density in gate oxide/Si interface. Cross sectional view of the fabricated device is shown in Fig. 2.1. The three different conditions of the capping layers are listed in Table 2.1.

2-2 Measurement Setup

2-2.1 Electrical Measurement Setup

Current-voltage (I-V) and capacitance-voltage (C-V) characteristics were evaluated by an HP4156A precision semiconductor parameter analyzer and an HP4284 LCR meter, respectively. Temperature-regulated hot chucks were used to control and fix the temperature at 25°C.

Charge pumping measurement is widely used to characterize interface state densities in MOSFET devices [28]. This type of measurement is very effective because it allows the exclusion of gate leakage contribution to the calculated interface state densities presented in thin gate oxides and at lower frequencies [29-30]. Therefore, to accurately analyze interface state densities or bulk traps in the dielectrics from charge pumping measurement results, we need to pay close attention to the leakage current issue. The basic charge pumping measurement includes the measurement of the substrate current while a series of voltage pulses with fixed amplitude, rise time, fall time, frequency, and duty cycle is being applied to the gate of the transistor (Figure 2.2), with source and drain connected to a small reverse bias, and substrate tied to the ground. This seup allows us to apply three conventional types of voltage pulse train to the gate electrode, as depicted in Figure 2-3, i.e., (a) fixed amplitude sweep, (b) fixed base sweep, and (c) fixed peak sweep.

In this thesis, “fixed amplitude sweep” was used to calculate interface trap density, and “fixed base sweep” was used to analyze the lateral distribution of

interface trap, respectively. Square-wave waveforms (f = 1MHz) were applied to the gate, and the base voltage was varied to let surface condition from inversion to accumulation, while keeping the pulse amplitude at 1.5V. A MOSFET with a gate area of A_G gives the charge pumping current as [31]:

$$I_{cp} = qA_G fN_{it} \tag{2-1}$$

, and interface trap density (N_{it}) could be calculated by using this formula.

2-2.2 Hot Carrier Reliability Measurement Setup

In our reliability measurement, the device was stressed with the drain voltage biased at a highly positive voltage, and the gate biased at the voltage where maximum I_{sub} occurred to accelerate the degradation. So we must first measure the Isub-V_G curve with the drain terminal biased at a fixed voltage to find V_G@$Isub_{max}$, before we performed the hot-carrier stressing. To monitor the degradation caused by the hot electrons, the I_D-V_G characteristics at V_{DS} = 0.05 V (linear region) and charge pumping current were measured before and after the stress. The degradations in terms of threshold voltage shift (ΔV_{th}), interface trap density degradation (ΔN_{it}), and transconductance degradation (ΔG_m), were observed in the accelerated stress test.

2-2.3 Extraction Procedure of Lateral Distribution of Nit

The lateral distribution of interface state post hot carrier stress of all splits was also discussed in this work. This method was built on [32] and the measurement setup is shown in Fig. 2.4. The experimental procedures of this method are described below.

(1) Measure the Icp-V_h curve on a virgin MOSFET from the drain junction (with the source junction floating), and from it establish the V_h versus $V_{th}(x)$ relationship[32] near the junction of interest.

(2) Record the Icp-V_h curve after hot-carrier injection.

(3) The hot-carrier-induced interface state distribution, $N_{it}(x)$, is obtained from the difference of the Icp-V_h curve before and after hot carrier stress.

Chapter 3
Results and Discussion

3-1 Electrical Characteristics of Locally Strained NMOSFETs

3-1.1 Basic Electrical Characteristics

The stress measurements were performed on Si wafers capped with a blanket SiN layer with different flow rate ratio of N_2/SiH_4. The results are showed in Table 3.1 It can be seen that the tensile stress becomes larger when N_2/SiH_4 flow rate ratio is larger. This is reasonable as the thermal expansion coefficient of a deposited film depends on the film's composition which can be adjusted by varying the flow rate of precursors.

Figure 3.1 shows I_D-V_D Characteristics of NMOSFETs for all splits of samples. It can be seen that Tensile-SiN-capped splits depict an obvious drain current enhancement with respective to the control devices. Further, the enhancement increases as flow rate ratio (N_2/SiH_4) increases. In contrast, current degradation is observed for the Compressive-SiN-capped samples. Obviously the current enhancement and degradation is straightly due to the strain type and magnitude of the strain introduced by the SiN capping layer. The Id-Vg characteristics of the same devices are shown in Fig 3.2. We can see that the impact of SiN-capping layer mentioned above also reflects on the result of transconductance (Gm). Fig 3.3 shows that subthreshold swing of all SiN capping splits depicts similar value and is slightly

lower than that of TEOS control. This is ascribed to the hydrogen species contained in the SiN that tends to passivate the interface states, resulting in better subthreshold swing among the splits. This is evidenced from the results of charge pumping current (Icp), as shown in Fig. 3.4. Obviously, all SiN capping splits have lower Icp than TEOS controls.

Fig 3.5 shows the percentage change in transconductance (Gm) of the Tensile-SiN-capped and Compressive-SiN-capped samples with respect to the controls, as a function of channel length. We can see that the drive current enhancement reaches about 0.8%, 8.8%, and 15.4% at a channel length of 0.4 μm for Tensile-SiN capped devices with N_2/SiH_4 flow rate ratio of 1, 2, and 20, respectively, while the device capped with compressive SiN shows about -12.6% degradation. It can also be seen that when the channel length decreases, the strain effect enhances. In other words, the strain is distributed locally near the source and drain, and the overall impact becomes more significant as channel length is shorter. The capacitance-voltage characteristics of the samples are shown in Fig 3.6. It can be seen that the oxide thickness difference among all splits is negligible, indicating that the above-mentioned results are not caused by the oxide thickness difference. The poly depletion effect is not observed in the SiN-Capped devices. From our group's previous studies, poly depletion effect was clearly observed when LPCVD SiN was

deposited to serve as the tensile strain booster. The LPCVD process was performed at a medium temperature of 780˚C which had a much lower solid solubility than high temperature [33](e.g., 950 ℃, the RTA temperature used in the fabrication to active the dopants in the poly). Since the PECVD process was performed at 300˚C which was so low that the associated thermal budget would not affect the activated carrier concentration, therefore the poly depletion effect did not get worse.

It is well known that the use of interlayer dielectric will increase RC time delay. The dielectric constant of the deposited SiN film should thus be considered. Fig 3.7 shows the dielectric constant of different SiN film, it is clearly seen that there is no distinct difference among all splits of samples, thus these deposited films would not worsen the RC-delay issue.

.

3-1.2 Short Channel Effects

Threshold voltage (V_{th}) roll-off characteristics of the devices are shown in Fig. 3.8. The results are obtained at V_{DS} = 0.05 V. It is shown that all samples depict a reverse-short-channel-effect (RSCE). This can probably be explained by boron segregation at the implant-damaged regions located near the edge of the channel. Additional thermal budget may alleviate the reverse-short-channel-effect. It might be related to the redistribution of dopants that effectively reduced the boron segregation effect [34]. In this thesis, however, the passivation layer was deposited by PECVD

operated at 300 ℃, a temperature too low to redistribute the dopants in the channel, it thus has negligible influence on this phenomenon.

Drain induced barrier lowing (DIBL) is another guide for evaluating the short channel effects. We use the interpolation method to calculate DIBL effect for all splits of devices. The results are shown in Fig. 3.9, basically no distinct difference among different splits is observed. It points out that SiN capping layer does not complicate the DIBL effect of the samples.

3-2 Hot Carrier Degradation of Locally Strained NMOSFETs

From the discussion mentioned in Chapter 1, it is expected that devices with SiN capping would encounter serious hot carrier degradation. Typical results of hot-electron stressing for the control and three other splits are shown in Fig 3.10. Channel length and width of the test devices are 0.5 μm and 10 μm, respectively. The devices were stressed at V_{DS} = 4.6 V and V_{GS} at maximum substrate current. The I_D-V_G characteristics at V_{DS} = 0.05 V were measured before and after the stress to check the degradation caused by the hot electrons. As shown in Fig 3.10, the degradation is the worst in the SiN-1 sample among all samples. Fig. 3.11 and Fig. 3.12 show shift of threshold voltage and generated interface state density as a function

of stress time for all splits of samples, respectively, of hot-electron stressing at V_{DS} = 4.6 V and V_{GS} at maximum substrate current performed on all splits of devices with channel length/width = 0.5μm/10μm. As can be seen in the figures, the effect of flow rate of precursors in SiN deposition is significant. We can see that the device lot with ratio of N_2/SiH_4=1 depicts the worst degradation in terms of the largest ΔV_{th}. By contrast, the lot with flow rate ratio N_2/SiH_4=20 apparently shows much improvement in this aspect, although it also results in the largest mobility and on-current enhancement. Increase in interface state generation (ΔN_{it}) shows the same trend. This finding is interesting and important, and is ascribed to the hydrogen content and the dynamic transport of these hydrogen species by the thermal cycles during processing. It is well known that the breaking of Si-H bonds at the interface is one of the major reasons responsible for the hot-carrier degradation. The abundant hydrogen species contained in the SiN definitely aggravate the reliability. Hydrogen atoms tend to bond with nitrogen for nitrogen-rich film with increasing N_2 flow rate, N-H bonds are thermally more stable than Si-H bonds [35]. This may result in less diffusion of hydrogen species from the SiN to the oxide/channel interface. In addition, less Si-H bonds is expected for flow rate ratio of N_2/SiH_4=20, since N_2 instead of NH_3 serves as the major nitrogen source. More evidences can be found in Fig. 3.13 and Fig 3.14. Fig. 3.13 shows the charge pumping current after 5000-second hot carrier stressing

(V_G@$Isub_{max}$ and V_{DS} = 4.6 V) for the three splits of devices, and Fig. 3.13 shows the increase in charge pumping current after the stressing. As mentioned above, the hydrogen species contained in the SiN tends to passivate the interface states. More H-terminated bonds at the interface are expected for the SiN-1 split, and these bonds would dissociate and result in largest increases in charge pumping current shown in the figures. In contrast, it is seen that the SiN-1 and SiN-3 samples exhibit less generated interface states among the three Tensile-SiN-capped devices, implying H-terminated bonds are dramatically reduced.

3-3 Analysis of the Distribution of Interface Trap Density

The measurement presented in Section 2-2.3 was used to extract lateral distribution of interface trap state. It should be noted that the local V_{th} and V_{fb}, across the MOSFET, are not uniform due to the lateral doping variation with a schematic like that shown in Fig. 3.15. In order to detect the interface states, the pulse train during the measurement must undergo alternate accumulation and inversion cycles. There should be no Icp as the voltage level of the high-voltage (V_h) is lower than the minimum V_{th} under the gate. When V_h starts to exceed V_{th} at certain channel locations under the gate, Icp begins to grow. From the profile illustrated in Fig. 3.15, before V_h reaches the maximum local Vth in the channel, interface states that contribute to Icp are those residing near the drain side, owing to that fact that the needed electrons

cannot yet flow to the drain side from the source.

We choose the control sample as an example. If we assume that interface state density is spatially uniform along the channel, which can be written as

$$I_{cp,\max} = q\, f\, N_{it}\, W\, L \tag{3-1}$$

where f is the gate pulse frequency, W the channel width, and L the channel length. Because V_{th} is not uniform, when V_h reaches the maximum local V_{th} in the channel, only interface states residing near the drain side (like the shadow region in Fig. 3.15) will contribute to Icp. In Fig. 3.16, the corresponding Icp (V_h) comes from the interface states distributed between the gate edge and the position where its local V_{th} is equal to V_h, i.e.,

$$I_{cp}(V_h) = q\, f\, N_{it}\, W\, x \tag{3-2}$$

where x represents the distance from the gate edge to the position where $V_{th}(x) = V_h$. Comparing (3-1) and (3-2), we can derive

$$x = \frac{L I_{cp}(V_h)}{I_{cp,\max}} \tag{3-3}$$

Fig. 3.17 shows the local V_{th} versus distance x of the control sample. The local V_{th} decreases sharply as x is smaller than 0.07 μm. We can therefore presume that the drain junction is near x = 0.07 μm.

After 10 second hot carrier stress (V_G@$Isub_{max}$ and V_{DS} = 4.5 V), the incremental charge pumping current (*ΔIcp*) is extracted and shown in Fig. 3.18. *ΔIcp*

at a certain V_h is proportional to the number of generated interface traps from the gate edge to the point x, and can be expressed as

$$\Delta I_{cp} = q\, f\, W \int_0^x N_{it}(x)\, dx \tag{3-4}$$

Therefore, Nit(x) generated by the hot carrier stress can be extracted using the following formula:

$$N_{it}(x) = \frac{d\Delta I_{cp}}{dx}\frac{1}{q\, f\, W} = \frac{d\Delta I_{cp}}{dV_h}\frac{dV_h}{dx}\frac{1}{q\, f\, W} \tag{3-5}$$

The relationship of $\frac{dV_h}{dx}$ versus x can be derived from V_h versus x, so the lateral distribution, *Nit (x)*, can be obtained from the measurement scheme mentioned above.

By utilizing the same procedure, the derived lateral profiles of the interface state distribution with all splits, extracted by Eq. (3-5), are shown in Fig. 3.19. From Fig. 3.19, we can realize and compare the damage region and amount of interface states generated by hot carrier stressing. We can see that the damage region is confined within the drain edge in all splits, which is reasonable since the degradation is confined t the drain edge under the HC stressing. It is obviously seen that the SiN-1 samples show larger degradation than the other splits. These results were consistent with the results and discussion mentioned in Section 3-2. In other words, the more hydrogen species exist at the source/drain edge, the larger interface states are generated, and therefore the worse degradation.

Chapter 4
Summary and Conclusion

4-1 Conclusion

In this thesis, the effects of PECVD SiN process and the channel strain induced by the SiN-capping layer on the device characteristics and hot-electron degradation were investigated. Several important phenomena were observed and summarized as follows.

Firstly, the channel strain induced by the tensile SiN capping layer over the gate greatly boosts the drive current of short-channel NMOS devices. For example, as high as 15.4 % enhancement is achieved for the SiN-capped NMOS devices with a flow rate ratio of N2/SiH4=20 at a channel length of 0.4 μm. This is ascribed to the large difference in the expansion coefficient between SiN film and Si-substrate. Since n-channel devices with a compressive SiN capping layer show lower Gm than the control samples, it can be confirmed that either current enhancement or current degradation can be observed by varying the strain polarity. In addition, we also find that without the associated thermal budget, the deposition of the PECVD SiN capping layer can not alleviate the reverse short-channel effect of the devices, and the poly-depletion effect will not be enhanced. Finally, we find that the dielectric constant for the SiN film grown with a flow rate ratio N2/SiH4=20 is not different from the

other two splits with different flow rate ratio.

Secondly, hot-electron degradation is negatively affected when the SiN layer is deposited over the gate. However, we find that the negative impact in reliability can be alleviated by properly tuning the flow rate of SiH4 and N2. The hydrogen atoms tend to bond with nitrogen for nitrogen-rich film with increasing N_2 flow rate, resulting in less diffusion of hydrogen species from the SiN to the oxide/channel interface.

In conclusion, we find that for the SiN-capped NMOS devices, the electrical performance and reliability both improve with increasing N_2 flow rate. In other words, SiN-capped devices with optimized SiN deposition condition can maintain enhanced mobility while showing alleviated hot-carrier degradation. Optimization of both SiN deposition process and the film properties is therefore essential for the implementation of uniaxial strain in NMOS devices.

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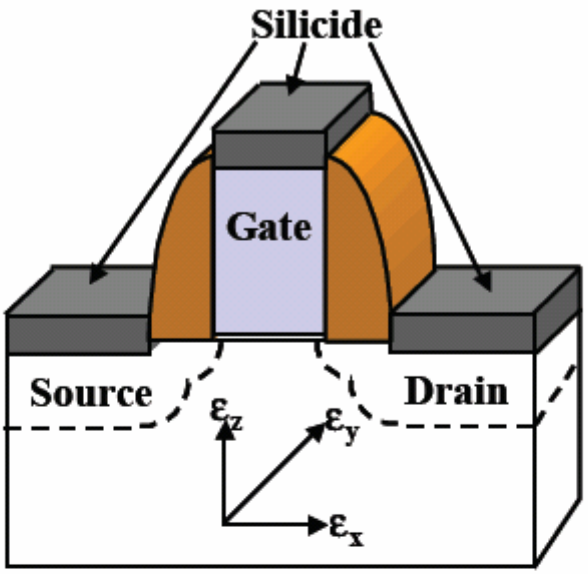


Figure 1 Schematic view of 3D process-induced strain components.

TABLE I Impact of 3D Strain Effects on CMOS Performance.
*Strain change = Increased tensile or decreased compressive strain

Direction of Strain Change*	CMOS Performance Impact	
	NMOS	PMOS
X	Improve	Degrade
Y	Improve	Improve
Z	Degrade	Improve

3D Strain Sensitivity of CMOS Current Drive

Fig. 1.1 Schematic illustration for 3D process-induce strain component[25]

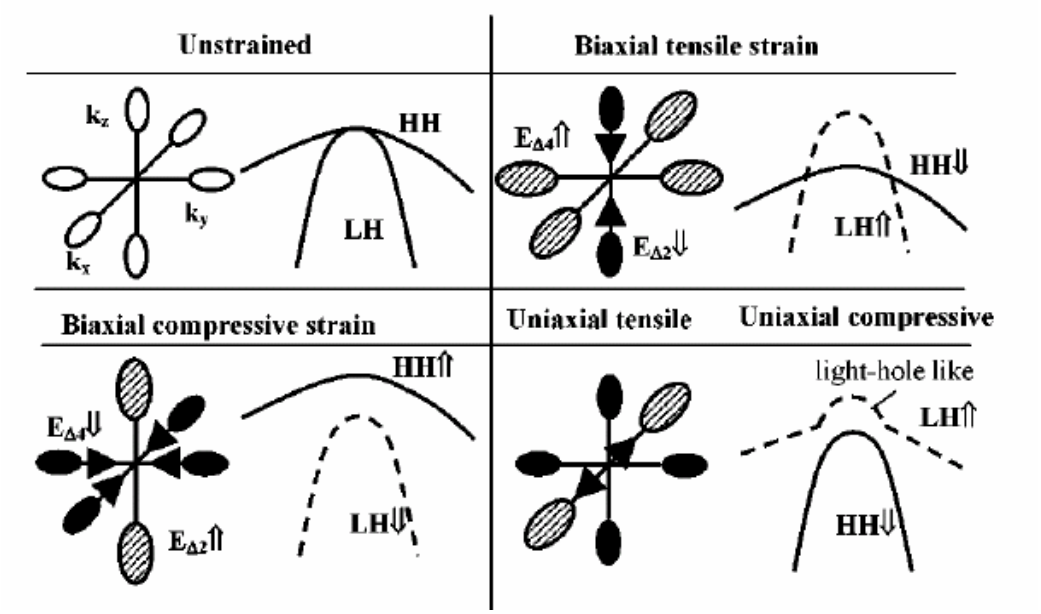


Fig. 1.2 Simple schematic of conduction and valence band bending with strain.[21]

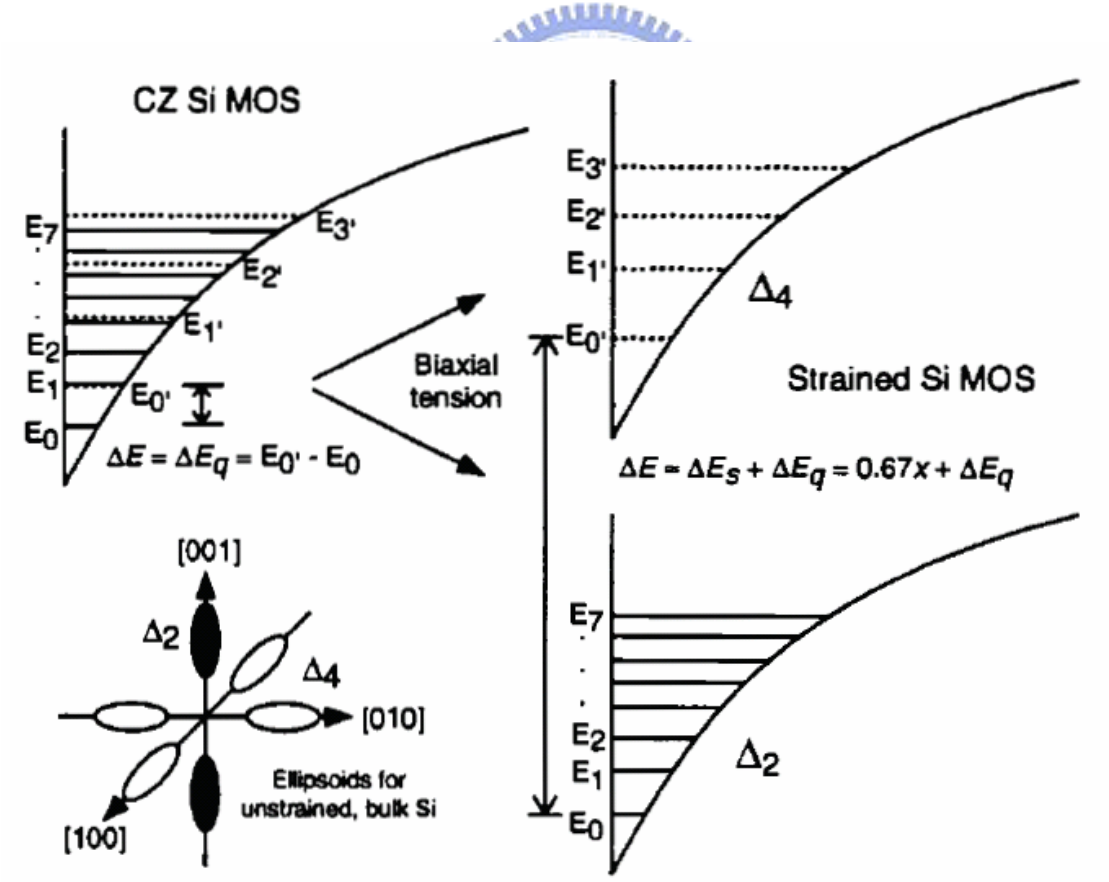


Fig. 1.3 Schematic diagram of the energy sub-bands with unstrained and bi-axial strain in an MOS inversion layer.[26]

Gate		SiN Passivation Layer (Flow rate ratio= N_2/ SiH_4)
Oxide 30Å	Undoped Poly-Si 1500Å	W/O (control)
		Flow rate ratio:1 SIN 3000Å
		Flow rate ratio:2 SIN 3000Å
		Flow rate ratio:20 SIN 3000Å
		Compressive SIN 3000Å

Table 2.1 Split table of capping layer and oxide thickness.

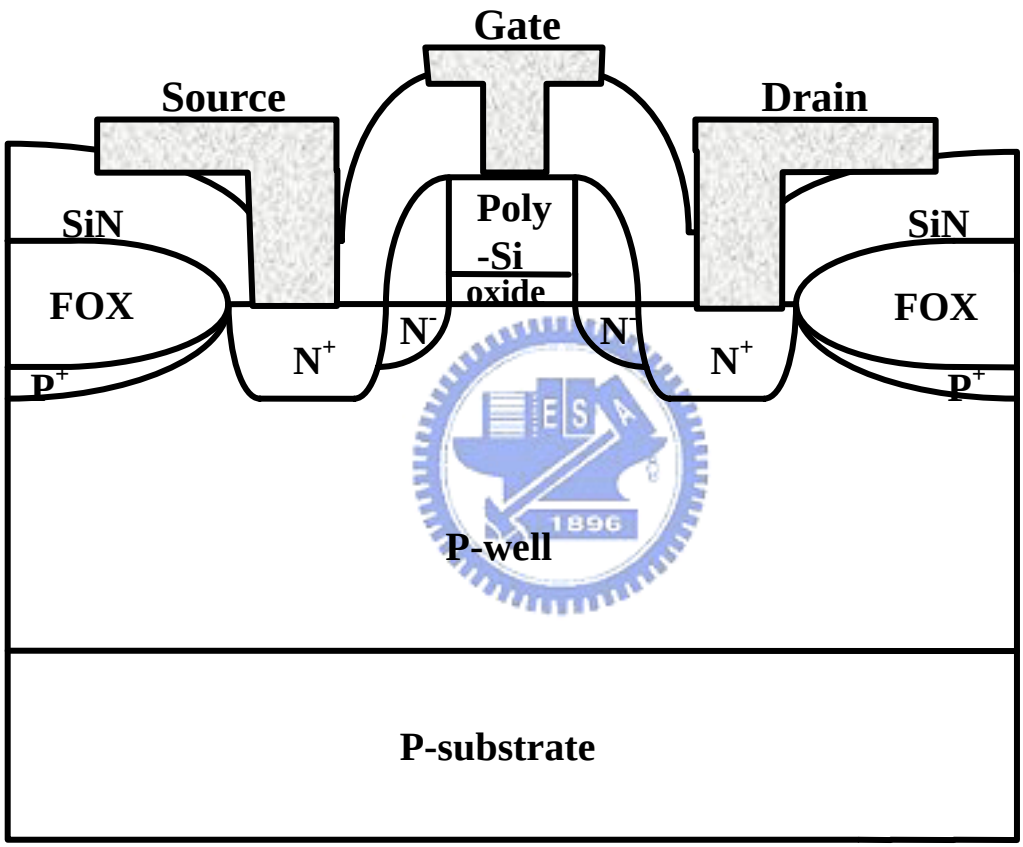


Fig 2.1 Schematic cross section of the local strained channel NMOSFET

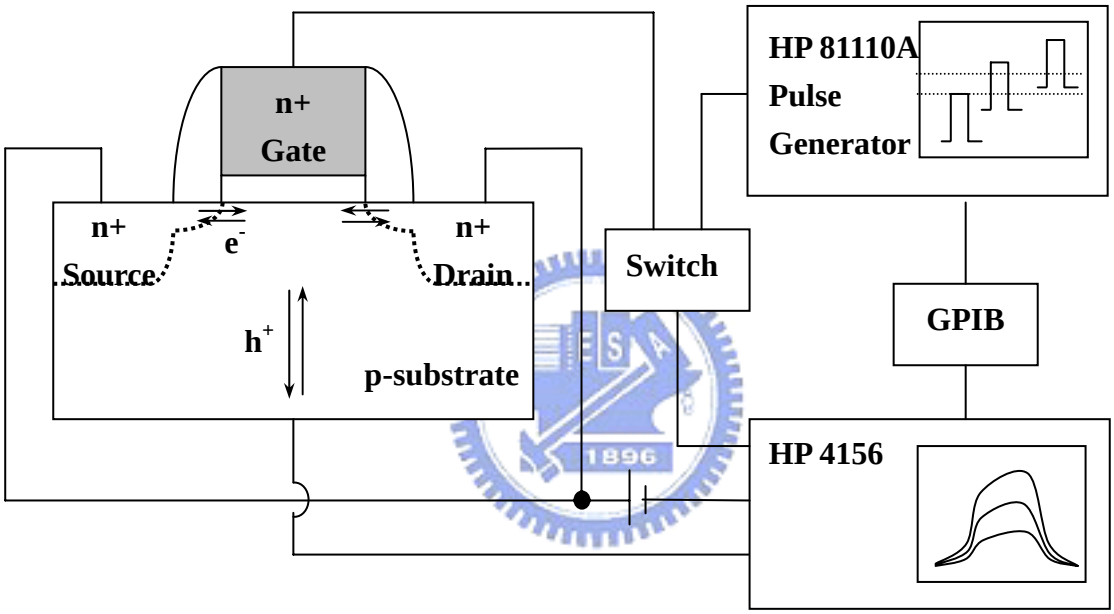


Fig . 2.2 Setup structure for charge pumping.

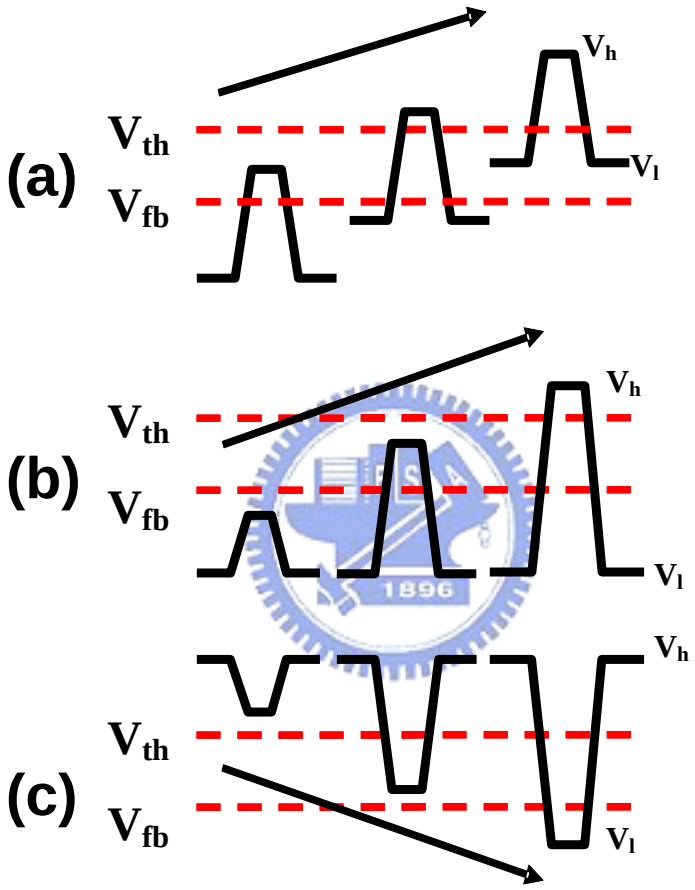


Fig.2.3 Schematic illustrations for the charge pumping measurement with (a) fixed amplitude, (b) fixed base sweep, and (c) fixed peak sweep. The arrows indicated the sweep directions.

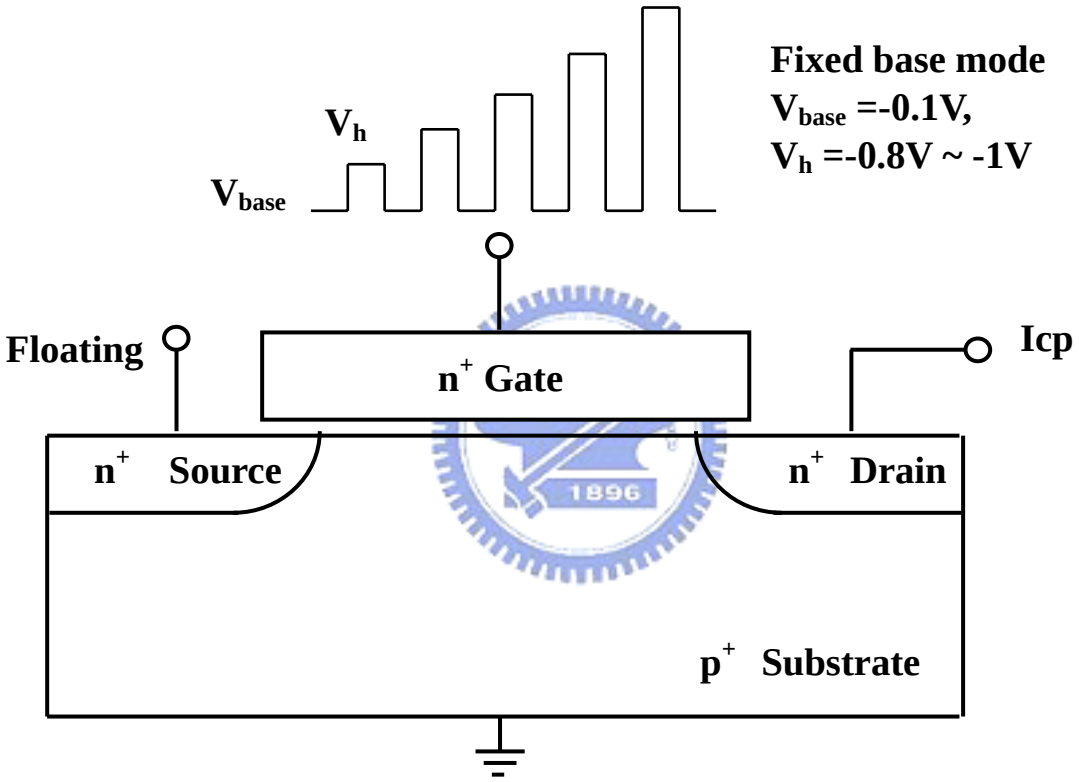


Fig. 2.4 The measurement setup of single junction charge pumping measurement

	SiH_4 (sccm)	NH_3 (sccm)	N_2 (sccm)	Stress (MPa)
SiN-1	50	6	50	99
SiN-2	50	6	100	300
SiN-3	50	6	1000	498

Table 3.1 Gas flow rate and mechanical stress for different nitride films deposited by PECVD.

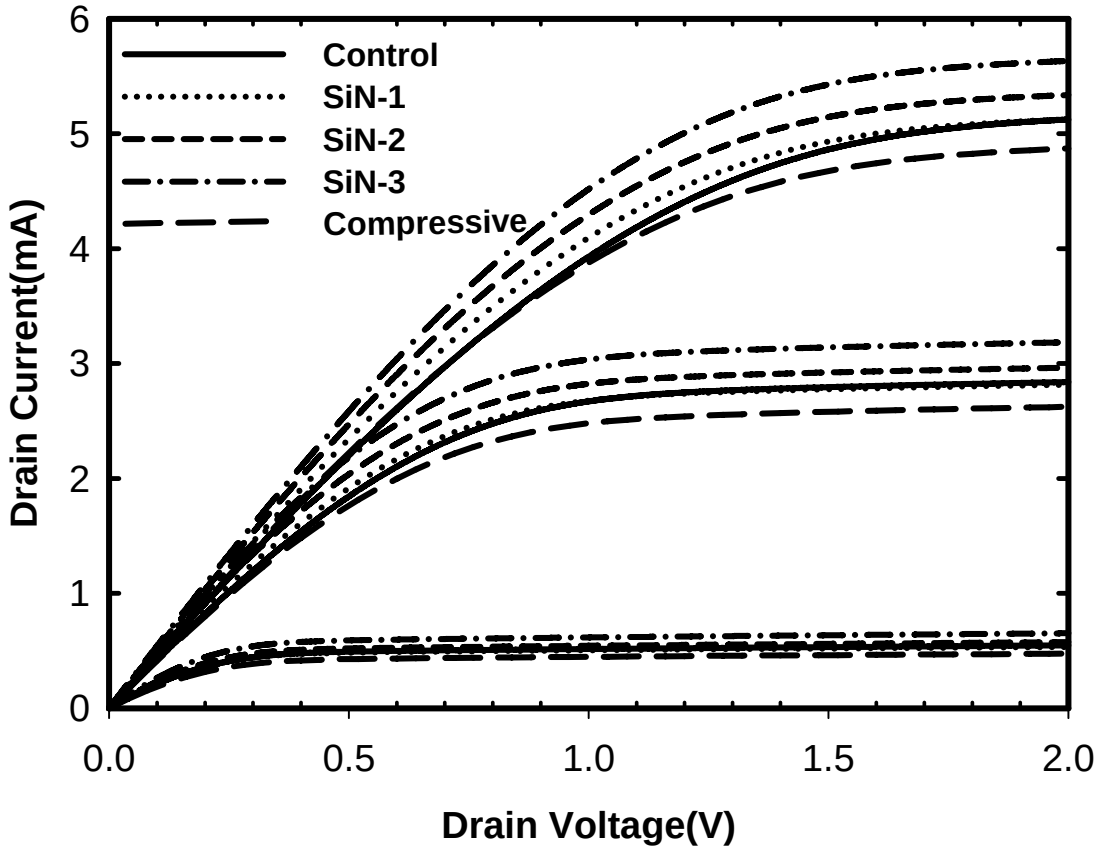


Fig.3.1 I_D-V_D Characteristics of different splits of NMOSFETs. Channel length/width = 0.5μm /10μm.

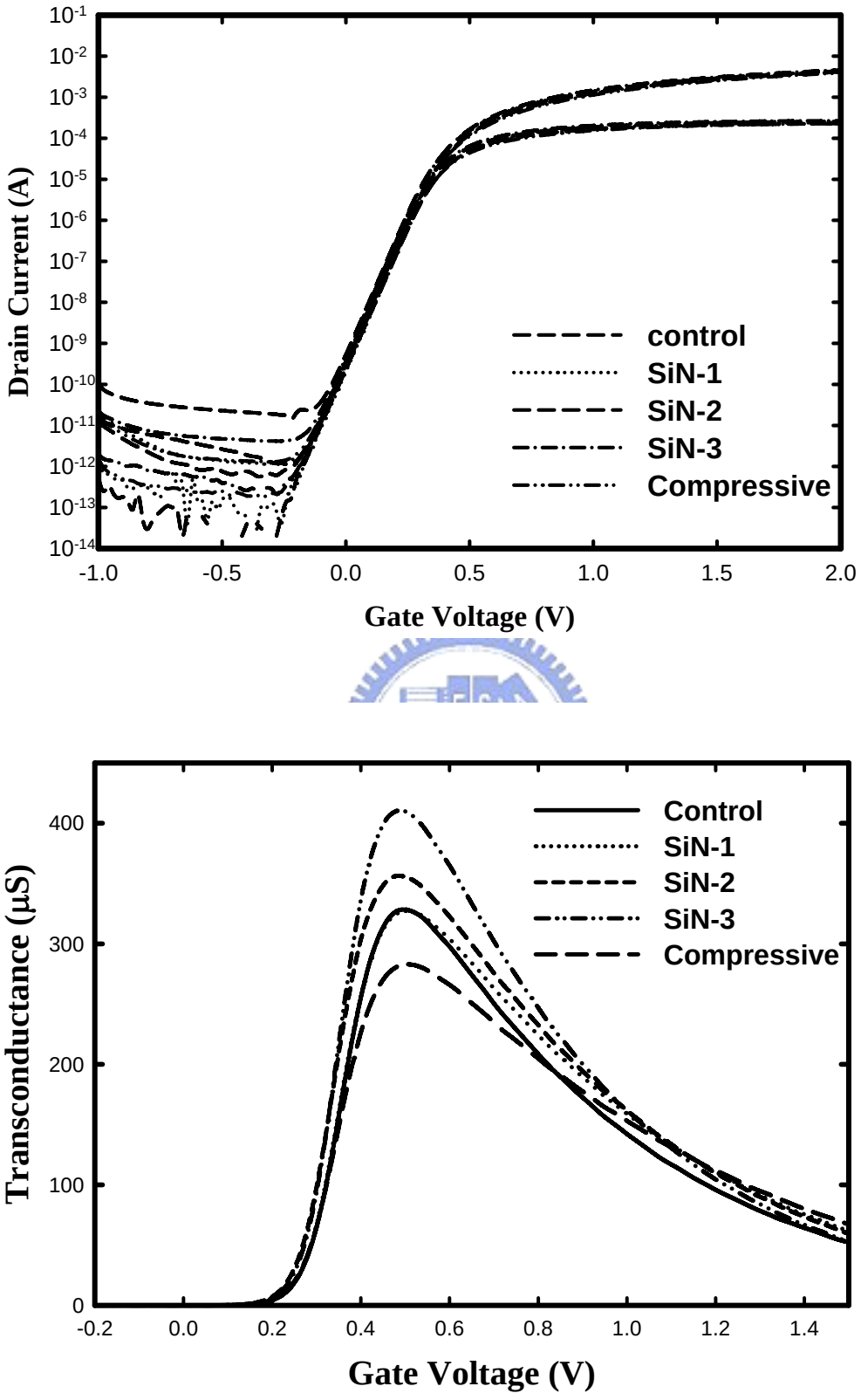


Fig.3.2 Subthreshold characteristics and transconductance of different splits of NMOSFETs. Channel length/width = 0.5μm /10μm.

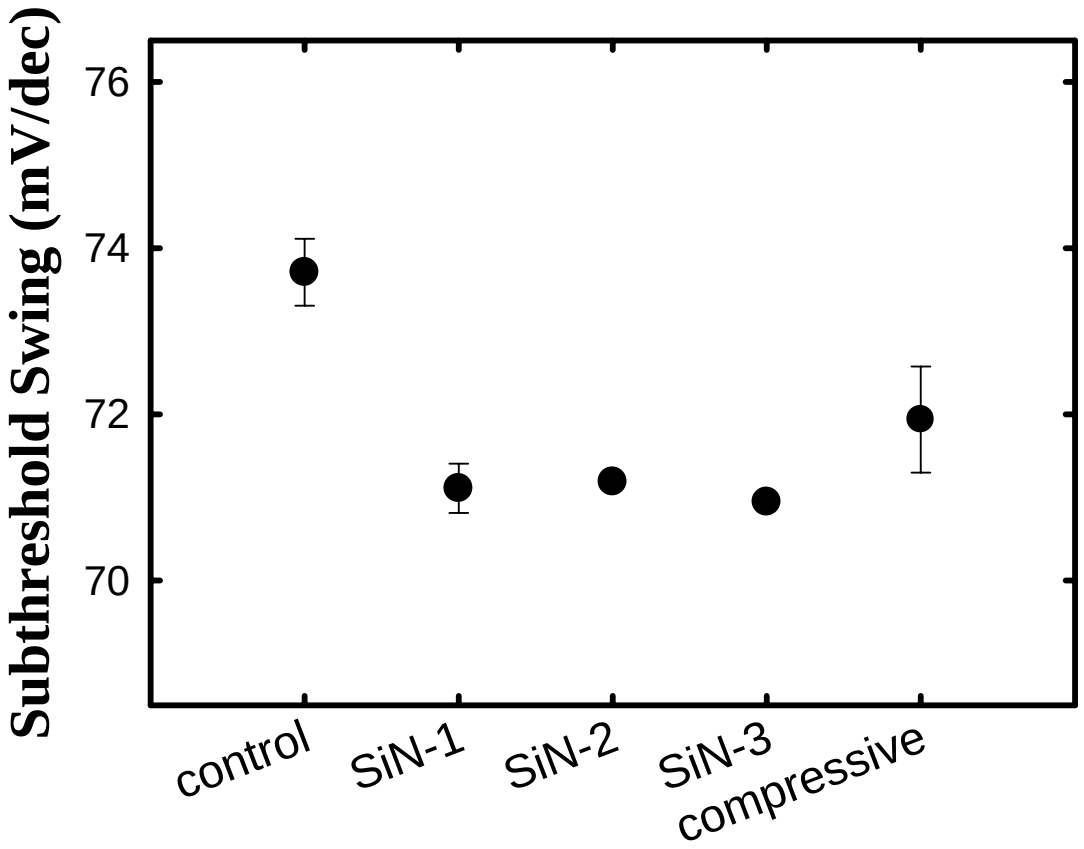


Fig. 3.3 Subthreshold swing of different splits of NMOSFETs. Channel length/width = 0.5μm /10μm.

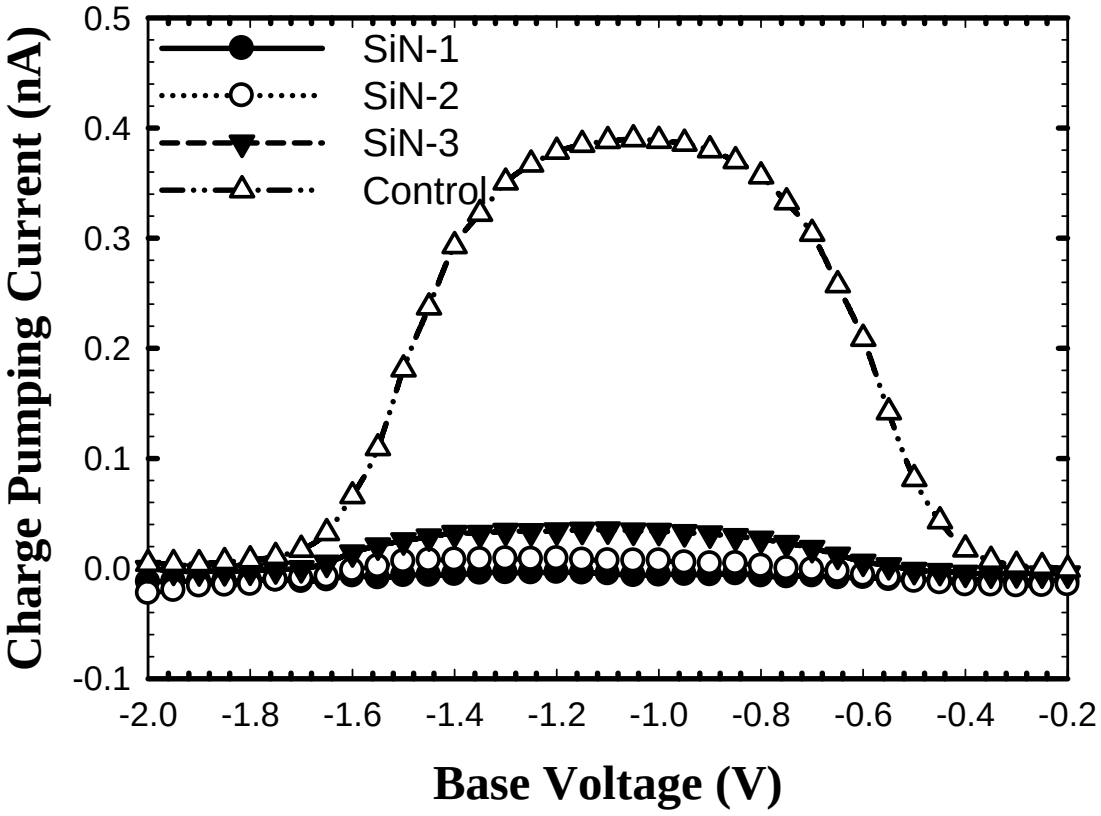


Fig. 3.4 Charge pumping current for three splits of fresh devices with channellength/width = 0.5μm/10μm. Measurement was performed under fixed amplitude of 1.5 V and frequency of 1 MHz.

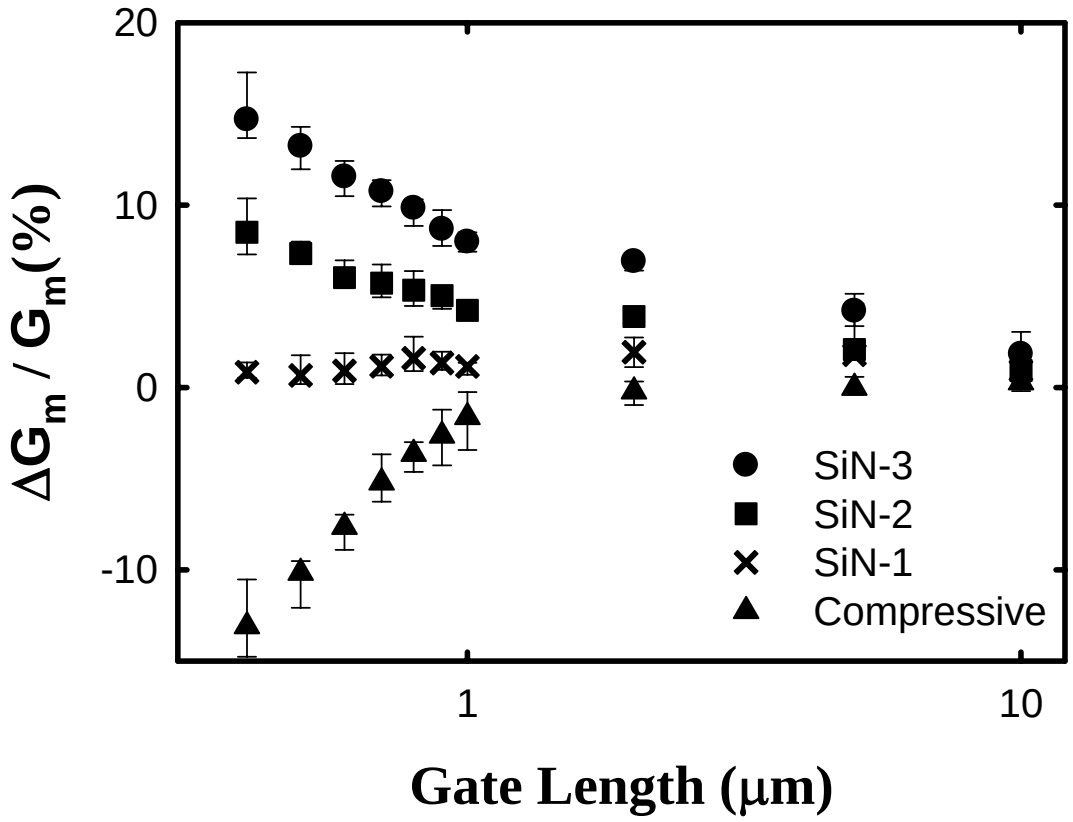


Fig. 3.5 Increase in transconductance versus channel length. The transconductance was measured at $V_G - V_{th} = -2$ V and $V_{DS} = -2$ V.

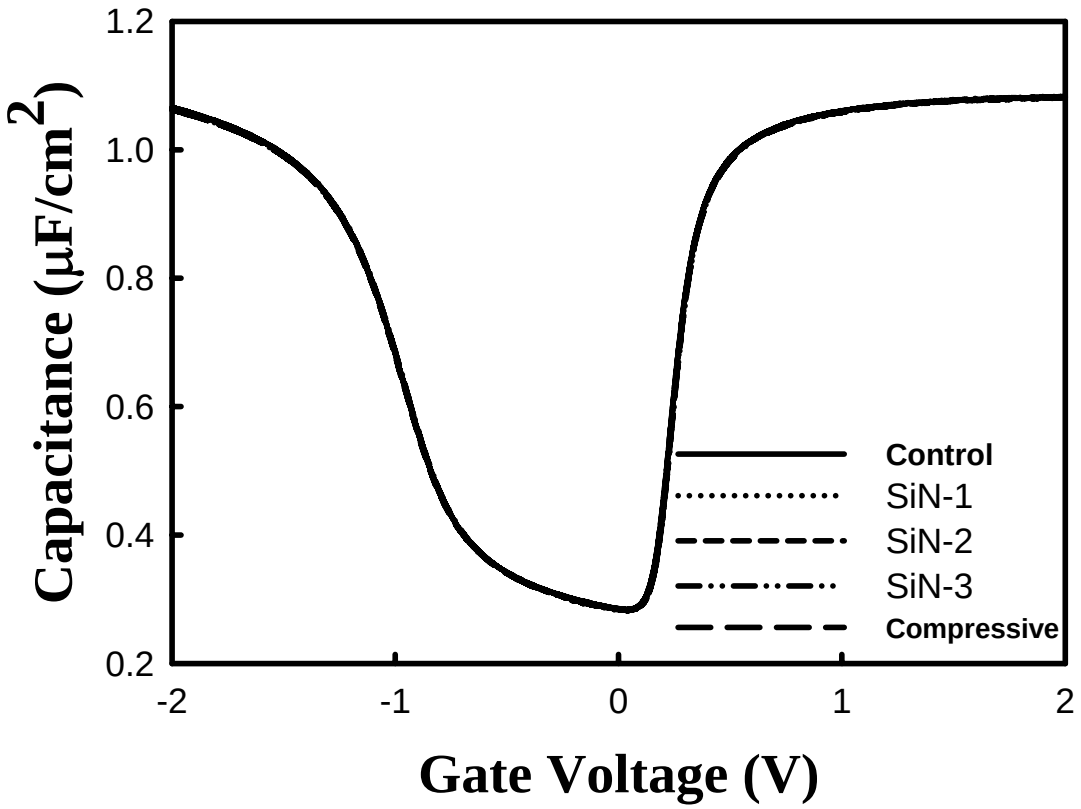


Fig. 3.6 Capacitance-Voltage (*C-V*) characteristics of different splits of NMOSFETs. Channel length/width = 50μm /50μm.

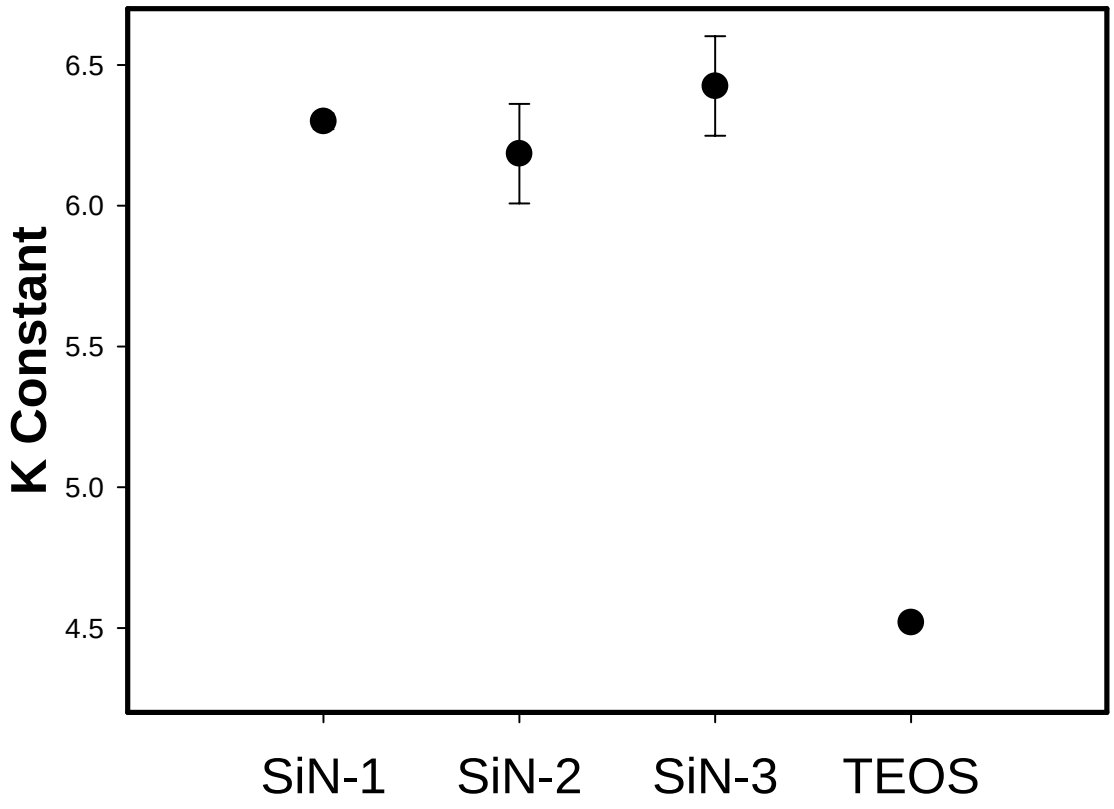


Fig. 3.7 Dielectric constant characteristics of different splits of NMOSFETs.

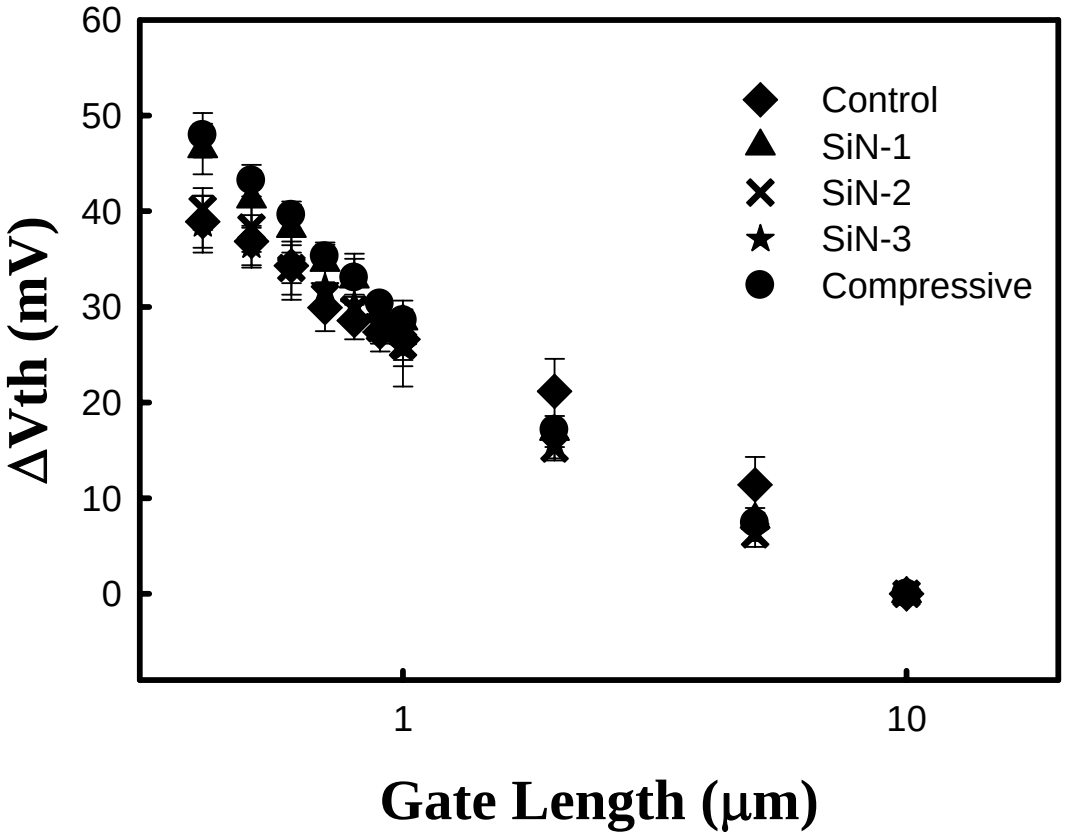


Fig. 3.8 Threshold voltage roll-off as a function of channel length for different splits of samples.

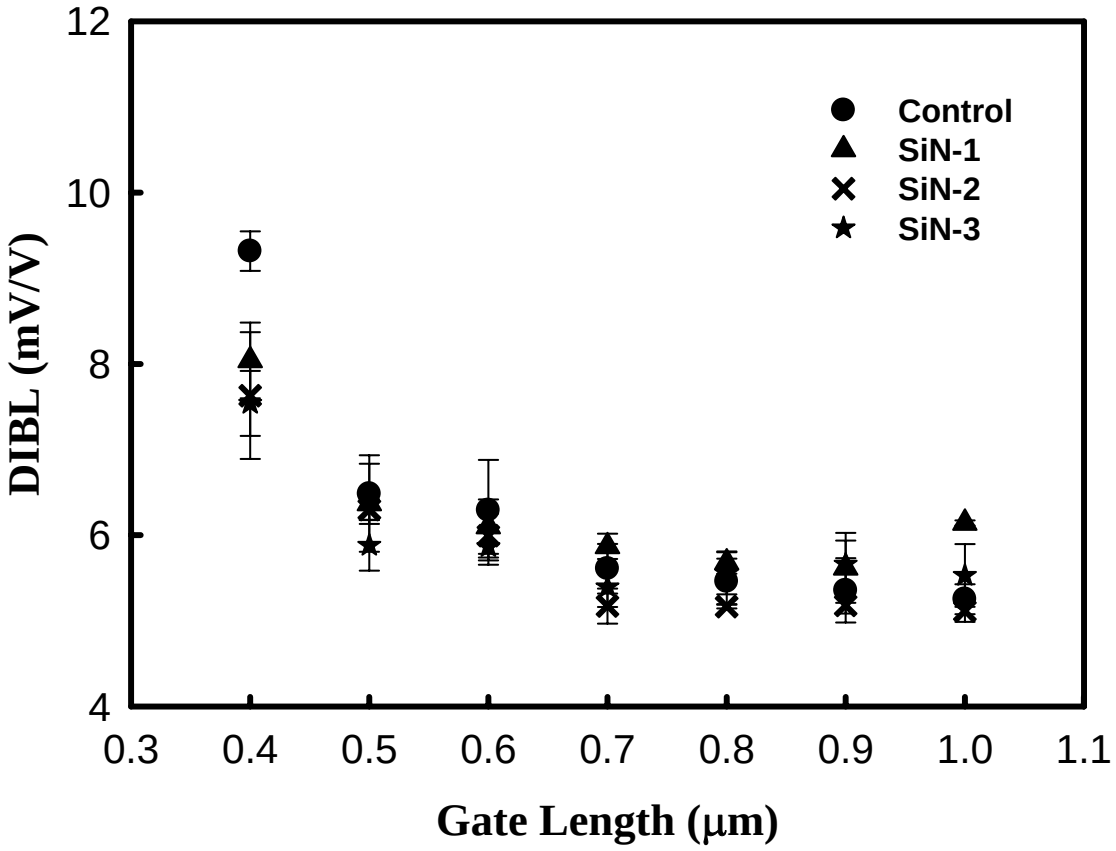
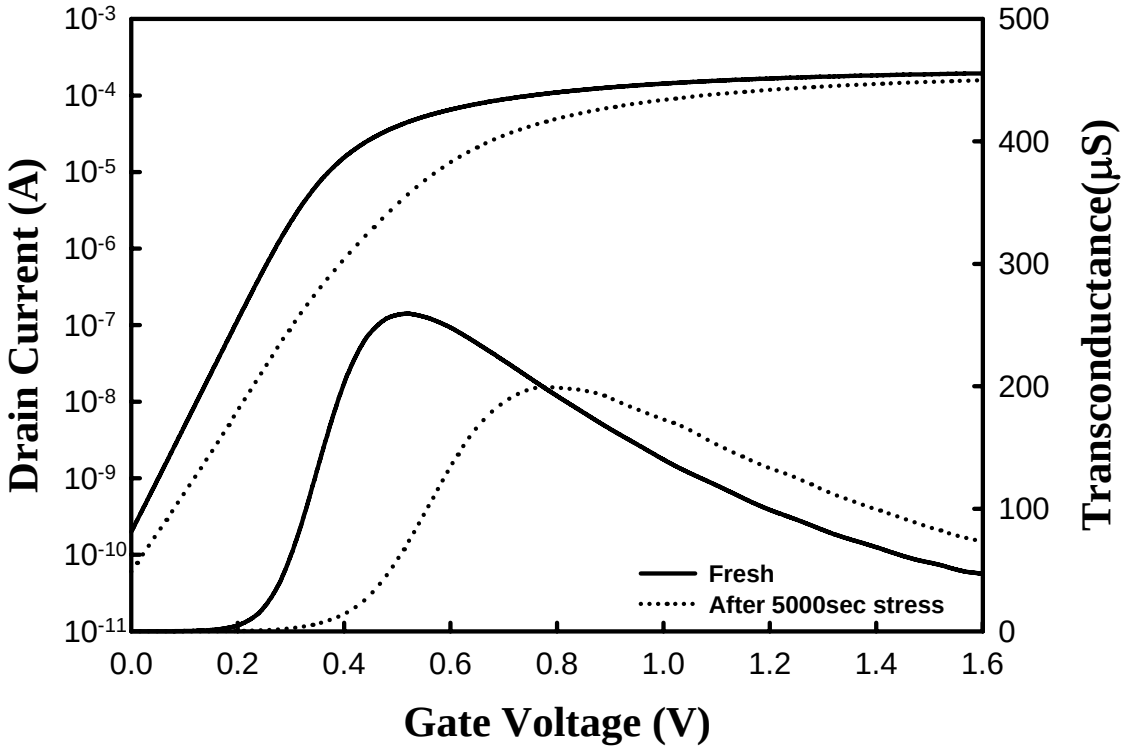
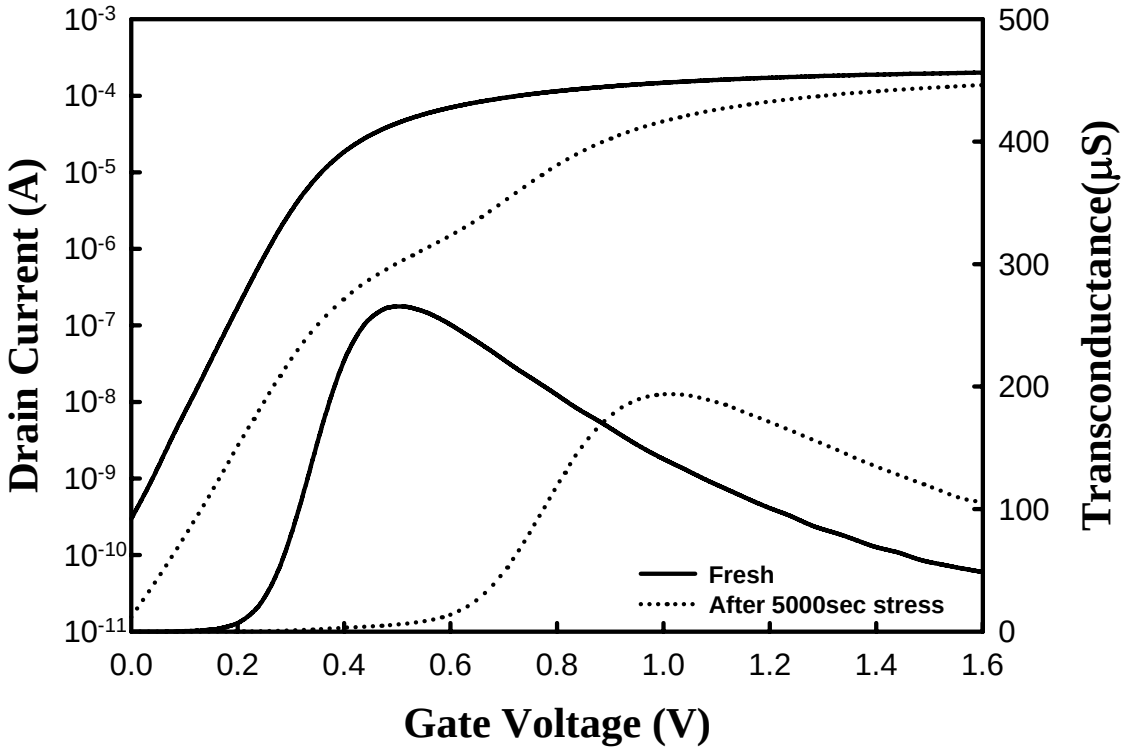


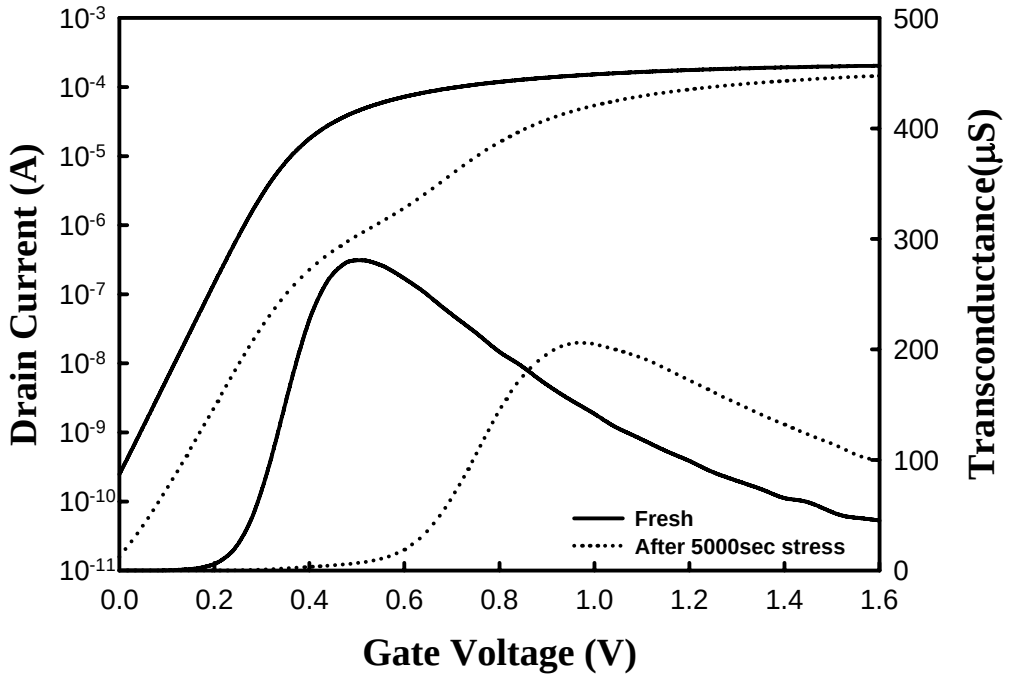
Fig. 3.9 Drain induced barrier lowing (DIBL) for different splits of NMOSFETs as a function of channel length. DIBL was evaluated by measuring the drain current change as V_{DS} was increased at some fixed gate voltage below threshold voltage.


Drain Current (A)
Transconductance(μS)
Gate Voltage (V)
Fresh
After 5000sec stress

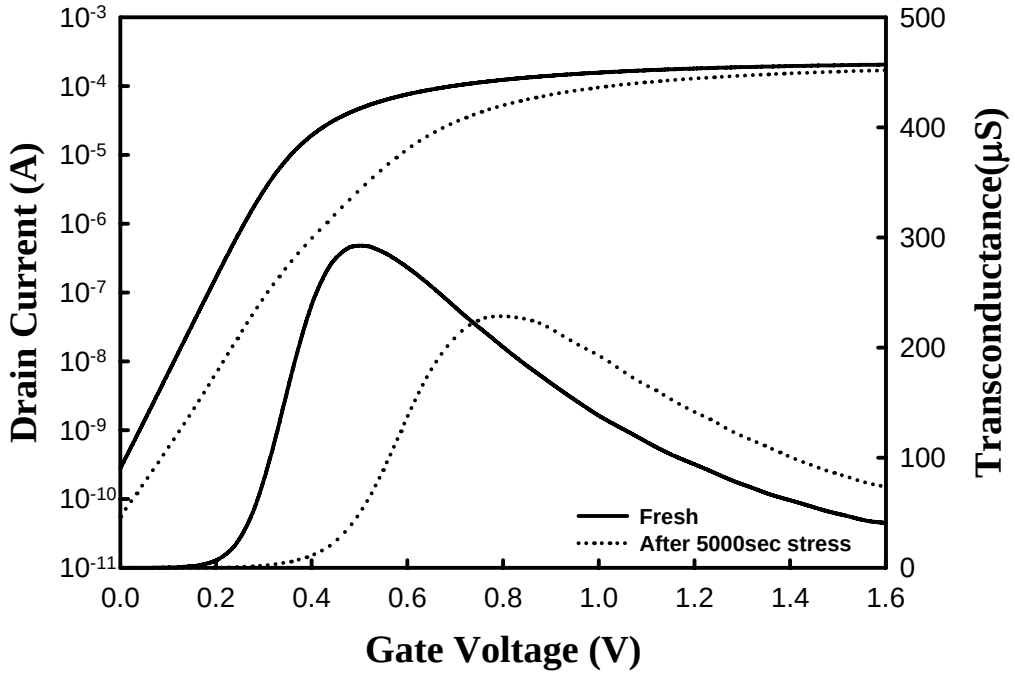
(a)


Drain Current (A)
Transconductance(μS)
Gate Voltage (V)
Fresh
After 5000sec stress

(b)



(c)



(d)

Fig. 3.10 Subthreshold characteristics and transconductance of devices before and after 5000sec hot-electron stressing. Channel length/width = 0.5μm/10μm. (a) Control sample. (b) SiN-1 Capped sample. (c) SiN-2 Capped sample (d).SiN-3 Capped sample

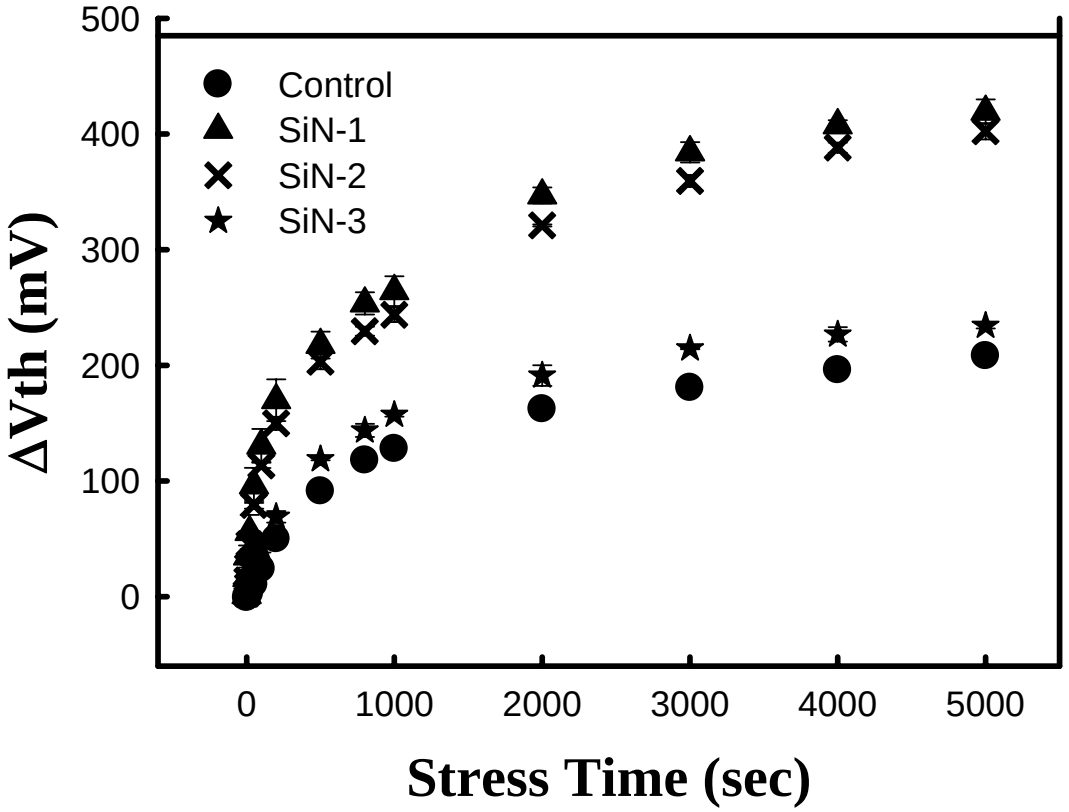


Fig. 3.11 Threshold voltage degradation of hot-electron stressing performed at V_{DS} = 4.6 V and V_{GS} at maximum substrate current on all splits of devices with channel length/width = 0.5μm/10μm.

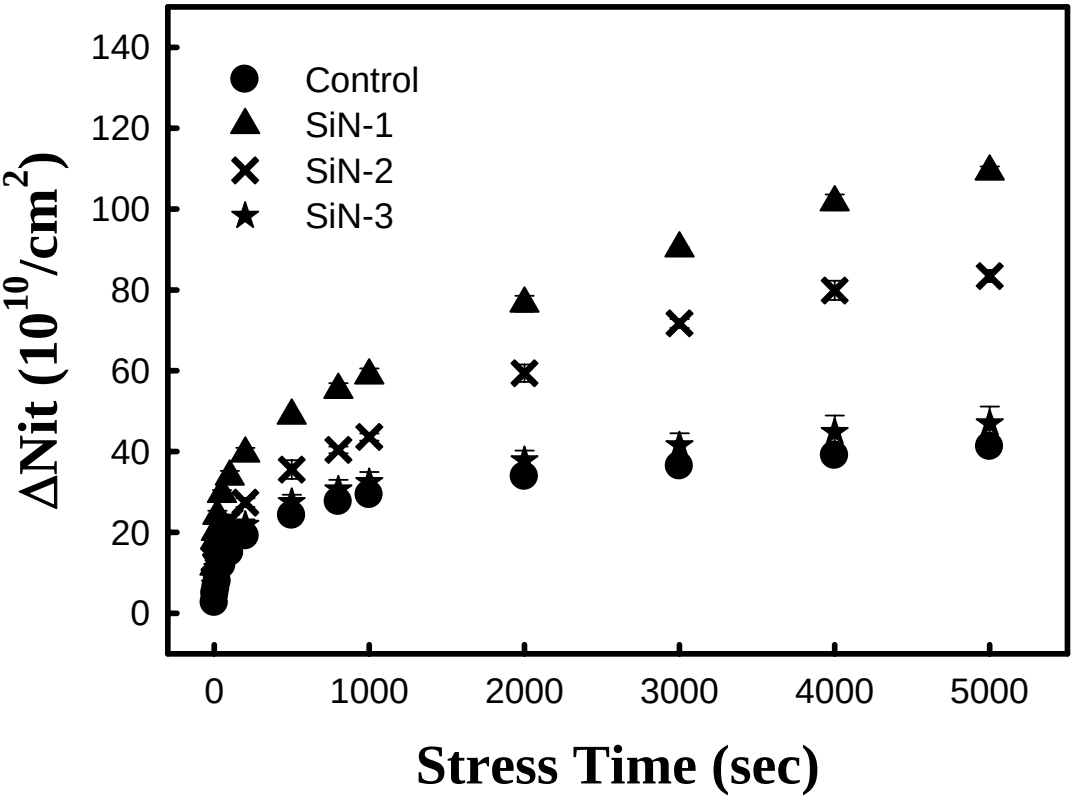


Fig. 3.12 Interface trap density degradation of hot-electron stressing performed at V_{DS} = 4.6 V and V_{GS} at maximum substrate current on all splits of devices with channel length/width = 0.5μm/10μm.

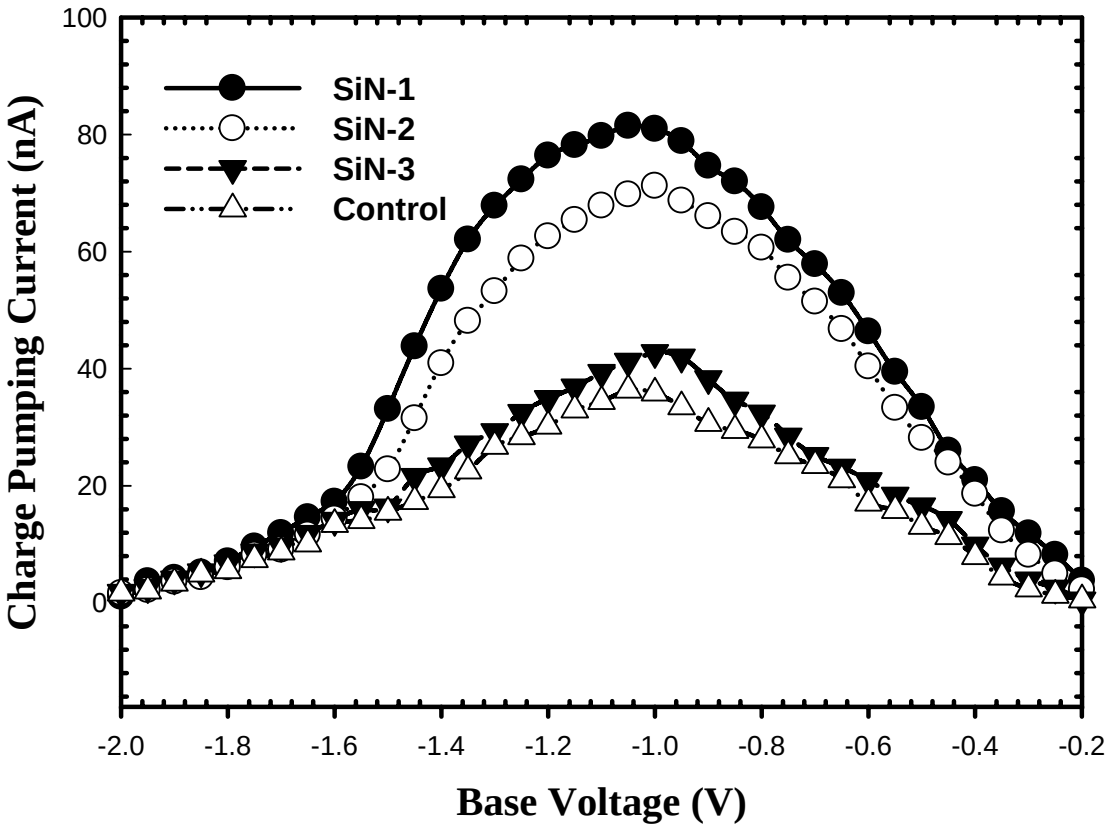


Fig. 3.13 Charge pumping current after 5000 second hot carrier stress (V_G@$Isub_{max}$ and V_{DS} = 4.6 V) for three splits of devices with channel length/width = 0.5μm/10μm.

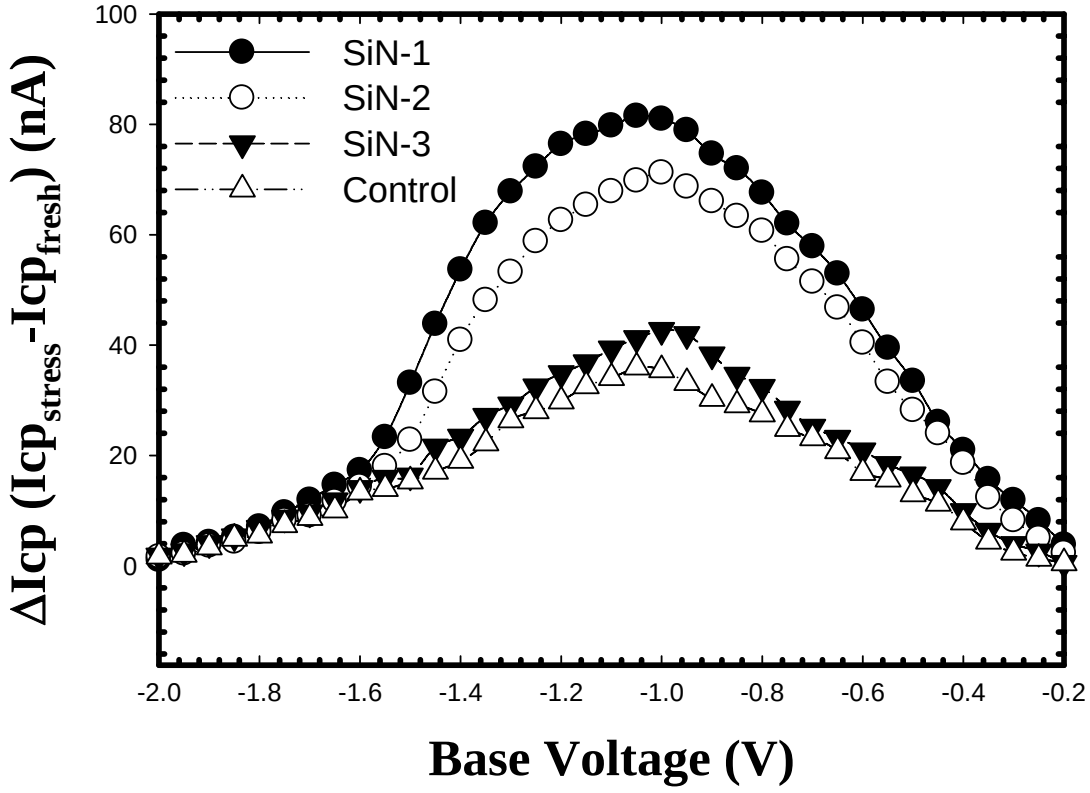


Fig. 3.14 Increase in charge pumping current after 5000 second hot carrier stress (V_G@$Isub_{max}$ and V_{DS} = 4.6 V) for three splits of devices with channel length/width = 0.5μm/10μm.

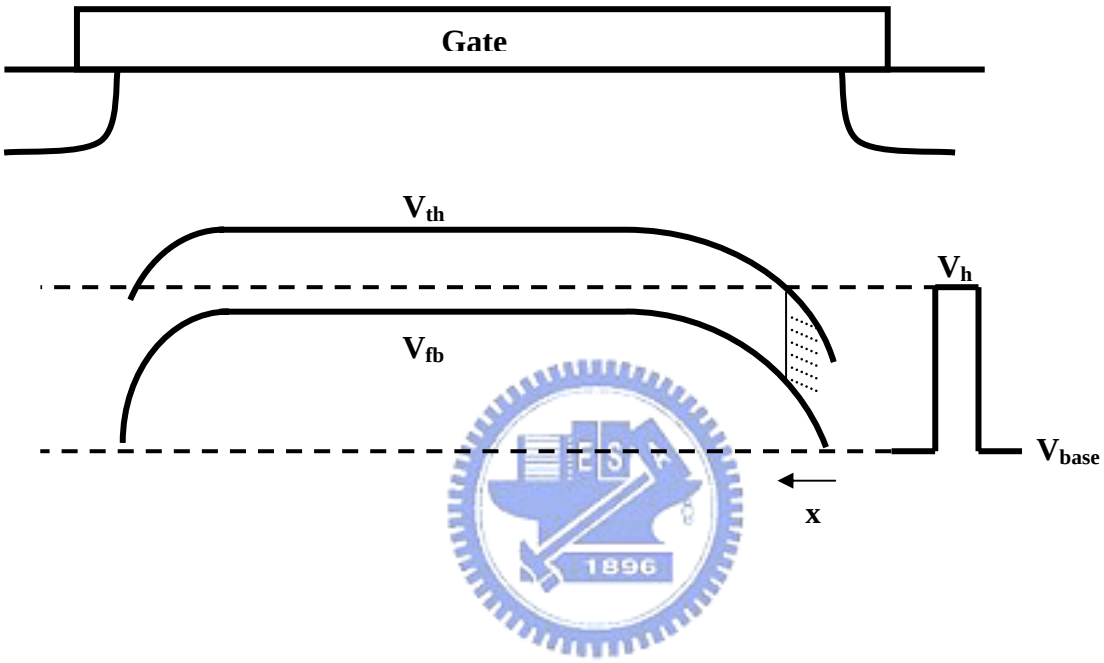


Fig. 3.15 Non-uniform distribution of local threshold voltage and flat-band voltage across the device caused by the variation of lateral doping concentration.

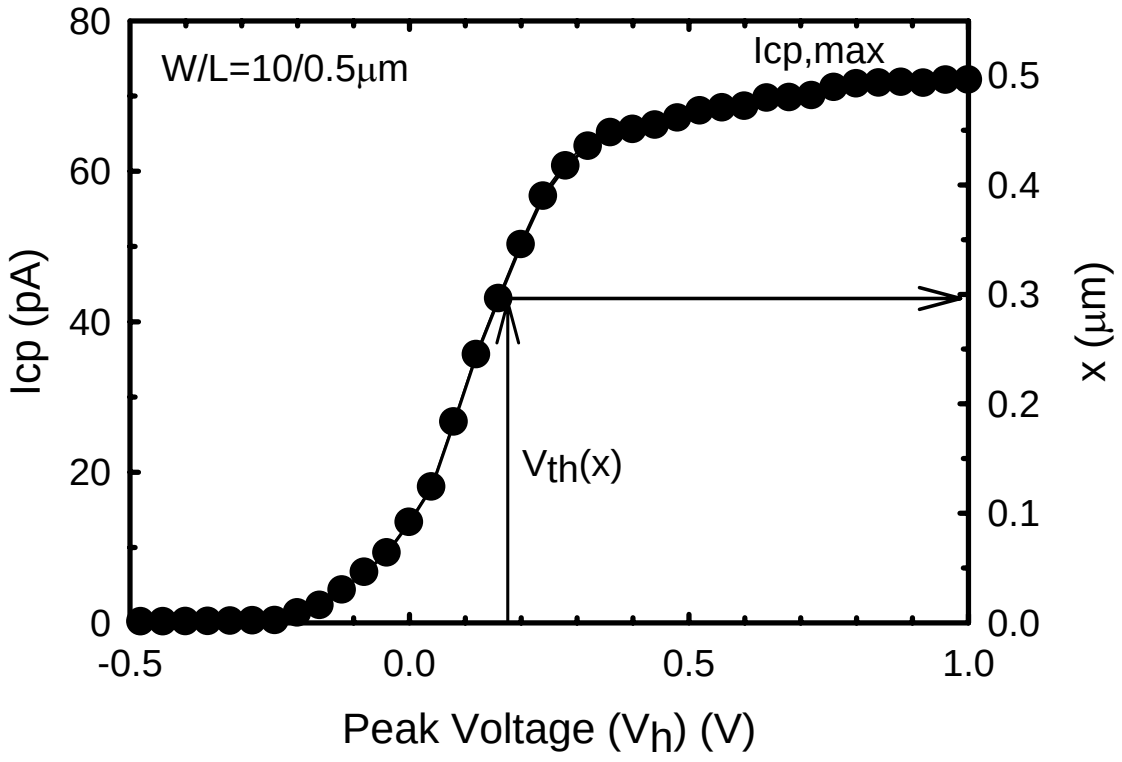


Fig. 3.16 Derivation of the relationship between local threshold voltage and lateral distance x from the single junction charge pumping data of the control device.

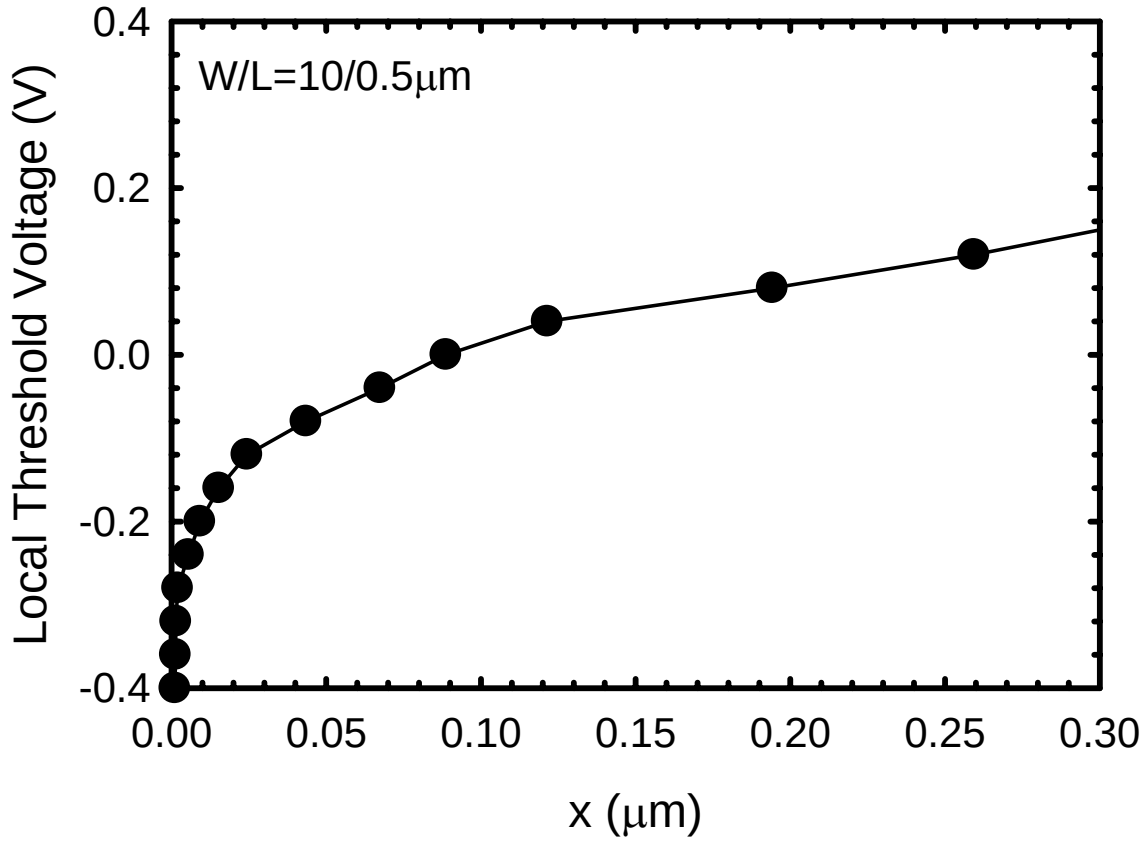


Fig. 3.17 Extracted lateral profile of local threshold voltage near the graded drain junction in the control sample.

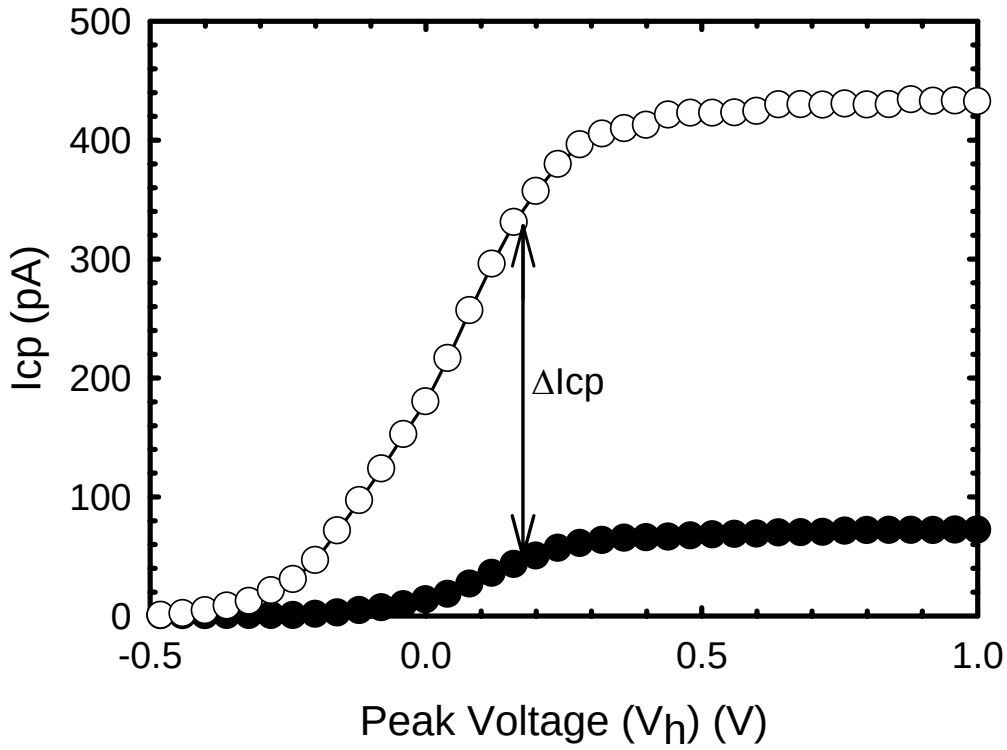


Fig. 3.18 Charge pumping current before and after 10 second hot-electron stressing (V_G@$Isub_{max}$ and V_{DS} = 4.6 V). Channel length/width = 0.5μm/10μm.

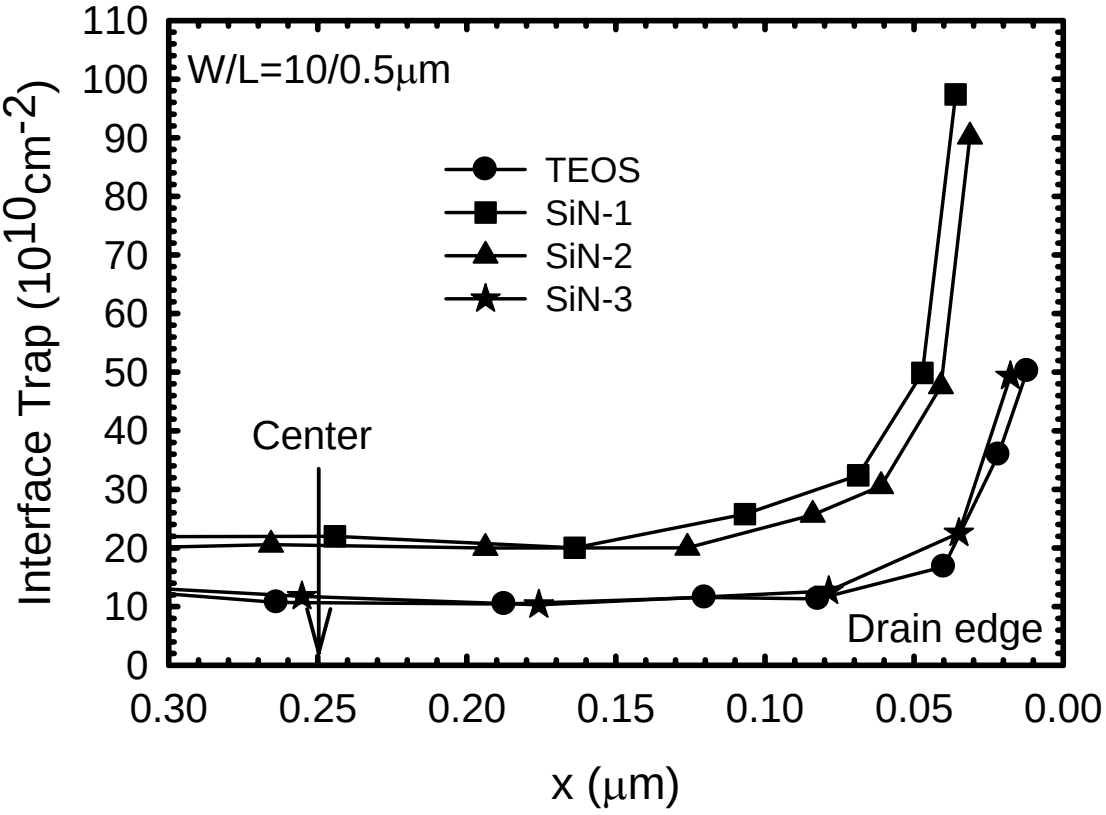


Fig. 3.19 Lateral profile of interface state generation under three different SiN capping flow rate ratio

簡歷

姓名 :詹凱翔

性別 : 男

生日 : 72.01.31

出生地 : 台北市

籍貫 : 台灣省 台北市

地址 : 北縣新店市五峰路 79 號 3F

學歷 :

台北市私立延平中學 1997.09~2001.06

國立交通大學 電子物理學系 2001.09~2005.06

國立交通大學 電子工程所 2005.09~2007.06

論文題目 :

電漿氣相輔助沉積氮化矽覆蓋層之形變 N 型金氧半場效電晶體電流增強方法與可靠度研究

A Study of Drive Current Enhancement Methods and Relability Issues of Strained NMOSFETS with PECVD SiN Capping Layer