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碩 士 論 文

二氧化鉿與氧化鋁鉿之堆疊式閘極在
金氧半場效電晶體上的特性研究

Investigation of HfO2/SiON and HfAlO/SiON gate stack on the Characteristics of MOSFETs

研 究 生：邱大峰

指導教授：葉清發　博士

羅正忠　博士

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研 究 生：邱大峰　Postgraduate：Da-Feng Chiou
指導教授：葉清發 博士　Advisor：Dr. Ching-Fa Yeh
羅正忠 博士　Dr. Jen-Chung Lou

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研 究 生：邱大峰　　　　　　　　　　　　　　指 導 教 授：葉清發 博士

羅正忠 博士

國立交通大學　電子工程學系　電子工程所

摘 要

隨著金氧半場效電晶體尺寸的微縮，傳統的閘極介電質-二氧化矽-厚度微縮到 1 到 1.5 奈米時，大量的漏電流將會從介電層直接穿遂過去，嚴重傷害到電晶體的可靠度與特性，因此利用高介電常數介電質來取代傳統的二氧化矽是勢在必行的。因為高介電常數介電質在與二氧化矽相等的等效厚度下，有較厚的實際介電層，故可以抵擋大量的直接穿遂電流。然而，在高介電常數的介電質中所產生的遷移率衰減與臨界電壓的不穩定都是其主要的存在問題。所以提昇驅動電流大小並且了解高電藉常數介電質導致的可靠度下降問題都是本研究主要的探討重點。

本論文首先探討氧化鋁鉿應用在堆疊式閘極N型金氧半場效電晶體下的特性。經由電壓-電流與電壓-電容等圖來萃取此高介常數介電質的等效厚度。另一部分，實驗中使用電漿增強式化學氣相沉積之氮化矽層，沉積在二氧化鉿與氧化鋁鉿的金氧半場效電晶體上，利用較厚的氮化矽厚度會產生較大的伸張應力現象發現N型金氧半場效電晶體之驅動電流隨著氮化矽厚度增加而增大。接著，我們

也探討，二氧化鉿高介電常數介電質材料具伸張應變通道的金氧半場效電晶體，其定電壓應力的可靠度特性分析以及偏壓變溫不穩定特性(BTI)。發現雖然較厚的氮化矽厚度可以提升N型金氧半場效電晶體的驅動電流，但定電壓應力、偏壓變溫不穩定特性卻在覆蓋較厚的氮化矽之電晶體下更為嚴重。特別是在高溫條件下，氮化矽層造成的區域應力導致較多的介面狀態產生，這可能是由於通道內的應能量造成大量矽氫鍵結斷裂。

Investigation of HfO2/SiON and HfAlO/SiON gate stack on the Characteristics of MOSFETs

Postgraduate：Da-Feng Chiou　　　　Advisors：Dr. Chin-Fa Yeh
Dr. Jen-Chung Lou

Department of Electronics Engineering & Institute of Electronics

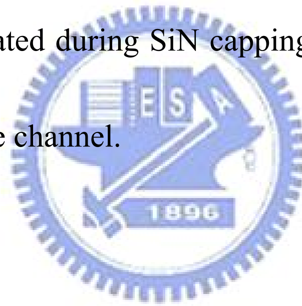
National Chiao Tung University

Abstract

As the conventional SiO_2-based gate insulator scales down to 1.0nm~1.5nm, a large direct tunneling current generates through ultra-thin oxide which cause a serious degradation in reliability and performance of device. Utilizing high-k dielectric to replace SiO_2-based gate as an insulator to eliminate high leakage current is necessary due to its larger physical thickness under the same equivalent oxide thickness. However, mobility degradation and threshold voltage instability are the mainly concern. Therefore, enhance mobility while keeping low leakage current is our aim to realize. Beside, the reliability discussion for high-k dielectric needs to be understood.

In this thesis, the electrical characteristics of HfAlO/SiON gate stack of nMOSFET is discussed first. We extract the equivalent oxide thickness of HfAlO by capacitance-voltage curve and we carried out with capping SiN layer on HfAlO/SiON and HfAlO/SiON gate stack. The SiN film deposited by PECVD is used to induce

tensile strain locally in the channel region. Driving currents on nMOSFETs devices are enhanced as the thickness of SiN layer increases due to increasing tensile strain in the channel region. Constant voltage stress (CVS) and bias temperature (BTI) characteristics of nMOSFET with tensile strain in the channel region are also discussed. We can find that the nMOSFETs devices with thicken SiN capping layer enhances drive current, the reliability concerns on CVS and BTI become huger when thicken SiN capping layer deposited. More interface states are generated in high CVS of nMOSFET with thicken SiN capping layer. This expresses that a higher amount of hydrogen incorporated during SiN capping layer deposition as well as the high strain energy stored in the channel.



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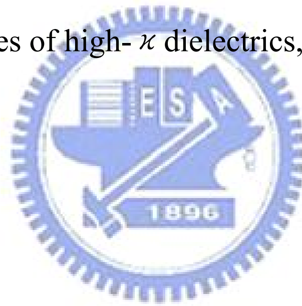

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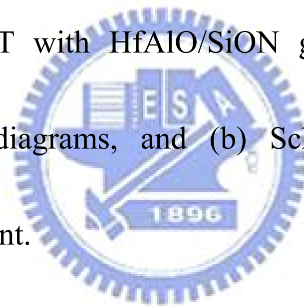

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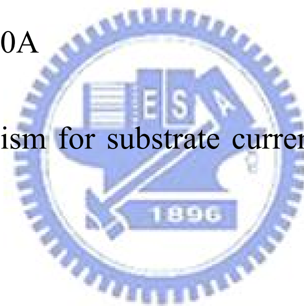

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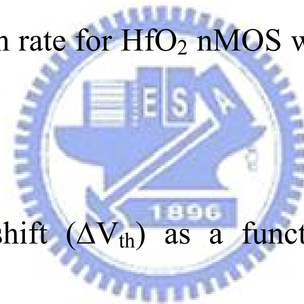

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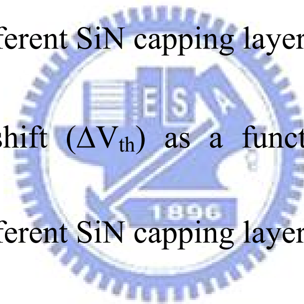


Chapter 1
Introduction

1.1 Backgrounds and Motivation

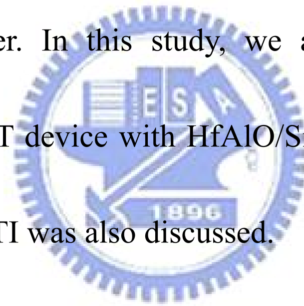
According to the international technology roadmap of semiconductor (ITRS) (Table 1-1), the metal oxide semiconductor field effect transistors (MOSFET) of high density integration circuit and high performance, device geometry such as channel length and thickness of gate dielectric would be reduced. However, as the conventional gate dielectric scales down to 1.0nm~1.5nm, the viability of SiO_2 will face several challenges like a large leakage current occurs through the ultra-thin oxide by direct tunneling mechanism [1]. This phenomenon increases standby power consumption and loss of inversion charge which degrade the reliability and performance of device seriously. In order to suppress the leakage current and maintain excellent performance of device, replace the conventional SiO_2-based dielectric by high-k dielectric as a gate insulator is necessary. High-k dielectric can efficiently reduce direct tunneling current through the oxide efficiently due to its high dielectric constant. At same equivalent oxide thickness (EOT) high-k dielectric has thicker physical thickness. Therefore, high-k dielectric is being pursued as possible

replacement for SiO_2.

Several high-k dielectrics are investigated in the literature, among these high-k dielectrics, Hafnium oxide (HfO_2) is the most promising candidate due to its high permittivity (k ~ 20 for HfO_2) as compared to Al_2O_3 and Si_3N_4 , high thermodynamic stability on silicon (47.6Kcal/mol at 727℃) as compared to TiO_2 and Ta_2O_5 and its relatively high band gap (~5.8ev) among its high-k contender, appropriate barrier height for both electrons and holes (>1ev), and compatible with poly-silicon gate process. However, Hafnium oxide also has some challenge such as trapping in the bulk dielectric and interfacial layer between high-k and Si-sub which cause mobility degradation and threshold voltage instability especially in its quite low crystallize temperature (< 500 ℃) [2-5], which restricts to the thermal budget after the post deposition anneal (PDA) and brings about the leakage current and non-uniformity associated with grain boundaries. By contrast, Al_2O_3 dielectric is an extremely promising selection on terms of its chemical, thermal stability as well as its high barrier offset and band gap (barrier height of electron and hole are 2.9ev and 4.3ev, band gap about 8.3ev) (Table1-2). In order to gain high dielectric constant and thermal stability, we avoid the low crystallize temperature by adding Al to HfO_2. It can be seen that the crystallize temperature increase between 500 and 600 ℃ for 6.8% Al containing , which is about 200℃ higher than without Al. If the Al concentration

is increased further to about 31.7%, the depending crystallize temperature will increase between 800 ~ 900 ℃, which is about 400 ℃ higher than HfO_2 without Al [5].

Besides, enhanced turn-on current by tensile stress in nMOSFET is investigated. [6] The uniaxial strain was induced by depositing SiN capping layer on HfO2/SiON and HfAlO/SiON gate stack nMOSFET device and the magnitude of driving current is proportion to the thickness of SiN capping layer. However, the reliability concern such as negative bias temperature instability (NBTI) becomes worsened as compared to thinner SiN capping layer. In this study, we analyses the characteristic and performance of the nMOSFET device with HfAlO/SiON gate stacking structure, the reliability concerns such as BTI was also discussed.



1.2 Organization of This Thesis

In this thesis, we discuss methodically the HfO2/SiON and HfAlO/SiON gate stacking structure in terms of five chapters.

In chapter 1, we show the background and motivation respectively and the characteristics of high-k dielectric.

In chapter 2, we explain the process flow of MOSFET device about the HfO2/SiON and HfAlO/SiON gate stacking structure and illustrate the method of measurement techniques.

In chapter 3, after measurement we show some basic electrical characteristics about HfAlO with different thickness of SiN capping layer such as Id-Vg, Id-Vd, C-V, charge pumping…etc. By these data we can verify what type interfacial layer is and use carrier separation to obtain leakage current mechanism.

In chapter 4, we discuss the reliability issues with device that utilized HfO2/SiON dielectric. BTI (bias temperature instability) is also an important part of reliability issues.

In chapter 5, we summarize the important issues of this study. Some recommendations for future works are investigated.

Year of Production	2006	2007	2008	2009	2010	2011	2012
EOT(physical) for high-performance(nm)	1.1	1.1	1.0	1.0	0.9	0.65	0.9
Electrical thickness adjustment for gate depletion and inversion layer effects (nm)	0.74	0.74	0.7	0.7	0.7	0.27	0.25
Normal gate leakage current density linit(at 25oC)(A/cm2)	536	800	800	1180	1100	1560	2000

Table 1-1 2006 International Technology Roadmap of Semiconductor (ITRS)

	High-κ Dielectrics		
	Al_2O_3	ZrO_2	HfO_2
Bandgap (eV)	8.3	5.82	6.02
Barrier Height to Si (eV)	2.9	1.5	1.6
Dielectric Constant	9	~ 25	~ 25
Heat of Formation (Kcal/mol)	399	261.9	271
ΔG for Reduction (MO_x + Si → M + SiO_x)	63.4	42.3	47.6
Thermal expansion coefficient (10^{-6} $^oK^{-1}$)	6.7	7.01	5.3
Lattice Constant (Å) (5.43 Å for Si)	4.7- 5.2	5.1	5.11

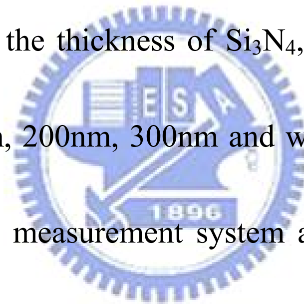
Table 1-2 Materials properties of high-κ dielectrics, Al_2O_3, ZrO_2 and HfO_2.

Chapter 2
Device fabrication and Measurement Setup

2.1 Experimental Details

In this section, we expound the process flow of the nMOSFET device fabrication systematically. Local oxidation of silicon (LOCOS) was applied for device isolation. The nMOSFET devices were fabricated on 6-inch p-type (100) Si wafer by conventional integration process. After LOCOS formation, before dielectric deposited, we dipped the dilute-HF about seven minutes to eliminate the native oxide that on the active area, then we avoided the contamination of organic element, particle and metal ion by standard RCA clean. At once, a thin interfacial layer of SiON was formed by oxide rapid thermal anneal (RTA) at 800℃ in N_2O ambient with 30 seconds and it was measured approximate 0.7 nm by ellipsometer analysis. This film can alleviate the interfacial layer growth and prevent the leakage current through the dielectric. And then the 30nms HfO_2 and HfAlO films were deposited by atomic layer deposition (ALD) immediately. In order to improve the dielectric film quality, following RTA at 600℃ for $Hf0_2$ and 700℃ for HfAlO with 20 seconds in N_2 ambient is necessary. A 200nm poly-silicon was deposited on the dielectric by low pressure chemical vapor deposition (LPCVD) then the gate electrode

was defined by I-line stepper after I-line PR coating and etched by electron cyclotron resonance etcher (ECR). After removing sidewall polymer by SC-1 (NH_4OH:H_2O_2:H_2O=1:1:5), S/D extension implant was done in order to avoid the hot carrier effect in the channel. A 200nm spacer formation was carried out by plasma enhance chemical vapor deposition (PECVD) then etched by TEL5000 system. Subsequently, S/D implantation was finished. Then definition and implantation of body region was achieved respectively. Afterwards, the stress induced by Si_3N_4/SiO2 capping layer was deposited by PECVD. In order to verify the relation between the stress effect and the thickness of Si_3N_4, we divided the Si_3N_4 thickness into four parts such as 100nm, 200nm, 300nm and without Si_3N_4. We obtained the magnitude of stress by stress measurement system and it showed 184.3 Mpa a for 100nm, 226.9 Mpa for 200nm and 432Mpa for 300nm. In some studies, we know that the stress magnitude is relative to the concentration of nitrogen in Si_3N_4 deposition. Final, Al-Si-Cu metallization were implemented by physical vapor deposition (PVD) system. After metal etching, forming gas annealing at 400℃ in H2/N2 ambient for 30 minutes was used to fix dangling bond and reduces interfacial state density. We show the process flow and the cross section of nMOSFET device in Fig 2-1 and Fig 2-2 respectively.



2.2 Measurement setup

Some basic electrical characteristics of the nMOSFET device such as current-to-voltage and capacitance-to-voltage were extracted by Agilent 4156C precision semiconductor parameter and HP 4284 LCR meter respectively.

First, we can obtain the equivalent oxide thickness of the HfAlO and HfO_2 dielectric MOSFET device from the capacitance in inversion region of C-V profile without considering quantum effect. The equation is

$$C_{inversion} = \frac{\varepsilon_{oxide} A}{EOT} \qquad (2\text{-}1)$$

whereas ε, A are permittivity and device area respectively. In addition, the interface state density (N_{it}) was measured by charge pumping method [7]. A series of continuous square waveforms (f = 1 MHz) were generated and applied to gate by 8110 pulse generator while source, drain and body were grounded. Besides, we fix the magnitude of the square waveforms at 1.5V and the base voltage was varied from accumulation to inversion. After measurement, we gained a list of the charge pumping current (I_{cp}) data and calculated the N_{it} from the equation

$$I_{cp} = q f N_{it} A \qquad (2\text{-}2)$$

whereas q, A and f are electron charge, the area of device and frequency of pulse respectively. Fig 2-3 shows the configuration of charge pumping measurement setup. Besides, total trap density ($\triangle N_{tot}$) include of the interfacial trap and bulk trap was

calculated form threshold voltage shift (△V_{th}) by assuming that the charge was trapped at the interface between the dielectric and Si substrate. The equation is

$$\Delta N_{tot} = \frac{C\Delta V_{th}}{qA} \tag{2-3}$$

therefore, we can obtain the ΔN_{ot} (oxide trap or bulk trap) from (2-2) and (2-3) by following equation

$$\Delta N_{ot} = \Delta N_{tot} - \Delta N_{it} \tag{2-4}$$

However, by measuring the charge pumping current (I_{cp}) wuth variable fall and rise times, we can obtain the energy distribution of the interface states in a relatively huge part of the forbidden energy gap on both sides of midgap [8-9]. Interface states act as acceptor-like or donor-like which depend on their relative state to the band gap. Donor-like interface states are neutral when they are empty or negative when occupied by electron. In contrast, acceptor-like states are positive when they are empty or neutral when occupied by electron. Relative position depends on its Fermi level and an interface trap will be occupied by an electron or empty. Simultaneously, we listed some useful equations for analyzing whether acceptor-like or donor-like interface states.

$$\frac{I_{cp}}{f} = 2qD_{it}AkT\left[\ln\sqrt{t_r t_f} + \ln\left(\frac{|V_{fb} - V_t|}{|V_a|}V_{th}n_i\sqrt{\sigma_n\sigma_p}\right)\right] \tag{2-5}$$

$$E_{em,e} - E_i = -kT \ln\left(V_{th} n_i \sigma_n \frac{\left|V_{fb} - V_{th}\right|}{\left|V_a\right|} t_f + e^{\frac{\left(E_i - E_{f,inv}\right)}{kT}} \right) \quad (2\text{-}6)$$

$$E_{em,h} - E_i = +kT \ln\left(V_{th} n_i \sigma_p \frac{\left|V_{fb} - V_{th}\right|}{\left|V_a\right|} t_r + e^{\frac{\left(-E_i - E_{f,acc}\right)}{kT}} \right) \quad (2\text{-}7)$$

$$N_{it}\left(E_2\right) = -\frac{t_f}{qATf} \frac{dI_{cp}}{dt_f} \qquad (t_r \text{ constant}) \quad (2\text{-}8)$$

$$N_{it}\left(E_1\right) = -\frac{t_r}{qATf} \frac{dI_{cp}}{dt_r} \qquad (t_r \text{ constant}) \quad (2\text{-}9)$$

If we gained the result that $N_{it}(E_2)$ was an extensive variation and $N_{it}(E_1)$ was almost similar according to equation (2-5), (2-6) and (2-8), we could observe that it existed strong fall time dependence of charge pumping curve for fixed rise time. It shows that acceptor-like interface states exist because huge interface state variation is near conduction band. Similarly, $N_{it}(E_1)$ was a large variation and $N_{it}(E_2)$ was almost similar according to (2-5), (2-7) and (2-9), it means that it existed strong rise time dependence of charge pumping curve for fixed fall time and donor-like interface states exist because large interface variation is near valence band.

The electron mobility of nMOSFET was measured by split C-V method. The effective mobility of electron was measured at low drain bias and then gave

$$\mu_{eff} = \frac{g_d L}{W Q_n} \quad (2\text{-}10)$$

Where the Q_n was measured from capacitance measurement and drain conductance g_d was defined as

$$g_d = \frac{\partial I_D}{\partial V_{DS}} \bigg|_{V_{GS} = \text{constant}} \quad (2\text{-}11)$$

The capacitance meter was connected between the gate and the source/drain were connected together with the substrate grounded. Therefore, Q_n was observed as follows

$$Q_n = \int_{-\infty}^{V_{GS}} C_{gs} dV_g \qquad (2\text{-}12)$$

And effective electric field produced by the voltage was express as

$$E_{eff} = \frac{Q_b + \eta Q_n}{K_s \varepsilon_0} \qquad (2\text{-}13)$$

Qb was measured from capacitance measurements. The capacitance meter was connected between the gate and substrate and the source/drain were connected grounded together. Therefore,

$$Q_b = \int_{fb}^{V_{GS}} C_{gb} dV_g \qquad (2\text{-}14)$$

where Q_n and Q_b were charge densities in depletion layer and inversion layer respectively. The parameter η = 1/2 was for electron. And subsequently universal mobility was accomplished by this equation

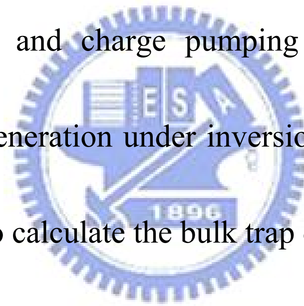
$$\mu_{eff} = \frac{638}{1 + \left(\frac{\varepsilon_{eff}}{area}\right)^{1.69}} \qquad (2\text{-}15)$$

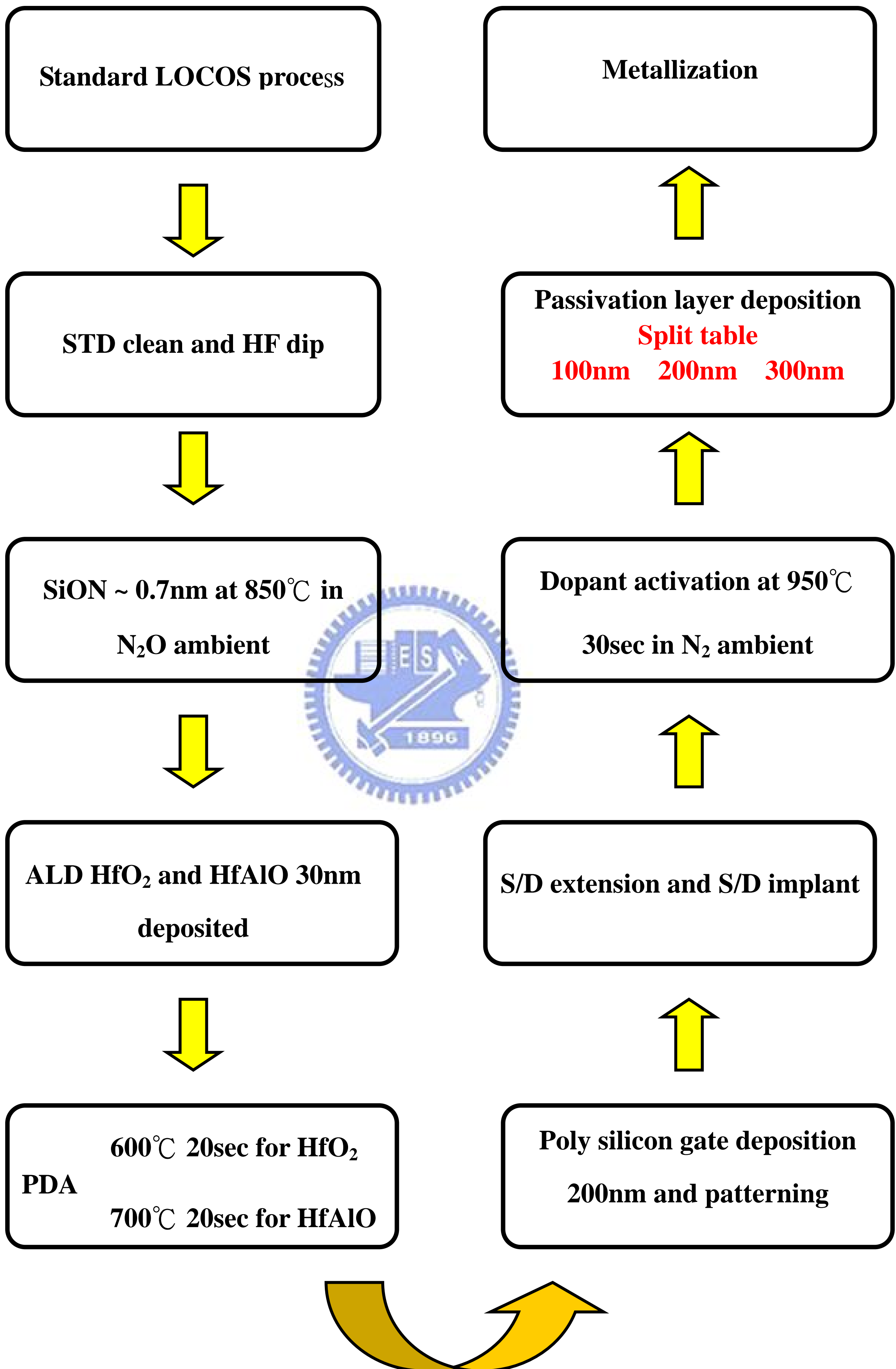
We can obtain the data that we need easily from above all equation. Fig 2-4 illustrates the configuration of split C-V measurement setup.

Carrier separation measurement is shown in Fig 2-5 and Fig 2-6 for nMOSFET and pMOSFET respectively. This method is used to make sure that the component

of gate leakage current under different state (i.e. inversion or accumulation). By comparing the I_G, I_{SD} and I_B that we can define which path dominates the leakage mechanism.

Subsequently, in CVS measurement method, a constant voltage stress was applied to the gate of device and the source/drain/substrate were grounded respectively. We obtained the measurement data such as Id-Vg and charge pumping during the stress intervals that Fig 2-5 shows the configuration of CVS measurement setup. After analyzing these data we could observe the shift of transconductance (Gm) and threshold voltage and charge pumping measurement is also used to calculate the interface state generation under inversion. In the same way, we could use equation (2-3) and (2-4) to calculate the bulk trap density after stressing.




Standard LOCOS process
STD clean and HF dip
SiON ~ 0.7nm at 850℃ in
N₂O ambient
ALD HfO₂ and HfAlO 30nm
deposited
PDA
600℃ 20sec for HfO₂
700℃ 20sec for HfAlO
Poly silicon gate deposition
200nm and patterning
S/D extension and S/D implant
Dopant activation at 950℃
30sec in N₂ ambient
Passivation layer deposition
Split table
100nm 200nm 300nm
Metallization

- Standard LOCOS process
- STD clean and HF dip
- SiON ~ 0.7nm at 850℃ in N_2O ambient
- ALD HfO_2 and HfAlO 30nm deposited
- PDA at 600℃ 20sec for HfO_2 and 700℃ 20sec for HfAlO in N_2 ambient
- Poly silicon gate deposition 200nm and patterning
- S/D extension and S/D implant
- Body engineering
- Dopant activation at 950℃ 30sec in N_2 ambient
- Passivation layer deposition **(split table: 100nm, 200nm and 300nm SiN)**
- Metallization

Fig 2-1 The process flow of nMOSFET device with HfO2 and HfAlO gate stack

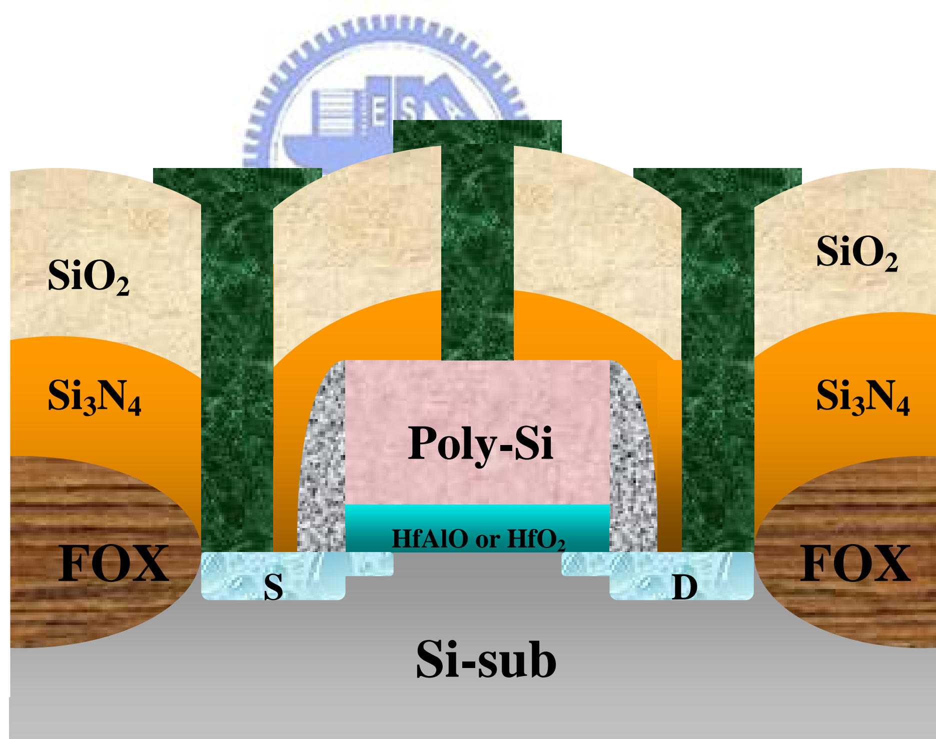


Fig 2-2 The cross section of nMOSFET with HfO2 and HfAlO gate stack

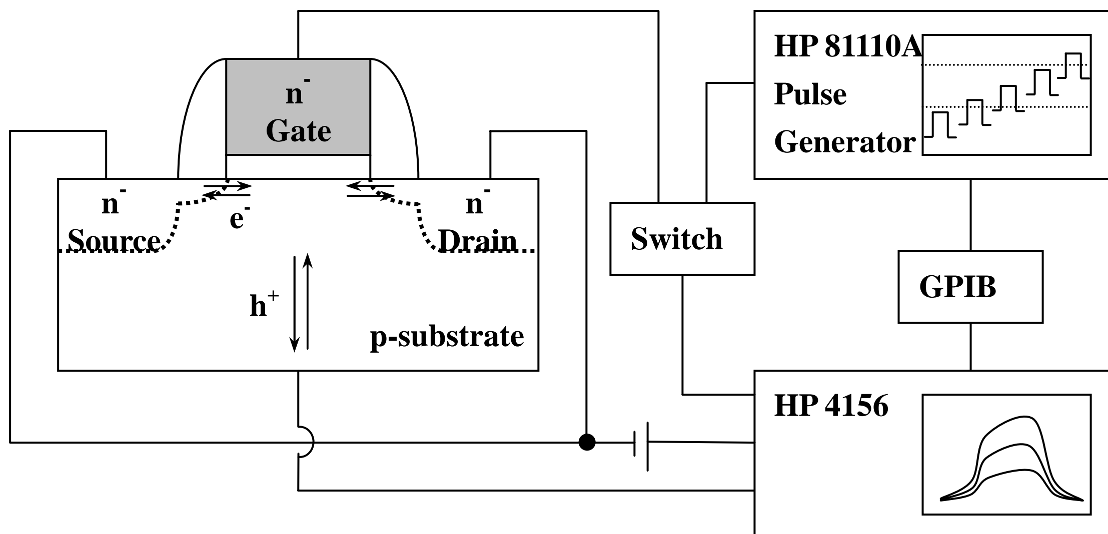


Fig 2-3 Configuration of charge pumping measurement setup

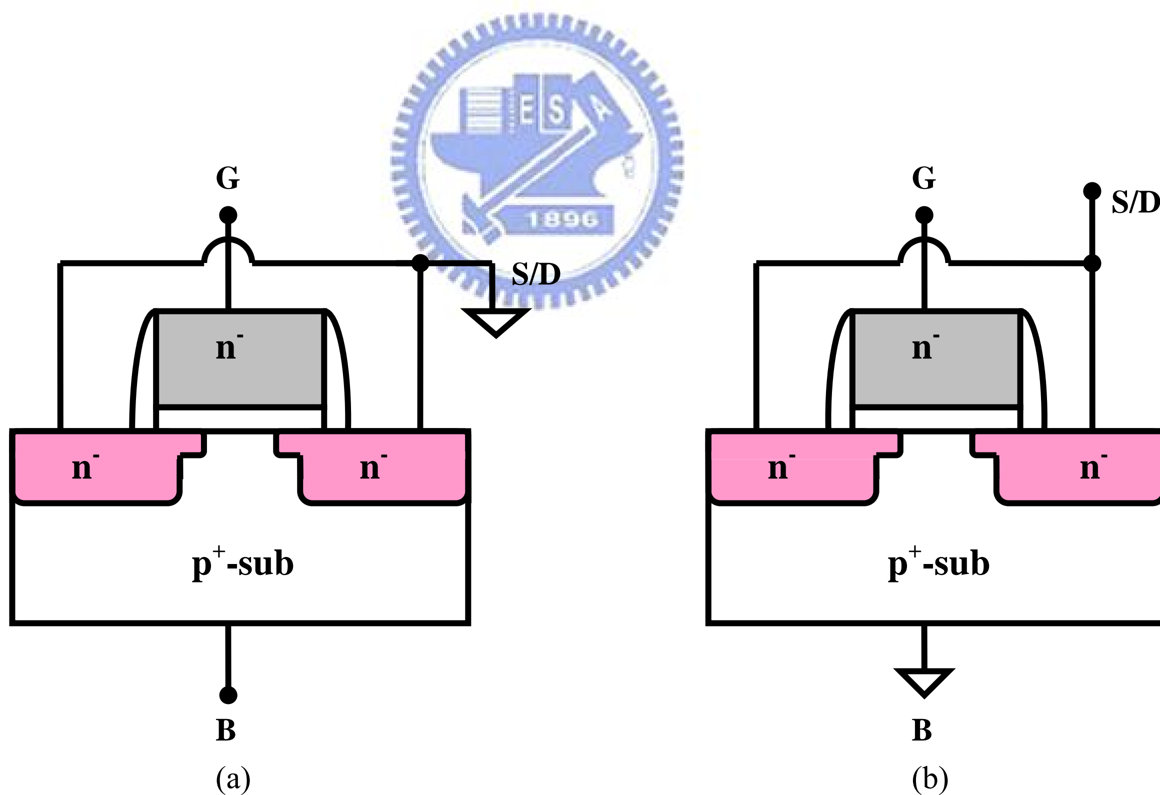


Fig. 2.4 Configuration for (a) gate-to-substrate (C_{gb}) (b) gate-to-channel (C_{gc}) capacitance measurements

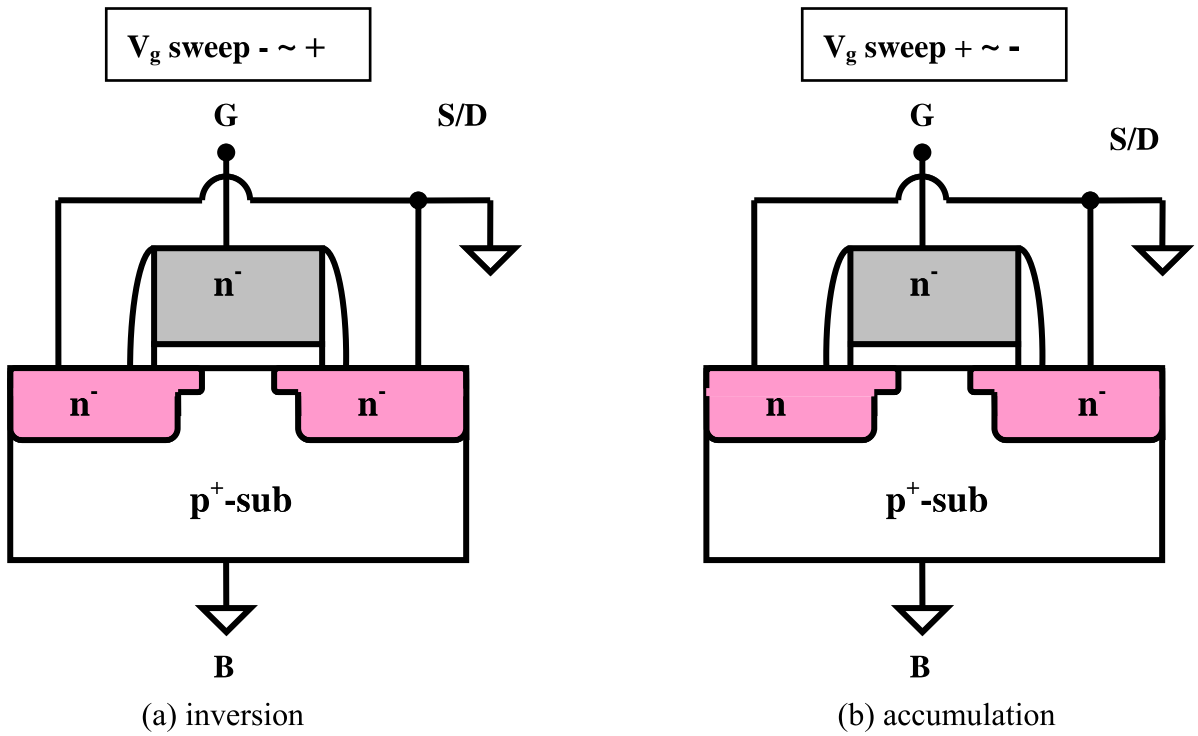


Fig 2-5 Configuration of Carrier Separation measurement setup for nMOSFET

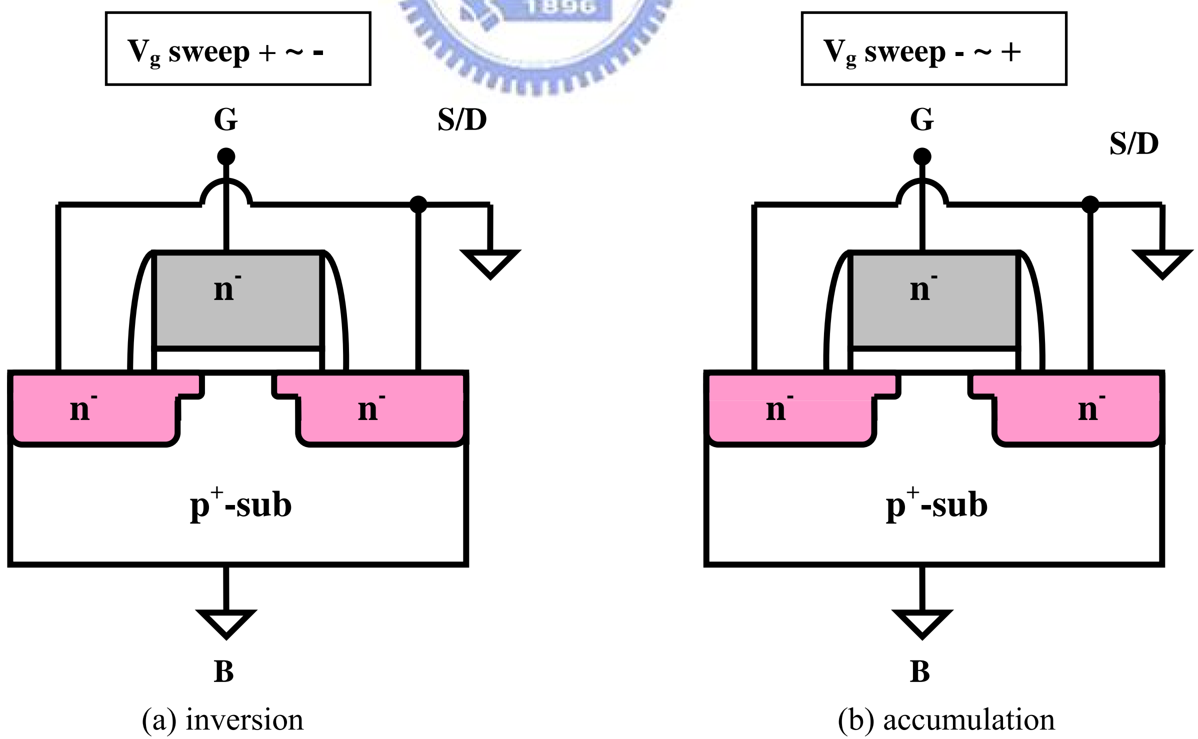


Fig 2-6 Configuration of Carrier Separation measurement setup for pMOSFET

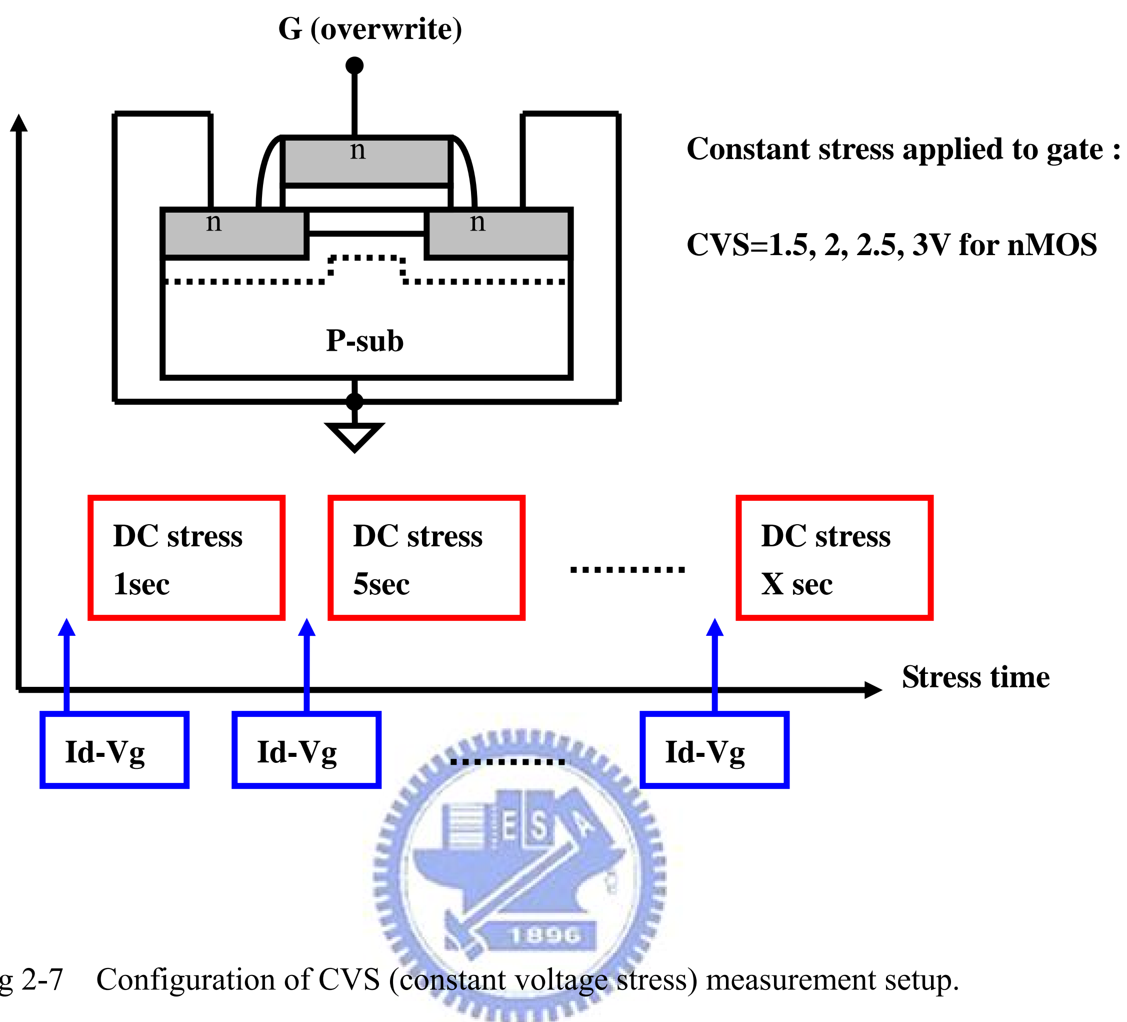


Fig 2-7 Configuration of CVS (constant voltage stress) measurement setup.

Chapter 3
Result and discussion

3.1 Introduction

Scaling of COMS has not only led to an increase of integration circuit density but also a corresponding enhancement in the transistor performance. However, when gate length scaled down to the nanometer order, some limitation such as gate oxide leakage current and and power density, make geometric scaling an increasingly challenging task. In order to continue CMOS device performance improvement, the industry needs a new scaling vector. Starting with the 90-nm technology generation, mobility enhancement through uniaxial process-induced strained Si has emerged as the next scaling vector being widely adopted in logic technologies [10~12].

Strain improves MOSFET drive current by altering the band structure of the channel. Biaxial and uniaxial strained silicon technologies are promising for enhancement of CMOS performance [13]. Biaxial tensile strain can be done by using a wafer-based approach of a thin strained Si layer on a thick relax SiGe virtual substrate, however, biaxial tensile strained silicon is difficult to implement because of some disadvantages of SiGe, such as misfit and threading dislocations, Ge up-diffusion, fast diffusion of S/D extensions, and cost [14~17]. Besides, high

threading dislocation density (typically > 10^4 cm^{-2}) of the virtual SiGe substrates represents a major obstacle for practical applications. In contrast, uniaxial strain can easily be applied by modifying capping layer deposition [18][19], shallow trench isolation [20][21], source/drain material [22], silicidation [23], packing process [24], and so on. In this paper, we utilized the SiN capping layer as a stressor due to its high stability and compatibility of conventional COMS process flow. Recently, it has been shown that the mechanical stress from a contact etch-stop SiN layer over the gate electrode can significantly affect the drive current [25][26]. Depending on the deposition conditions, the SiN capping layer can generate either tensile or compressive stress [26]. It thus can be applied to the NMOS devices that benefit from tensile stress, as well as PMOS devices that benefit from compressive stress[27].

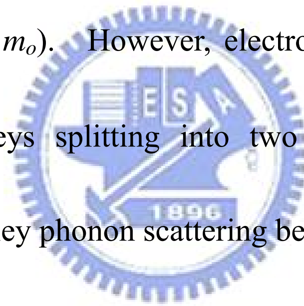
3.2 Brief Review of Strained Si

The carrier mobility is given by $\mu = \frac{q\tau}{m^*}$, where $1/\tau$ is scattering rate and m^* is the conductivity effective mass. Strain enhance the mobility by reducing the conductivity effective mass and/or the scattering rate. For electrons, both mass and scattering rate reducing are generally accepted as important for mobility enhancement[28]. However, for holes, only mass change due to band warping and repopulation [29] plays a significant role at today's manufacturable stress level (about < 1GPa) since strain-induced valence band splitting is smaller than that for the conduction band. Furthermore, though there has been focus on reduced in-plane mass to increase the mobility, increasing the out-of-plane mass for electrons and holes is also now understood to equally important factor for maintaining the mobility enhancement at high vertical fields, Fig 3-1 shows the definition of in- and out-of-plane. For electron transport in bulk Si at room temperature, the conduction band consists of six degenerate valley as shown in Fig 3-2(a) and these valleys are equal energy. The effective mass for any direction is the reciprocal of the curvature of the electron energy function. For unstressed bulk Si, the total electron conductivity mass, m^*, is given by

$$m^* = \left[\frac{1}{6}\left(\frac{2}{m_l}\right) + \left(\frac{4}{m_t}\right)\right]^{-1}$$

where m_l is longitudinal mass (parallel to the axis) about $0.98m_o$ and m_t is transverse

mass (perpendicular to the axis) about 0.19 m_o, where m_o is the free electron mass. After stressing, the valleys of Si are shown in Fig 3-2(b). For MOSFETs on a wafer, advantage strain removes the degeneracy between the four in-plane valley (Δ_4) and the two out-of-plane (Δ_2) by splitting them in energy as shown in Fig 3-2(c). The lower energy of the Δ_2 valleys means that they are preferentially occupied by electron. The electron mobility partly improves via a reduced in-plane and increased out-of-plane m^* due to the favorable mass of the Δ_2 valleys, which result in more electrons with an in-plane transverse effective mass (m_t = 0.19 m_o) and out-of-plane longitudinal mass (m_l = 0.98 m_o). However, electron scattering is also be reduced due to the conduction valleys splitting into two sets of energy levels, which suppresses the rate of intervalley phonon scattering between the Δ_2 and Δ_4 valleys.



For holes, the valence band structure of Si is more complex than the conduction band. Due to this complex structure as well as valence band warping under the strain that results in a larger mobility enhancement than electron. These two factors are also the reason that strained pMOSFET is a key focus in advantage logic technology. For unstrained Si at room temperature, holes occupy the top two band：the heavy and light hole bands. The unstrained constant energy surfaces for the two bands of Si are shown in Fig 3-3(a). With the application of strain, the hole effective mass becomes highly anisotropic due to band warping, and the energy levels become mixtures of

pure heavy, light, and split-off bands. Thus, the light and heavy hole bands lose their meaning, and holes increasingly occupy the top band at higher strain due to the energy splitting. The warped top two bands are shown in Fig 3-3(b), (c) and (d) for the three most common types of stresses. As shown in Fig 3-3 (b) and (c), the narrow constant energy surface in the channel direction for uniaxial compression creates a desire mass that about 40% smaller in-plane mass as compared to biaxial tensile strain. It is important to achieve high hole mobility by a low in-plane conductivity mass for the top band (namely a narrow width to the constant energy surface along the channel direction). This result is due to the difficulty of significantly enhancing hole mobility by reducing the intervalley scattering rate. Hole intervalley scattering rate is not significantly reduced for stress less than 1 GPa since the band splitting is less than the optical phonon energy (60mev). Splitting is greater than 60mev and stress is greater than 1GPa are necessary to suppress the intervalley phonon scattering rate (see Fig 3-4). This is why the change of effective mass plays a more significant role than reduced phonon scattering in hole mobility enhancement.

Hole mobility at high vertical field with uni-axial compressive and biaxial tensile stresses would have different behaviors. Fig 3-5 shows the energy shift with confinement for both uniaxial and biaxial stress. E_{top} represents the top band with large out-f-plane mass for uniaxial stress and small out-f-plane mass for biaxial stress

which compare to the second band, E_{second}. Thus, uniaxial has a small shift in energy (indicates E_{top} which compares to unstrained) due to confinement for it, but there is a large shift for biaxial. As shown in Fig 3-5, the strain-induced band splitting (E_{top}-E_{second}) increases for uniaxial strain but decreases for biaxial stress. Thus, confinement favors occupation of the top band for uniaxial compressive stress and the second band for biaxial tensile stress. The net effect is strain and confinement additive for uniaxial compressive stress and subtractive for biaxial tensile stress. Thus, the competing effects of strain and confinement on band splitting is a factor of lost hole mobility in biaxial tensile stress for pMOSFET at high vertical fields. For uniaxial stress, the band splitting increased that maintains the hole mobility enhancement at high vertical fields. This is why the uniaxial compressive stress is extensively adopted in pMOSFET [12][31] [32].

For NMOSFETs, it has been reported that the threshold voltage shift caused by bi-axial tensile stress is larger than the case with uni-axial tensile strain [33]. For PMOSFETs, larger shift of light-hole band edge under bi-axial tensile strain leads to larger shift in V_{th}, compared with the case with uni-axial compressive strain [34].

3.3 Electrical Characteristics of MOSFETs with different thickness of SiN capping layer and materials

The C-V curve and EOT value are shown in Fig 3-6 and Fig 3-7 respectively, it can be seen that the different SiN thickness which induced strain will not change the equivalent oxide thickness of device. By this fact, we can make sure that the drive current enhancement is not caused by EOT decrease. By equation $\kappa = \varepsilon_{ox} \frac{T_{physical}}{EOT}$, where ε_{ox} is the dielectric constant of SiO_2 and $T_{physical}$ is the real thickness of gate dielectric. Then, we can obtain that the dielectric constant, "κ", is about 12. The relation of I_d-V_g and G_m-V_g characteristic of HfAlO gate stack nMOSFET with different SiN capping layer thickness that upon the gate are shown in Fig 3-8 and Fig 3-9. Simultaneously, the I_d-V_d is also shown in Fig 3-10. It is about 2 times enhancement for I_d and G_m between the without SiN and SiN 3000A. The improvement of drain current and transconductance is obviously proportional to the thickness of SiN layers. The mechanism which results in these results might be as follows: These SiN capping layers upon the poly-Si gates with highly tensile stress cause the poly-Si gates under them to be with compressive strain, and then the tensile strain is caused in the channel regions by these compressive poly-Si gates upon channel regions. The results might also be caused by another mechanism: The SiN capping layers with highly tensile stress are directly deposited on the source/drain

regions in the two terminals of channels. These SiN layers cause the source/drain regions under them compressive and the channel regions are implicated to become tensile. Fig 3-11 and Fig 3-12 show that the relation of drain current and transconductance of HfO_2 gate stack pMOSFET with different tensile SiN capping layer. According to [12], it can be obtained the degradation of drain current for pMOSFET in such a tensile stress and it is about 14.8% and 30.8% degradation of I_d and G_m respectively in figure. The relation between drain current and channel length of HfAlO gate stack nMOSFET is shown in Fig 3-13 and G_m is in Fig 3-14. By above result, we can know that the strain effect is strong with short channel especially when channel length downs to 0.35μm. However, it can be also seen that the drain current enhancement is saturated when channel length is above 2μm. In addition, Fig 3-15 shows that the relation of drain current with different areas of channel, when area of channel is large, the strain effect will not enhance the drain current. Unlike biaxial strain, driving current improvement with uniaxial strain obviously takes place in short channel device. This is also fit to the scaling-down demand.

The subtreshold swing versus to channel length of HfAlO gate stack nMOSFET with different SiN capping layer thickness is shown in the Fig 3-16. We find that the subthreshold swing of SiN 3000A shows the better interface state than others. Thus, we can find that the strain will improve the subthreshold swing in device. Fig 3-17

shows that the V_{th} roll-off characteristic with different thickness of SiN capping layer. It can be seen that when the channel length is scaled below 1μm, the roll-off phenomenon is more series. Fig 3-18 indicates that gate leakage current seems not to be increased as SiN thickness thicker. The extra hydrogen species come from the SiN layer as a result of using SiH_4 and NH_3 as precursors during deposition. It is well known that the PE-SiN film contains a substantial amount of hydrogen [35]. Fig 3-19 expresses the charge pumping current for different thickness of SiN layer. We obtain that the charge pumping current decreased as the thickness of SiN capping layer increased from 0 A to 3000 A. This means that the extra hydrogen species come from the SiN layer as a result of using SiH_4 and NH_3 as precursors during deposition and a lot of dangling bond could be fixed and therefore reduced interfacial state. It is well known that the PE-SiN film contains a substantial amount of hydrogen [35]. These hydrogen could passivate interfacial state that located on interfacial layer. So, depositing thicker SiN would take long time and more interfacial state could be fixed. The brief pasivation diagram is in Fig 3-20, it can be seen that when SiN is deposited by PECVD, a lot of hydrogen species will locate at the interface to passivate the interface states.

Carrier separation analysis is investigated to clarify the leakage path in gate stack MOSFET [36]. The contributing carrier of leakage currents consist of holes and

electrons. Fig 3-21, Fig 3-22, Fig 3-23 and Fig 3-24 express carrier separation results under inversion regions and accumulation regions for n^+-gate nMOSFETs with different thickness of SiN layer of HfAlO/SiON gate stack. By above result, we can find that the I_G is close to I_{SD} under inversion region, it means that the source/drain current dominates the leakage current. In contrast, the substrate current dominates the leakage current under accumulation region. This phenomenon indicates electron from S/D that goes through high-k dielectric to gate is the major component of conduction mechanism under inversion region. We can easily explain this mechanism by band-diagram in Fig 3-25(a) and carrier separation current component is in Fig 3-25(b). The substrate current which corresponds to hole current from the gate, while source/drain current corresponds to electron current from silicon substrate under inversion region. Hole supplied from gate valence band on nMOSFET are confined by less generation of minority holes in n^+-gate. In other words, carrier which go through gate dielectric are influenced by barrier height and distance[37]. Due to the asymmetry of the HfAlO/SiON (Fig 3-25(a)) and structure, we can deduce that holes from gate electrode are hard to go through the dielectric compared to electrons from the channel. In brief, electron current from the channel is the predominant injection current under stressing. Similarly, the inference also is used to explain the leakage component under accumulation region. Fig 3-26 (a) expresses

the band-diagram to interpret possible leakage current from under accumulation. Fig 3-26(b) shows the current component flow in carrier separation experiment. Fig 3-27, Fig 3-28, Fig 3-29 and Fig 3-30 show that the gate leakage current with different thickness of SiN under inversion regions and these are measured form room temperature to 125℃. We obtain the leakage current increased as temperature elevated. This phenomenon means that the conduction mechanism must be relate trap-related like schottky-emission, trap-assisted tunneling, Frenkel-Poole emission, etc. Then, the result which we get accords with Frenkel-Poole emission for electron current. Fig 3-31, Fig 3-32, Fig 3-33 and Fig 3-34 show that the excellent linearity relation for source/drain current (electron) with different thickness of SiN under inversion region, and Fig 3-35, Fig 3-36, Fig 3-37 and Fig 3-38 for substrate current (hole current). Then, the fitting curve can be acquired from these dorms as follows：

$$I \propto V \ \exp\left(\frac{2a\sqrt{V}}{T} - \frac{q\Phi_B}{k_B T}\right)$$

$$J = B * E_{eff} \exp\left(\frac{-q(\Phi_B - \sqrt{qE_{eff} / \pi\varepsilon_{\mathrm{HfAlO}}\varepsilon_0})}{k_B T}\right) ; \ B = q\mu NT, \ a = \frac{\varepsilon_{SiO_2}}{\varepsilon_{\mathrm{HfAlO}}} = const$$

$$\ln\left(\frac{J}{E_{eff}}\right) = \frac{-q\sqrt{q / \pi\varepsilon_r\varepsilon_0})}{k_B T}\sqrt{Eeff} - \frac{q\Phi_B}{k_B T}$$

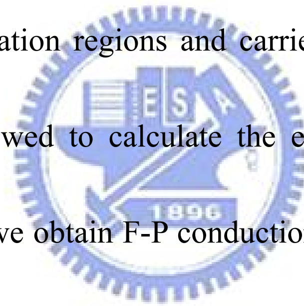
$\Rightarrow$ Intercept gives the Barrier height ($-\frac{q\Phi_B}{k_B T}$)

Where B is a constant which is about the trapping density and carrier mobility in insulator, Φ_B is the barrier height, E_{eff} is the electric field in HfAlO films, ε_0 is the free space permittivity, k_B is Boltzmann constant, and T is the temperature in Kelvin.

This tendency indicates that both electron and hole conduction mechanisms are the same, and the result agrees well with the F-P conduction mechanism. Barrier hight Φ_B and dielectric constant ε_{HfAlO} of HfAlO/SiON can be calculated. The value of electron Φ_B for without SiN, SiN 1000A, SiN 2000A and SiN 3000A under inversion are about 0.737eV, 0.722eV, 0.645eV and 0.621eV and Φ_B for hole are 0.639eV, 0.614eV, 0.571eV and 0.464eV. The Φ_B to be discussed in this chapter is the "effective" value that is representative of the HfAlO/SiON gate stack [49]. We consider the case when the injected carrier flow across HfAlO/SiON by hopping via the trap sites with energy barrier Φ_B, whose value depends on the fabrication process[50]. Fig 3-39 shows energy band diagram to present conduction mechanism through HfAlO/SiON gate stack with different SiN capping layer. And Fig 3-40 shows that the result od electron and hole trap with different SiN capping layers. This indicates that less barrier height as SiN capping layer increases.

3.4 Summary

In this chapter, we verify that PECVD SiN capping layer is tensile strain and suitable for nMOSFETs application. Therefore, as SiN capping layer thickness increases, driving current has a huge enhancement. Besides, we observe that interface states become less when SiN capping layer thickens. It may be attributed that a large amount of hydrogen generated from SH_4 and NH_3 and then passivate the interfacial layer and we verify the number of interface states by using charge pumping method. Eventually, we utilize carrier separation method to make sure the current component under inversion and accumulation regions and carrier separation measurement with different temperature is followed to calculate the electron and hole barrier height under inversion region then, we obtain F-P conduction mechanism is matched. This indicates that less barrier height as SiN capping layer increases.



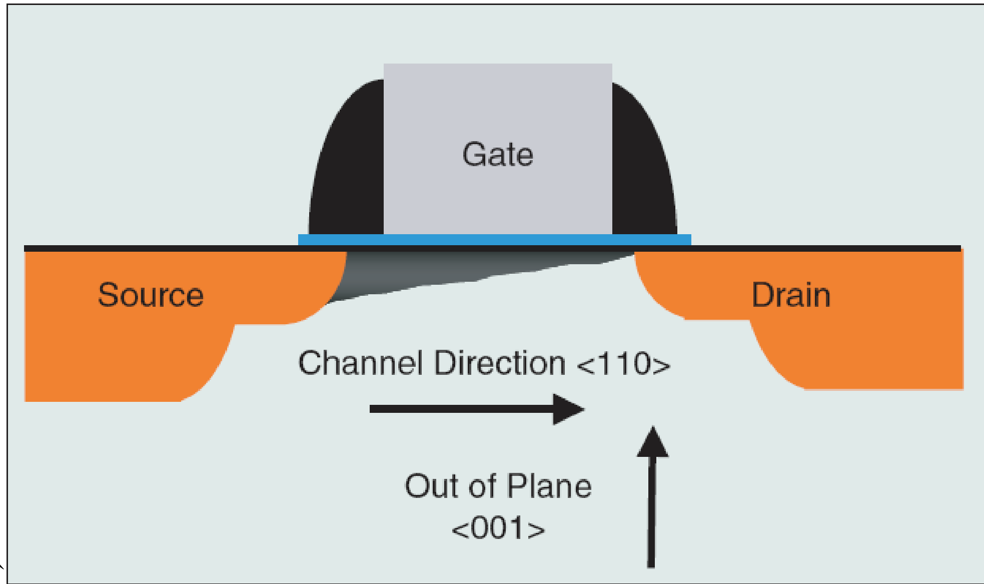


Fig 3-1 Definition of in- and out-of-plane direction

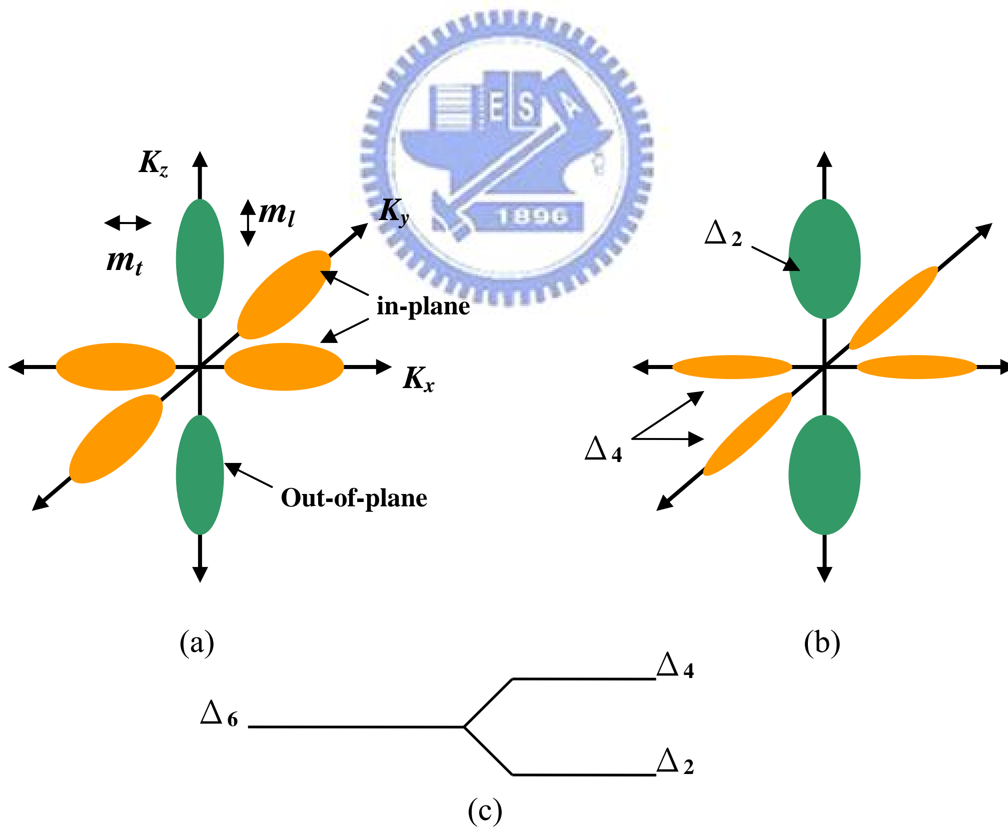


Fig 3-2 Ellipsoids of constant electron energy in reciprocal ("k") space (a) Unstrained Si (b) Strained Si ; (c) Strain splits the energy level as shown, removing the degeneracy between the Δ_4 and Δ_2

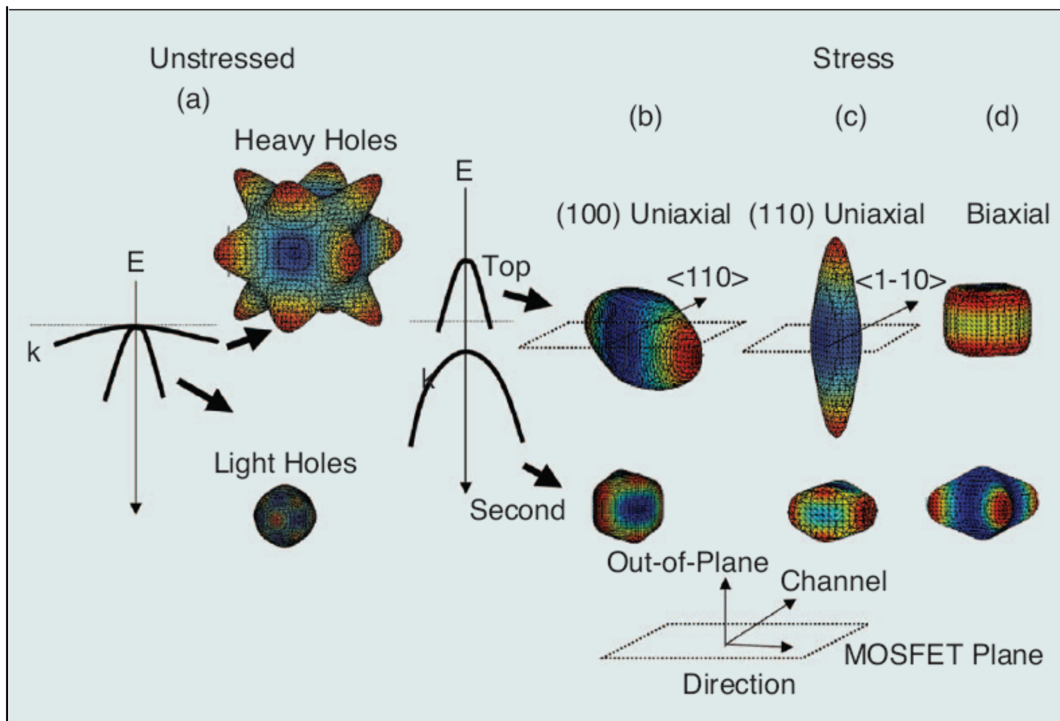


Fig 3-3 Hole constant energy surfaces at 25meV obtained from six band kp calculations for common types of stresses：(a) unstressed, (b) longitudinal compression on (100) wafer (c) longitudinal compression on (110) wafer, and (d) biaxial tension

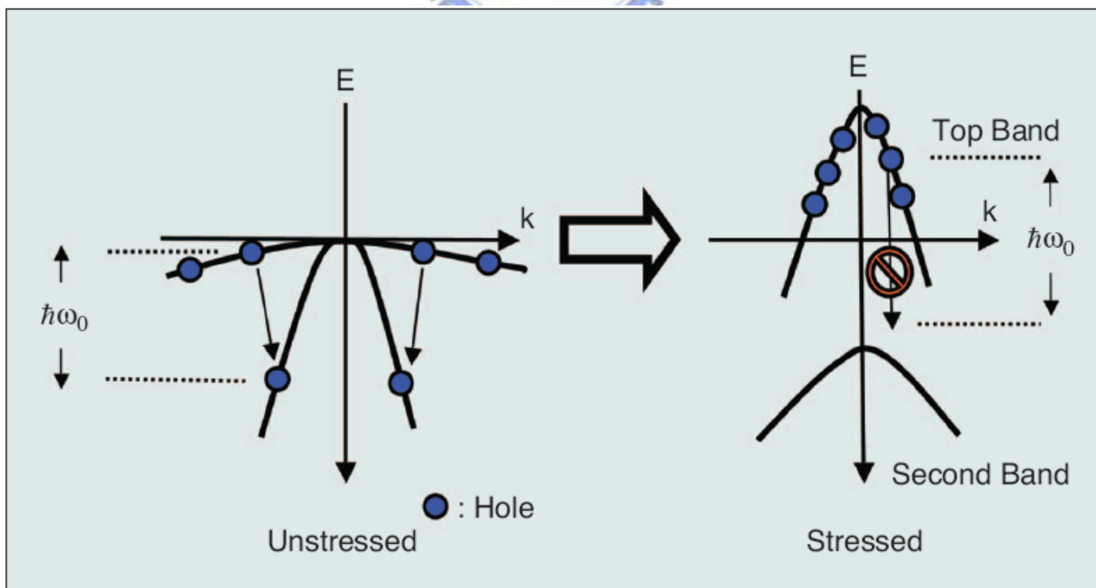


Fig 3-4 Hole intervalley phonon scattering process. High stress and splitting larger than the optical phonon energy (60 meV) are required to suppress scattering.

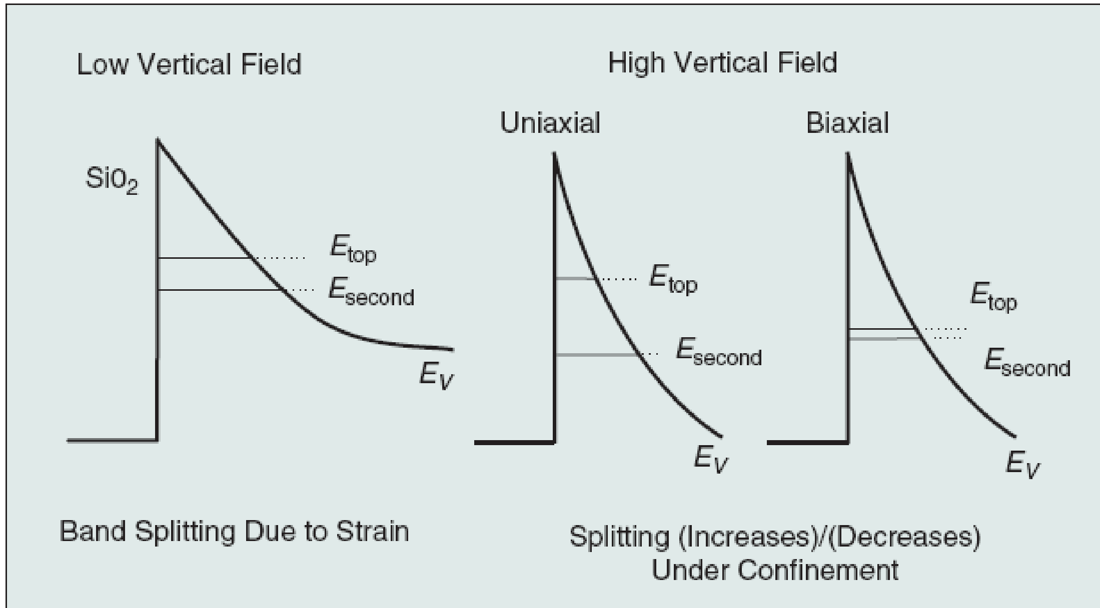


Fig 3-5 Simplified schematic of valence band splitting of strained Si as a function of gate overdrive.

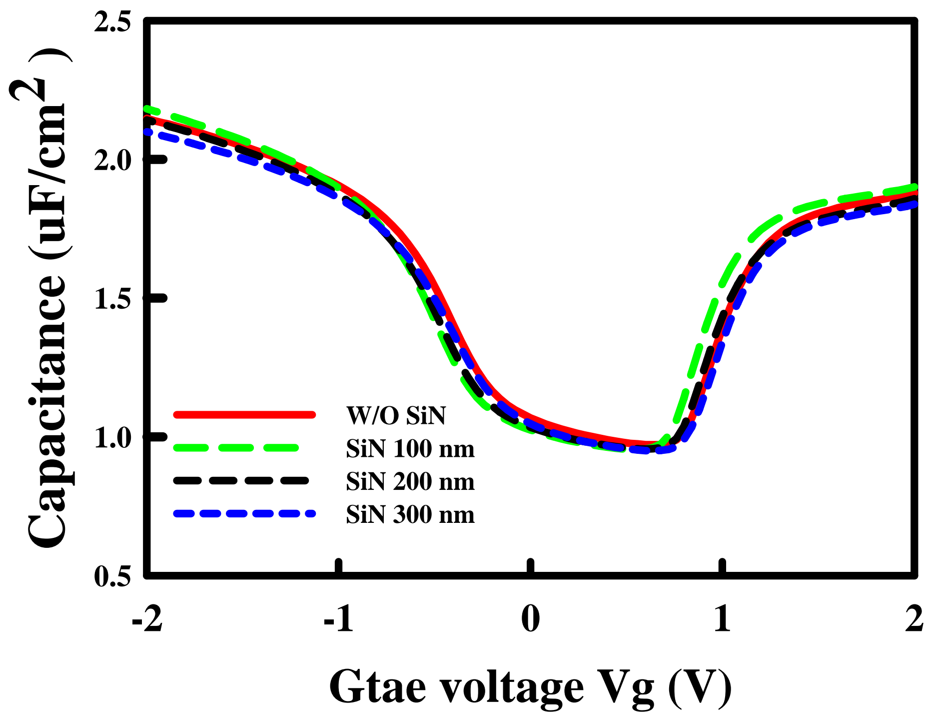


Fig 3-6 The C-V curve of the HfAlO gate stack nMOSFET

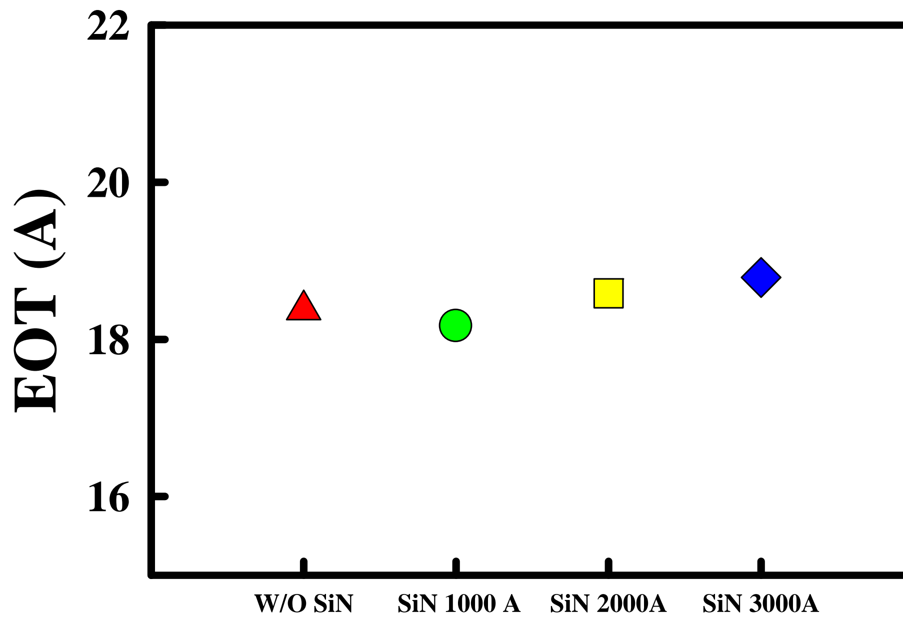


Fig 3-7 The EOT for HfAlO gate stack nMOSFET

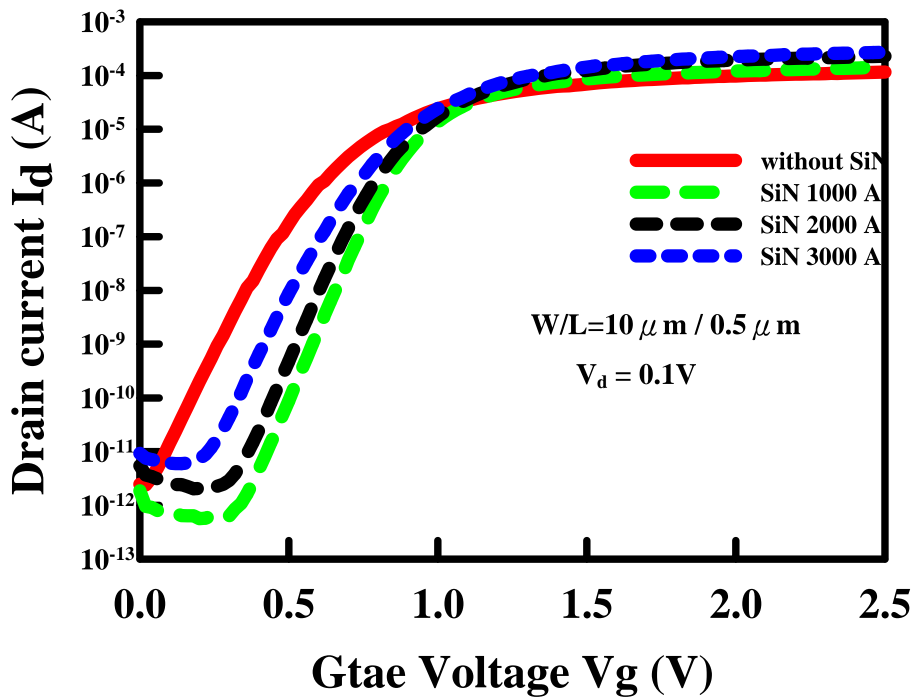


Fig 3-8 The drain current versus to gate voltage with different SiN capping layer for HfAlO gate stack nMOSFET

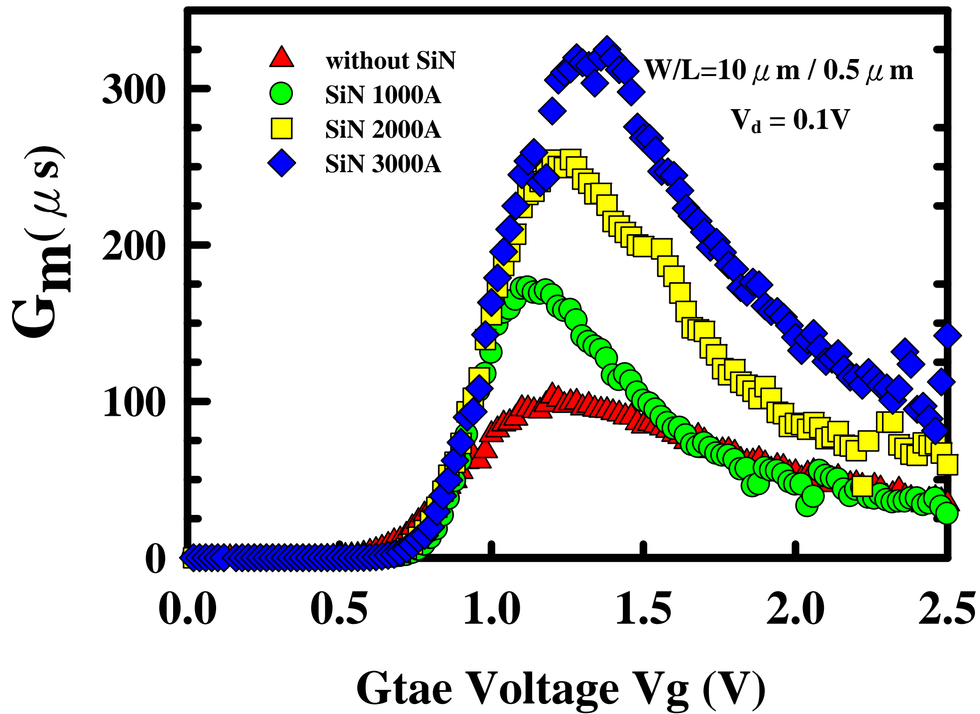


Fig 3-9 The Transconductance of devices with different capping layers for HfAlO gate stack nMOSFET

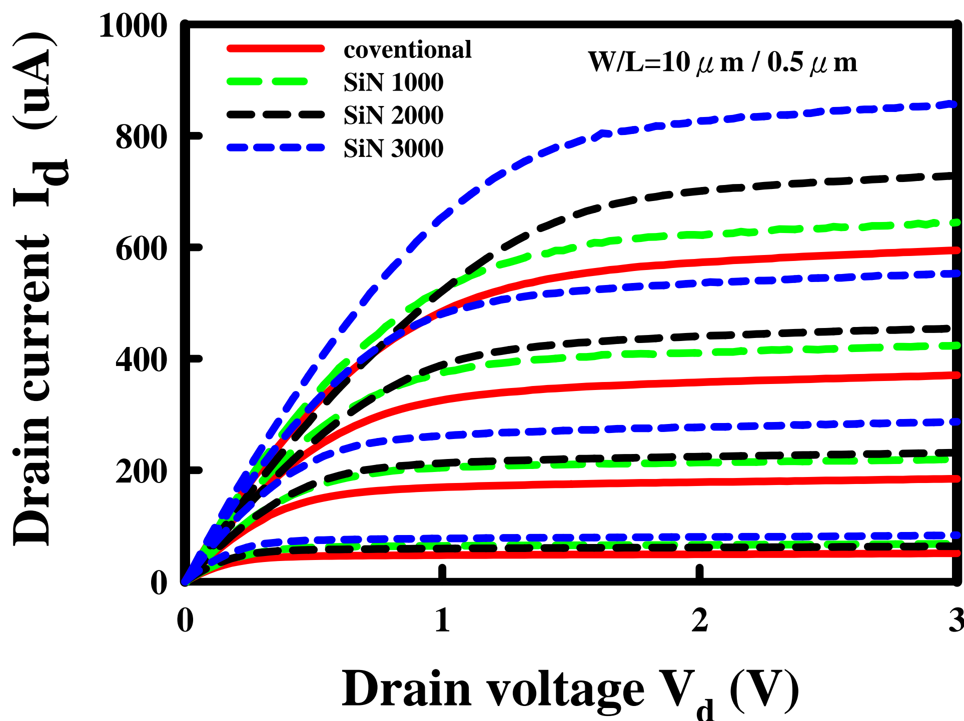


Fig 3-10 The drain current versus to gate voltage with different SiN capping layer for HfAlO gate stack nMOSFET

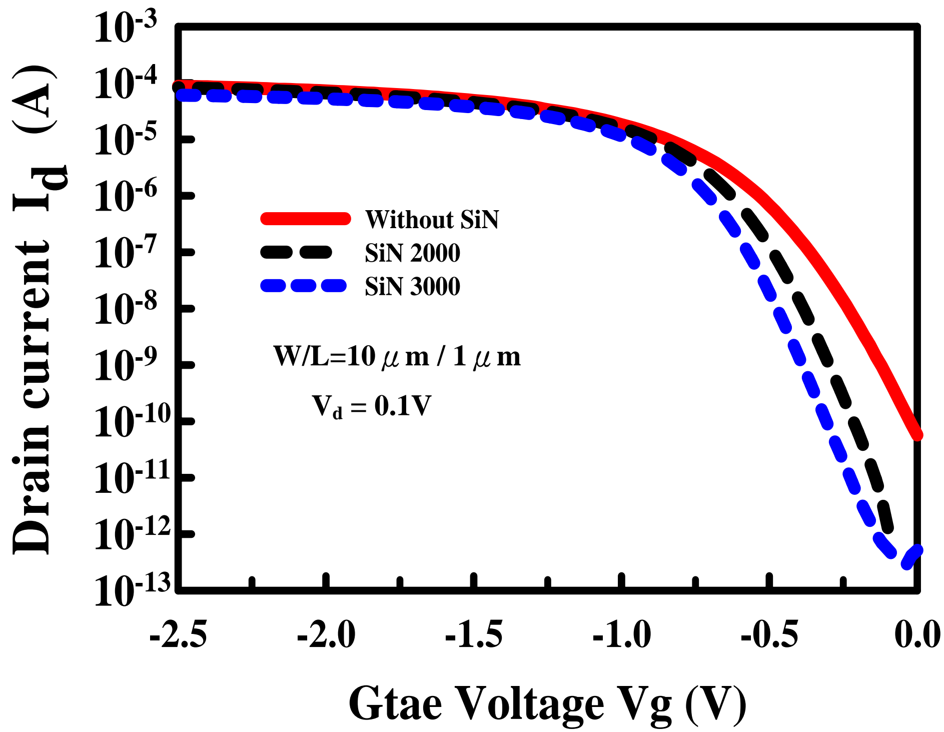


Fig 3-11 The drain current versus to gate voltage with different SiN capping layer for HfO_2 gate stack pMOSFET

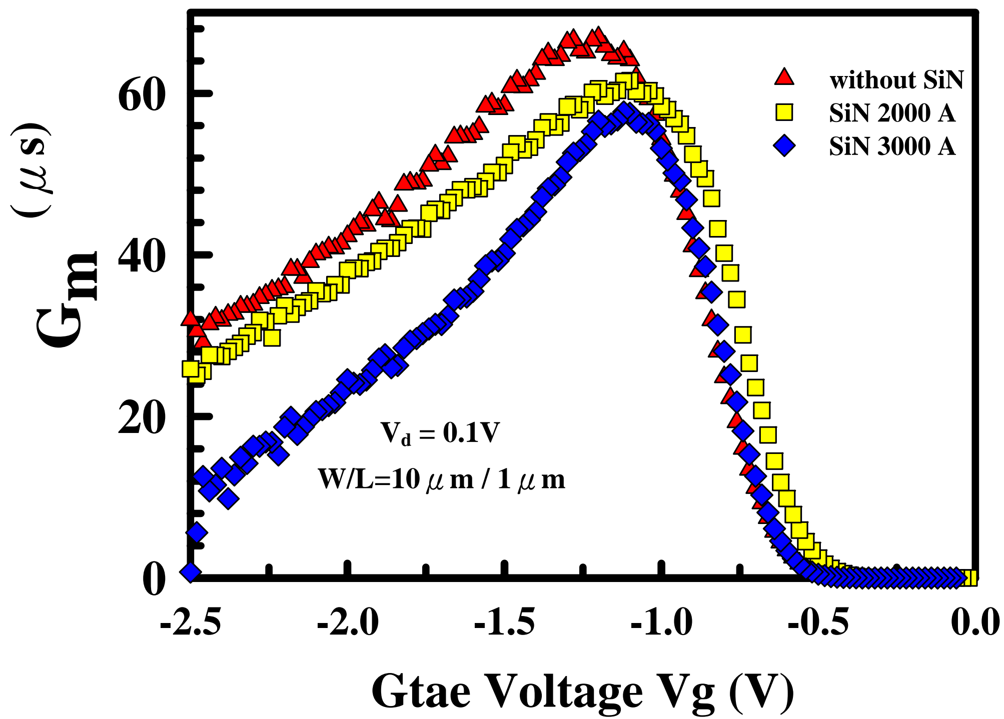


Fig 3-12 The transconductance of devices with different capping layers for HfO_2 gate stack pMOSFET

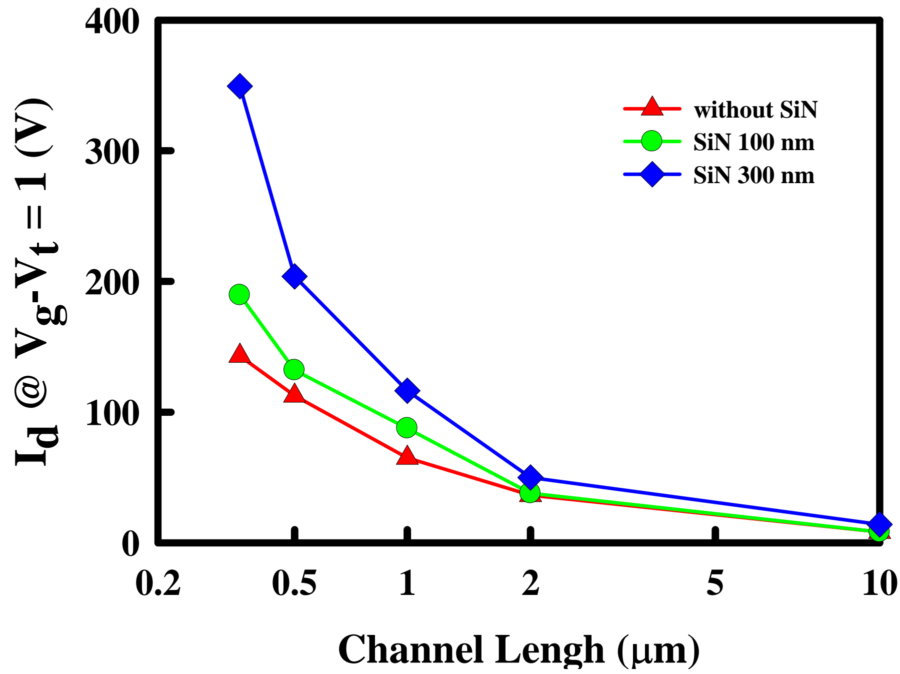


Fig 3-13 The drain current versus to different channel length for HfAlO gate stack nMOSFET

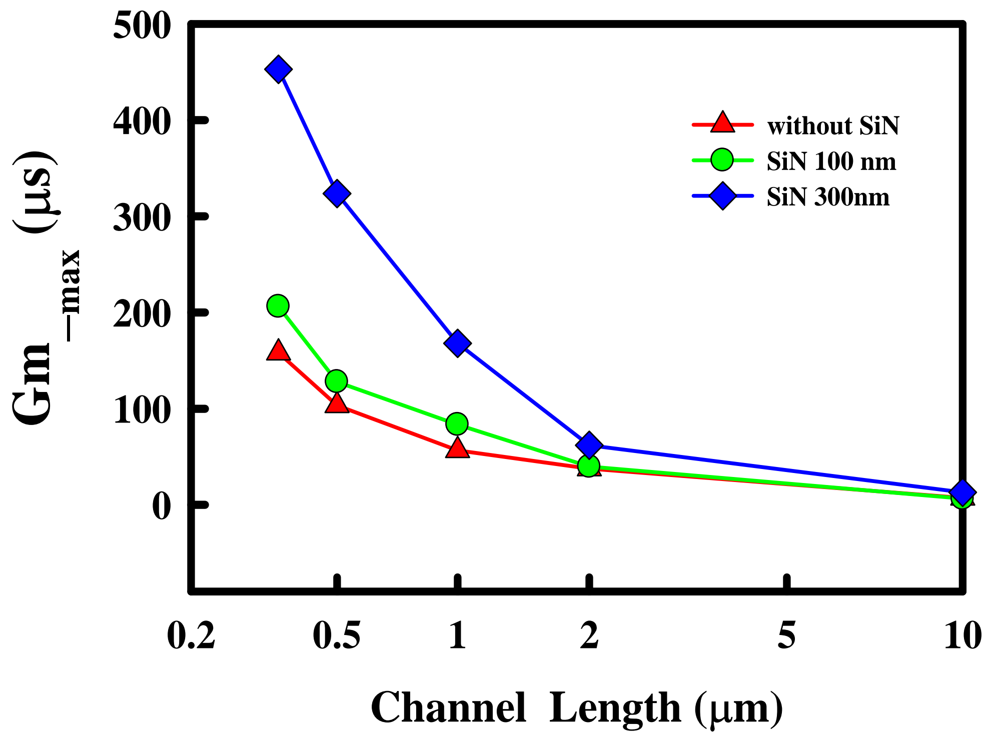


Fig 3-14 The maximum transconductance versus to different channel length for HfAlO gate stack nMOSFET

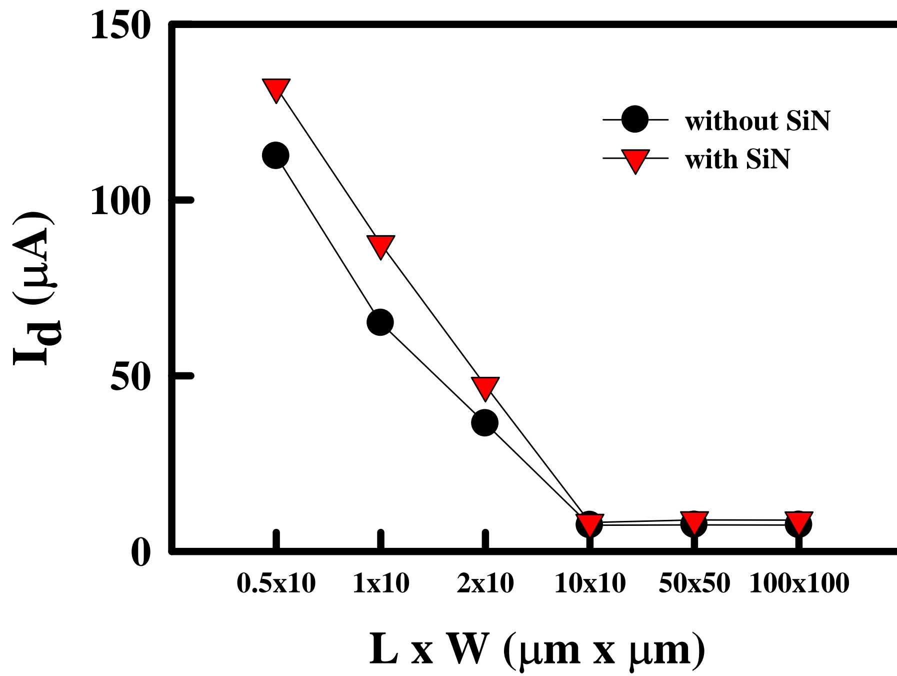


Fig 3-15 The drain current versus to different area for HfAlO gate stack nMOSFET

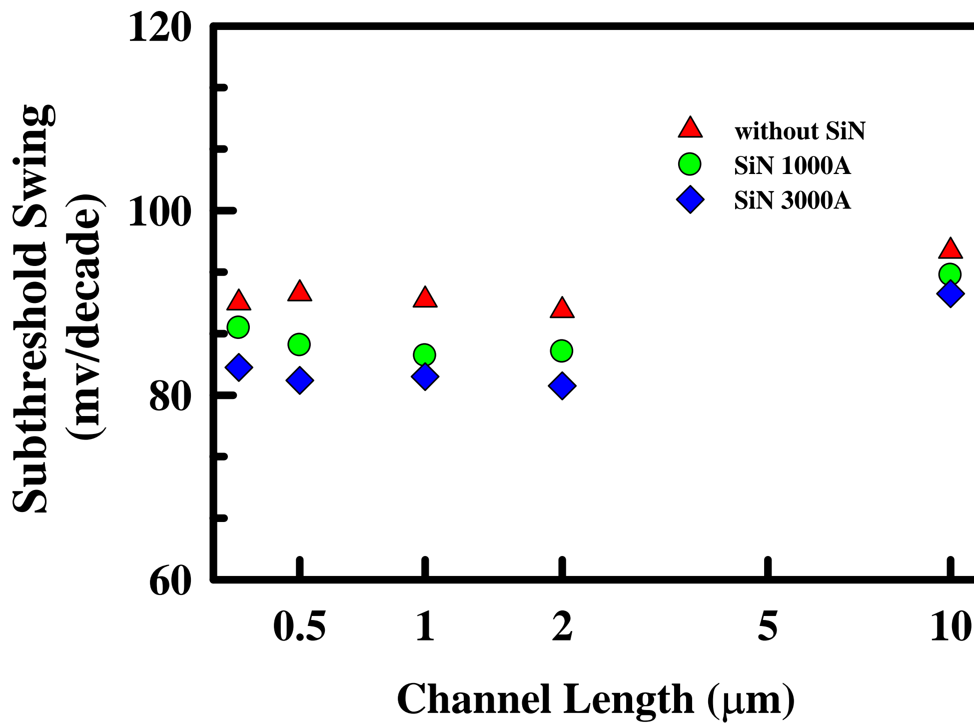


Fig 3-16 The subthreshold swing versus to different channel length for HfAlO gate stack nMOSFET

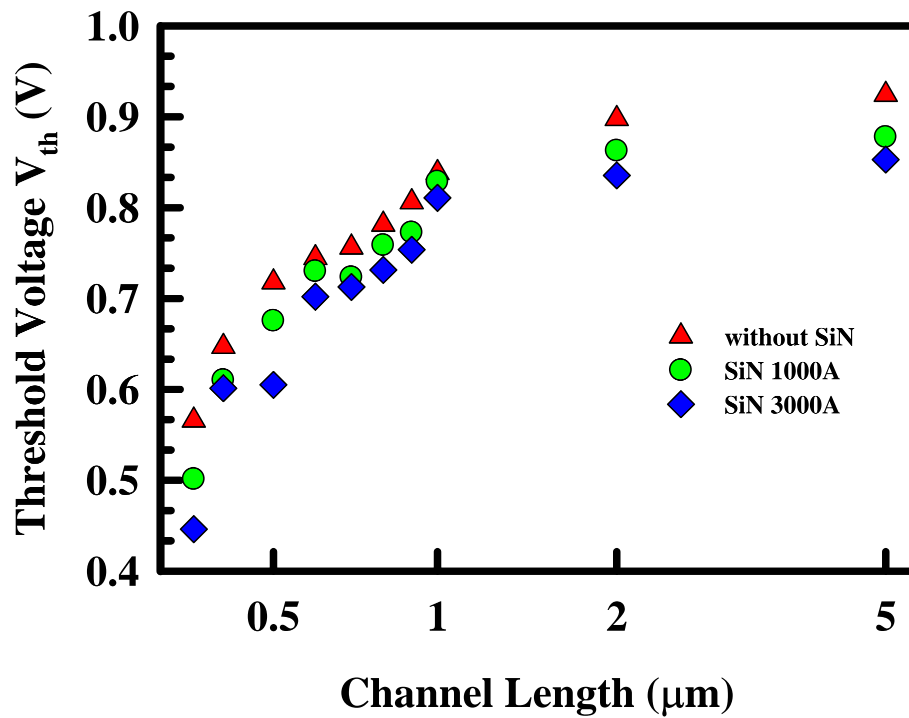


Fig 3-17 Vth roll-off characteristics for HfAlO gate stack nMOSFET

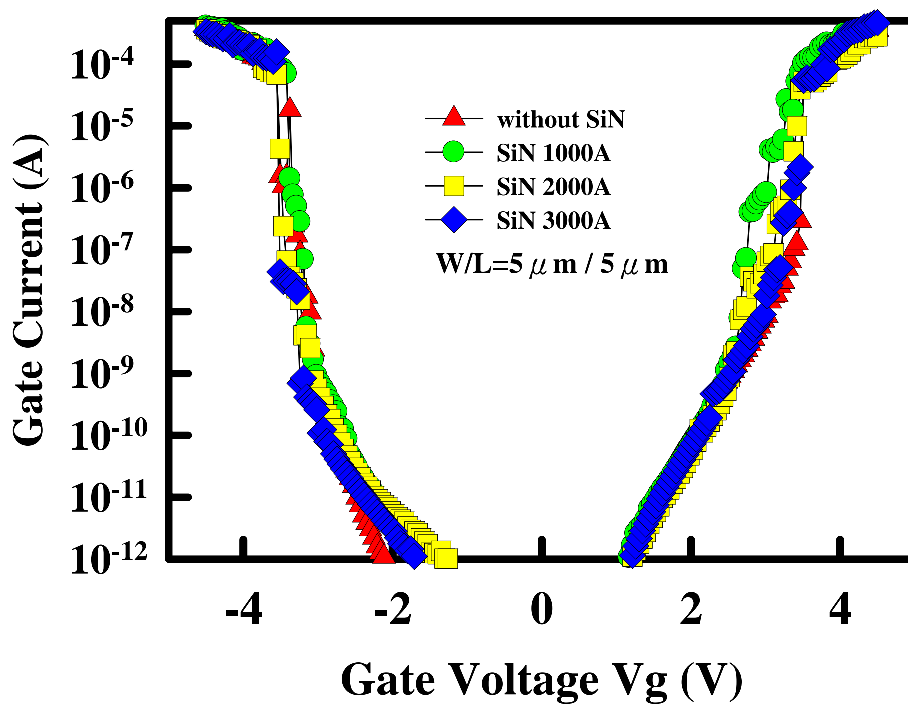


Fig 3-18 Gate leakage current versus gate bias for fresh n-channel devices at room temperature

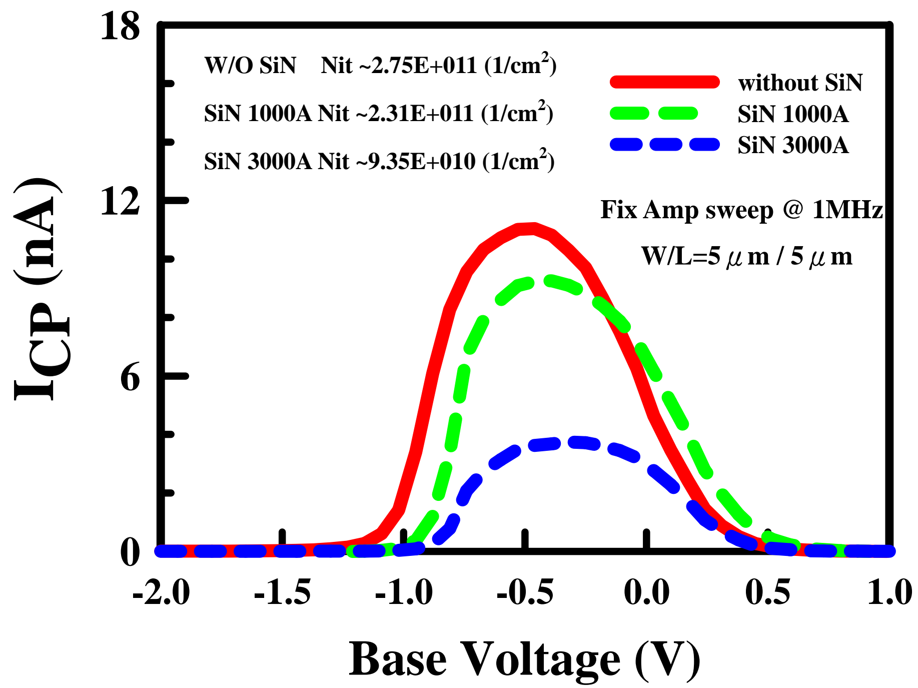
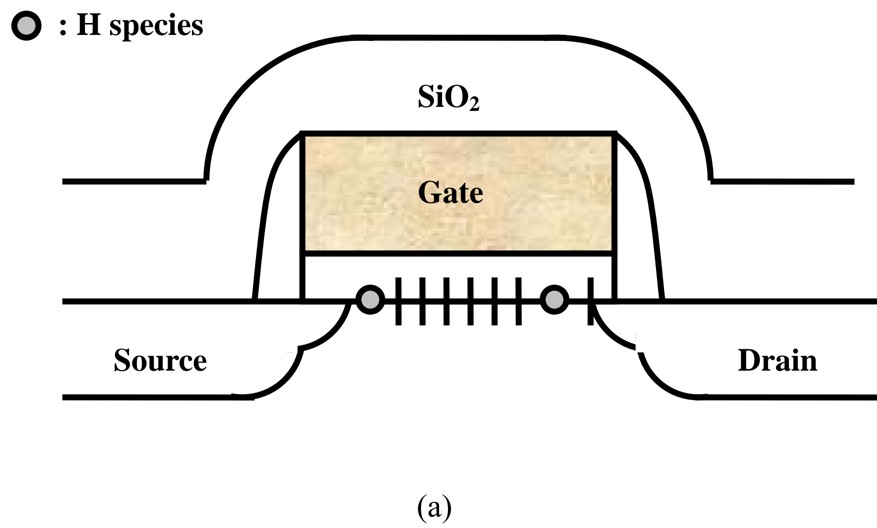
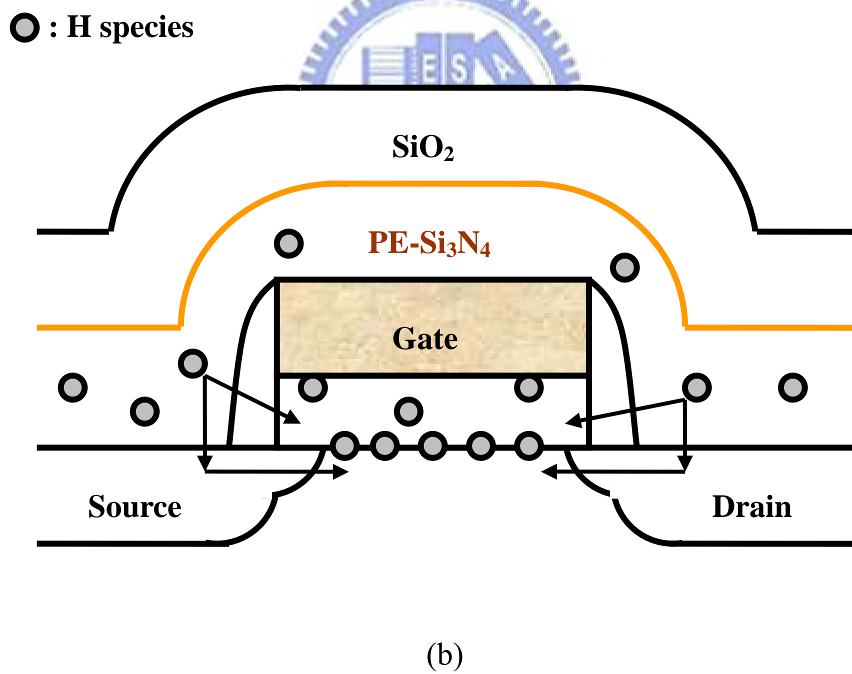


Fig 3-19 Charge pump current for HfAlO gate stack nMOSFET with different SiN thickness

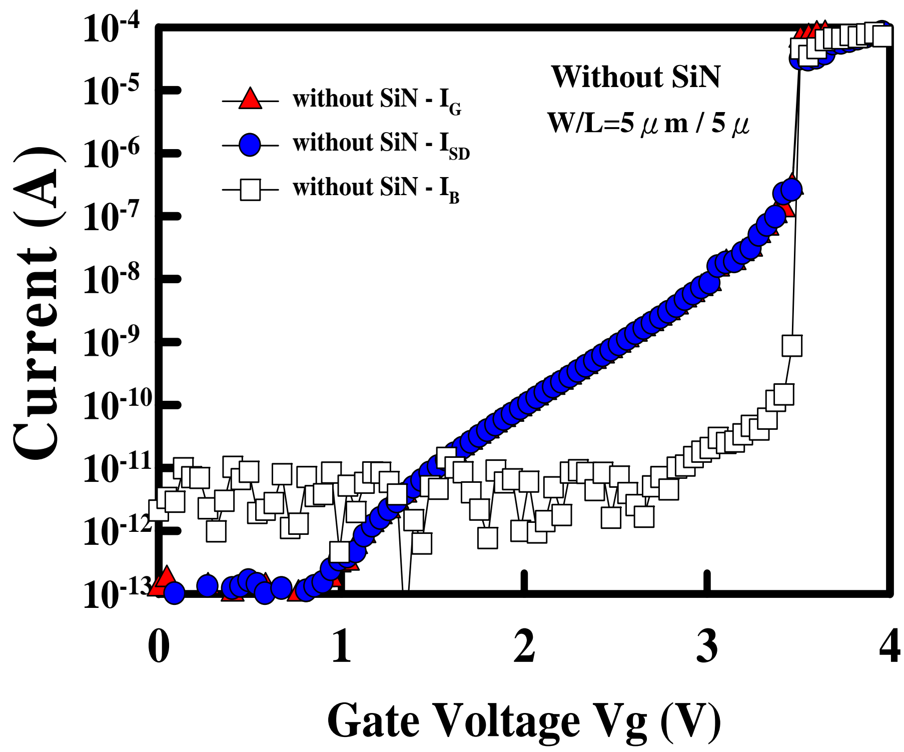


(a)

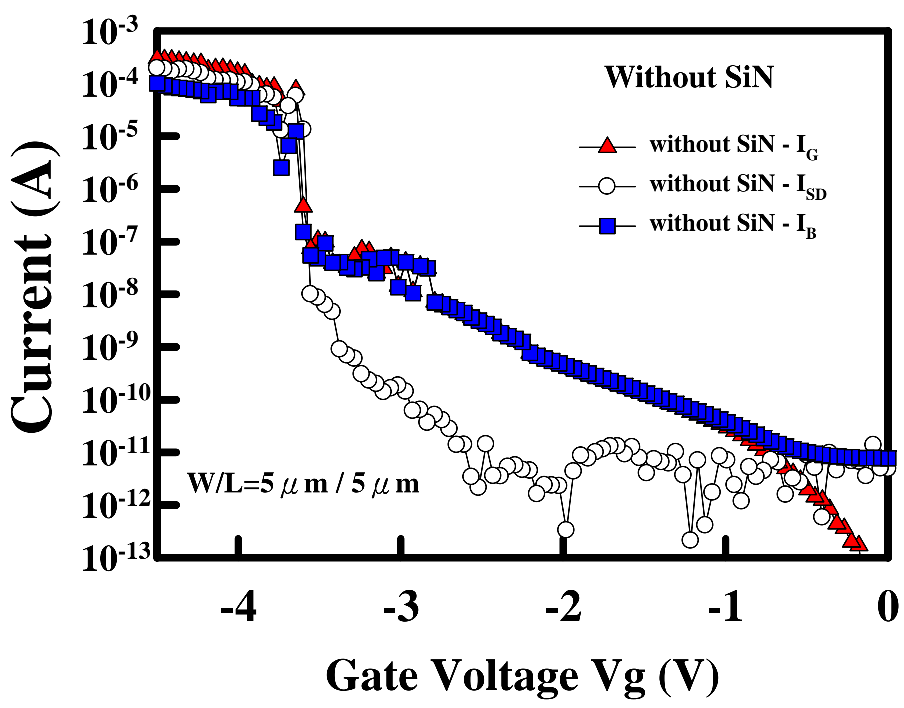


(b)

Fig. 3.20 (a) In control devices, hydrogen species mainly locate at the interface to passivate the interface states. (b) In SiN-capping devices, a large amount of hydrogen species from the SiN layer diffuse to the gate oxide layer and passivate the Si/HfAlO interface.

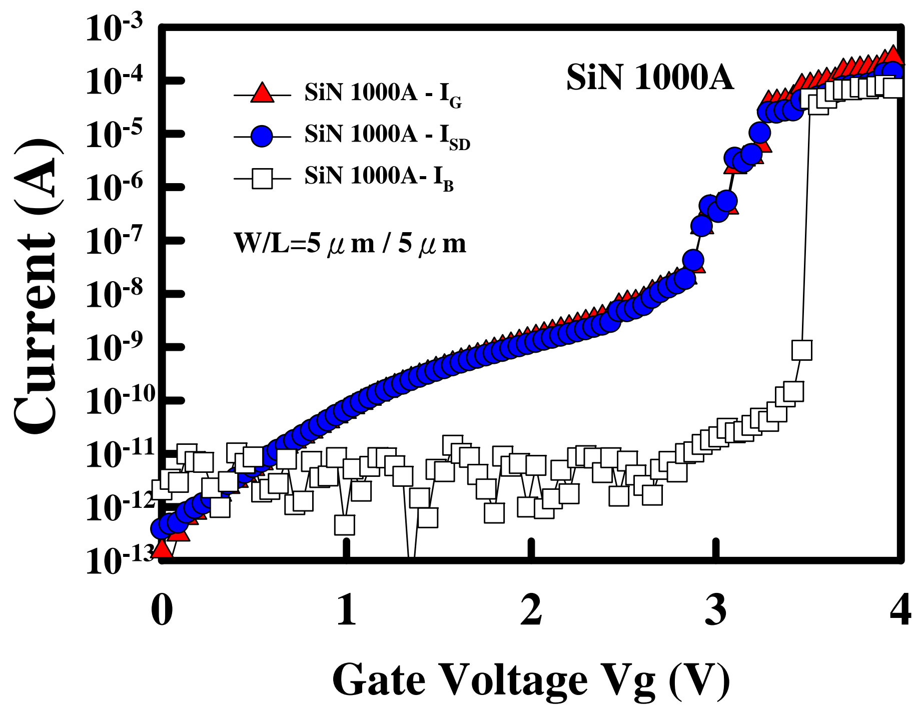


(a)

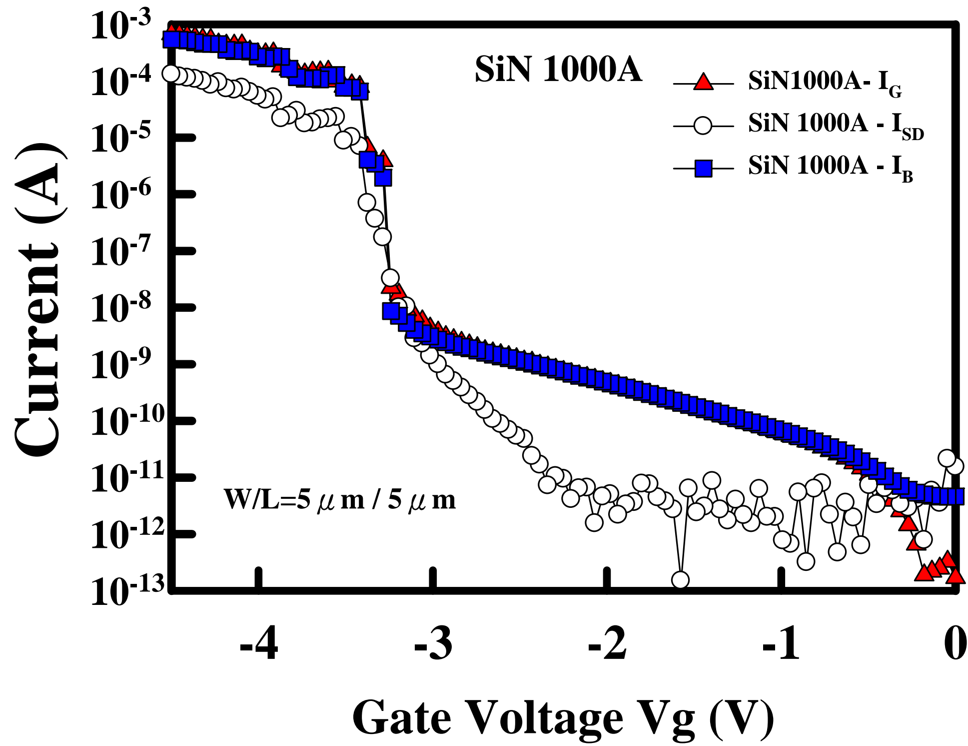


(b)

Fig 3-21 Carrier separation for HfAlO without SiN under (a) inversion (b) accumulation

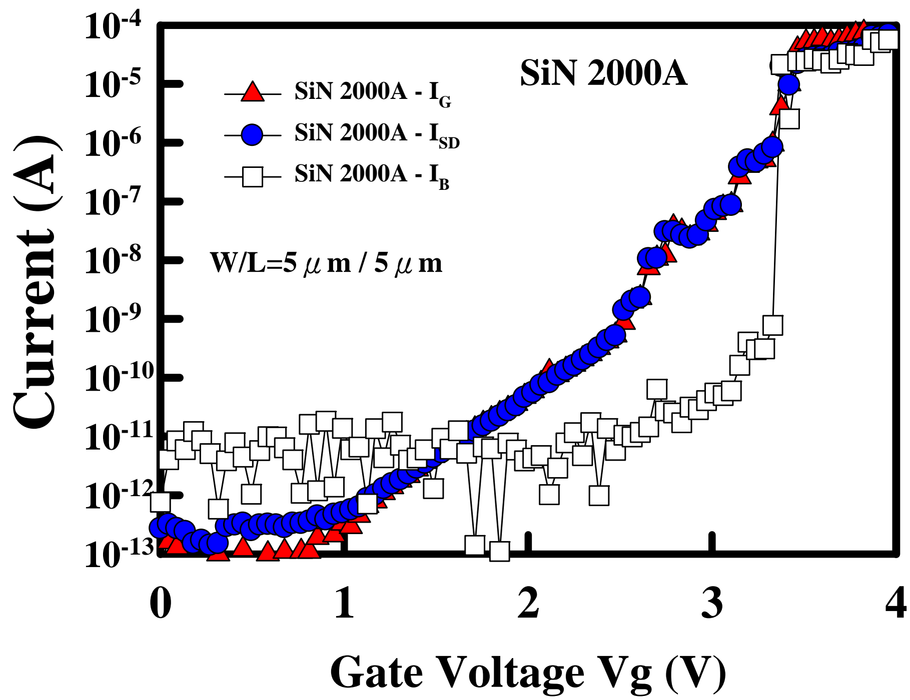


(a)

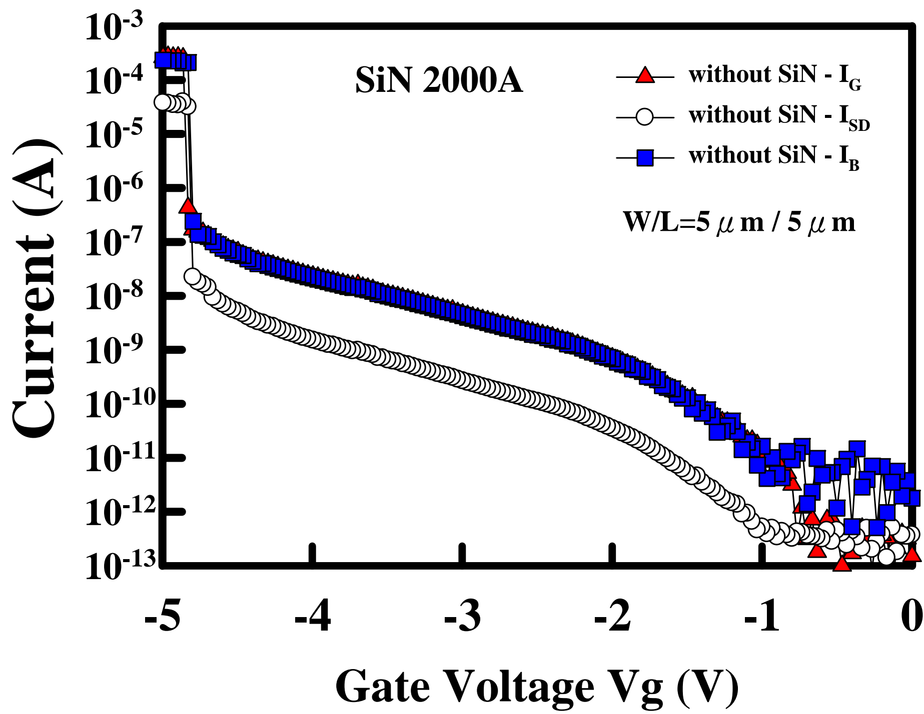


(b)

Fig 3-22 Carrier separation for HfAlO with SiN 1000A under (a) inversion (b) accumulation

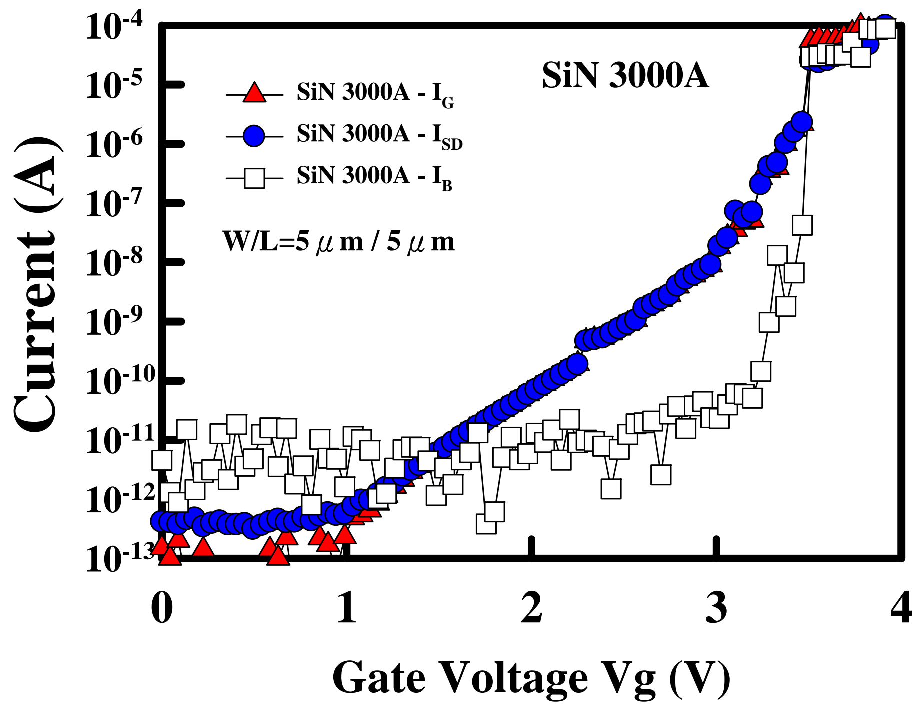


(a)

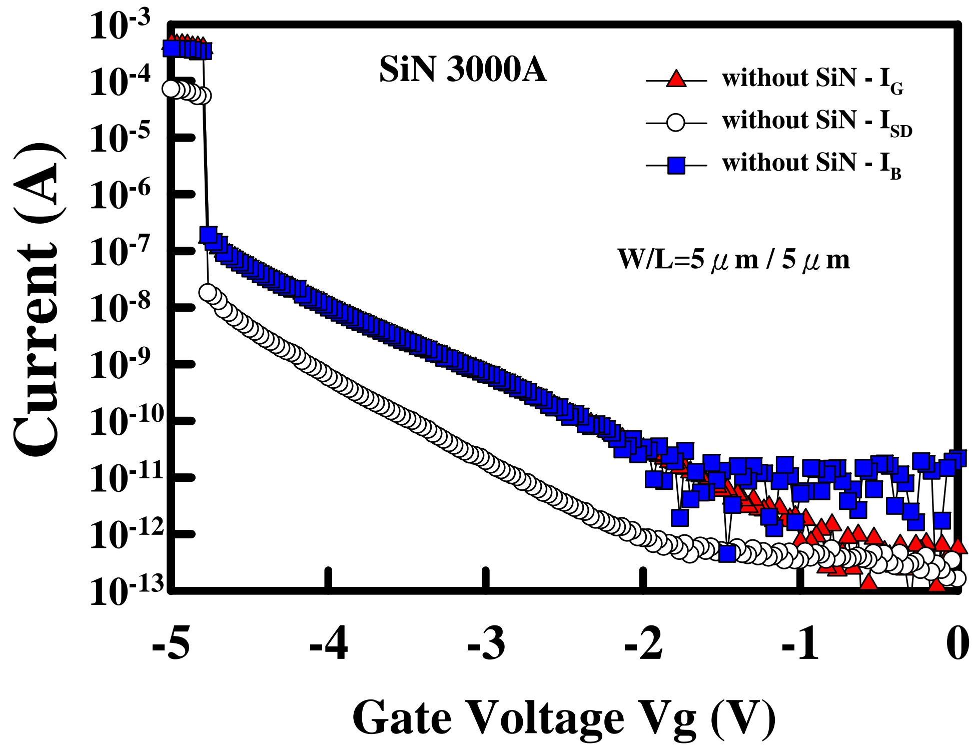


(b)

Fig 3-23 Carrier separation for HfAlO with SiN 2000A under (a) inversion (b) accumulation

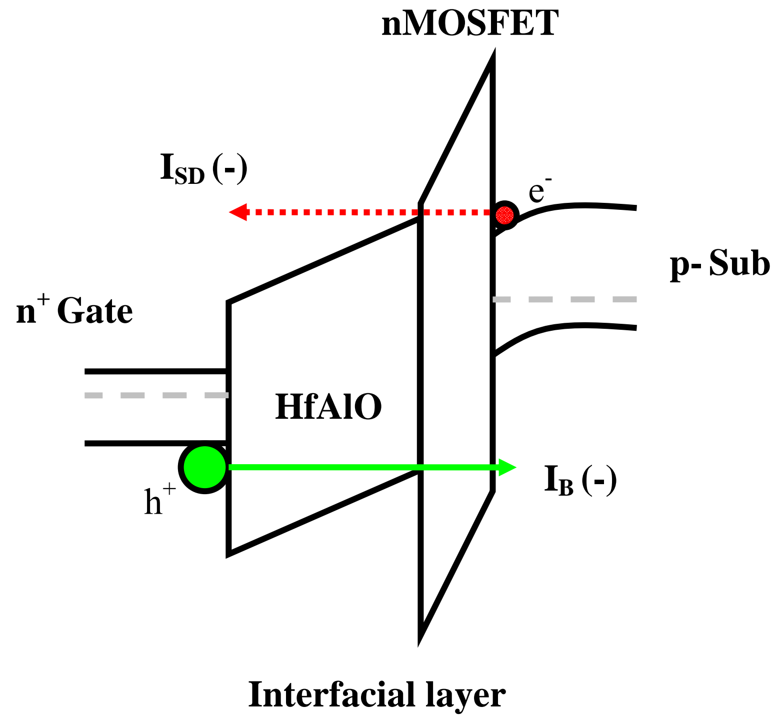


(a)

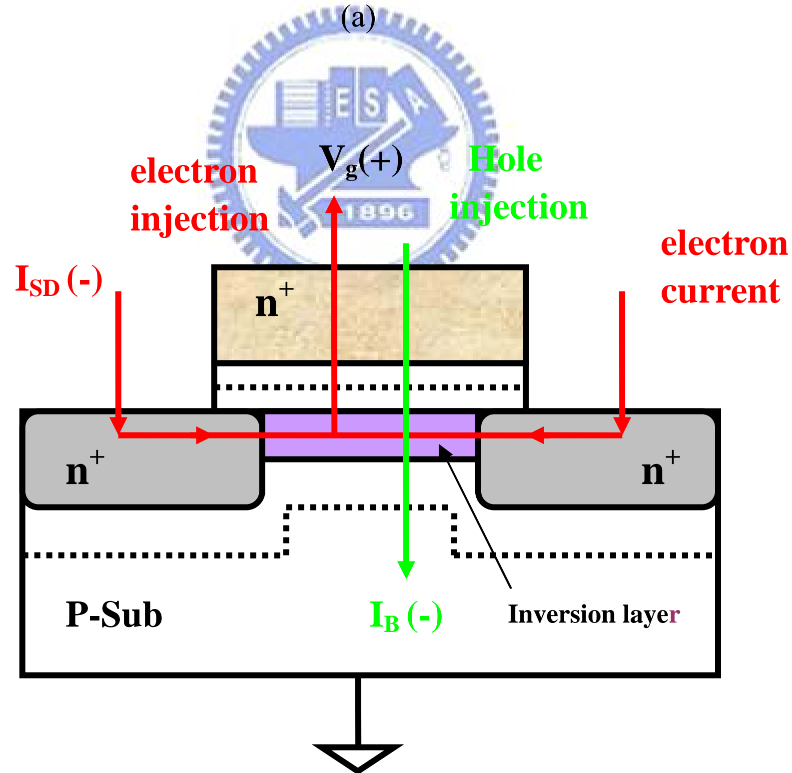


(b)

Fig 3-24 Carrier separation for HfAlO with SiN 3000A under (a) inversion (b) accumulation

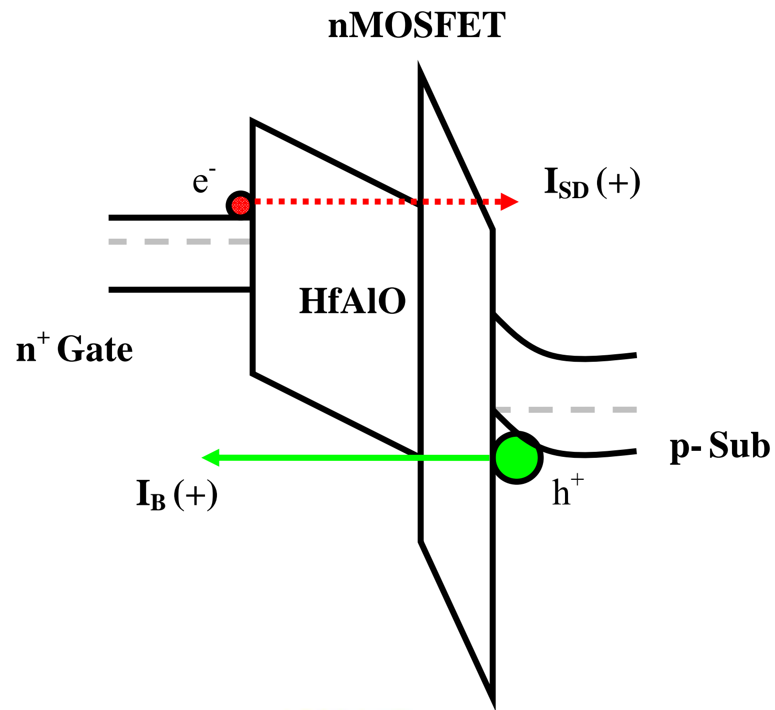


(a)

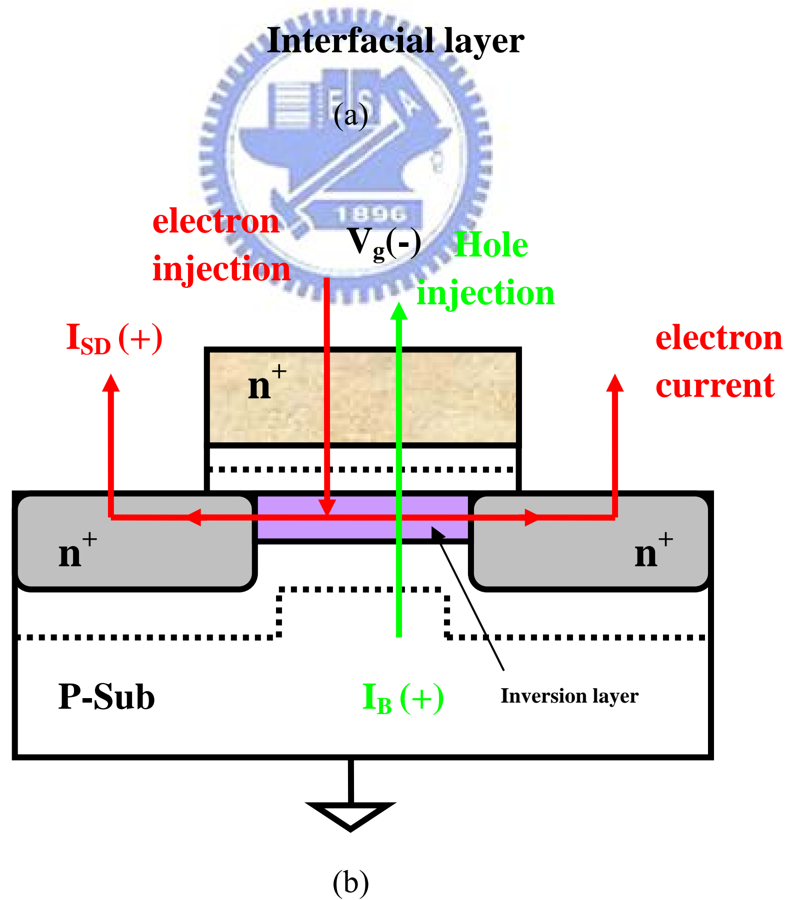


(b)

Fig 3-25 n+-gated nMOSFET with HfAlO/SiON gate stack under inversion region (a) Band diagrams, and (b) Schematic illustration of carrier separation experiment.



(a)



(b)

Fig 3-26 n+-gated nMOSFET with HfAlO/SiON gate stack under accumulation region (a) Band diagrams, and (b) Schematic illustration of carrier separation experiment.

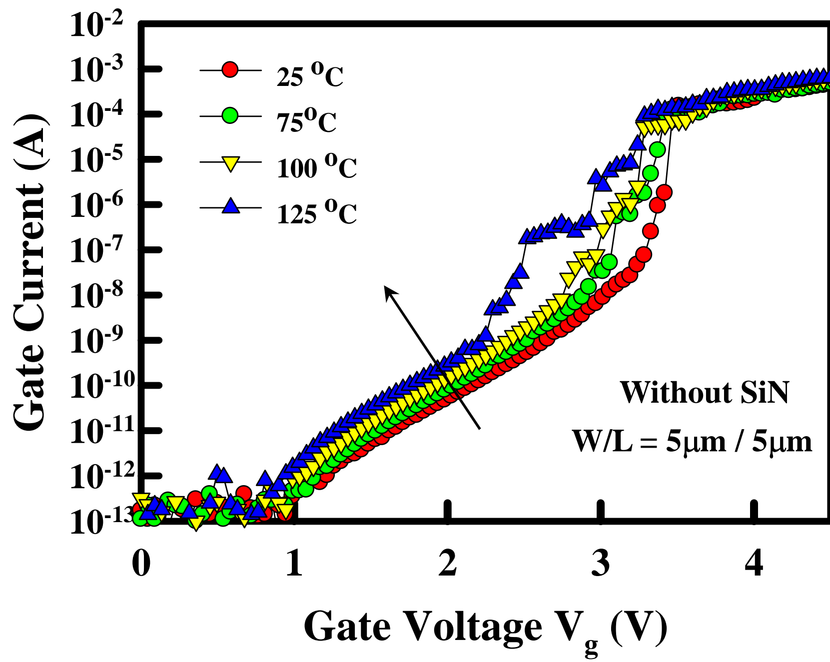


Fig 3-27 Gate leakage current versus gate bias without SiN for fresh n-channel devices at various temperatures

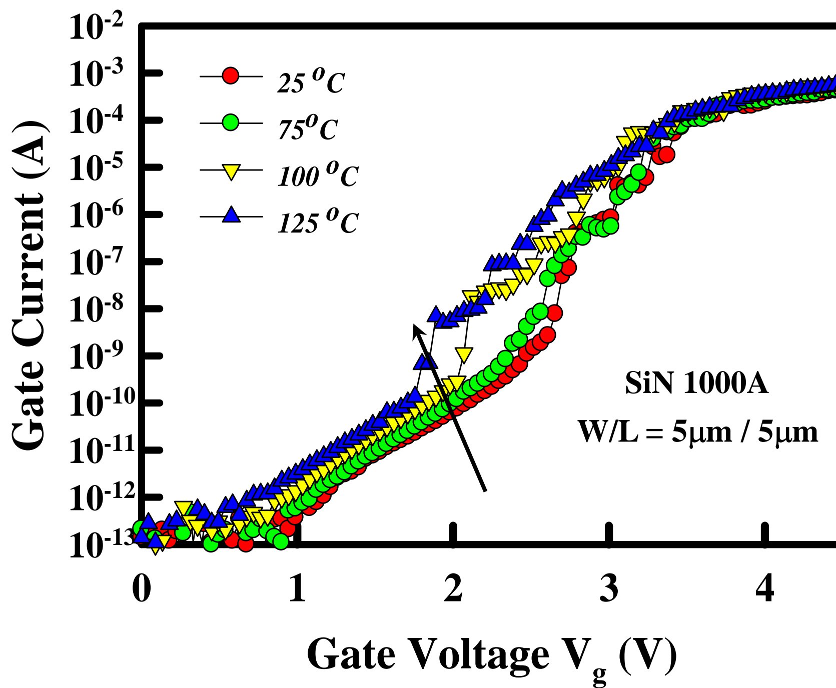


Fig 3-28 Gate leakage current versus gate bias with SiN 1000A for fresh n-channel devices at various temperatures

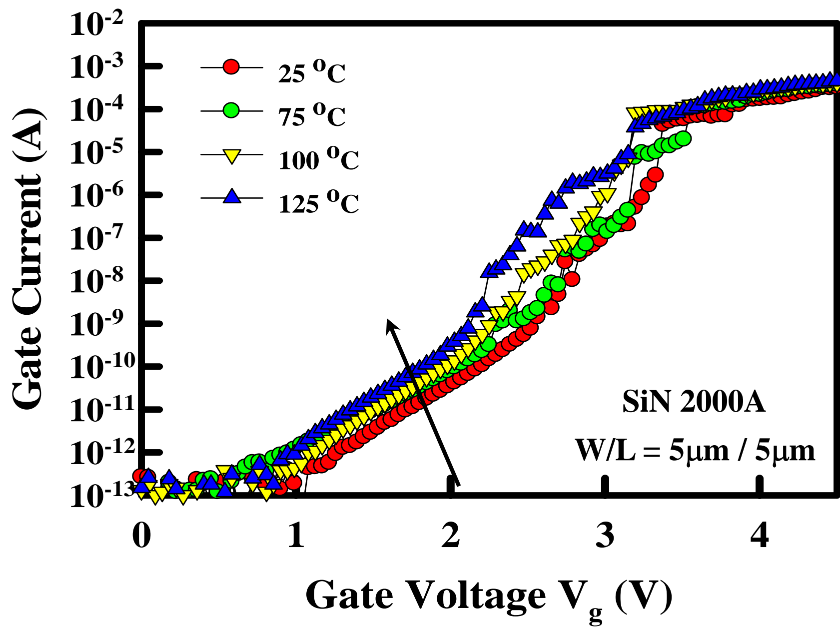


Fig 3-29 Gate leakage current versus gate bias with SiN 2000A for fresh n-channel devices at various temperatures

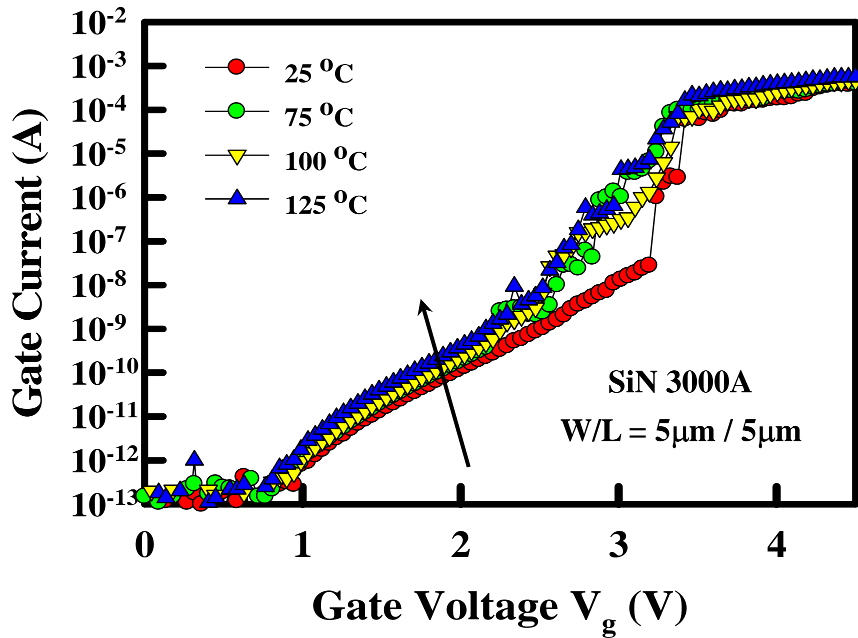


Fig 3-30 Gate leakage current versus gate bias with SiN 3000A for fresh n-channel devices at various temperatures

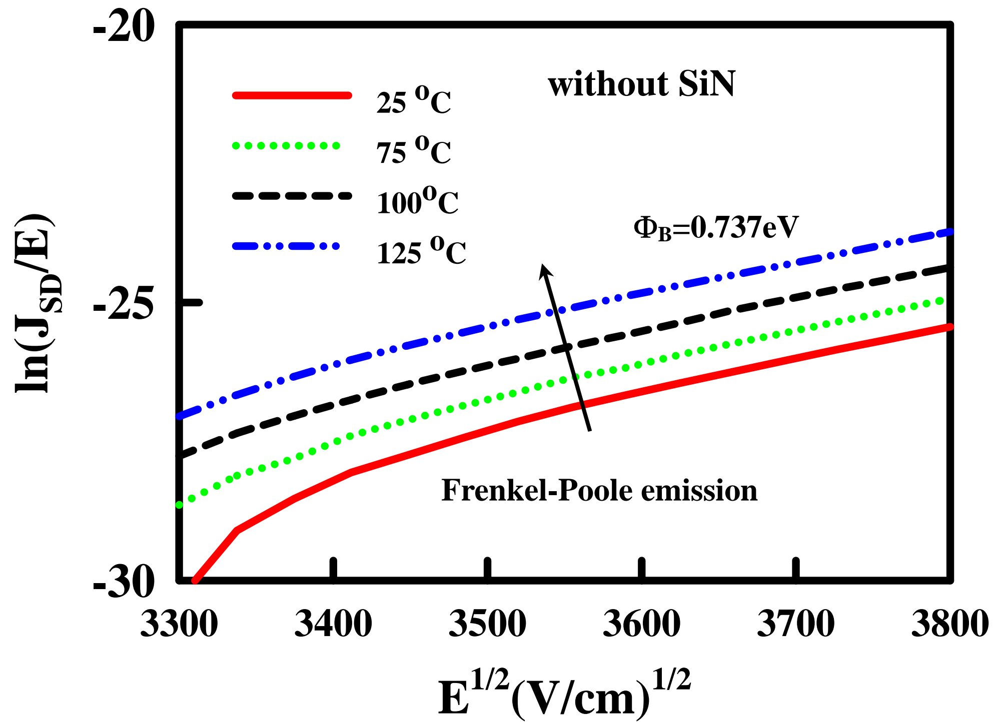


Fig 3-31 Conduction mechanism for source/drain current fitting under inversion region without SiN

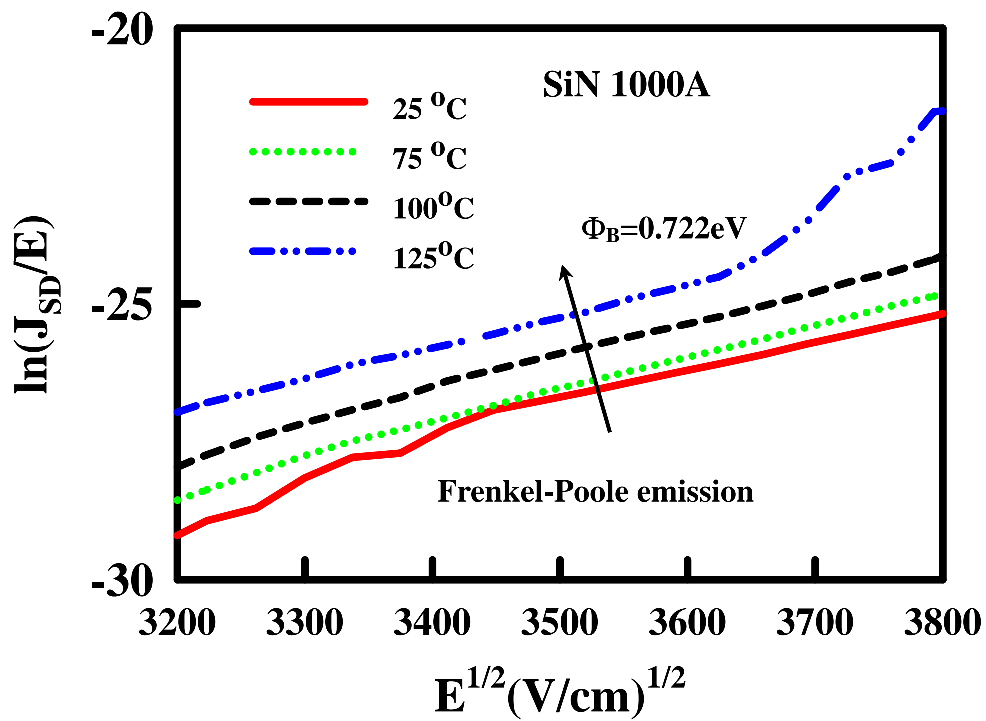


Fig 3-32 Conduction mechanism for source/drain current fitting under inversion region with SiN 1000A

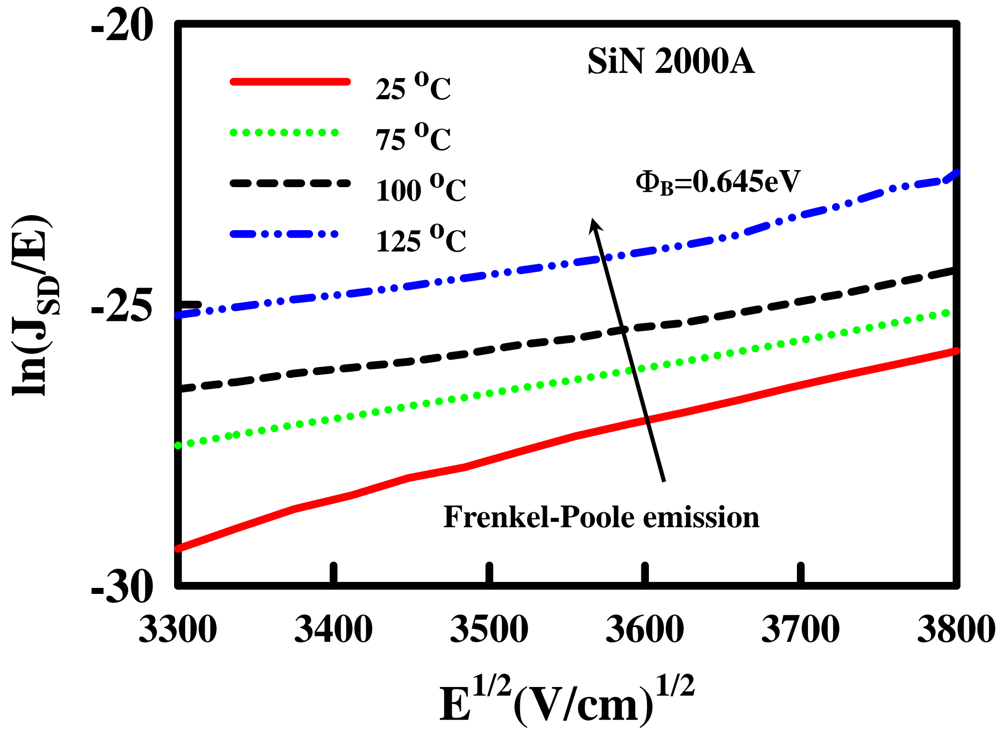


Fig 3-33　Conduction mechanism for source/drain current fitting under inversion region with SiN 2000A

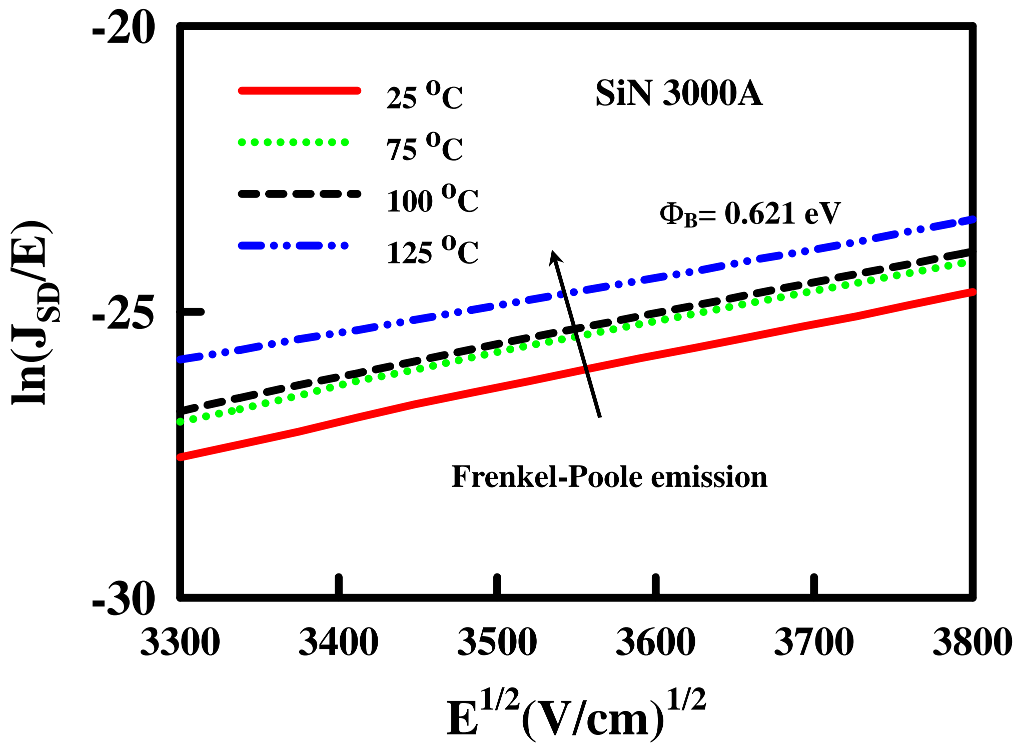


Fig 3-34　Conduction mechanism for source/drain current fitting under inversion region with SiN 3000A

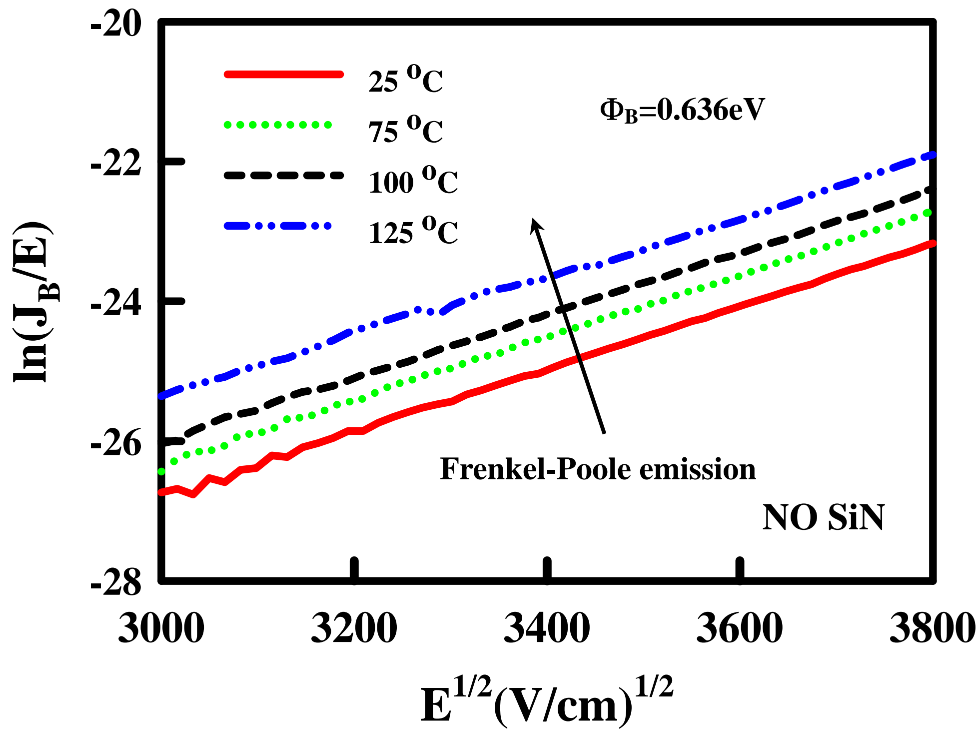


Fig 3-35 Conduction mechanism for substrate current fitting under inversion region without SiN

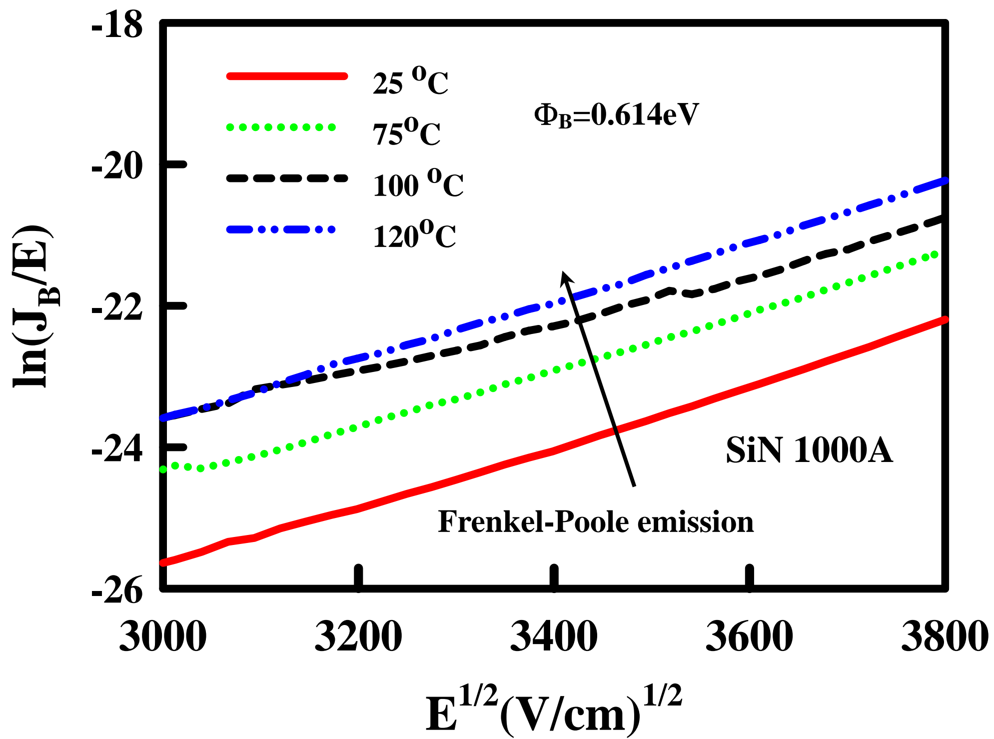


Fig 3-36 Conduction mechanism for substrate current fitting under inversion region with SiN 1000A

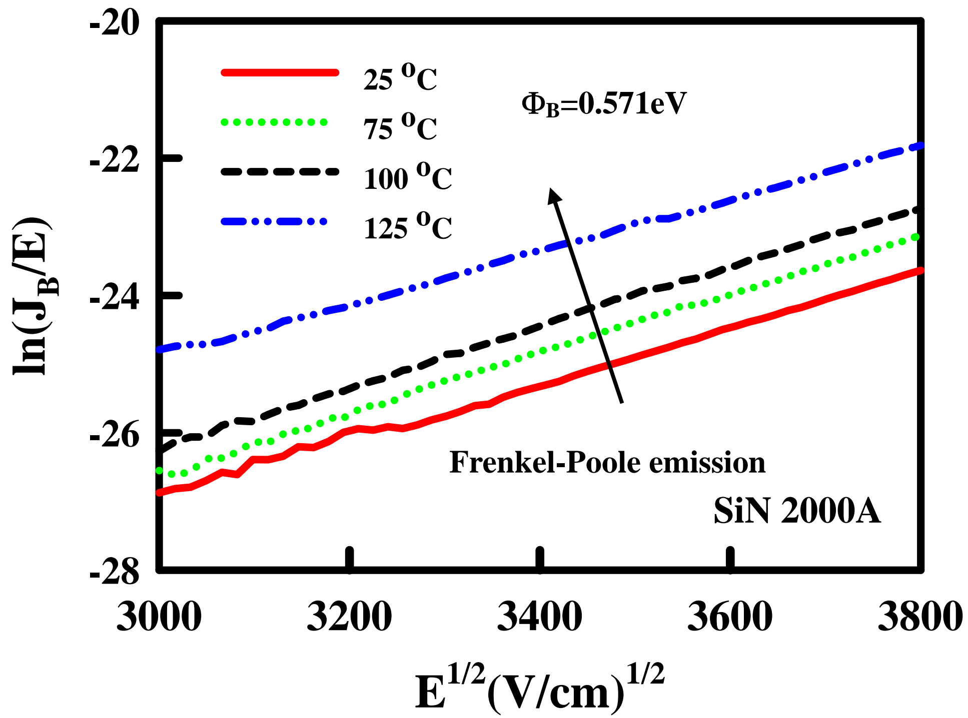


Fig 3-37 Conduction mechanism for substrate current fitting under inversion region with SiN 2000A

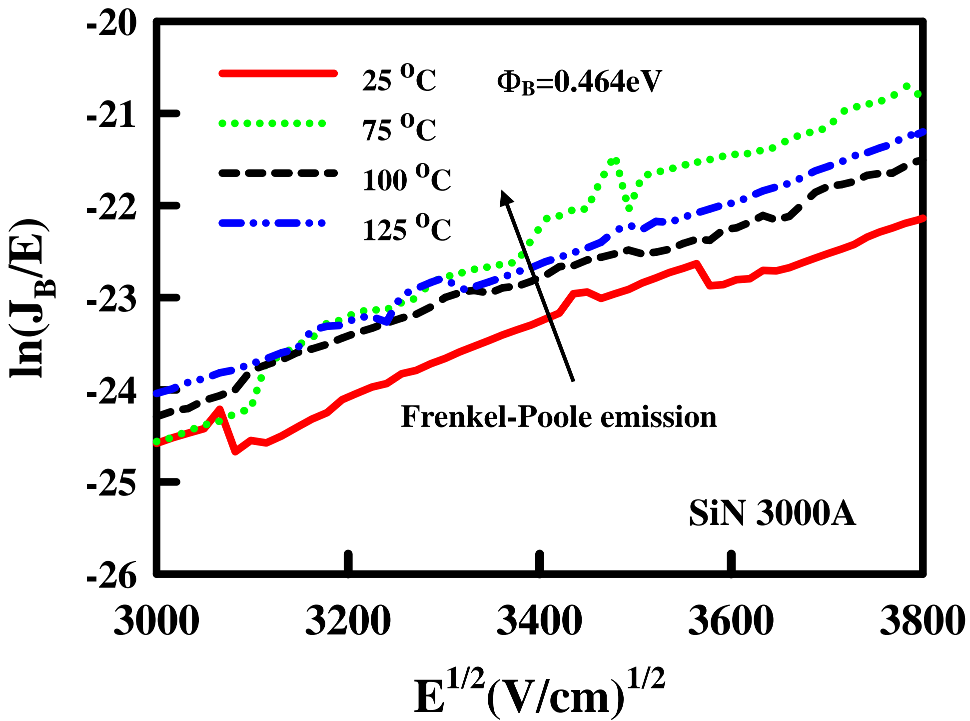


Fig 3-38 Conduction mechanism for substrate current fitting under inversion region with SiN 3000A

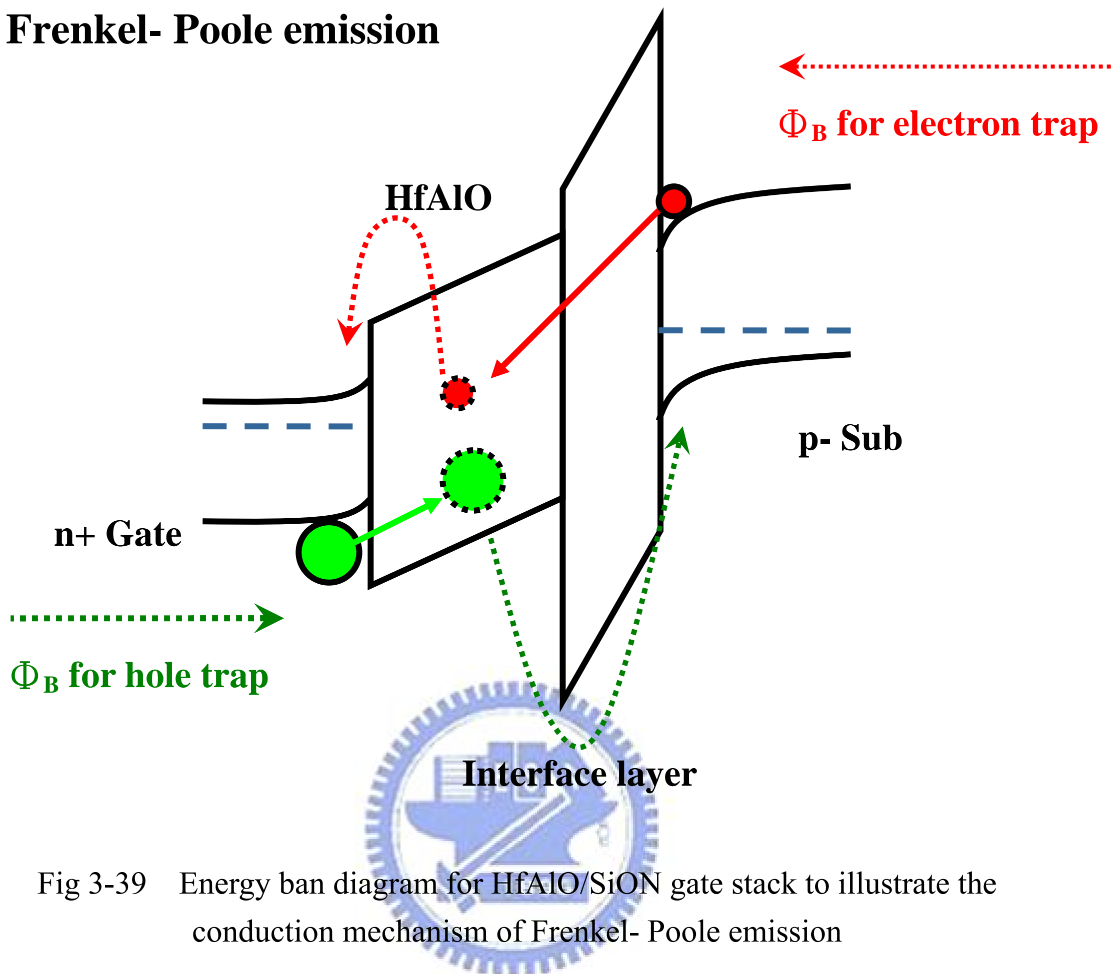


Fig 3-39 Energy ban diagram for HfAlO/SiON gate stack to illustrate the conduction mechanism of Frenkel- Poole emission

SiN capping Layer thickness	No SiN	SiN 1000	SiN 2000	SiN 3000
Φ_B for electron trap	0.737	0.722	0.645	0.621
Φ_B for hole trap	0.636	0.614	0.571	0.464

Fig 3-40 The result of electron and hole trap with different SiN capping layer

Chapter 4
Reliability of MOSFETs with HfO_2/SiON Gate Stack

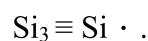
4-1 Introduction

Recently, mobility enhancement by channel strain engineering has emerged as an effective approach to boost the performance of scaled devices, especially local-strain technology [38,39]. A method to introduce tensile strain for nMOSFET and compressive strain for pMOSFET is to add a SiN capping layer deposited by plasma-enhanced CVD (PECVD) [40,41]. Though strained channel could enhance the mobility and the drive current of the device, but potentially it could also degrade the device's reliability characteristics. From the results presented in Chapter 3, hydrogen species unintentionally incorporated in the thin stress-induced film may also adversely affect the device reliability characteristics. The device reliability issue is therefore a potential concern when the local strain is introduced, and should therefore be carefully addressed. Negative bias temperature instability (NBTI) is well known as the lifetime-limiting reliability concerns in CMOS devices when the gate oxide thickness is scaled to 3.5 nm and below (worse than PBTI in nMOSFET) [42]. Conventionally, characterization of NBTI is primarily based on static experimental

data. However, for real-life operations of digital circuits, the applied bias to the gate of pMOSFET in a CMOS inverter is being switched between "high" and "low" voltages incessantly. In line with this, the evaluation of the dynamic NBTI (DNBTI) characteristics seems to be more practical for reliability characterization. In this aspect, it has been reported that the dynamic NBTI (DNBTI) effect greatly prolongs the lifetime of pMOSFET operating in a practical digital circuit [43]. A physical model has also been proposed for DNBTI involving the interaction of the released hydrogen re-passivating Si dangling bonds during the passivation time [44]. However, reports on DNBTI of devices with SiN capping are lacking. In this work we investigate the issue by performing dynamic and AC stress measurements on pMOSFET with a compressively strained channel.

4-2 Brief Review of NBTI

Negative Bias Temperature Instability (NBTI) has been known since the very early days of MOS device development, have been observed as early as 1976 [45]. As the oxide thickness is scaled to nanometer, hot carrier effects become less important due to the reduced operation voltage [46]. NBTI refers to the generation of positive oxide charge and interface traps under negative gate bias at elevated temperatures. The interface trap density induced by NBTI increases with decreasing dielectric thickness, whereas the fixed oxide charge induced by NBTI appears to have no thickness dependence. The shift in threshold voltage and degradation in transconductance have been suggested to be due to the interfacial electrochemical reactions related to the holes from the channel inversion layer for pMOSFET. When the Si is oxidized, the bonding configuration at the surface is as shown in Fig 4-1 (a) and 4-1 (b) with most Si atoms bonded to oxygen at the surface. Some Si atoms bond to hydrogen. An interface trapped charge, often called interface trap, is an interface trivalent Si atom with an unsaturated (unpaired) valence electron at the SiO2 /Si interface. It is usually denoted by

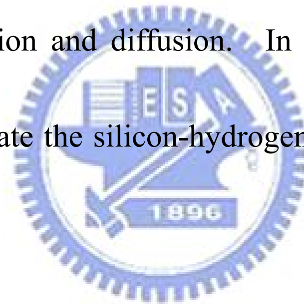


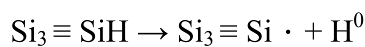
$Si_3 \equiv Si \cdot$.

The ≡ represents tree complete bonds other Si atoms and · indicates the fourth, unpaired electron in a dangling bond. Interface traps are designated as $D_{it}(cm^{-2}\ eV^{-1})$,

Q_{it}(C/cm^2), and N_{it}(cm^{-2}) and they are acceptor-like in the upper half and donor-like in the lower half of the band as shown in Fig 4-2 for pMOSFET and Fig 4-3 for nMOSFET respectively. Since the fixed oxide charge (Q_f) is positive, we have at inversion：n channel：(Q_f - Q_{it}), p channel：(Q_f + Q_{it}), hence pMOSFET have more serious degradation in NBTI.

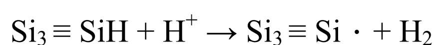
We discuss the two basic approaches for modeling interface trap generation during NBTI process. The first models discuss trap creation via hydrogen interaction dynamics. The second set of models describes more general trap creation via chemical species interaction and diffusion. In first models, it indicates that a high electric field can dissociate the silicon-hydrogen bond, then, it can be modeling as equation





$Si_3 \equiv SiH \rightarrow Si_3 \equiv Si \cdot + H^0$

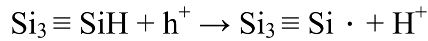
where H^0 is a neutral interstitial hydrogen atom or atomic hydrogen. Recently first –principles calculations show that the positively charged hydrogen or proton H+ is the only stable state of hydrogen at the interface and that H+ reacts directly with the SiH to form an interface trap, it also can be written as



$Si_3 \equiv SiH + H^+ \rightarrow Si_3 \equiv Si \cdot + H_2$

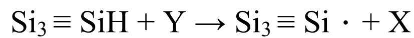
the mobile positive H^+ migrates towards the negatively charged dipole region if SiH molecule. The H^+ atom then reacts with the H^- to form H_2 leaving behind a

positively charged Si dangling bond. A different model is used to describe NBTI via the interaction of SiH with "hot hole" or holes near the interface. It is given by



$Si_3 \equiv SiH + h^+ \rightarrow Si_3 \equiv Si \cdot + H^+$

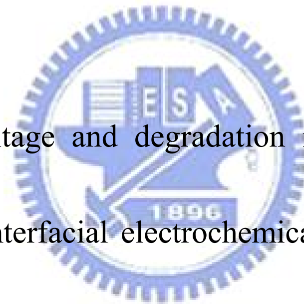
Another model, reaction and diffusion model, is



$Si_3 \equiv SiH + Y \rightarrow Si_3 \equiv Si \cdot + X$

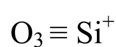
this model assumes that species Y diffuses to the interface and creates an interface trap, where Y is unknown. In this model, stress results in a negative shift in threshold voltage showing a power-law dependence on stress time:

$\Delta V_{th} = At^b$



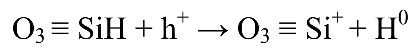
The shift in threshold voltage and degradation in transconductance have been suggested to be due to the interfacial electrochemical reactions related to the holes from the channel inversion layer. The exponential value of the power law equation is about 0.25, which could be explained by the diffusion-controlled electrochemical reactions.

Fixed oxide charge are designated as Q_f (C/cm^2) and N_f (cm-^{2}). The fixed oxide charge is a charge near the dielectric/Si interface, contributing mainly to threshold voltage shift. Q_f is also a byproduct trivalent Si defect in the oxide, denoted by



$O_3 \equiv Si^+$

Q_f generation can be modeled as



$$O_3 \equiv SiH + h^+ \rightarrow O_3 \equiv Si^+ + H^0$$

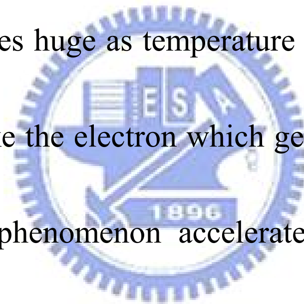
according this model, we can determine that the fixed oxide charges are generated from the dissociation of SiH bonds.

4-3 Reliability of MOSFETs with HfO_2/SiON gate stack

Fig 4-4 expresses I_d-V_g characteristics before stress and after stress 1000s with SiN (blue line) and without SiN (red line) capping layer at room temperature. We can know that no serious degradation of subthreshold swings both in with and without SiN capping layer but a positive V_{th} shift after stress is observed obviously. It indicates that there is no serious interface trap generation during stress process because interface trap generation can cause the subthreshold swing degradation. Instead, electron trapping in gate dielectrics is the mainly cause of threshold voltage shift after stress, and we can find the threshold voltage shift in with-SiN capping layer is larger than in without-SiN capping layer, it means that the strain which caused by depositing SiN capping layer will degrade the reliability of device.

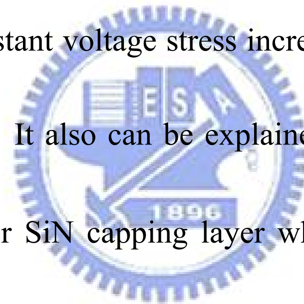
Fig 4-5 shows that the threshold voltage shift as a function of stress time for HfO_2 nMOSFETs without SiN, Fig 4-6 shows that the threshold voltage shift as a function of stress time for HfO_2 nMOSFETs with SiN 1000A, Fig 4-7 shows that the threshold voltage shift as a function of stress time for HfO_2 nMOSFETs with SiN 2000A, Fig 4-8 shows that the threshold voltage shift as a function of stress time for HfO_2 nMOSFETs with SiN 3000A. In above figurations, we can find that the threshold voltage shift become huge as the constant voltage stress increases, and the carrier trapped by gate dielectric bulk is electron due to the threshold voltage shift is

postive. It may be attributed that more electron-hole pairs which generate in channel region and tunnel to the gate dielectrics and then turn to great threshold voltage instability. In the same way, we can obtain that the bulk traps in gate dielectric bulk almost occupy all of charges which calculate from threshold voltage shift. Fig 4-9 shows that the threshold voltage shift is as a function of stress time for HfAlO nMOSFETs without SiN capping layer under various temperature. Fig 4-10 shows that the threshold voltage shift is as a function of stress time for HfAlO nMOSFETs with SiN 1000A capping layer under various temperature. It can be seen that the the threshold voltage shift becomes huge as temperature increases. It may be attributed that the high temperature make the electron which generated from electron-hole pairs get higher energy and this phenomenon accelerates the electron trapped in gate dielectric. Fig 4-11 shows that the threshold voltage shift of HfO_2 nMOSFET is as a function of stress time which compares without SiN and with SiN 3000A under CVS 1.5V and CVS 2.5V. It also obtains the same result which we expect. The cause of serious degradation with thicker SiN capping layer could be explained as follows: One is that more Si-H bonds with thicker SiN capping layer which come from the reaction of SiH_4 and NH_3 precursor break when constant voltage stress applies. The other is great tensile strain as thickness of SiN capping increase, and it brings about more strain energy which is stored in the channel. [49-50] Fig 4-12 shows that the



Gm_max degradation rate with different SiN thickness. It can be seen that the Gm-_max degradation increased as the thickness of SiN thickened.

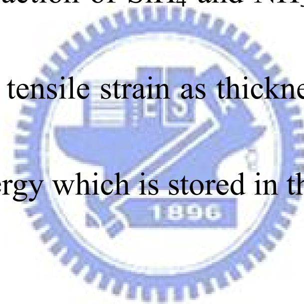
Fig 4-13 shows that the threshold voltage shift as a function of stress time for HfAlO nMOSFETs without SiN, Fig 4-15 shows that the threshold voltage shift as a function of stress time for HfAlO nMOSFETs with SiN 1000A, Fig 4-17 shows that the threshold voltage shift as a function of stress time for HfAlO nMOSFETs with SiN 2000A, Fig 4-19 shows that the threshold voltage shift as a function of stress time for HfAlO nMOSFETs with SiN 3000A. We also can find the threshold voltage shift become large as the constant voltage stress increases. The results are the same which compared with HfO_2. It also can be explained by two reason： One is that more Si-H bonds with thicker SiN capping layer which come from the reaction of SiH_4 and NH_3 precursor break when constant voltage stress applies. The other is great tensile strain as thickness of SiN capping increase, and it brings about more strain energy which is stored in the channel. Fig 4-14 shows that the threshold voltage shift is as a function of stress time for HfAlO nMOSFETs without SiN capping layer under various temperature. Fig 4-16 shows that the threshold voltage shift is as a function of stress time for HfAlO nMOSFETs with SiN 1000A capping layer under various temperature. Fig 4-18 shows that the threshold voltage shift is as a function of stress time for HfAlO nMOSFETs with SiN 2000A capping layer under

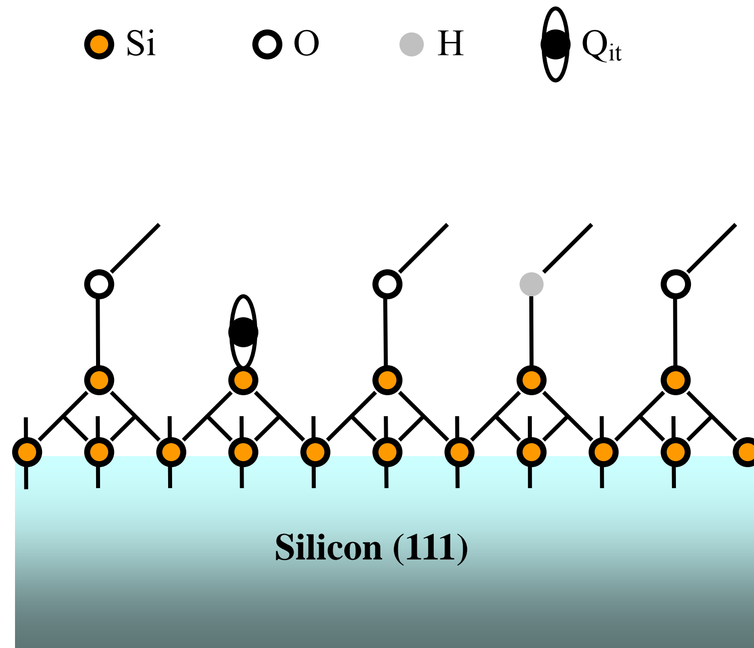


various temperature. Fig 4-20 shows that the threshold voltage shift is as a function of stress time for HfAlO nMOSFETs with SiN 3000A capping layer under various temperature. The results are also the same compared with HfO_2. The threshold voltage shift is more serious as the temperature increases. Fig 4-21 and Fig 4-22 express the threshold voltage shift as a function of stress time for HfAlO nMOSFETs with different SiN capping layer under CVS 2V at 25℃ and 125℃. We can find that the strain will cause the threshold voltage shift larger than without strain, even if at room temperature or 125℃. Therefore, we can sure that although the strain technique improves the driving current, the reliability is also be degraded. And Fig 3-23 reveals Gmmax degradation rate with different SiN thickness. It also obtains the same result which we expect.

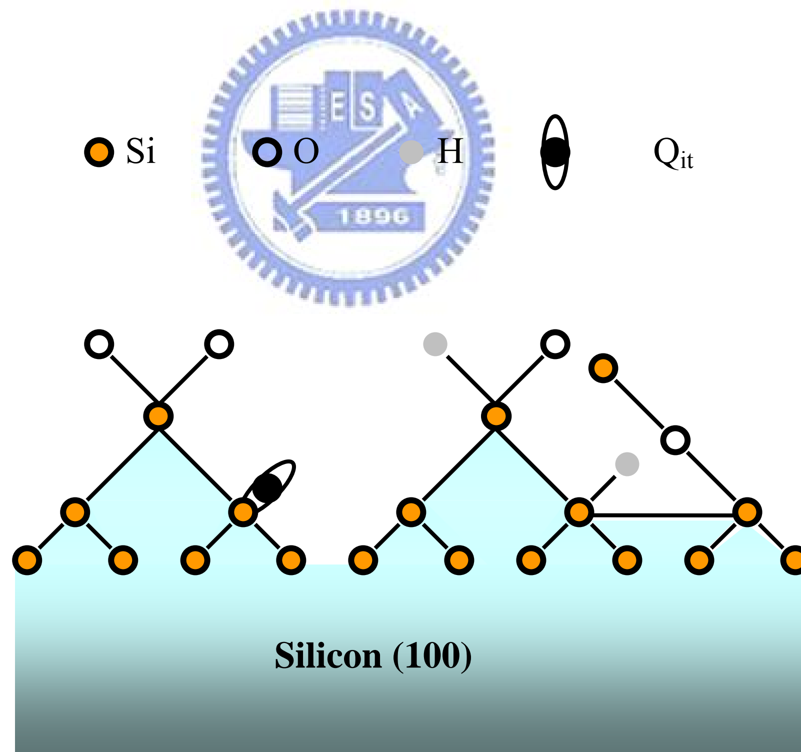
4-4 Summary

The CVS reliability of nMOSFETs with HfO_2/SiON and HfAlO/SiON is investigated in this chapter. The CVS under various temperature is also shown. It is believed that CVS degradation is related to the electron traps in gate dielectric. And therefore cause threshold voltage shift. We observe that serious degradation such as threshold voltage shift occurs as SiN capping layer thickens. And we also find that threshold voltage shift with high temperature is larger when the thickness of SiN thickness increases. It can be explained by more Si-H bonds with thicker SiN capping layer which come from the reaction of SiH_4 and NH_3 precursor break when constant voltage stress applies or great tensile strain as thickness of SiN capping increase, and it brings about more strain energy which is stored in the channel.





(a)



(b)

Fig 4-1 Bonding configuration at the surface of the (a) (111) Si surface and (b) (100) Si surface.

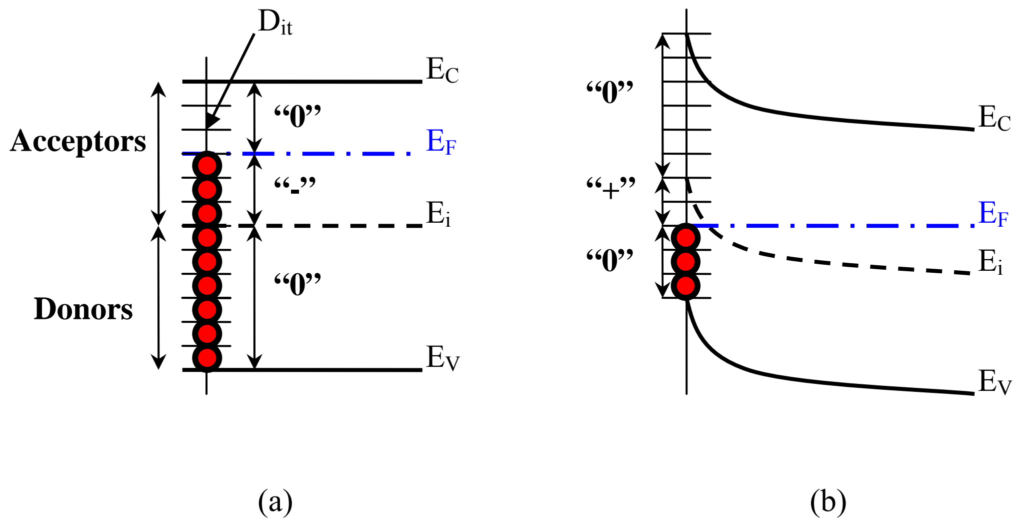


Fig 4-2 Band diagrams of the Si substrate of a p-channel MOS device (a) negative interface trap charge at flat-band and (b) positive interface trap charge at inversion.

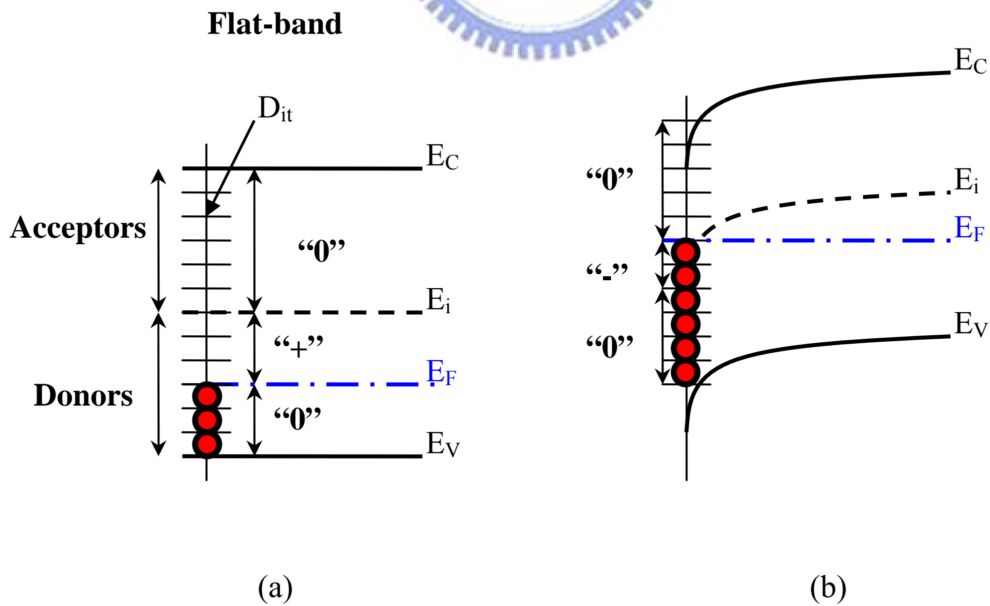


Fig 4-3 Band diagrams of the Si substrate of a n-channel MOS device (a) positive interface trap charge at flat-band and (b) negative interface trap charge at inversion.

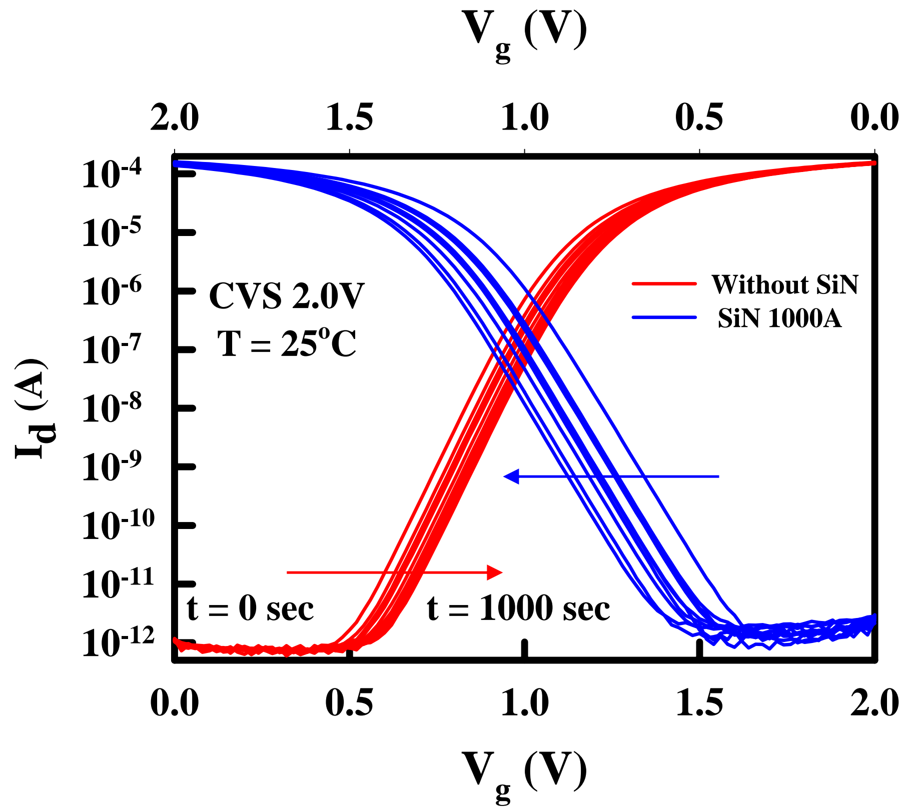


Fig 4-4 I_d-V_g for HfO_2 nMOSFETs before and after stress 1000s with and without SiN capping layer at room temperature.

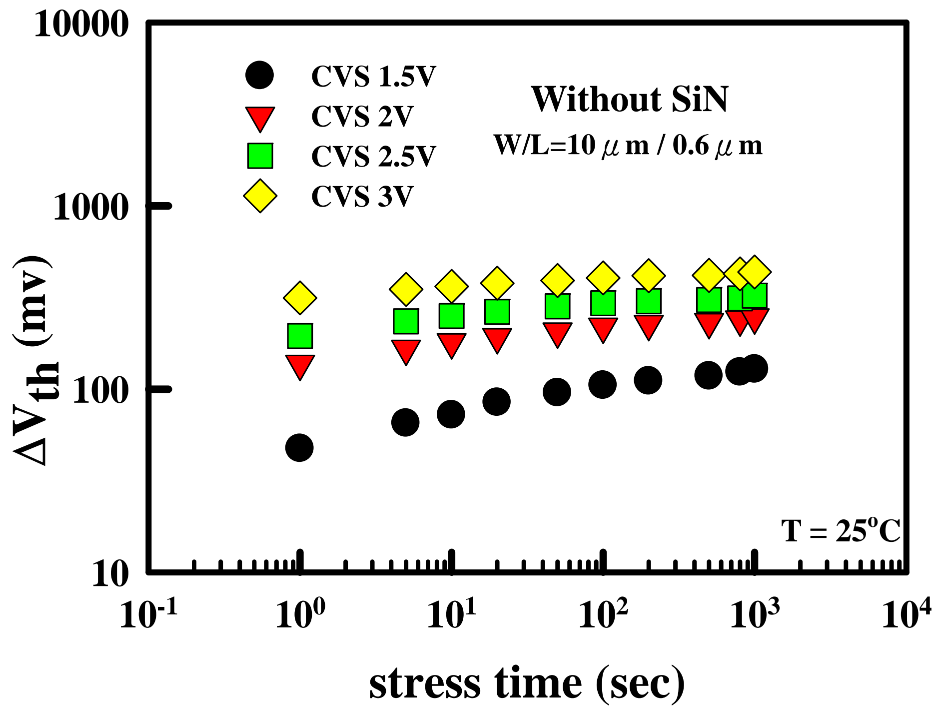


Fig 4-5 Threshold voltage shift (ΔV_{th}) as a function of stress time for HfO_2 nMOSFETs without SiN.

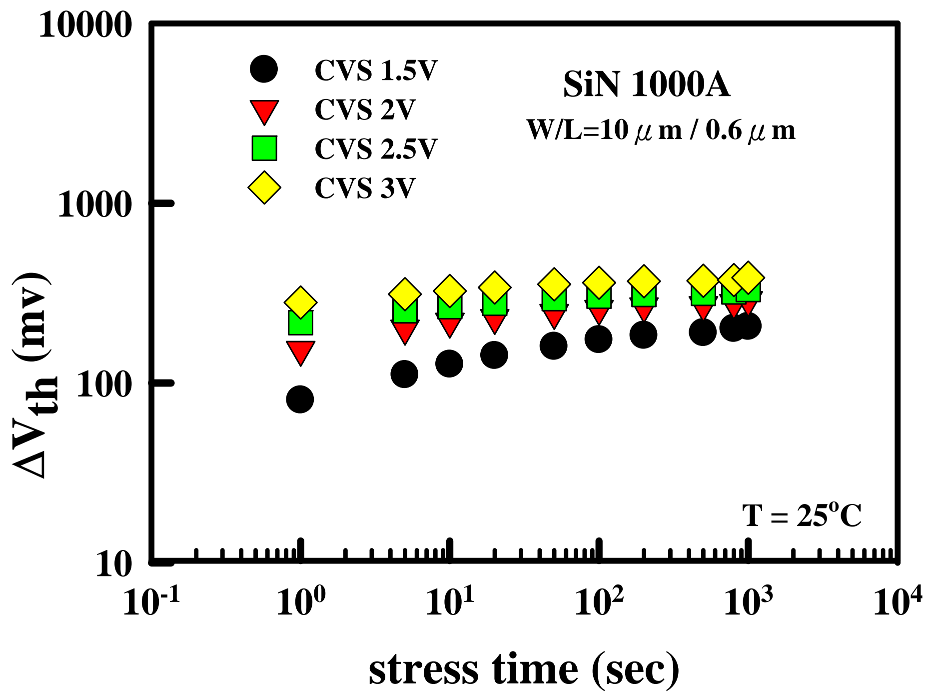


Fig 4-6 Threshold voltage shift (ΔV_{th}) as a function of stress time for HfO_2 nMOSFETs with SiN 1000A

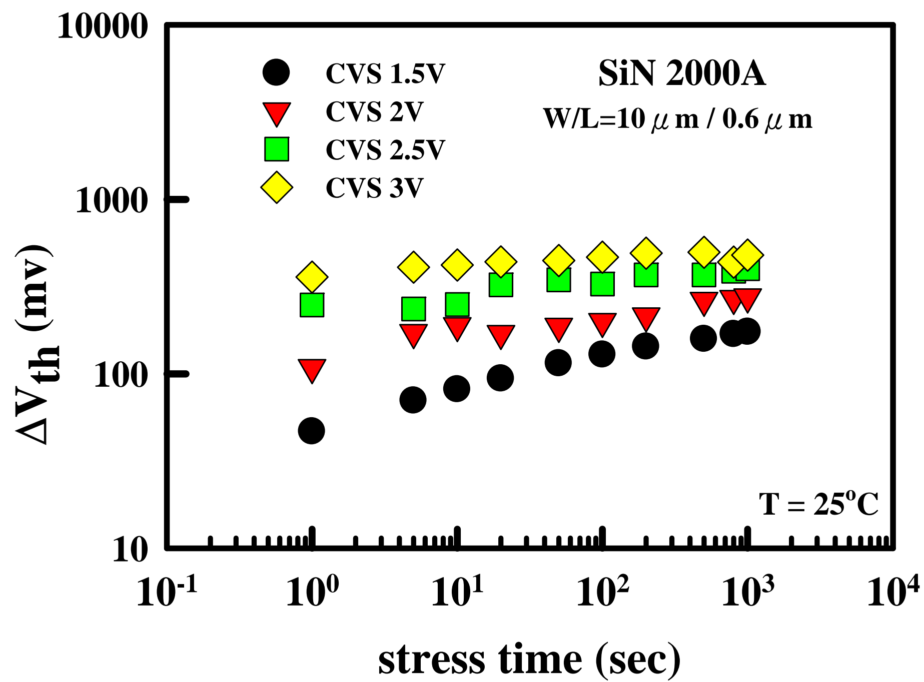


Fig 4-7 Threshold voltage shift (ΔV_{th}) as a function of stress time for HfO_2 nMOSFETs with SiN 2000A

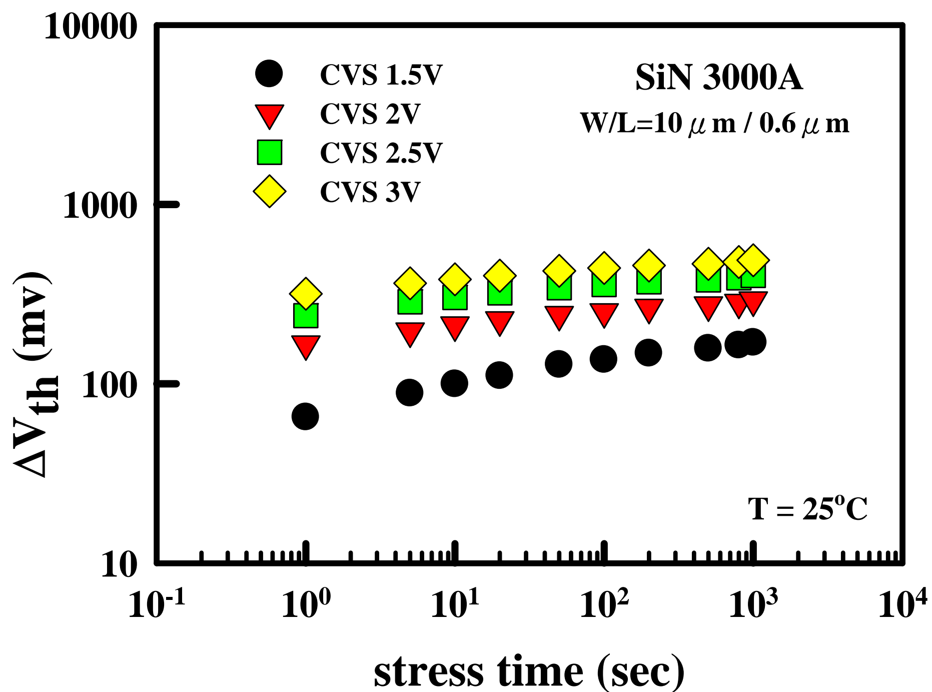


Fig 4-8 Threshold voltage shift (ΔV_{th}) as a function of stress time for HfO_2 nMOSFETs with SiN 3000A

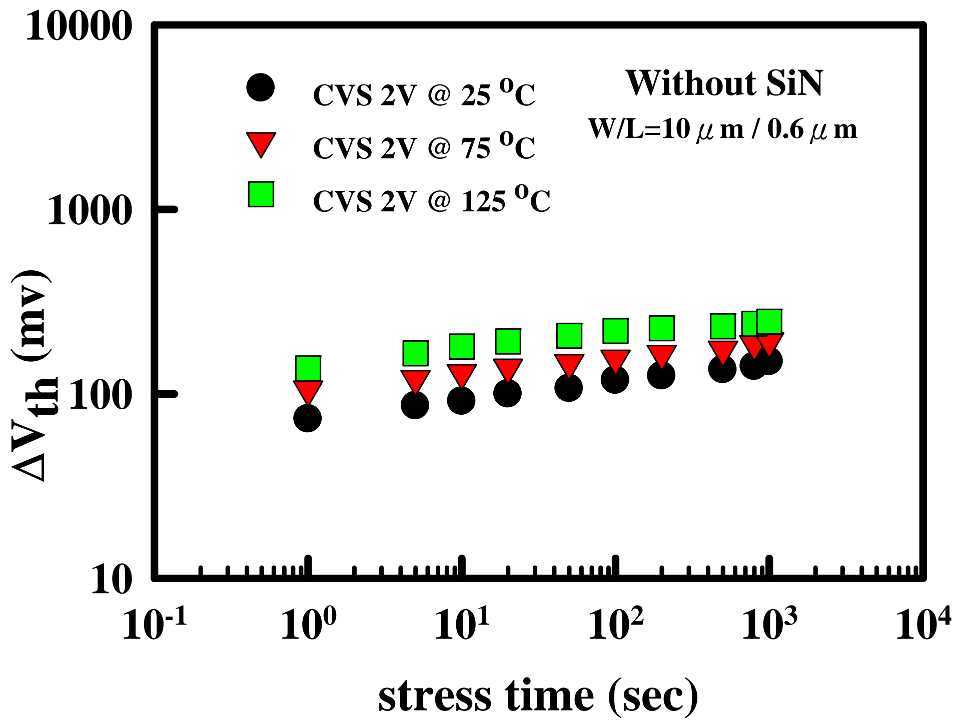


Fig 4-9 Threshold voltage shift (ΔV_{th}) as a function of stress time for HfO_2 nMOSFETs withoutSiN capping layer under various temperature

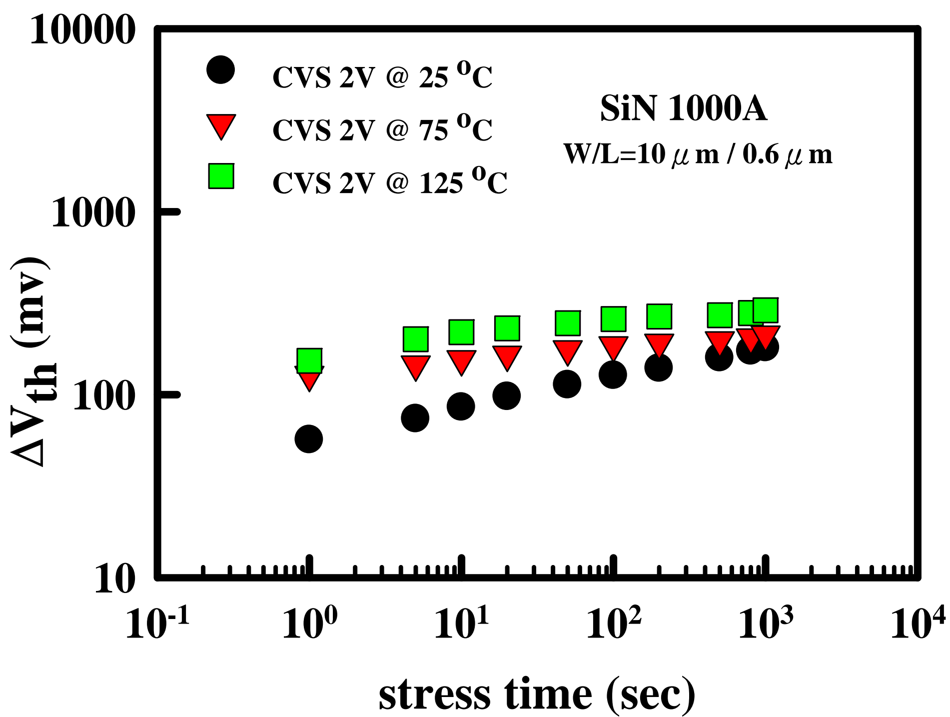


Fig 4-10 Threshold voltage shift (ΔV_{th}) as a function of stress time for HfO_2 nMOSFETs with SiN 1000A capping layer under various temperature

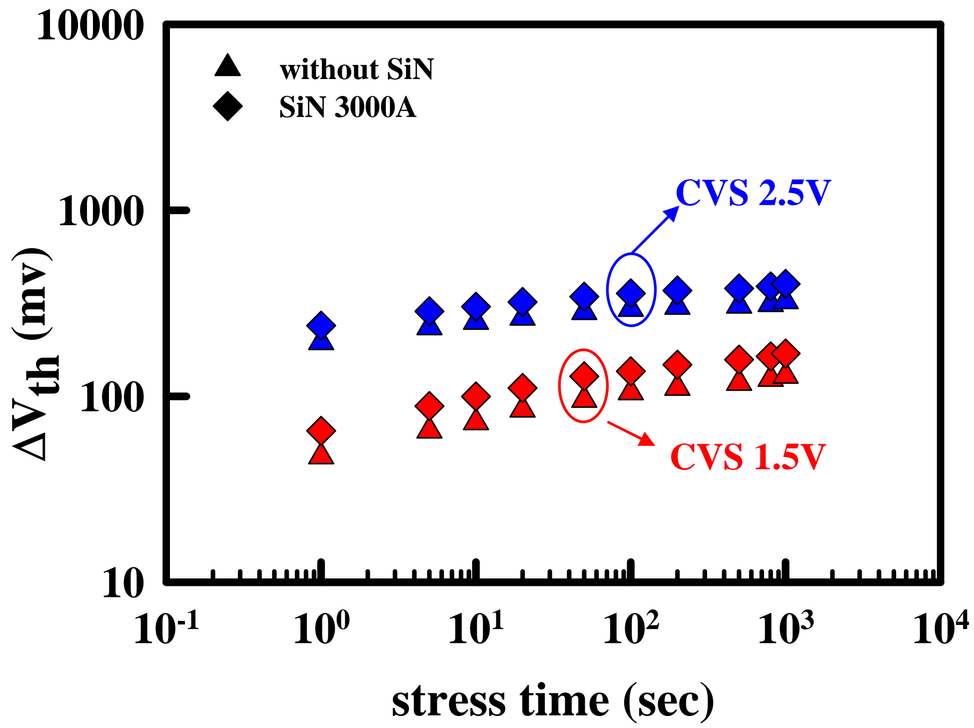


Fig 4-11 Threshold voltage shift (ΔV_{th}) of HfO_2 nMOS as a function of stress time which compares without SiN and with SiN 3000A under CVS 1.5V and CVS 2.5V

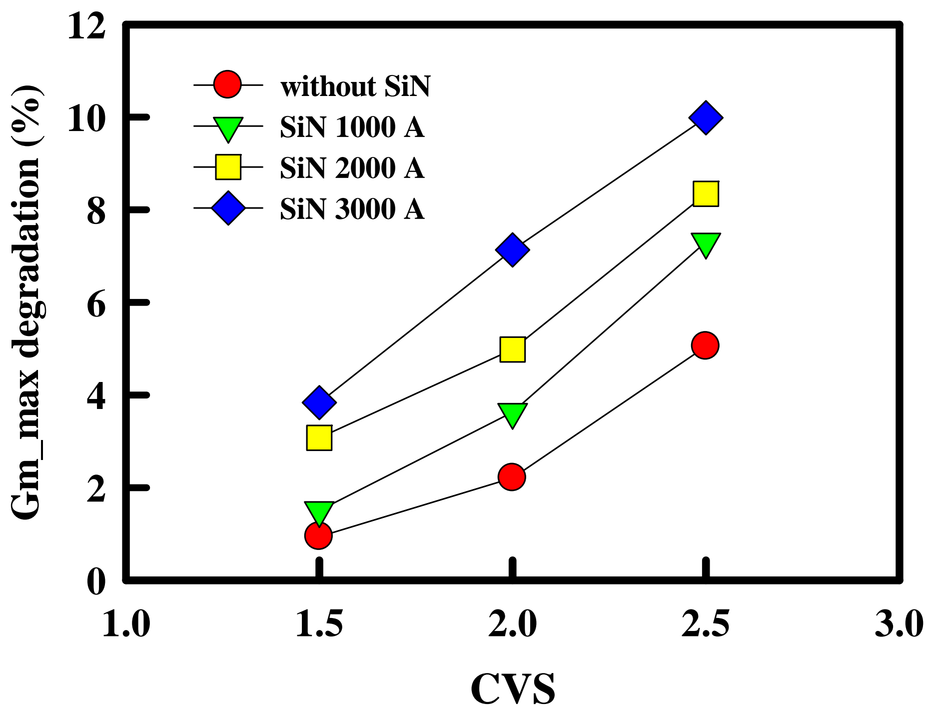


Fig 4-12 Gm_max degradation rate for HfO_2 nMOS with different SiN thickness after CVS 1000 sec

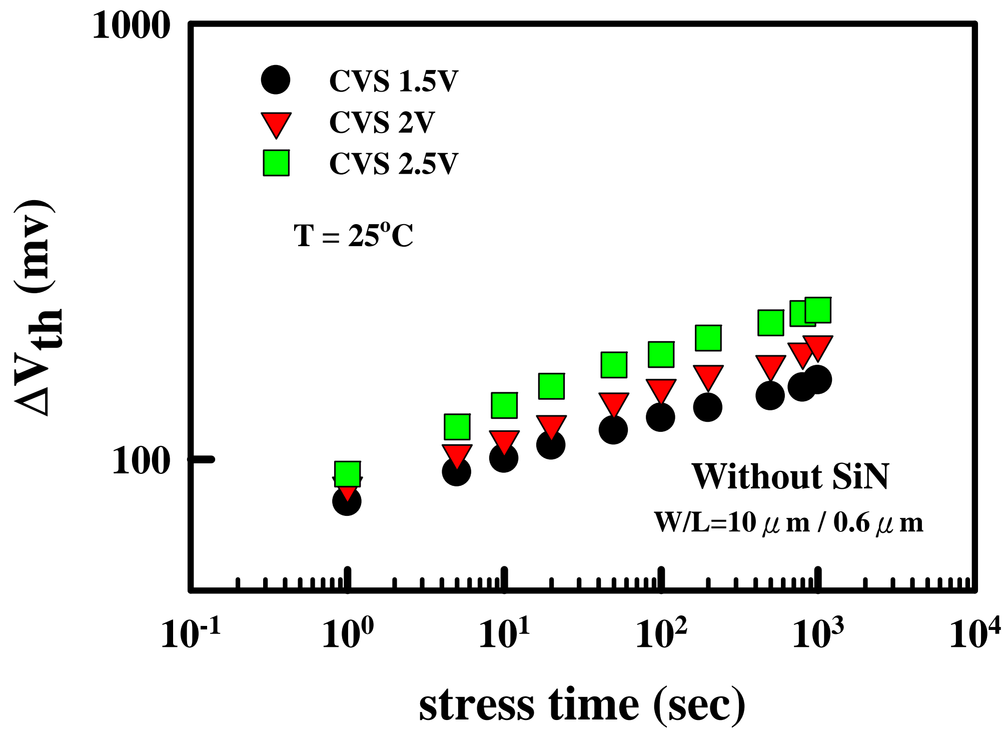


Fig 4-13 Threshold voltage shift (ΔV_{th}) as a function of stress time for HfAlO nMOSFETs without SiN

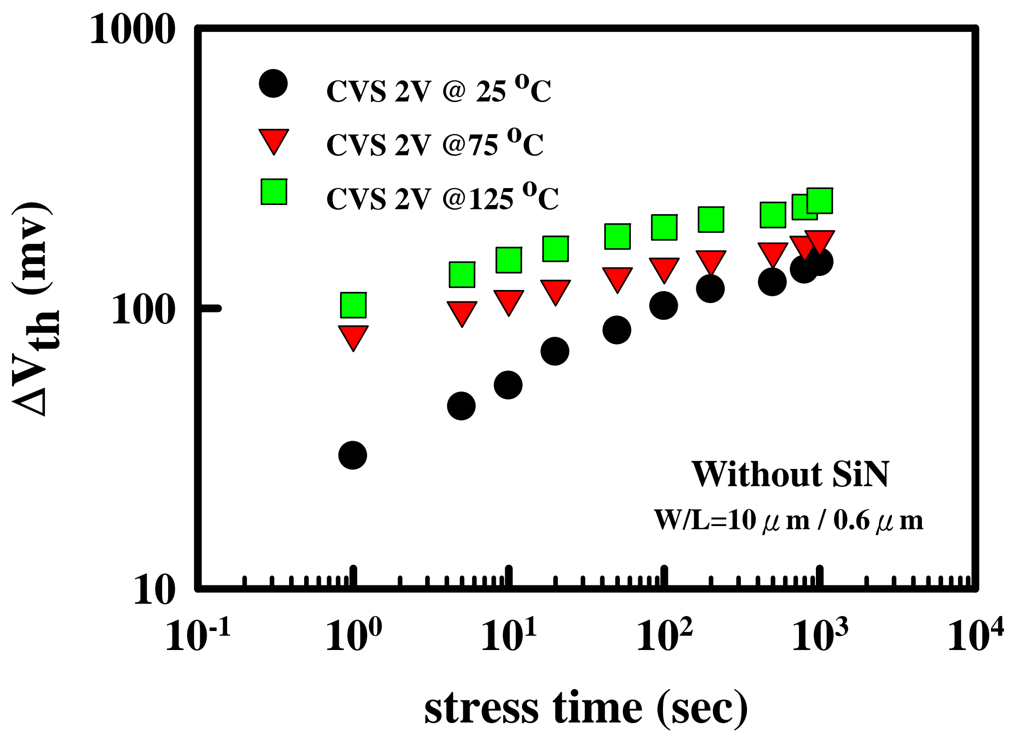


Fig 4-14 Threshold voltage shift (ΔV_{th}) as a function of stress time for HfAlO nMOSFETs without SiN capping layer under various temperature

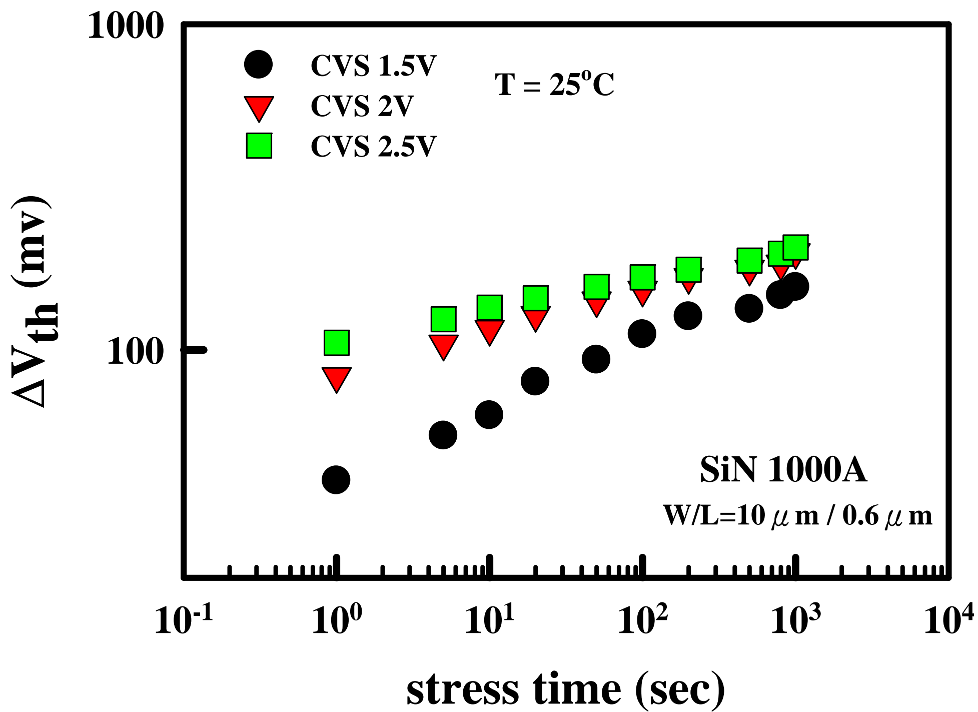


Fig 4-15 Threshold voltage shift (ΔV_{th}) as a function of stress time for HfAlO nMOSFETs with SiN 1000A

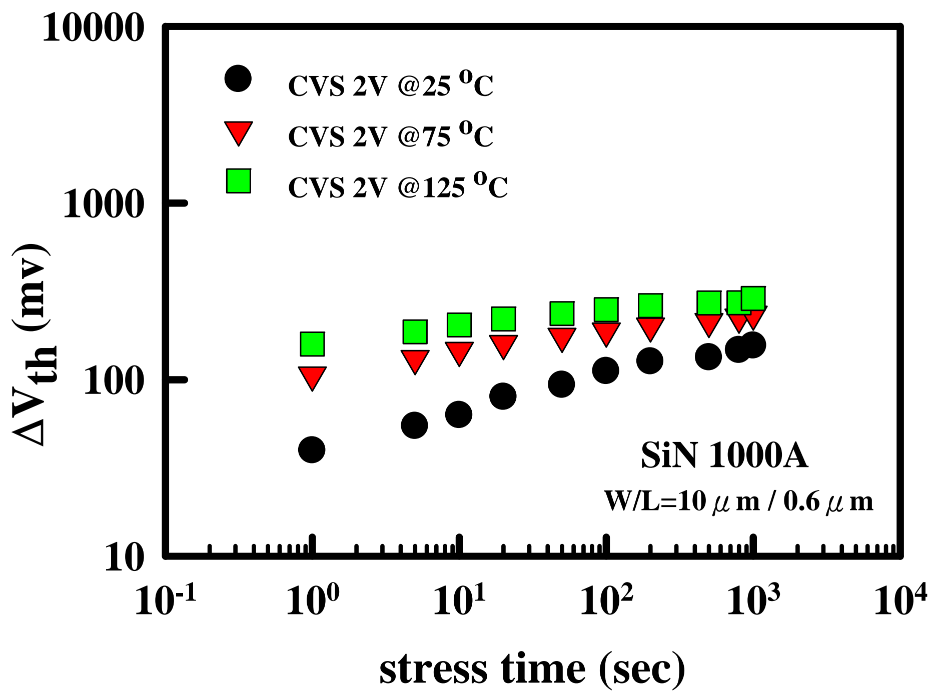


Fig 4-16 Threshold voltage shift (ΔV_{th}) as a function of stress time for HfAlO nMOSFETs with SiN 1000A capping layer under various temperature

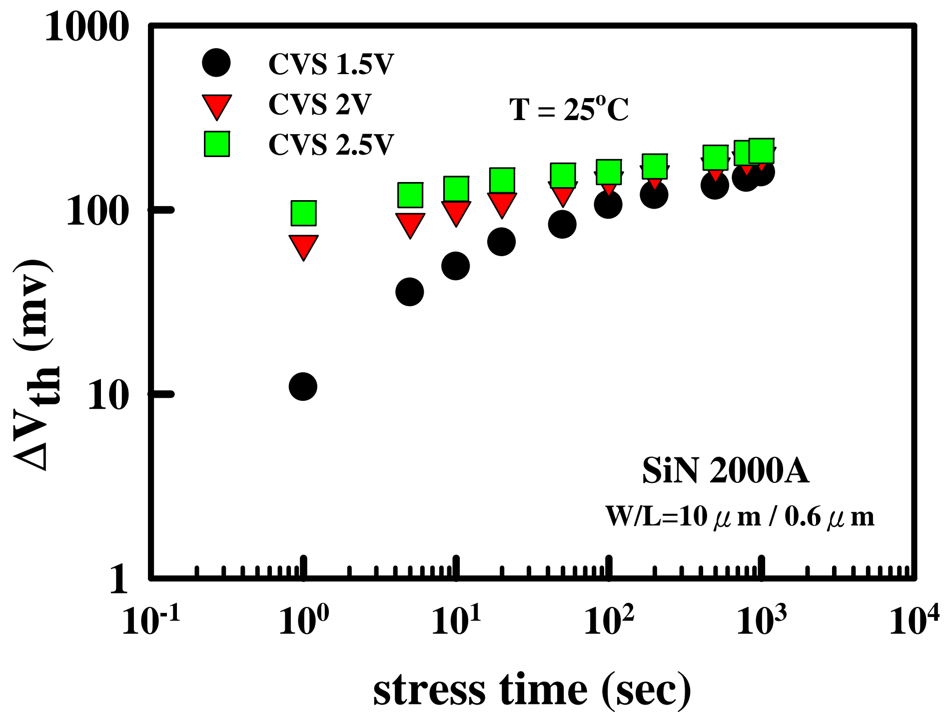


Fig 4-17 Threshold voltage shift (ΔV_{th}) as a function of stress time for HfAlO nMOSFETs with SiN 2000A

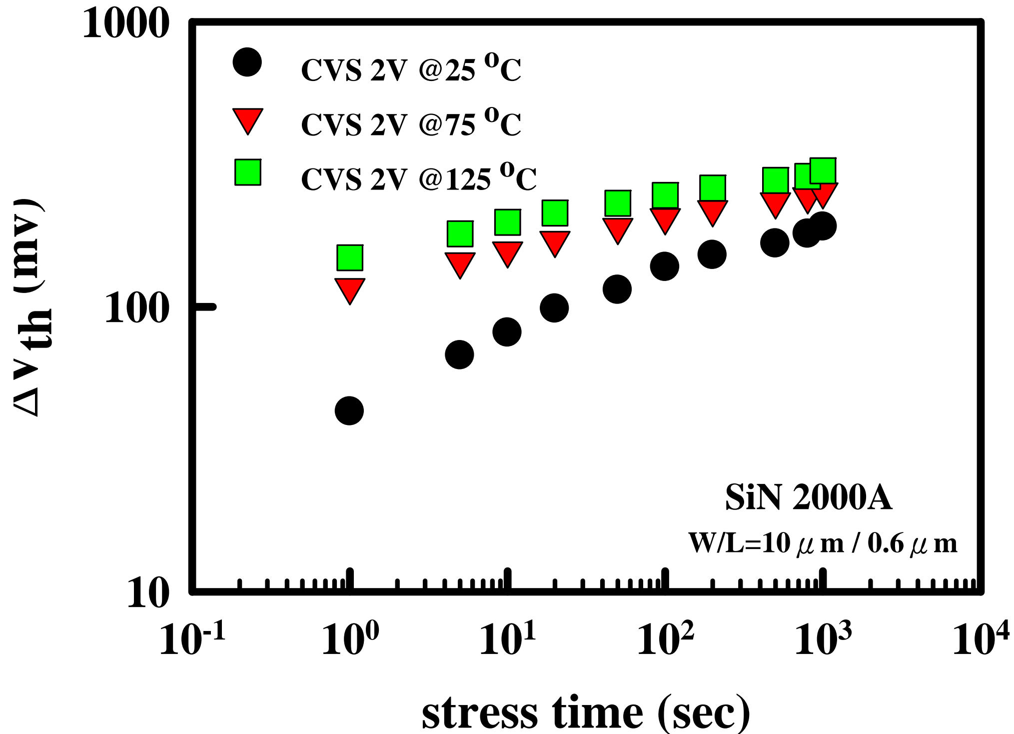


Fig 4-18 Threshold voltage shift (ΔV_{th}) as a function of stress time for HfAlO nMOSFETs with SiN 2000A capping layer under various temperature

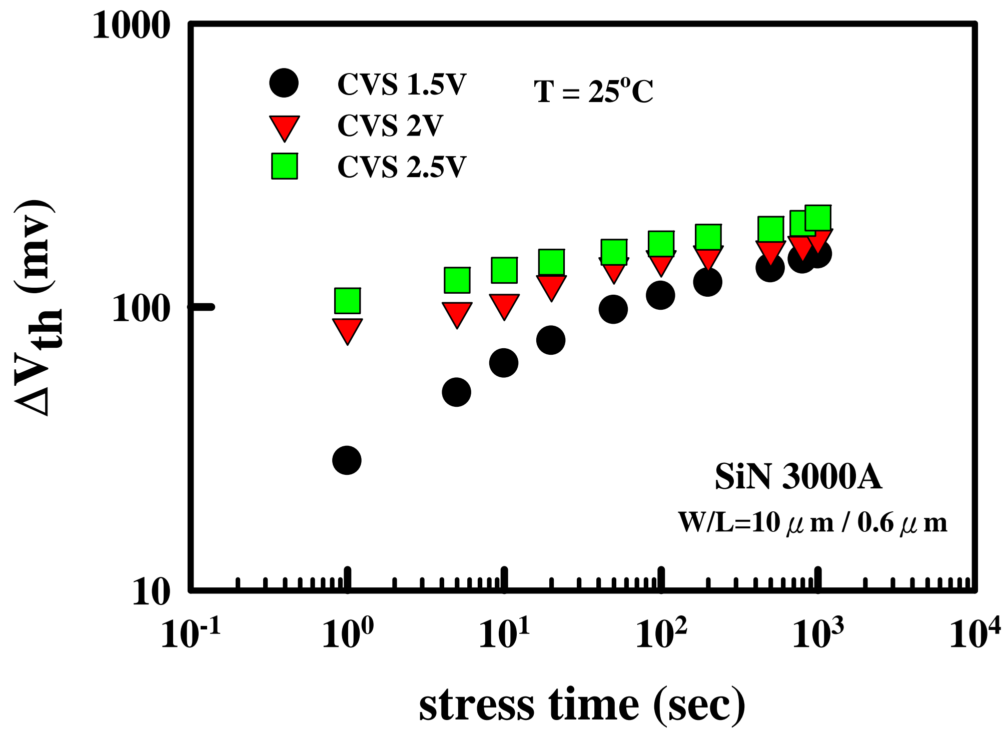


Fig 4-19 Threshold voltage shift (ΔV_{th}) as a function of stress time for HfAlO nMOSFETs with SiN 3000A

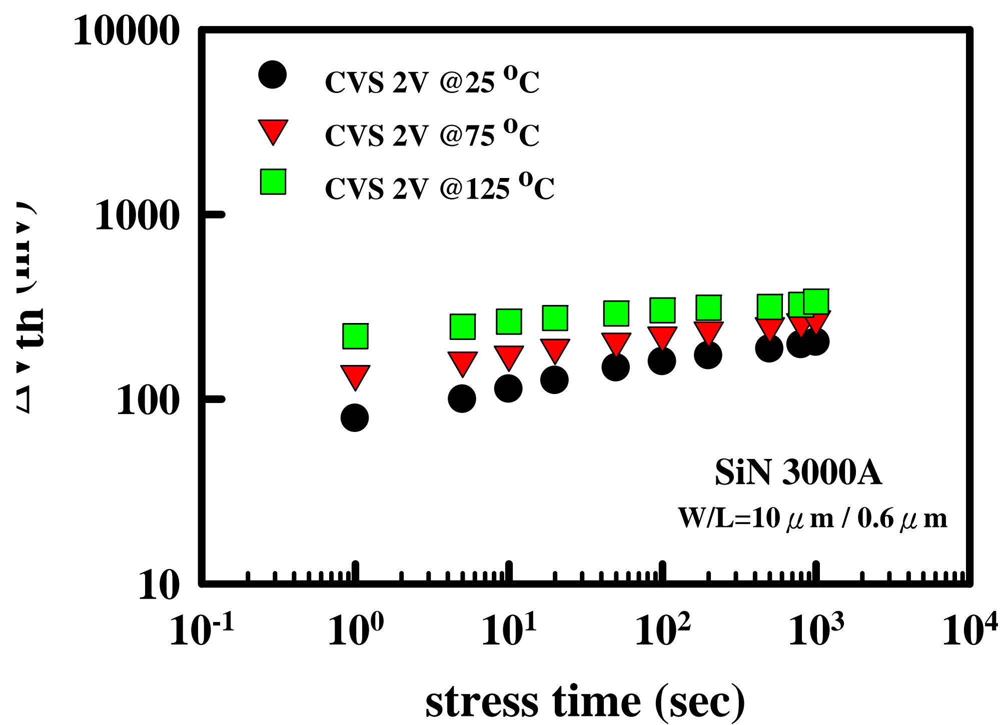


Fig 4-20 Threshold voltage shift (ΔV_{th}) as a function of stress time for HfAlO nMOSFETs with SiN 3000A capping layer under various temperature

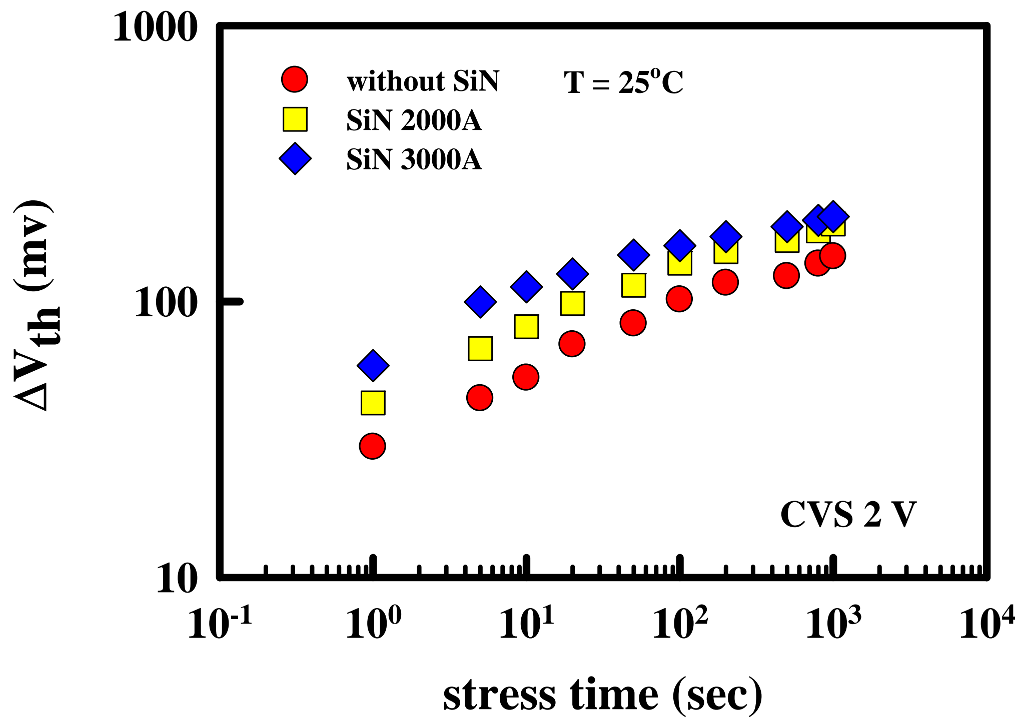


Fig 4-21 Threshold voltage shift (ΔV_{th}) as a function of stress time for HfAlO nMOSFETs with different SiN capping layer under CVS 2V at 25℃

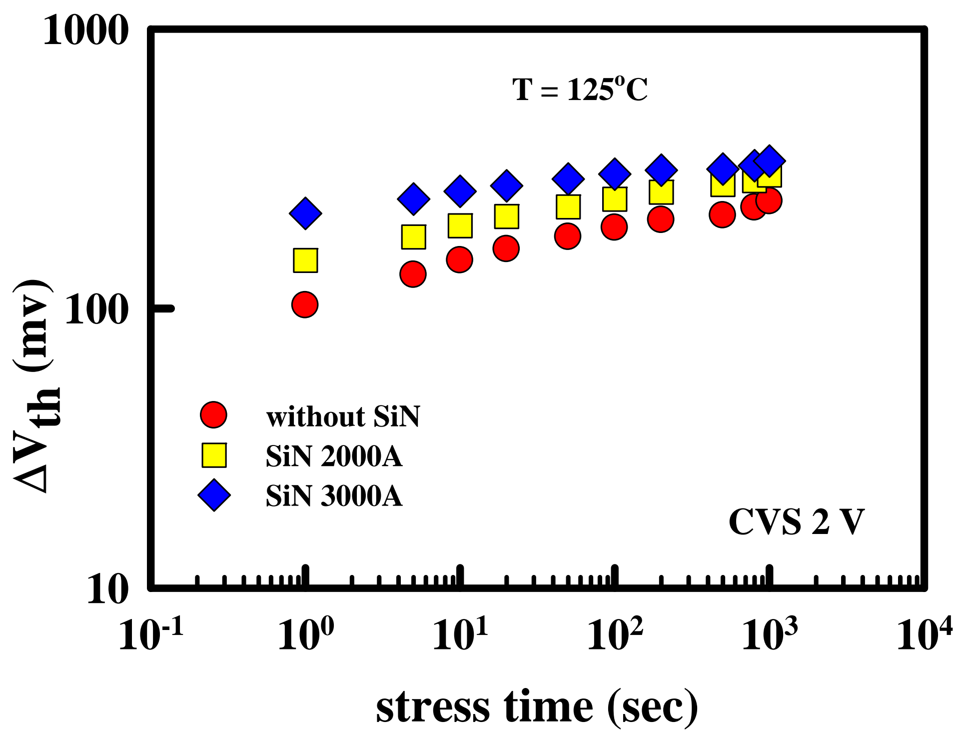


Fig 4-22 Threshold voltage shift (ΔV_{th}) as a function of stress time for HfAlO nMOSFETs with different SiN capping layer under CVS 2V at 125℃

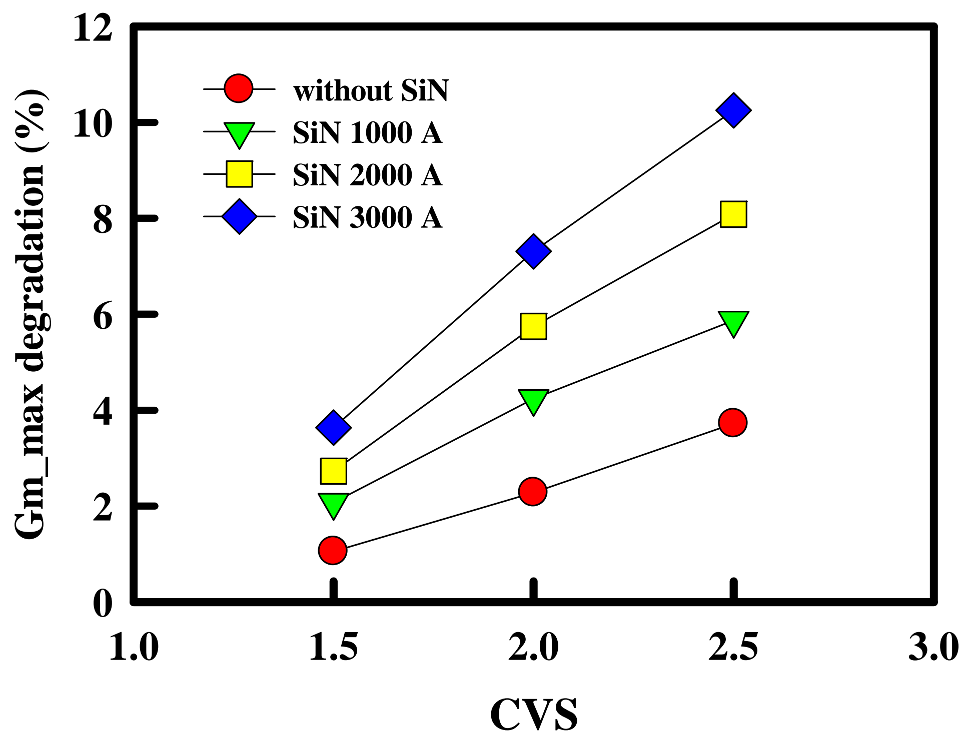
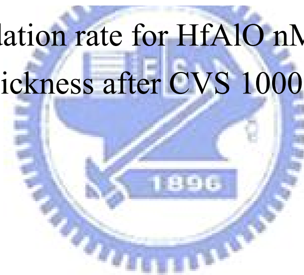


Fig 4-23 Gmmax degradation rate for HfAlO nMOSFETs with different SiN thickness after CVS 1000secs



Chapter 5
Conclusions and Future Work

5-1 Conclusions

In this paper, we verify that PECVD SiN capping layer is tensile strain and suitable for nMOSFETs application. Therefore, as SiN capping layer thickness increases, driving current has a huge enhancement. Besides, we observe that interface states become less when SiN capping layer thickens. It may be attributed that a large amount of hydrogen generated from SH_4 and NH_3 and then passivate the interfacial layer and we verify the number of interface states by using charge pumping method. Eventually, we utilize carrier separation method to make sure the current component under inversion and accumulation regions and carrier separation measurement with different temperature is followed to calculate the electron and hole barrier height under inversion region then, we obtain F-P conduction mechanism is matched. This indicates that less barrier height as SiN capping layer increases.

The CVS reliability of nMOSFETs with HfO_2/SiON and HfAlO/SiON is investigated in this chapter. The CVS under various temperature is also shown. It is believed that CVS degradation is related to the electron traps in gate dielectric. And therefore cause threshold voltage shift. We observe that serious degradation such as threshold voltage shift occurs as SiN capping layer thickens. And we also find that

threshold voltage shift with high temperature is larger when the thickness of SiN thickness increases. It can be explained by more Si-H bonds with thicker SiN capping layer which come from the reaction of SiH_4 and NH_3 precursor break when constant voltage stress applies or great tensile strain as thickness of SiN capping increase, and it brings about more strain energy which is stored in the channel.

5-2 Future Work

There are many issues that we can't discuss completely. We list some goals for future work as follows.

1. HRTEM is used to verify real thickness and estimate value of the dielectric constant for HfO2/SiON and HfAlO/SiON gate stack.
2. Because of actual CMOS circuit operation, AC gate bias with specific frequency and duty cycle is usually utilized. Therefore, AC stress with Dynamic AC stress application is more realistic and can provide additional insights into the trapping behavior.
3. Fast transient pulsed Id-Vg measurement is also used to evaluate charge-trapping phenomena precisely.
4. Charge pumping measurement on CVS.
5. Find the better recipe of surface treatment to gain good interfacial layer quality.

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簡歷

姓名：邱大峰

性別：男

年齡：23 歲（民國 72 年 8 月 28 日）

籍貫：台灣省台北市

學歷：私立淡江大學電機工程學系　　（90.9-94.6）

　　　國立交通大學電子工程研究所（94.9-96.7）

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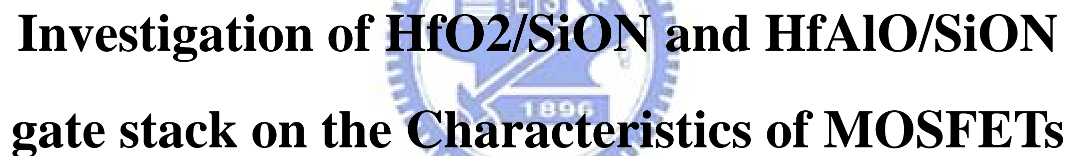

Investigation of HfO2/SiON and HfAlO/SiON gate stack on the Characteristics of MOSFETs

二氧化鉿與氧化鋁鉿堆疊式閘極

在金氧半場效電晶體上的特性研究