Chapter 2

Robust Ultrathin Oxynitride with High Nitrogen Diffusion Barrier near its Surface Formed by NH3 Nitridation of ChemicalOxide andReoxidation with O2

2-1 Introduction

The continuous shrinkage of device dimension below a quarter-micro requires highly reliable ultra-thin dielectric film. In this thickness range, not only breakdown but also wear out of dielectric films is one of the key technology issues. As an alternative gate dielectric, nitrided oxide has drawn considerable attention due to their superior performance and reliability properties over conventional SiO2. For example, in a P^+-gate device, boron can easily diffuse into the channel region through the ultrathin gate oxide layer during the dopant activation process [58], [59], leading to threshold voltage being shifted. In principle, a small voltage shift that results from boron penetration will not cause a problem as long as it is predictable. The situation can be improved with modified threshold-adjusted implants. However, boron penetration not only causes the threshold voltage V_T to be shifted, but also degrades the process margin by increasing the spread of V_T. Since boron penetration is sensitive to gate dielectric thickness, the thickness variation of the gate oxide plays an important role in controlling the degree of boron penetration. In fact, it has been

reported that boron penetration increases exponentially with decreasing oxide thickness. Furthermore, the threshold voltage variation degrades a device’ s performance and increases its off-state leakage current.

On possible approach to form nitride oxides was post-oxidation annealing, including ammonia (NH3), nitrous oxide (N2O) and nitric oxide (NO) annealing. unfortunately, they usually require specific tools or gas. It is desired to have a simple way to obtain the film and retain its quality. In fact, reoxidized NH_3-oxynitride was proposed in the late 80s to the early 90s, however on thick thermal oxide,. The difference between this process (reoxidized NH_3-oxynitride) and the process mentioned above is that the former technique suffered a much higher thermal budget. The process temperature is around 1050℃ or even higher[60]. The film obtained by such process technology always comes out with a thick film. Compared with that in the case of the new process (developed in this paper), both thin thickness and film quality can be obtained successfully with low thermal budget, i.e., at low reoxidation temperature (900℃). Meanwhile, chemical oxide as a starting oxide can provide a better controllability in film thickness[61]. Nowadays, lower process temperatures and thinner oxynitride films are preferred in ULSI technology.

In addition, it is well known that gate dielectric doped with nitrogen can effectively suppress boron diffusion. However, the side effect is that the gate oxide

suffers from the oxide reliability issue owing to nitrogen piled up along the interface between the silicon substrate and oxynitride [52]. Ideally, we would like to have a nitrogen-doped dielectric with high nitrogen content close to the surface, which can effectively block boron diffusion, while low nitrogen content is distributed in the interface, which would not degrade oxide reliability.

In this chapter, an alternative approach for forming an oxynitride gate dielectric with high nitrogen content distributed close to the surface is demonstrated. The proposed approach is realized by NH_3 nitridation of chemical oxide and reoxidation with O_2. By this technique, the desirable nitrogen concentration profile can be obtained to meet the requirement of device performance. It is noted that the process proposed here is simple and fully compatible with current IC industry fabrication technology.

2-2 Experiment procedure

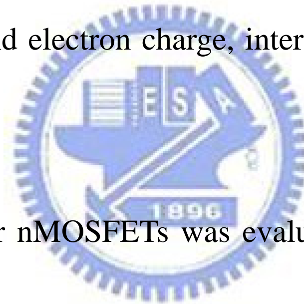
Standard local oxidation of silicon (LOCOS) process was applied for devices isolation. The nMOSFETs were fabricated on 6-inch p-type (100) Si wafers utilizing conventional self-align process. After dipping sacrificial oxide about seven minutes, standard RCA clean was used to remove organic, particle and metal contamination. At once， The oxynitride growth included three process stages－chemical oxide growth,

nitridation and subsequent dry oxidation. First, the wafers were immediately immersed into H_2O_2 solution at room temperature for 20 min to grow 10-A-thick chemical oxide. Following that, the chemical oxide was nitrided using a furnace in low-pressure (120 mTorr) NH_3 ambient at 700℃ for 30 min. The nitrided chemical oxide was then placed in atmospheric O_2 ambient at 932℃ and annealed in N_2 at 932℃ for 10 min to form a robust oxynitride. Furthermore, a conventional oxide grown at 800℃ was also prepared to serve as the control sample. A 200nm poly-silicon was deposited by low pressure chemical vapor deposition (LPCVD). Subsequently, gate electrode was defined by I-line lithography stepper and etched by ECR etching system. After removing sidewall polymer, S/D extension implant was executed. Spacer formation was carried out by ultra-high-vacuum chemical vapor deposition (UHVCVD). To continue patterning and S/D implant. Then, rapid thermal anneal (RTA) was performed at 950°C for 20 sec in N_2 ambient to activate dopants. Afterwards, SiO_2 capping layer (5000A) was deposited by plasma-enhanced CVD (PECVD). Al-Si-Cu metallization were implemented by PVD system. After metal etching, Fermi gas annealing at 400℃ for 30minutes in N_2/H_2 ambient was used to fix dangling bond and reduce interfacial state density, Fig.2-1 shows the experimental flow, and Fig.2-2 shows the nMOSFET structure.

Basic electrical characteristic such as I-V and C-V was measured by a 4156C

precision semiconductor parameter analyzer and HP4282 LCR meter. The equivalent oxide thickness (EOT) was obtained from I-V accumulation region without calculating poly depletion and substrate condition.

Besides, Interface state density (N_{it}) conversion was evaluated from charge pumping method. A square-wave generated from 81110A was applied to the gate electrode while source/drain and body were grounded. The time varying gate voltage with fix pulse amplitude at 1.5V was to be driven from inversion to accumulation. From the equation $N_{it} = \frac{\mathrm{Icp}}{qAf}$ whereas A, f and q are the area of gate electrode, the frequency of pulse voltage and electron charge, interface state density (N_{it}) could be extracted.



The electron mobility for nMOSFETs was evaluated by split C-V method. The effective mobility was measured at low drain voltage and then gave

$$\mu_{\mathrm{eff}} = \frac{\mathrm{g_d L}}{\mathrm{WQ_n}}$$

Where the drain conductance g_d was defined as

$$g_d = \frac{\partial I_D}{\partial V_{DS}} \Big|_{V_{GS} = constant}$$

Q_n was measured from capacitance measurements. The capacitance meter was connected between the gate and the source-drain connected together with the substrate grounded. Therefore, Q_n was expressed as follows

$$Q_n = \int_{-\infty}^{V_{GS}} C_{gc} dV_g$$

And effective electric field produced by the gate voltage was express as:

$$E_{eff} = \frac{Q_b + \eta Q_n}{K_s \varepsilon_o}$$

$$Q_b = \int_{Vfb}^{V_{GS}} C_{gb} dV_g$$

$$Q_n = \int_{-\infty}^{V_{GS}} C_{gc} dV_g$$

Where Q_b and Q_n were charge densities in depletion layer and inversion layer, respectively. The parameter ηb=1/2 was for electron mobility. And subsequently universal mobility was accomplished by this equation.

$$\mu_{eff} = \frac{638}{1 + \left(\frac{\varepsilon_{eff}}{area} \right)^{1.69}}$$

Above all equations, we easily can extract all of the data what we need.

2-3 Results and Disscussions

2-3-1 Extract Tox using Accumulation Direct-Tunneling Currents

As oxide thickness shrinkage down to the direct-tunneling region, tunneling current will strongly dependent on the oxide thickness. For example, tunneling current will be increased by 10 times as oxide thickness decreases from 22A¢X to 20 A¢X Therefore, using direct-tunneling current to extract oxide thickness becomes feasible solution. Since gate current in inversion mode is strongly dependent on the poly

depletion effect and threshold shifts, using inversion gate current to determine oxide thickness becomes more difficult. On the other hand, using accumulation gate current to determine oxide thickness is much easier since it will be independent on the poly depletion and substrate condition. As a result, a simple model can be used to evaluate Tox from accumulation gate current at different gate bias, named DTIV [62]:

$$\text{For Vg=-1.5V; Tox=}\frac{[10.1-\log(Jg)]}{6.2}$$

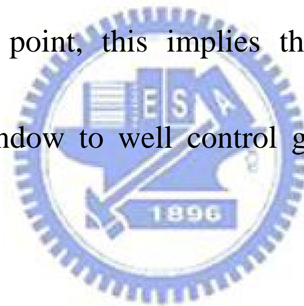
$$\text{For Vg= -1V; Tox=}\frac{[9.6-\log(Jg)]}{6.5}$$

Where Jg is the accumulation gate current density united A/cm^2 and Tox united nm.

2-3-2 Electrical Characteristics of nMOSFETs with Ultrathin Oxynitride has High Nitrogen Concentration near its Surface Formed by NH3 Nitridation of Chemical Oxide and Reoxidation with O2

A nitrogen distribution profile across the 25A and 70 A oxynitride gate dielectric revealed by secondary ion mass spectrometry (SIMS) are shown in Fig. 2-3. Apparently high nitrogen concentration with a peak located at the dielectric surface is observed. Such high nitrogen concentration is more helpful in resisting the boron penetration of the gate dielectric from the P^+ polysilicon electrode. The low nitrogen concentration at the interface also improves reliability [63], [64]. Figure 2-4 shows the

C-V shift of P^+-gated samples for the ultrathin oxynitride (23 A) and conventional oxide (30 A) with annealing at 900℃ for various times (60, 90 and 120 min). Comparing oxynitride with conventional oxide, it is apparent that the C-V curve shift in oxynitride is relatively smaller than that in conventional oxide. This implies that boron penetration is highly impeded by this oxynitride film. Meanwhile, the oxidation rates for the wafers, which have an existing oxide film grown by the conventional method or our nitrided-chemical oxide, are compared in Fig. 2-5. The results show that the oxidation rate of the nitrided-chemical oxide is much smaller than that of the conventional oxide. At this point, this implies that the nitrided-chemical oxide provides a wider process window to well control gate oxide thickness if ultrathin oxide is needed.



The measured gate current-voltage (I-V) of the N^+-gated MOSFET with EOT 24 A oxynitride films are shown in Fig.2-6. An Ig-Vg curve with a very low leakage current of is obtained. This is attributed to the clean chemical oxide. When the process of chemical oxide formation proceeds, the clean oxide inhibits defect formation because it does not require a high-temperature process. This means that chemical oxide as a starting oxide is essential in this process. Fig. 2-7 shows that significant reduction of leakage currents is obtained. Because, effective nitrogen incorporation from NH_3 nitridation the chemical oxide film increases dielectric constant, which

allows physically thicker film with EOT to suppress the direct tunneling leakage current SiO_2.

For further study, the hysteresis in the C-V characteristics of the N^+-gated sample with 24 A oxynitride film was also evaluated. The data are shown in Fig.2-8. The figure shows that there is no hysteresis found in the high-frequency C-V curve, indicating that the film has a very low bulk or interface trap density. Fig.2-9 shows that the dominant conduction mechanisms in this oxynitride are direct tunneling and F-N tunneling. Frenkel-Poole conduction mechanism does not exist, because Ig-Vg curve is weak temperature dependence. We believe the limited of traps in this oxynitride is probably responsible for this, because the F-P conduction requires a high density of traps.

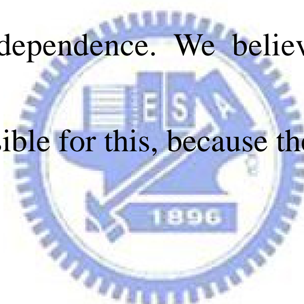


Fig. 2-10(a) shows a family of drain current curves of an nMOSFET transistor while Fig.2-10(b) shows the corresponding transconductance and current at Vd=0.1V characteristics. The oxynitride device exhibits high drain current and high transcondance(418uS). The mobility of oxynitride compare to conventional oxide shows at Fig.2-11.

Fig 2-12 shows the Vth-roll-off characteristics. When channel length is less than 1um, Vth-roll-off phenomenon is more serious. Fig 2-13 indicates the sub-threshold swing of devices with different channel length. And we find that sub-threshold swing

is almost the same in different channel length. The Vth Weibull distribution in oxynitride and conventional oxide shows in Fig.2-14. It shows that oxynitride Vth has uniform distribution.

2-4 Summary

We have proposed an approach for forming high quality ultrathin oxynitride films with a nonuniform nitrogen content distribution, which has high content at the surface and low content at the interface between oxynitride and the silicon substrate, without using extra equipment or gas and which is totally compatible with current semiconductor fabrication technology. Such film exhibit substantially lower leakage current than their thermal oxide counterparts and demonstrates excellent suppression of boron diffusion. The direct tunneling and FN tunneling dominate the current transport in the oxynitride film, which weakens the temperature dependenxe. The oxynitride device exhibits high drain current and high transcondance(418uS) and good mobility.

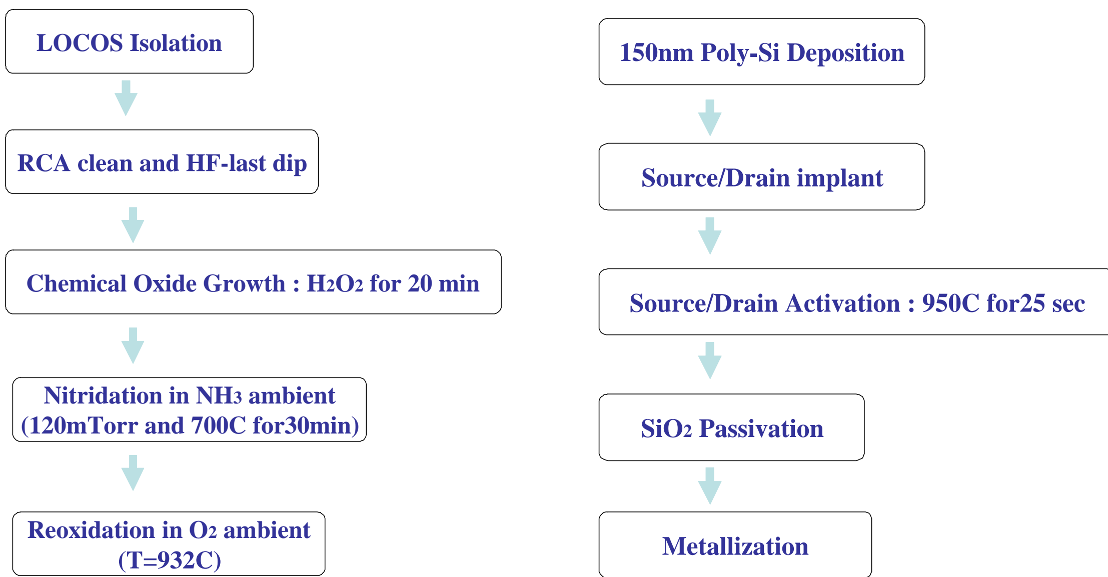


Fig.2-1 Experimental Flow.

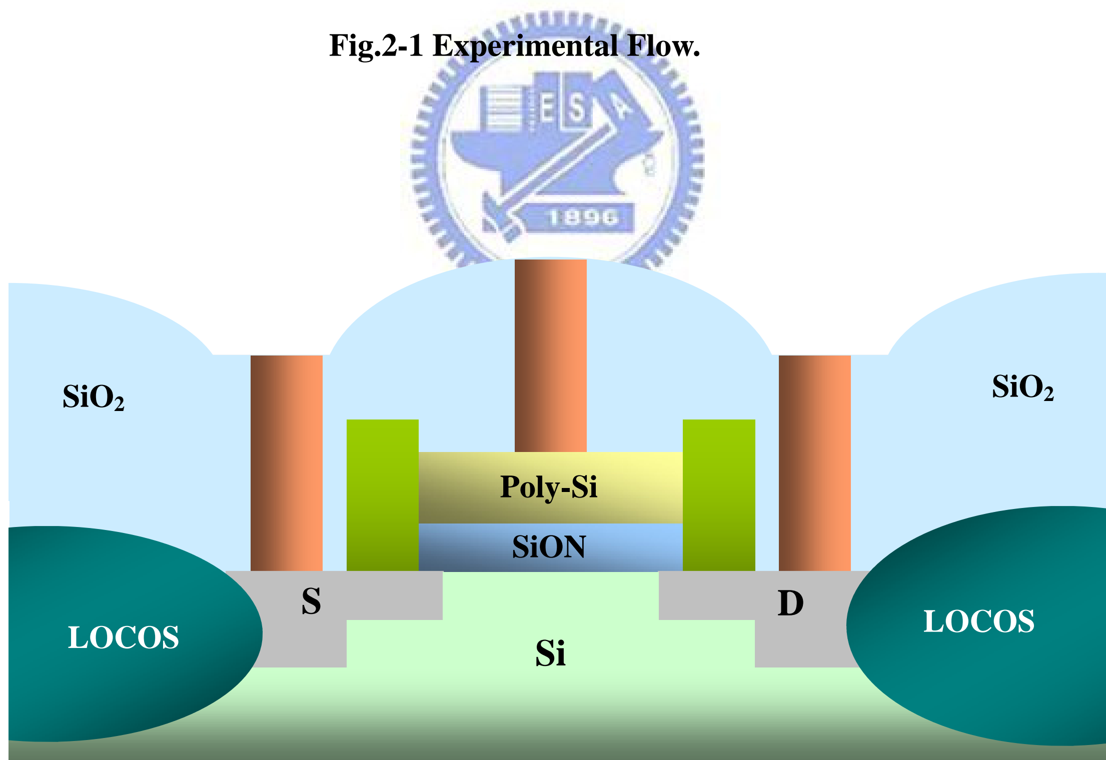
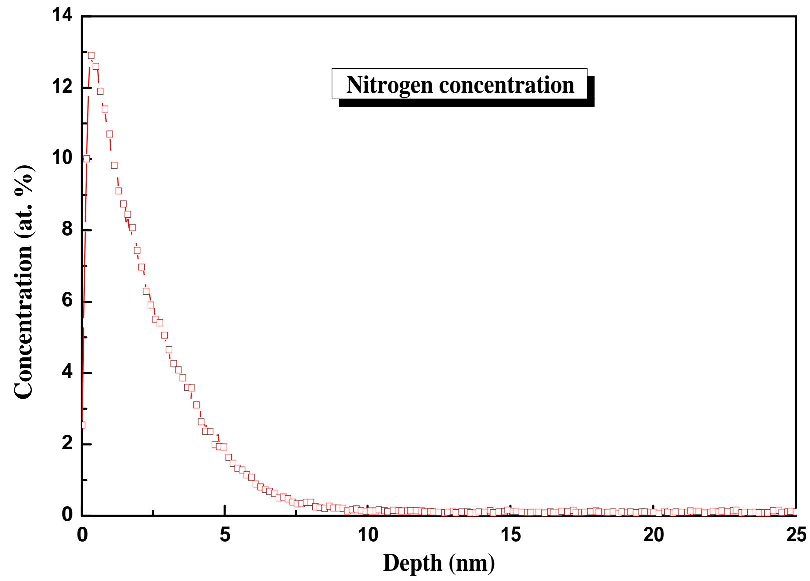
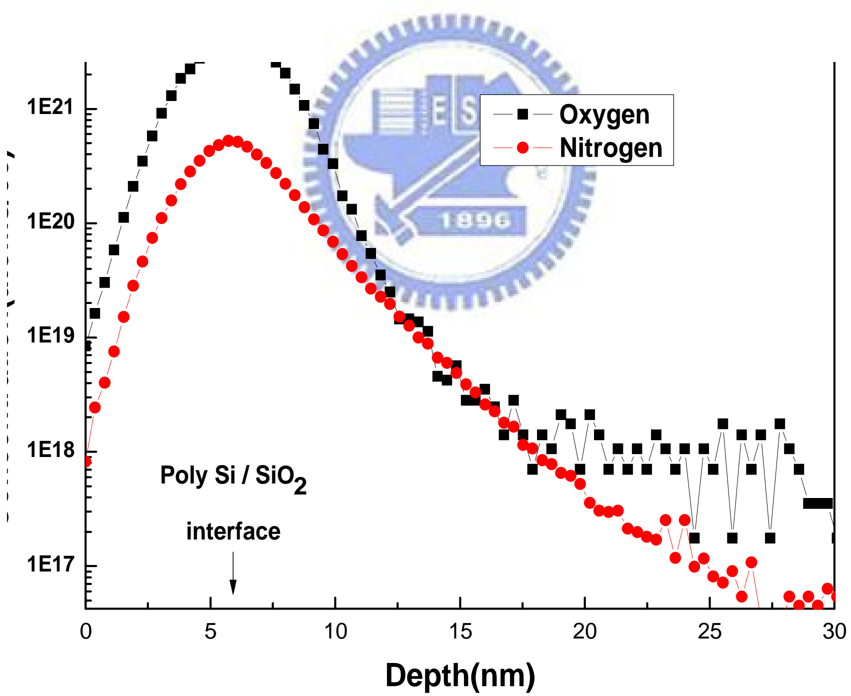


Fig2-2 nMOSFET structrre.



(a)



(b)

Fig.2-3 SIMS profile of oxygen and nitrogen distribution of (a) 70 A and (b) 25 A oxynitride.

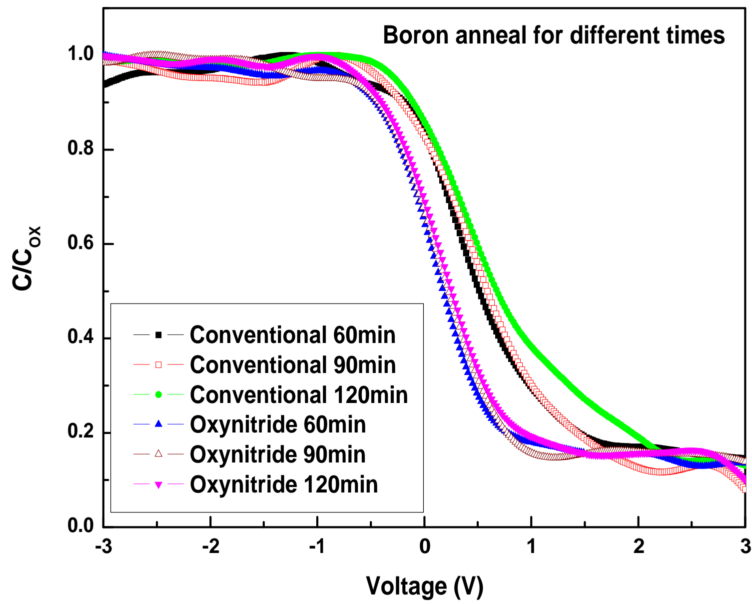


Fig. 2-4 High-frequency C-V characteristics of p^+-gated MOS capacitor for ultrathin oxynitride (23 A) and conventional oxide (30 A) with different annealing times.

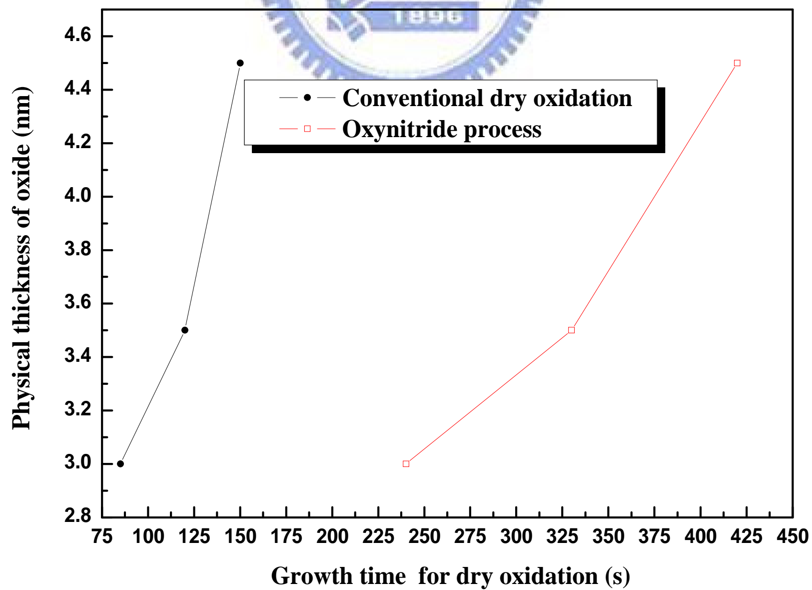


Fig.2-5 Growth time for dry oxidation versus physical thickness of oxide for conventional dry oxidation and oxynitride processes.

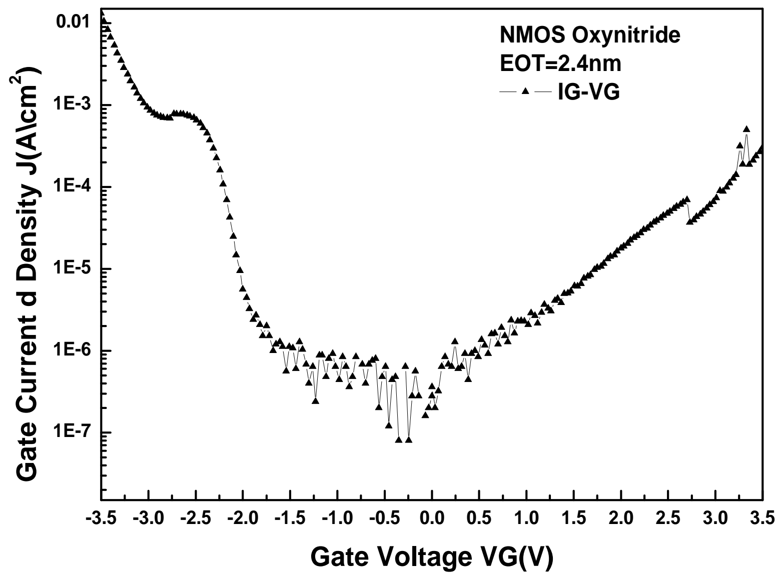


Fig.2-6 Gate leakage current density versus gate bias for fresh n-channel devices at room temperature.

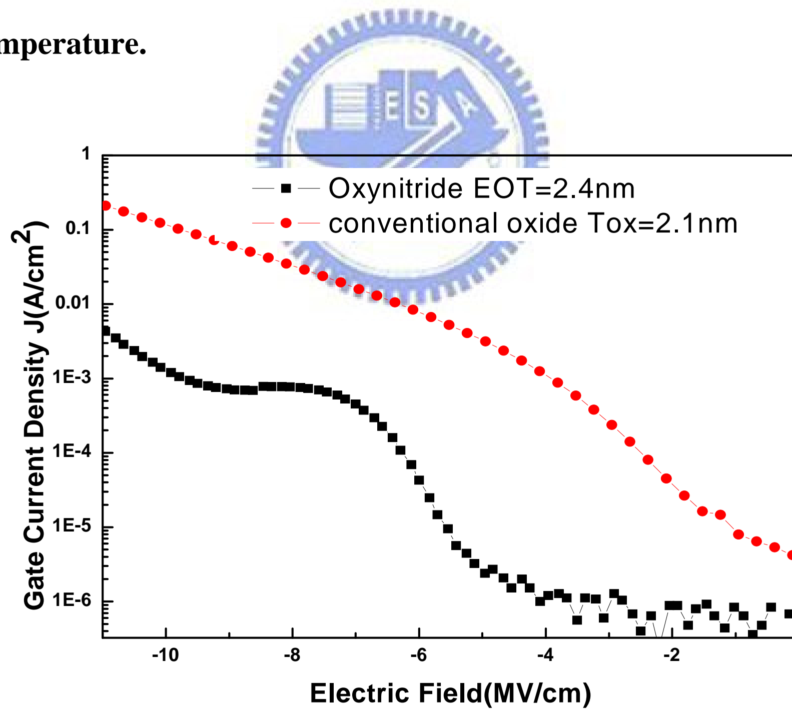


Fig2-7 Gate leakage current density versus electric field of pure thermal oxide and oxynitride.

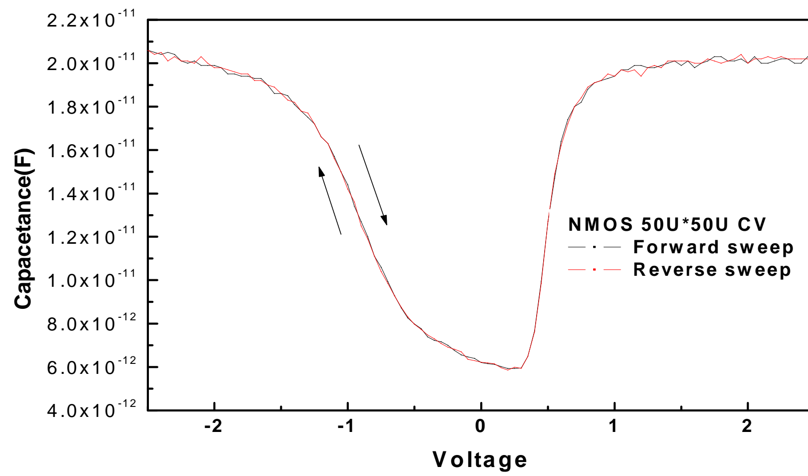


Fig2-8 Hystersis characteristics of oxynitride film with EOT=24A.

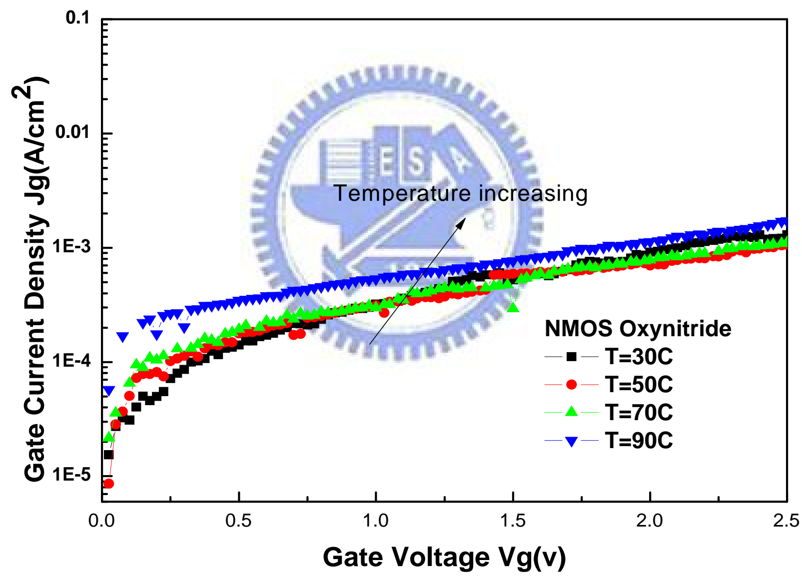
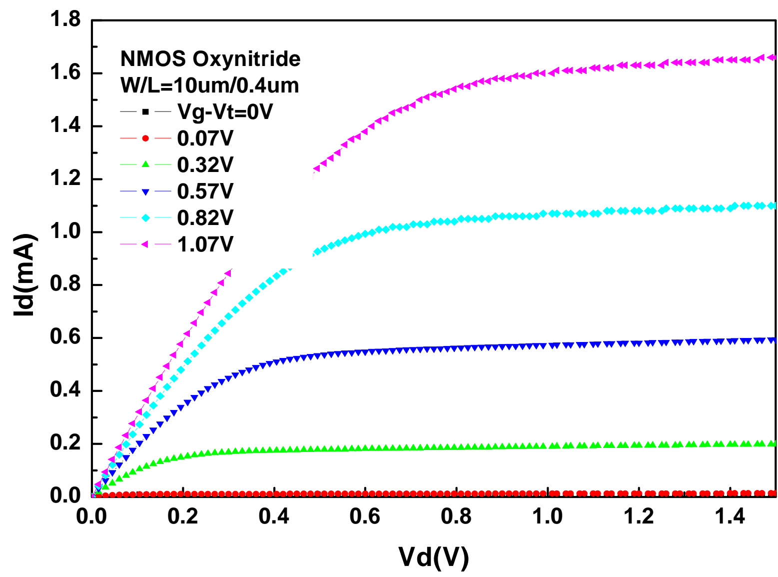
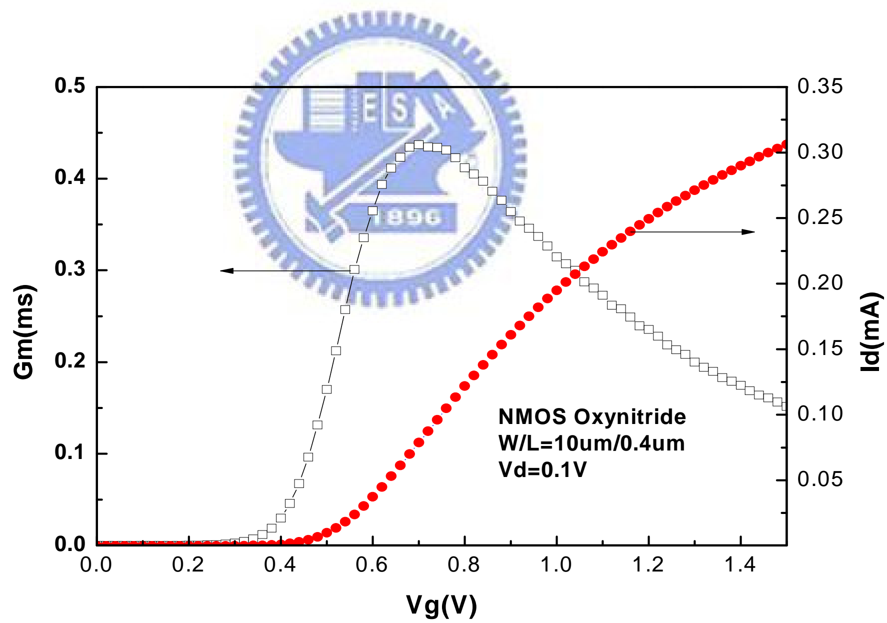


Fig. 2-9 I-V characteristics at various temperature.



(a)



(b)

Fig.2-10 (a) Id-Vd characteristics (b) Gm and Id-Vg characteristic of oxynitride for nMOSFET.

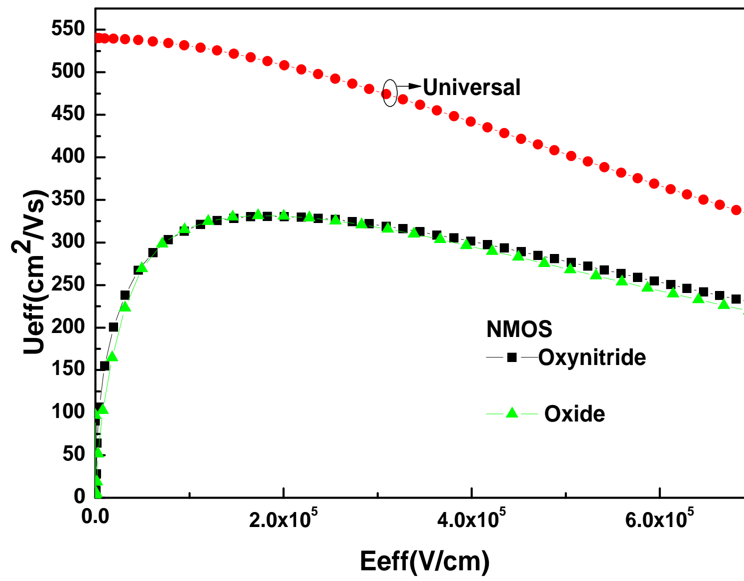


Fig.2-11 Compared electron mobility with oxynitride and oxide measured by split-CV method.

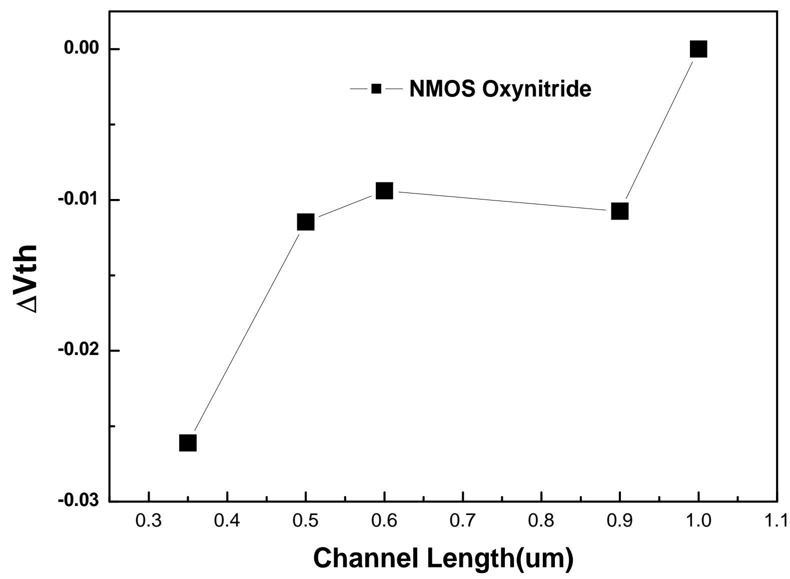


Fig.2-12 Vth roll off characteristic of oxynitride.

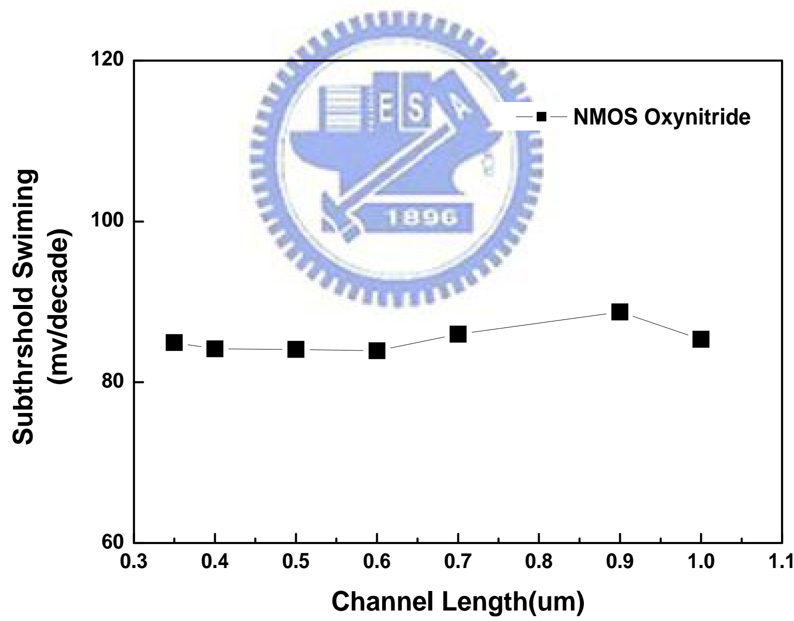


Fig.2-13 Subthreshold swing of devices with different channel length.

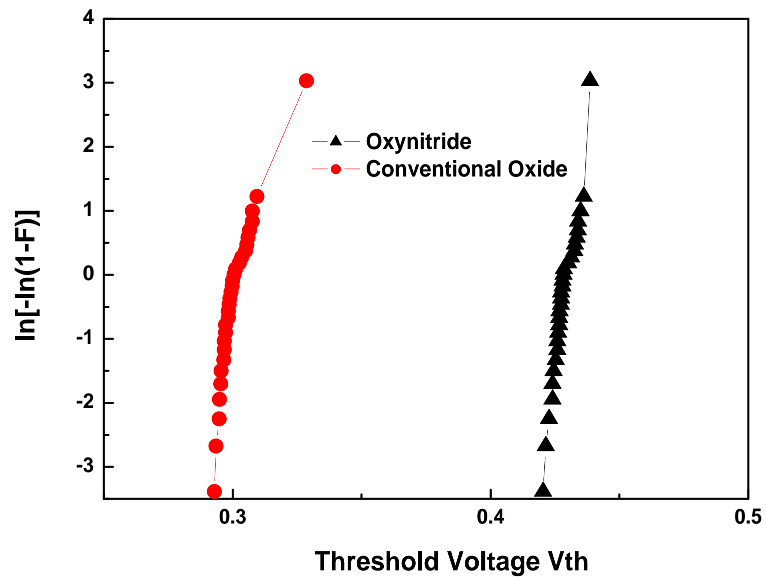


Fig.2-14 Vth Weibull distribution in oxynitride and conventional oxide.