

Chapter 3

Reliability characteristic of

Robust Ultrathin Oxynitride with High Nitrogen Diffusion

Barrier near its Surface Formed by NH₃ Nitridation of

ChemicalOxide andReoxidation with O₂

3.1 Introduction

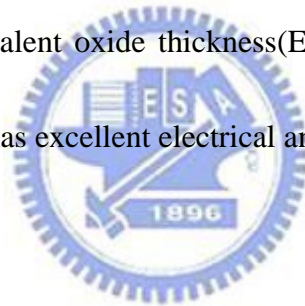
Recently, reliability is an important issue in scaled MOSFET. During high voltage stress, defects can be generated in the devices, which in turn cause threshold voltage shifts and devices characteristics degradation. The device parameter variation can lead to circuit failures, both for analog and digital application.

Moreover, it has been reported that the temperature acceleration effect and the stress induced leakage current(SILC) reliability were severe enough to raise concern over the further scaling down of thermal oxide. This SILC phenomenon may be due to enhanced FN tunneling by building of the generated holes similarly to the intrinsic breakdown. As the dielectric film is thinner, it has been a seriously problem with regard to not only retention characteristic but also read disturb for Flash memories. Ultrathin oxynitride films have been reported with good performance in SILC.

Besides, hot carrier effects in SiO₂ gate dielectric has been one of a major

concerns for device scaling, especially nMOSFETs while the pMOSFETs has less problematic due to smaller impact ionization formation and the higher valence band barrier height. What hot carriers we mention is near the drain regions where charge carriers are accelerated by the field and become hot, can overcome the oxide barrier and inject into the gate. Hot carriers induce damage to the gate oxide and may be trapped there, thereby degrading the device performances.

Reliability of ultrathin oxynitride will discuss in this chapter. We will find the oxynitride which we proposed not only increase dielectric constant of the resulting film to achieve thinner equivalent oxide thickness(EOT) without degrading SiO₂/Si interface properties, but also has excellent electrical and reliability characteristics.



3.2 Measurement setup

SILC on nMOSFETs is measured under accumulation. A constant voltage stress is applied to the gate of a device, while the source/drain and substrate are grounded. After stress, measures such as IG-VG, ID-VG and charge pumping are concluded. IG-VG can reveal the leakage current increasing after constant voltage stress, because constant voltage stress produces defect in the dielectric. ID-VG measurements are used to evaluate G_m variations and threshold voltage shift. And charge pumping measurements are also used to obtain interface density generation.

Analogous method which we measure is applied to HCI (hot carrier injection). Their

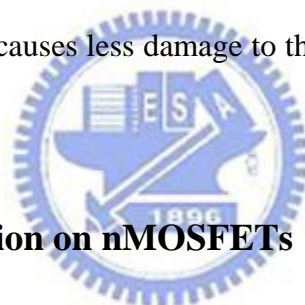
difference is that using extra high voltage is applied to drain electrode which causes impact ionization in the depletion region near the drain side and electron-hole pairs are generated. At the same time, holes will flow toward substrate to form substrate current (I_{sub}). For the purpose of application for degradation from HCI, nMOSFETs devices are stressed at the max substrate current corresponding gate voltage which regards as the most efficient generation of hot carriers. Eventually, we exploit the most serious degradation method to evaluate HCI. And Fig 3-1 reveals basic measurement method for SILC and HCI.

3-3-1 Stress Induce Leakage Current on nMOSFET

Fig 3-2(a) and Fig.3-2(b) expresses I_d-V_g characteristics for oxynitride and conventional oxide before stress and after stress 1000s. It can be seen conventional oxide has serious degradation of V_{th} shift after stress. Relatively, oxynitride has good performance in SILC. Then, Fig 3-3(a) and Fig.3-3(b) shows in detail the threshold voltage shift and interface trap density shift which compares oxynitride with oxide. Besides, we observe that threshold voltage shift becomes huge as constant voltage stress increases. It may be attributed that more electron-hole pairs which generate in channel region and tunnel to the gate dielectrics which turn to great threshold voltage instability. Fig.3-4(a) shows the result after constant voltage stress at -3V for sample with $EOT=24 \text{ \AA}$. No significant SILC was observed after 1000 sec

stressing. In Fig.3-4(B), it shows the sample after different constant voltages stressing during 1000sec stressing. No significant SILC increase of leakage current was observed for these samples also.

Fig.3-5(a) and Fig.3-5(b) ,respectively, show the threshold voltage shift and interface trap density shift in oxynitride with different temperature. We find that threshold voltage shift and interface trap density shift increase with temperature increasing, so that, the device will accelerate to breakdown. Fig.3-6 shows that the longer time-to-breakdown(Tbd) for the oxynitride film is primarily attributed to its lower leakage current, which causes less damage to the dielectric and thus contributes to a longer dielectric lifetime.



3-3-2 Hot Carrier Injection on nMOSFETs

As the channel length aggressively scales down, device induces by hot carrier injection represents one of the most reliability limit. Fig 3-7 reveals I_{sub} current versus gate voltage with different channel length. It is clear that the substrate current increase as channel length reduces. Besides, it have been demonstrated that the worst hot-carrier condition varies from $V_g = V_d/2$ to $V_g=V_d$. Thus we easily try two conditions $V_g= I_{sub}|_{max}$ and $V_g=V_d$ to obtain the most serious degradation. Fig 3-8(a) and Fig.3-8(b) shows the result with different HCI conditions. The larger degradation which happens at $V_g= 1/3V_d$. Therefore, we attain larger threshold

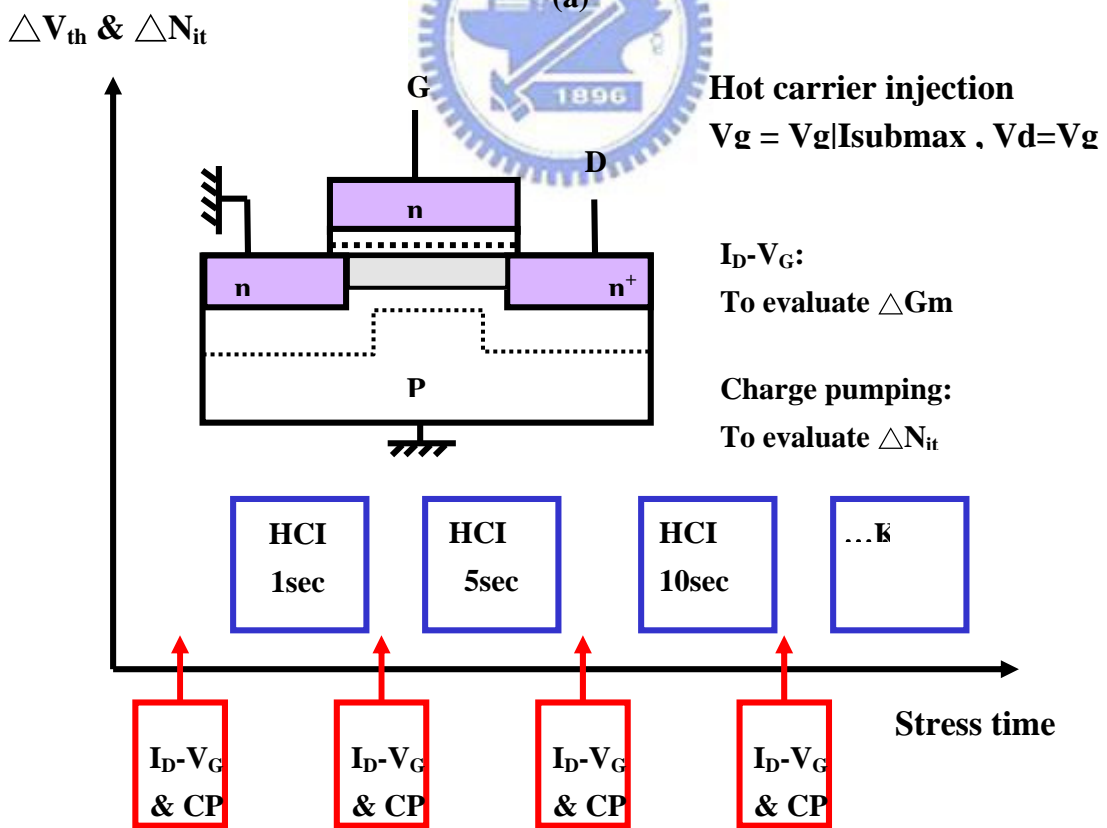
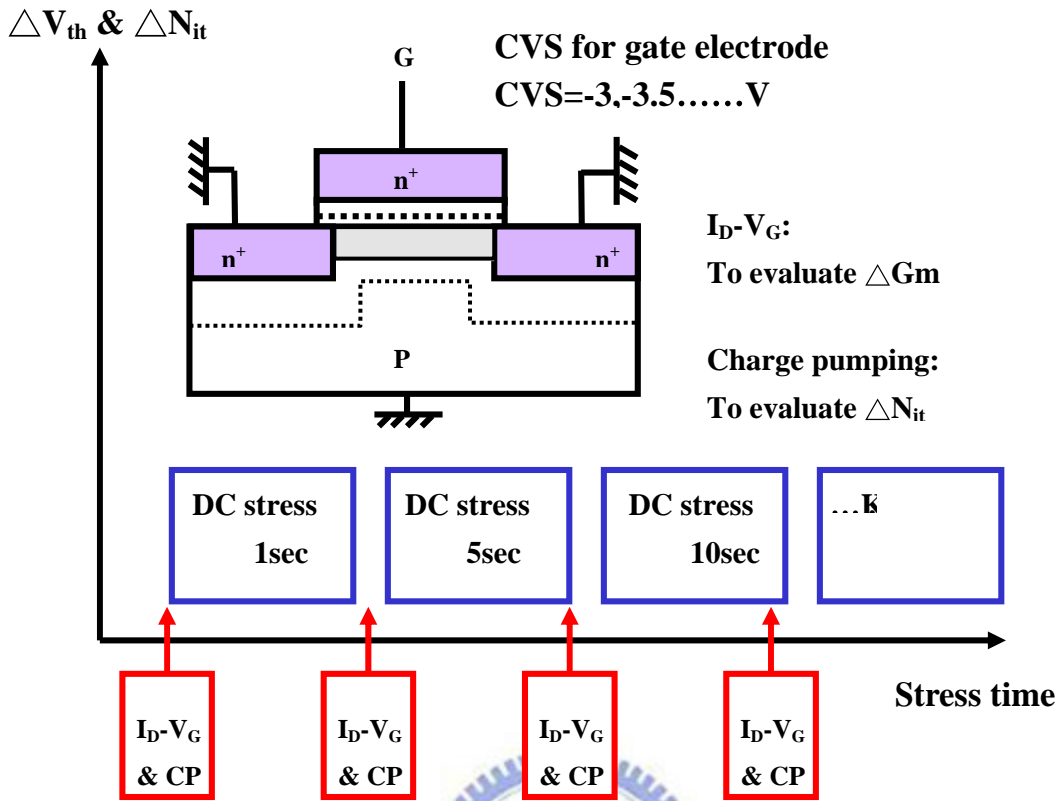
voltage shift and huge interface state variations at $V_g = 1/3 V_d$ condition. Fig.3-9 shows oxynitride suffers hot-carrier-injection in worse case $V_g=1/3V_d$, and obtains long lifetime.

Besides, Fig 3-10(a) and Fig.3-10(b) shows the comparison HCI with CVS. We observe that almost the same interface state density shift but more serious threshold instability represent with CVS. It hints that extra voltage stress to drain electrode and therefore some electrons have probability to run to drain electrode. Therefore, less electrons surpass barrier height and generate less oxide traps. This is why less threshold voltage shift obtains with HCI.

3-3-3 Summary

From SILC and HCI characteristics, it turns out that the film shows its robust property. Currently, gate oxide failure is reported to be a limiting factor for the scaling of oxide thickness. Owing to its significant reduction of lower leakage current, oxynitride film can extend the scaling limit of SiO_2 in terms of dielectric reliability as well as stand-by power consumption. Again, this implies that this new process can provide a high-quality gate dielectric film.





(a)

(b)

Fig 3-1 Basic measurement method for (a) CVS (b) HCI

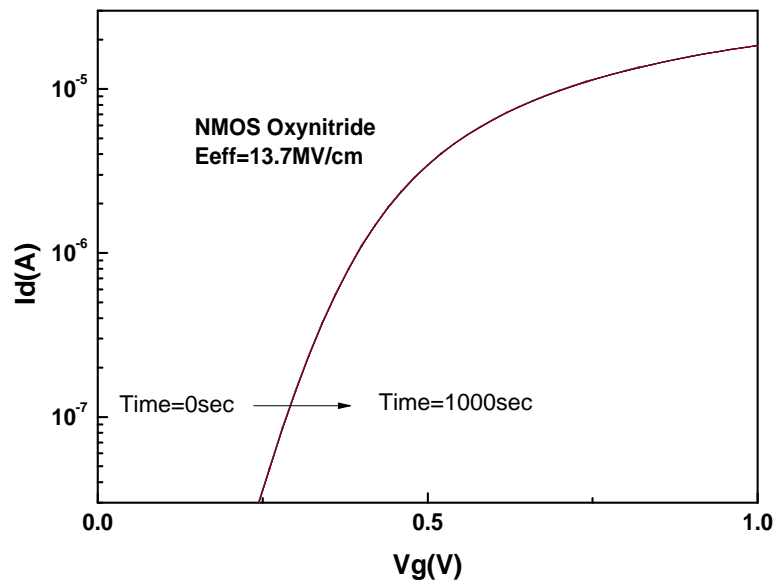


Fig.3-2(a) I_d - V_g characteristics for n^+ -gate nMOSFETs before stress and after stress 1000 s at 25 °C with oxynitride.

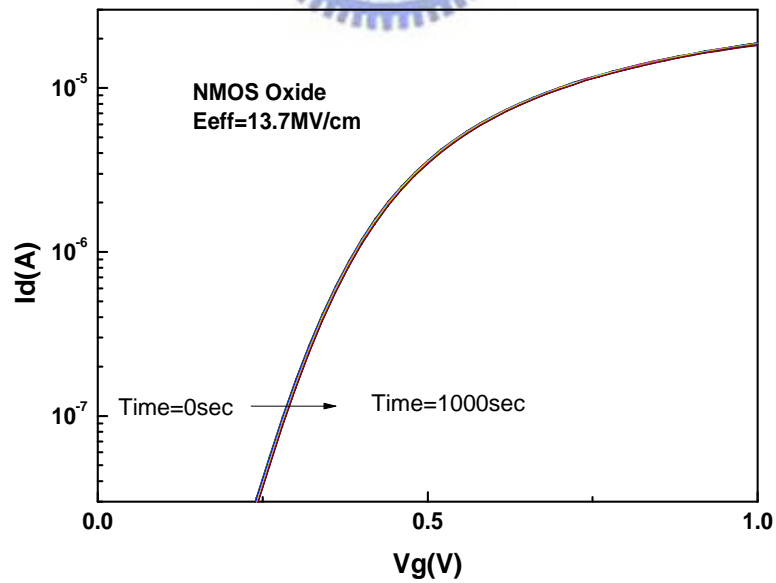
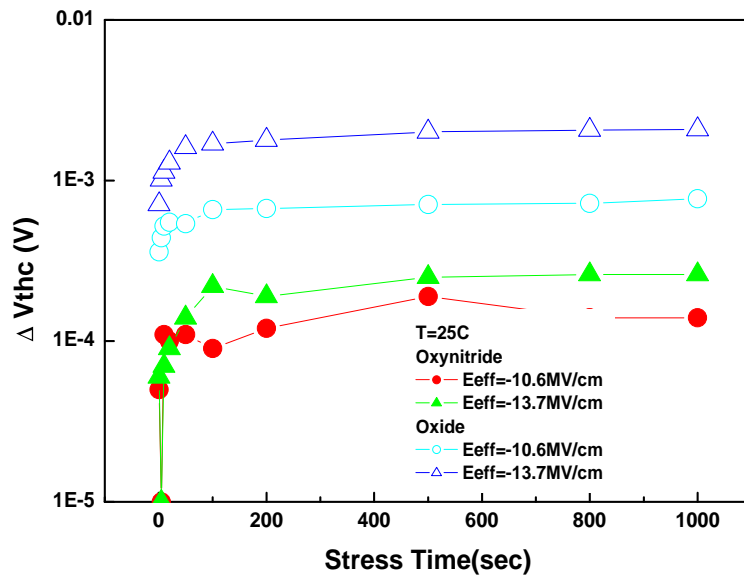
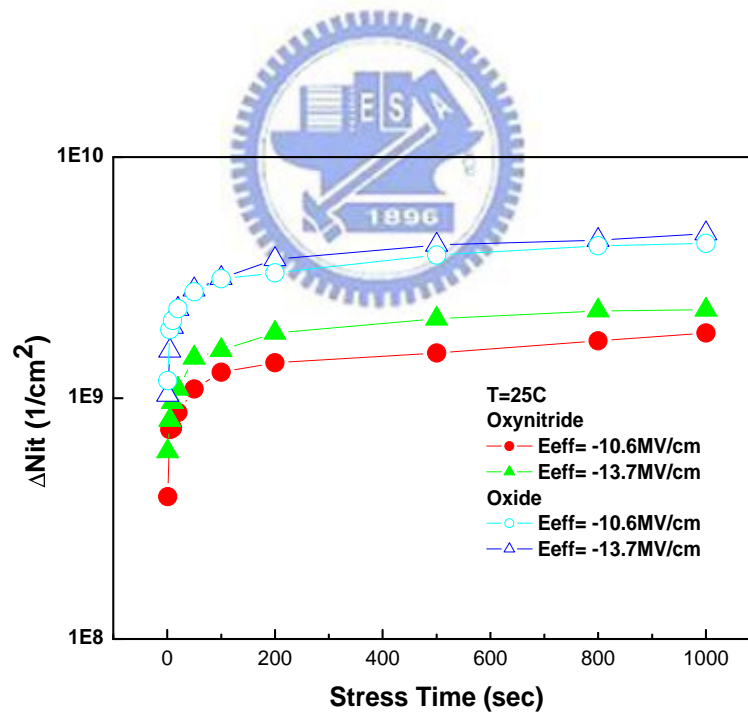


Fig.3-2(b) I_d - V_g characteristics for n^+ -gate nMOSFETs before stress and after stress 1000 s at 25 °C with conventional oxide.

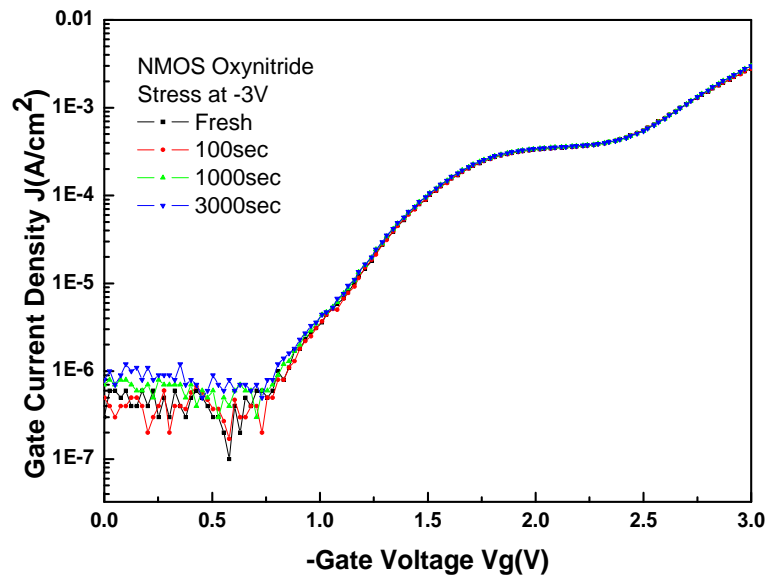


(a)

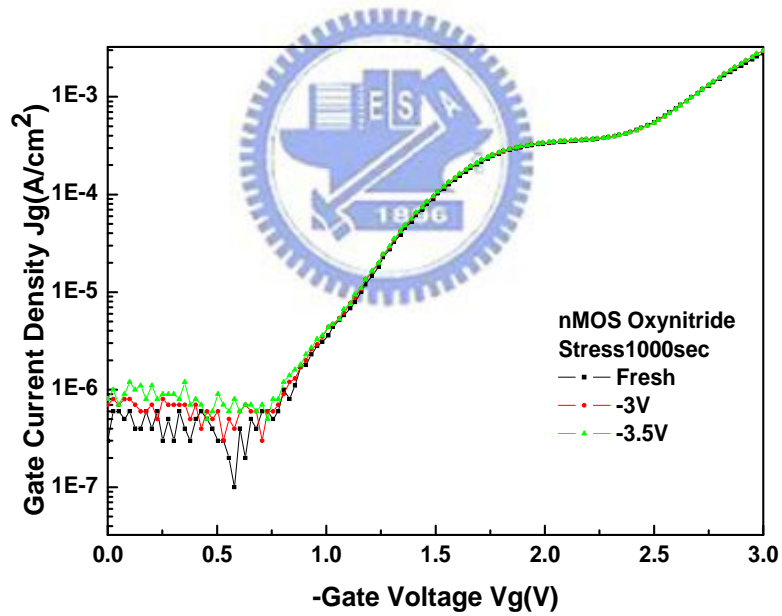


(b)

Fig.3-3 (a) Threshold voltage shift , and (b) Interface trap density shift as a function of stress time which compares oxynitride with oxide.

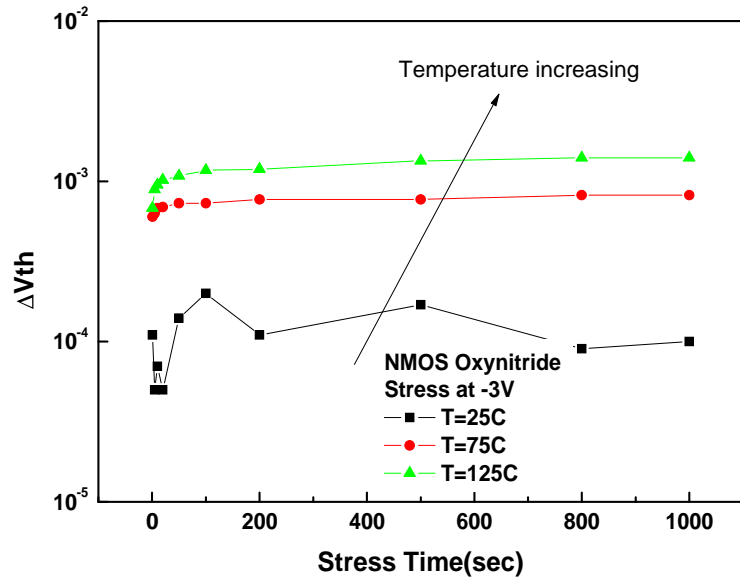


(a)

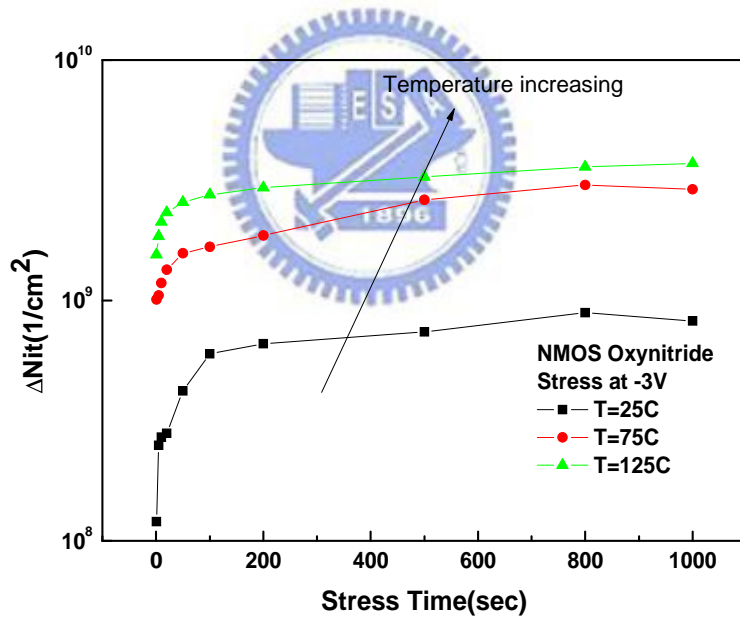


(b)

Fig.3-4 SILC under constant voltage stress during different (a) voltage stress and (b) time stress for oxynitride film.



(a)



(b)

Fig.3-5 (a) Threshold voltage shift , and (b) Interface trap density shift with different temperature in oxynitride.

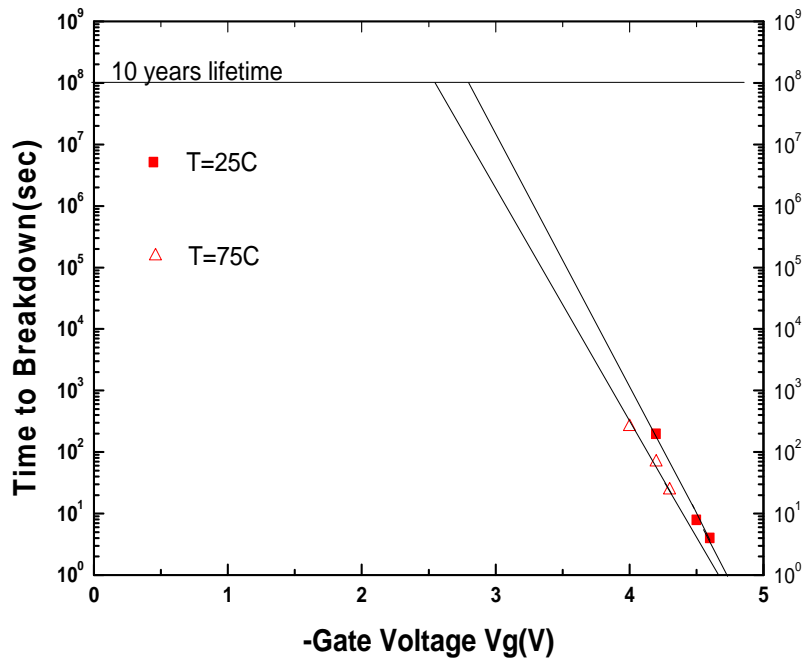


Fig.3-6 Comparison of intrinsic lifetime projection for oxynitride film in different temperature.



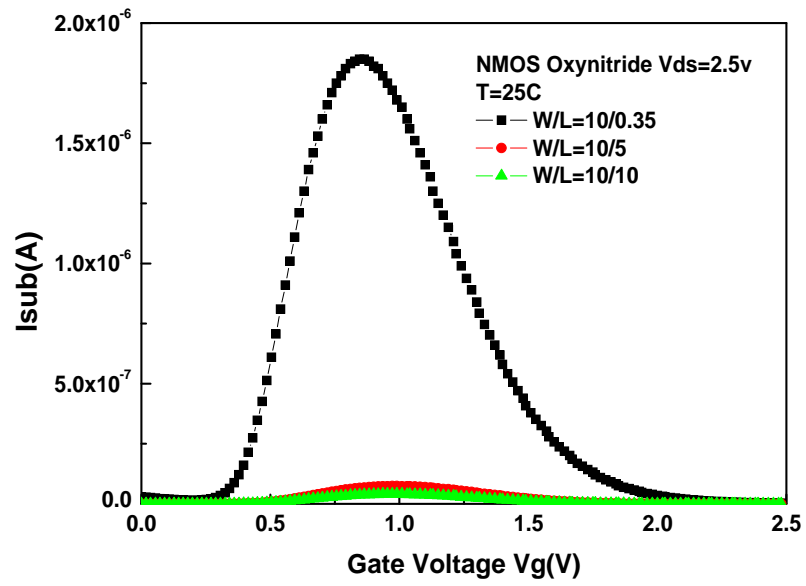
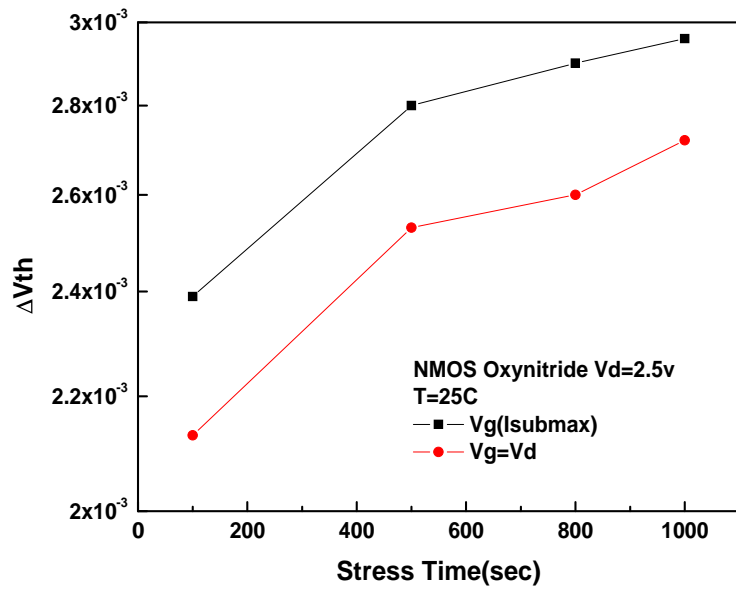
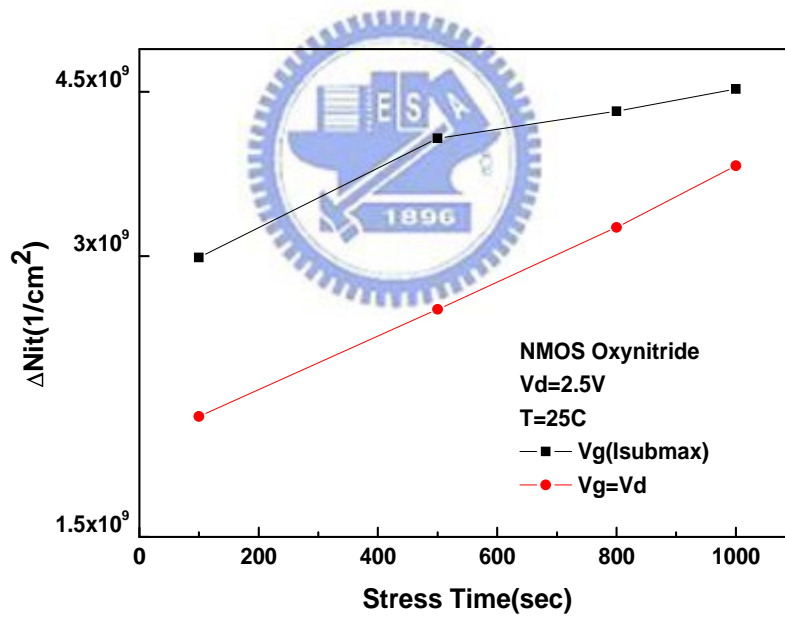


Fig.3-7 Substrate current versus gate voltage with channel lengths of 10um , 5um and 0.35um.





(a)



(b)

Fig.3-8 (a) Threshold voltage shift, and (b) Interface trap density shift with different HCI methods.

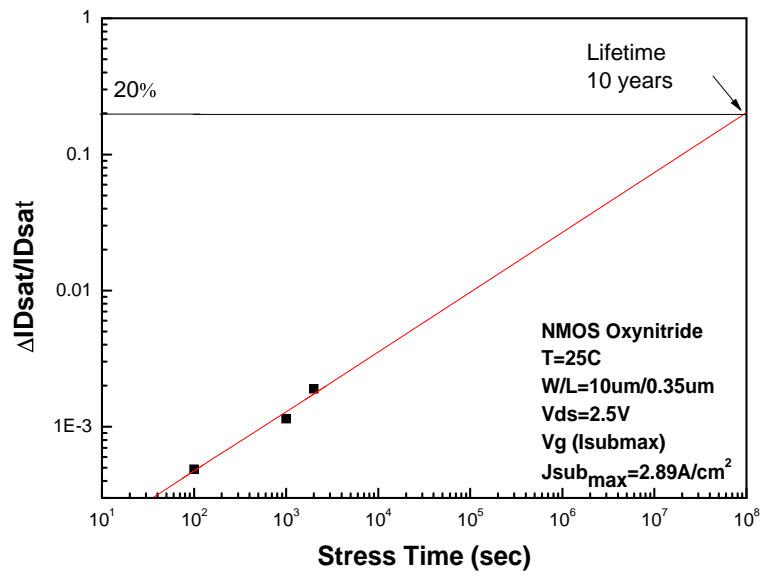
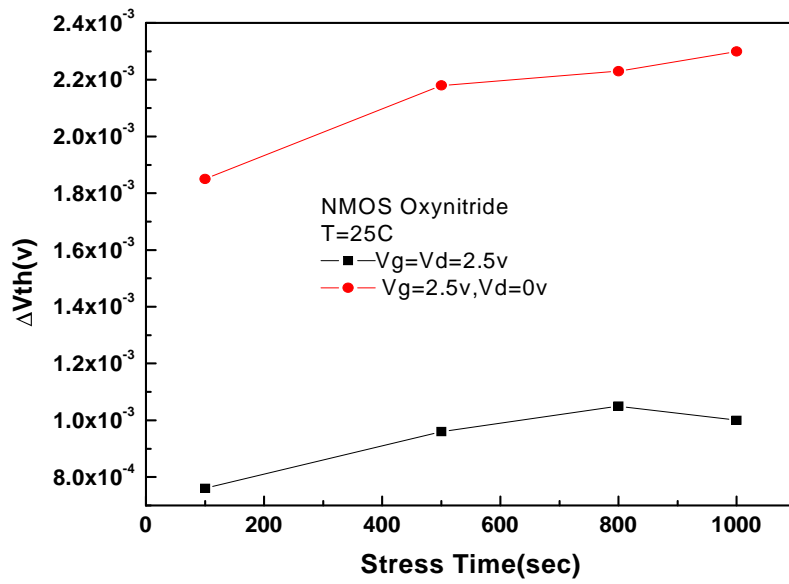
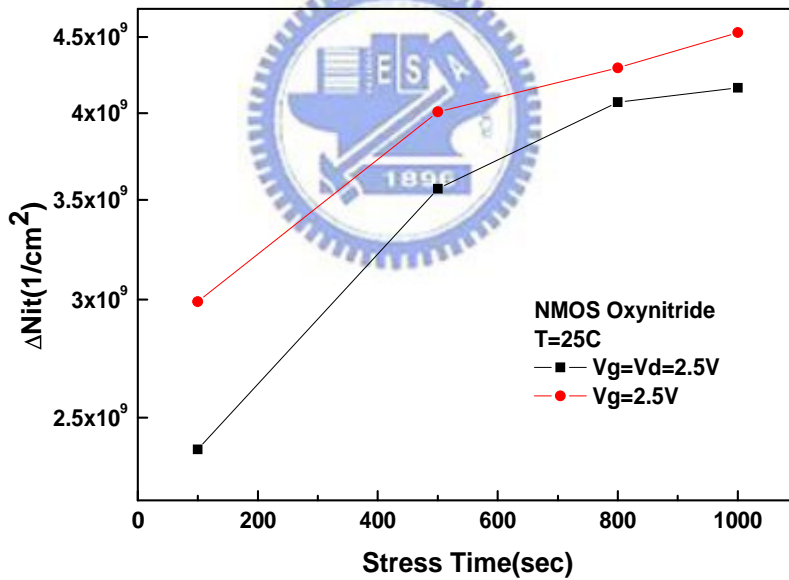


Fig . 3 - 9 H C I l i f e t i m e f o r o x y n i t r i d e .





(a)



(b)

Fig.3-10(a) Threshold voltage shift, and (b) Interface trap density shift as a function of stress time which compares HCI with CVS.