

References

Chapter 1

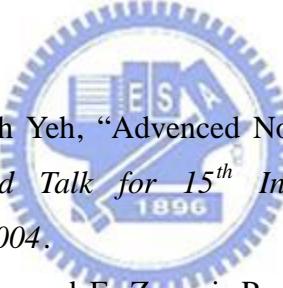
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論文題目：

鎳矽氧化物與鎳矽氮化物奈米點在非揮發性記憶

體應用之研究

Study on the Application of Ni-Si-O and Ni-Si-N

Nanocrystal for Nonvolatile Memory

著作目錄(Publication List)

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專利：

中華民國專利

1. 張鼎張、陳緯仁、劉柏村、涂峻豪、張俊彥、葉睿龍，「以鎳矽氧化物(NiSixOy)與鎳矽氮化物(NiSixNy)作為儲存層的非揮發性記憶體結構與其製作方法」(申請中)