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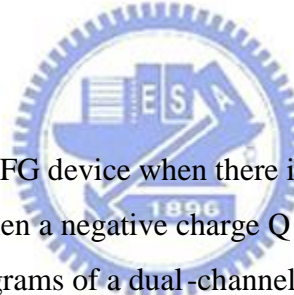RTA process at 600 ℃.

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Figure Captions

Chapter 1

Figure 1-1 The structure of the conventional floating gate nonvolatile memory device. Continuous poly-Si floating gate is used as the charge storage element.

Figure 1-2 The development of the gate stack of SONOS EEPROM memory devices. The optimization of nitride and oxide films has been the main focus in recent years.

Figure 1-3 The structure of the SONOS nonvolatile memory device. The nitride layer is used as the charge-trapping element.

Figure 1-4 The structure of the nanocrystal nonvolatile memory device. The semiconductor nanocrystals or metal nanocrystals are used as the charge storage element instead of the continuous poly-Si floating gate.

Chapter 2

Figure 2-1 I–V curves of an FG device when there is no charge stored in the FG (curve A) and when a negative charge Q is stored in the FG (curve B).

Figure 2-2 Energy band diagrams of a dual-channel SONOS transistor under (a) program (b) erase operation. electrons, holes.

Figure 2-3 (a) Schematic cross-section of nanocrystal memory device structure; (b) illustration of write process: inversion-layer electron tunnels into the nanocrystal; (c) illustration of erase process: accumulation layer hole tunnels into the nanocrystal, electron in nanocrystal can tunnel back to the channel.

Figure 2-4 Fourth approaches to programming methods, described by Hu and White. (a) Direct tunneling (DT) (b) Fowler-Nordheim tunneling (FN) (c) modified Fowler-Nordheim tunneling (MFN) (d) trap assistant tunneling (TAT).

Figure 2-5 Schematic cross section of MOSFET. The energy-distribution function at point (X_1, Y_1) is also shown.

Chapter 3

Chapter 4