Chapter 3

Formation and nonvolatile memory effect of Ni-Si-O and Ni-Si-N nanocrystal

3.1 Motivation

Nonvolatile memory (NVM) plays an important role in the market of portable electronic products and current requirements of further NVM are the high density cells, low-power consumption, high-speed operation and good reliability for the scaling down devices [3.1-3.3]. However, all of the charges stored in the floating gate will leak into the substrate if the tunnel oxide has a leakage path in the conventional NVM during endurance test. Therefore, the tunnel oxide thickness is difficult to scale down in terms of charge retention and endurance characteristics. The nonvolatile nanocrystal memories are one of promising candidates to substitute for conventional floating gate memory, because the discrete traps as the charge storage media have effectively improved data retention under endurance test for the scaling down device [3.4, 3.5]. The metal nanocrystal memories were extensively investigated over semiconductor nanocrystal, because of several benefits, such as enhanced control ability of gate (i.e. stronger coupling with the conduction channel), higher density of states (DOS), smaller energy disturbance and larger work function (faster programming time and better data retention) [3.5,3.6]. A nonvolatile memory device for various metal nanocrystals has been formed by several experiment techniques, for instance, self-assembled of tungsten (W) nanocrystal by using thermal oxidation process [3.7], separation of nickel (Ni) or gold (Au) nanocrystal by direct thermal annealing [3.8, 3.9], formation of platinum (Pt) or cobalt (Co) nanocrystal by using molecular beam epitaxy (MBE) [3.10, 3.11].

In recent years, nickel silicide has been widely used in advanced CMOS device as contact and interconnection materials. The larger work function of nickel silicide is ~5eV

within the silicon bandgap which enhances better retention. Most important of all, nickel silicide can be formed at low temperature annealing [3.12]. As a result of those advantages, nickel silicide is chosen as the storage material of memory device. Its implementation is compatible with the current manufacturing technology of semiconductor industry and represents a viable candidate for nonvolatile memory application.

Some methods have been developed recently for the preparation of Ni-Silicide metal nanocrystal nonvolatile memory. Such as, Yeh *et al.* fabricated of $NiSi_2$ nanocrystals embedded in SiO_2 with memory effect by oxidation of the amorphous $Si/Ni/SiO_2$ structure [3.13]. However, the formation of nanocrystals needs thermal oxidation process at high temperature 900 ^oC for a long duration. Chen *et al.* present the stacked Ni-Silicide nanocrystal memory was fabricated by sputtering a co-mix target ($Ni_{0.3}Si_{0.7}$) followed by RTO process [3.14]. Due to Ni atoms diffusing during the RTO process, the position and distribution of Ni silicide nanocrystals is random and uncontrollable.

The composition of deposited Ni silicide film was the critical process to determine the result of the size of the nanocrystals. In order to control thickness of the thin film more easily, a novel material target of sputter-deposited was used as the source of Ni silicide film. In the present research, the Ni-Silicide (Ni_xSi_{1-x}) was widely studied using cosputtering method (two targets used). However, it is difficult to uniformly control the component of the deposited Ni silicide thin film. The component of the film Ni_xSi_{1-x} can be well controlled using a co-mix target with a fixed component ratio. The target is manufactured by powder of Nickel (30%)-Silicon (70%) and it is compressed directly, not sintering. Atoms of this target do not interconnect so that it could use to deposit a fixed ratio film under low power operation.

In this thesis, we introduced oxygen incorporated $Ni_{0.3}Si_{0.7}$ layer as charge trapping layer by sputtering a co-mix target ($Ni_{0.3}Si_{0.7}$) in the argon (Ar) and oxygen (O_2) environment at room temperature. The purpose to initially incorporate oxygen in $Ni_{0.3}Si_{0.7}$ layer is to reduce the temperature and duration of thermal treatment for nanocrystal formation. In addition, the distribution of Ni silicide nanocrystals can be well controlled without Ni atoms diffusing during thermal oxidation. In previous reports, the charge trapping layer also can contain some Si-N bonds which increase trapping states to

improve charge storage capacity and reliability for the nonvolatile metal nanocrystal memory devices [3.15]. Another similar process for nitrogen incorporated $Ni_{0.3}Si_{0.7}$ layer is carried out by sputtering a co-mix target ($Ni_{0.3}Si_{0.7}$) in the argon (Ar) and nitrogen (N_2) environment.

3.2 Nonvolatile Ni-Si-O Nanocrystal Memory

3.2.1 Experimental Procedures

Figure 3-1(a) and (b) exhibit schematics of the experimental procedures. This nonvolatile memory-cell structure in this letter was fabricated on a 4 in. p-type silicon (100) wafer. After a standard RCA process which removed native oxide and micro-particles, 3-nm-thick tunnel oxide was thermally grown by a dry oxidation process in an atmospheric pressure chemical vapor deposition furnace (APCVD). Subsequently, a 10-nm-thick charge tapping layer was deposited by reactive sputtering of $Ni_{0.3}Si_{0.7}$ co-mix target in the Ar/O_2 (24 standard cubic centimeters per minute (sccm)/2sccm) ambiance at room temperature, and the DC sputtering power was set to 80 W. This step can obtain an oxygen incorporated $Ni_{0.3}Si_{0.7}$ layer as a charge trapping layer in our memory structure. Then, a 30-nm-thick blocking oxide was deposited by the plasma enhanced chemical vapor deposition (PECVD) system at 300 ^{o}C. During the foregoing process, the Ni-Si-O nanocrystals could be found to precipitate and embed in SiO_x layer. Al gate electrodes on back and front side of the sample were finally deposited and patterned to form a metal/oxide/insulator/oxide/silicon (MOIOS) structure. A control sample that went through the same processing steps except for the oxygen deficient $Ni_{0.3}Si_{0.7}$ film (by sputtering in the only Ar ambiance) was fabricated for comparison.

Electrical characteristics, including the capacitance-voltage (C-V), current density-voltage (J-V), retention, and endurance characteristics, were also performed. The J-V and C-V characteristics were measured by Keithley 4200 and HP4284 Precision LCR Meter with high frequency 100 kHz. In addition, Transmission electron microscope (TEM) and X-ray photoelectron spectroscopy (XPS) were adopted for the micro-structure analysis and chemical material analysis.

3.2.2 Results and Discussion

Figure 3-2(a) and (b) show cross-sectional TEM image of oxygen deficient $Ni_{0.3}Si_{0.7}$ layer and oxygen incorporated $Ni_{0.3}Si_{0.7}$ layer, respectively. There is non-isolated nanocrystal present in the oxygen deficient $Ni_{0.3}Si_{0.7}$ layer, as shown in Fig. 3-2(a). Without a well isolation from dielectric, discrete storage nodes does not exist to store charge. Figure 3-2(b) exhibits the oxygen incorporated $Ni_{0.3}Si_{0.7}$ layer containing spherical and separated nanocrystals. The average diameter of the nanocrystals is approximately 5-6 nm and the area density of the nanocrystals is estimated to be about 1.33×10^{12} cm^{-2}. Furthermore, it is found that the thickness of tunnel oxide is larger than 3 nm by TEM analysis, due to the contribution of SiO_x layer in the charge trapping layer (oxygen incorporated $Ni_{0.3}Si_{0.7}$ layer).

Capacitance-voltage (C-V) hysteresis obtained with oxygen deficient $Ni_{0.3}Si_{0.7}$ layer and oxygen incorporated $Ni_{0.3}Si_{0.7}$ layer are respectively shown in Fig. 3-3(a) and (b). From Fig. 3-3(a), it hasn't any memory window or charge storage ability to be found for this MOIOS structure of oxygen deficient $Ni_{0.3}Si_{0.7}$ layer. On the contrary, it is clearly observed that 0.8 V and 2.5 V memory windows can be obtained under ±10 V and ±15 V gate voltage operation, as shown in Fig. 3-3(b). Moreover, the hysteresis loops follow the counterclockwise due to injection of electrons from the deep inversion layer and discharge of electrons from the deep accumulation layer of Si substrate [3.16]. Hence, we can be enough to define "1" and "0" states using this nanocrystal memory structure. As a result, our electrical characteristics of C-V show that nonvolatile memory effect is influenced by oxygen doping.

The XPS analysis by using an Al $K\alpha$ (1486.6 eV) x-ray radiation is demonstrated the chemical composition of the charge trapping layer. To correct possible charging effect of the film, the binding energy was calibrated using the C 1s (284.6 eV) spectra of hydrocarbon that remained in the XPS analysis chamber as a contaminant. As shown in Fig. 3-4(a), the Ni $2p$ core-level photoemission spectra consist of two main $2p_{3/2}$ (854.5-855.8 eV) and $2p_{1/2}$ (873 eV) lines and corresponding satellites. According to previous research, the peak position and profile of Ni $2p_{3/2}$ are similar to Ni-Si-O signal by XPS analysis [3.17]. Hence, we can consider that the charge trapping layer is composed of Ni-Si-O ternary element. This consideration is also verified by the XPS O

1*s* photoemission spectra, as shown in Fig. 3-4(b). By the fitting result of experiment data, it is found that the main peak can be composed into two components which center at 531.5 eV and 532.4 eV corresponding to Ni-Si-O bond and Si-O-Si bond, respectively [3.18]. During the course of our investigation, we found that these nanocrystals are enough reasoned to be composed of Ni-Si-O ternary element and embedded in SiO_x. In addition, we can use XPS analysis to roughly define the atomic concentrations which nickel, silicon, and oxygen of charge trapping layer are 14%, 47%, and 39%, respectively.

The reliability issues, such as retention and endurance, were also tested in this work. Figure 3-5 demonstrates the data retention characteristics of the nonvolatile Ni-Si-O nanocrystal memory at room temperature. The memory cell is programmed by 10 V, 5 s, and -10 V, 5 s gate pulses for Data "1" and "0", respectively. The flat band voltage shift is obtained by comparing the *C-V* curves from a charged state and the quasi-neutral state. The memory window significantly decays during the first 100 s due to charge emission from the shallow traps in SiO_x (partial oxidized *a*-Si) matrix. However, a 1.2 V memory window (charge remained ratio of 40%) from the elongation line of the decay trend can obtain even after 10 years. Endurance characteristics for Ni-Si-O nanocrystals embedded in SiO_x matrix are shown in Fig. 3-6. Pulses ($V_G - V_{FB} = \pm$ 5 V, 0.1 ms) were applied to evaluate endurance characteristics for the P/E operations. The obvious closure of voltage window between the program and erase state results from degradation of SiO_x dielectric. It is also believed that the SiO_x quality is much worse than the tunnel oxide. The defect generation under P/E operation will increase leakage paths and degrade the charge storage capability. However, it retains a memory window of 0.6V which is enough to define "1" and "0" of memory states.

3.3 Nonvolatile Ni-Si-N Nanocrystal Memory

3.3.1 Experimental Procedures

Figure 3-7 indicates a schematic of experimental procedures. This memory-cell structure was fabricated on a 4 in. p-type silicon (100) wafer. After a standard RCA process which removed native oxide and micro-particles, 3-nm-thick tunnel oxide was

thermally grown by a dry oxidation process in an atmospheric pressure chemical vapor deposition furnace (APCVD). Subsequently, a 10-nm-thick nitrogen incorporated $Ni_{0.3}Si_{0.7}$ layer was deposited by reactive sputtering of $Ni_{0.3}Si_{0.7}$ co-mix target in the Ar (24 sccm) and N_2 (10 sccm) environment at room temperature, and the DC sputtering power was set to 80 W. Then, a 30-nm-thick blocking oxide was deposited by the plasma enhanced chemical vapor deposition (PECVD) system at 300 ^{o}C. Hence, the Ni-Si-N ternary nanocrystals could be found to precipitate and embed in SiN_x during the foregoing process. Al gate electrodes on back and front side of the sample were finally deposited and patterned to form a metal/oxide/insulator/oxide/silicon (MOIOS) structure.

Electrical characteristics, including the capacitance-voltage (C-V), current density-voltage (J-V), retention, and endurance characteristics, were also performed. The J-V and C-V characteristics were measured by Keithley 4200 and HP4284 Precision LCR Meter with high frequency 100 kHz. In addition, Transmission electron microscope (TEM) and X-ray photoelectron spectroscopy (XPS) were adopted for the micro-structure analysis and chemical material analysis.

3.3.2 Results and Discussion

Figure 3-8 exhibits a cross-sectional HRTEM image of the nitrogen incorporated $Ni_{0.3}Si_{0.7}$ layer containing spherical and separated nanocrystals embedded in the SiN_x matrix. It is found that the thickness of tunnel oxide is larger than 3 nm, due to the contribution of SiN_x layer by HRTEM analysis. This SiN_x matrix can be used to improve charge storage ability for nonvolatile memory application [3.19]. Moreover, the average diameter of the nanocrystals is approximately 5-6 nm and the area density of the nanocrystals is estimated to be about 1.08×10^{12} cm^{-2} by HRTEM analysis.

To further investigate the nanocrystal, we have performed XPS analysis by using an Al *Kα* (1486.6 eV) X-ray radiation to demonstrate the chemical composition of the nanocrystals. To correct possible charging effect of the film, the binding energy was calibrated using the C 1s (284.6 eV) spectra of hydrocarbon that remained in the XPS analysis chamber as a contaminant. Figure 3-9(a) shows the XPS Ni 2*p* core-level photoemission spectra which consist of two main peaks, $2p_{3/2}$ (~ 855 eV) and $2p_{1/2}$ (~ 873 eV), with two small satellite peak. According to other literature values, Ni $2p_{3/2}$ binding

energies are at 852.3 eV and 853.4 eV for metallic nickel (Ni–Ni) and Ni-silicide (Ni–Si), respectively [3.20]. However, above-mentioned peak signals are not obviously observed at the Ni $2p_{1/2}$ peak by XPS analysis. Due to the strong electronegativity of nitrogen atom, it is reasonably assumed that the larger Ni $2p_{1/2}$ binding energy (~ 855 eV) of the nanocrystals can be assigned to Ni–Si–N ternary bond. This result is also supported by the XPS N 1*s* photoemission spectra, as shown in Fig. 3-9(b). By the fitting result of binding energy, it is found that the main peak can be compose into two components which center at 398.5 eV and 397 eV corresponding to Si–N bond and Ni–N bond, respectively [3.21,3.22]. In addition, we can use XPS analysis to roughly define the atomic concentrations which nickel, silicon, and nitrogen of charge trapping layer are 16.6%, 56%, and 27.4%, respectively.

The typical capacitance-voltage (*C-V)* hysteresis obtained with gate voltage from accumulation to inversion and in reverse is shown in Fig. 3-10. It is clearly observed that 1.5 V and 3.5 V memory windows can be obtained under ±10 V and ±12 V operation, respectively. The MOIOS structure with the Ni-Si-N nanocrystals embedded in SiN_x matrix exhibits clear counterclockwise hysteresis by a flat band voltage (V_{FB}) shift, indicating the significant memory effect. We consider that the charges can be stored in both the Ni-Si-N nanocrystal and the SiN_x traps. Moreover, the hysteresis loops follow the counterclockwise due to injection of electrons from the deep inversion layer and discharge of electrons from the deep accumulation layer of Si substrate. Hence, this memory window of Ni-Si-N nanocrystals embedded in SiN_x matrix is enough to be defined “1” and “0” states.

Retention characteristics of the memory structure with Ni-Si-N nanocrystals are illustrated in Fig. 3-11. The retention measurements are performed at room temperature by operating a ±10 V gate voltage stress for 5 s. The flat band voltage shift is obtained by comparing the *C-V* curves from a charged state and the quasi-neutral state. When carriers are stored in the nanocrystals, the stored charges will raise the nanocrystal potential energy and increase the probability of escaping from the nanocrystal to the silicon substrate [3.23]. Moreover, carriers trapped in the shallow traps are unstable and can easily leak back to the silicon substrate. It is found that the window of V_{FB} significantly reduces during the first 100 s, and becomes more stable for long retention time. This

result is consistent with partial carriers trapping in the shallow trap state of the SiN_x matrix around the nanocrystals. However, the long-term extrapolated gives a memory window of 1.4V (total charge loss ratio 50%) after ten years. The majority carriers stored in the deep trapping states of Ni-Si-N nanocrystals surrounding with SiN_x matrix exhibit good retention characteristics.

Endurance characteristics for Ni-Si-N nanocrystals embedded in SiN_x matrix are shown in Fig. 3-12. Pulses (V_G - V_{FB} = ± 5 V, 0.1 ms) were applied to evaluate endurance characteristics for the P/E operations. An obvious difference of two logical states can be maintained until 10^4 P/E cycles. Subsequently, the closure of window between two logical states appears after 10^4 P/E cycles. We consider that this closure is caused by the degradation of SiN_x dielectric. However, this memory structure exhibits better endurance characteristics than Ni-Si-O nanocrystal memory. This result will be integrated and discussed in the Chapter 4. Consequently, it retains a large window of 1V which is enough to define "1" and "0" of memory state.

3.4 Mechanism of Ni-Si-O and Ni-Si-N Nanocrystal Formation by DC Sputter at Room Temperature

3.4.1 Gibbs free energy

In thermodynamics, the Gibbs free energy is a thermodynamic potential which measures the "useful" or process-initiating work obtainable from an isothermal, isobaric thermodynamic system. When a system changes from a well-defined initial state to a well-defined final state, the Gibbs free energy (ΔG) equals the work exchanged by the system with its surroundings, less the work of the pressure forces, during a reversible transformation of the system from the same initial state to the same final state. The change (ΔG) in Gibbs free energy is a parameter to measure a spontaneous tendency of the reaction. The ΔG is usefully defined by

$$\Delta G = \Delta H - T\Delta S$$

Where H is the enthalpy, T is temperature, and S is the entropy. If ΔG is negative, the reaction is a spontaneous. If ΔG is positive, the reverse reaction is a spontaneous. The larger ΔG value indicates that the reaction is easier to take place with higher reaction rate.

After reaction, the ΔG value represents the energy which is released as heat to the environment. At chemical equilibrium, the rate of forward reaction is equal to the rate of reverse reaction, $\Delta G = 0$. In generally, the ΔG value is nearly dominated by the enthalpy (ΔH) because the $T\Delta S$ value is much less than ΔH.

3.4.2 Results and Discussion

Figure 3-13(a), (b), and (c), respectively, show cross-sectional TEM image of oxygen and nitrogen deficient $Ni_{0.3}Si_{0.7}$ layer, oxygen incorporated $Ni_{0.3}Si_{0.7}$ layer, and nitrogen incorporated $Ni_{0.3}Si_{0.7}$ layer which are directly capped by Al metal film. This intention is to exclude the influence of PECVD blocking oxide deposition at 300 ^{o}C for nanocrystal formation. Obviously, there is non-isolated nanocrystal present in the uniform $Ni_{0.3}Si_{0.7}$ layer, as shown in Fig. 3-13(a). In contrast, Figure 3-13(b) exhibits the oxygen incorporated $Ni_{0.3}Si_{0.7}$ layer containing spherical and separated nanocrystals. To further research the formation of Ni-Si-O nanocrystal, the enthalpies ($-\triangle H$) of Si–O and Ni–O at room temperature, are 799 and 382 kJ mol $^{-1}$, respectively [3.24]. Hence, because of the higher enthalpy of Si–O compared with Ni–O, the oxygen radicals can interact with Si atom easier than Ni atom during the sputter process. When oxygen and silicon atom joint to form bonding, will release energy as heat to the environment. The self-assembled phenomenon of Ni-Si-O nanocrystal can be explained that the released energy will induce Ni atoms to diffuse in the SiO_x during the sputtering process. Therefore, we can be simple and uniform to form Ni-Si-O nanocrystals at low temperature by our experimental method. A similar result, as shown in Figure 3 -13(c), the clear Ni-Si-N nanocrystal image distributes in the nitrogen incorporated $Ni_{0.3}Si_{0.7}$ layer. For chemical characteristics of Si–N and Ni–N, the enthalpies ($-\triangle H$) at room temperature, are 470 and 70~85 kJ mol $^{-1}$, respectively [3.24,3.25]. Hence, because of the higher enthalpy of Si–N compared with Ni–N, the N radicals can interact with Si atom easier than Ni atom during the sputtering process. Similarly, when nitrogen and silicon atom joint to form bonding, will release energy as heat to the environment. The self-assembled phenomenon of Ni-Si-N nanocrystal can be explained that the released energy will induce Ni atoms to diffuse in the SiN_x during the sputtering process. In the previous research, Ni atom can diffuse in the SiN_x even at room temperature and

formation of a Ni-Si-N ternary solid solution [3.26]. Therefore, the nanocrystals are simple and uniform to be formed at low temperature by sputtering a co-mix target in the Ar/N_2 environment.

3.5 Comparison of Electrical Characteristics between Ni-Si-O and Ni-Si-N Nanocrystal Nonvolatile Memory

The comparisons of memory window and nanocrystal density between two type nonvolatile memory devices are listed in Table 3-1. The estimated density of Ni-Si-O nanocrystal by TEM analysis is close to that of Ni-Si-N nanocrystal. Compared with Ni-Si-O nanocrystal embedded in SiO_x, Ni-Si-N nanocrystal embedded in SiN_x as charge trapping layer exhibits lager memory window under ±10V operation. Additional accessible charge trap states in SiN_x matrix cause the much larger memory effect [3.19]. From an electrostatics consideration, SiN_x matrix with a higher dielectric constant will cause a smaller voltage drop across the charge trapping layer and a greater voltage drop across the tunnel oxide. This will result in increasing of the electric field across the tunnel oxide, and charges can tunnel more efficiently from substrate into the trapping layer.

The current density-voltage (J-V) characteristics of different MOIOS structure by gate voltage sweeping from 0 V to 10 V and 0 V to -10 V are shown in Fig. 3-14. It is clear that the leakage current of the memory structures containing Ni-Si-O or Ni-Si-N nanocrystals is significantly reduced as compared to that of control sample. This result can be explained introducing the coulomb blockade effect. From Fig. 3-3(a), it shows neglectful C-V hysteresis for control sample with oxygen deficient $Ni_{0.3}Si_{0.7}$ layer. In contrast, the structures containing Ni-Si-O or Ni-Si-N nanocrystals exhibit charge storage capability demonstrated in Fig. 3-3(b) and Fig. 3-10. The electron charge will raise the nanocrystal potential energy and reduce the electric field across the tunnel oxide, resulting in reduction of the tunneling current density.

Table 3-2 lists the retention characteristics for Ni-Si-O and Ni-Si-N nanocrystal nonvolatile memory. The NiSiN nanocrystal embedded in SiN_x shows enhanced retention characteristics, that is, a larger long-term extrapolated window of 1.4V (charge remained ratio of 50%) is maintained after ten years. According to previous research [3.19], the

charge can be shared among the nitride trap, the enhanced field by stored charge (Coulomb blockade) through the tunneling oxide can be reduced. This result decreases the probability of charge escaping from the nanocrystal. Moreover, charges are likely to be relaxed to the nitride traps. Leakage through the intermediate medium can also be inefficient due to Coulomb blockade. Therefore, carriers stored in nanocrystal can not easily leak back to the silicon substrate.

3.6 Summary I

The nonvolatile memory structure of Ni-Si-O nanocrystals embedded in the SiO_x layer was fabricated by sputtering a co-mix target ($Ni_{0.3}Si_{0.7}$) in an Ar/O_2 environment at room temperature. It can be considered that the oxygen plays a critical role during sputter process for the formation of nanocrystal. The self-assembled phenomenon of Ni-Si-O nanocrystal can be explained that the released energy will induce Ni atoms to diffuse in the SiO_x during the sputtering process. The high density ($\sim 10^{12}$) nanocrystal can be simple and uniform to be fabricated in this study. The memory window of nickel-silicon-oxygen nanocrystals enough to define "1" and "0" states is clearly observed for the nonvolatile memory application. The retention and endurance characteristic are good enough to be maintained after 10 years and 10^6 P/E cycles. In addition, this novel and ease fabrication technique of Ni-Si-O nanocrystals can be compatible with current manufacture process of the integrated circuit manufacture.

Another similar process for Ni-Si-N nanocrystals is also proposed by sputtering a co-mix target ($Ni_{0.3}Si_{0.7}$) in the argon (Ar) and nitrogen (N_2) mix-gas environment at room temperature. It was found that high density Ni-Si-N nanocrystals embedded in the silicon nitride (SiN_x). The self-assembled phenomenon of Ni-Si-N nanocrystal can be explained that the released energy will induce Ni atoms to diffuse in the SiN_x during the sputtering process. A larger memory window of 3.5 V was observed after ±12V voltage sweep as compared with Ni-Si-O nanocrsytal memory. This improvement is attributed to additional accessible charge trap states in the SiN_x matrix. Furture, the heterogeneous charge trapping layer by combining Ni-Si-N nanocrystals and SiN_x exhibits better retention and endurance characteristics than Ni-Si-O nanocrsytal.

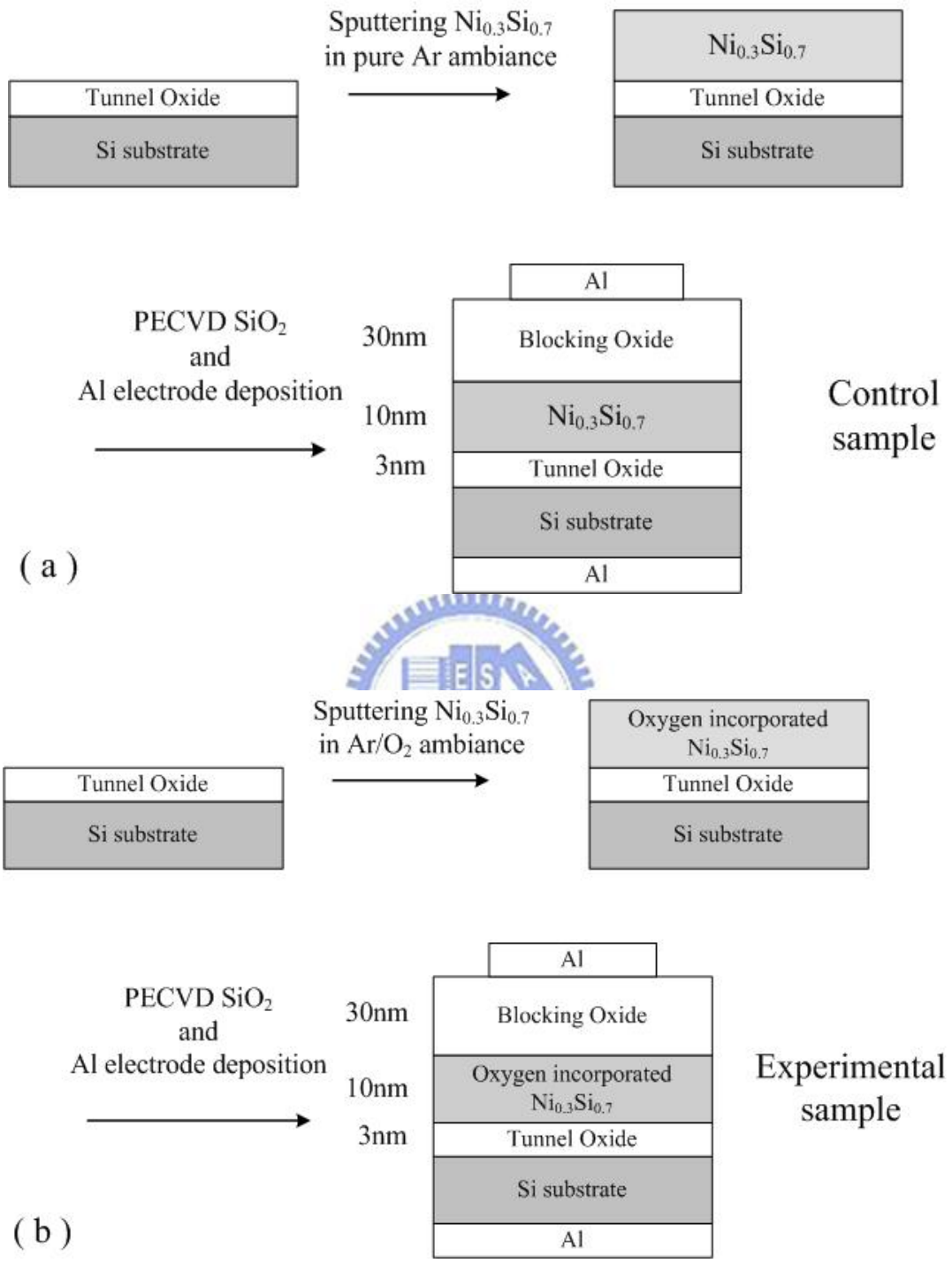
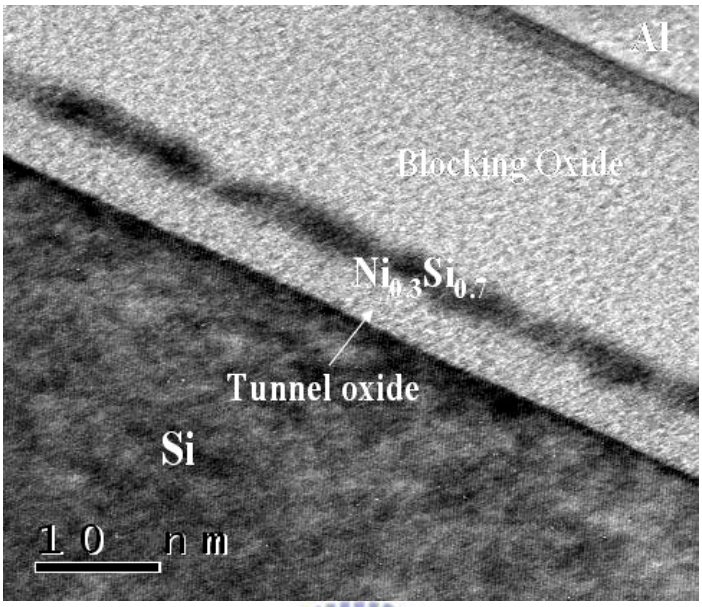
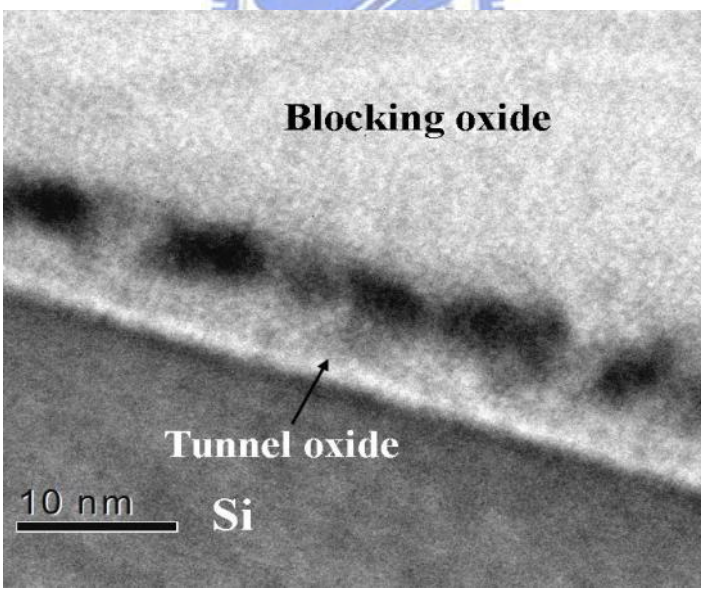


Figure 3-1 Schematics of the experimental procedures. (a) Oxygen deficient $Ni_{0.3}Si_{0.7}$ layer and (b) Oxygen incorporated $Ni_{0.3}Si_{0.7}$ layer as charge trapping layer.

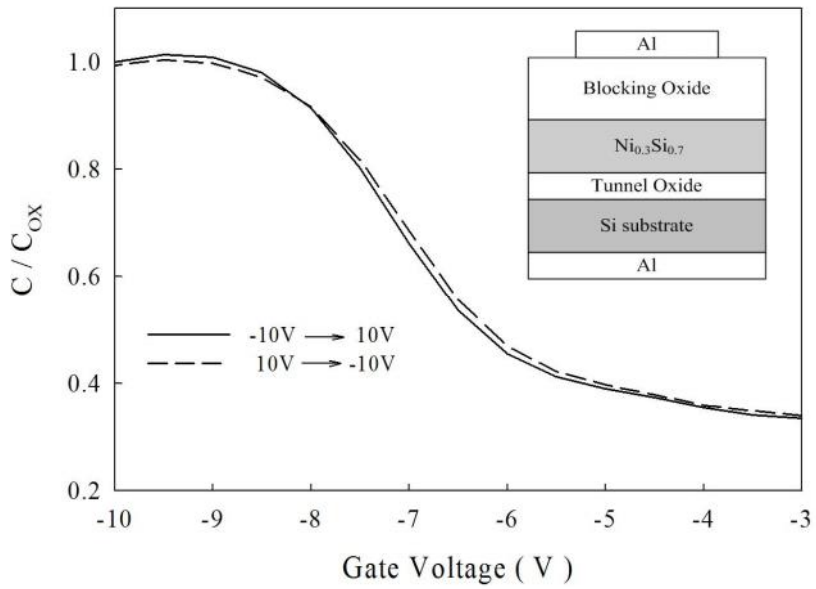


(a)

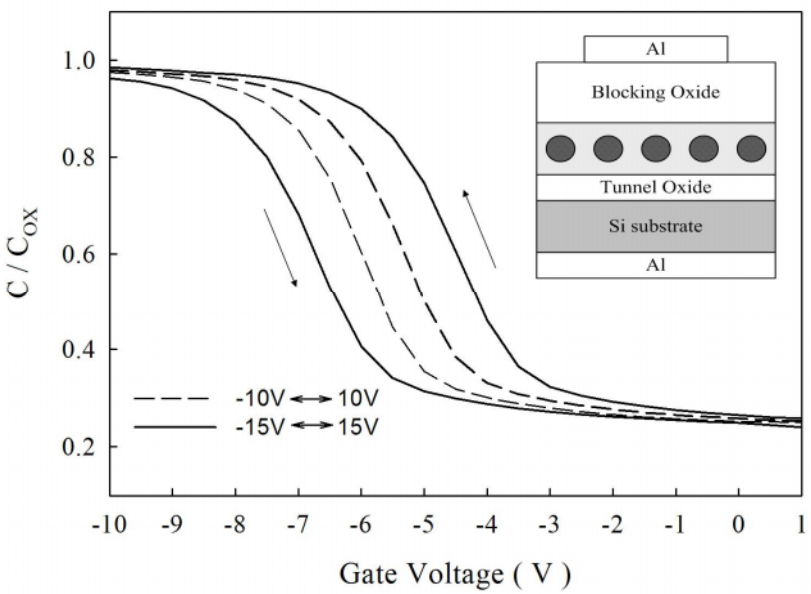


(b)

Figure 3-2 Cross-sectional TEM images of the MOIOS structure with (a) oxygen deficient $Ni_{0.3}Si_{0.7}$ layer and (b) oxygen incorporated $Ni_{0.3}Si_{0.7}$ layer, respectively.



(a)



(b)

Figure 3-3 Capacitance-voltage (C-V) hysteresis of the fabricated MOIOS structure with (a) oxygen deficient $Ni_{0.3}Si_{0.7}$ layer and (b) oxygen incorporated $Ni_{0.3}Si_{0.7}$ layer.

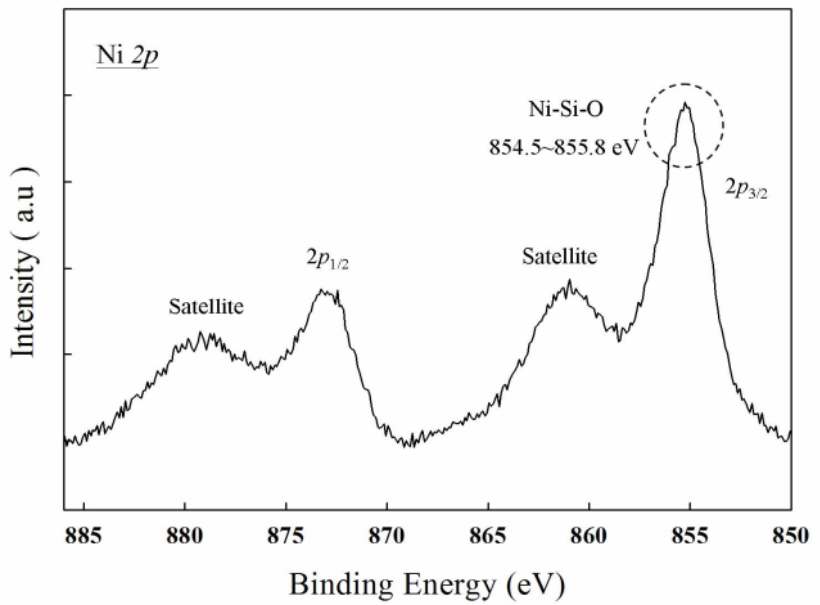


Figure 3-4(a) Ni 2*p* XPS analysis of the oxygen incorporated $Ni_{0.3}Si_{0.7}$ layer. The peak position and profile of Ni $2p_{3/2}$ are similar to Ni-Si-O signal.

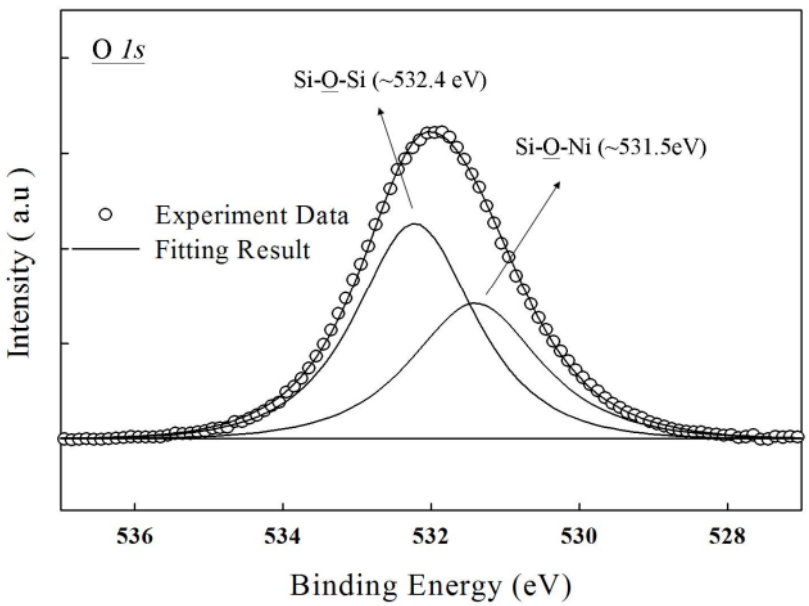


Figure 3-4(b) O 1*s* XPS analysis of the oxygen incorporated $Ni_{0.3}Si_{0.7}$ layer. Empty circles and straight line indicate experimental and fitting results, respectively. The main peak can be composed into two components which center at 531.5 eV and 532.4 eV corresponding to Ni-O-Si bond and Si-O-Si bond.

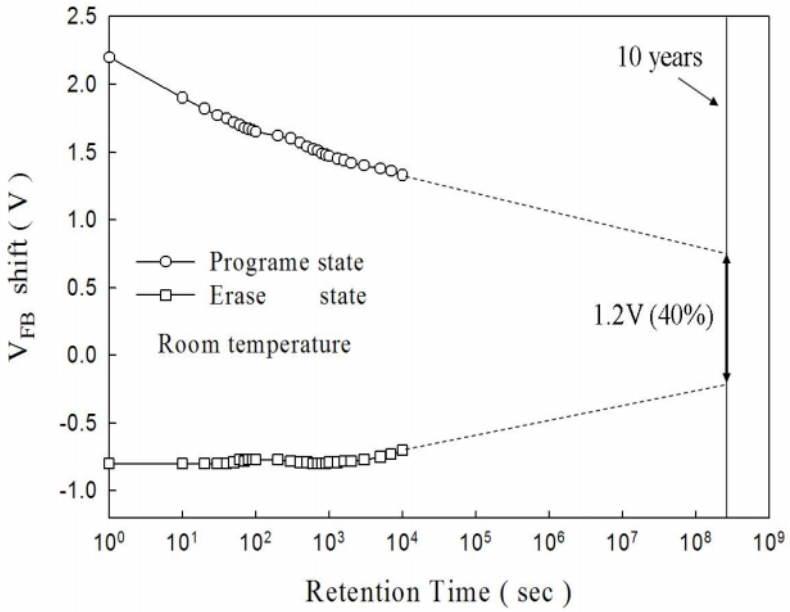


Figure 3-5 Data retention characteristics of the Ni-Si-O nanocrystal memory at room temperature.

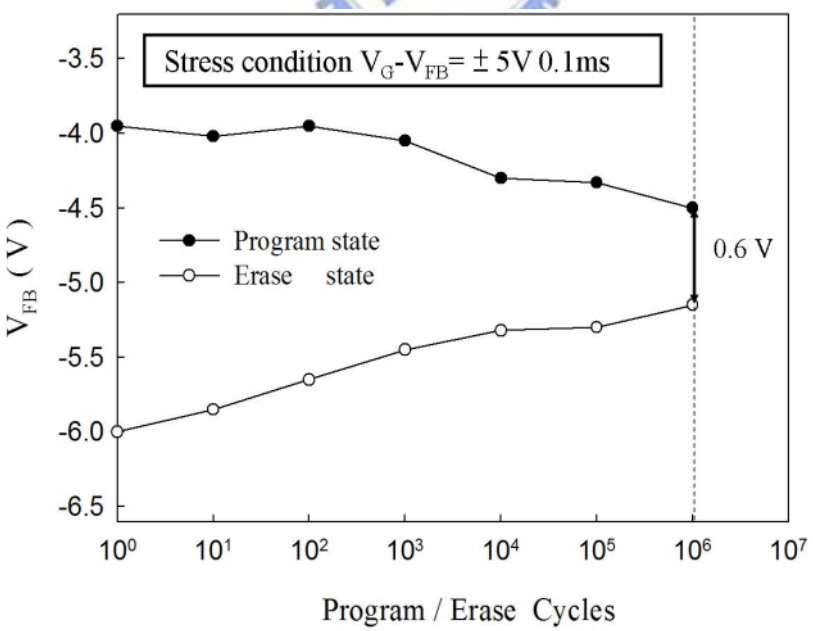


Figure 3-6 Endurance characteristics of the Ni-Si-O nanocrystal memory.

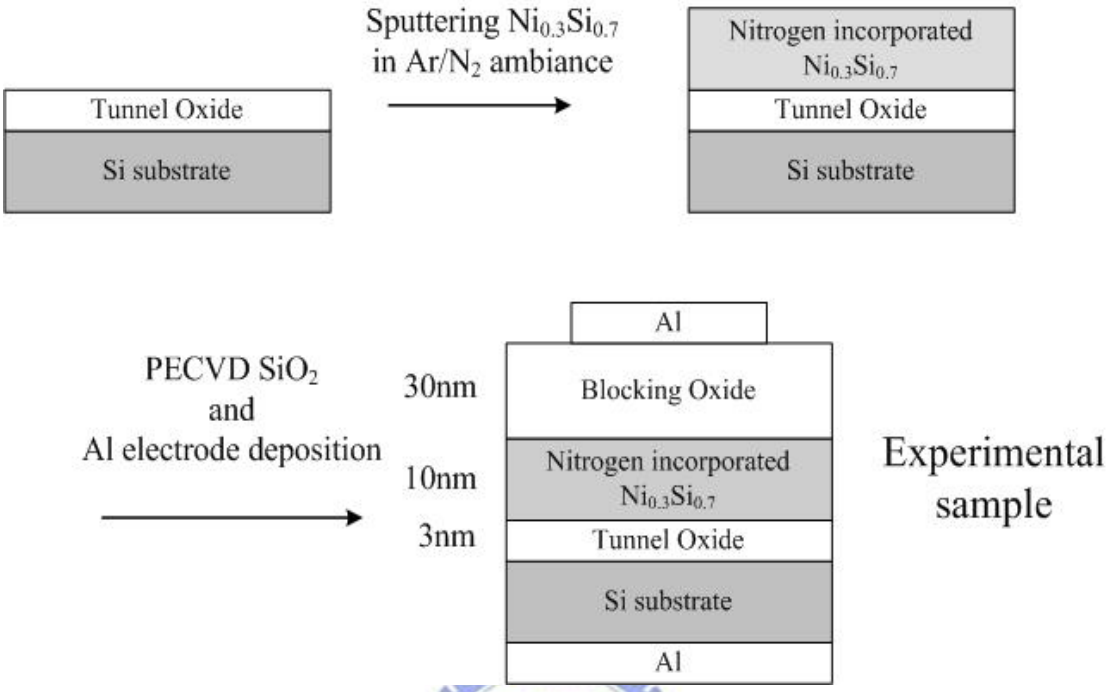


Figure 3-7 Schematics of the experimental procedures. Nitrogen incorporated $Ni_{0.3}Si_{0.7}$ layer was fabricated as charge trapping layer.

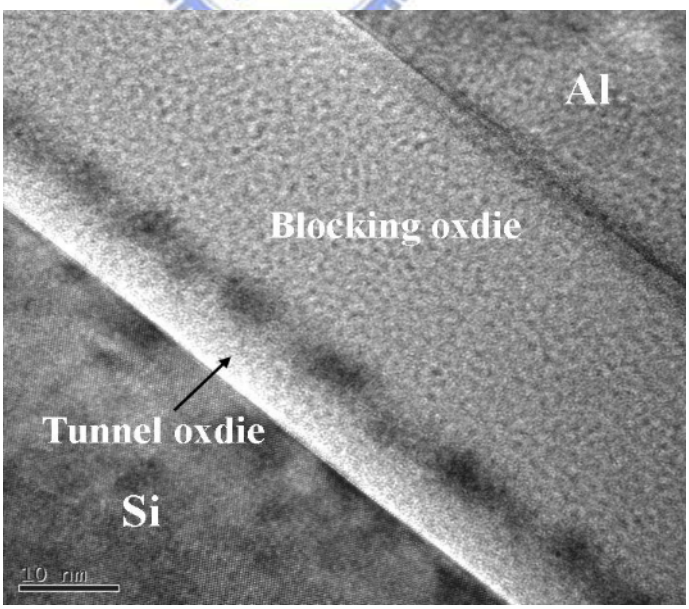


Figure 3-8 Cross-sectional TEM image of the MOIOS structure with nitrogen incorporated $Ni_{0.3}Si_{0.7}$ layer.

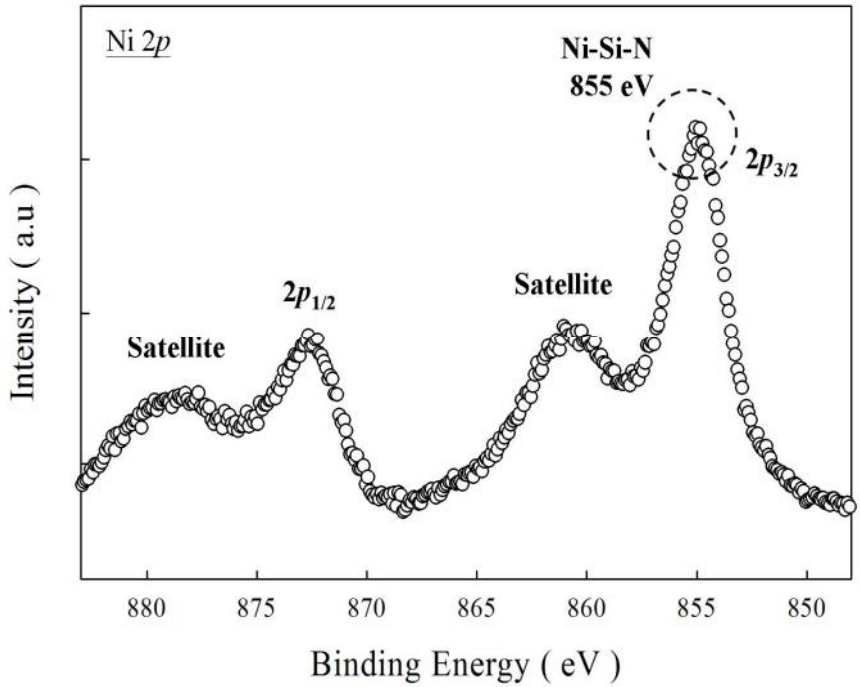


Figure 3-9(a) Ni 2*p* XPS analysis of the nitrogen incorporated $Ni_{0.3}Si_{0.7}$ layer. The Ni $2p_{3/2}$ peak can be asigned to Ni-Si-N ternary bond.

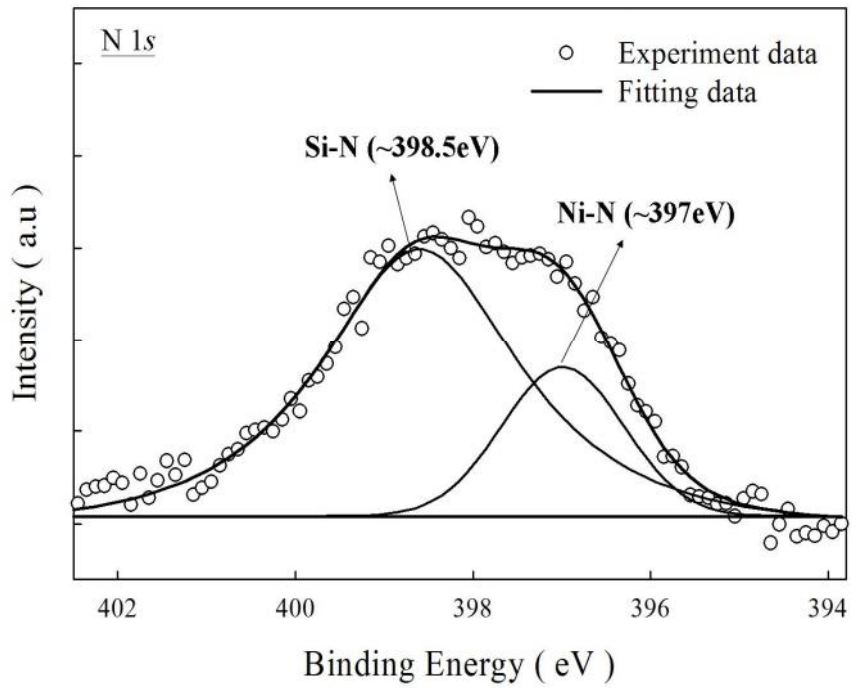


Figure 3-9(b) N 1*s* XPS analysis of the charge trapping layer. Empty circles and straight line indicate experimental and fitting results, respectively.

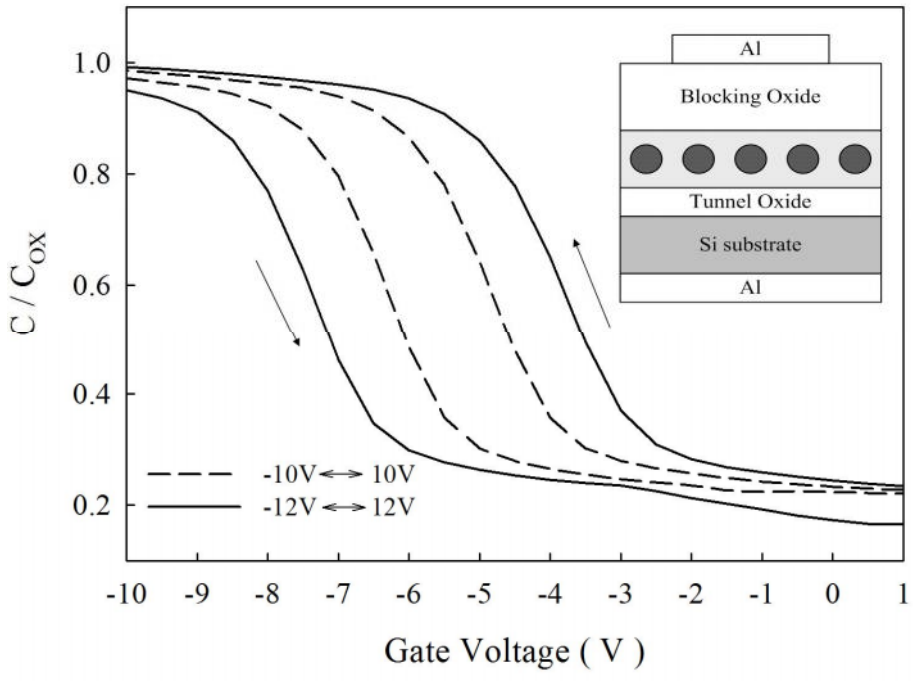


Figure 3-10 Capacitance-voltage (C-V) hysteresis of the fabricated MOIOS structure with Ni-Si-N nanocrystal embedded in SiN_x.

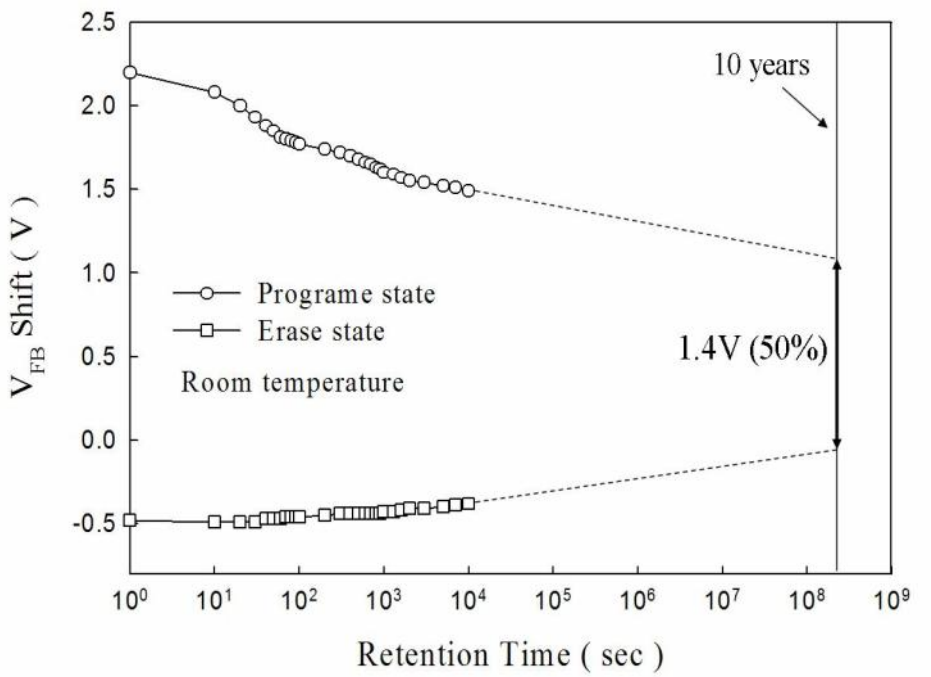


Figure 3-11 Data retention characteristics of the Ni-Si-N nanocrystal memory at room temperature.

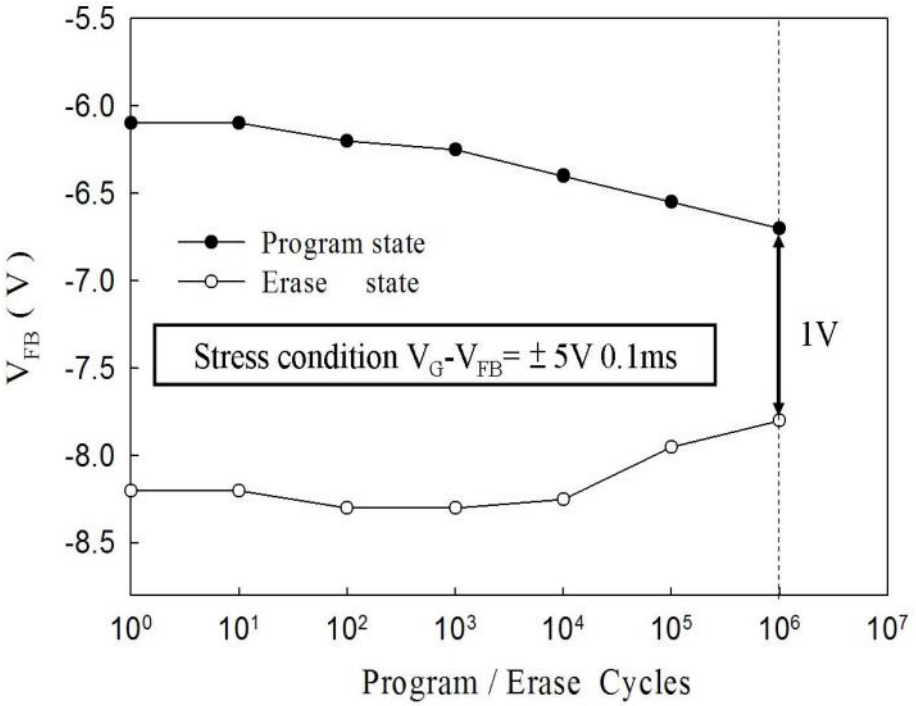


Figure 3-12 Endurance characteristics of the Ni-Si-N nanocrystal memory.

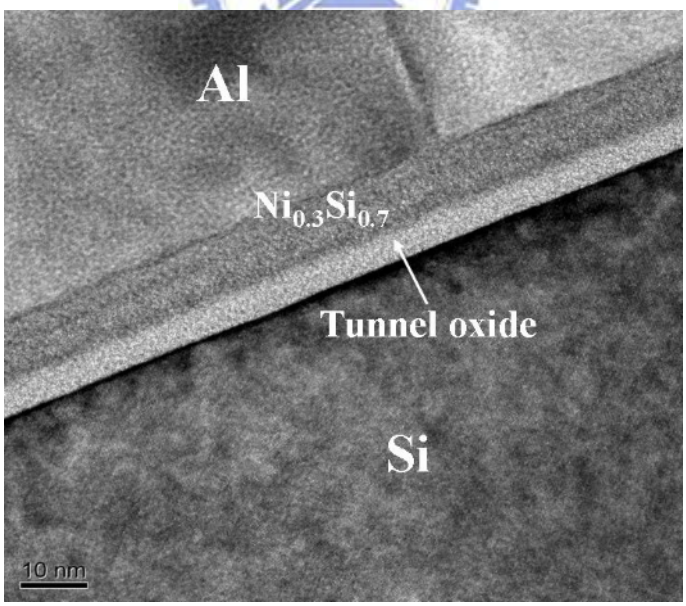


Figure 3-13(a) Cross-sectional TEM image of oxygen and nitrogen deficient $Ni_{0.3}Si_{0.7}$ layer (without capping oxide by PECVD).

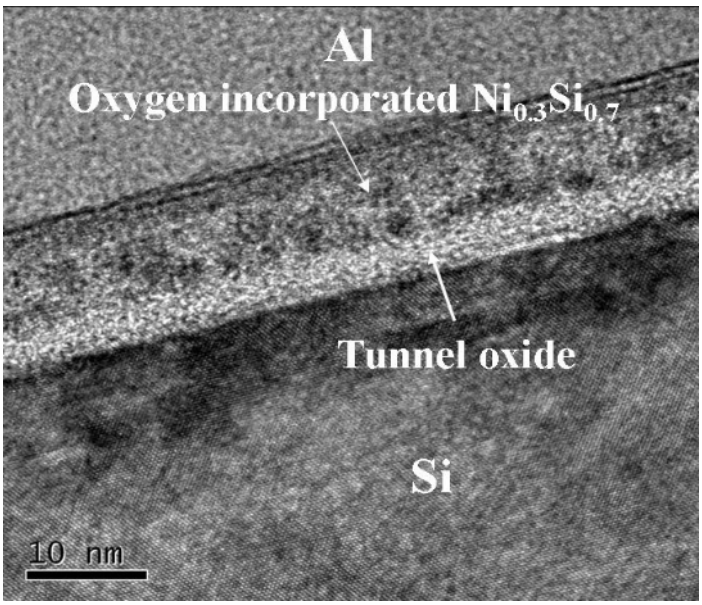


Figure 3-13(b) Cross-sectional TEM image of oxygen incorporated $Ni_{0.3}Si_{0.7}$ layer (without capping oxide by PECVD).

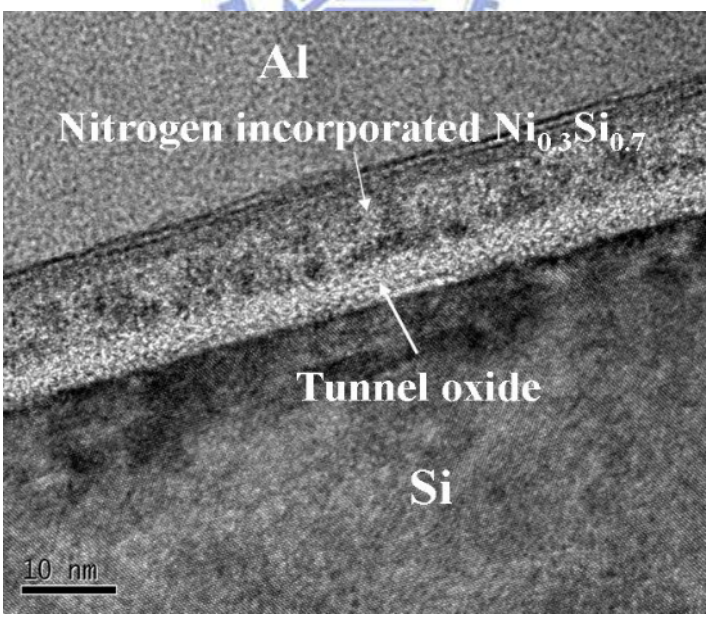


Figure 3-13(c) Cross-sectional TEM images of nitrogen incorporated $Ni_{0.3}Si_{0.7}$ layer (without capping oxide by PECVD).

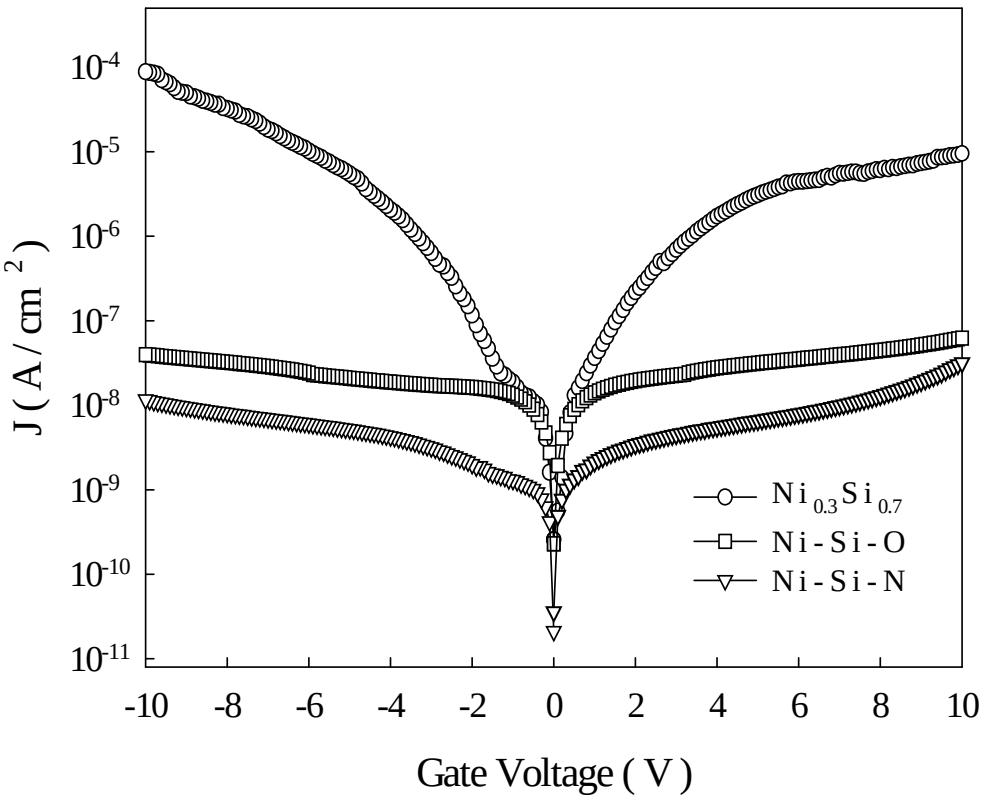


Figure 3-14 The current density-voltage (J-V) characteristics of the MOIOS structure with different charge trapping layer.

Table 3-1 Comparisons of memory window and nanocrystal density between two type nonvolatile memory devices.

Nonvolatile Memory	Memory window under ±10V operation	NC density (cm^{-2})
Ni-Si-O Nanocrystal embedded in SiO_x	0.8V	1.33×10^{12}
Ni-Si-N Nanocrystal embedded in SiN_x	1.5V	1.08×10^{12}

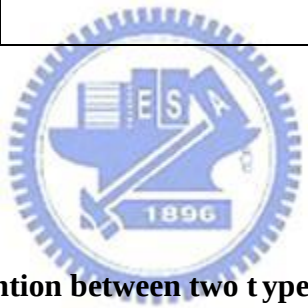


Table 3-2 Comparisons of retention between two type nonvolatile memory devices.

Nonvolatile Memory	Memory window after 10 years	Remained Charge Ratio
Ni-Si-O Nanocrystal embedded in SiO_x	1.2V	40%
Ni-Si-N Nanocrystal embedded in SiN_x	1.4V	50%