Chapter 4

Improved Performance of Nonvolatile Ni-Si-O and Ni-Si-N Nanocrystal Memroy by Thermal Treatment

4.1 Motivation

Some reports indicate that Ni silicidation process was performed by RTA thermal treatment [4.1]. For using RTA process, the crystalline quality of nanocrystal is promoted due to the silicidation of Ni/Si system. Nanocrystals with good crystalline quality can offer higher density of states for storage capacity. In addition, the rapid temperature annealing can improve quality of dielectric surrounding with nanocrystals.. Therefore, the reliability issues would be improved after the RTA process.

4.2 Thermal Treatment for Ni-Si-O Nanocrsytal Memory

4.2.1 Experimental Procedures

Figure 4-1 indicates a schematic of experimental procedures. This nonvolatile memory-cell structure in this letter was fabricated on a 4 in. p-type silicon (100) wafer. After a standard RCA process which removed native oxide and micro-particles, 3-nm-thick tunnel oxide was thermally grown by a dry oxidation process in an atmospheric pressure chemical vapor deposition furnace (APCVD). Subsequently, a 10-nm-thick charge tapping layer was deposited by reactive sputtering of $Ni_{0.3}Si_{0.7}$ co-mix target in the Ar/O_2 (24sccm/2sccm) ambiance at room temperature, and the DC sputtering power was set to 80 W. This step can obtain an oxygen incorporated $Ni_{0.3}Si_{0.7}$ layer as a charge trapping layer in our memory structure. Next, the rapid thermal annealing (RTA) process was performed in nitrogen (N_2) atmosphere. The annealing conditions are 500°C for 100sec and 600°C for 100sec. Then, a 30-nm-thick blocking oxide was deposited by the plasma enhanced chemical vapor deposition (PECVD) system

at 300°C. Al gate electrodes on back and front side of the sample were finally deposited and patterned to form a metal/oxide/insulator/oxide/silicon (MOIOS) structure.

Electrical characteristics, including the capacitance-voltage (C-V), current density-voltage (J-V), retention, and endurance characteristics, were also performed. The J-V and C-V characteristics were measured by Keithley 4200 and HP4284 Precision LCR Meter with high frequency 100 kHz. In addition, Transmission electron microscope (TEM) and X-ray photoelectron spectroscopy (XPS) were adopted for the micro-structure analysis and chemical material analysis.

4.2.2 Results and Discussion

Figure 4-2 shows the forward and reverse sweep C-V characteristics, indicating the electron charging and discharging effects of the charge trapping layer. As seen in Figure 4-2(a), the C-V hysteresis of Ni-Si-O nancrystals (NCs) embedded in SiO_x layer after RTA annealing at 500°C for 100 sec. The sweeping conditions were, operated from -5 V to 5 V and reversely, operated from -10 V to 10 V and reversely. The flat-band voltage shifts are 0.8 V and 3 V, respectively. The C-V hysteresis loops are counterclockwise, which is due to injection of electrons from the deep inversion layer and injection of holes from the deep accumulation layer of Si substrate [4.2]. Figure 4-2 (b) shows C-V hysteresis of Ni-Si-O NCs embedded in SiO_x layer after RTA annealing at 600°C for 100 sec. By changing the sweep range from (−5 V, 5 V) to (−10 V, 10 V), 0.5 V and 1.8 V memory windows are obtained, respectively. The C-V hysteresis loops are also counterclockwise due to substrate injection. Both the results of C-V shifts from Figure 4-2 indicate that the charging effects of Ni-Si-O NCs after RTA annealing are more significant.

Figure 4-3(a) shows typical cross-sectional TEM image of Ni-Si-O NCs embedded in SiO_x layer after RTA at 500°C for 100 sec. The mean size and aerial density of the nanocrystals were estimated to be about 4-5 nm and 2.77×10^{12} cm^{-2}, respectively. Figure 4-3(b) exhibits cross-sectional TEM image of Ni-Si-O NCs embedded in SiO_x layer after RTA annealing at 600°C for 100 sec. The nanocrystals have an average size of 4–5 nm with a high density of 2.87×10^{12} cm^{-2}. We found that the nanocrystals become smaller and the higher aerial density is obtained after RTA annealing.

The current density-voltage (J-V) characteristics under positive and negative biases for the samples before and after thermal treatment are shown in Fig.4-4. It is clear that the leakage current of samples after RTA annealing is significantly reduced as compared to that of the sample before thermal treatment. It is evident that the quality of charge trapping layer is improved by thermal treatment. The RTA treatment will reduce the defects in the SiO_x matrix and NC/SiO_x interface. In addition, we also performed the XPS analysis of Si 2*p* spectra to demonstrate the improvement for the quality of SiO_x, as shown in Fig.4-5. The peak signal of Si–O bonding is observed according to their binding energy [4.3]. After the RTA at 500 ^oC and 600 ^oC, the peak signal of Si–O bonding increased and shifted toward higher binding energy. This agrees with the above result of J-V characteristic.

The charge retention characteristics of Ni-Si-O nanocrystals embedded in SiO_x after thermal treatment are demonstrated in Fig.4-6. This measurement is carried out at room temperature using ±10 V gate voltage stress for 5 sec. The shift in the flat-band voltage as a function of time is obtained by comparing the C-V curves. Fig.4-6(a) exhibits retention characteristic of charge storage layer after RTA at 500 °C for 100 sec. A memory window of 1.3 V is expected to maintain after 10 years, which is approximately 45% of the stored charges retained in the nanocrystals. In the meantime, the retention characteristic after RTA at higher 600 °C for 100 sec is also shown in Fig.4-6(b). The long-term extrapolated gives a memory window of 1V (charge retained ratio 50%) after 10 years. The endurance characteristics of MOIOS structure after RTA at 500 °C and 600 °C are shown in Fig.4-7(a) and (b), respectively. Pulses ($V_G - V_{FB} = \pm$ 5 V, 0.1 ms) were applied to evaluate endurance characteristics for the P/E operations. We found that it appears a slight closure of window during P/E operation in both thermal conditions. However, the memory window of 1.2 and 1.5 V can be kept after 10^6 cycles, respectively.

A comparison of memory characteristics for different trapping layers before and after RTA annealing in N_2 is presented in Table 4-1. By taking account of the memory window, it indicates the improvement for storage capacity after thermal treatment. The previous study has been carried out to investigate the silicidation of Ni/Si system during RTA annealing at 500 and 600 ºC and annealing time of 60 seconds [4.1]. We consider similar silicidation reaction for the Ni-Si-O nanocrystals during the RTA process. During

the RTA process, the metallic Ni-Silicide (NiSi) nanocrystals precipitate and show good crystalline quality. The metallic NiSi nanocrystal with good crystalline quality has higher density of states to store charge and cause larger memory window. In addition, during the silicide processing, the oxygen were pushed down towards the NiSi/SiO_x interface since the solubility of oxygen in NiSi is much lower than that in Si resulting in the formation of an oxygen rich Si layer at the NiSi/SiO_x interface. This model called Silicidation Induced Impurity Segregation (SIIS) is widely used in explaining the mechanisms of dopants segregation during silicide processing [4.4]. As seen in Table 4-1, the reliability issues such as retention and endurance, are significantly improved after the RTA process. According the results of J-V characteristic and XPS analysis, it is believed that thermal treatment (RTA) can reduce the defects (leakage path) in the SiO_x matrix which surrounds the nanocrystal. It decreases the probability of charge escaping from the nanocrystal. The quality of SiO_x is also strengthened to bear the P/E cycling stress.

4.3 Thermal Treatment for Ni-Si-N Nanocrsytal Memory

4.3.1 Experimental Procedures

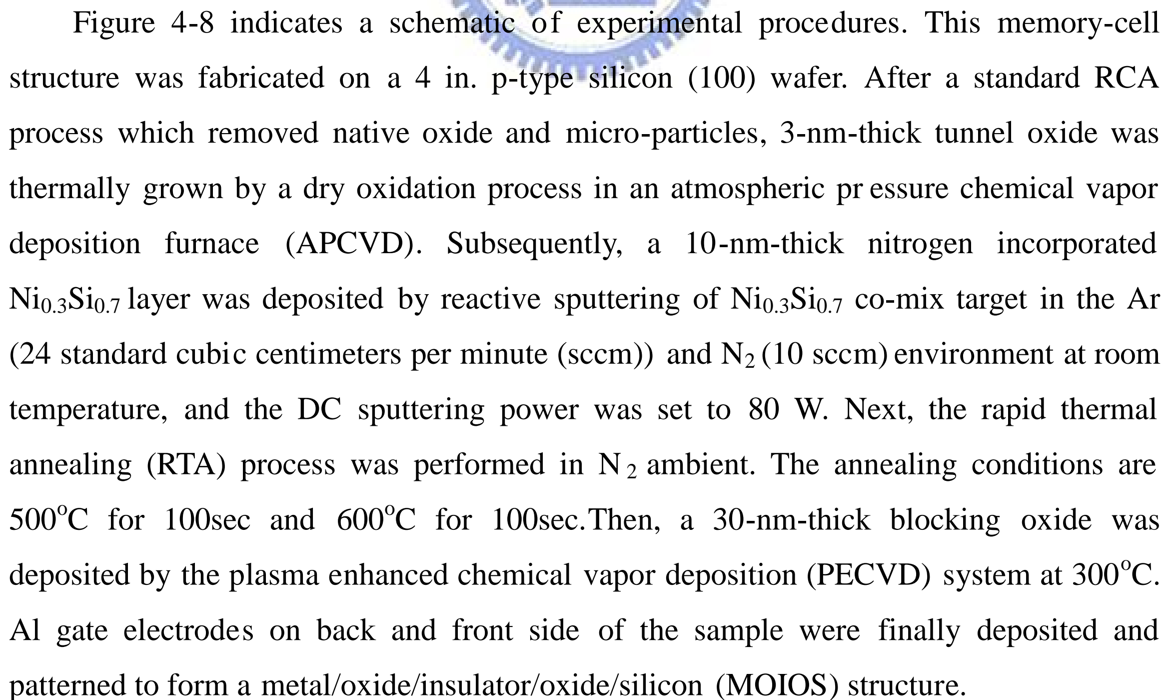


Figure 4-8 indicates a schematic of experimental procedures. This memory-cell structure was fabricated on a 4 in. p-type silicon (100) wafer. After a standard RCA process which removed native oxide and micro-particles, 3-nm-thick tunnel oxide was thermally grown by a dry oxidation process in an atmospheric pressure chemical vapor deposition furnace (APCVD). Subsequently, a 10-nm-thick nitrogen incorporated $Ni_{0.3}Si_{0.7}$ layer was deposited by reactive sputtering of $Ni_{0.3}Si_{0.7}$ co-mix target in the Ar (24 standard cubic centimeters per minute (sccm)) and N_2 (10 sccm) environment at room temperature, and the DC sputtering power was set to 80 W. Next, the rapid thermal annealing (RTA) process was performed in N_2 ambient. The annealing conditions are 500°C for 100sec and 600°C for 100sec.Then, a 30-nm-thick blocking oxide was deposited by the plasma enhanced chemical vapor deposition (PECVD) system at 300°C. Al gate electrodes on back and front side of the sample were finally deposited and patterned to form a metal/oxide/insulator/oxide/silicon (MOIOS) structure.

Electrical characteristics, including the capacitance-voltage (C-V), current

density-voltage (J-V), retention, and endurance characteristics, were also performed. The J-V and C-V characteristics were measured by Keithley 4200 and HP4284 Precision LCR Meter with high frequency 100 kHz. In addition, High resolution transmission electron microscope (HRTEM) and X-ray photoelectron spectroscopy (XPS) were adopted for the micro-structure analysis and chemical material analysis.

4.3.2 Results and Discussion

Figure 4-9 shows the forward and reverse sweep C-V characteristics, indicating the electron charging and discharging effects of the charge trapping layer. As seen in Figure 4-9(a), the C-V hysteresis of Ni-Si-N nancrystals (NCs) embedded in SiN_x layer after RTA annealing at 500^oC for 100 sec. The sweeping conditions were, operated from -5 V to 5 V and reversely, operated from -10 V to 10 V and reversely. The flatband voltage shifts are 0.8 V and 3 V, respectively. The C-V hysteresis loops are counterclockwise, which is due to injection of electrons from the deep inversion layer and injection of holes from the deep accumulation layer of Si substrate. Figure 4-9 (b) shows C-V hysteresis of Ni-Si-N NCs embedded in SiN_x layer after RTA annealing at 600^oC for 100 sec. By changing the sweep range from (−5 V, 5 V) to (−10 V, 10 V), 0.5 V and 1.8 V memory windows are obtained, respectively. The C-V hysteresis loops are also counterclockwise due to substrate injection. Both the results of C-V shifts from Figure 4-9 indicate that the charging effects of Ni-Si-N NCs after RTA annealing are more significant.

Figure 4-10(a) shows typical cross-sectional TEM image of Ni-Si-N NCs embedded in SiN_x layer after RTA at 500^oC for 100 sec. The mean size and aerial density of the nanocrystals were estimated to be about 4-5 nm and 2.49×10^{12} cm^{-2}, respectively. Figure 4-10(b) exhibits cross-sectional TEM image of Ni-Si-N NCs embedded in SiN_x layer after RTA annealing at 600^oC for 100 sec. The nanocrystals have an average size of 4–5 nm with a high density of 2.78×10^{12} cm^{-2}. We found that the nanocrystals become smaller and the higher aerial density is obtained after RTA annealing.

The current density-voltage (J-V) characteristics under positive and negative biases for the samples before and after thermal treatment are shown in Fig.4-11. It is clear that the leakage current of samples after RTA annealing is significantly reduced as compared to that of the sample before thermal treatment. It is evident that the quality of charge

trapping layer is improved by thermal treatment. The RTA treatment will reduce the defects in the SiN_x matrix and NC/SiN_x interface. In addition, we also performed the XPS analysis of N 1*s* spectra to demonstrate the improvement for the quality of SiN_x, as shown in Fig.4-12. The peak signal of Si–N and Ni-N bonding are observed according to their binding energy [4.5,4.6]. After the RTA at 500 °C and 600 °C, the peak signal of Si–N bonding shifted toward higher binding energy. This agrees with the above result of J-V characteristic. In addition, the peak signal of Ni-N decreases after RTA treatment. The Ni-N bonding almost disappears after RTA at 600 °C.

The charge retention characteristics of Ni-Si-N nanocrystals embedded in SiN_x after thermal treatment are demonstrated in Fig.4-13. This measurement is carried out at room temperature using ±10 V gate voltage stress for 5 sec. The shift in the flat-band voltage as a function of time is obtained by comparing the C-V curves. Fig.4-13(a) exhibits retention characteristic of charge storage layer after RTA at 500 °C for 100 sec. A memory window of 2.1 V is expected to maintain after 10 years, which is approximately 52% of the stored charges retained in the nanocrystals. In the meantime, the retention characteristic after RTA at higher 600 °C for 100 sec is also shown in Fig.4-13(b). The long-term extrapolated gives a memory window of 1.8V (charge retained ratio 56%) after 10 years. The retention characteristic was also performed at 85°C, which increases the charge loss rate. However, an expected memory window of 0.6V after 10 years is still enough to define two memory states.

The endurance characteristics of MOIOS structure after RTA at 500 °C and 600 °C are shown in Fig.4-14(a) and (b), respectively. Pulses ($V_G - V_{FB} = \pm 5$ V, 0.1 ms) were applied to evaluate endurance characteristics for the P/E operations. We found that the program/erase flat-band voltage shows almost no shifts up to 10^6. Both of thermal conditions retain a clear difference of 2.1V between program and erase state.

A comparison of memory characteristics for different trapping layers before and after RTA annealing in N_2 is presented in Table 4-2. By taking account of the memory window, it indicates the improvement for storage capacity after thermal treatment. The previous study has been carried out to investigate the silicidation of Ni/Si system during RTA annealing at 500 and 600 ºC and annealing time of 60 seconds [4.1]. We consider similar silicidation reaction for the Ni-Si-N nanocrystals during the RTA process. During

the RTA process, the metallic Ni-Silicide (NiSi) nanocrystals precipitate and show good crystalline quality. The metallic NiSi nanocrystal with good crystalline quality has higher density of states to store charge and cause larger memory window. In addition, as seen in Fig.4-12, the peak signal of Ni-N decreases after RTA treatment. We consider that nitrogen was pushed towards NiSi/SiN_x interface during the silicide processing. As mentioned above, this similar situation could be explained by Silicidation Induced Impurity Segregation (SIIS) [4.4]. As seen in Table 4-2, the reliability issues such as retention and endurance, are significantly improved after the RTA process. According the results of J-V characteristic and XPS analysis, it is believed that thermal treatment (RTA) can reduce the defects (leakage path) in the SiN_x matrix which surrounds the nanocrystal. It decreases the probability of charge escaping from the nanocrystal. The quality of SiN_x is also strengthened to bear the P/E cycling stress.

Finally, the endurance properties of NiSi NCs embedded in SiO_x and SiN_x after RTA process at 600 ℃ are discussed. As shown in Table 4-3, the memory structure of nanocrystal embedded in SiN_x exhibits better endurance characteristic than that of nanocrystal embedded in SiO_x. The electrostatic simulations were performed for electric field distribution from Si substrate, as shown in Fig.4-15. The vertical electric fields set by the MOIOS structure with/without the nanocrystals were simulated, where tunnel oxide thickness *Tox* is set 3 nm, metal NC diameter *D* is set 5 nm, blocking oxide thickness *Cox* is set 30 nm, distance between NCs and tunnel oxide or blocking oxide is set 2 nm, and the dielectric constants of SiO_x and SiN_x were given to 3.9 and 7.5, respectively. Fig.4-15(a) shows the simulated electric field distribution of metal NC embedded in SiO_x. Obviously, the electric field between NC and Si substrate enhanced by the metal NCs is much larger than that without NCs. This indicates the electric field is enhanced strongly near metal NC. On the contrary, Fig.4-15(b) shows the simulated electric field distribution of metal NC embedded in SiN_x. The electric field between NC and Si substrate enhanced by the MOIOS structure with metal NCs is larger than that of MOIOS structure without NCs. However, the difference of electric field between NC and Si substrate is less than that of NCs embedded in SiO_x. In the other words, the distribution of electric field is more uniform since high permittivity (ε) of nitride. Considering the distribution of electric field, the charge transition under P/E operation is

illustrated in Fig.4-16. In the MOIOS structure containing NiSi nanocrystals embedded in SiO_x, the dominant charge transition is tunneling through the dielectric underneath NCs due to stronger electric field. Hence the tunnel oxide and SiO_x matrix underneath NCs will be degraded seriously. Oppositely, the charge transition is more uniform due to the electric field distribution in the MOIOS structure containing NiSi nanocrystals embedded in SiN_x. The results will alleviate the degradation for tunnel oxide and SiN_x layer. Therefore, combining NCs and SiN_x can improve the endurance characteristic for P/E cycling operation.

4.3 Summary II

Table 4-4 is the comparison results of memory characteristic for NCs memorys in our work. By taking account of the memory window, it indicates the improvement for storage capacity after thermal treatment. We consider silicidation reaction for the Ni-Si-O and Ni-Si-N nanocrystals. During the RTA process, the metallic Ni-Silicide (NiSi) nanocrystals precipitate and show good crystalline quality. The NiSi nanocrystal with good crystalline quality has higher density of states to store charge and cause larger memory window. The reliability issues such as retention and endurance, are significantly improved after the RTA process. According the results of J-V characteristic and XPS analysis, it is believed that thermal treatment (RTA) can reduce the defects (leakage path) in the dielectric (SiO_x or SiN_x) which surrounds the nanocrystal. It decreases the probability of charge escaping from the nanocrystal. The quality of dielectric is also strengthened to bear the P/E cycling stress.

A comparison of memory characteristics for nanocrystals embedded in SiOx and SiN_x is also discussed in Table 4-4. The charge storage layer of nanorystal embedded in SiN_x shows larger memory window. This result is attributed to additional accessible charge trap states in SiN_x matrix. For retention property, the stored charge can be shared among the nitride trap, the enhanced field by stored charge (Coulomb blockade) through the tunneling oxide can be reduced. This result decreases the probability of charge escaping from the nanocrystal. Moreover, charges are likely to be relaxed to the nitride traps. Leakage through the intermediate medium can also be inefficient due to Coulomb blockade. Therefore, nanocrystals embedded in SiN_x show enhanced retention

characteristics. In addition, because of high permittivity (ε) of nitride, the charge transition is more uniform due to the electric field distribution. Combining NCs and SiN_x as charge trapping layer can improve the endurance characteristic for P/E cycling operation.

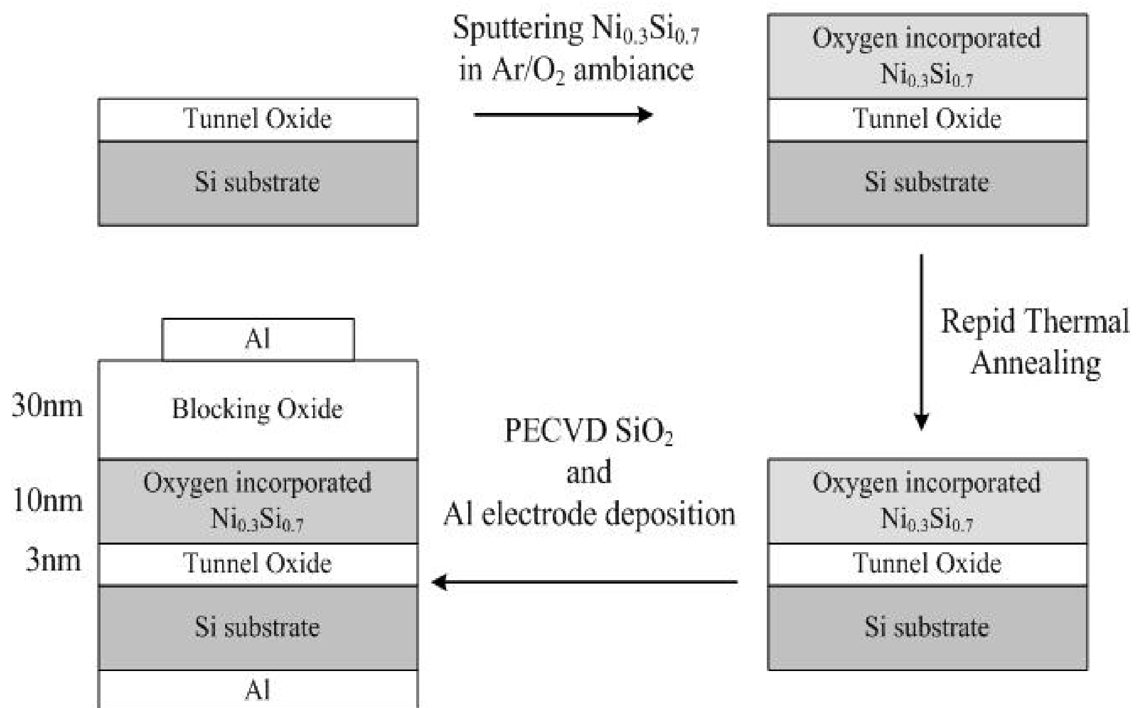
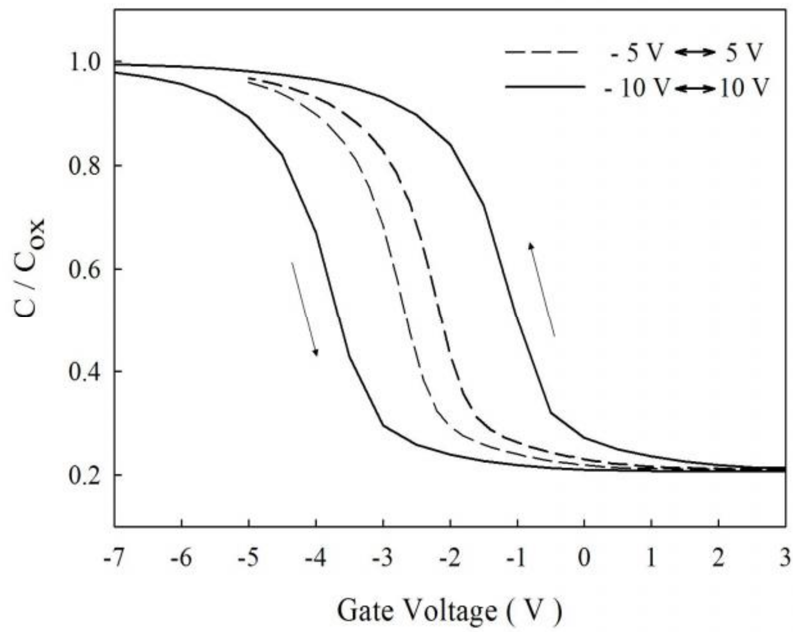
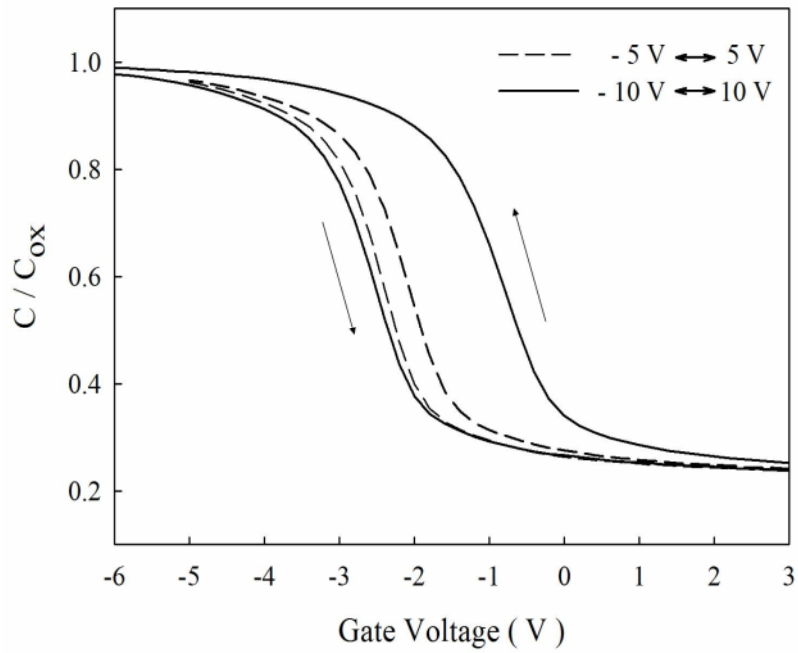


Figure 4-1 Schematics of the experimental procedures. Addtional rapid thermal annealing is applied before PECVD deposition

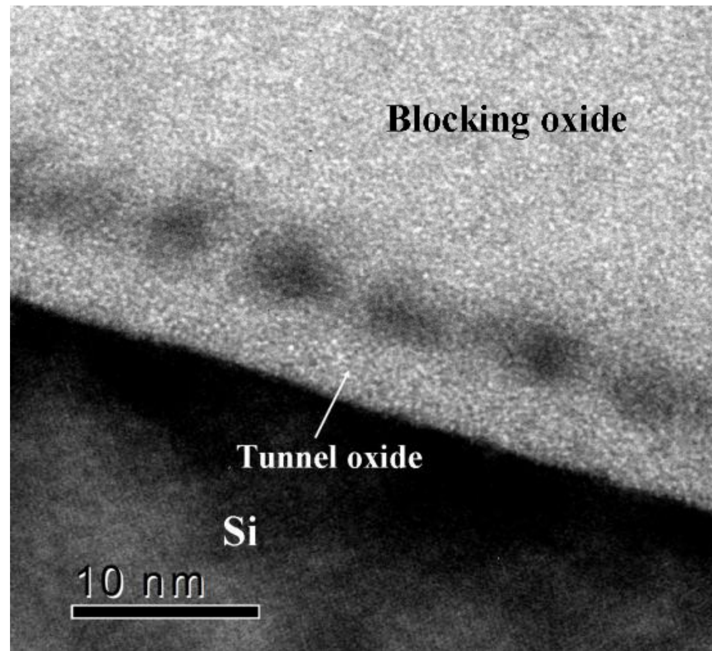


(a)

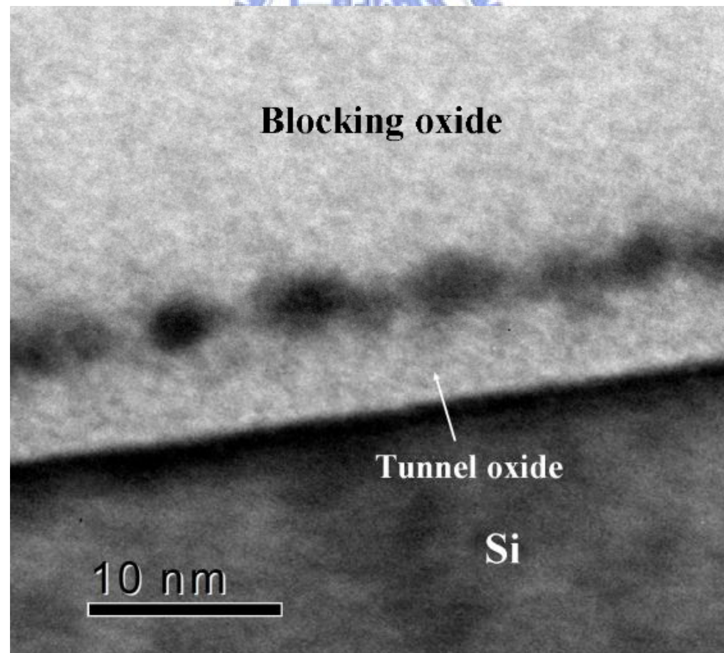


(b)

Figure 4-2 Capacitance-voltage (C-V) hysteresis of Ni-Si-O nanocrystal embedded in SiO_x after RTA at (a) 500 ^oC for 100 sec and (b) 600 ^oC for 100 sec.



(a)



(b)

Figure 4-3 Cross-sectional TEM images of the Ni-Si-O nanocrystals embedded in SiO_x after RTA at (a) 500 ^oC for 100 sec and (b) 600 ^oC for 100 sec.

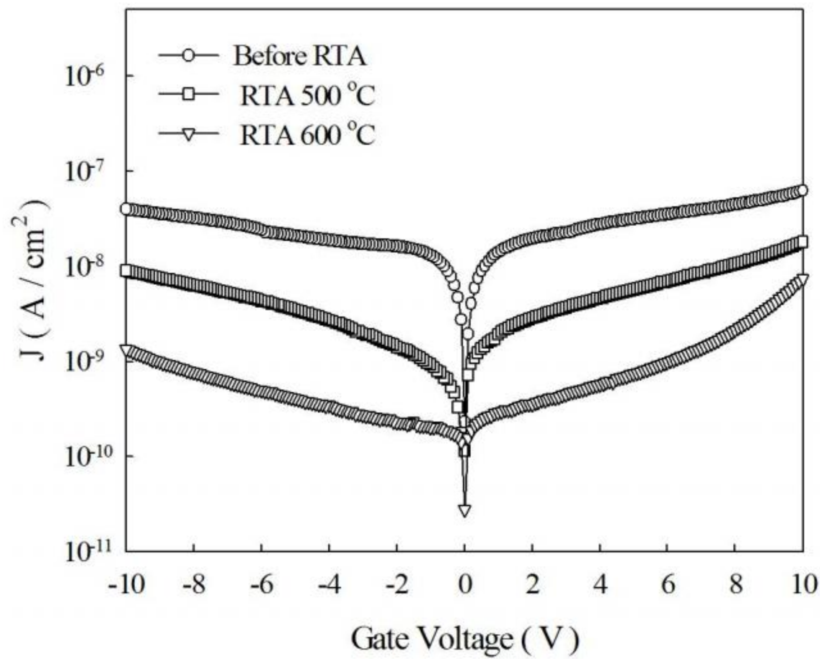


Figure 4-4 The current density-voltage (J-V) characteristics of MOIOS structure with Ni-Si-O nanocrystals embedded in SiO_x before and after RTA treatment.

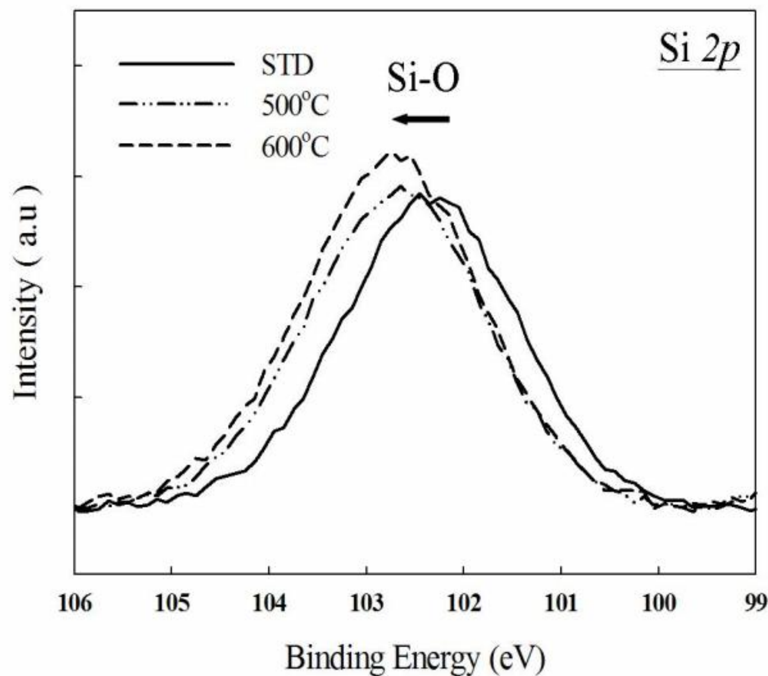
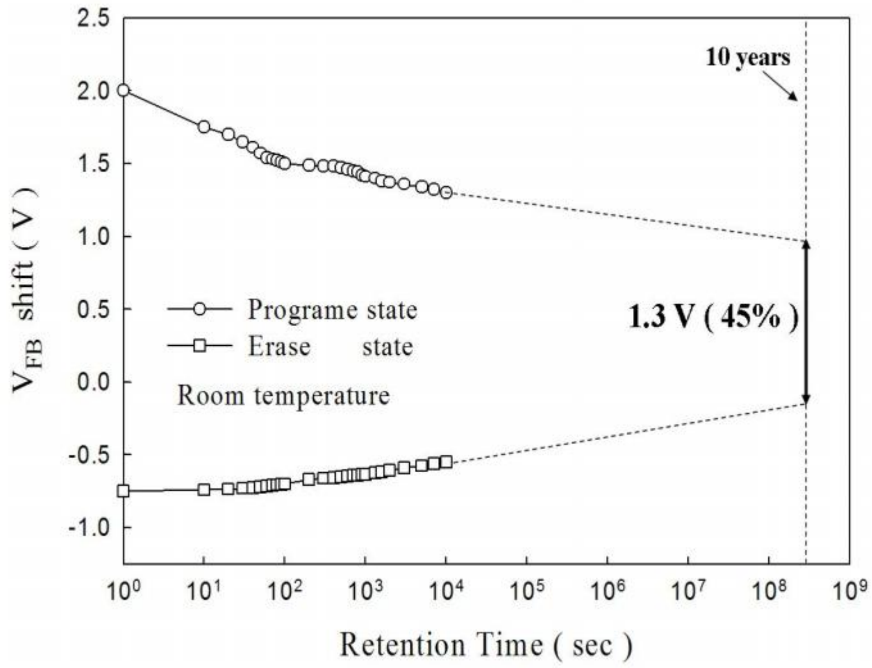
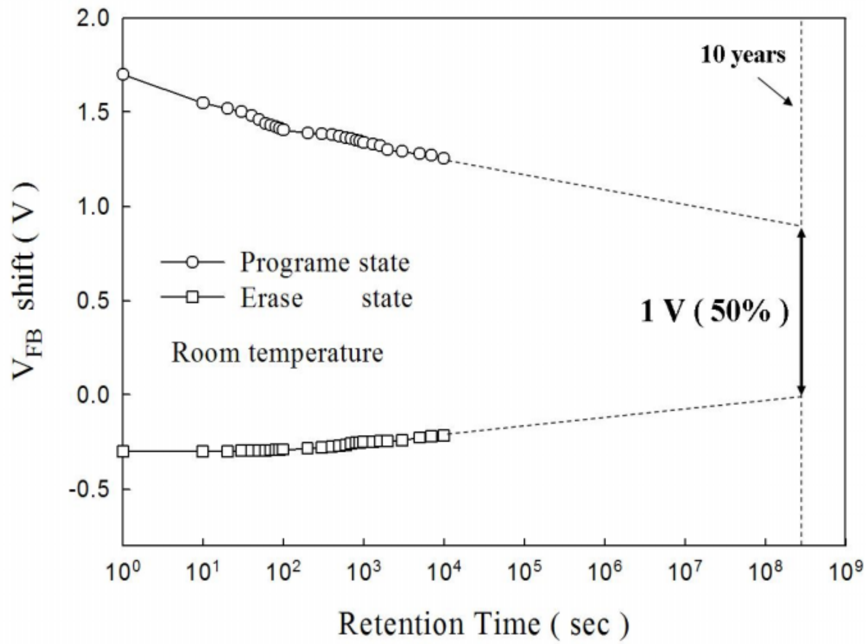


Figure 4-5 XPS analysis of Si 2p spectra for the Ni-Si-O nanocrystals embedded in SiO_x before and after RTA. The peak signal of Si–O bonding increased and shifted toward higher binding energy after the RTA treatment.

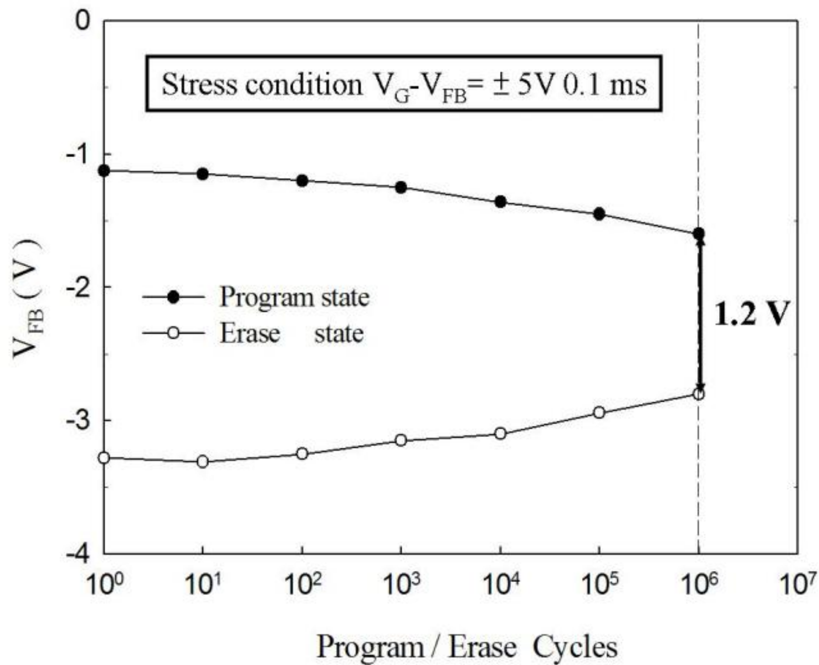


(a)

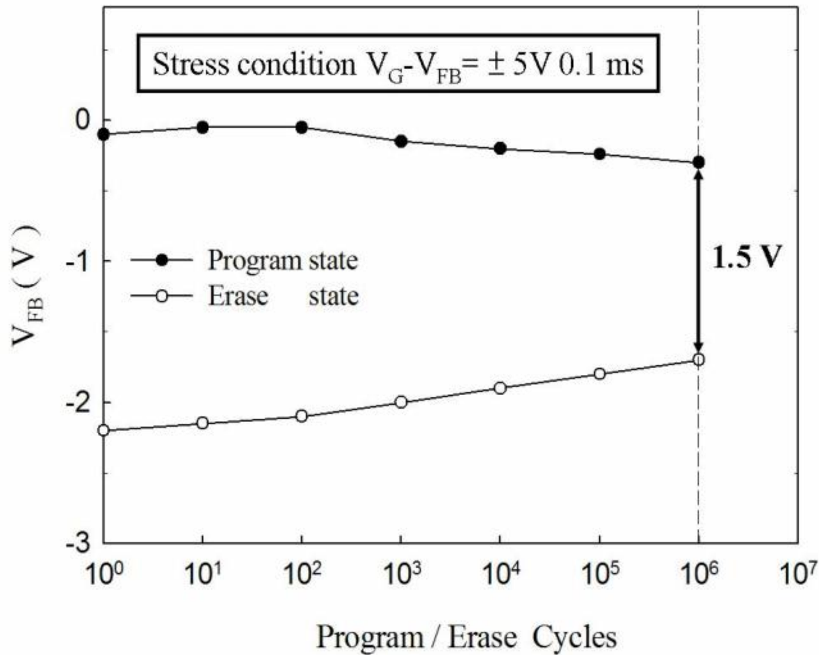


(b)

Figure 4-6 Charge retention characteristics of the Ni-Si-O nanocrystal memory after RTA at (a) 500 °C for 100 sec and (b) 600 °C for 100 sec.



(a)



(b)

Figure 4-7 Endurance characteristics of the Ni-Si-O nanocrystal memory after RTA at (a) 500 °C for 100 sec and (b) 600 °C for 100 sec.

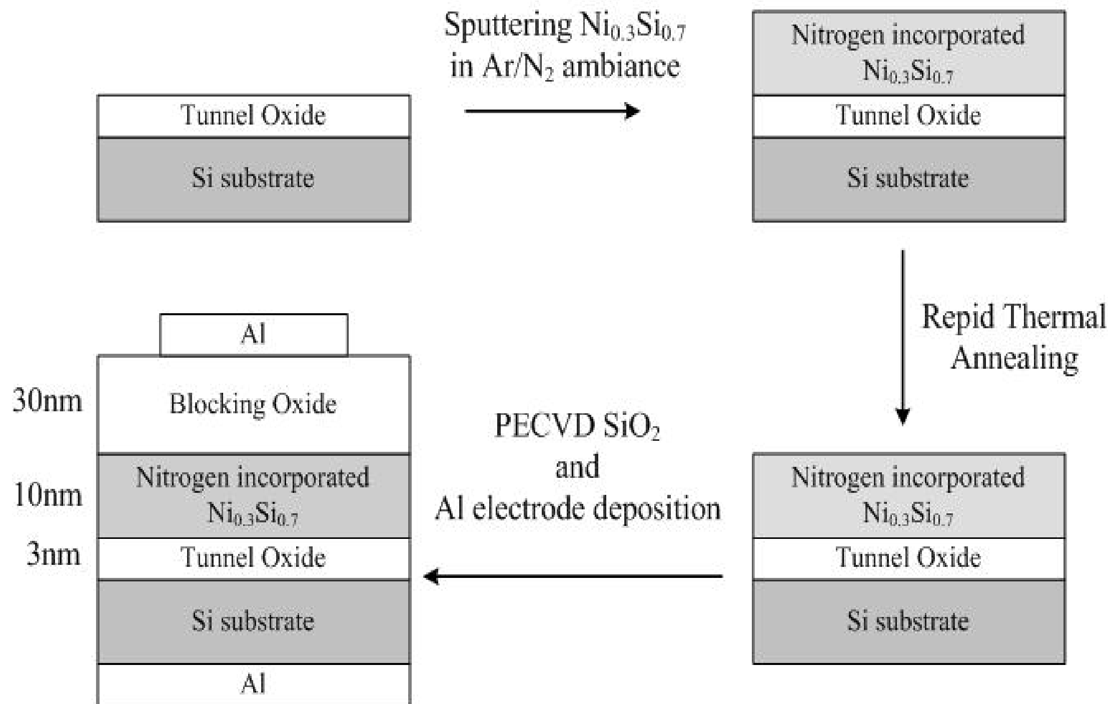
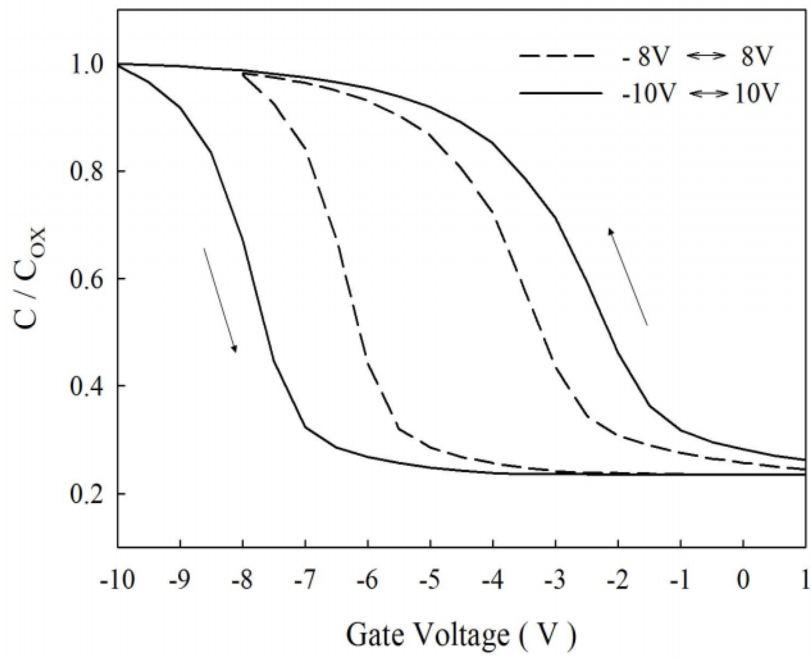
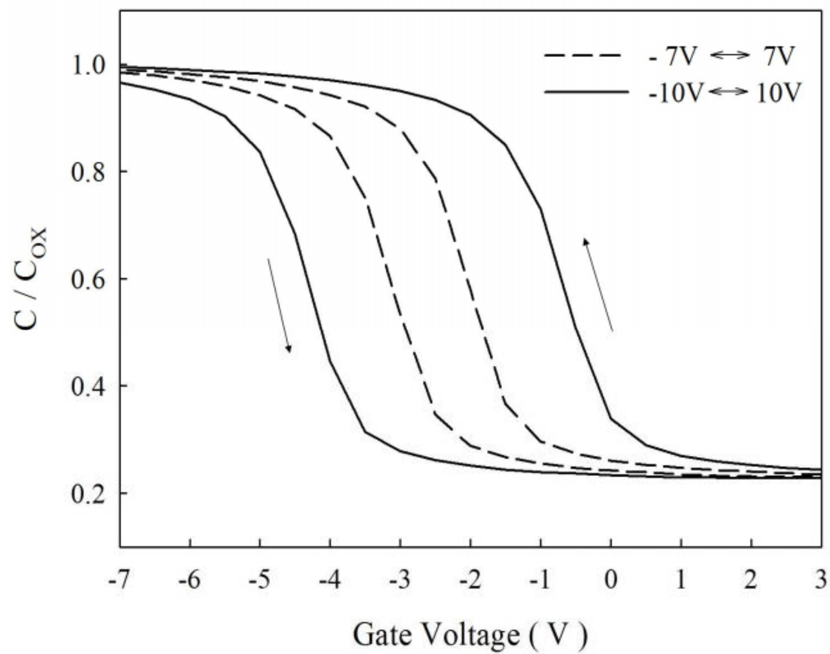


Figure 4-8 Schematics of the experimental procedures. Addtional rapid thermal annealing is applied before PECVD deposition

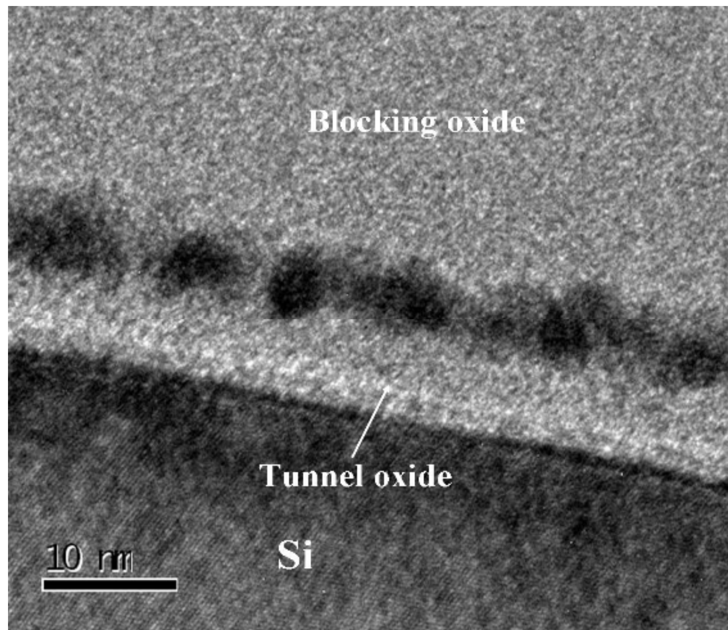


(a)

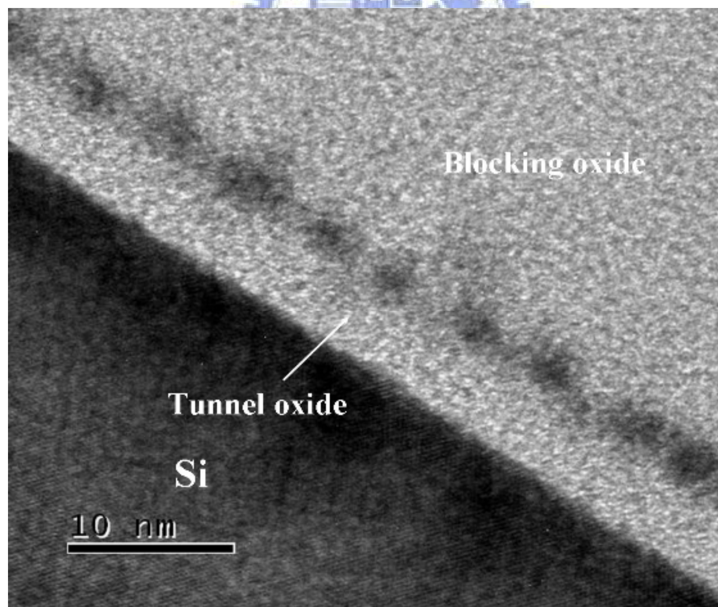


(b)

Figure 4-9 Capacitance-voltage (C-V) hysteresis of Ni-Si-N nanocrystal embedded in SiN_x after RTA at (a) 500 ^oC for 100 sec and (b) 600 ^oC for 100 sec.



(a)



(b)

Figure 4-10 Cross-sectional TEM images of the Ni-Si-N nanocrystals embedded in SiN_x after RTA at (a) 500 ^oC for 100 sec and (b) 600 ^oC for 100 sec.

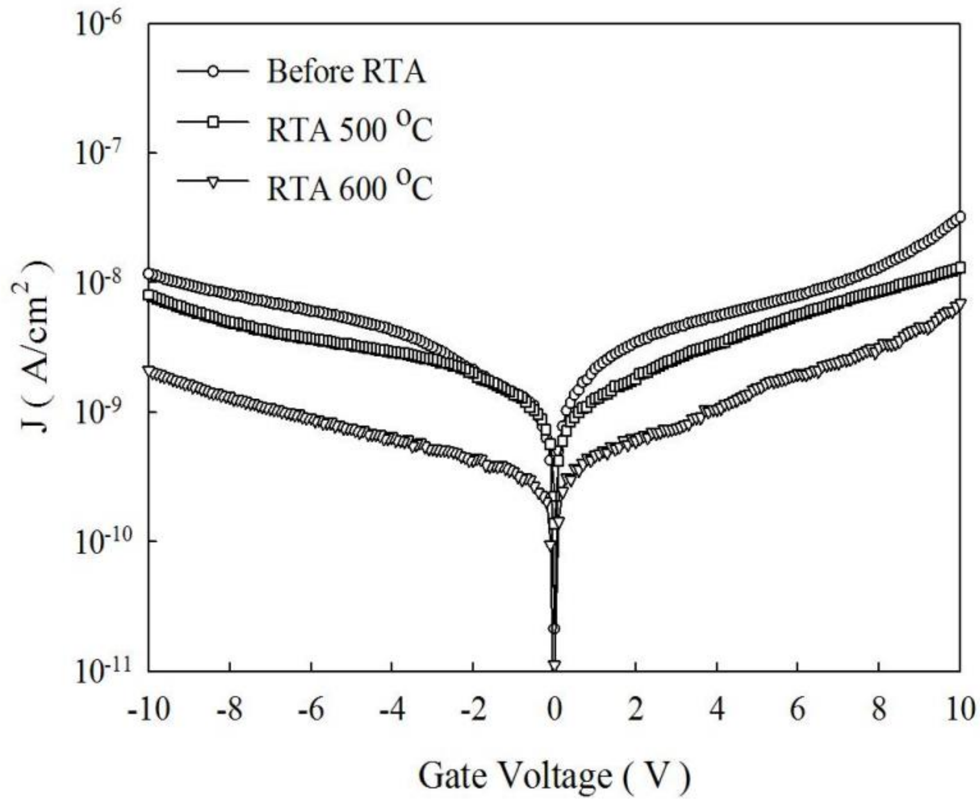


Figure 4-11 The current density-voltage (J-V) characteristics of MOIOS structure with Ni-Si-N nanocrystals embedded in SiN_x before and after RTA treatment.

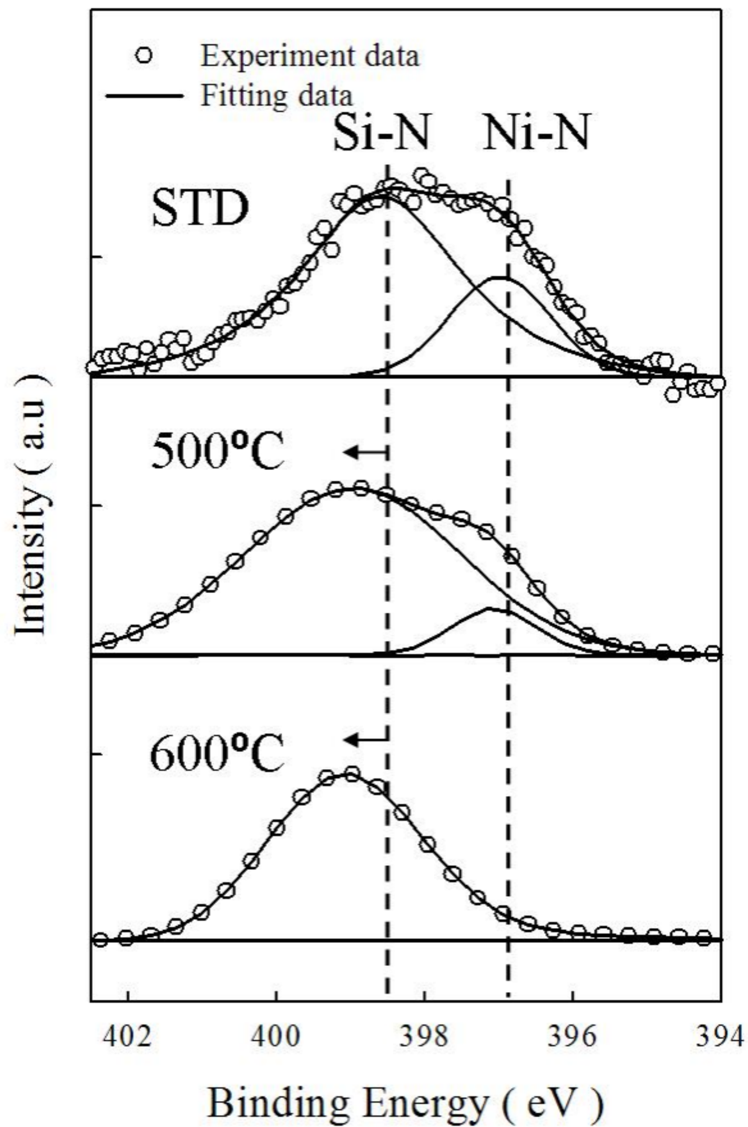
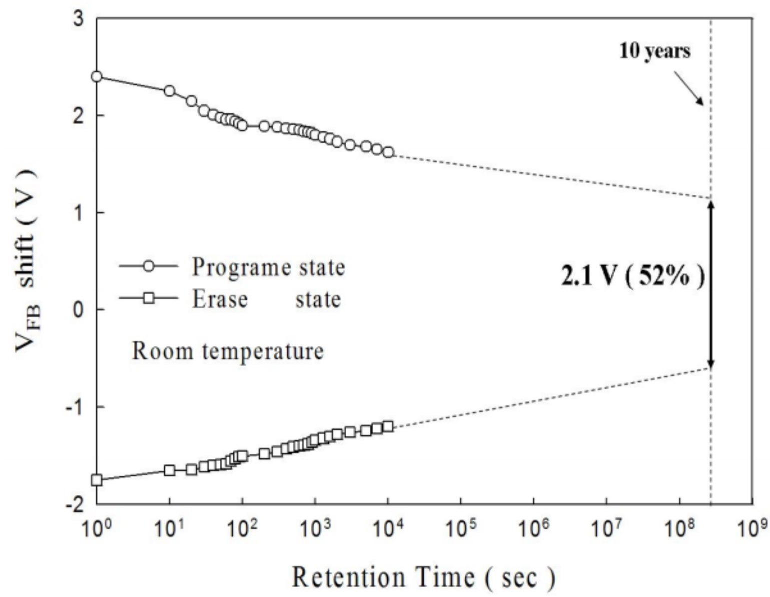
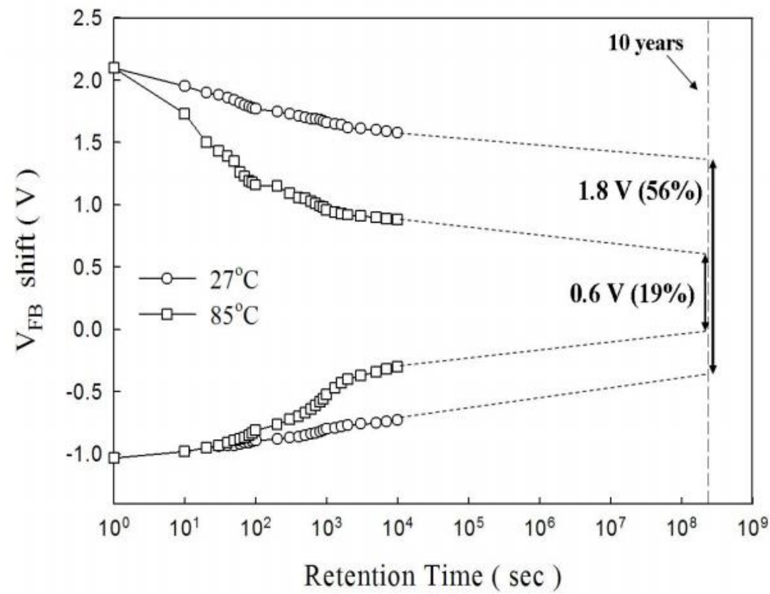


Figure 4-12 The XPS analysis of N 1*s* spectra for Ni-Si-N nanocrystals embedded in SiN_x before and after RTA. After the RTA process, the peak signal of Si–N bonding shifted toward higher binding energy. In addition, the peak signal of Ni-N decreases.

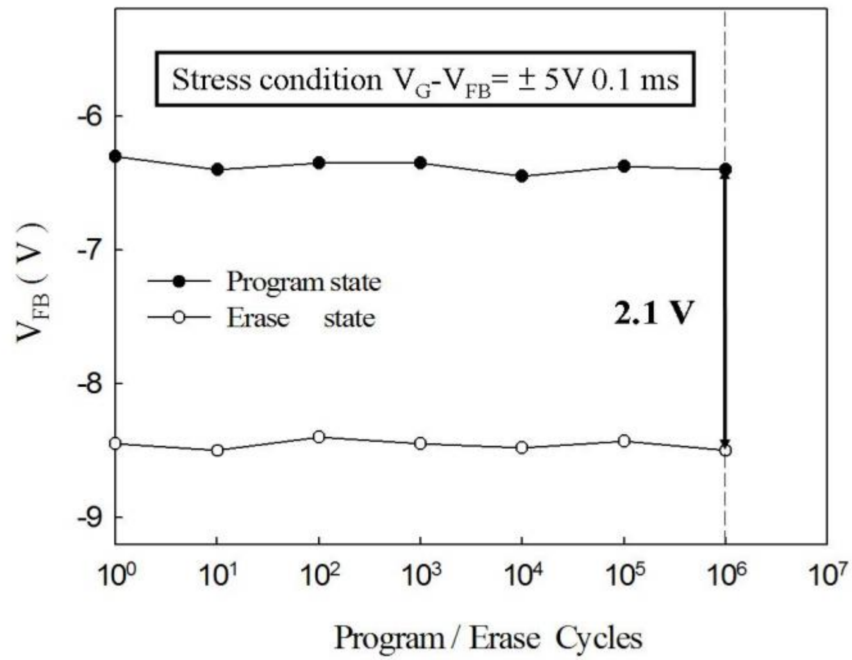


(a)

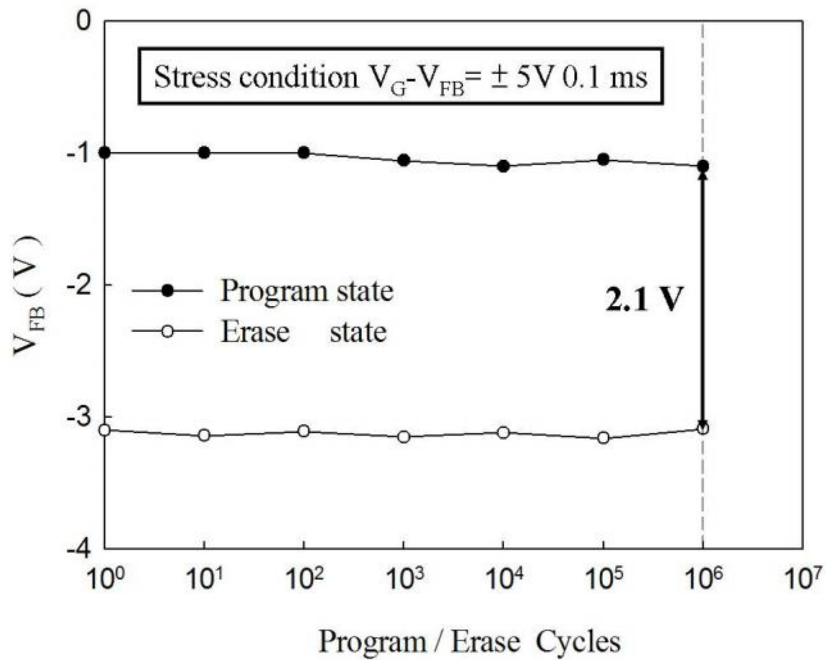


(b)

Figure 4-13 Retention characteristics of the Ni-Si-N nanocrystal memory after RTA at (a) 500 °C for 100 sec and (b) 600 °C for 100 sec.

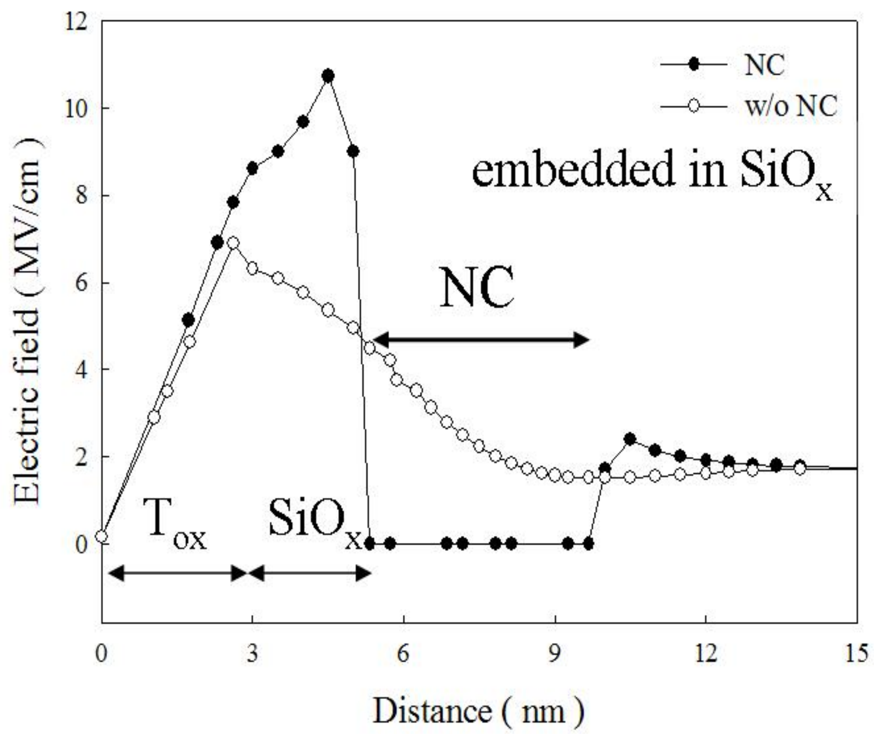


(a)



(b)

Figure 4-14 Endurance characteristics of the Ni-Si-N nanocrystal memory after RTA at (a) 500 ^{o}C for 100 sec and (b) 600 ^{o}C for 100 sec.



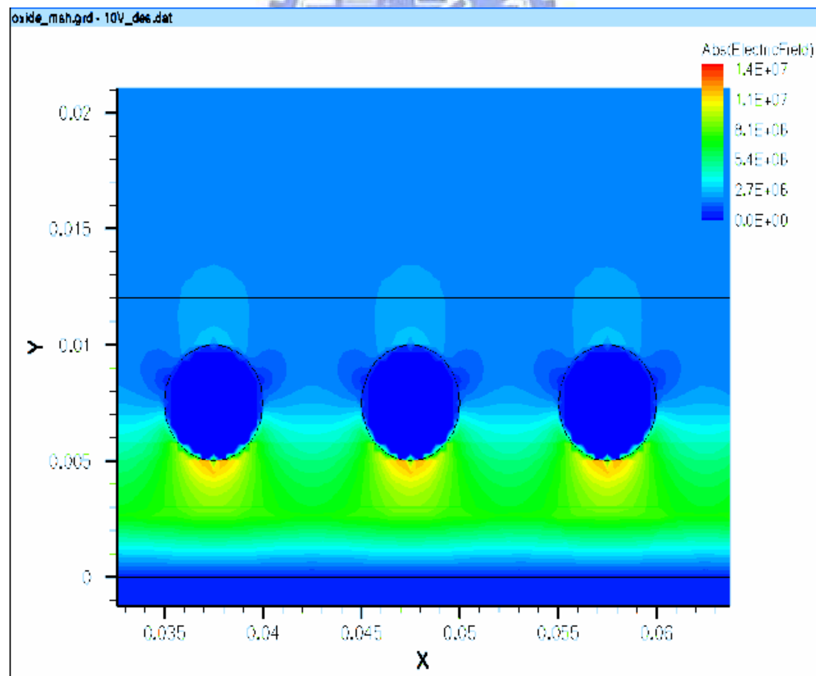
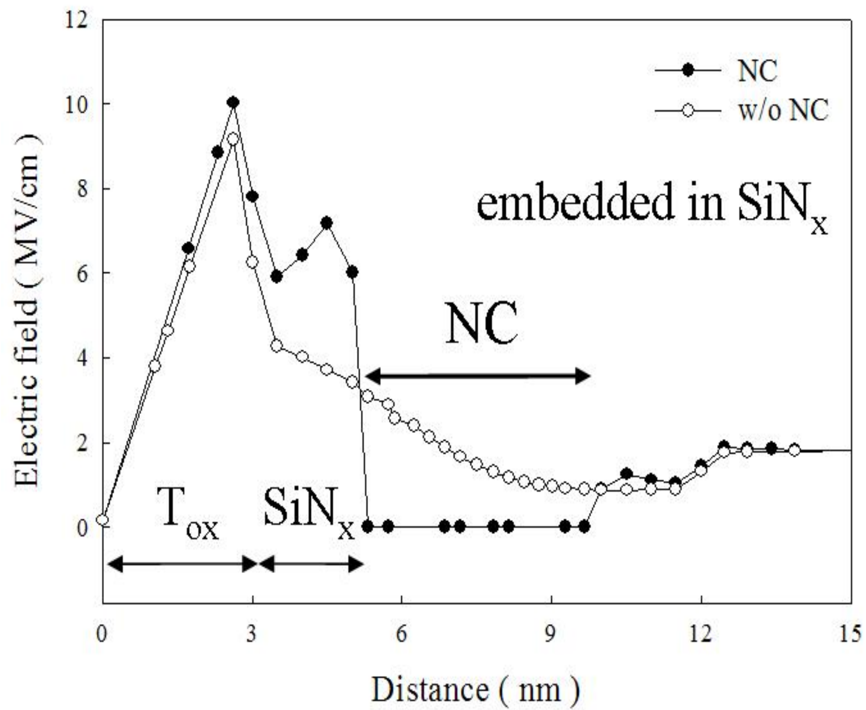


Figure 4-15(a) The simulation for electric field distribution of metal NC embedded in SiO_x.



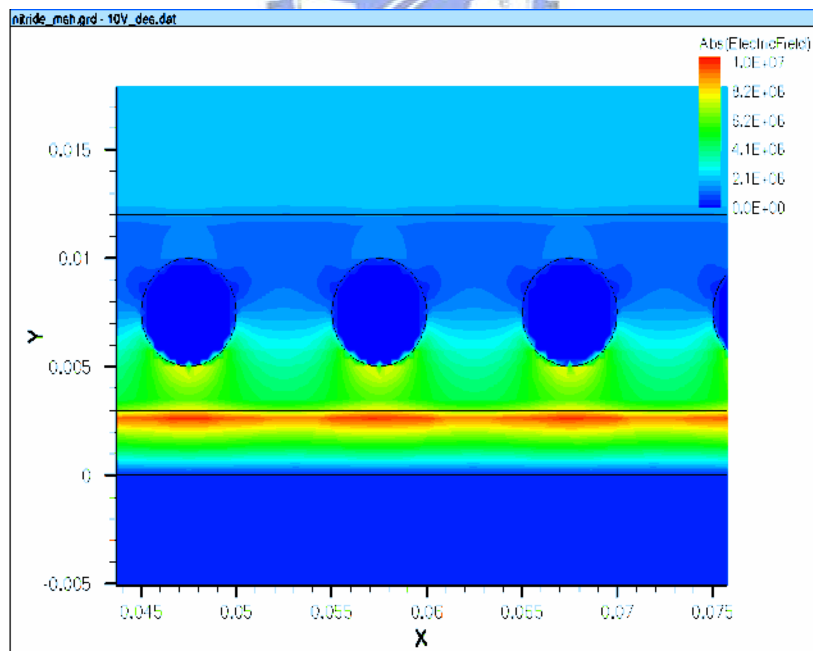
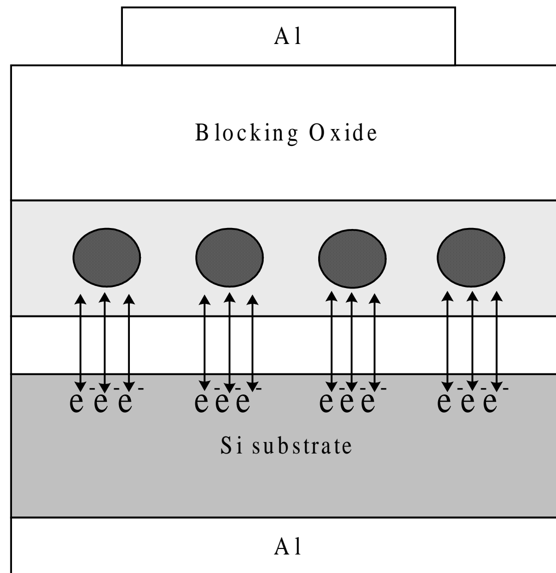
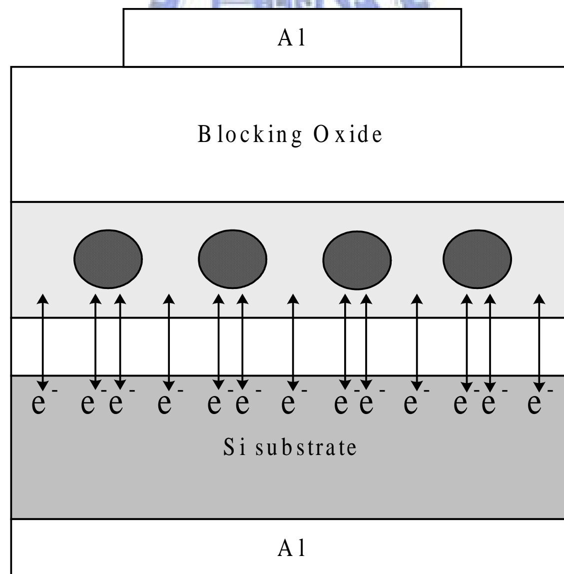


Figure 4-15(b) The simulation for electric field distribution of metal NC embedded in SiN_x.



(a)



(b)

Figure 4-16 Charge transition under Program/Erase operation for the MOIOS structure containing NiSi nanocrystals embedded in (a) SiO_x and (b) SiN_x

Table 4-1 Comparisons of memory characteristics for Ni-Si-O nanocrystal memory before and after RTA annealing in N_2.

Nonvolatile Memory	Memory window under ±10V	Memory window after 10 years	Memory window after 10^6 P/E
Ni-Si-O STD	0.8 V	40 %	0.6 V
Ni-Si-O 500 ℃	3.0 V	45 %	1.2 V
Ni-Si-O 600 ℃	1.8 V	50 %	1.5 V

Table 4-2 Comparisons of memory characteristics for Ni-Si-N nanocrystal memory before and after RTA annealing in N_2.

Nonvolatile Memory	Memory window under ±10V	Memory window after 10 years	Memory window after 10^6 P/E
Ni-Si-N STD	1.5 V	50 %	1.0 V
Ni-Si-N 500 ℃	5.0 V	52 %	2.1 V
Ni-Si-N 600 ℃	4.0 V	56 %	2.1 V

Table 4-3 Endurance properties of NiSi nanocrystal embedded in SiO_x and SiN_x after RTA process at 600 ºC.

Nonvolatile Memory	Memory window after 10^6 P/E
NiSi nanocrystal embedded in SiO_x	1.6 V
NiSi nanocrystal embedded in SiN_x	2.1 V

Table 4-4 Summary of memory characteristics for nanocrystal memories in our work.

Nonvolatile Memory	Memory window under ±10V	NC density (cm^{-2})	Memory window after 10 years	Memory window after 10^6 P/E
Ni-Si-O STD	0.8 V	1.33×10^{12}	40 %	0.6 V
Ni-Si-O 500 ºC	3.0 V	2.77×10^{12}	45 %	1.2 V
Ni-Si-O 600 ºC	1.8 V	2.87×10^{12}	50 %	1.5 V
Ni-Si-N STD	1.5 V	1.08×10^{12}	50 %	1.0 V
Ni-Si-N 500 ºC	5.0 V	2.49×10^{12}	52 %	2.1 V
Ni-Si-N 600 ºC	4.0 V	2.78×10^{12}	56 %	2.1 V