Chapter 5

Multi-Layer Ni Silicide Nanocrystal Memory

5.1 Motivation

The enhancement of performance and retention properties of nonvolatile memory devices using nanocrystals (NCs) is currently under intensive investigation since it potentially overcomes the scaling limitations of conventional nonvolatile memories (NVMs) beyond the 65 nm technology node [5.1,5.2]. A typical target is a density of NC at least 10^{12} cm^{-2} with a diameter of 5-6 nm or below. Approximately 100 NCs can control the channel of a memory FET with a 100 ×100 nm^2 active area [5.3]. High density NCs with uniform distribution is still a very demanding concern.

Recently, double-layer metal nanocrystal memories have charge storage and retention improvement over single-layer metal nanocrystals [5.4,5.5]. The first advantage of double layer nanocrystals is the high number density of nanocrystals, which is related to the amount of stored charges in a given area. Larger threshold voltage shift can be achieved by doubling nanocrystal layer without reducing the size and spacing of nanocrystals. In addition, retention improvement of aligned double-layer nanocrystal structure is reported in [5.6]. Even though stacked nanocrystals are not exactly aligned, the lower layer nanocrystals can still help reduce the charge leakage from the upper layer nanocrystals. Because of the thicker tunneling oxide of the upper-layer nanocrystals, direct tunneling from the upper nanocrystals to the channel is mostly suppressed. In this chapter, multi-layer structure nanocrystal memory is fabricated layer by layer using the sputtering deposition. Moreover, we explore the charge storage and retention properties of multi-layer nanocrystal compared with single-layer nanocrystal.

5.2 Experimental Procedures

Figure 5-1 indicates a schematic of key process steps. This memory-cell structure was fabricated on a 4 in. p-type silicon (100) wafer. After a standard RCA process,

3-nm-thick tunnel oxide was thermally grown by a dry oxidation process in an atmospheric pressure chemical vapor deposition furnace (APCVD). Subsequently, a 10-nm-thick nitrogen incorporated $Ni_{0.3}Si_{0.7}$ layer was deposited by reactive sputtering of $Ni_{0.3}Si_{0.7}$ co-mix target in the Ar (24 sccm) and N_2 (10 sccm) environment at room temperature, and the DC sputtering power was set to 80 W. Next, the rapid thermal annealing (RTA) process was performed in N_2 ambient. The annealing conditions are 500^{o}C for 100sec. On top of the single layer of nanocrystals, a 5 nm silicon nitride as interlayer is deposited by the plasma enhanced chemical vapor deposition (PECVD) system at 300^{o}C. The second nanocrystal layer was formed using the same recipe mentioned in the first nanocrystal layer. Then, a 30-nm-thick blocking oxide was deposited by the PECVD. Al gate electrodes on back and front side of the sample were finally deposited and patterned.

Electrical characteristics, including the capacitance-voltage (C-V), retention, and endurance characteristics, were also performed. The C-V characteristics were measured by Keithley 4200 and HP4284 Precision LCR Meter with high frequency 100 kHz. In addition, High resolution transmission electron microscope (HRTEM) was adopted for the micro-structure analysis.

5.3 Results and Discussion

Figure 5-2 shows typical cross-sectional TEM image of multi-layer NiSi nanocrystal structure. Especially, the lower-layer nanocrystal layer separated to two layers. We consider this phenomenon is because that a segment of Ni atoms diffuse into PECVD SiN_x during the second RTA process. Therefore, the upper-layer nanocrystal size was larger than lower-layer. There are totally three layers of nanocrsytal in this structure.

Figure 5-3 shows the forward and reverse sweep C-V characteristics, indicating the electron charging and discharging effects of multi-layer NiSi nanocrystal memory. It is clearly observed that 5 V and 13 V memory windows can be obtained under ±5 V and ±10 V operation, respectively. The C-V hysteresis loops are counterclockwise, which is due to injection of electrons from the deep inversion layer and injection of holes from the deep accumulation layer of Si substrate. The memory window of 13V for multi-layer nanocrystal structure is much larger than 5V for single-layer nanocrystal at the same

voltage sweeping (±10 V) condition. The enhancement of storage capacity is attributed to the high number density of nanocrystal, which is related to the amount of stored charges in a given area.

The charge retention properties of different memory structure at 27°C and 85°C demonstrated in Fig. 5-4(a) and (b), respectively. This measurement is carried out using gate voltage stress. The shift in the flatband voltage as a function of time is obtained by comparing the C-V curves. Obviously, the multi-layer NiSi nanocrystals have better charge retention characteristic than the single-layer. The leakage of stored charges in the upper-layer nanocrystals can be suppressed by Coulomb Blockade and energy level quantization from the lower-layer nanocrystals. Moreover, the endurance characteristic of multi-layer nanocrystals is tested in Fig. 5-5. Pulses (V_G - V_{FB} = ± 5 V, 0.1 ms) were applied to evaluate endurance characteristic for the P/E operations. The results show negligible degradation of memory window up to 10^6 P/E cycles. It retains a clear difference of 2.1V between program and erase state.

5.4 Summary Ⅲ

Multi-layer Ni silicide nanocrystal memory was obtained layer by layer using the sputtering deposition followed by low temperature RTA process. We have demonstrated multi-layer metal nanocrystal memory has charge storage and retention improvement over single-layer metal nanocrystals. The increased number density of nanocrystals can enlarge the memory windows. The leakage of stored charges in the upper-layer nanocrystals can be suppressed by Coulomb Blockade and quantization from the lower-layer nanocrystals. In addition, significant C-V curve shift of 5 V and good endurance characteristic are observed under voltage operation of 5 V. The implementation of the present structure is compatible with the current manufacturing technology of semiconductor industry and represents a viable candidate for low-power nano-scaled nonvolatile memory devices.

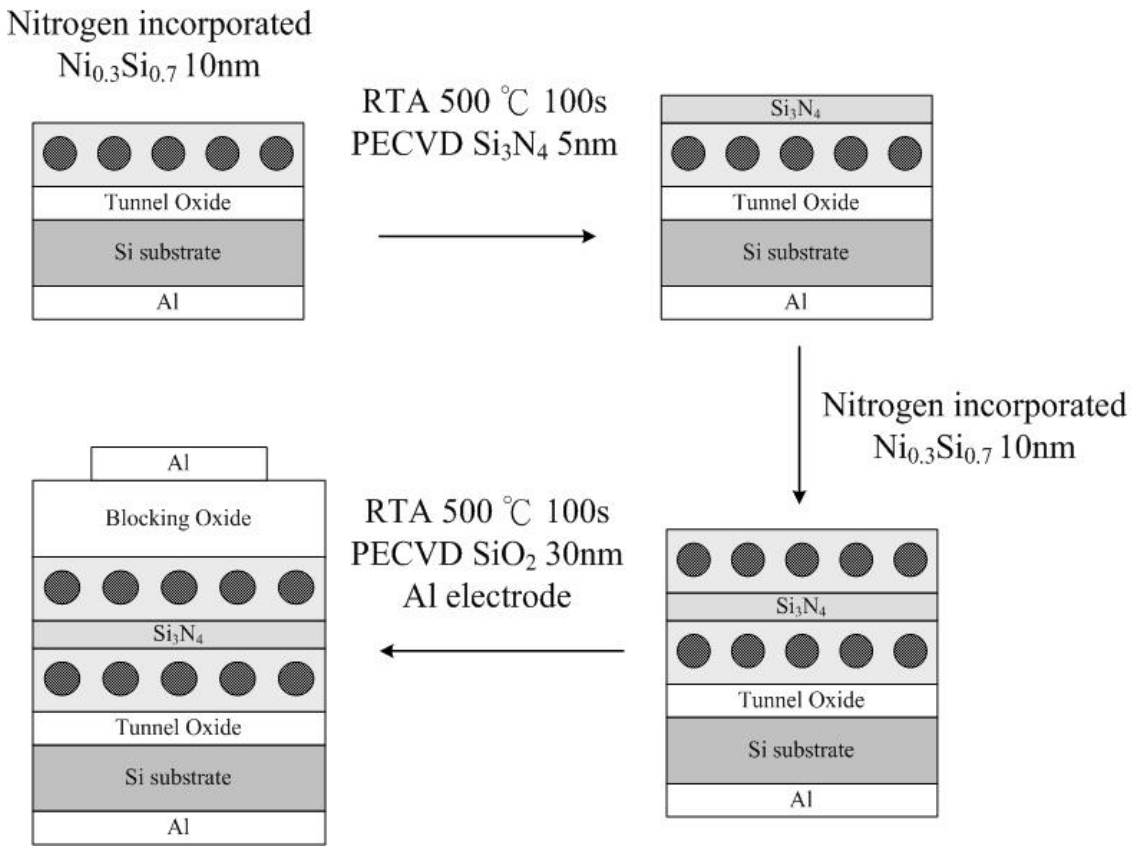


Figure 5-1 Schematics of key process steps for multi-layer Ni silicide nanocrystal memory.

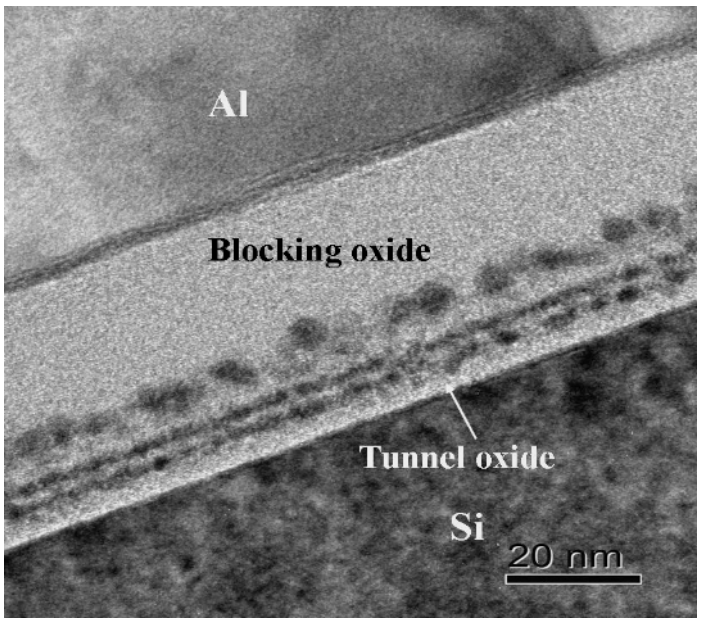


Figure 5-2 Cross-sectional TEM image of multi-layer NiSi nanocrystal structure.

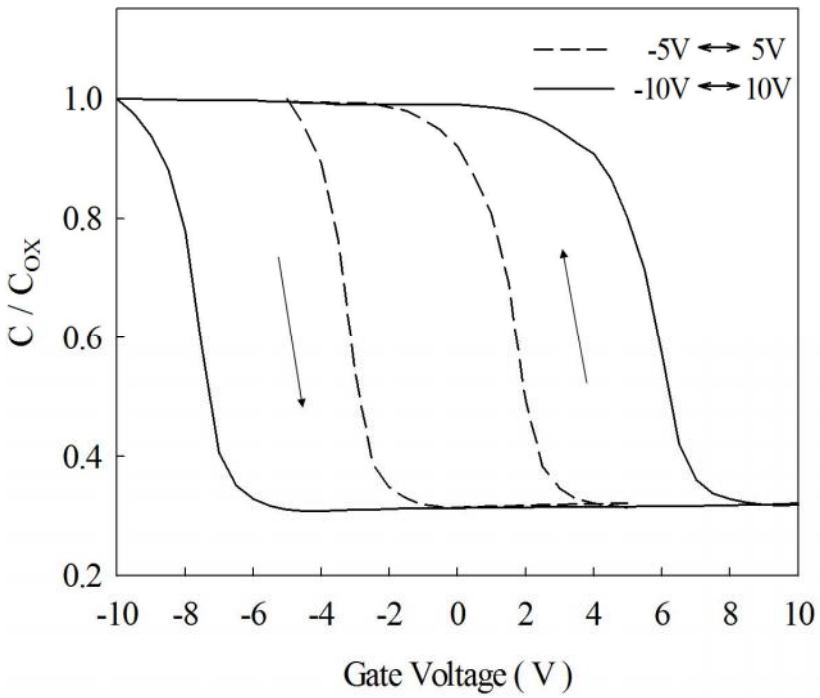
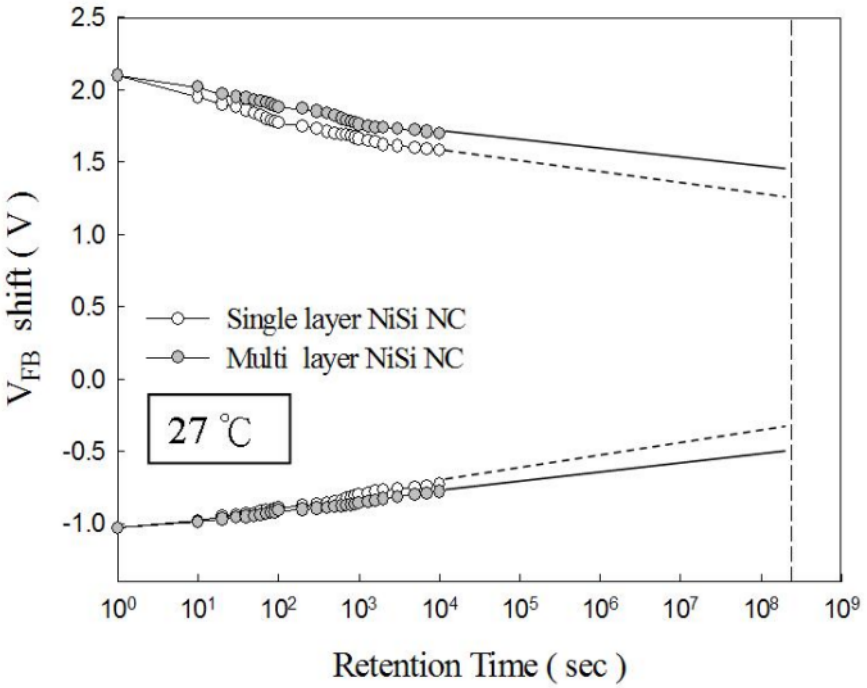
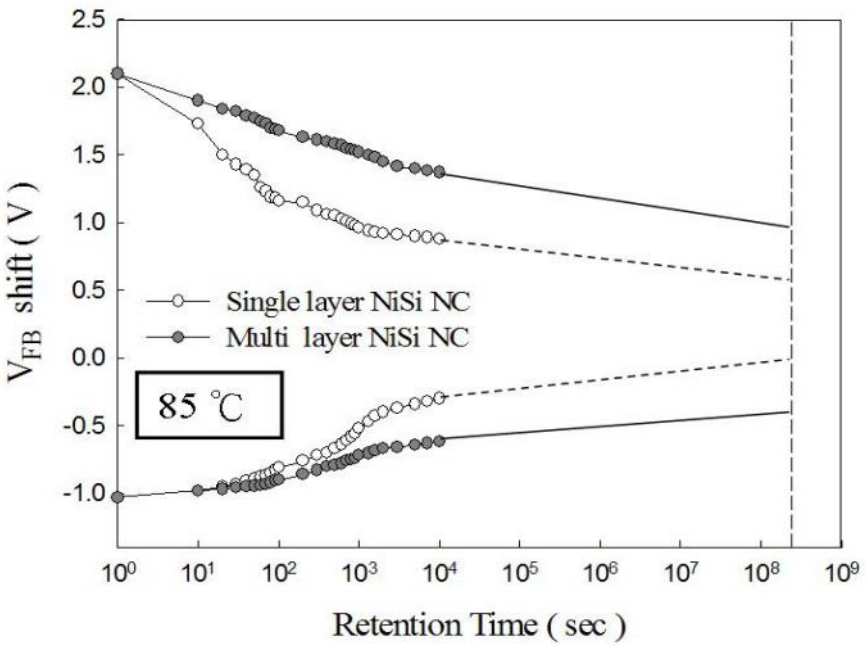


Figure 5-3 Capacitance-voltage (C-V) hysteresis of multi-layer NiSi nanocrystal memory.



(a)



(b)

Figure 5-4 Retention characteristics of the multi-layer NiSi nanocrystal memory as compared with single-layer NiSi nanocrystal memory at (a) 27 ^{o}C and (b) 85 ^{o}C.

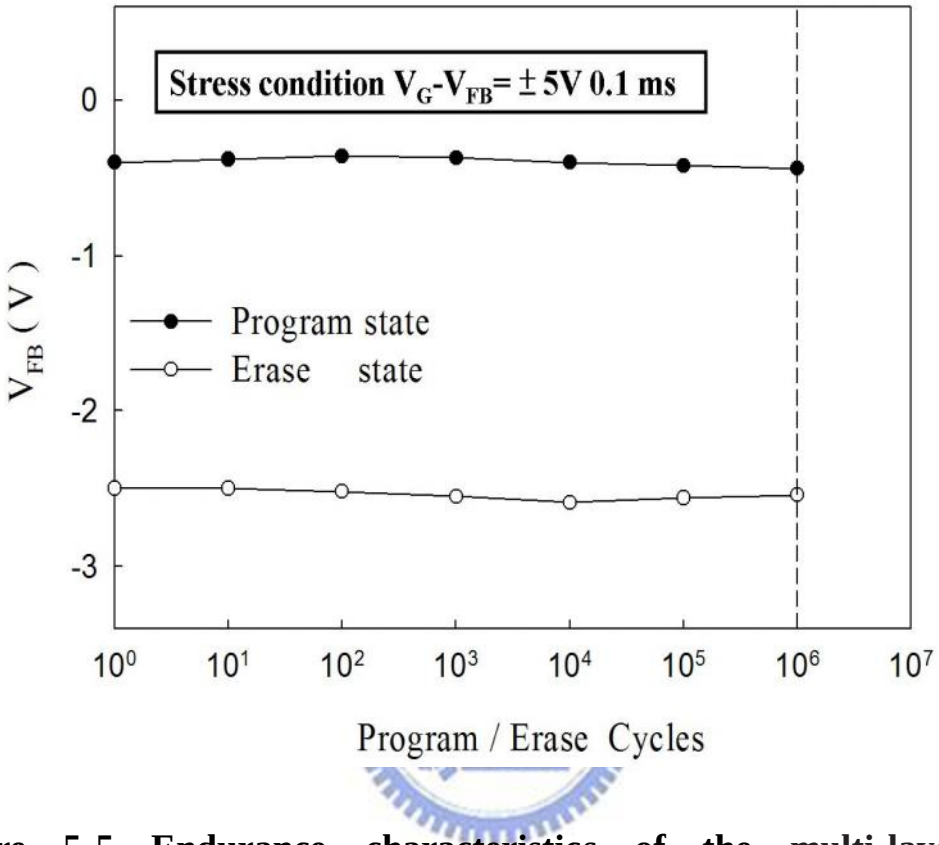


Figure 5-5 Endurance characteristics of the multi-layer NiSi nanocrystal memory.