Chapter 6

Conclusions

6.1 Conclusions

In this thesis, a novel and ease fabrication technique of Ni-Si-O and Ni-Si-N nanocrystals was demonstrated for the application of nonvolatile memory. The nonvolatile memory structure of Ni-Si-O nanocrystals embedded in the SiO_x layer was fabricated by sputtering a co-mix target ($Ni_{0.3}Si_{0.7}$) in an Ar/O_2 environment at room temperature. It can be considered that the oxygen plays a critical role during sputter process for the formation of nanocrystal. The high density ($\sim 10^{12}$ cm^{-2}) nanocrystal can be simple and uniform to be fabricated. Another similar process for Ni-Si-N nanocrystals is also proposed by sputtering a co-mix target ($Ni_{0.3}Si_{0.7}$) in the argon (Ar) and nitrogen (N_2) mix-gas environment at room temperature. It was also found that high density Ni-Si-N nanocrystals embedded in the silicon nitride (SiN_x). This fabrication technique for the application of nonvolatile nanocrystal memory can be compatible with current manufacture process of the integrated circuit manufacture.

A rapid thermal annealing (RTA) with low temperature (500°C~600°C) and short duration (100sec) is used to improve the crystalline quality of nanocrystals and memory characteristic. During the RTA process, the metallic Ni-Silicide (NiSi) nanocrystals precipitate and show good crystalline quality. The NiSi nanocrystal with good crystalline quality has higher density of states to store charge and cause larger memory window. The reliability issues, such as retention and endurance, are significantly improved after the RTA process. According the results of J-V characteristic and XPS analysis, thermal treatment (RTA) can reduce the defects (leakage path) in the dielectric (SiO_x or SiN_x) which surrounds the nanocrystal. It decreases the probability of charge escaping from the nanocrystal. The quality of dielectric is also strengthened to bear the P/E cycling stress.

The charge storage layer of nanocrystal embedded in SiN_x shows larger memory

window and better reliability over nanocrystals embedded in SiO_x. The improvement of charge storage capacity is attributed to additional accessible charge trap states in the SiN_x matrix. For retention property, the stored charge can be shared among the nitride traps, the enhanced field by stored charge (Coulomb blockade) through the tunneling oxide can be reduced. This result decreases the probability of charge escaping from the nanocrystal. Moreover, charges are likely to be relaxed to the nitride traps. Leakage through the intermediate medium can also be inefficient due to Coulomb Blockade. Therefore, nanocrystals embedded in SiN_x show enhanced retention characteristics. In addition, because of high permittivity (ε) of nitride, the charge transition is more uniform due to the electric field distribution. Combining NiSi nanocrystals and SiN_x as charge trapping layer can improve the endurance characteristic for P/E cycling operation.

Multi-layer Ni silicide nanocrystal memory was obtained layer by layer using the sputtering deposition followed by low temperature RTA process. We have demonstrated multi-layer metal nanocrystal memory has charge storage and retention improvement over single-layer metal nanocrystals. The increased number density of nanocrystals can enlarge the memory windows. The leakage of stored charges in the upper-layer nanocrystals can be suppressed by Coulomb Blockade and quantization from the lower-layer nanocrystals. In addition, 5 V memory window under $\pm$ 5V operation and superior endurance characteristic are obtained, which is suitable for the application of low-power nanoscaled nonvolatile memory.