國　立　交　通　大　學

電子工程學系電子研究所

博　士　論　文

無線近距離資料傳輸基頻收發器設計技術之研究

Baseband Design Techniques for Wireless Proximity Data Transmission

研究生：游瑞元

指導教授：李鎮宜博士

中華民國九十七年七月

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摘要

無線應用中的近距離資料通訊系統為本論文專注的主軸。在這樣的系統中，功率和效能是最主要需要克服的問題，而本論文著重在使用全數位的設計方案來降低功率與增進系統效能。而這些方案的驗證平台則是使用無線正交展頻調變為基礎的基頻處理器。

近距離資料通訊的相關問題，則是在兩個系統中來探討與評估。一為 IEEE 802.15.3a MB-OFDM 超寬頻系統；另一則為自有定義之系統，命名為 uPHI/WiBoC。這兩者系統分別歸類於無線個人網路(WPAN)以及無線近身網路(WBAN)當中。這兩個系統的共通特性為以封包為基礎之短距離通訊系統。在使用的超寬頻系統中，其傳輸數率為 480Mb/s，在這樣的高速傳輸速率之下，系統效能顯得相當容易受到非理想效應干擾，而傳輸與接收功率也分別被定義在 180mW 與 323mW 以下。在自有定義之 uPHI/WiBoC 系統下，則是專注在一毫瓦以下(sub-mW)的功率設計方案，同時其傳輸速率則屬於低速的系統 (<10Mb/s)。綜合上述情境下，本文在基頻處理器中提出幾樣以數位設計方案，來達到低功率與高效能的目的，而這樣的設計理念可同時應用在低速與高速無線短距離通訊系統之中。

第一個方案為全數位式鏡相消除技術，用來解決 RF 與基頻訊號在轉換過程中所產生的實虛兩軸不批配的問題，這個現象消減基頻處理器在解調變訊號的效能。在這個方案之中，定義了一個誤差函數，可應用在窄頻與寬頻的條件之下，此誤差函數使得系統

可使用可適性的技術來達到系統效能改進。此方案可以校正 2dB 的增益誤差及 20° 的相位誤差。同時最大可以改善 2.5dB 的訊躁比。

在動態取樣時序控制的方案當中，可將訊號取樣頻率從 Nyquist 或更高的頻率調降至符號頻率。此數位智慧型控制方案大幅降低基頻的功率消耗，同時使得訊號可在最佳取樣點取樣。使用此智慧型控制方案，最大可以增進 1.7dB 的訊躁比，同時可以有效降低 40%功率消耗。

在遲滯電路的設計方案之中，本概念使用於全數位控制震盪器中，此震盪器可應用於全數位鎖相迴路與全數位延遲迴路之中。這兩個迴路的應用情境，通常為持續作動的電路，因此通常會連續消耗動態與靜態功率。而這個遲滯電路與一般的標準函式庫元件相較起來，在訊號延遲產生效果上，可降低 72.12~99.26%的功率消耗。而在整體全數位控制震盪器效能上，則可以降低 98%的功率以及 95%的面積。

在硬體實現部分，則是藉由超寬頻與 uPHI/WiBoC 的基頻處理器來驗證相關方案的概念。超寬頻基頻處理器整合了全數位鏡相消除技術與動態取樣時序控制技術，降低了 40%的功率消耗。而在 uPHI/WiBoC 基頻處理器，則是應用了電壓域以及功率域的分割方案，來達到以電路層級的功率控制與能量節省，這使得此基頻處理器能夠操作在最低 0.5V 的電壓，達到 10μW 以下的功率消耗。

Baseband Design Techniques for Wireless Proximity Data Transmission

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Abstract

Proximity data communications in wireless applications are targeted in this work. The proposals are studied to overcome power and performance issues in this communications scenario. The power reductions and performance improvements are all achieved by digital approaches evaluated in a wireless OFDM-based baseband processor.

The proximity data communications is explored and evaluated in the IEEE 802.15.3a MB-OFDM UWB and an in-house designed system (uPHI/WiBoC) that corresponds to the wireless personal area network (WPAN) and the wireless body area network (WBAN), respectively. Both of them are packet-based short range wireless communications schemes. The MB-OFDM UWB is designed for high speed 480Mb/s transmissions so that it is performance sensitive in such high rate communication with power budget no more than 180mW and 323mW in transmission and receiving, respectively. The uPHI/WiBoC system is designed with low rate communications (<10Mb/s) in the sub-mW power constraint. Accordingly, this work proposes several digital-based schemes in the baseband for power reductions and performance improvements to meet both the low-rate to high speed short range wireless communications systems.

The first proposal is an all-digital I/Q-mismatch cancellation (ADIQMC) proposed to solve I/Q mismatch during RF conversions that degrades baseband decoding performance. This work defines the error function in both narrow and wide band channel so that the error

cancellation can be achieved adaptively. The gain- and phase-error tolerances are 2dB and 20° , respectively, with maximum 2.5dB SNR reduction.

The dynamic sample-timing control (DSTC) reduces the sampling rate in an ADC circuit from Nyquist rate or higher rate to the symbol rate. This digital smart control scheme largely reduces the baseband power consumption and enables the best-position signal sampling. This DSTC scheme enables a possible maximum 1.7dB SNR improvement with 40% power reduction.

The hysteresis delay cell (HDC) is designed and applied to the utilization in a digitally controlled oscillator (DCO) that may be used in an all-digital phase locked loop (ADPLL) or an all-digital delay locked loop (ADDLL). The DCO circuits in an ADPLL or an ADDLL are an always-active circuits that continuously consume dynamic and static power even in the chip inactive duration. The HDC, depending on the topologies, provides a 72.12~99.26% power reduction compared to a cell-based delay cell. The overall DCO dynamic power and area with the HDC designs are reduced by 98% and 95%, respectively, compared to a cell-based DCO design.

The baseband processors are implemented in both of the MB-OFDM UWB and uPHI/WiBoC systems. The UWB baseband processor integrates the ADIC and DSTC circuits, providing a 40% power reduction evaluated with a whole physical layer circuits. The uPHI/WiBoC applies the voltage-domain and power-domain partitions for circuit-level power control and energy saving. This enables the WBAN baseband processor operated in minimum supply voltage 0.5V with sub-10μW power consumption.

誌謝

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Chapter 1:

Motivations

More Moore and more than Moore are currently opposite but both critical trends in semiconductor developments. These dual trends correspond to the Moore's Law and system integration law as illustrated in Fig. 1-1 [1]. More Moore is achieved by integrating more and more transistors into a specific core area, providing a condensed chip design circuitry. On the other hand, the trend of the more than Moore presents heterogeneous integrations with existing technologies, such as semiconductor, micro-electro-mechanical systems (MEMS), scavenging energy source, etc.

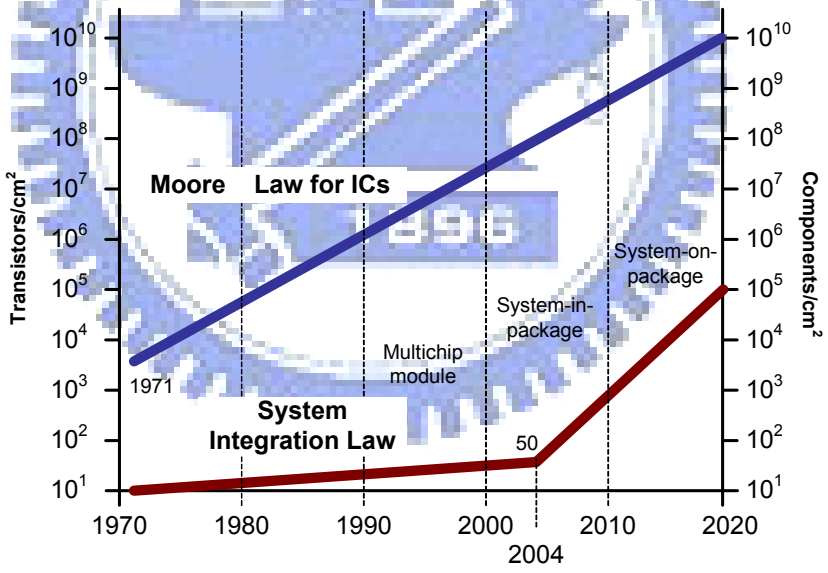


Fig. 1-1. The two trends in semiconductor developments

More Moore trend is pursued in increased processing speed and chip computing power. Those applications are required with shorter processing time and more function services. Wireless systems toward this tendency may be found in IEEE 802.11b, 802.11a/g, UWB, and next generation Giga-bit/sec UWB that serve higher data rate with increased processing speed and signal bandwidth as the technology process progresses. The high-data-rate demands require higher computation complexity and hardware cost to achieve large media transmissions. This implies that more and more transistors are integrated in a wireless chip, especially a digital baseband processor. As a result, power consumption becomes the vital problem, especially integrated in a portable device.

The more-than-Moore trend faces design challenges in integrating several components into a tiny stack, including reductions of device area and eliminations of external components. These can be particularly found in wireless sensor-oriented devices applied in the systems such as wireless body area networks (WBAN) or wireless sensor networks. One key point in designing more-than-Moore based heterogeneous devices is the reduction of circuit power. The target power in a device is suggested below micro-Watt (μW). If this μW-device is achieved, lots of energy-limited sources by scavenging-based approaches like motions, temperatures, or solar power can be attached with an extreme tiny size or even integrated inside. Otherwise, it is necessary to replace those scavenging sources with high-capacity battery for a normal device operation if large power is drawn. In other words, a tiny device is achieved only when little power is consumed in the circuits. However, it is not easy to reduce device power without eliminations of external components. Any passive or active external components result in large power waste compared with any integrated circuits because signals have to go through many unnecessary paths for the

reasons of level translations, signal protections, etc. This largely reduces energy efficiency and increases difficulty in the device-size shrinking. Accordingly, low power is required for heterogeneous devices to achieve tiny area, and eliminations of external components are one of the ways to achieve the low-power purpose.

A general spectrum of the more-Moore and more-than-Moore trends is shown in Fig. 1-2. This spectrum summarizes the key categories towards more-Moore and more-than-Moore sides. The more-Moore side may have baseline CMOS and memory designs. For the possible designs with variant material substrates, the more-than-Moore side may include the radio-frequency (RF) circuits, high-voltage (HV) power designs, passive components, sensor devices, and further bio-oriented interfaces.

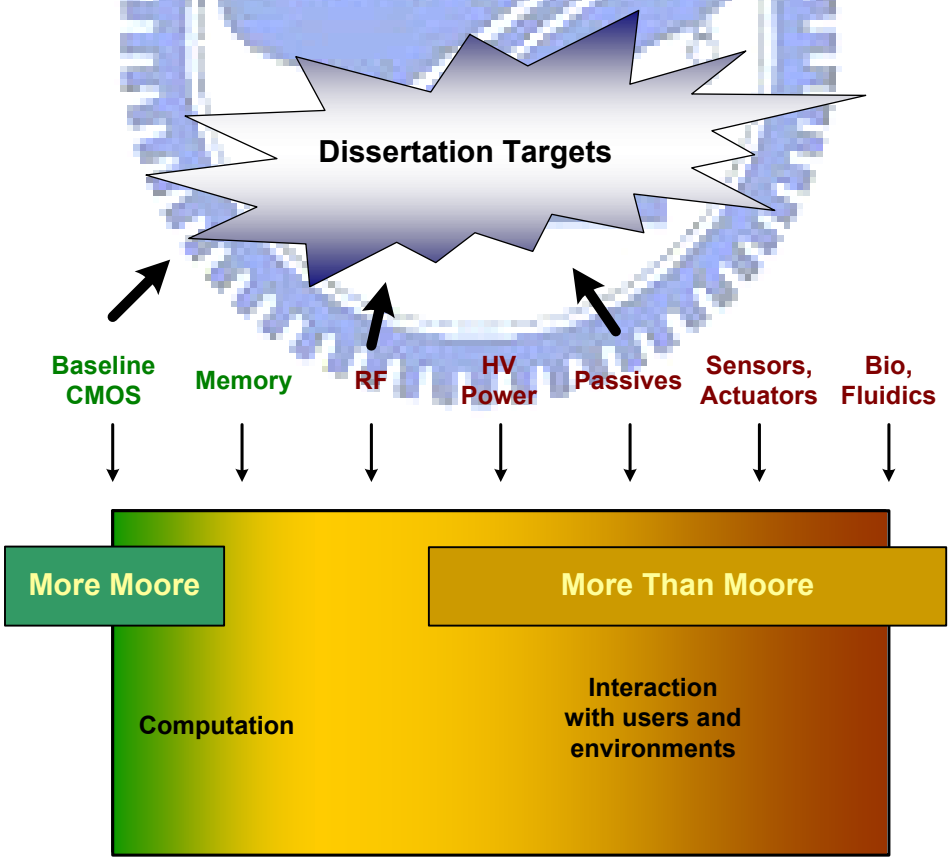


Fig. 1-2. The more-Moore and more-than-Moore spectrum

In the progress of this two-trend spectrum of semiconductor industry, the power, performance, and cost always play crucial role that may possible dominate the market development and applications. As each item in this spectrum proceeds to advanced or higher integration, those indicator matrices (power, performance, and cost) becomes more and more difficult to solve. Accordingly, this dissertation focuses on the problem solving in the bottleneck of (1) baseline CMOS (2) RF circuits (3) passive components. The evaluation cases will be the wireless communications systems on the OFDM-based modulation scheme.

The improvements of baseline CMOS, RF circuits, and passive components may target on power saving, performance improvement, and area shrinking for highly integration. Those can be explored by the point of view in the system level, architecture level, and circuit level as illustrated in Fig. 1-3. Moreover, the approaches may be also considered as digitally-based analog circuit calibration/controlling or all digital designs. In the system level approach, the all-digital I/Q-mismatch cancellation RF calibration is applied to improve RF circuit and overall system performance in digital signal process. Furthermore, a dynamic sampling-timing control (DSTC) approach controls the sampling timing of data converters, providing better system performance and reduced power consumption. Then an embedded silicon-crystal generator (ESCG) is designed for the passive component elimination of external crystal. Then, a hysteresis delay cell (HDC) clock source design corresponds to the baseline CMOS design that targets mainly on an-order power reduction in the clock generation design. In the circuit-level design considerations, the distributed coarse-grain power control (DCGPC) is utilized for power reduction in the baseline CMOS circuit designs.

In the evaluation platforms, OFDM-based wireless communications systems, those design innovations are achieved and demonstrated in a baseband circuit, as shown in Fig. 1-4. Those building blocks have the design philosophy that improves the baseline CMOS, RF circuits, and the passive component eliminations.

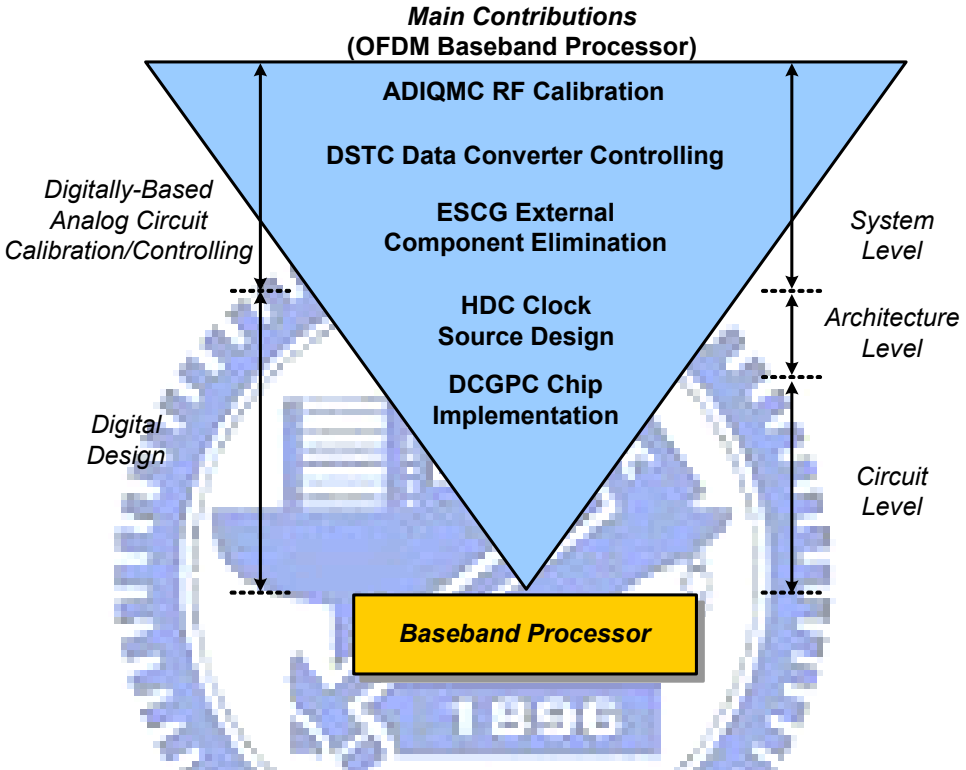


Fig. 1-3. The contribution matrix

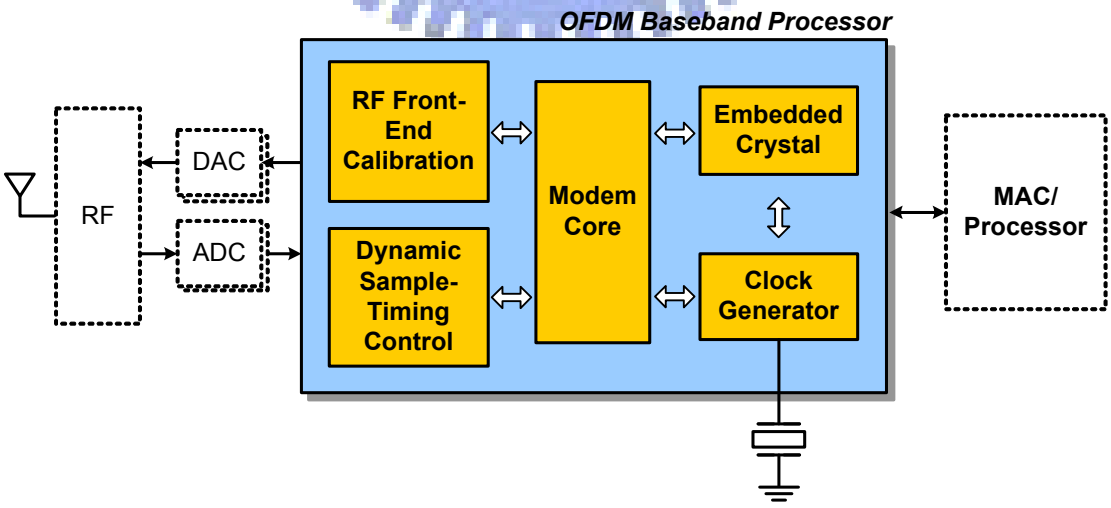


Fig. 1-4. The evaluation vehicle

The main idea to achieve the proximity data and power transmission is to modify some analog-circuit behaviors of those components, like RF circuits, analog-to-digital converters (ADC), and external crystal, into a digital-based design that can largely reduce the design efforts of those collaborative devices. Moreover, the digital design itself also adopts circuit-topology techniques to further reduce power consumption. In other words, the data and power issues of a wireless physical-layer device are re-directed to and focused on the digital baseband design that can be designed with lower power and cost. The approaches are achieved without sacrificing system performance. Those contribution items, more specifically, may shortly be summarized as follows.

1-1 All-digital I/Q-mismatch cancellation (ADIQMC) for RF front-end performance improvement

Radio-frequency (RF) circuits are utilized to up-covert baseband signals to a high-frequency band in a transmitter side, and on the contrary, down-convert them to a baseband frequency in a receiver. This up-down conversion is achieved via a set of orthogonal bases, $A \cdot \cos\omega t$ and $A \cdot \cos(\omega t+\pi/2)$, for frequency mixing. In realistic hardware circuits, however, the orthogonal bases cannot be designed as expected in terms of gain balance (A) and phase offset (π /2), resulting in unwanted-image and desired-signal blending in decoded signals. This distorts signals and degrades system performance. This part provides an all-digital I/Q-mismatch cancellation (ADIC) approach to eliminate unnecessary image signals in an all-digital signal process behavior.

1-2 Dynamic sampling-timing control (DSTC) for ADC power reduction

Nyquist frequency is a fundamental frequency that should be used to sample an analog continuously waveform without loss of information. In wireless applications, a baseband processor usually applies a sampling frequency that is even more than Nyquist rate, say 4x or 8x of signal bandwidth, to acquire more accurate signal sampling and possible better signal quality. This high sampling-frequency, however, drives an analog-to-digital convert (ADC) circuit operating in a rather high frequency status and generates digital signals that are a multiple of original transmitted samples. This in term increases ADC circuit sampling power and complicates digital signal processing. The proposed dynamic sample-timing control (DSTC) in this part presents an architecture in additional to its corresponding computation algorithm that enables a baseband receiver sampling incoming waveforms at the frequency that is equal to the symbol rate in the transmitter. This symbol-rate sampling behavior minimizes operation efforts in an ADC circuit, resulting in minimized ADC operation power. At the same time, the loading of digital signal processing is reduced. The overall scenario is designed without loss of system performance.

1-3 Hysteresis delay cell (HDC) for clock generator power reduction

A clock generator stays active all the time because digital signal process requires clock trigger edge for computation. This part of circuit cannot be turned off even if a system is not in operation. An always-on operation implies that circuit power is continuously consumed, including dynamic and static power. As the power from data

computation and signal transformation is getting lower and lower, the amount of clock-generation power becomes obvious. However, state-of-the-art clock generators apply inverters/buffers concatenated together for large delay generation. Those short-delay components (inverters/buffers) require too many charge-discharge actions in each delay generation, resulting in tremendous power waste. Consequently, this proposal provides a design scheme, cell-based transition-free delay generation (TFDG), to prevent components output from unnecessary charge-discharge transitions. This reduces dynamic and static power consumed in clock signal generations.

1-4 Dynamic coarse-grain power control (DCGPC) for power reduction

A wireless transceiver, including the RF and the baseband processor, is in active only when signals are ready for transmission or receiving. Otherwise, most of the building blocks stay in the idle mode. This idle status does not waste too much static power until deep submicron circuit process is applied. One of the most effective approaches to reduce static power is isolating supply-power source from its feeding components. This work proposes a dynamic coarse-grain power control (DCGPC) scheme to cut off power paths in any inactive building blocks for most leakage power savings. The DCGPC distributes over the whole circuit floorplan to provide individual on-off controls.

1-5 Embedded silicon-crystal generation (ESCG) for cost and power reduction

An oscillator or a crystal is necessary for wireless applications or sequential signal computations. It provides an accurate and PVT-insensitive reference frequency for clock generations. The crystal components and oscillator circuit are presented as the forms of the two-pin and four-pin stand-alone components, respectively, outside of a chip. Its area size usually occupies more than 50% of a main chip. The power dissipation is in the order of 10mW. As technology progresses, the system and consequently chip area are approaching highly-integrated extreme small area and uW power level. This external physical crystal or oscillator becomes an obstruction to achieve this goal. Accordingly, this work proposes an embedded silicon-crystal generation (ESCG) to provide a pseudo crystal that can be implemented in a silicon substrate. In other words, it can be further integrated in a whole chip system with circuit design approaches. This largely reduces the interfacing efforts between chip-chip communications. The power consumption and area size are accordingly shrunk.

Chapter 2:

Introduction

Short range and low power orthogonal frequency-division multiplexing (OFDM) based wireless communications systems are targeted in this work. The selected demonstration systems include:

(1) the multi-band OFDM ultra wide-band (MB-OFDM UWB) system defined in IEEE 802.15.3a [2]

(2) the wireless body on a chip (WiBoC) system defined by an in-house protocol [3]

The MB-OFDM UWB and WiBoC are classified as wireless personal area network (WPAN) and wireless body area network (WBAN), respectively, as shown in Fig. 2-1.

The unique features of both the elaborated WPAN and WBAN systems from the other network applications can be listed as follows. In other words, this work focuses on those issues for the problem solving.

(1) *Portable device*:

A portable device is usually power-thirty. Not only the power has to be reduced, but also the duration is a major concern. Otherwise, several applications addressed in WPAN and WBAN won't be applied.

(2) *Small form factor*:

Among the portable devices, the hardware of WPAN and WBAN is

especially required to be in small form factor for convenient or even ubiquitous carrying. So, robust signal process with reduced calibration components in addition to reduced power consumption with possible tiny battery is the necessary design constraint to achieve this goal.

(3) *Packet-based transmission*:

WPAN and WBAN are almost designed with packet-based transmission. All the signal process techniques are developed under this assumption.

(4) *Mild channel effects*:

The short distance transmission is also the feature for both the WPAN and WBAN systems. This implies a milder Doppler and multipath fading channel effects. This enables the following researches focus more on system operations among every building block in terms of algorithm and hardware implementation.

(5) *OFDM modulation*:

The elaborated system protocols from the WPAN and WBAN applies the OFDM modulation so that the development methodologies may target on both the time-domain and frequency-domain approaches.

According to the system features as listed, this work proposes several schemes to approach the more-Moore and more-than-Moore design goals, including the ADIC, DSTC, HDC, DCGPC, and ESCG that are described in Chapter 1.

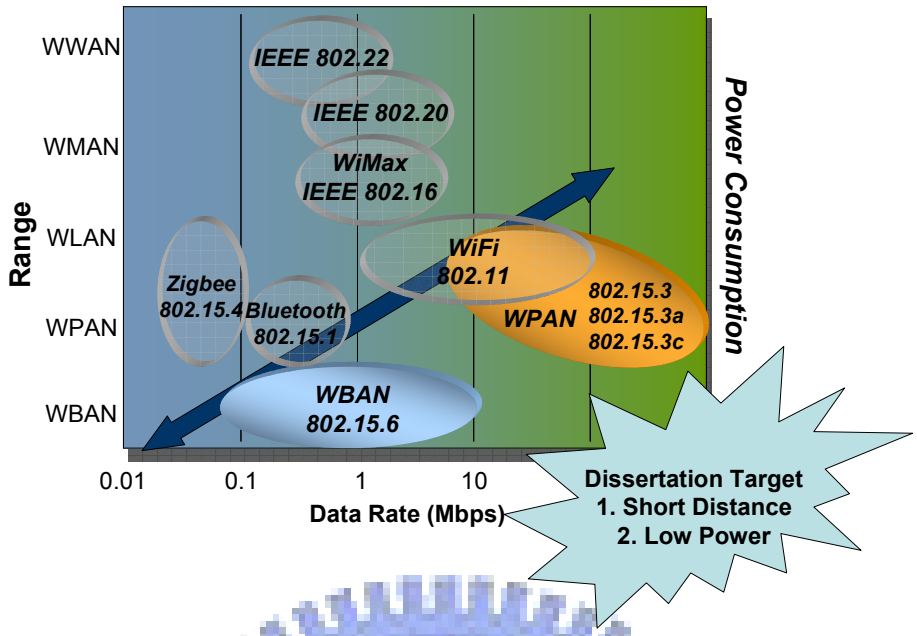


Fig. 2-1. The target short range platforms for evaluations

The WPAN is operated in the range of 1~10 meters that is defined as personal communications area. The system is almost implemented in a portable device so that power consumption is the main concern in this kind of applications. Usually, the power is required to be less than 100mW so that a battery can support the operation for the necessary working duration. The possible data rate may be ranged from a mega to a giga bit per second.

The WBAN is also a short-range communications system that provides an even shorter transmission distance than the WPAN, i.e. within 3 meters. The target power is no more than 10mW. Existing working group toward this application may be found in IEEE 802.15.6, but the standard is far from standardized at present (the year 2008, July). Consequently, an in-house protocol (WiBoC) is evaluated in this work that targets on a sub-mW WBAN system design.

In the following, a brief review of the system specifications for both the MB-OFDM UWB and WiBoC will be introduced.

2-1 Multi-Band OFDM Ultra Wideband in WPAN

The MB-OFDM UWB is defined in IEEE 802.15.3a [2]. This system utilizes the unlicensed UWB band from 3.1~10.6GHz, providing a wireless personal area network with data payload communication capabilities of 53.3, 55, 80, 106.67, 110, 160, 200, 320, and 480 Mb/s. Among those provided data rates, the 53.3, 106.67, 110, and 200Mb/s are mandatory in supporting the communications. This UWB employs orthogonal frequency division multiplexing (OFDM) as the core modulation scheme. Each OFDM symbol utilizes 128 subcarriers for transformations, and a total of 112 subcarriers are used for signal transmission, including 100 subcarriers as information carriers and 12 pilot tones for communications synchronizations. The other 10 subcarriers are used as guard tones to release the spectrum mask design efforts. The subcarriers are modulated by quadrature phase shift keying (QPSK). The rest of six unused subcarriers (128-122) are filled with null values that are located in the side band and the DC index. The QPSK symbol rate is 528M Symbol/sec. Therefore, the occupied unshaped spectrum for each OFDM symbol is 528MHz. The evaluated forward error correction coding scheme include both a convolutional code and a low-density parity check code (LDPC). The convolutional code is used with a coding rate of 1/3, 11/32, 1/2, 5/8, and 3/4. The mappings between QPSK symbols and OFDM subcarriers are factorized by a conjugate symmetric parameter. When the IFFT input is regarded as conjugate symmetric, the N used subcarriers, for example, are generated by a total of N/2 information subcarriers. If the time-spreading is further

applied to be twice, the symbols of the IFFT output is generated from the number N to 2N, resulting in an overall spreading gain (2N)/(N/2)=4. A higher transmission speed corresponds to a lower overall spreading gain so that the spectrum efficient is highest. The summary of the baseband modulation is given in Table 2-1.

TABLE 2-1. DATA RATE PARAMETERS OF MB-OFDM-BASED UWB SYSTEM

Data Rate (Mb/s)	Modulation	Coding rate (R)	Conjugate Symmetric Input to IFFT	Time Spreading Factor	Overall Spreading Gain	Coded bits per OFDM symbol (N_{CBPS})
53.3	QPSK	1/3	Yes	2	4	100
55	QPSK	11/32	Yes	2	4	100
80	QPSK	½	Yes	2	4	100
106.7	QPSK	1/3	No	2	2	200
110	QPSK	11/32	No	2	2	200
160	QPSK	½	No	2	2	200
200	QPSK	5/8	No	2	2	200
320	QPSK	½	No	1 (No spreading)	1	200
400	QPSK	5/8	No	1 (No spreading)	1	200
480	QPSK	¾	No	1 (No spreading)	1	200

This system also utilizes a time-frequency code (TFC) to interleave coded data over three frequency bands, and each group consisting of the three frequency bands is also defined as a band group. The UWB spectrum (3.1~10.6GHz) is used for four such band groups, and each group is composed of the three bands, except a band group with only two bands. In other words, there are four 3-band TFC and one 2-band TFC that provide the capability to define possible eighteen separate logical channels, as illustrated in Fig. 2-2. When the system is operated in a certain band group, say band group #1, there are three bands available for transmission. The TFC controls what time and what band the packet is going to be sent within this band group. This controlling is in the scope of an OFDM symbol, so every OFDM symbol may be sent

in different band number in a band group. An example can be seen in Fig. 2-3. It shows that each OFDM symbol is transmitted in the order of band #1, band #2, and band #3. This behavior is also identified as frequency hopping so that the effects of interference can be reduced. The pattern of the TFC can be further referred to the specification [2].

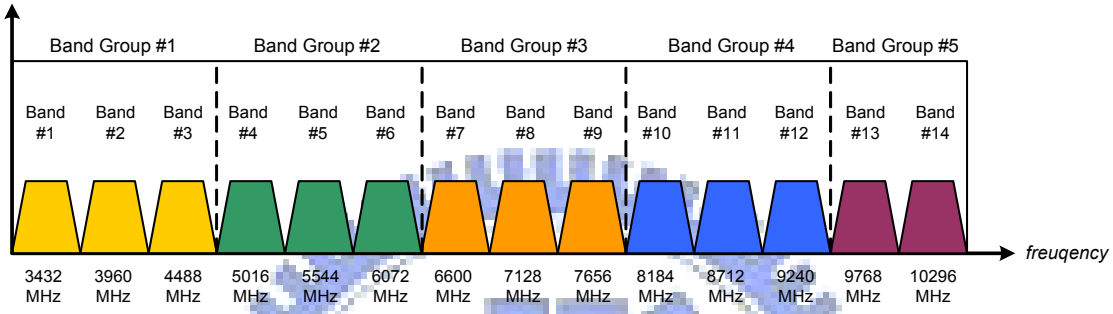


Fig. 2-2. The band group plans in the UWB spectrum

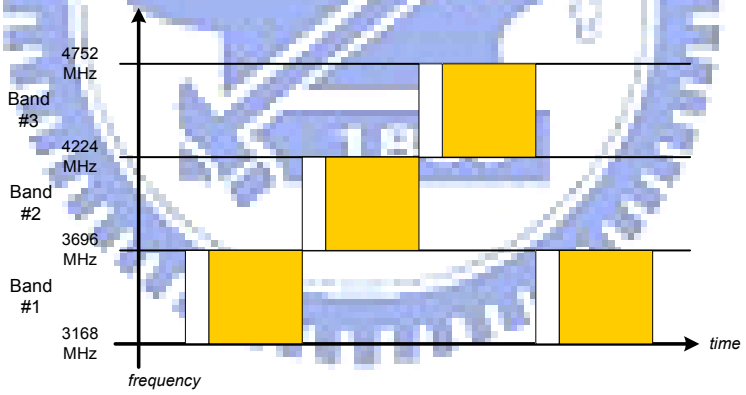


Fig. 2-3. The example of band transitions in a band group

The packet format of the MB-OFDM UWB system is shown in Fig. 2-4. It consists of a preamble, a header, a payload body, and some tail information. The preamble is composed of 30 OFDM symbols (21 for packet synchronization, 3 for frame synchronization, and 6 for channel estimation). The header describes the packet information, including data rate, packet length, initial state, MAC address, etc. The

payload contains the information in the form of OFDM symbols. The signal in the payload may be modulated and transmitted in variable allowable data rate with the length from 0~4095 bytes.

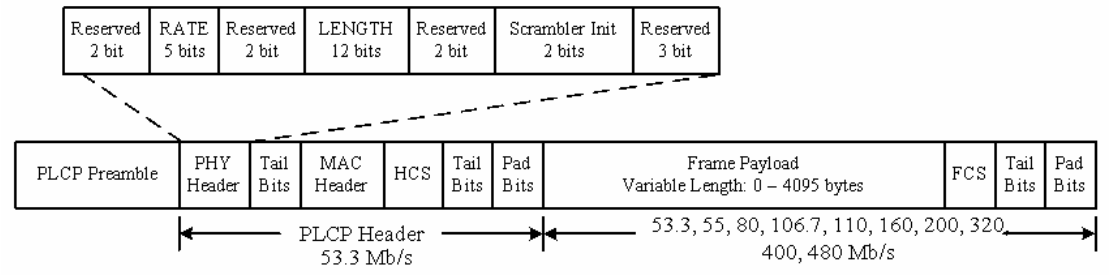


Fig. 2-4. Packet format of MB-OFDM UWB system

Table 2-2 summarizes the time domain information for this system. The subcarrier spacing 4.125MHz is from 528MHz bandwidth divided by 128 subcarriers. So, the IFFT or FFT period is equal to 128 multiplied by per symbol duration (1/528MHz) as 242.42ns. The OFDM zero padded cyclic prefix is composed of 32 samples with 60.61ns, and the guard interval duration for band transition is 9.47ns consisting of 5 samples.

TABLE 2-2. SYSTEM PERAMETER SUMMARY

Parameter	Value
N_{SD}: Number of data subcarriers	100
N_{SDP}: Number of defined pilot carriers	12
N_{SG}: Number of guard carriers	10
N_{ST}: Number of total subcarriers used	122 (= N_{SD} + N_{SDP} + N_{SG})
$\triangle_F$: Subcarrier frequency spacing	4.125 MHz (= 528 MHz/128)
T_{FFT}: IFFT/FFT period	242.42 ns ($1/\triangle_F$)
T_{CP}: Cyclic prefix duration	60.61 ns (= 32/528 MHz)
T_{GI}: Guard interval duration	9.47 ns (= 5/528 MHz)
T_{SYM}: Symbol interval	312.5 ns (T_{CP} + T_{FFT} + T_{GI})

The power requirements for UWB system are provided in Table 2-3. In 90nm and 130nm process, the maximum power in transmission is within 145mW and 180mW, respectively. The receiver side allows a little higher value, say 236mW and 323mW, respectively. The sleep power is also constrained within 20μW.

TABLE 2-3. POWER BUDGET OF PHY LAYER OF IEEE 802.15.3A SYSTEM

Process	Data Rate (Mb/s)	Transmitter	Receiver	CCA (Signal Detect)	Power Save (Deep Sleep Mode)
90 nm	110	93 mW	155 mW	94 mW	15μW
	200	93 mW	169 mW	94 mW	15μW
	480	145 mW	236 mW	94 mW	15μW
130 nm	110	117 mW	205 mW	117 mW	18μW
	200	117 mW	227 mW	117 mW	18μW
	480	180 mW	323 mW	117 mW	18μW

For more information about the MB-OFDM UWB system, a detail discussion of system performance and baseline implementation can be found in [4].

2-2 In-House Protocols (uPHI & WiBoC) in WBAN

2-2-1 Application Scenarios

Wireless body area network (WBAN) has been promoted by IEEE 802.15 working group since 2007 [5]. The goal of the system is to provide a wireless vehicle for human healthcare and medical applications. Before the completeness of the standardization, this work proposes a system with in-house protocols by two versions. One is named as ubiquitous personal healthcare inspector (uPHI) [6], and the other

advanced version is called wireless body-on-a-chip (WiBoC) [3]. The details will be discussed later.

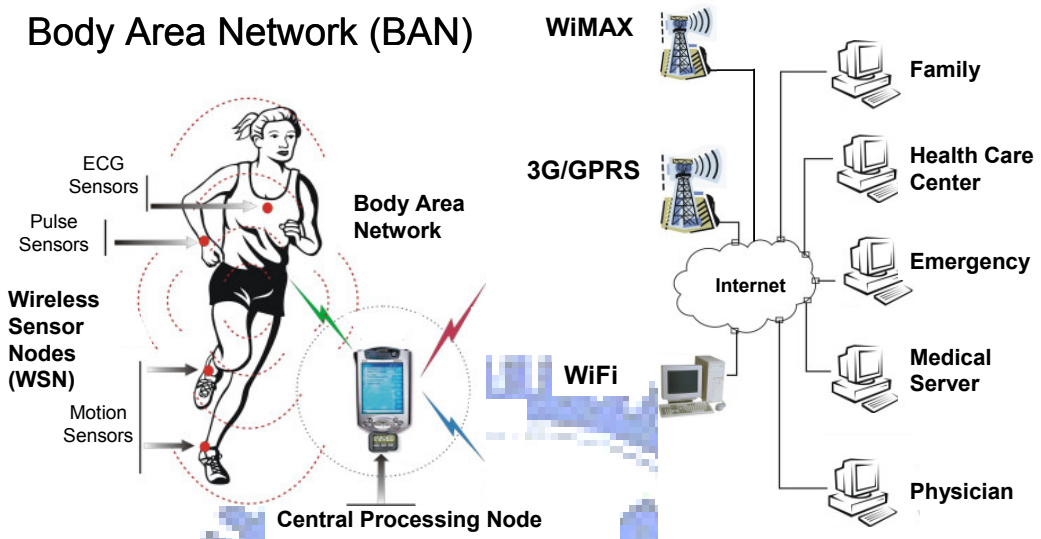


Fig. 2-5. Network in wireless body area network applications

The body information tends to be analyzed and monitored by any remote application centers. Many patients and non-patients can benefit from continuous monitoring as a part of a diagnostic procedure, optimal maintenance of a chronic condition or during supervised recovery from an acute event or surgical procedure, as shown in Fig. 2-5. The WBAN, however, only provides limited short range signal transmission. As a result, it is usually combined with long-distance transmission media, such as WiFi [7], mobile phone network, or WiMAX [8]. Then, those data are sent to any server sides via wired-line internet system. As long as the server side provides corresponding applications, like healthcare, emergency reaction, medical diagnosis, or physician consulting, a ubiquitous monitoring application is then achieved. The infrastructure of those existing wireless systems is quite mature. Consequently, the bottleneck of ubiquitous services becomes the short-range body-around WBAN system.

The healthcare and medical oriented applications are the first targeted application. Any sensors that interact or interface with human body can result in a specific application. The surface measured information includes electroencephalography (EEG), electro-cardiogram (ECG), blood pressure, motion activities, etc. On the other hand in the implanted applications, applications include a hearing-aid device, artificial eyes, brain abnormal detection, blood content measurement, stomach capsule, etc. The wireless device integrated with those kinds of sensors should be designed in an extreme tiny size. Furthermore, the power consumption is limited in micro-watt (μW) level such that any external components like a battery or passive components can be integrated together with the wireless platform.

The WBAN is featured by short range communications, low data rate, and specifically extreme low power consumption that are designed within a highly integrated tiny area, as shown in Fig. 2-6. A readout sensor is usually combined with WBAN systems to provide a human body's physical information. Then the WBAN wirelessly transmits those sensed body signals to a remote device. Body information can be divided into (1) surface-obtained, including electro-cardiogram (ECG), body temperature, motion status, etc., and (2) implanted-measured, including capsule-based stomach monitoring, glucose level, etc.

The raw data rate of body signals ranges from sub-kbps to more than Mbps, depending on the measured signal source [9][10]. In other words, the wireless vehicle is only required to serve wireless transmission in the speed below Mbps. Moreover, a portable or monitoring device usually placed by wireless readout circuit, and the transmission distance becomes as short as several meters or even sub-one-meter. Accordingly, the WBAN emphasizes quite different features than previous consumer

wireless applications. It focuses on tiny size capability, power consumption level, energy source, and any possible human body impacts.

In the target operation scenario, the system allows lots of people coexistence [3][6]. Assume each person may bring his or her own central processing node (CPN) integrated in a portable device, for example, a PDA, a watch, or a notebook. The CPN gathers body signals by wireless sensor nodes (WSNs) attached or implanted in a specific person. Every CPN is capable of receiving signals from a multiple of WSNs. Thus, multiple accesses are also considered. Moreover, the CPN suppresses the mutual interference from other WSNs and out-band interference from unknown devices. As the CPN receives signals from WSNs, it may further transmit those signals to hospital or any kind of media operation centers via existing network, like WiMAX or Wireless LAN. Thus, this results in the expected operation scenario.

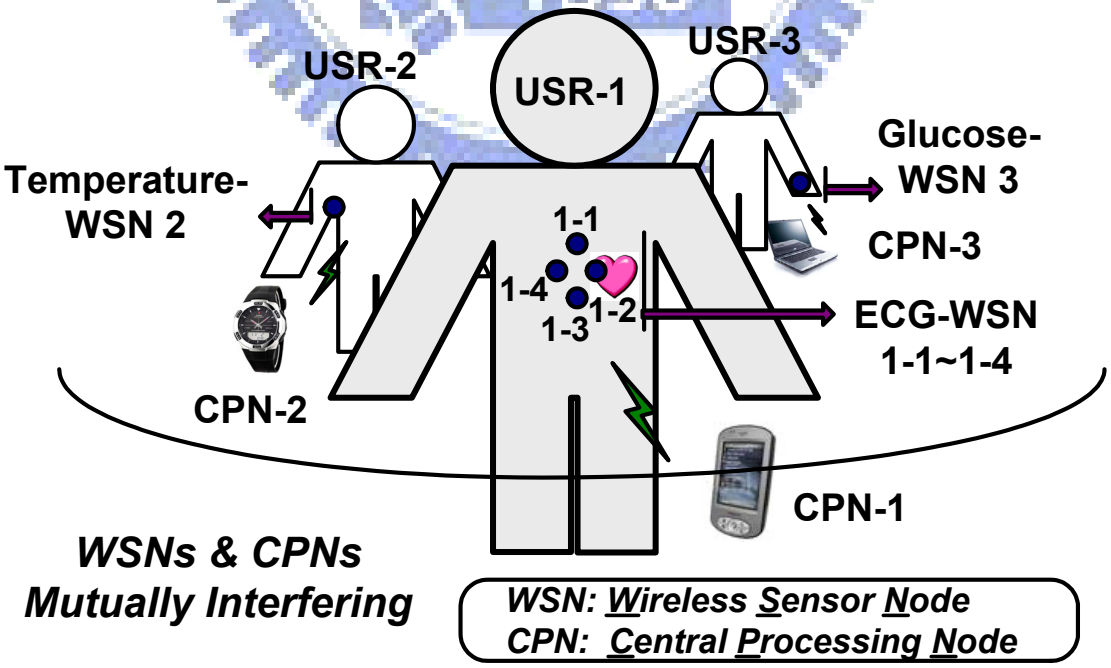


Fig. 2-6. Multiple sensors in coexistence operation scenarios

Beyond the healthcare applications, the WBAN is also designed for possible applications, including fitness monitoring, wearable audio, video stream, remote control, and I/O devices, as shown in Fig. 2-7 [11][12][13]. As long as someone wears a set of transceiver, he/she is able to utilize this device to communicate with the environments. For example, a sensor integrated in a shoe can measure the speed and motion duration of a sportsman. Moreover, it can be further used for place allocation. Consequently, a remote center can trace what places someone passed by, providing total achieved mileage information and route, the total amount of burned calories, the blood pressure and heart beat statistics. Moreover, some possible examples for implanted applications are also illustrated in Fig. 2-8 [14][15].

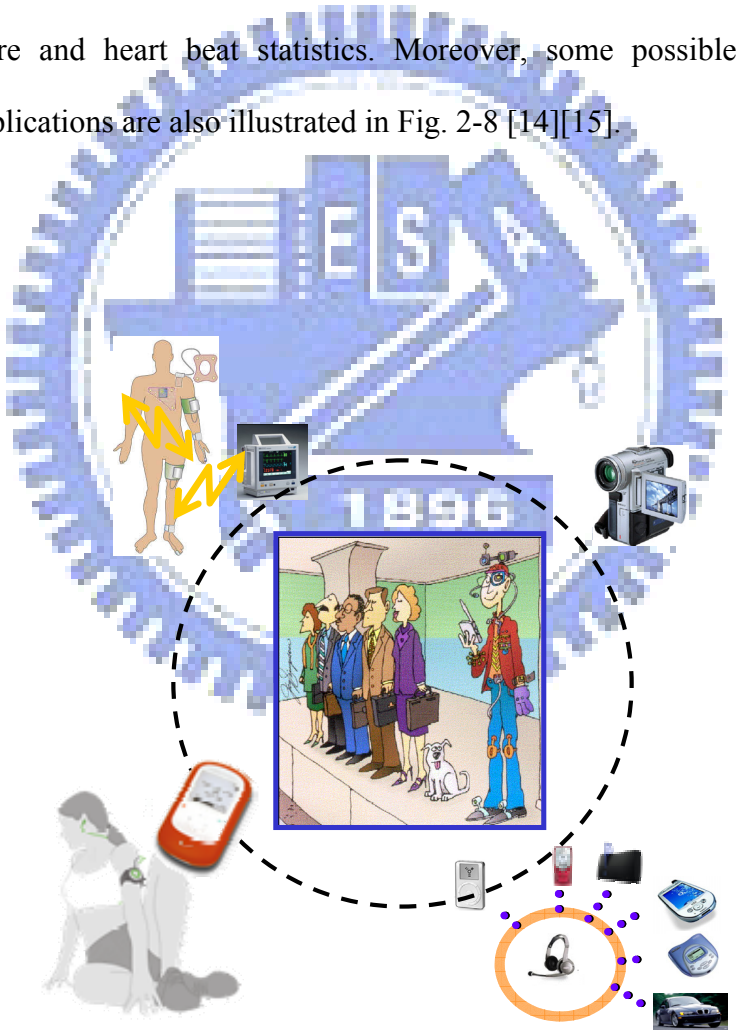


Fig. 2-7. Applications on wearable devices

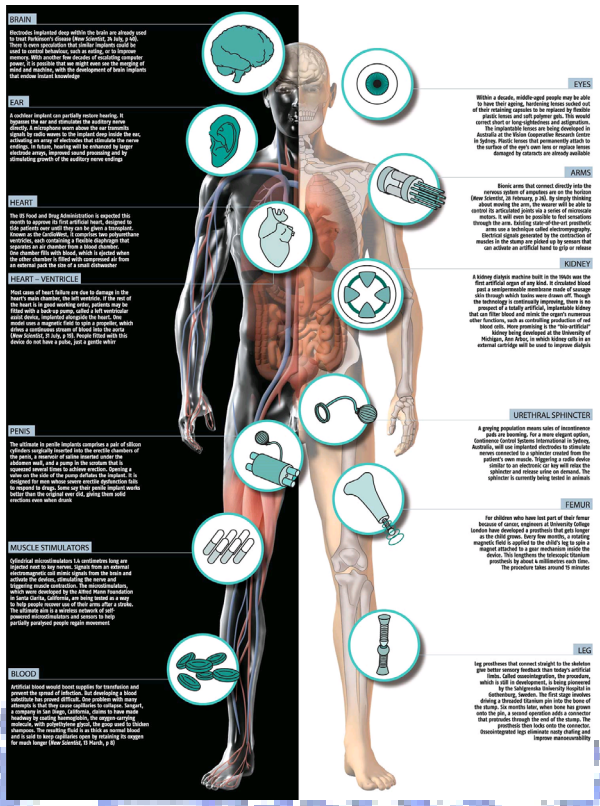


Fig. 2-8. Implanted devices in WBAN applications

2-2-2 WBAN System Design Constraints

The above discussion reveals that WBAN covers a wide range of short distance body-oriented applications. The non-implanted, invasive, or entertainment applications are targeted in this system. Therefore, the WBAN system should be designed with the following considerations:

(1) Physical layer

(2) MAC layer

(3) Network architecture

(4) BAN topography, technology, channel models, and metrics

(5) BAN scalability, bitrate/throughput, range, QoS, power consumption, and power saving supports

(6) Regulatory compliance, spectrum allocation, and coexistence

(7) IPR

(8) Security aspects

(9) Human safety requirements

Moreover, the specification can be categorized and featured by wearable BAN applications and implant BAN systems [16], as shown in Fig. 2-9. First, the operation environment issue is addressed, including the radio frequency band, operation channel modeling, and body safety. The on-the-body WBAN applications should also follow the free-used frequency band, such as the band specialized for industry-science-medical bands, ultra-wideband radio bands, and any other free bands. The channel effects on the wearable systems focus on the multipath effects because someone may move to any unexpected environments like buildings, offices, large plain non-obstruction places, etc. This results in signal transmission paths difficult for prediction. As a result, the wearable devices should be able to overcome the worst possible wireless condition, and the multipath model should be concerned for this category. On the other hand in implant devices, the possible existing radio frequency is defined at 1.4GHz WMTS band [17], MICS band, ISM band, or UWB band. The signal is expected passing through a human body that consists of skin and lots of water. This transmission condition results in the wireless signals mainly destroyed by its magnitude or power. In other words, the main concern of channel model in this case can be claimed as path-loss phenomenon. Beside the radio frequency and channel mode, the common issues for both of the systems are the impacts to a human body, say specific absorption rate (SAR) of microwaves. This is still a non-well-defined factor in this draft WBAN system. The second critical issue is the interference problem. The WBAN should perform high reliable behavior immunized to any sudden interference resulting in malfunction of a wireless device, because

some of the devices are related to life-condition operations. It can not tolerate any electro-problems in life threatening. The interference can be defined as inter-interference and intra-interference. For the inter-interference, it comes from a set of the on-the-body devices or the set of invasive devices. For the intra-interference, a wearable device may interfere with the implanted device or vice versa. Accordingly, the system is designed with the specifications that can tolerate high interference.

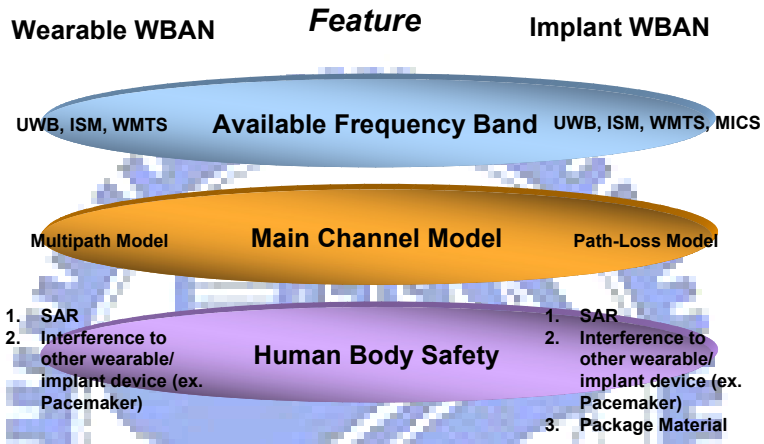


Fig. 2-9. Design features in wearable and implant WBAN links

More specifically in the system requirements, the physical layer is designed following those guidelines:

(1) Operates on, inside, or in the vicinity of the body

(2) Limited range (<.01 ~ 2meters)

(3) The channel model will include human body effects. (absorption, health effects)

(4) Extremely low consumption power (.1 to 1mW) for each device

(5) Capable of energy scavenging /battery-less operation

(6) Support scalable data rate 0.01~1Mbps (opt 10Mbps)

(7) Support different classes of QoS for high reliability, asymmetric traffic, power constrained

(8) Needs optimized, low complexity MAC and networking layer

(9) High number of simultaneously operating piconets required

(10) Applications specific, security/privacy required

(11) Small form factor for the whole radio, antenna, power supply system

(12) Locating radios (“find me”) mode

Table 2-4 illustrates the main difference between the WBAN and other 802 standards [18].

TABLE 2-4. POWER BUDGET OF PHY LAYER OF IEEE 802.15.3A SYSTEM

	Other 802 standards	BAN
Configuration	15.3, 15.4 MAC	Single scalable MAC with reliable delivery
Power consumption	Low power consumption	Extremely low power while communicating to protect human tissue
Power source	Conventional power source	Possible scavenge operation
Requirements (QoS)	Low latency	Guaranteed and reliable response to external stimuli
Frequency band	ISM	Medical authorities approved bands for in and around human body
Channel	Air	Air, vicinity of human body, inside human body
Safety for human body	None	Required (eg. SAR)

2-2-3 uPHI Specifications

According to the design constraints described in part 2-2-2, the uPHI protocol is designed. This protocol only focuses on the physical layer designs that enable this work to highlight the contributions and characteristics in the WBAN applications.

First, the radio frequency band is determined in the band 1.4GHz. This radio frequency is specialized for health and medical uses. Instead of the industry-science-medical (ISM) band, 1.4GHz provides a low-interference environment for higher reliability signal transmission. This prevents the signal interference from the popular commercial wireless communications systems as shown in Fig. 2-10. The detail criterion in designing a circuit in the band can be further referred to [17].

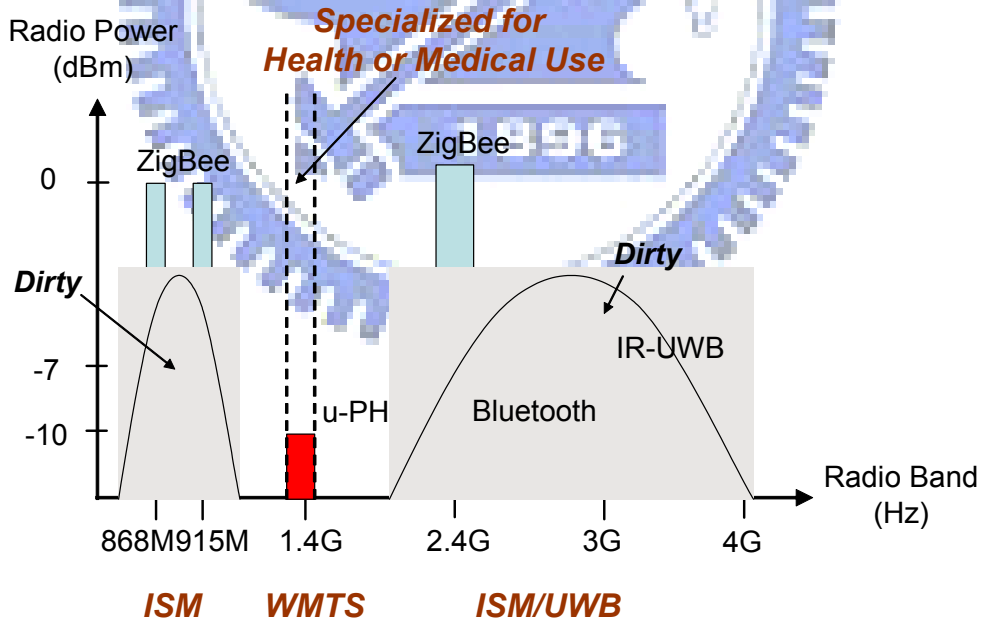


Fig. 2-10. Spectrum distribution and reliability for WMTS, UWB, and ISM bands

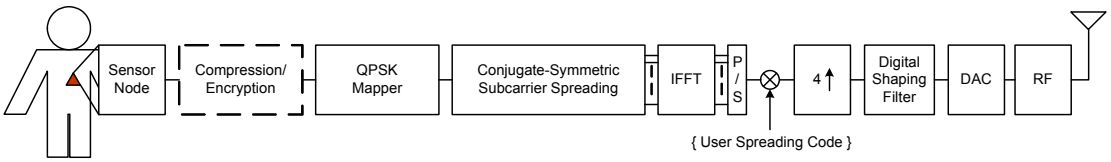


Fig. 2-11. Brief uPHI block diagram in a WSN

The system block diagrams in a transmitter are depicted in Fig. 2-11 that modulates signals according to the multi-tone CDMA (MT-CDMA) scheme [19]. The body signals come from a WSN. Depending on variant application requirements, an optional data compression or encryption could be added in signal processing. For the WBAN applications, it is required to have extreme low power consumption in a transmitter because a transmitter is made as small as possible for wearability, and is usually energy and battery limited. To achieve this goal, a function block of conjugate-symmetric subcarrier spreading is added to reduce the two-path transmission circuits (in-phase and quadrature-phase paths) to a single-path one. For example, assume the input subcarriers to an inverse fast Fourier transformation (IFFT) has the form of

$$S = \{0, d_{N/2+1}, d_{N/2+2}, \ldots, d_1, 0, d_1^*, \ldots, d_{N/2-2}^*, d_{N/2-1}^*\} \tag{2-1}$$

where d is the frequency-domain subcarrier and N is the IFFT block size. So, it is derived that

$$s = IFFT\{S\}_N = \mathrm{Re}\{s\} \tag{2-2}$$

In other words, every input pattern with the form of Eq. (2-1) results in a zero imaginary part of the IFFT output. This equivalently saves one path of DAC and RF circuits, and thus the corresponding power consumption and hardware cost are

reduced. Those subcarriers in set S are duplicated one time, and this is also considered as spectrum spreading with spreading factor two. In a constellation mapper, it modulates signals into QPSK, and a higher order modulation more than 16-QAM is undesired in the system to prevent from the peak-to-average-power ratio (PAPR) problems. Considering the robustness to a fading channel and PAPR problems, a 16-point IFFT is used for OFDM modulation. The guard interval with 1/8 OFDM block size is applied prior to each OFDM symbol. Therefore, the system achieves the equalization ability to a fading channel. This low-order constellation mapper and small block size IFFT reduce the PAPR problem with the aid of digital reduction techniques [20][21] to achieve mild signal distortion and low out-of-band spurious interference. Then the IFFT output is spread by the spreading code and sent to a DAC. Finally, the word-length of DAC circuit decides the computation complexity and system performance. The packet format applied to the uPHI platform is illustrated in Fig. 2-12. In the beginning of a packet, there are ten periodic short preambles concatenated for timing synchronization. In the middle of the packet is the body for frame synchronization. Finally is the payload part carrying the data information.

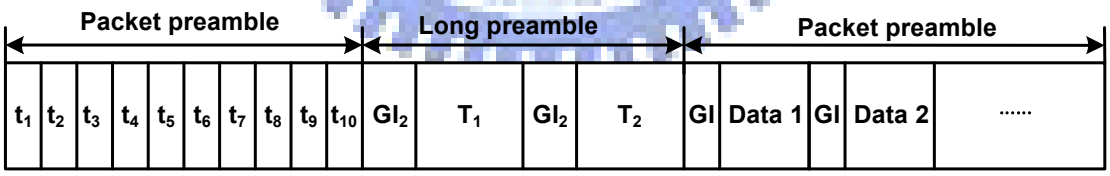


Fig. 2-12. Packet format of the uPHI platform

In the signal power spectrum, WMTS has strict radiation power intensity definition. In the low band, 608-614MHz, the maximum in-band and out-of-band electrical field strength is defined as 200mV/m and 200uV/m, respectively. In the high band, 1395-1400MHz and 1429-1432MHz, the maximum in-band and out-of-band

field strength is 740mV/m and 540uV/m, respectively. Both the high and low band has the field strength measured at a 3-meter distance. As a result, a signal spectrum mask is specified in Fig. 2-13. This equivalently defines the allowable bandwidth for baseband signal transmission, i.e. 3MHz. To meet this spectrum mask design challenge, the digital signals before DAC circuit are upsampled four times and applied to a digital shaping filter to balance the power and design challenges between the RF front-end and baseband circuits. Table 2-5 summarizes the features of the uPHI system, including the channel, modulation, and packet features.

TABLE 2-5. UPHI SYSTEM PARAMETER SUMMARY

Parameter	Features
RF Band	1.4GHz WMTS band
Maximum Data Throughput	86kb/s
User Spreading Code Type	Gold Code
Spreading Code Length	31
Spreading Code Chip Rate	3Mc/s
IFFT/FFT Block Size	16
Guard Interval Duration	20.6 us
Constellation Mapper	QPSK
Coded bits per subcarrier	2
Data bits per OFDM symbol	24

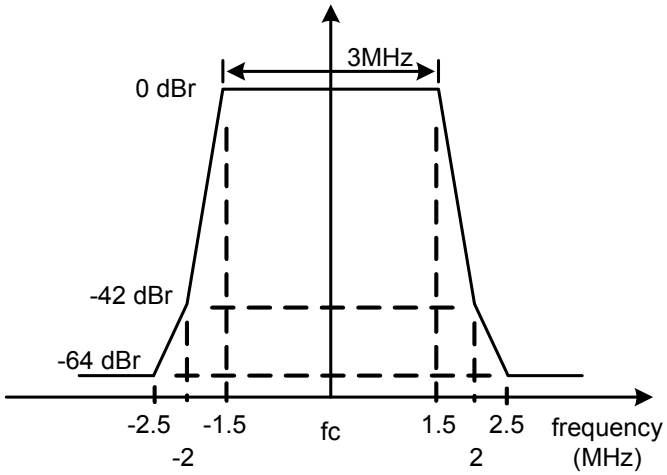


Fig. 2-13. The designed spectrum mask for the WMTS band

2-2-4 WiBoC Specifications

The system behavioral scheme of WiBoC is shown in Fig. 2-14 based on the pure OFDM modulation scheme. Here we depict this operation for multi-user in a view of time axis. The body signals are gathered and transmitted from the WSNs. The CPN, which is integrated in a portable device such as a personal digital assistant (PDA), receives the human body signals from WSNs for ubiquitous monitoring. When the WSNs and CPN is activated, they are initially in a reset state. In the beginning of network establishment, the CPN waits for sign-in signals from possible WSN nodes. After all WSNs join this network, the CPN broadcasts frames to every WSN (downlink process) for timing and frequency synchronizations. After the network synchronization in the downlink process, each WSN starts to gather body signals and transmits to the CPN (uplink process). Finally, the CPN receives the body information from WSNs. The proposed communication system operates in 1.4GHz radio band, and occupies 5MHz bandwidth.

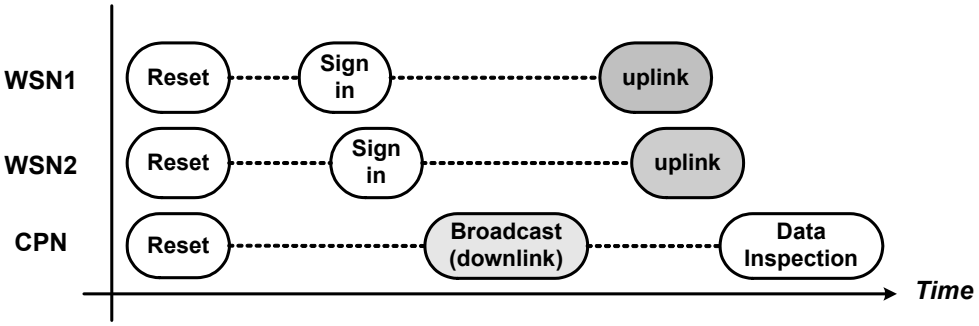


Fig. 2-14. Timing sequence for the WSN and CPN communications

Fig. 2-15 shows the downlink broadcast frame. The first two repeated short preambles are used for the symbol timing synchronization and the coarse CFO estimation. The following two GI are for the boundary detection. The subsequent two long preambles are used to perform channel estimation and further fine CFO estimation. In the end of the frame, concatenated SCO preambles are used to perform SCO estimations.

Uplink frame structure is shown in Fig. 2-16. The preambles and the data are scrambled into a frame. The first GI is composed of the repeated subset of long preambles. It is used to perform symbol timing synchronization and symbol boundary detection. The following two long preambles are used for channel estimation. The signal field indicates the number of OFDM symbols in this frame. The final part of the frame is the payload data. Table 2-6 reveals the WiBoC system features in terms of radio frequency, signals bandwidth, modulations, and frame durations. Note that a convolutional code is applied in this version to verify the coded performance in the WBAN applications. This convolutional code applies a generator polynomial (133,171) [7].

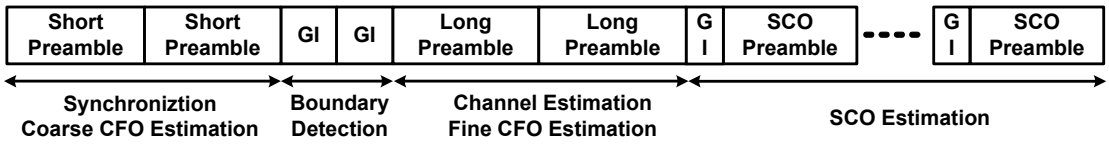


Fig. 2-15. Frame format for the downlink transmission

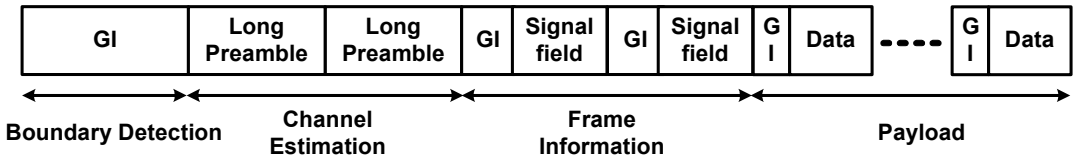


Fig. 2-16. Frame format for the uplink transmission

TABLE 2-6. WIBOC SYSTEM PARAMETER SUMMARY

Parameter	Feature
RF band	1.4GHz WMTS band
Spectrum Bandwidth	5MHz
Constellation Mapper	QPSK
IFFT/FFT Block Size	64
Maximum Data Throughput	4.85 Mbps
Guard Interval Duration	0.4 μs
Data Bit per OFDM symbols	48
FEC Encoder	K=7 Convolutional Code with Generator Polynomial (133,171)

Table 2-7 compares the difference between the uPHI and WiBoC platforms. The designed RF spectrum and available signal bandwidth is the same. Both of them utilize QPSK modulation. The uPHI applies the MT-CDMA scheme with 31-length spreading Gold code whereas the WiBoC uses the pure OFDM modulation. The maximum data rates are 143kb/s and 4.85Mb/s, respectively. This dual modem system can perform both of the high interference toleration and high data rate requirements,

satisfying the possible applications in both high rate wearable devices and interference-rejection low rate implanted requirements.

TABLE 2-7. UPHI AND WIBOC SYSTEM PARAMETER SUMMARY

	uPHI	WiBoC
RF Band	1395~1400MHz	1395~1400MHz
Spectrum BW	5M	5M
Constellation Mapper	MT-CDMA	OFDM
Constellation Mapper	QPSK	QPSK
Spreading Code Chip Rate	3Mc/s	Non-used
IFFT/FFT Block Size	16	64
Maximum Data Rate	143kb/s	4.85Mb/s
User Spreading Code Type	Gold Code	Non-used
Spreading Code Length	31	Non-used
Duration of signal symbol	185.81 μs	13.2 μs
Guard Interval Duration	20.6 μs	0.4 μs
Data bits per OFDM symbol	12x2=24	24 x2=48

The development of the WBAN applications can be illustrated in Fig. 2-17. It can be traced back to the year 2005. A project launched by IMEC was defined as Human++ [22]. At the same time, the MAGNET [23] from European was also devoted in this system. Later in the year 2006, the IEEE 802.15 started the interest and study group [24] for the market and technical survey on the potential WBAN applications. In the same year, Japan proceeded the ubiquitous-Japan project [25] as the domestic infrastructure construction. Moreover, the alliance Continua [26] from

USA also joined the development of WBAN applications. In the year 2007, Nokia proposed a commercial product Wibree [27] for both the short range communications and WBAN applications.

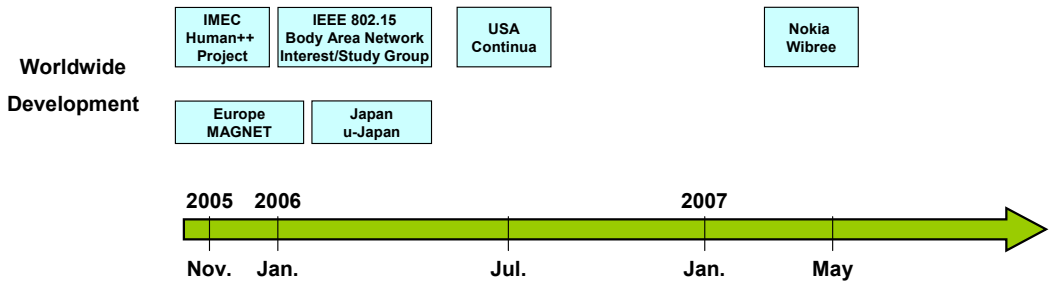


Fig. 2-17. Worldwide development in WBAN systems

For those working groups devoting the development of WBANs, it can be found in the Bluetooth alliance, body sensor network (BSN), and Imperial College in UK. The publications focus on this domain also can be found in the BioCAS and TBCAS from IEEE. For further WBAN authentications, some institutes can be found in Fig. 2-18.

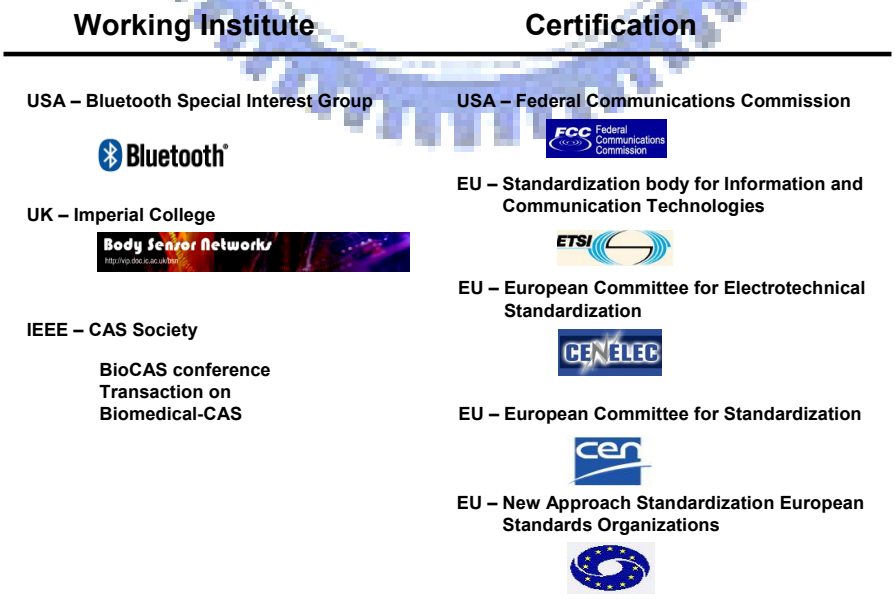


Fig. 2-18. Active working groups toward the WBAN applications

Chapter 3:

I/Q-Mismatch Calibration

3-1 Background and Overview

Radio-frequency (RF) circuits are utilized to up- and down-covert baseband signals between a transmission radio frequency and a baseband frequency. In realistic hardware circuits, this conversion processes introduce I/Q imbalances in terms of gain errors and phase errors, resulting in unwanted-image and desired-signal blending in decoded signals. Un-calibrated or free-designed RF circuits may perform up to 1dB gain error and 10 phase error that destroy correct signal decoding. Most of existing design approaches solves this problem by analog approaches that require circuit overdesign, large device area for reduce mismatch, and design experience. Even the most carefully design cannot prevent the imbalance from the non-ideal circuit implementation, manufacturing, board-level design, etc, resulting in remaining unsolved mismatch and degraded system performance.

Accordingly, this chapter describes an all-digital front-end calibration scheme, I/Q-mismatch calibration. This digitally-assisted signal calibration releases design efforts in the RF front-end analog circuit designs, especially in the systems with the OFDM modulation. This calibration is achieved by the digital-signal process techniques so that any remaining or imbalanced distortion during signal down conversion process can be computationally eliminated, improving the overall system performance and easing the system matching efforts. The role of this digitally RF calibration is introduced as shown in Fig. 3-1.

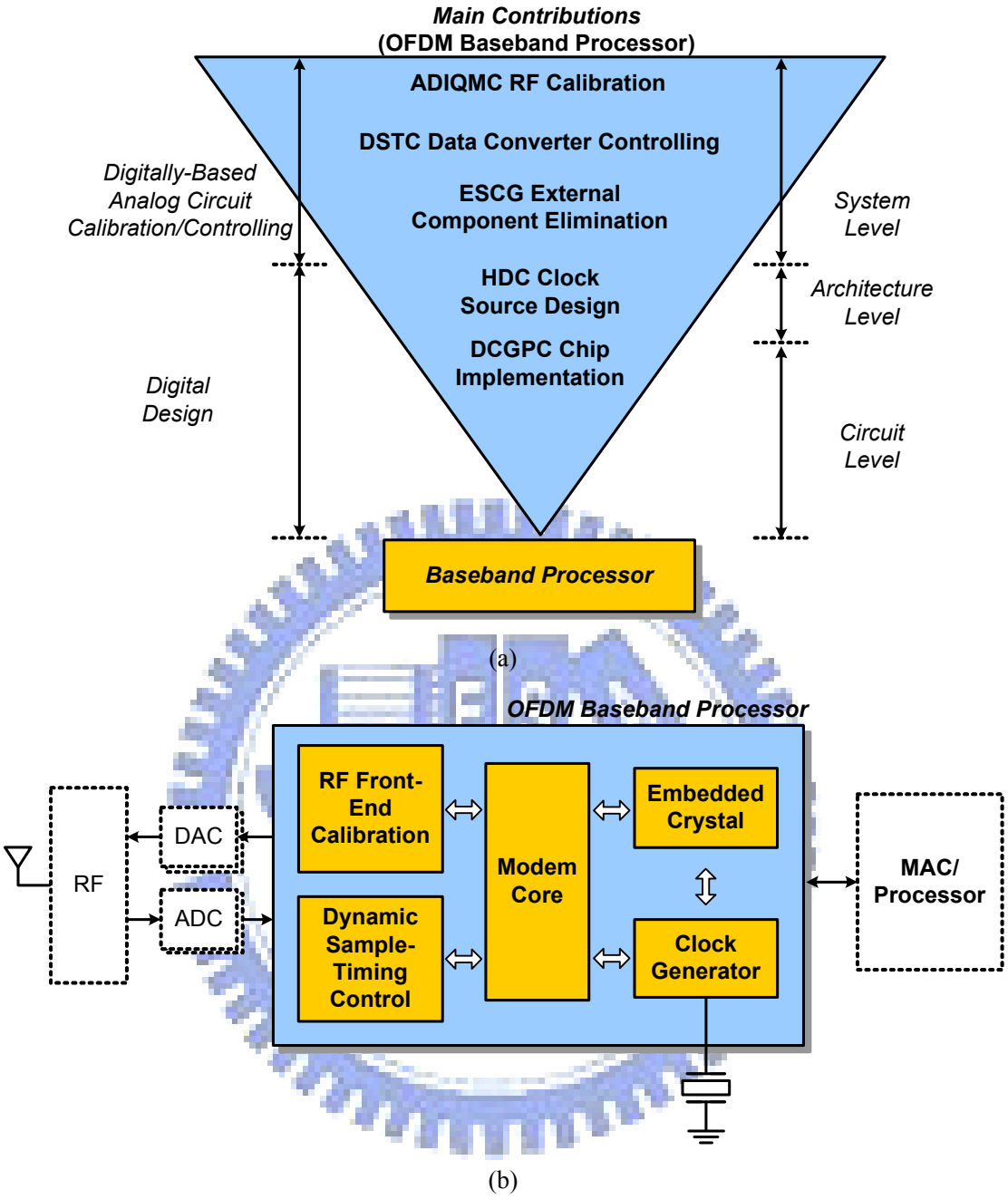


Fig. 3-1. The role of the digitally RF front-end calibration in the power and data proximity scheme

Orthogonal Frequency Division Multiplexing (OFDM) [28][29] is an effective and spectrally efficient signaling technique for wireless communications over frequency selective fading channels. Unfortunately, OFDM is sensitive to non-ideal front-end effect and non-perfect synchronization such as residual carrier frequency

offset (CFO), clock timing drift (CTD), symbol timing misalignment (STM), etc., leading to serious system performance degradation. It also demands severe front-end specifications, and results in an expensive front-end circuit in terms of design complexity and development period. There exist mature approaches in parameter estimation and compensation [30]. However, those algorithms become unstable or invalid when the non-ideal RF effect, I/Q mismatch (IQM), is involved. This problem is due to gain and phase mismatch between in-phase (I) and quadrature-phase (Q) paths in RF circuits. IQM is especially obvious as the transceiver in OFDM system uses the direct-conversion architecture because of design complexity and hardware cost [31][36].

To be more specifically, IQM occurs when the RF mixers in I and Q channels have different power gain, and the generated waveforms do not possess exact 90 degree phase difference. Usually, IQM effect is ignored by designers in system simulation level since the mismatch phenomenon does not appear until RF circuit is manufactured. In other words, IQM arises when the circuit size cannot be made exactly as the expected size in manufacturing process, and the behavior does not meet simulation conditions due to process, voltage, and temperature (PVT) variations.

As a result, the IQM correction capability plays an important role especially in high speed wireless communication since the error tolerance becomes much smaller as modulation order gets higher. Such systems, for example, can be found in [28][37] with 64QAM and 256QAM. Likewise, the broadband RF circuit will inevitably suffer from more challenge in designing accurate I/Q balanced signal paths, and consequently emphasize the importance of IQM correction capability.

Among existing IQM correction techniques, some are proposed to combat IQM under Rayleigh fading channel with gain and phase errors within 0.414dB and 10 degree respectively [32]. This gain error tolerance 0.414dB is not large enough as suggested 1dB in [35], and the non-adaptive estimation accuracy is not adequate due to limited samples for calculation. On the other hand, the CFO effect will largely degrade IQM estimation, thus the algorithm has to be modified in accordance with joint IQM and CFO phenomenon [33]. Although both CFO and IQM are jointly considered, the tolerated CFO range under IQM effect is only 5% OFDM subcarrier frequency spacing, which is far from the general requirement 38.4% or ± 25 ppm at carrier frequency 2.4GHz [28]. In addition, some designs apply FIR filters for signal correction [34]. This uses the matrix computation and minimum cost function search, resulting in higher cost and computation complexity as the number of filter coefficient increases.

The IQM problems can be modeled as narrowband [40] or wideband [34][42] scenarios depending on the concerned signal bandwidth. In the narrowband modeling, gain and phase errors are considered as a constant. With this assumption [40] presents a theoretical analysis on the mismatch problem. Also, adaptive compensation schemes are exploited in the literatures with post-FFT approach [39] and pre/post-FFT approach [43]. Considering joint IQM and DC offset problems, a data-aided calibration approach can be found in [41]. Under the narrowband assumption, the channel frequency response is considered as quasi-continuous in consecutive subcarriers, [32] estimates the gain and phase errors based on the smooth-channel property.

In wideband IQM problems, gain and phase errors vary with spectrum frequency, i.e. a non-constant (frequency selective) gain and phase errors in the concerned signal band. Therefore, [42] exploits IQM effects from different filter responses with a two-tone calibration technique. [34] takes IQM estimation in time domain in a NLS adaptive manner. The IQM calibration in a chip implementation can be found in [38].

Considering system performance, error tolerance, computation cost, and robustness to channel complexity, we propose an all digital hybrid-domain filterless adaptive compensation (HD-FAC) technique. It calculates the error function in frequency domain and adaptively updates the single coefficient for signal compensation in time domain without using any delayed-line filters. Moreover, HD-FAC is able to estimate and compensate IQM under Rayleigh fading channel and CFO effect with gain error 1dB and phase error 10 degree as suggested in [35]. Also, the Rayleigh fading channel has the statistics of RMS 50ns, and CFO tolerance is 38.4% subcarrier frequency spacing or ± 25 ppm at 2.4GHz carrier frequency, which satisfies the specification [28].

3-2 I/Q-Mismatch Modeling

A general form of IQM model in a direct conversion receiver is shown in Fig. 3-2. This provides a universal modeling for both the frequency-independent and frequency-selective IQM scenario. The frequency independent gain error ε and phase error φ are multiplied to incoming signals from the antenna.

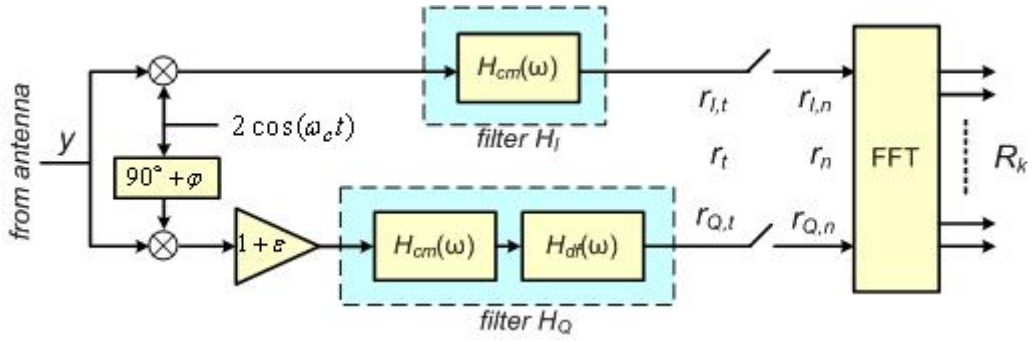


Fig. 3-2. OFDM receiver with frequency-selective IQM

Those circuit components through a RF down-conversion process, including mixers, amplifiers, low-pass filters, and A/D converters, in general contribute frequency-selective mismatches, which are modeled as equivalent filters H_I and H_Q in I and Q paths, respectively. This pair of filters may perform different responses so that the filters can be further factorized as a common response $H_{cm}(\omega)$ and a differential response $H_{df}(\omega)$. Assume the response of the in-phase path is defined as the common response $H_{cm}(\omega)$, then the in-phase and quadrature-phase responses can be characterized as

$$\begin{cases} H_I(\omega) = H_{cm}(\omega) \\ H_Q(\omega) = H_{cm}(\omega) \cdot H_{df}(\omega) \end{cases} \tag{3-1}$$

Assume the impulse responses of these two filters are real, then the response of the transfer function in positive and negative frequencies is symmetric in its conjugate. Thus, we have the dual property

$$\textit{Dual Property I}: \quad \begin{cases} H_{cm}(\omega) = H_{cm}^{*}(-\omega) \\ H_{df}(\omega) = H_{df}^{*}(-\omega) \end{cases} \tag{3-2}$$

Signal from transmitter side, y, may be expressed as

$$y = A\cos(\omega \cdot t + \theta) - B\sin(\omega \cdot t + \theta) \tag{3-3}$$

where $A+jB$ is the baseband digit denoting the compound form in I and Q branches respectively. Assume that the RF circuits in RX is of coherent demodulation in the upper branch as depicted in Fig. 3-2, thus the down-converted information then becomes

$$\begin{aligned} r &= IFFT\{I_{BB} \cdot H_I + jQ_{BB} \cdot H_Q\} \\ &= IFFT\{A \cdot H_I + j[(1-\varepsilon)\sin(\varphi) \cdot A + (1-\varepsilon)\cos(\varphi) \cdot B] \cdot H_Q\} \end{aligned} \tag{3-4}$$

where I_{BB} and Q_{BB} are the received baseband data in I and Q channel respectively. Also, (3-4) can be further summarized as

$$r = \alpha \cdot y * h_I(t) + \beta \cdot (y)^* * h_Q(t) \tag{3-5}$$

where the $h_I(t)$ and $h_Q(t)$ denotes the I and Q paths impulse responses of H_I and H_Q, respectively. The parameters are defined as signal gain (SG) and image gain (IG), respectively.

$$\begin{aligned} SG &: \alpha = 0.5 * [1 + (1+\varepsilon)e^{-j\varphi}] \\ IG &: \beta = 0.5 * [1 - (1+\varepsilon)e^{j\varphi}] \end{aligned} \tag{3-6}$$

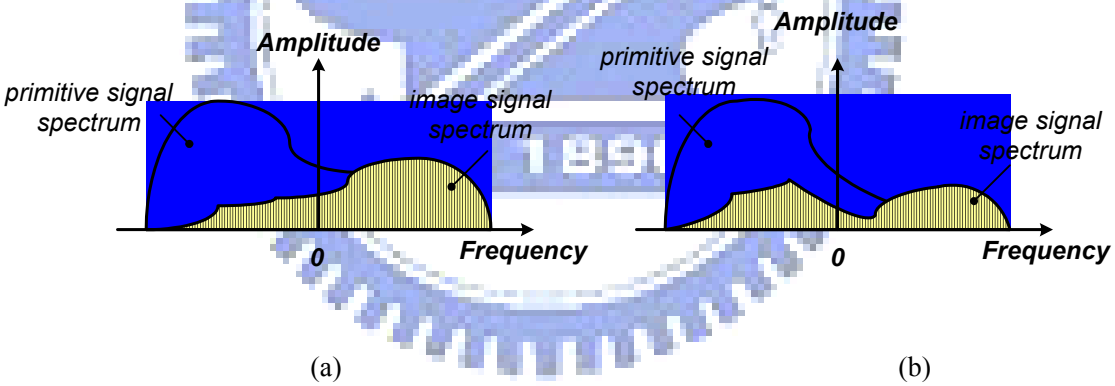
The IQM modeling equation can be extended to a frequency-selective basis that means the gain and phase errors are variant and dependent on the frequency located. Therefore, the received signal y with frequency-selective distortion is expressed as [34]

$$\begin{aligned} r &= IFFT\{R_k\} \\ &= IFFT\{\alpha_k \cdot Y_k \cdot H_{cm,k} + \beta_k \cdot Y_{-k}^* \cdot H_{cm,k}\} \end{aligned} \tag{3-7}$$

that α_k and β_k describe the equivalent gain and phase errors on a frequency basis. The frequency is expressed by the variable *k* in digital domain. The SG and IG can be further described by

$$\begin{aligned} SG: \alpha_k &= 0.5*[1+(1+\varepsilon)e^{-j\varphi}\cdot H_{df,k}] \\ IG: \beta_k &= 0.5*[1-(1+\varepsilon)e^{j\varphi}\cdot H_{df,k}] \end{aligned} \tag{3-8}$$

It is found $H_{df,k}$ is the key factor that causes the SG and IG varying with frequency. Fig. 3-3 shows an example of IQM-distorted signals in frequency domain. The received subcarriers are composed of primitive signals with the signal gain ($\alpha_k \cdot Y_k$) and image interferences with image gain ($\beta_k \cdot Y_{-k}^*$). If the distortion gain is frequency dependent, both of the primitive signals and the image interferences are frequency-selective distorted due to the differential factor $H_{df,k}$.



(a) (b)

Fig. 3-3. IQM distorted signals with (a) constant gain and phase errors (signal and image gains) (b) frequency-selective gain and phase errors (signal and image gains).

The IQM parameters in a narrow-band scenario degenerate to constant values. The common gain $H_{cm}(\omega)$ becomes a constant gain so that it is compensated by the automatic gain control (AGC) loop in the synchronization procedure. In other words, $H_{cm}(\omega)$ can be ignored in this narrow-band condition. The differential gain $H_{df}(\omega)$,

also a constant value, is merged into the gain error , and is not separately discussed. Moreover, the gain (ε) and phase (φ) errors become independent of frequency distribution. The signal gain (α) and mirror gain (β) in (3-8) are also independent of the frequency index k. As a result, signals with IQM distortion are reformulated as

$$\begin{aligned} r &= IFFT\{R_k\} \\ &= IFFT\{\alpha \cdot Y_k + \beta \cdot Y_{-k}^*\} \\ &= \alpha \cdot y + \beta \cdot y^* \end{aligned} \tag{3-9}$$

and

$$\begin{aligned} SG &: \alpha = 0.5 * [1 + (1+\varepsilon)e^{-j\varphi}] \\ IG &: \beta = 0.5 * [1 - (1+\varepsilon)e^{j\varphi}] \end{aligned} \tag{3-10}$$

3-3 I/Q-Mismatch Compensation

Although OFDM is robust to multipath fading channel, the IQM, however, cannot be eliminated by the simple equalization scheme which is used to combat the multipath effects. To see why it is, we return to (3-7) for examining the primitive received signal model in frequency domain. If there are no gain/phase errors in RF circuits, MG is reduced to zero and SG becomes unit. Then the channel estimation and signal equalization can be through conventional methods. As can be seen in, however, the estimated channel response goes far from the correct one as IQM gets severe. Therefore, the signal compensated straightforwardly by the estimated channel becomes

$$\begin{aligned} X_k' &= \frac{R_{BB,k}}{\hat{H}_k} \\ &= \frac{\alpha \cdot Y_k + \beta \cdot Y_{-k}^*}{\alpha \cdot H_k + \beta \cdot \frac{X_{-k,N}^*}{X_k} \cdot H_{-k}^*} \end{aligned} \tag{3-11}$$

It is obviously that $X_k^{'}$ cannot be identical to the original transmitted signal even if the channel is clean. In other words, OFDM equalization works only when Corollary 1 is satisfied, but it turns out to be impossible if IQM exists.

Corollary 1

Conventional OFDM equalization only works when the subcarrier does not mutually interfered by the one elsewhere.

To see the physical meaning, we go through two special cases, one exists only gain error and the other phase error only. For the first one, the signal in passband is down-converted by an in-phase and quadrature-phase bases with exact 90 degree difference in their phases and mismatch gain response. This results in a distorted baseband signal and can be represented by a linear combination of the original transmitted signal and its conjugate one. Due to the existence of conjugate part, the transformed frequency response is equivalent to the subcarrier from the mirror position in the spectrum, and therefore a contradiction of Corollary 1. In the second case of phase error only, the down-converted baseband signal in either I or Q branch will contain an interference from the cross part, i.e., the received real part signal contains the information from both real and imaginary part in transmitted one, and vice versa. Then it is certainly a combination of conjugate and original ones, too. Therefore, results in the same conclusion as in the first case. To summarize the effects, we can regard the signal suffering from a phase rotation and gain attenuation in the view of constellation.

The IQM compensation could be done in either time domain or frequency domain. Before the IQM-error estimation is discussed, the compensation approach is

disclosure first so that the gain and phase errors can be investigated from the compensation signal which has remaining errors in it.

3-3-1 Time-domain compensation

Time-domain compensation scheme is used for frequency-independent IQM scenario. As the IQM-distorted signal is received, the IQM distortion is first compensated in time domain. According to (3-5), the received signal can be modeled in a matrix form as

$$\begin{aligned} r &= \alpha \cdot x + \beta \cdot x^* \\ &= \begin{bmatrix} (\alpha_R + \beta_R) & -(\alpha_I - \beta_I) \\ (\alpha_I + \beta_I) & (\alpha_R - \beta_R) \end{bmatrix} \cdot \begin{bmatrix} x_R \\ x_I \end{bmatrix} \\ &= M \cdot x \end{aligned} \tag{3-12}$$

where $\alpha = \alpha_R + j\alpha_I$ and $\beta = \beta_R + j\beta_I$. By taking the matrix inverse of (3-12), the corrected signal may be formulated as

$$\begin{aligned} M^{-1} \cdot r &= \frac{1}{\det(M)} \begin{bmatrix} (\alpha_R - \beta_R) & (\alpha_I - \beta_I) \\ -(\alpha_I + \beta_I) & (\alpha_R + \beta_R) \end{bmatrix} \cdot \begin{bmatrix} r_R \\ r_I \end{bmatrix} \\ &= \frac{1}{\det(M)} \left(\begin{bmatrix} \alpha_R & \alpha_I \\ -\alpha_I & \alpha_R \end{bmatrix} \cdot \begin{bmatrix} r_R \\ r_I \end{bmatrix} - \begin{bmatrix} \beta_R & \beta_I \\ \beta_I & -\beta_R \end{bmatrix} \cdot \begin{bmatrix} r_R \\ r_I \end{bmatrix} \right) \\ &= \frac{\alpha^* \cdot r_{BB} - \beta \cdot r_{BB}^*}{|\alpha|^2 - |\beta|^2} \end{aligned} \tag{3-13}$$

As a result, the signal compensation can be achieved by (3-14), and this is used for time-domain IQM signal calibration.

$$y_c = \frac{\alpha^* \cdot r - \beta \cdot r^*}{|\alpha|^2 - |\beta|^2} \tag{3-14}$$

3-3-2 Frequency-domain compensation

IQM-distorted signals in frequency domain is expressed as

$$R_k = \alpha_k \cdot Y_k \cdot H_{cm,k} + \beta_k \cdot Y_{-k}^* \cdot H_{cm,k} \tag{3-15}$$

where footnote k denotes the discrete frequency index. As a result, the compensation is achieved by

$$\begin{aligned} Y_k &= \frac{\alpha_{-k}^* R_k - \beta_k R_{-k}^*}{\alpha_k \alpha_{-k}^* - \beta_k \beta_{-k}^*} \\ &= \frac{\alpha_{-k}^* (\alpha_k Y_k H_{cm,k} + \beta_k Y_{-k}^* H_{cm,k}) - \beta_k (\alpha_{-k}^* Y_{-k}^* H_{cm,-k}^* + \beta_{-k}^* Y_k H_{cm,-k}^*)}{\alpha_k \alpha_{-k}^* - \beta_k \beta_{-k}^*} \end{aligned} \tag{3-16}$$

Comparing this frequency-selective compensation equation with the frequency-independent one, it is found that the frequency-independent IQM scenario has constants α_k, β_k, and $H_{cm,k}$. Consequently, this compensation formulation degenerates to the time-domain expression when replacing constant SG, IG, and common filter responses into the frequency-selective IQM calibration scheme. In other words, this frequency-selective based signal expression can be regarded as a general form for the IQM problem modeling.

3-4 IQM Parameter Estimations

3-4-1 Narrow-band adaptive estimation

The IQM calibration is achieved via the estimations of signal gain and mirror gain. Instead of directly estimation SG and IG, the estimation errors are computed first to update the SG and IG parameters that are used for the signal calibration. If the signal is transmitted via a physical channel, there is inevitably noise added to the

information signals, resulting in the error-estimation of essential parameters for the IQM calibration. Accordingly, the estimation error is defined for the SG and IG parameters as *delta-SG (dSG)* and *delta-MG (dMG)*.

$$\begin{aligned} dSG &: \Delta_\alpha = \alpha - \hat{\alpha} \\ dMG &: \Delta_\beta = \beta - \hat{\beta} \end{aligned} \tag{3-17}$$

where the hat notation denotes a parameter that comes from estimations. The IQM-distorted signal compensated by the estimated SG and IG can be expressed as

$$\hat{y}_c = \frac{\hat{\alpha}^* \cdot r - \hat{\beta} \cdot r^*}{|\hat{\alpha}|^2 - |\hat{\beta}|^2} \tag{3-18}$$

Therefore, there is absolutely an error amount between y_c and $\hat{y}_c$ due to non-ideal signal compensation. In order to represent the compensated signal as a function of error terms, (3-17) is substituted into $\hat{y}_c$, and we have

$$\hat{y}_c = \hat{K} \cdot [\hat{\alpha}^* (\Delta_\alpha + \hat{\alpha}) \cdot y_c + \hat{\alpha}^* \cdot \beta \cdot y_c^* - \hat{\beta} \cdot \alpha^* \cdot y_c^* - \hat{\beta} \cdot (\Delta_\beta + \hat{\beta})^* \cdot y_c] \tag{3-19}$$

where $\hat{K} = \frac{1}{|\hat{\alpha}|^2 - |\hat{\beta}|^2}$. According to (3-10), we find out the property

$$\alpha = 1 - \beta^* \quad \text{and} \quad \hat{\alpha} = 1 - \hat{\beta}^* \tag{3-20}$$

This is further inferred that $\Delta_\alpha = -\Delta_\beta^*$ from (3-17) and (3-20). As a result, (3-13) can be summarized as

$$\hat{y}_c = y_c - (\Delta_\beta^* \cdot y_c - \Delta_\beta \cdot y_c^*) \cdot \hat{K} \tag{3-21}$$

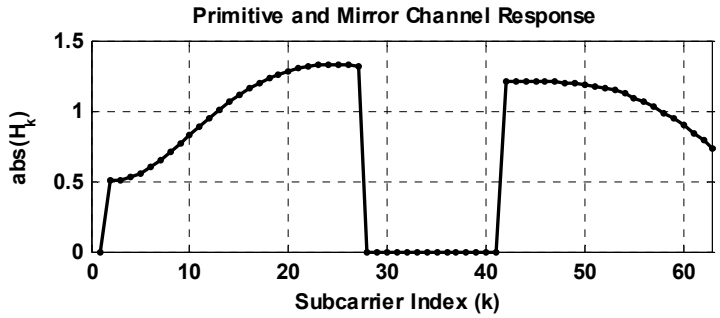
Prior to SG and MG estimation, the incoming signals should be left uncompensated. This is equivalent to set parameters as $\hat{\alpha}=1$ and $\hat{\beta}=0$, i.e. $\beta=\Delta_\beta$. Therefore, our problem becomes how to estimate the *dMG* parameter Δ_β. After the CFO compensation of $\hat{y}_c$ with $e^{-j\omega\cdot t}$, we have

$$\hat{y}=y-(\Delta_\beta^*\cdot y-\Delta_\beta\cdot y^*\cdot e^{-j2\omega\cdot t})\cdot\hat{K} \tag{3-22}$$

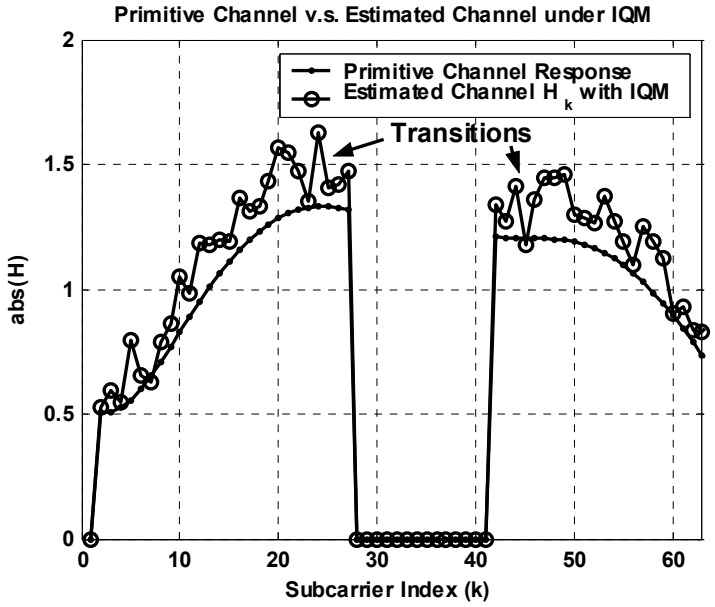
If the received signal belongs to preamble, it will be used for channel estimation. Then (3-22) is transformed into frequency domain and divided by the pre-defined preamble. The estimated channel may be expressed as

$$\hat{H}_k=\frac{\hat{Y}_k}{X_k}=(1-\Delta_\beta^*\cdot\hat{K})\cdot H_k+(\Delta_\beta\cdot\frac{X_{-k,N}}{X_k}\cdot D_{-2\varepsilon}\cdot\hat{K})\cdot H_{-k,N}^* \tag{3-23}$$

with $X_k\in\{+1,-1\}$. This result is composed of two product terms. The first product term shows that the primitive channel response is multiplied by a complex gain, and the second product term can be regarded as interference since the channel response comes from the mirror part and the variables in the bracket are all non-ideal effects. On the other hand, the ratio $X_{-k,N}/X_k$ may be positive or negative depending on the values defined in preamble. Therefore, this ratio decides if the second product term is added or deducted by the first product term, resulting in large value transitions in estimated channel responses on specific subcarrier indices. These transitions are due to IQM effect and can be seen in Fig. 3-4.



(a)



(b)

Fig. 3-4. Channel response with IQM effect (a) primitive channel response and the mirror response (b) estimated channel response under gain error 1 dB and phase 10 degree.

If gain error or phase error becomes more severe, the amplitude transitions in the consecutive channel responses will get larger. Therefore, we can extract Δ_β from those transitions of estimated channel responses. From (3-23), we consider two

consecutive subcarriers with large transitions, i.e. $X_{-k,N}/X_k$ and $X_{-k-1,N}/X_{k+1}$ have opposite signs with subcarrier indices k and $k+1$ respectively. Then the difference between the estimated channel responses becomes

$$\hat{H}_k - \hat{H}_{k+1} = (1 - \Delta_\delta^* \hat{K})(H_k - H_{k+1}) + (\Delta_\delta D_{-2\varepsilon} \hat{K})(\frac{X_{-k}}{X_k} H_{-k}^* - \frac{X_{-k-1}}{X_{k+1}} H_{-k-1}^*) \quad (3\text{-}24)$$

where the block size N is omitted for notation simplicity. We assume our operating environment has slow varying frequency response, so the consecutive channel subcarriers are approximately equal, i.e. $H_k - H_{k+1} \approx 0$. So, the first product term in (3-24) can be eliminated. On the other hand, $\frac{X_{-k}}{X_k} H_{-k}^*$ in the second product term can be derived by replacing index k with $-k$ in (3-23), then we have

$$\frac{X_{-k}}{X_k} H_{-k}^* = \left[\frac{X_{-k}}{X_k} \hat{H}_{-k}^* - (\Delta_\delta^* D_{-2\varepsilon}^* \hat{K}) H_k \right] \Big/ (1 - \Delta_\delta \hat{K}) \quad (3\text{-}25)$$

$\frac{X_{-k-1}}{X_{k+1}} H_{-k-1}^*$ can be derived in a similar way by replacing k with -k-1 in (3-23). Then substitute these two terms into (3-24), eliminate the product term associated with $(-H_k + H_{k+1})$, and it becomes

$$\Delta_\beta = \frac{(\hat{H}_k - \hat{H}_{k+1}) \cdot (|\hat{\alpha}|^2 - |\hat{\beta}|^2)}{(\hat{H}_k - \hat{H}_{k+1}) + D_{-2\varepsilon} \cdot (\frac{X_{-k,N}}{X_k} \hat{H}_{-k,N}^* - \frac{X_{-k-1,N}}{X_{k+1}} \hat{H}_{-k-1,N}^*)} \quad (3\text{-}26)$$

Therefore, we find out the difference Δ_β between β and $\hat{\beta}$. With this value, we can update our parameters to improve the compensation accuracy.

$$\begin{cases} \hat{\beta}_{update,t} = \hat{\beta}_{t-1} + \mu \cdot \Delta_{\beta,t-1} \\ \hat{\alpha}_{update,t} = 1 - \hat{\beta}_{update,t}^* \end{cases} \quad (3\text{-}27)$$

where μ is the adaptive step size. As $\hat{\beta}$ approaches β, the large transitions in estimated channel response will become smaller and smoother. This in turn makes the estimation error Δ_β smaller, and achieves the parameter adaptation. To sum up, we apply the parameters, $\hat{\alpha}$ and $\hat{\beta}$, to do signal compensation, and the rest transitions in estimated channel response are used to update $\hat{\alpha}$ and $\hat{\beta}$. So, the compensation accuracy is improved.

To summarize the overall adaptation algorithm, we depict the operation loop in Fig. 3-5. Before MG and SG estimation, the received signal is left uncompensated of I/Q mismatch, so the compensation parameters are set to be $\hat{\alpha}$=1 and $\hat{\beta}$=0 respectively as the initial values.

Moreover, the signal is compensated in the order of IQM followed by CFO. The estimation and compensation are done in frequency and time domain respectively, and $\hat{\alpha}$ and $\hat{\beta}$ are adaptively updated without any delayed-line filters.

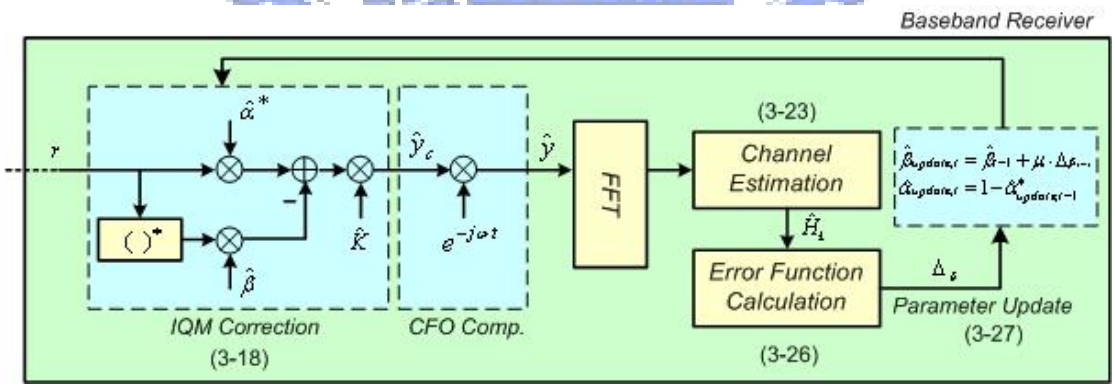


Fig. 3-5. Summary of the overall adaptation loop.

The SG and IG parameters in a wideband scenario are expressed by the base of frequency indices k. Again, both of SG and IG are regarded as the composition of estimation values ($\hat{\alpha}_k$ and $\hat{\beta}_k$) and estimation errors ($\Delta\alpha_k$ and $\Delta\beta_k$).

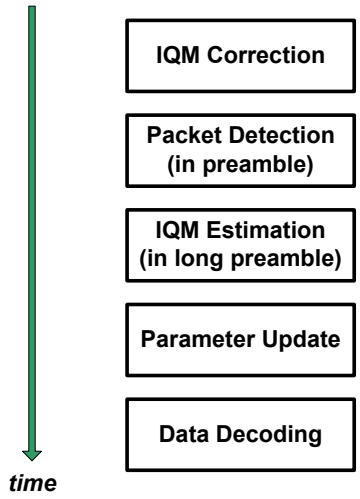


Fig. 3-6. Summary of the overall adaptation loop.

All of the incoming signals are compensated by the IQM correction building block. Although the IQM is not estimated before any packet detection, the data-path and compensation-flow go through the IQM block. Compensating the IQM or not depends on the values of the SG and IG parameters. In other words, the signals may be considered as uncompensated with the SG=1 and IG=0, even the compensation is applied to the received signals. The next step after the IQM-correction building block is the packet detection. This conventionally takes the preamble for packet recognition. Then the channel response is estimated after the packet detection. The estimated channel response is used for the IQM parameter estimation at the same time. With this value, the IQM SG and IG are updated, and the later-on coming signals are compensated by the latest estimated parameters as they are received in a baseband receiver. This means the rest of incoming signals are compensated by IQM, and the normal decoding flow starts for the signal demodulation. This reference time-chart is illustrated in Fig. 3-6.

3-4-2 Wide-band-based estimation

The SG and IG parameters in a wideband scenario are expressed by the base of frequency indices k. Again, both of SG and IG are regarded as the composition of estimation values ($\hat{\alpha}_k$ and $\hat{\beta}_k$) and estimation errors ($\Delta\alpha_k$ and $\Delta\beta_k$).

$$\begin{cases} \alpha_k = \hat{\alpha}_k + \Delta\alpha_k \\ \beta_k = \hat{\beta}_k + \Delta\beta_k \end{cases} \tag{3-28}$$

When the estimated parameters are applied for IQM compensation, an uncompensated error may exist in the calibrated signals due to non-ideal parameter estimation. To express the IQM compensated signals in terms of SG or IG estimation errors, we start the calculation from a non-ideal IQM compensation by (3-16)

$$\begin{aligned} \hat{Y}_k &= \frac{\hat{\alpha}_{-k}^* R_k - \hat{\beta}_k R_{-k}^*}{\hat{\alpha}_k \hat{\alpha}_{-k}^* - \hat{\beta}_k \hat{\beta}_{-k}^*} \\ &= \frac{\hat{\alpha}_{-k}^* (\hat{\alpha}_k Y_k H_{cm,k} + \hat{\beta}_k Y_{-k}^* H_{cm,k}) - \hat{\beta}_k (\hat{\alpha}_{-k}^* Y_{-k}^* H_{cm,-k}^* + \hat{\beta}_{-k}^* Y_k H_{cm,-k}^*)}{\hat{\alpha}_k \hat{\alpha}_{-k}^* - \hat{\beta}_k \hat{\beta}_{-k}^*} \end{aligned} \tag{3-29}$$

where $\hat{Y}_k$ is the compensated signals. We further replace the α_k and β_k values with estimated values and estimation errors (3-28) into (3-29), then we have

$$\begin{aligned} \hat{Y}_k = \hat{C}_k [&(\hat{\alpha}_k \hat{\alpha}_{-k}^* - \hat{\beta}_k \hat{\beta}_{-k}^*) Y_k H_{cm,k} + \\ &(\hat{\alpha}_{-k}^* \Delta\beta_k Y_{-k}^* H_{cm,k} - \hat{\beta}_k \Delta\alpha_{-k}^* Y_{-k}^* H_{cm,-k}^*) + \\ &(\Delta\alpha_k \hat{\alpha}_{-k}^* Y_k H_{cm,k} - \Delta\beta_{-k}^* \hat{\beta}_k Y_k H_{cm,-k}^*)] \\ = Y_k H_{cm,k} + \hat{C}_k [&(\hat{\alpha}_{-k}^* \Delta\beta_k - \hat{\beta}_k \Delta\alpha_{-k}^*) Y_{-k}^* H_{cm,k} + \\ &(\Delta\alpha_k \hat{\alpha}_{-k}^* - \Delta\beta_{-k}^* \hat{\beta}_k) Y_k H_{cm,k}] \end{aligned} \tag{3-30}$$

where $H_{cm,k} = H_{cm,-k}^*$ and $\hat{C}_k = 1/(\hat{\alpha}_k \hat{\alpha}_{-k}^* - \hat{\beta}_k \hat{\beta}_{-k}^*)$. From the dual property I, it is derived that $\alpha_k = 1 - \beta_{-k}^*$. If the estimated SG and IG are defined as $\hat{\alpha}_k = 1 - \hat{\beta}_{-k}^*$, we then further get another dual property in the estimation errors.

Dual Property II: $\Delta\alpha_k = -\Delta\beta_{-k}^*$ (3-31)

Back substitute (3-31) into (3-30), the proposed novel expression in terms of IG estimation errors becomes

$$\hat{Y}_k = Y_k H_{cm,k}(1 - \Delta\beta_{-k}^* \hat{C}_k) + \Delta\beta_k Y_{-k}^* H_{cm,k} \hat{C}_k \quad (3\text{-}32)$$

where $Y_k = X_{H,k}H_k$ or $X_{p,k}H_k$ depending on whether a channel preamble $X_{H,k}$ or information data $X_{p,k}$ is sent. When $\hat{\alpha}_k$ and $\hat{\beta}_k$ are set to 1 and 0 respectively, it is to keep the received signals uncompensated. This is taken as the initial value prior to any estimation. This means we are able to estimate the parameter error $\Delta\beta_k$ instead of calculating the β_k directly. Then the $\Delta\beta_k$ is used to update the previous estimation $\hat{\beta}_k$ to achieve the adaptive estimation and compensation.

Estimated Channel Frequency Response

A packet format shown in Fig. 3-7 is assumed for the SG and IG estimation. The channel preamble $X_{H,k}$ and the pilots $X_{p,k}$ in data OFDM symbols are used for IQM extraction with the values $k \in \{-55,-45,...,45,55\}$ denoting the pilot indices, and the values are also assumed to own the property

$$\begin{cases} X_{H,k} = X_{H,-k}^* \\ X_{p,k} = X_{p,-k} \end{cases} \quad (3\text{-}33)$$

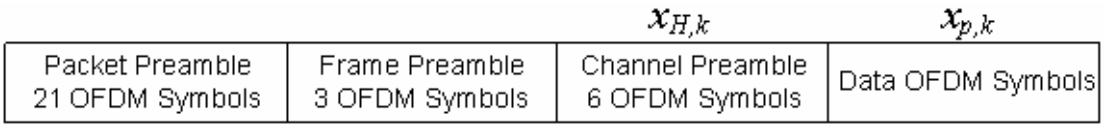


Fig. 3-7. The packet format for IQM estimation

From (3-32) and (3-33), we have the estimated channel frequency response (CFR) equal to

$$\hat{H}_k = \frac{\hat{Y}_k}{X_{H,k}} = [H_k(1-\Delta\beta^*_{-k}\hat{C}_k) + \Delta\beta_k H^*_{-k}\hat{C}_k]\cdot H_{cm,k} \tag{3-34}$$

It shows that the estimated CFR is distorted by three factors. First, an estimation error $\Delta\beta^*_{-k}$ results in a distortion term $(1-\Delta\beta^*_{-k}\hat{C}_k)$ to the actual CFR. Also, it induces image CFR interference from the mirrored subcarrier index. Then the circuit common response $H_{cm,k}$ in a down-conversion process is multiplied to constitute the estimated CFR. This means that a greater IQM results in a larger distortion in an estimated CFR, increasing errors in the equalized data, when the estimated CFR is applied for channel equalization. Therefore, the estimated CFR has to be refined when better SG and IG are estimated during the adaptive iterations.

Equalized Pilot Tones

The pilots after the channel are $Y_k = X_{p,k}H_k$ and $Y^*_{-k} = X^*_{p,-k}H^*_{-k}$. Substituting the image pilot $X^*_{p,-k}$ with $X_{p,-k} - 2\mathrm{Im}\{X_{p,-k}\}j$, we have the equalized pilot tones $\hat{Y}_k / \hat{H}_k$ expressed as

$$\hat{X}_{p,k} = \frac{\{X_{p,k}H_k(1-\Delta\beta^*_{-k}\hat{C}_k) + \Delta\beta_k[X_{p,-k} - 2\mathrm{Im}\{X_{p,-k}\}j]Y^*_{-k}\hat{C}_k\}H_{cm,k}}{[H_k(1-\Delta\beta^*_{-k}\hat{C}_k) + \Delta\beta_k H^*_{-k}\hat{C}_k]\cdot H_{cm,k}} \tag{3-35}$$

According to (3-33), the term $X_{p,-k} - 2\mathrm{Im}\{X_{p,-k}\}j$ is equal to $X_{p,k} - 2\mathrm{Im}\{X_{p,k}\}j$. As a result, the estimated pilot tone in (3-35) can be shortened as

$$\hat{X}_{p,k} = X_{p,k} - \frac{2\Delta\beta_k H^*_{-k}H_{cm,k}\,\mathrm{Im}\{X_{p,k}\}j}{\hat{H}_k} \tag{3-36}$$

In the image index -*k*, we follow the derivation above by replacing the $X_{p,-k}$ with $X^*_{p,-k} - 2\,\mathrm{Im}\{X^*_{p,-k}\}$. Then we have

$$\hat{X}_{p,-k} = X^*_{p,-k} - \frac{2H_{-k}H_{cm,-k}(1-\Delta\beta^*_k\hat{C}_{-k})\,\mathrm{Im}\{X^*_{p,k}\}j}{\hat{H}_{-k}} \tag{3-37}$$

Thus, the IQM effect can be described in a product term in (3-36)'s right hand side, which represents as an error vector to the clean subcarrier $X_{p,k}$. Therefore, the image rejection ratio (IRR) could be calculated directly from (3-36)

$$IRR_{(dB)} = 20\log(\frac{2\Delta\beta_k H^*_{-k}H_{cm,k}\,\mathrm{Im}\{X_{p,k}\}j}{\hat{H}_k} / X_{p,k}) \tag{3-38}$$

To extract the IG estimation error, we take the dual subcarriers, (3-36) and (3-37), to eliminate the CFR variable. Thus, we have

$$\frac{(X^*_{p,-k} - \hat{X}^*_{p,-k})\hat{H}^*_{-k}}{(X_{p,k} - \hat{X}_{p,k})\hat{H}_k} = \frac{1-\Delta\beta_k\hat{C}^*_{-k}}{\Delta\beta_k\hat{C}_k} \tag{3-39}$$

where the common circuit response $H_{cm,k}$ and pilot imaginary part are cancelled according to the dual property and (3-33). As a result, the IG estimation error is summarized as

$$\Delta\beta_k = \frac{(X_{p,k} - \hat{X}_{p,k})\hat{H}_k(\hat{\alpha}_k\hat{\alpha}^*_{-k} - \hat{\beta}_k\hat{\beta}^*_{-k})}{(X_{p,k} - \hat{X}_{p,k})\hat{H}_k + (X_{p,-k} - \hat{X}^*_{p,-k})\hat{H}^*_{-k}} \tag{3-40}$$

Thus, the SG estimation error is

$$\Delta\alpha_k = -\Delta\beta^*_{-k} = \frac{-(X^*_{p,-k} - \hat{X}^*_{p,-k})\hat{H}^*_{-k}(\hat{\alpha}_k\hat{\alpha}^*_{-k} - \hat{\beta}_k\hat{\beta}^*_{-k})}{(X^*_{p,-k} - \hat{X}^*_{p,-k})\hat{H}^*_{-k} + (X^*_{p,k} - \hat{X}_{p,k})\hat{H}_k} \tag{3-41}$$

So, the estimated SG and IG used for signal compensation are adaptively updated by

$$\begin{cases} \hat{\alpha}_{k,update,t} = \hat{\alpha}_{k,t-1} + \mu \cdot \Delta\alpha_{k,t-1} \\ \hat{\beta}_{k,update,t} = \hat{\beta}_{k,t-1} + \mu \cdot \Delta\beta_{k,t-1} \end{cases} \tag{3-42}$$

To illustrate the overall calibration algorithm, it can be summarized as Fig. 3-8.

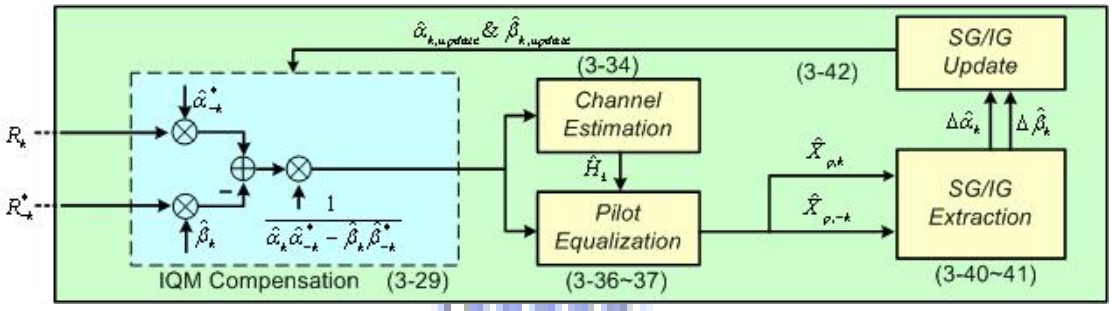


Fig. 3-8. Summary of the overall estimation and compensation behavior.

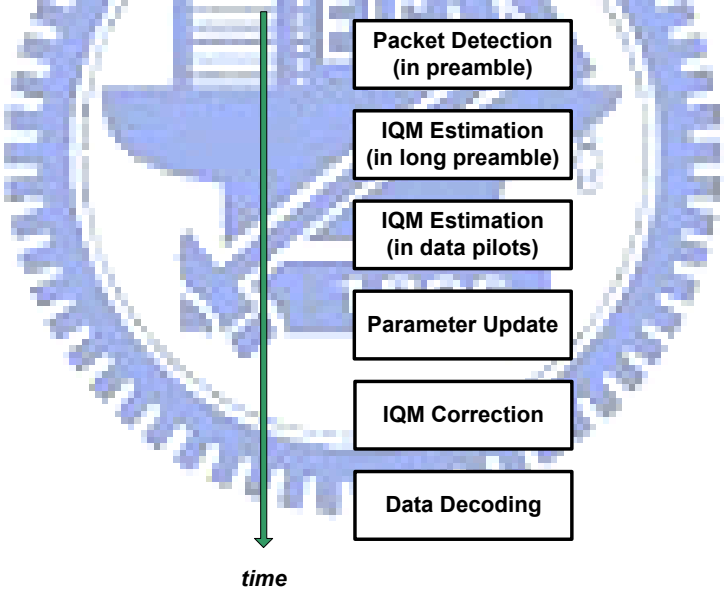


Fig. 3-9. Summary of the overall estimation and compensation behavior.

The overall behavior in a time-line base is summarized in Fig. 3-9. The frequency-domain based approach is somewhat different as the time-domain based one. A packet is detected first, and then the channel is estimated. Similarly, the estimated channel response is used for the later extraction of the IQM parameter

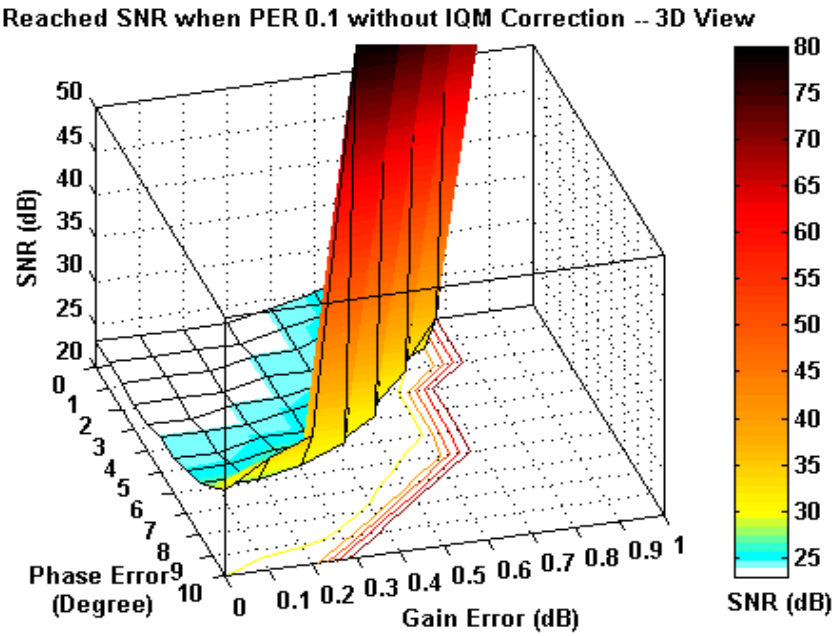
values. When the data information signals are received with the pilots interlaced in each OFDM symbol, the pilots are extracted to compute the SG and IG values. Those computed results directly feedback to the correction block for data compensation and data decoding. Recursively, the later-on pilots in OFDM symbols are utilized for more accurate IQM extraction to achieve the adaptive calculation. Those behaviors after the packet detection are done in the frequency domain.

3-5 Simulation Results

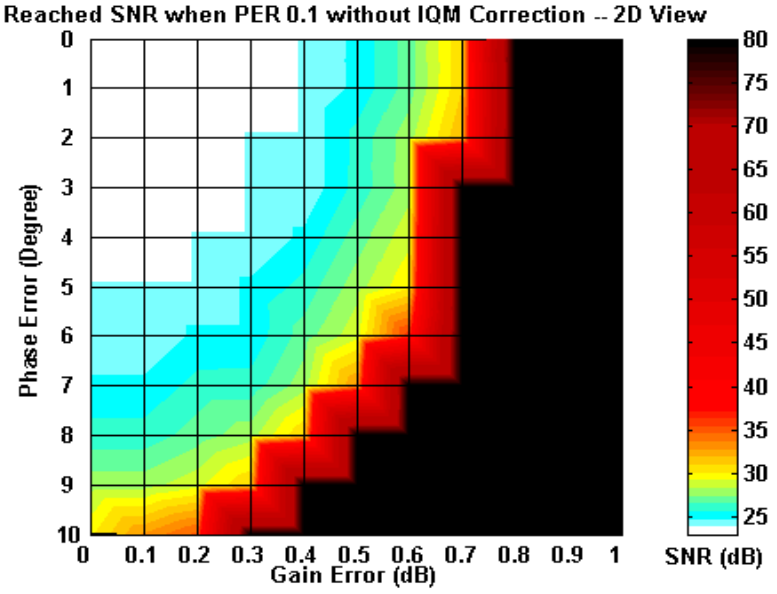
3-5-1 Narrow-band adaptive scheme

To verify our proposed HD-FAC algorithm, we apply ERP-OFDM in IEEE 802.11g [28] as our OFDM simulation vehicle. In this system, data rate ranges from 6M to 54Mbps, and the QAM has different modulation order from BPSK to 64QAM. Also, the receiver is concatenated with an outer receiver, which applies Viterbi algorithm for the final data decoding. In order to verify the proposed algorithm, the most sensitive transmission mode, 54Mbps with 64 QAM, is chosen. Since OFDM is robust to fading channel, we also target the simulation environment on Rayleigh fading channel with coherent bandwidth 20MHz. In the simulations, 1024 packets are sent at each SNR value, and each packet consists of 1024 information bytes. To see how IQM degrades system performance without compensation, we simulate the PER performance in sweeping different gain and phase errors to the system under Rayleigh fading channel. When PER reaches 0.1, we can see the SNR distribution with different phase and gain errors as shown in Fig. 3-10. If we trace the axis where only phase error exists, we found that the SNR value degrades more than 30 dB. On the other hand, we can find the system has dramatic degradation even with only gain error. So, gain error has larger impact on the system. It can be observed not only system

degrades fast but unrecoverable errors occur with increased gain and phase errors, especially when the two effects exist together. Therefore we cannot get a high performance OFDM processor without any compensation.



(a)



(b)

Fig. 3-10. System performance without IQM correction under Rayleigh fading channel. The reached SNR at PER 0.1 with different gain and phase error values (a) the 3-D view (b) the corresponding projection in 2-D view.

Before examining overall system performance of our proposed algorithm, we first look at the impact of different step sizes on adaptive tracking and system behavior. The absolute value of Δ_β is simulated under Rayleigh fading channel at SNR 25 dB and depicted in Fig. 3-11, and the PER with corresponding step sizes are shown in Fig. 3-12.

Although different step sizes result in different convergence time and variation, the system reaches the similar performance. This is due to the convergent time is fast enough and the residual estimation error does not dominate the system performance. Therefore, we choose a step size 0.5 for our further simulation since this number will simplify the computation and update process.

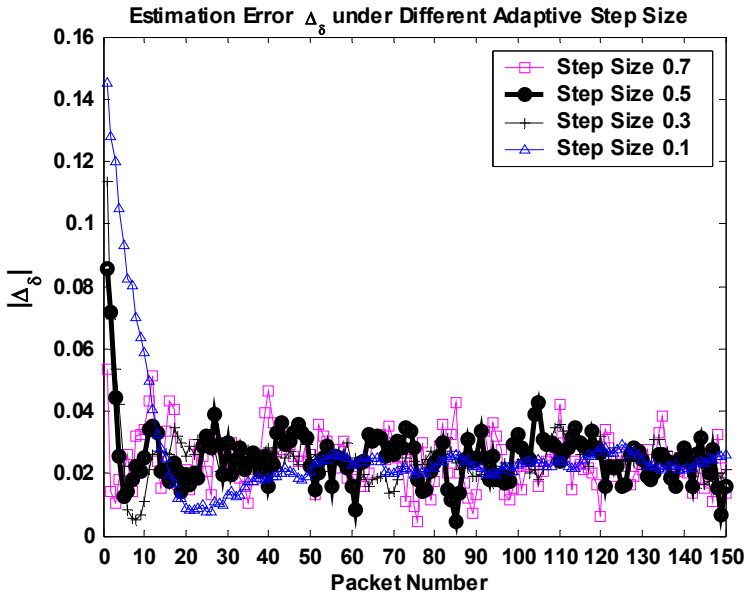


Fig. 3-11. $\Delta\beta$ convergence with G.E. 1dB and P.E. 10 degree in Rayleigh fading channel @ SNR 25dB.

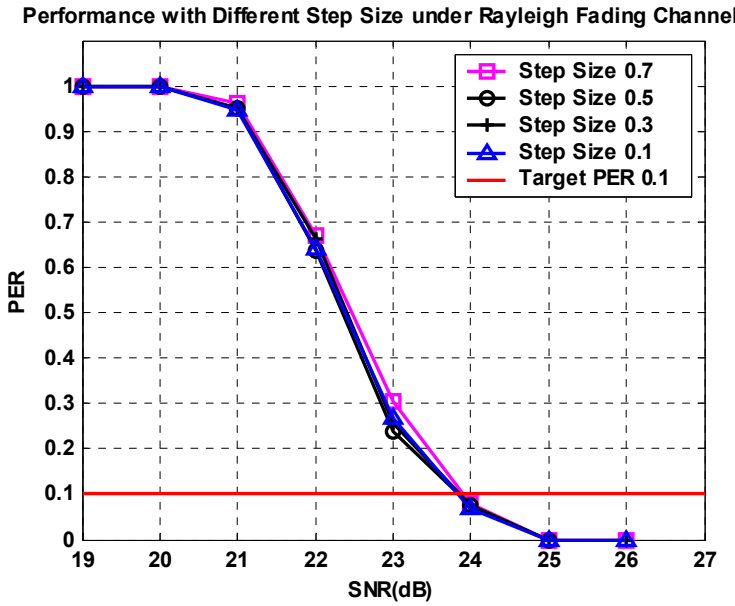
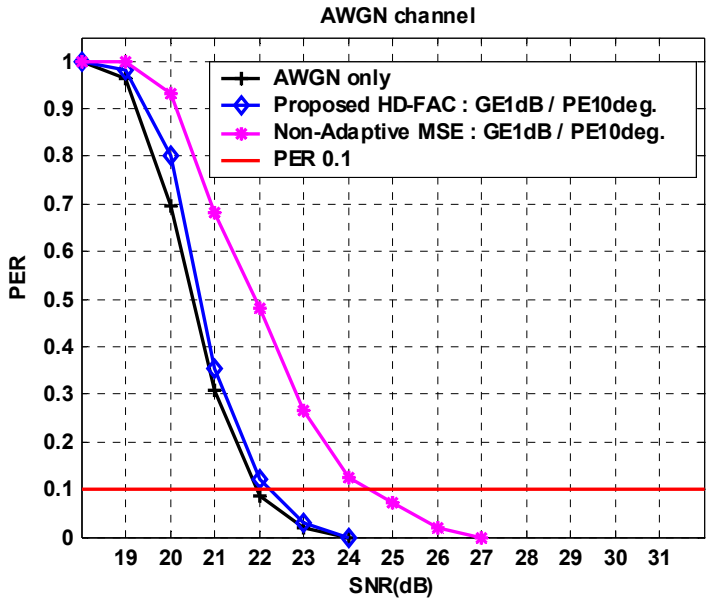


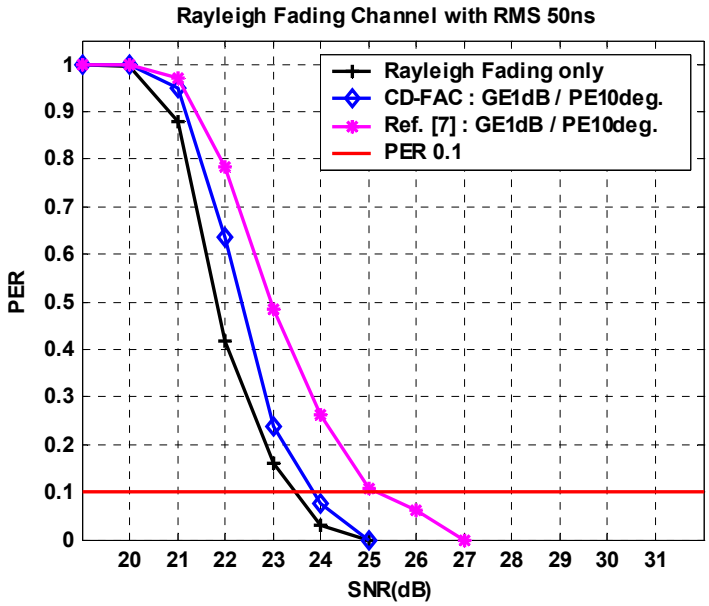
Fig. 3-12. PER simulation with different step sizes under gain error 1dB and phase error 10 degrees

In the following, we set up three channel conditions to verify our algorithm and system. First is the pure AWGN environment. The second is Rayleigh fading channel with RMS 50ns. The third is Rayleigh fading channel in addition to 120kHz CFO, which is equivalent to 38.4% subcarrier frequency spacing or 50 ppm at 2.4G carrier frequency as specified in [28]. To verify HD-FAC algorithm, gain and phase errors are set to be 1dB and 10 degree as suggested in [35], and the results are shown in Fig. 3-13. In Fig. 3-13(a) of AWGN and IQM channel, we apply a non-adaptive MSE-based algorithm for IQM estimation as our reference design, which can be seen in [32] for example. Due to the limited available samples for IQM calculation, the estimation is not accurate enough. Therefore, as we apply our proposed HD-FAC algorithm, the system performance is largely improved more than 2dB at PER 0.1, and the performance has only 0.3dB SNR loss in pure AWGN environment. In the Rayleigh fading channel with RMS 50ns, which consists of exponential decaying power with uniform random distributed phase, our system results in 0.5dB SNR loss

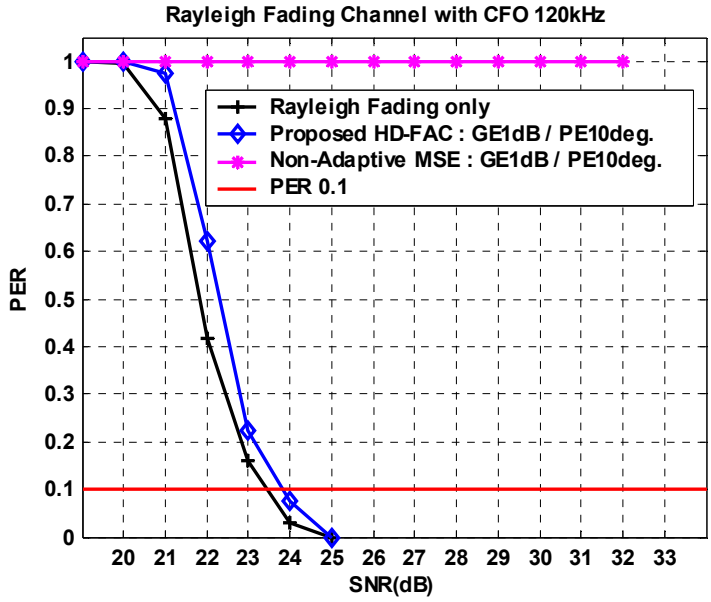
whereas the reference design possesses about 1.5dB SNR loss. In the last simulation condition, the channel is applied with fading channel in addition to CFO 120 kHz, and the CFO is estimated by correlation in long-preamble field of a packet. There exists an estimation error of CFO amount, but this provides HD-FAC an initial CFO value for Δ_β estimation. Then the IQM compensated signal will make a more accurate CFO estimation, and in turn improve the IQM estimation and compensation by adaptation. From Fig. 3-10(c), we see the performance has only about 0.5dB SNR loss, showing the stability and robustness under Rayleigh fading channel and CFO environment. We summarize the simulation performance in terms of SNR loss in Table 3-1.



(a)



(b)



(c)

Fig. 3-13. IQM compensation performance with GE 1 dB and PE 10 degree under (a) AWGN channel (b) Rayleigh fading channel (c) Rayleigh fading and CFO channel.

TABLE 3-1. SNR LOSS UNDER DIFFERENT CHANNEL CONDITIONS

GE / PE	1 dB / 10 degree		
Channel	AWGN	Rayleigh Fading (RMS 50ns)	Rayleigh Fading (RMS 50ns) CFO (120kHz)
Proposed HD-FAC	0.3	0.5	0.5
Non-Adaptive MSE	2.2	1.5	Inf

The performance is evaluated under (a) AWGN (b) Rayleigh Fading channel with RMS 50ns (c) Rayleigh Fading channel with RMS 50ns and CFO with 120kHz.

To illustrate the system operation, we show the estimated channel response before and after IQM compensation in Fig. 3-14. In the initial state, the channel is estimated without any correction, so there are obvious amplitude transitions in the estimated channel. After the proposed HD-FAC, the estimated channel becomes more continuous and approaches the primitive channel response. In initial state, the data compensated by IQM and the initial estimated channel has the constellation shown in Fig. 3-15(a). On the other hand, when the estimated IQM parameter $\hat{\alpha}$ and $\hat{\beta}$ become more accurate, the IQM compensation is improved and also the data is compensated by a more realistic channel response, which has the steady state constellation shown in Fig. 3-15(b). Both of the channel conditions in Fig. 3-14 and Fig. 3-15 are simulated under Rayleigh fading channel with CFO 120kHz at SNR 30dB.

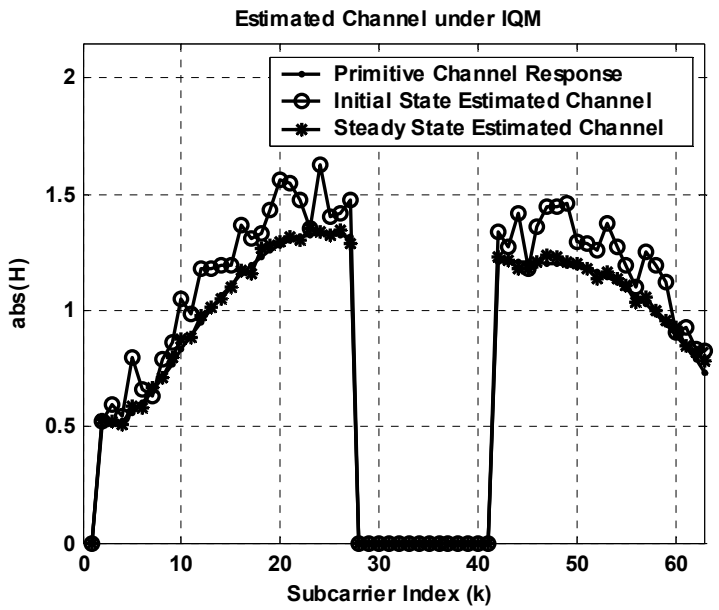
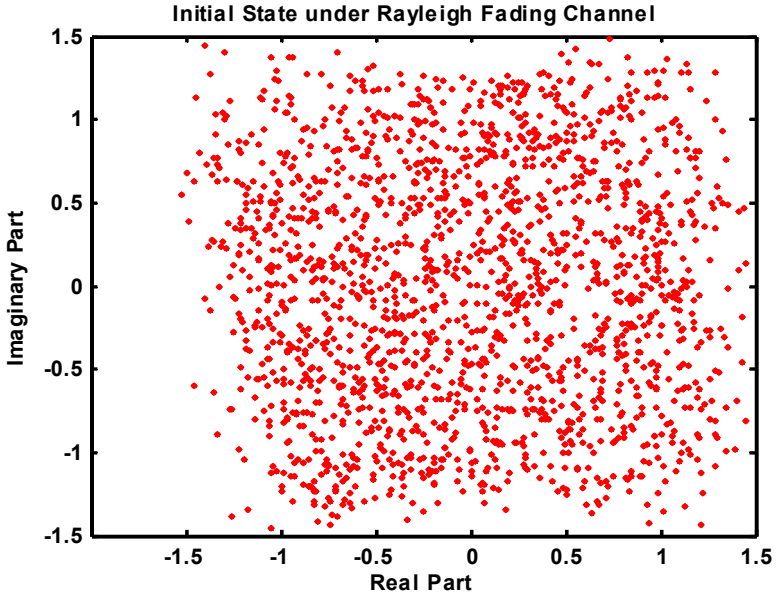
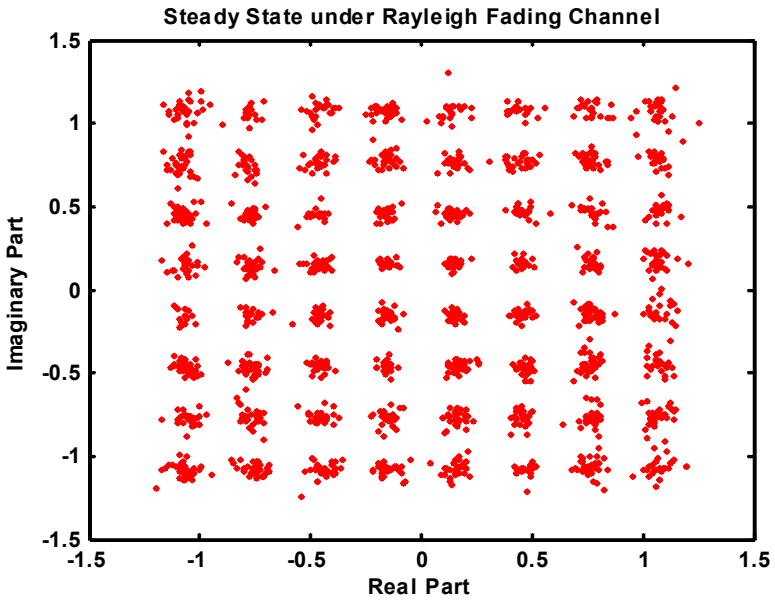


Fig. 3-14. Estimated channel resopnse with the proposed HD-FAC under gain/phase errors 1dB and 10 deg., and Rayleigh fading channel RMS 50ns @ SNR 30dB



(a)



(b)

Fig. 3-15. Constellation with the proposed HD-FAC under gain/phase errors 1dB and 10 degrees and Rayleigh fading channel RMS 50ns @ SNR 30dB (a)Initial State (b)Stable State.

The computation requirements for HD-FAC are listed and compared without considering $\hat{H}_k$ and X_k's calculation and storage since they do not belong to IQM estimation or compensation. In HD-FAC, the value $\hat{K} = \frac{1}{|\hat{\alpha}|^2 - |\hat{\beta}|^2}$ is calculated and stored for the use of both compensation and *dMG* computation. Therefore, we need three value storage elements for $\hat{\alpha}$, $\hat{\beta}$, and $\hat{K}$ in compensation stage. Then, the stored value $\frac{1}{|\hat{\alpha}|^2 - |\hat{\beta}|^2}$ is used for Δ_β computation as indicated in (3-26), and do not need to compute its value again. In comparison with time-domain non-adaptive least-square algorithm [34], it applies a delay-line filter for IQM compensation. Assume a 5th order filter is used, so it needs five coefficients and an additional gain factor for data filtering, resulting in 6 multiplications and 5 additions. To determine the values of filter coefficients, a minimum cost function search is applied, largely increasing the computation requirements. The computation

requirements for HD-FAC and time-domain non-adaptive least-square algorithm are summarized in TABLE 3-2.

TABLE 3-2. COMPUTATION REQUIREMENT

	Proposed HD-FAC		5^{th} Order Time-Domain Non-Adaptive LS-based Algorithm	
	Compensation	Δ_β Computation	Compensation	Coeff. Calc.
Multiplication	5	3	6	10
Addition	5	4	5	5
Differentiation	0	0	0	5
Value Storage	3	0	6	2

The table lists the operators and necessary value storages for the proposed HD-FAC and its comparison

3-5-2 Wide-band scheme

To evaluate the proposed wideband IQM calibration capability, the multi-band OFDM ultra-wideband (MB-OFDM) [2] is selected as the simulation platform, in which signals are modulated as QPSK in a 528MHz bandwidth with maximum data rate 480Mbps. Each OFDM symbol is formed by 128 subcarriers, and 112 out of them ($k = \{-56 \sim 56 \mid k \in R, k \neq 0\}$) are information subcarriers, including 12 pilot tones ($k = \{-55,-45,...,45,55\}$), which are then used for IQM estimation. In the outer receiver, a Viterbi decoder is provided for error correction.

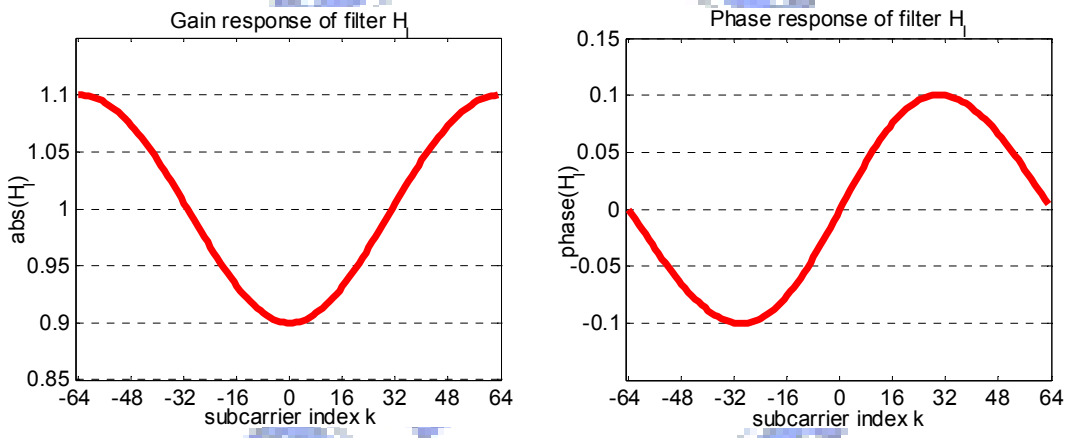
The 1dB gain error and 10 degree phase error are applied to the system as the simulated IQM range. The $H_{cm,k}$ and $H_{df,k}$ reflect if the IQM is frequency independent or frequency selective. In a frequency-independent IQM, we have the responses

$H_{cm,k}=H_{df,k}=1$ for all index k. When a frequency-selective IQM is considered, we set the filter response to be [34]

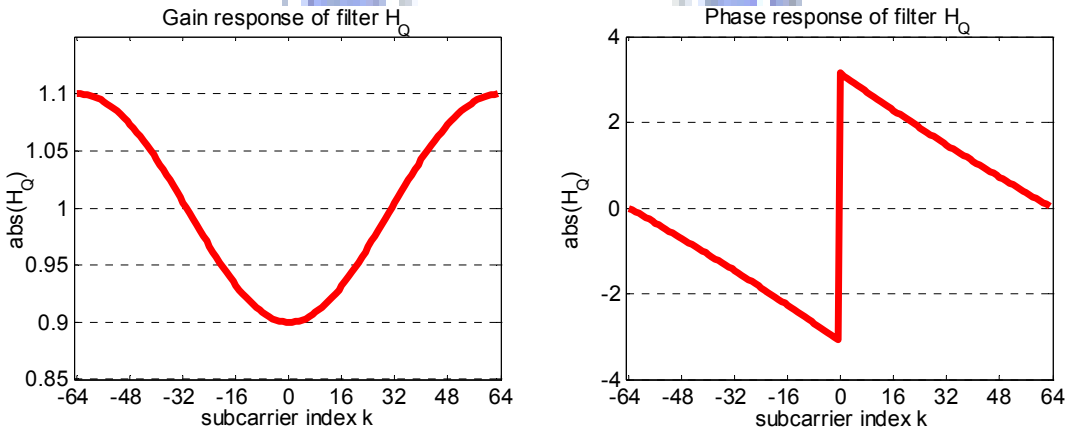
$$\begin{aligned} H_{cm,k} &= FFT_{128}\{[1 \quad 0.1]\} \\ H_{cm,k} \cdot H_{df,k} &= FFT_{128}\{[0.1 \quad 1]\} \end{aligned} \tag{3-43}$$

The amplitude and phase responses of filters H_I and H_Q are shown in Fig. 3-16. The pilot tones in each OFDM symbols are used for IQM estimation, and the estimation results are refined adaptively when an OFDM symbol comes. Since there are only limited subcarrier indices representing the pilot tones, only the pilot indices perform exact IQM estimations when a noiseless channel is assumed. If the IQM is constant over the whole concerned frequency range, the estimation results from pilot indices are duplicated to every subcarrier indices. When IQM is frequency selective, however, an interpolation becomes necessary to provide SGs and IGs in every spectrum index. Fig. 3-17 shows the SG and IG responses in a frequency-selective manner, in which the SG and IG values are estimated exactly in the pilot indices, say -35 and -25. The rest SG and MG between two pilot tones are calculated by 1st-order (linear) or 2nd-order interpolation. The resulting IRR is illustrated in Fig. 3-18, which shows that the pilot indices have infinite IRR values representing a perfect estimation. It is also found that the 2nd-order interpolation promises a reasonable IRR level (min. 45dB) for signal compensation [42]. In a noiseless channel the signal constellation before and after compensation are shown in Fig. 3-19. The calibrated signal constellation in Fig. 3-19(b) has an average IRR 47.9dB, which presents a matching result by calculating from (3-38) directly. Fig. 3-20 shows the signal constellation before and after calibration in a SNR 20dB condition.

Finally, we show the overall system performance in terms of packet error rate (PER) in frequency-independent and frequency-selective conditions. In a frequency-independent IQM scenario, it is found that the PER curves with adaptive calibrations almost merge with the zero-IQM AWGN curve when 1dB gain error and 10^{o} phase error are simulated. In a frequency-selective IQM scenario, it is found the uncompensated signals perform diverged PER even when the gain and phase errors are zeros. By the proposed adaptive calibration, the PER curves approach the AWGN zero-IQM curve with SNR loss less than 0.4dB, which also performs better by SNR 2.5dB than the one with non-adaptive behavior.



(a)



(b)

Fig. 3-16. The frequency-selective IQM modeling with transfer function of (a) filter H_I (b) filter H_Q

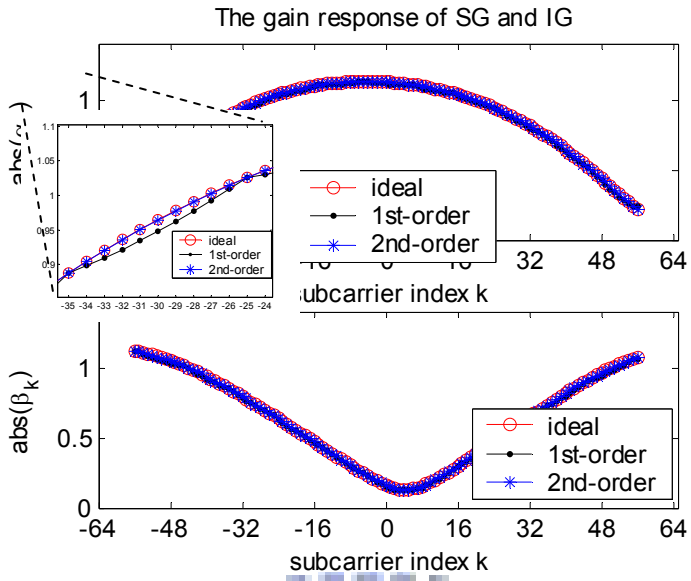


Fig. 3-17. The ideal SG and IG responses with the estimations in 1st-order and 2nd-order interpolations.

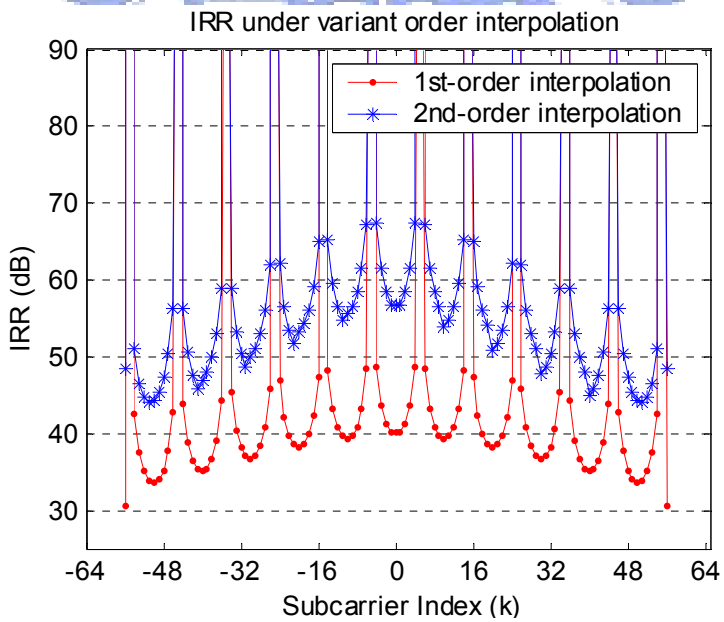
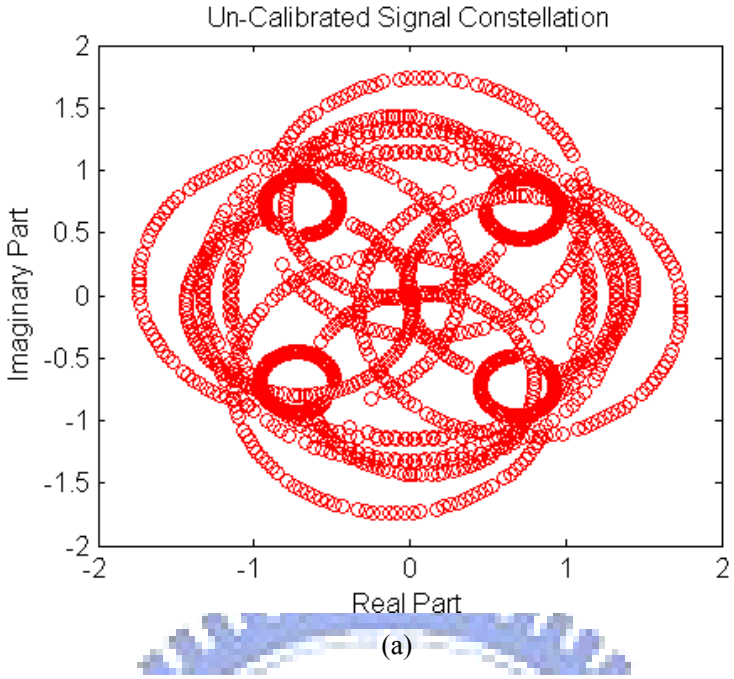
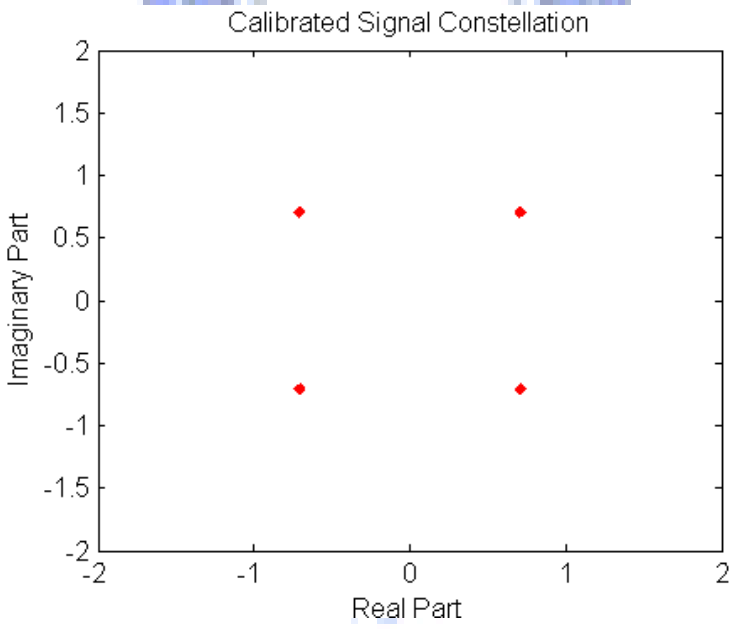


Fig. 3-18. The image rejection ratio (IRR) after compensation in a frequency selective IQM condition.

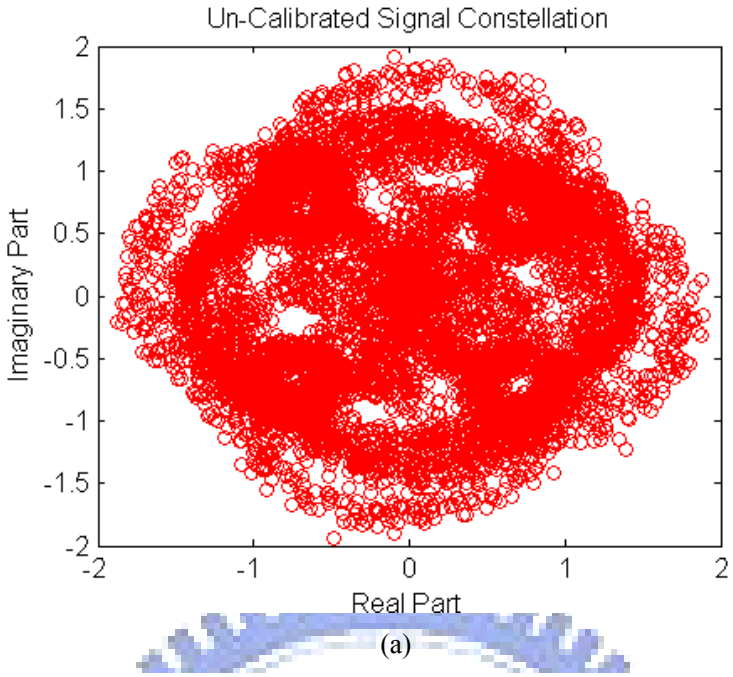


(a)

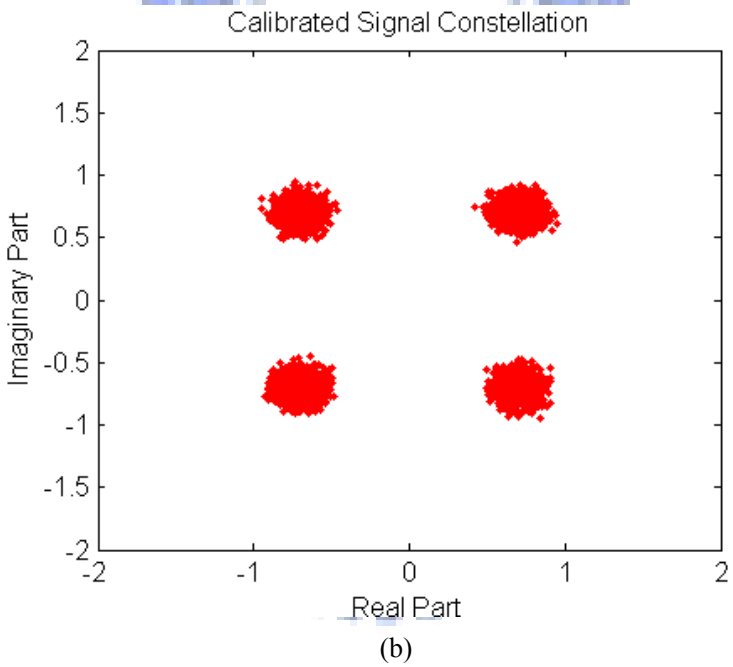


(b)

Fig. 3-19. The signal constellation under the frequency-selective IQM in 1dB gain error and 10^{o} phase error (a) without and (b) with calibration.



(a)



(b)

Fig. 3-20. The signal constellation under the frequency-selective IQM in 1dB gain error and 10^{o} phase error (a) without and (b) with calibration in a SNR 20dB AWGN channel.

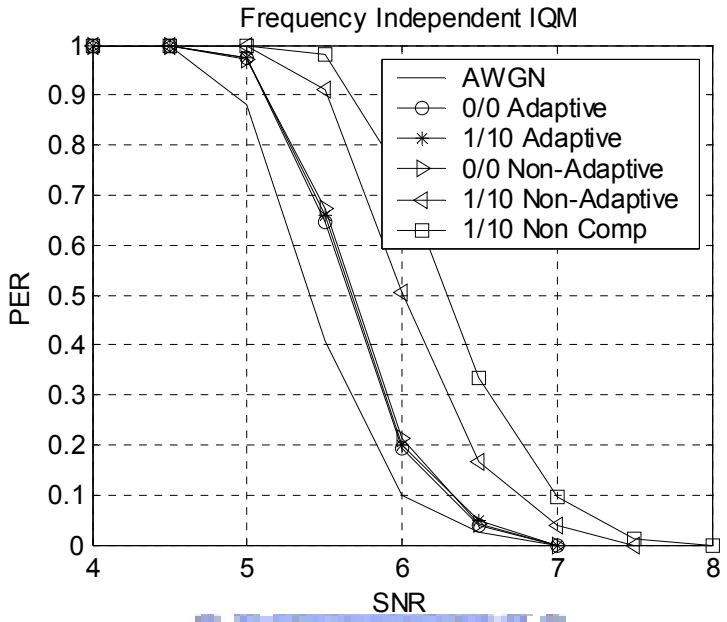


Fig. 3-21. The packet error rate in a frequency-independent IQM condition.

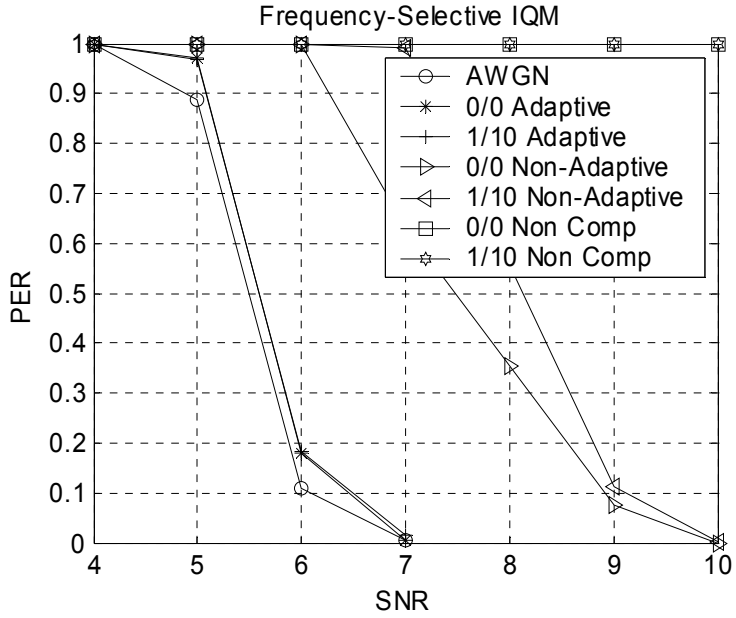


Fig. 3-22. The packet error rate in a frequency-selective IQM condition.

3-6 Summary

Adaptive IQM calibration approaches are presented in this chapter. The calibration is achieved in either frequency-independent or frequency-dependent scenario. The adaptive behavior is only achieved when an error function is defined.

This work provides both the error functions for the frequency-independent and frequency-dependent schemes. All of the calibration processes are done in an all-digital manner so that the signals are compensated by signal process techniques.

The frequency-independent calibration is realized by the proposed hybrid-domain filterless adaptive compensation scheme (HD-FAC). With an adaptive step size $\mu = 0.5$, the overall performance loss under different channel conditions is simulated to be less than 0.3dB in AWGN channel and 0.5dB in Rayleigh fading channel, respectively, in the 1dB gain-error and 10^{o} phase-error scenario.

The frequency-dependent calibration is achieved by the pilot-based IQM calibration. This approach achieves an average image rejection ratio 47.9dB in a frequency-selective mismatch condition with gain error 1dB and phase error 10^{o}. The overall system performance at packet error rate=8% has SNR loss less then 0.4dB, and requires a reduced 2.5dB SNR to reach this performance level compared to a non-adaptive calibration approach.

Chapter 4:

Dynamic Sampling-Timing Control

4-1 Background and Overview

Nyquist frequency is a fundamental frequency that should be used to sample an analog continuously waveform without loss of information. In wireless applications, a baseband processor usually applies a sampling frequency that is more than Nyquist rate, say 4x or 8x of signal bandwidth, to acquire more accurate signal sampling and better signal quality. This high-rate sampling, however, increases ADC circuit operation power and complicates digital signal processing, resulting in about 1/3 of total chip power of both RF and baseband. In other words, the ADC sampling frequency is highly correlated to the circuit operation power. An effective power reduction approach for the whole system is to reduce the sampling frequency to the symbol rate whereas the system performance is maintained.

Accordingly, this chapter describes a power reduction scheme, dynamic sample-timing control (DSTC), which enables a baseband receiver sampling incoming waveforms at the frequency that is equal to the symbol rate in the transmitter. This symbol-rate sampling behavior minimizes operation efforts in an ADC circuit, resulting in minimized ADC operation power. At the same time, the loading of digital signal processing is reduced. This data converter controlling is regarded as a digitally-based analog circuit controlling in a system level design. This DSTC collaborate signal process techniques from a baseband to smartly control an analog/digital converter (ADC) for reduced ADC sampling frequency. This lowered

sampling frequency dramatically reduces overall power consumption in a wireless baseband circuit operation. The role of this DSTC scheme is introduced as shown in Fig. 4-1.

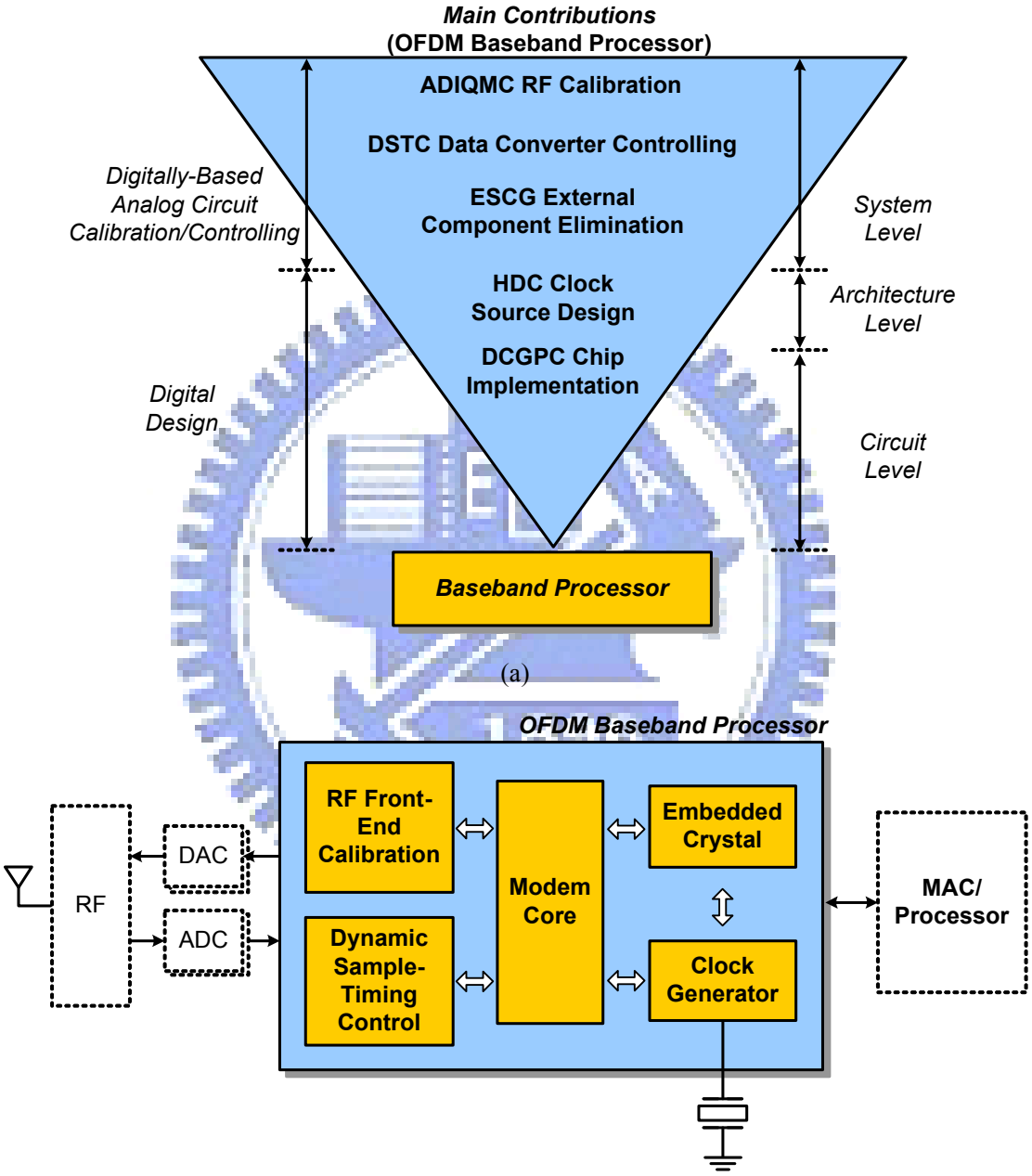


Fig. 4-1. The role of the dynamic sample-timing control in the power and data proximity scheme

Power consumption in a wireless device can be roughly divided as 1/3 from RF, 1/3 from data converter, and 1/3 from baseband signal process. It is found that

possible ways for power reduction are to reduce the power from each building block or to change the controlling behaviors between those circuits. Accordingly, this proposal is going to reduce the circuit power by a proper baseband control to the ADCs to achieve the low power purpose. A relationship of the power versus operating frequency for ADC circuits is revealed in Fig. 4-2. It is found that the power consumed is roughly twice when the operating frequency is doubled. In other words, a proper design and controlling of the ADC circuits to reduce the operating frequency to half frequency will effectively shrink the ADC power consumption to its half, resulting in dramatically power reduction in the whole system. A power budget is shown in Fig. 4-2 that is defined in a wireless system for portable device, ex: MB-OFDM UWB system [2]. It is found that a pair of ADC circuits operating at the frequency of the signal bandwidth almost consumes the power more than the power budget. If the operating frequency stays at the conventional Nyquist or more than 4x of bandwidth frequency, it meets difficulty to satisfy the system power budget. Therefore, this chapter describes a methodology applying synchronization techniques to reduce the required operating frequency that is used to drive the ADC circuits, resulting in power reduction.

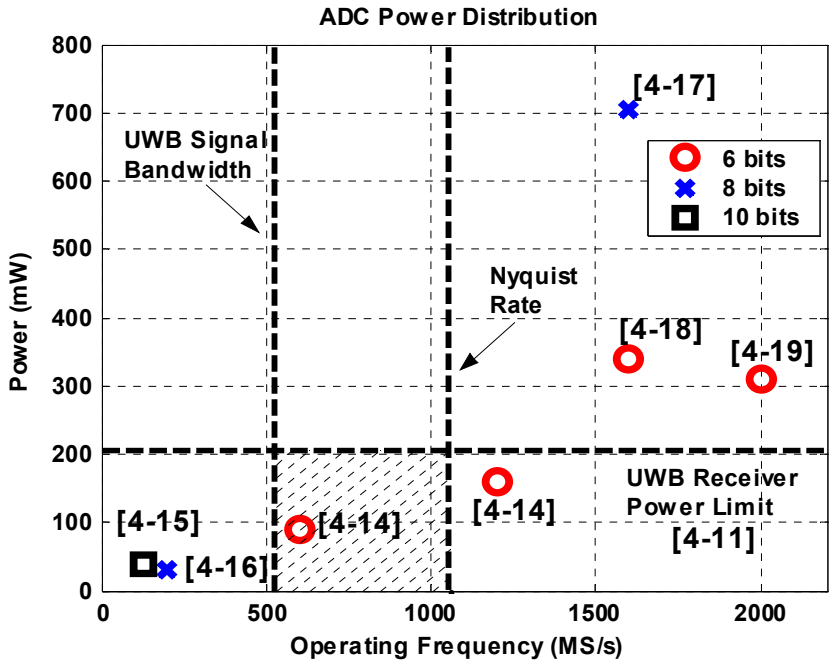


Fig. 4-2. The power and operating frequency for ADC circuits

Timing synchronization plays an important role in ensuring good signal decoding performance, since it determines the sampling timing and frequency of the analog-to-digital converter (ADC) on incoming signals or packets. Existing design approaches apply multi-rate sampling (at Nyquist rate or higher than 4× symbol rate [44][45][46]) to the incoming waveform with a fixed high-rate clock source that drives an ADC circuit. Those high-rate sampled signals are then calculated by an interpolation algorithm [47] to yield a symbol-rate signal stream for data decoding. This design methodology to designing power-thirsty portable devices is facing increasing difficulty, because both the ADC circuits and the interpolation circuits are operated at a higher processing rate, resulting in higher power consumption.

To enable power reduction with symbol-rate sampling, both Mueller-Muller detection (MMD) [48] and MMD-based timing recovery methods [49] have been proposed under a pulse amplitude modulation (PAM) scheme for best sampling timing search within a sample period. The literature explores the timing

synchronization issue in OFDM systems based on the best block-boundary search for each FFT transformation window [50][51]. However, those studies [50][51] do not guarantee that the signals in each block are sampled at the best sampling timing. Accordingly, multi-rate sampling schemes [44][45] have been developed to maintain system performance; hence the high-rate operations significantly increase power dissipation.

To maintain system performance and, in the meantime, to reduce power dissipation, this work presents a dynamic sample-timing control (DSTC) scheme for symbol-rate synchronization in OFDM systems, where the optimal sampling timing within a symbol-period interval can be calculated. Unlike multi-rate sampling methods [44][45][46], this DSTC requires aided circuits in a clock source design to generate a phase-tunable clock waveform that corresponds to the best sampling instance as calculated by the DSTC. A digitally-controlled oscillator (DCO) design concept [52] is applied to the phase-tunable clock generator (PTCG) design to enable this symbol-rate DSTC [12] for low-power wireless applications.

4-2 System Introduction

Signals in OFDM system are transformed by an *N*-point discrete inverse Fourier transformation (IDFT)

$$x[n] = \frac{1}{N}\sum_{k=0}^{N-1} X[k] e^{j\frac{2\pi kn}{N}} \tag{4-1}$$

where $X[k]$ is an information symbol stream with PSK or QAM encoded. OFDM signals after digital-to-analog conversion (DAC) are expressed as

$$x_T(t) = \sum_{n=-\infty}^{\infty} \left(\frac{1}{N} X[k] e^{j\frac{2\pi kn}{N}}\right) \cdot \mathrm{sinc}(t - nT_s) = \sum_{n=-\infty}^{\infty} x[n] \cdot \mathrm{sinc}(t - nT_s) \tag{4-2}$$

where T_s is the sample period. In order to meet spectrum mask requirements, the signal is filtered by a transmitter pulse response $f_T(t)$, and then transmitted in carrier frequency f_c. Thus, the passband representation is given by

$$s(t) = \mathrm{Re}\{[x_T(t) * f_T(t)] \cdot e^{j2\pi f_c t}\} \tag{4-3}$$

In up/down and analog/digital data conversions, the signal suffers from any non-ideal hardware distortion, including every filter response (f_T and f_R) from both the transmitter (TX) and the receiver (RX) sides. Therefore, down-converted signals in a receiver are given by

$$x_R(t) = [x_T(t) * f_T(t) * f_R(t)] \cdot e^{j2\pi \cdot f_{CFO} \cdot t} + w(t) * f_R(t) \tag{4-4}$$

where f_{CFO} is the carrier frequency offset (CFO) between the TX and RX, and $w(t)$ is additive white Gaussian noise (AWGN). After the ADC circuits, signals in digital time-domain are given by

$$x_{R;\varepsilon}[n] = \sum_n x_R(t) \cdot \delta[t - (n - \varepsilon)T_s] \qquad \varepsilon \in R,\ |\varepsilon| < \frac{1}{2} \tag{4-5}$$

where ε is a sampling phase offset of the sample period that is represented as a fraction of a sample period, and $\delta(t)$ is an impulse function with the definition

$$\delta(t) = \begin{cases} 1 & ,t = 0 \\ 0 & ,t \neq 0 \end{cases} \tag{4-6}$$

The system block diagram is illustrated in Fig. 4-3. Once a packet has been detected, the DSTC is activated to search the best sampling instance for the received waveform. In the search duration, the DSTC is tuned by sending a forward (Fwrd) or a backward (Brwd) command to the PTCG to generate the optimal clock phase for signal sampling in the ADCs. The PTCG first generates a clock signal with the required frequency. This clock is further used to generate N clock signal. Each of the N signals is delayed and separated by a delay fraction ε = Ts/N. Then, a multiplexer selects one of the clock signals to drive an ADC circuit for incoming waveform sampling. Then, the signals follow the conventional decoding flows.

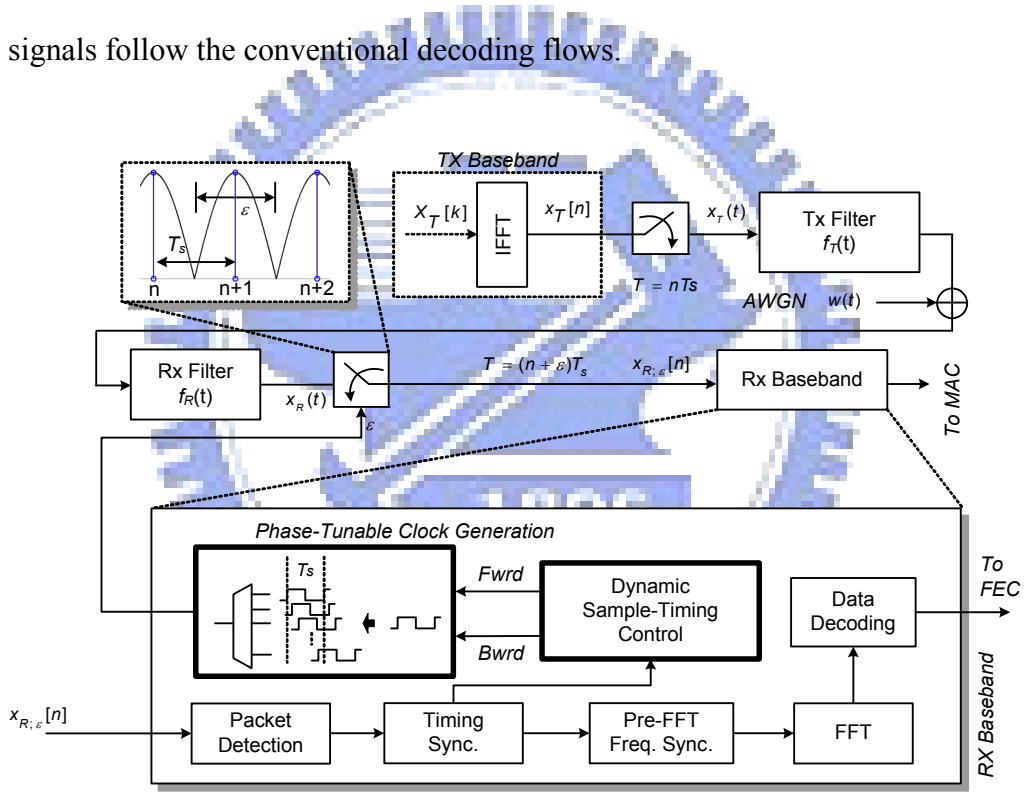


Fig. 4-3. Block diagram of the proposed baseband receiver with the aid of the proposed dynamic sample-timing control (DSTC) and phase-tunable clock generation (PTCG).

4-3 Dynamic Sample-Timing Control

The goal of this algorithm is to determine a signal sampling instance with the sampling rate equal to the symbol rate, $T = T_s$, where the inter-symbol interference

(ISI) associated with filter pulse responses is minimized. Assume the transmitter pulse response $f_T(t)$ and receiver analog prefilter $f_R(t)$ are considered to be the effectively equivalent response

$$f(t) = f_T(t) * f_R(t) \tag{4-7}$$

The overall system responses, including the transmitter and receiver filters, tend to comprise an overall impulse response equal to a certain filter response, like a sinc function, a raised-cosine function, or a butterworth function. Some representative filter responses are sketched as shown in Figs. 3-4~3-6, and those filters can be regarded as performance corners for the rest of discussion.

4-3-1 Sinc Filter

A sinc filter has a transfer function that is defined as unit amplitude in its gain response and signal symbol rate in its bandwidth. Although this is not hardware-implemented, it represents some performance corner in this DSTC design scheme. This rectangular transfer function has an impulse response expressed in Eq. (4-8). This corresponds to the simulated waveform as shown in Fig. 4-4.

$$f_{\sin c}(t) = \mathrm{sinc}(t) = \begin{cases} \dfrac{\sin(\pi t)}{\pi t} & ,if\ x \neq 0 \\ 1 & ,if\quad x = 0 \end{cases} \tag{4-8}$$

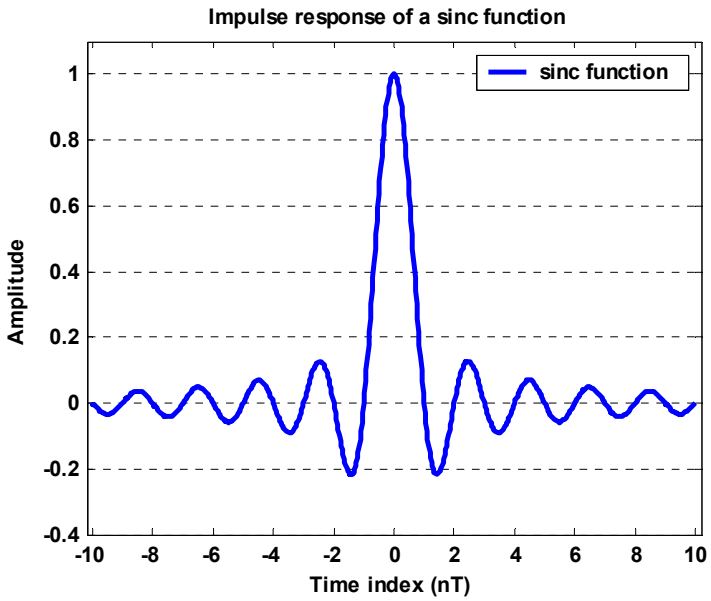


Fig. 4-4. Sinc function impulse response

4-3-2 Raised-Cosine Filter

A raised-cosine filter may be viewed as a composition of dual root-raised-cosine filters. The overall responses from a transmitter and a receiver may be assumed as an equivalent raised-cosine filter for scenario discussions and performance investigations. The property of a raised-cosine filter is that it allows an impulse response with long tails but zero-crossed at the signal-tap positions. In other words, the signal stream has inter-symbol-interference (ISI) phenomenon, but there is no signal distortion as long as the sampling instance is located at the best sampling positions. As a result, the ISI effects can be prevented when the sampling locations are carefully calculated. The impulse response of the raised-cosine filter is expressed in Eq. (4-9).

$$f_{raised-cosine}(t) = \mathrm{sinc}(\frac{t}{T})\frac{\cos(\frac{\pi\beta t}{T})}{1-\frac{4\beta^2 t^2}{T^2}} \tag{4-9}$$

The parameter β is defined as the roll-off factor. This factor determines how sharp the filter edge is, implying the damping and swing level of the impulse response tails. A larger roll-off factor reflects a sharper filter edge and also a shorter impulse response tails. The impulse responses are illustrated in Fig. 4-5 with the roll-off factor 0.2, 0.5, and 0.8.

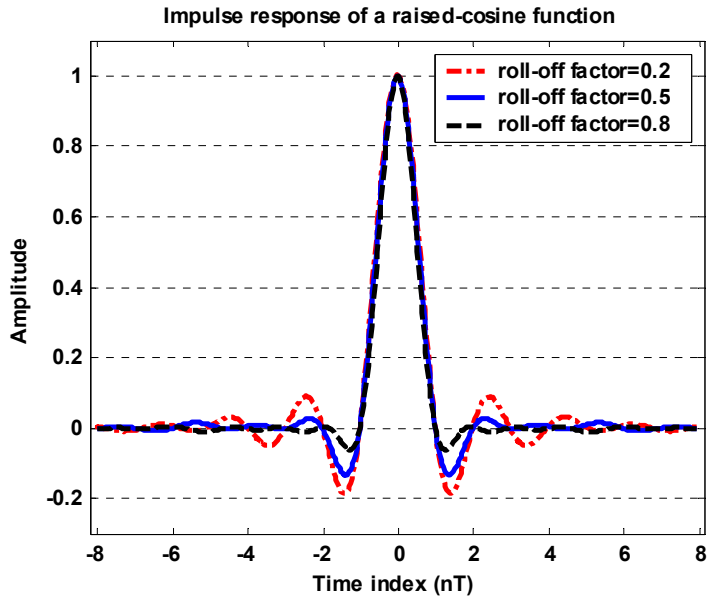


Fig. 4-5. Raised-cosine filter function impulse response with β = {0.2, 0.5, 0.8}

4-3-3 Butterworth Filter

The Butterworth filter is designed to have a frequency response that is as flat as mathematically possible in the passband. Butterworth has a slower roll-off, and thus require a higher order to implement a particular stopband specification. However, Butterworth filter has a more linear phase response in the passband than the Chebyshev and elliptic filters. Eq. (4-10) expresses a general form of a filter design.

$$f_{butterworth}(t) = L^{-1}\left\{\frac{B(s)}{A(s)}\right\} = L^{-1}\left\{\frac{b(1)s^{n} + b(2)s^{n-1} + \ldots + b(n+1)}{s^{n} + a(2)s^{n-1} + \ldots + a(n+1)}\right\} \qquad (4\text{-}10)$$

A 5th order of Butterworth filter is designed in this example so that the variable n in Eq. (4-10) is replaced with the number five. As a result, the corresponding transfer function has the following polynomials.

$$B(s) = \{0.022 \times s^2 + 0.122 \times s^4 + 0.244 \times s^3 + 0.244 \times s^2 + 0.122 \times s + 0.024\} \times 10^{-4}$$
$$A(s) = \{s^5 - 4.286 \times s^4 + 8.779 \times s^3 - 8.239 \times s^2 + 3.8697 \times s - 0.728\} \times 10^{-5} \quad (4\text{-}11)$$

This s-domain representation gives an impulse response as depicted in Fig. 4-6. A Butterworth does not guarantee a zero-crossing at a T-spaced location other than the main signal tap. So, an additional ISI is introduced in this filter, although the passband response performs linear and minimum ripple behaviors.

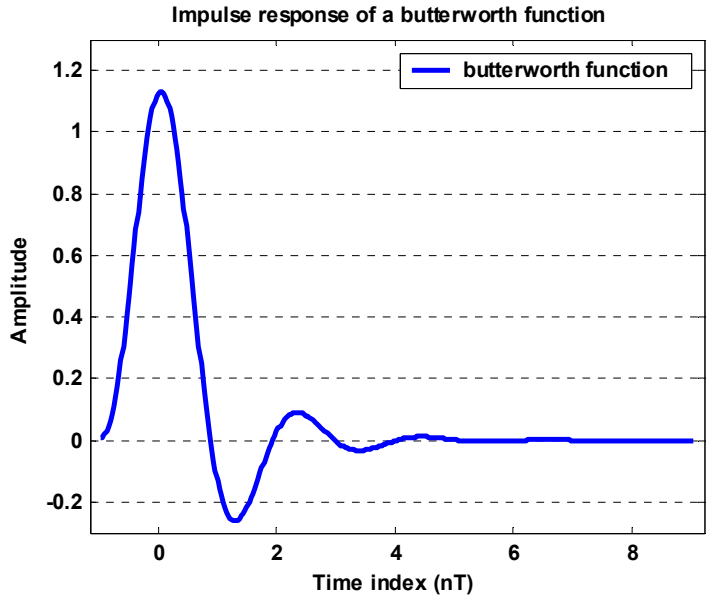


Fig. 4-6. Butterworth function impulse response

In the following, the filter responses take the mentioned sinc, raised-cosin, and 5th-order Butterworth filters for illustration. The DSTC algorithm is investigated from the main-tap and side-tap of those filters. The signal main-tap to the side-tap ratio is defined and maximized a

$$\varepsilon_{opt} = \arg \max_{\tau}\left(\frac{|f_{\varepsilon}[0]|^2}{\sum_{\substack{n=-\infty \\ n\neq 0}}^{\infty}|f_{\varepsilon}[n]|^2}\right) = \arg \max_{\tau}(SIR_{\varepsilon}) \tag{4-12}$$

where $f_{\varepsilon}[n]$ is the simplified notation from $f[(n-\varepsilon)T_s]$ and the ratio is the signal-to-ISI power ratio (SIR). Thus, the ε_{opt} is determined when the minimum ISI power sum appears in the denominator of Eq. (4-12). In other words, the SIR of the sampled signals becomes maximized when the optimum sampling instance is determined. Here, $f(t)$ is replaced by the filter impulse responses as shown in Figs. 4-4~4-6. A non-calibrated sampling timing error may yield low signal-integrity data even in the absence of noise, implying there is system performance degradation when sampling time is not well-calculated. The SIR response depends on the filter responses. Figs. 4-7~4-9 demonstrates the corresponding SIR curves from those corner filters (sinc, raised-cosine, and Butterworth filters). It is found that a sharper frequency response implies a better SIR curve performance. This is due to the faster convergence of the impulse response signal tails appeared as the side-lobes. In other words, fewer impulse tails contributes fewer interference taps. Consequently, a correct sampling position would provide excellent signal quality and overall performance. However, a sharper frequency response of a filter (implying fewer impulse response tails) requires higher order of a filter design, and thus requires high design cost. Accordingly, this SIR may be viewed as a design indicator that the system tradeoff between overall performance and filter design could be discussed in this way.

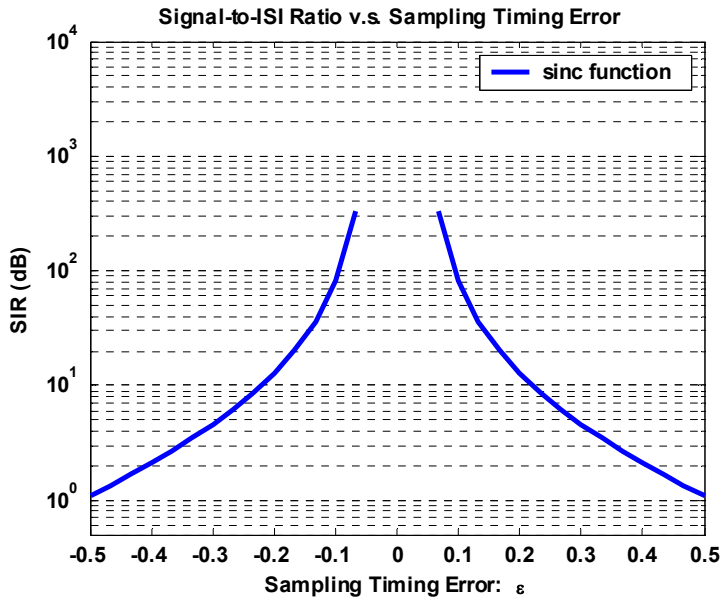


Fig. 4-7. The signal-to-interference-ratio (SIR) for a sinc function impulse resopnse

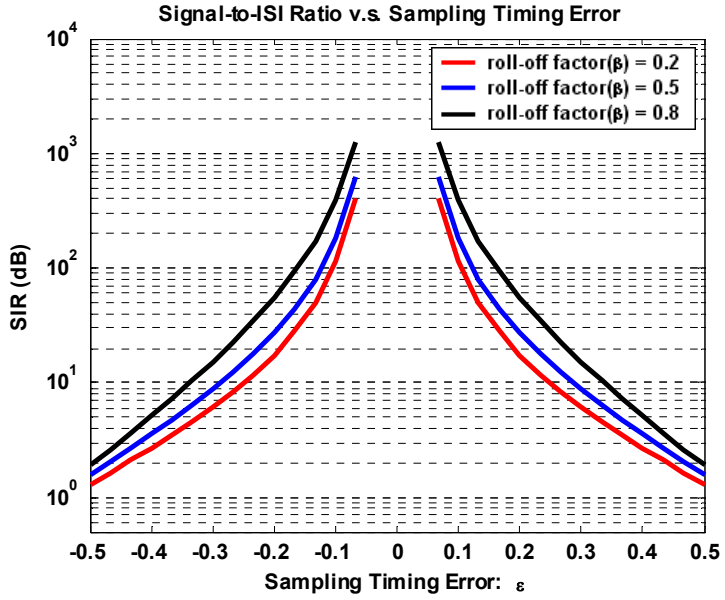


Fig. 4-8. The signal-to-interference-ratio (SIR) for a raised-cosine filter impulse response

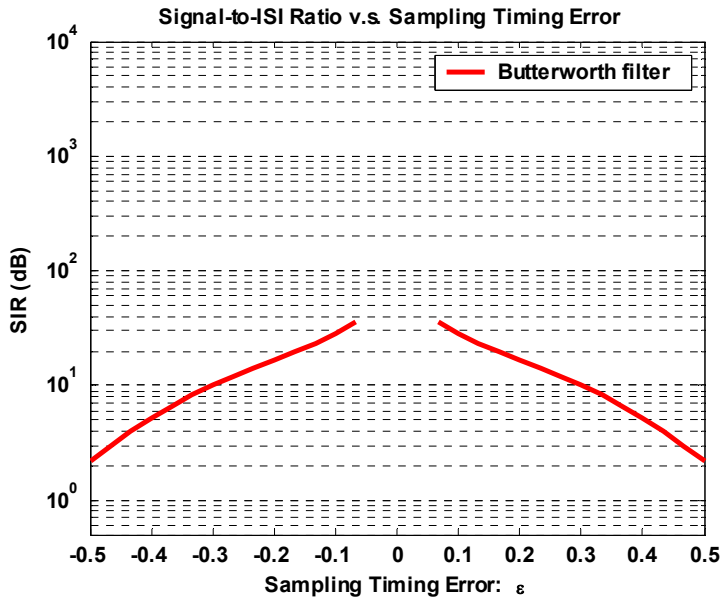


Fig. 4-9. The signal-to-interference-ratio (SIR) for a 5th-order Butterworth filter impulse response

To find the optimum sampling time ε_{opt}, the ratio given by Eq. (4-12) cannot be calculated directly because both the $f_T(t)$ and the $f(t) = f_T(t) * f_R(t)$ are unknown to any receivers. Therefore, an alternative approach, the maximum absolute-squared sum equivalent to Eq. (4-12) and also hardware realizable, is examined. Accordingly, the maximum absolute-squared-sum (MASS) of the received signals is

$$|r_\varepsilon[n]|^2 = |x_{R,\varepsilon}[n] + w_\varepsilon[n]|^2 \tag{4-13}$$

The expression is further described as

$$\left|x_{R;\varepsilon}[n]\right|^2 = \left|\sum_m x_{T;\varepsilon}[n-m] f_\varepsilon[m] e^{j(2\pi f_{CFO})(n+\varepsilon)T_s}\right|^2 + \left|w_{B;\varepsilon}[n]\right|^2 + 2\,\mathrm{Re}\left\{w_{B;\varepsilon}[n]\sum_m x_{T;\varepsilon}[n-m] f_\varepsilon[m] e^{j(2\pi f_{CFO})(n+\varepsilon)T_s}\right\} \tag{4-14}$$

where $w_{B;\varepsilon}$ is the band-limited zero-mean additive noise sampled at timing offset ε with $w_B = w(t) * f_R(t)$. The expectation of Eq. (4-14) is

$$E\left\{\left|x_{R;\varepsilon}[n]\right|^2\right\}=E\left\{\left|\sum_m x_{T;\varepsilon}[n-m]f_\varepsilon[m]e^{j(2\pi f_{CFO})(n+\varepsilon)T_s}\right|^2\right\}+E\left\{\left|w_{B;\varepsilon}[n]\right|^2\right\}+ E\left\{2\,\mathrm{Re}\left\{w_{B;\varepsilon}[n]\sum_m x_{T;\varepsilon}[n-m]f_\varepsilon[m]e^{j(2\pi f_{CFO})(n+\varepsilon)T_s}\right\}\right\} \quad (4\text{-}15)$$

Notably, $w_{B;\varepsilon}$ is assumed to be independent of transmitted signals, and the noise is a zero-mean random process with $E\{w_{B;\varepsilon}[n]\}=0$. So, the expectation of the cross term becomes zero.

$$\begin{aligned} & E\left\{2\,\mathrm{Re}\left\{w_{B;\varepsilon}[n]\sum_m x_{T;\varepsilon}[n-m]f_\varepsilon[m]e^{j(2\pi f_{CFO})(n+\varepsilon)T_s}\right\}\right\} \\ &= 2\,\mathrm{Re}\left\{E\{w_{B;\varepsilon}[n]\}E\left\{\sum_m x_{T;\varepsilon}[n-m]f_\varepsilon[m]e^{j(2\pi f_{CFO})(n+\varepsilon)T_s}\right\}\right\} \\ &= 0 \end{aligned} \quad (4\text{-}16)$$

Thus, the expected value of the received signals $x_{R;\varepsilon}$ is reduced to

$$E\{|x_{R;\varepsilon}[n]|^2\}=E\left\{\left|\sum_m x_{T;\varepsilon}[n-m]f_\varepsilon[m]\right|^2\right\}+\sigma_{B;w}^2 \quad (4\text{-}17)$$

where $\sigma_{B;w}^2$ represents the power of the color noise $w_{B;\varepsilon}$. The absolute-function operation suppresses the CFO factor. Therefore, the expected received signal power is composed of the transmitted signals filtered by the *f(t)* and the band-limited noise power. The effects of *f(t)* on the transmitted signals are expressed as main signal taps $f[n]|_{n=0}$ and their filter interference $f[n]|_{n\neq 0}$. Moreover, the expected power $E\{|x_{T;\varepsilon}[n]|^2|\}$ may be assumed to be a constant, say unit power, because every received signal power is adjusted by applying an automatic gain control (AGC) mechanism, thus normalizing the signal power to the dynamic range of the ADC. For simplicity, $E\{|x_{T;\varepsilon}[n]|^2|\}=1$ is defined. Accordingly, Eq. (4-17) becomes

$$E\{|x_{R;\varepsilon}[n]|^2\} = |f_\varepsilon[0]|^2 + \sum_{m\neq 0}|f_\varepsilon[m]|^2 + \sum_p \sum_{p\neq q} E\{x_{T;\varepsilon}[n-p]x^*_{T;\varepsilon}[n-q]\} f_\varepsilon[p] f^*_\varepsilon[q] + \sigma^2_{B;w} \quad (4\text{-}18)$$

Thus, Eq. (4-18) gives the summation of signal power, interference power, and cross-correlation term. This cross-correlation term can be expressed as

$$\begin{aligned} E\{x_{T;\varepsilon}[n-p]\cdot x^*_{T;\varepsilon}[n-q]\} &= E\left\{\sum_{k_1=0}^{N-1} X_T[k_1] e^{j\frac{2\pi k_1(n-p)}{N}} \sum_{k_1=0}^{N-1} X^*_T[k_2] e^{-j\frac{2\pi k_1(n-q)}{N}}\right\} \\ &= E\left\{\sum_{k_1=0}^{N-1} |X_T[k_1]|^2 e^{j\frac{2\pi k_1(q-p)}{N}}\right\} + \\ &\quad E\left\{\sum_{k_1=0}^{N-1}\sum_{\substack{k_2=2 \\ k_2\neq k_1}} X_T[k_1] X^*_T[k_2] e^{j\frac{2\pi[k_1(n-p)-k_2(n-q)]}{N}}\right\} \end{aligned} \quad (4\text{-}19)$$

Since X_T is the output symbol of BPSK, QPSK, or QAM, which is assumed to be i.i.d. variables with zero mean. The expectation $E\{X_T[k_1]X^*_T[k_2]|_{k_1\neq k_2}\}$ then reduces to zero. With the Parseval's theorem and the assumption $E\{|X_T[k_1]|^2\}=1$, it is inferred that $E\{|X_T[k_1]|^2\} = E\{|x_T[n]|^2\} = 1$ and is normalized to the ADC dynamic range. These information symbols are assumed to be independent, and then $E\{x_{T,\varepsilon}[n-p]x^*_{T,\varepsilon}[n-q]\} = E\{X_{T,\varepsilon}[k_1]X^*_{T,\varepsilon}[k_2]\}|_{k1\neq k2} = 0$. Therefore, Eq. (4-19) reduces to

$$E\{|x_{R;\varepsilon}[n]|^2\} = |f_\varepsilon[0]|^2 + \sum_{m\neq 0}|f_\varepsilon[m]|^2 + \sigma^2_{B;w} \quad (4\text{-}20)$$

Consequently, the expected absolute-squared value of the received signals is determined by the power of both the filter response and AWGN. Based on the SIR definition, Eq. (4-20) is rewritten as

$$E\{|x_{R;\varepsilon}[n]|^2\} = (SIR_\varepsilon + 1)\cdot I_\varepsilon + \sigma^2_{B;w} \quad (4\text{-}21)$$

where $I_\varepsilon = \sum_{m \neq 0} |f_\varepsilon[m]|^2$ is the interference power of the filter tail. A characteristic function (CF) of $E\{|x_{R;\varepsilon}[n]|^2\}$ is defined as

$$\text{CF} = (SIR_\varepsilon + 1) \cdot I_\varepsilon \tag{4-22}$$

A sharper CF curve is more easily recognized to calibrate the sampling timing errors. Fig. 4-5 plots a CF curve that corresponds to the raised-cosine filter of Fig. 4-4 in a noiseless channel. This finding reveals that the maximum $E\{|x_{R;\varepsilon}[n]|^2\}$ implies the optimum sampling instance ε_{opt}. Therefore, the ε_{opt} search based on the SIR curve in Eq. (4-12) is transferred to the search of the maximum $E\{|x_{R;\varepsilon}[n]|^2\}$, i.e.

$$\varepsilon_{opt} = \arg(\max E\{|x_{R;\varepsilon}[n]|^2\}) \tag{4-23}$$

According to the provided reference filter responses, the calculated absolute-squared sum of received signals in variant sampling offset can be depicted as following. The CF curves are the indicators for a receiver that the best sampling instance in each sample period is easy or difficult to identify. This indicator should be considered together with the SIR curve. A sharper SIR curve does not necessarily corresponds to a sharper CF curve. The design constraints are provided that the SIR is desired to be as flat and high as possible whereas the CF is sharper as possible. A sharper CF curves enables accurate calculation of best sampling instance for a receiver, and a high and flat SIR curve implies a miss-calculation of best sampling instance does not degrade the overall system performance too much. Figs. 4-10~4-12 illustrate the CF curves from different impulse responses. The proposed MASS calculation for the best sampling instance requires a sharper CF curve that is designed by the overall consideration of the system building block circuits. Moreover, the sharper CF curve

has larger noise immune capability that prevents the MASS computation from the disturbance from the noise.

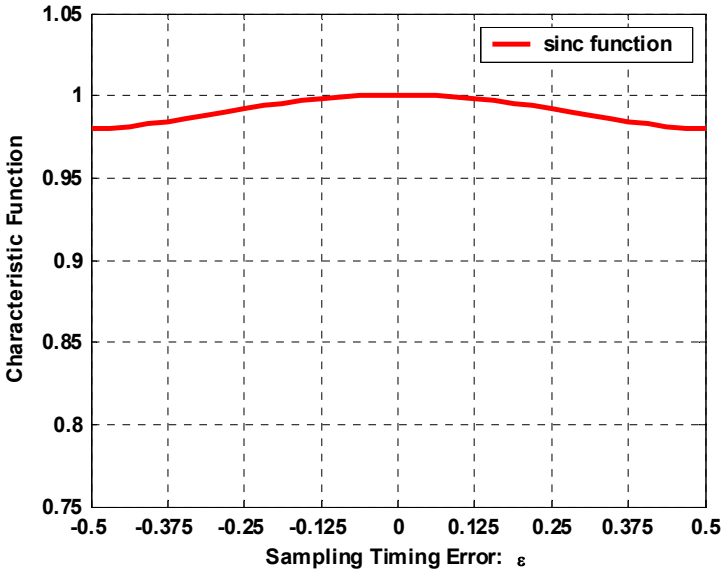


Fig. 4-10. Characteristic function of a sinc function

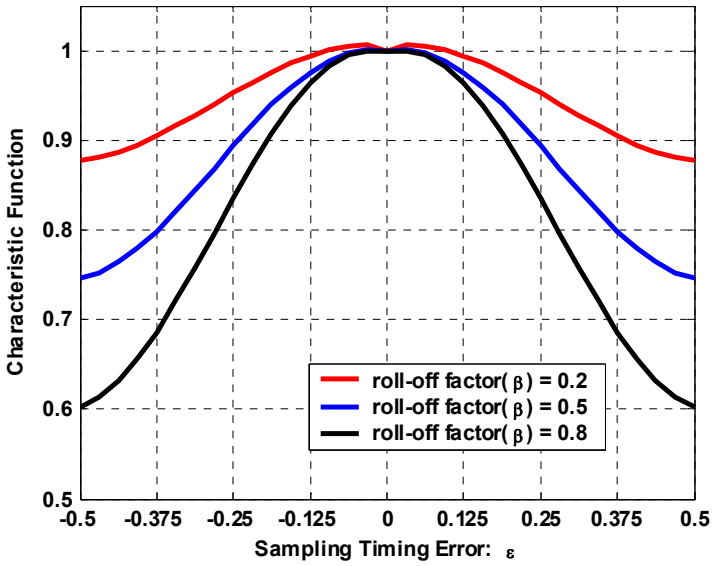


Fig. 4-11. Characteristic function of a raised cosine filter

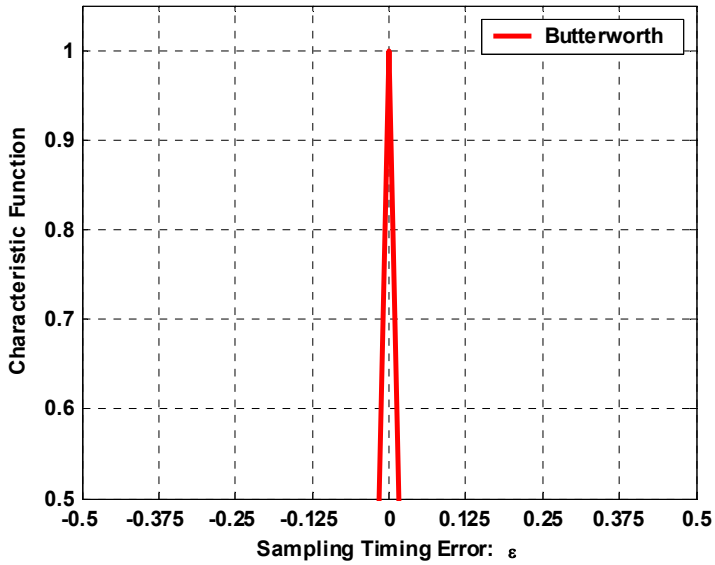


Fig. 4-12. Characteristic function of a 5th-order Butterworth filter

4-4 Simulation Results

The proposed DSTC and PTCG [38] are evaluated in a multi-band OFDM (MB-OFDM)-based UWB system [2] with a low-density-parity-check (LDPC) code for error correction [54]. The signal bandwidth is 528MHz with QPSK and OFDM modulations, and the maximum data rate 480Mbps is selected in the following simulations.

The frame format in each packet can be divided as the packet synchronization sequence (Packet Sync. Seq.), the frame synchronization sequence (Frame Sync. Seq.), the channel estimation sequence (Channel Est. Seq.), and the data OFDM symbols. Each OFDM symbol is transformed by 128-point inverse discrete Fourier transformation (IDFT). There is a time slot between every two OFDM symbols that does not transmit any information. This silent slot is used for each OFDM symbol to

change its transmission band frequency to another one. Accordingly, any change of controlling can be updated during this silent period as shown in Fig. 4-13.

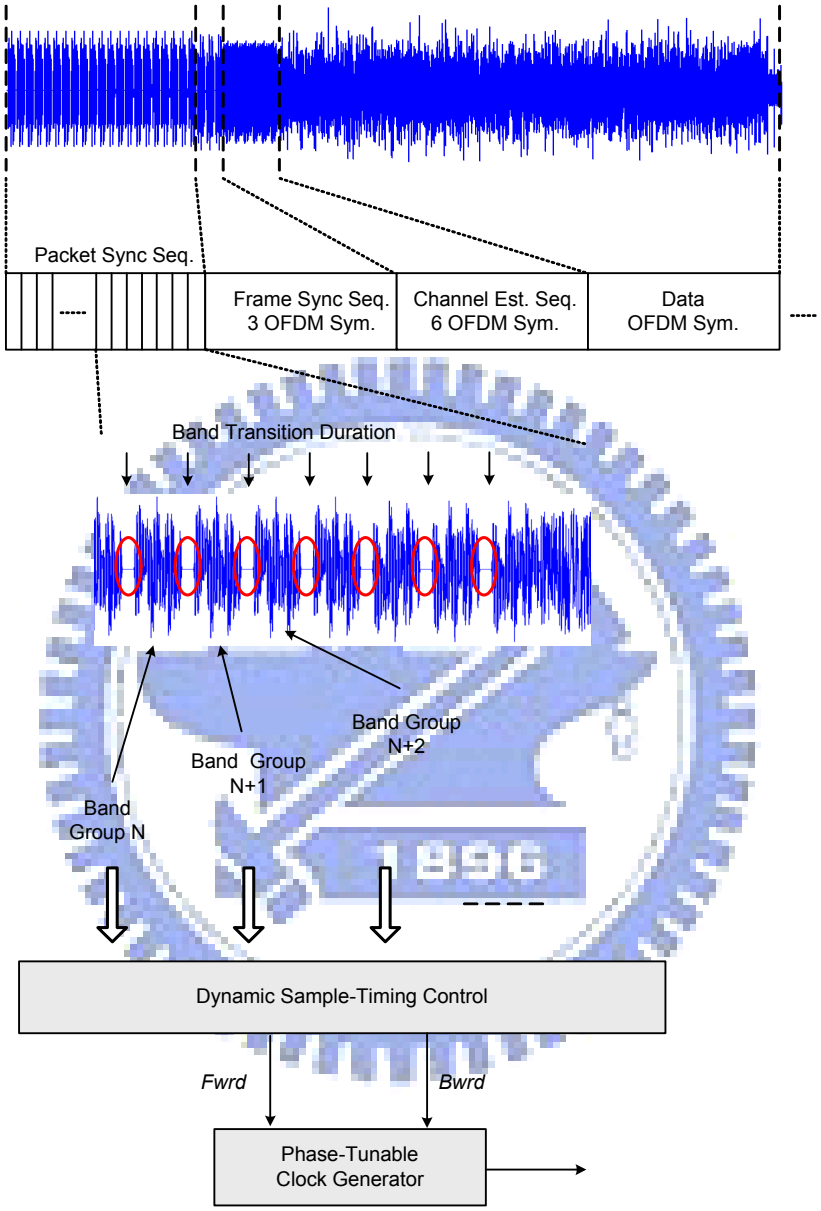


Fig. 4-13. Packet frame and waveform property for the DSTC operation

The dynamic timing-recovery starts the ε_{opt} search right after a packet is detected. Each packet is composed of 21 OFDM symbols at the beginning of each preamble frame (Packet Sync Seq), which is applied to the DSTC as shown in Fig.

4-14. With those 21 identical OFDM symbols in the packet sync sequence, each of which gives an absolute-squared sum, and the sampling time ε is changed in the time slots between OFDM symbols. In other words, the PTCG changes its output clock phase only during the time slots associated with band transitions such that signals in each OFDM symbol are sampled with the same clock phase within an OFDM block period as depicted in Fig. 4-14. This operation of DSTC corresponds to the flow shown in Fig. 4-15. In the band transition duration, the main function performs the PTCG update and sampling-instance shifting convergence. After the DSTC search process, the baseband starts the nominal signal synchronization and data decoding procedure.

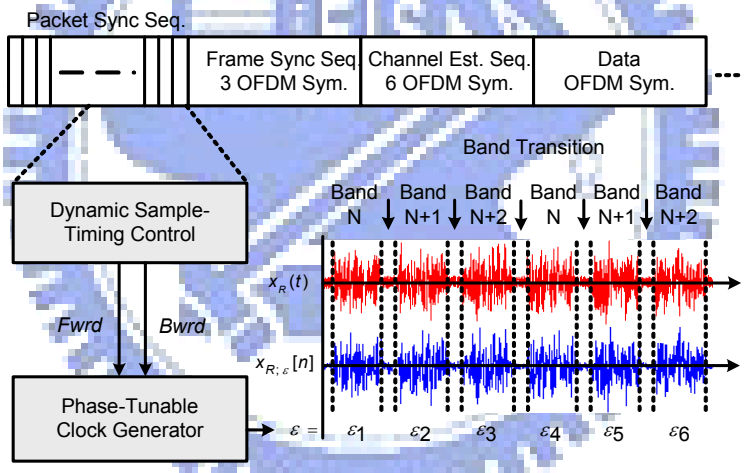


Fig. 4-14. Packet frame used for the DSTC computation

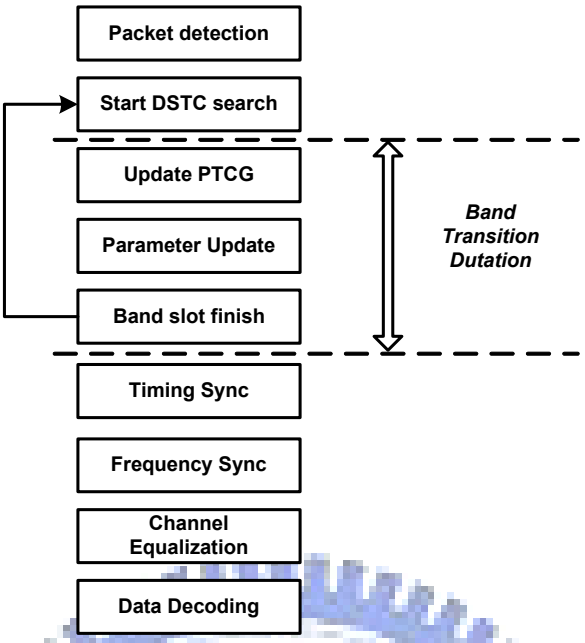


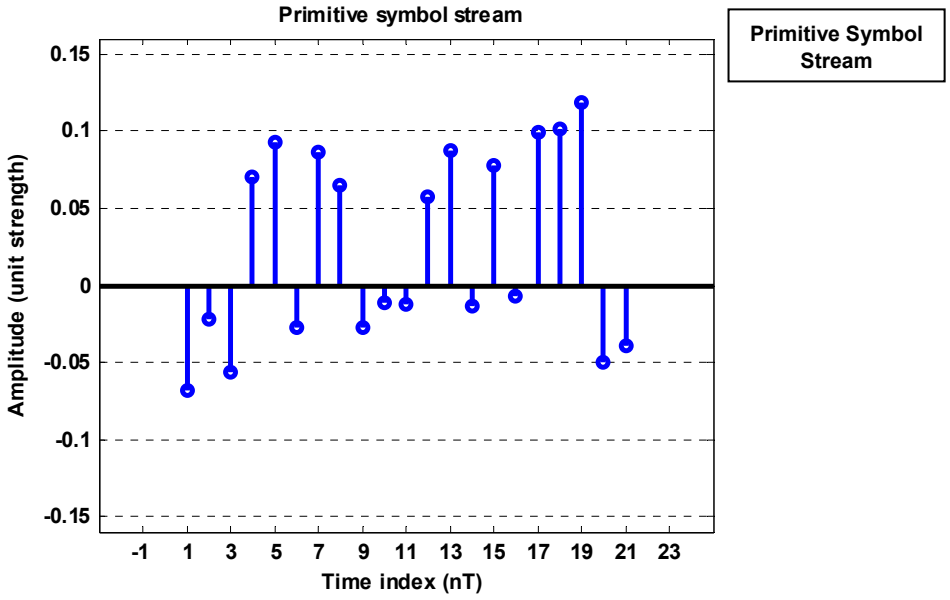
Fig. 4-15. The operation flow for the DSTC computation

The sampling error phenomenon is revealed only if the waveform is depicted in an analog-like method so that the sampling instance can be slightly shifter forward or backward to simulate the sampling uncertainty behaviors. In this part, the simulation flow and methodology for this DSTC algorithm are illustrated, as shown in Fig. 4-16. This also simulates and reflects the behaviors from the actual circuit operations.

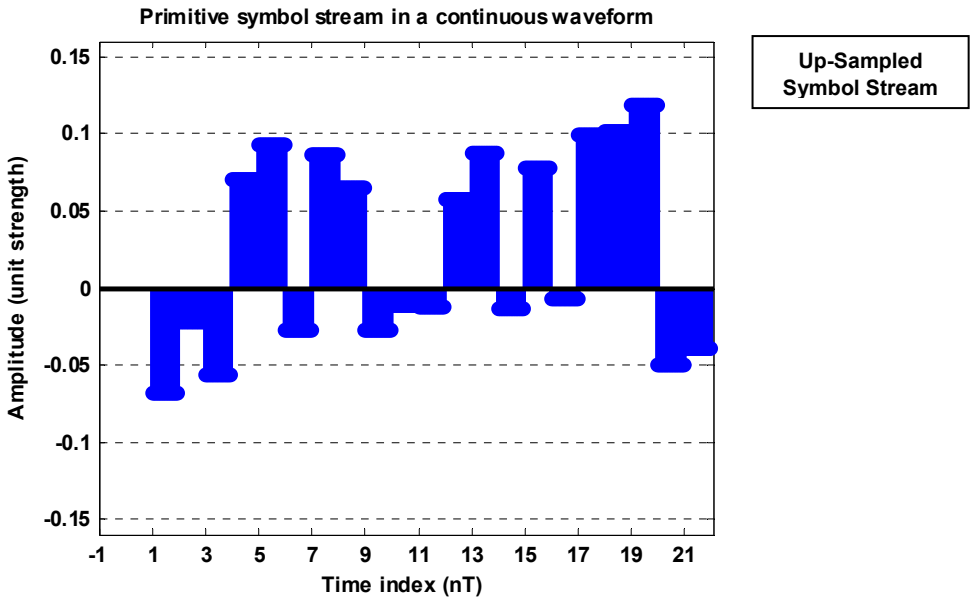
First, the samples after the baseband circuits, before the digital-to-analog conversion (DAC), are generated that constitute the primitive symbol stream. In actual circuit operations, the output of the baseband modulator is generated by the flip-flop circuits, so the symbol value lasts until next latching clock comes. Accordingly, each symbol is up-sampled to simulate the latch-and-hold phenomenon, as depicted in Fig. 4-16(b). Before the baseband digital signals are converted and transmitted to the receiver side, the equivalent filter response, including the DAC, RF-TX, channel, RF-RX, and the ADC circuits, has to be decided first. Usually, the system designers intend to give an

overall equivalent filter response equal to a raised-cosine filter response. From this point of view, this demo flow takes a raised-cosine filter response as an example. Note that the raised-cosine filter should be also sketched in the sampling rate that matches the one of the primitive symbol stream, as shown in Fig. 4-16(c). As a result, the signals are convolved with the equivalent filter impulse response as presented in Fig. 4-16(d). Then the colored noise is added to the signals in the receiver side.

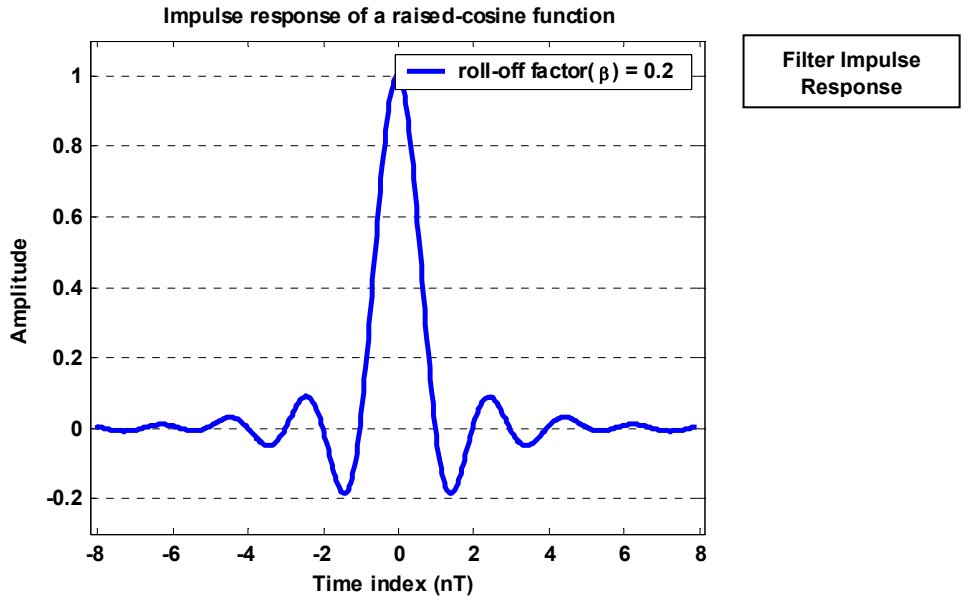
The signals before the ADC circuits are simulated in an analog-like waveforms. As a result, the system performance depends on the synchronization algorithm. Fig. 4-16(f)-(i) illustrate the down-sampled symbol stream using 1x symbol-rate down sampling, 2x and 4x symbol-rate down sampling. Moreover, the 1x symbol-rate down sampling also shows the sampling instance at the best and the worst sampling phases. Accordingly, the simulation flow and methodology allow the platform to simulate different down-sampling rate behaviors and also the sampling phase offset phenomenon.



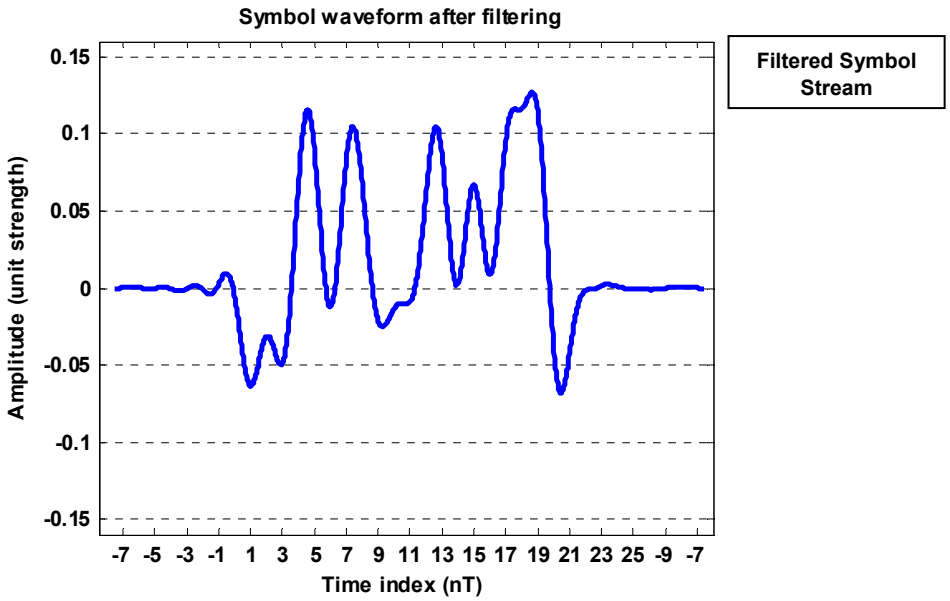
(a)


Primitive symbol stream in a continuous waveform
Amplitude (unit strength)
Time index (nT)
Up-Sampled Symbol Stream

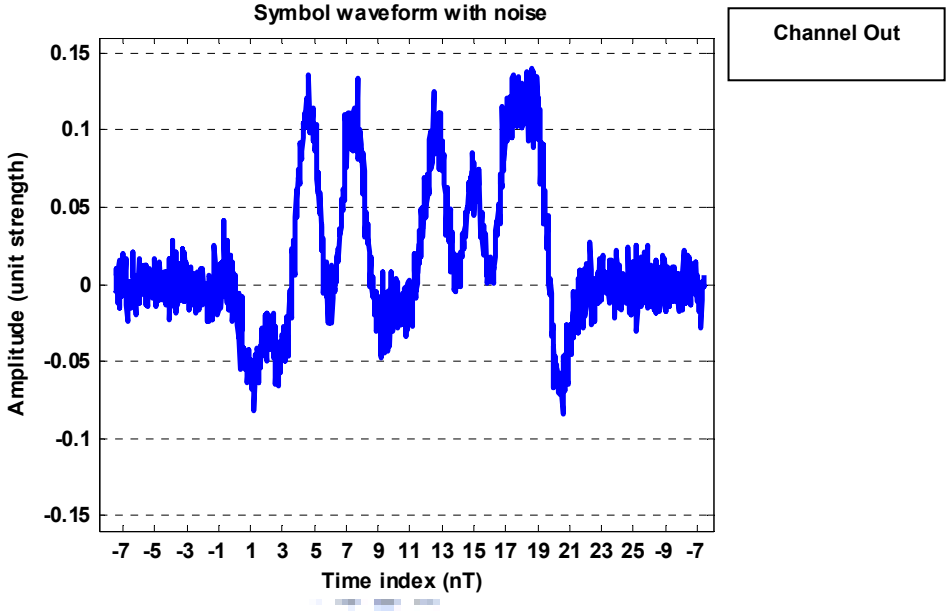
(b)


Impulse response of a raised-cosine function
roll-off factor(β) = 0.2
Amplitude
Time index (nT)
Filter Impulse Response

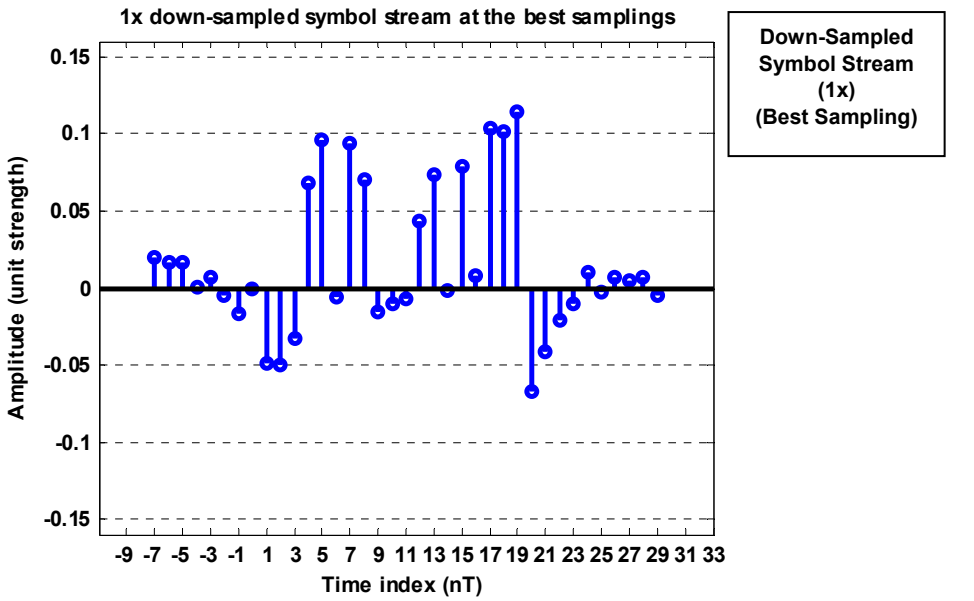
(c)


Symbol waveform after filtering
Filtered Symbol Stream
Amplitude (unit strength)
0.15
0.1
0.05
0
-0.05
-0.1
-0.15
-7 -5 -3 -1 1 3 5 7 9 11 13 15 17 19 21 23 25 -9 -7
Time index (nT)

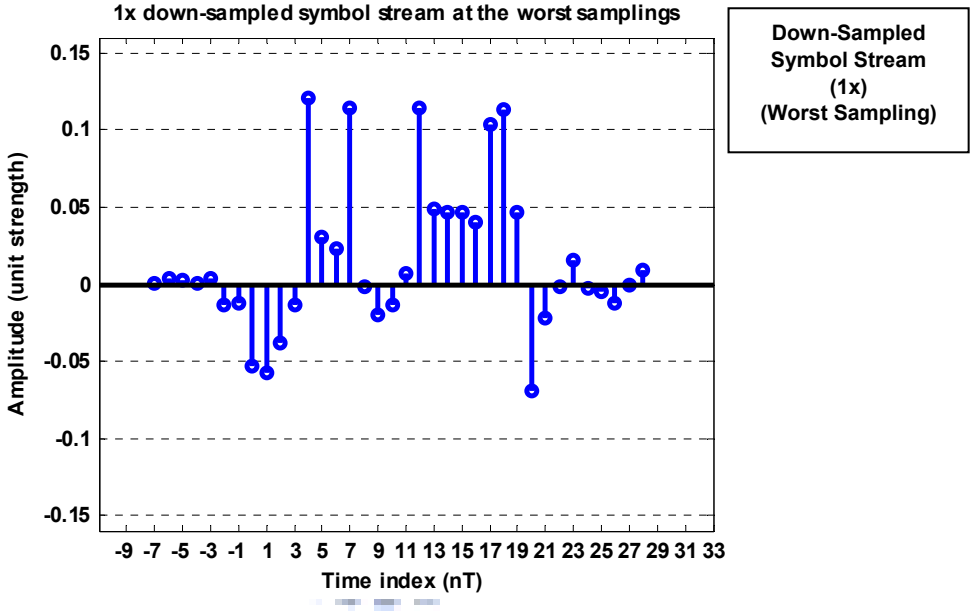
(d)


Symbol waveform with noise
Channel Out
Amplitude (unit strength)
0.15
0.1
0.05
0
-0.05
-0.1
-0.15
-7 -5 -3 -1 1 3 5 7 9 11 13 15 17 19 21 23 25 -9 -7
Time index (nT)

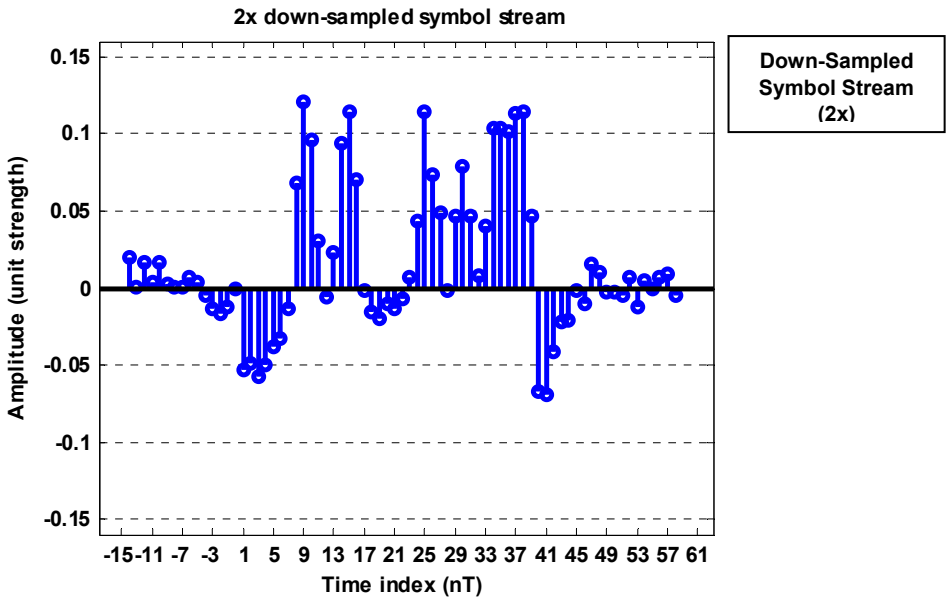
(e)


1x down-sampled symbol stream at the best samplings
Down-Sampled
Symbol Stream
(1x)
(Best Sampling)
Amplitude (unit strength)
0.15
0.1
0.05
0
-0.05
-0.1
-0.15
-9 -7 -5 -3 -1 1 3 5 7 9 11 13 15 17 19 21 23 25 27 29 31 33
Time index (nT)

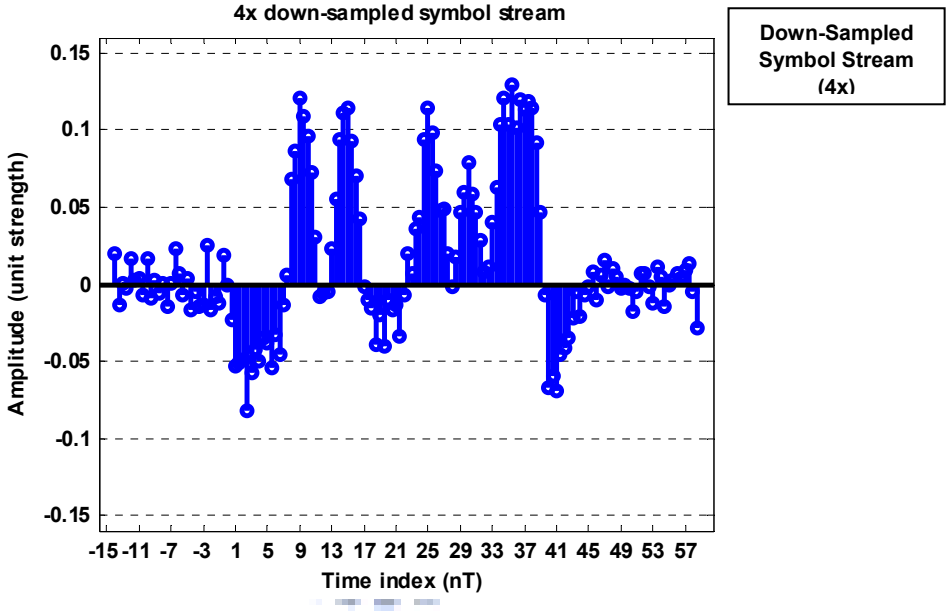
(f)


1x down-sampled symbol stream at the worst samplings
Down-Sampled
Symbol Stream
(1x)
(Worst Sampling)
Amplitude (unit strength)
0.15
0.1
0.05
0
-0.05
-0.1
-0.15
-9 -7 -5 -3 -1 1 3 5 7 9 11 13 15 17 19 21 23 25 27 29 31 33
Time index (nT)

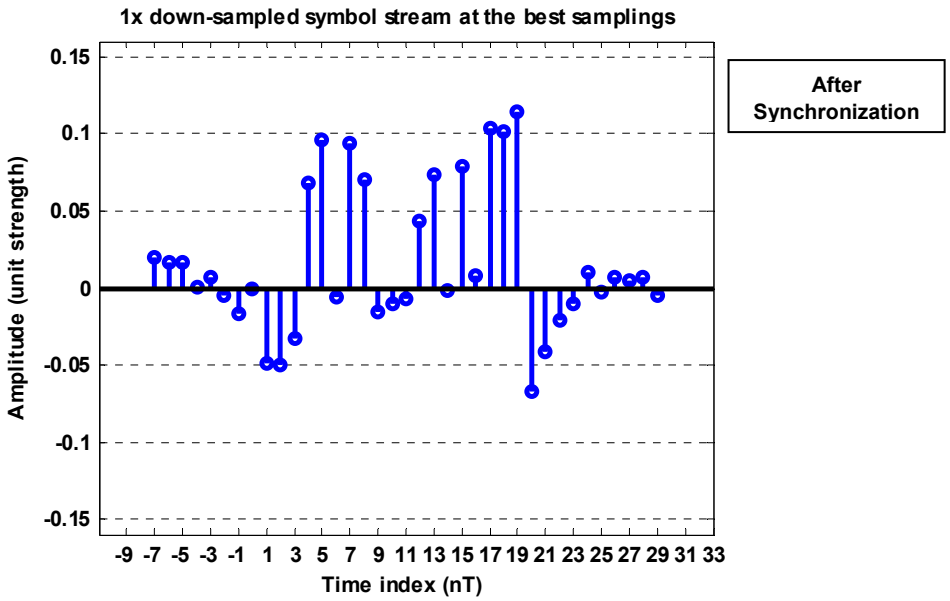
(g)


2x down-sampled symbol stream
Down-Sampled Symbol Stream (2x)
Amplitude (unit strength)
0.15
0.1
0.05
0
-0.05
-0.1
-0.15
-15 -11 -7 -3 1 5 9 13 17 21 25 29 33 37 41 45 49 53 57 61
Time index (nT)

(h)


4x down-sampled symbol stream
Down-Sampled Symbol Stream (4x)
Amplitude (unit strength)
0.15
0.1
0.05
0
-0.05
-0.1
-0.15
-15 -11 -7 -3 1 5 9 13 17 21 25 29 33 37 41 45 49 53 57
Time index (nT)

(i)



(j)

Fig. 4-16. The flow and methodology for DSTC simulations

Fig. 4-17 plots the overall system performance. The solid curve, s(ε), represents the SNR required to reach a packet error rate (PER) of 8%, where whole packets are sampled at a fixed and identical sampling offset ε. When the DSTC algorithm is applied, the optimal sampling instance is sought during the preamble. Before the end of the preamble, the DSTC decides which timing instance is the best for sampling in terms of system performance. Since the DSTC is operated in a noisy environment, it does not always choose the best sampling instance. Consequently, the dotted-curve, p(ε), represents the probability of the final decision made by the DSTC. The system with sinc function has a stable performance over every possible sampling instance phase. Since a sinc function has a transfer function equivalent to the rectangular filter in frequency domain, the added noise power level to signal power over the whole signal bandwidth is the same. In other words, the noise is equally applied to the signals in terms of spectrum domain. Therefore, a sampling error causes system performance degradation in terms of two factors. One is the mentioned SIR feature, and another is the noise level. In this evaluation case, the decoding process can be

achieved in the sub-5dB SNR level. The noise power in this level is much higher than the interference level. In addition, the noise is evenly applied to the signals, so the resulting system performances (required SNR at 8% PER) are almost the same with variant sampling timing error. Therefore, the SNR of the system required to reach PER=8% is given by

$$SNR_{PER=8\%} = \int_{-0.5}^{0.5} s(\varepsilon) \cdot p(\varepsilon) \cdot d\varepsilon \tag{4-24}$$

It is also found that this probability function is correlated to the characteristic function derived in the proposed DSTC section. Although a sinc function condition does not provide clear characteristic to identify which instance is the best for signal sampling, the stable system performance has little impact due to the sampling error.

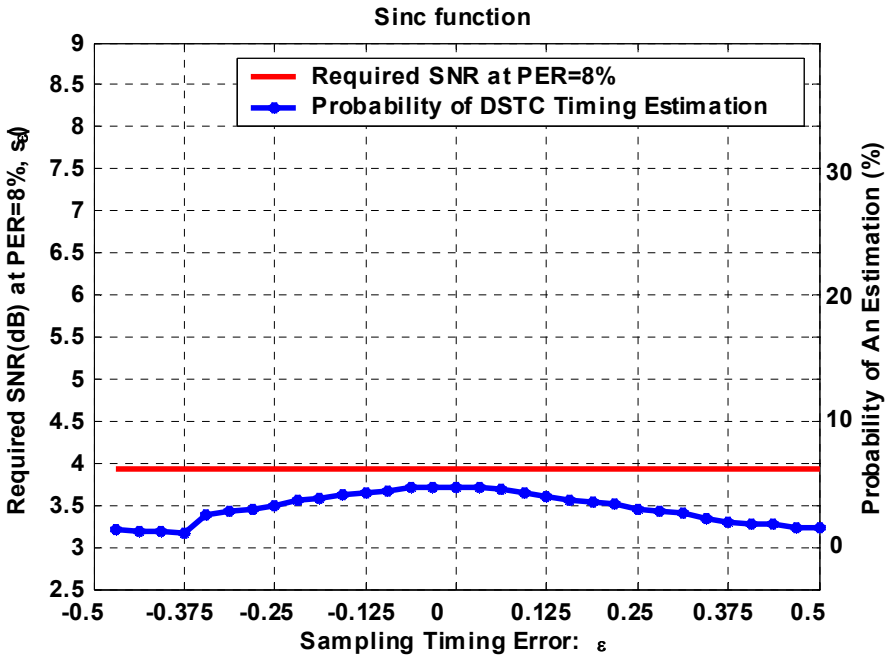


Fig. 4-17. System performances on a corresponding sampling instance and the determined sampling-timing probability with DSTC algorithm in the sinc function condition

The same simulation conditions are applied with only the filter changed to a raised-cosine filter with roll-off factor 0.2~0.8. The resulting performance with variant sampling error is depicted in Figs. 4-18~4-20. The one with Butterworth filter is illustrated in Fig. 4-21. A larger roll-off factor implies a filter with less sharp frequency edge response. This causes the sideband signals more easily interfered by AWGN noise. In the time-domain expression, an inaccurate sampling instance will not only be abrupt by filter interference but also suffer from more noise power. Consequently, the largest roll-off factor filter provides the most performance difference in the best and worst sampling instances as shown in Fig. 4-20. Moreover, the best sampling in this case suffers from the least noise, including the filter interference and AWGN noise. This implies that an incorrect sampling position has a large amount noise power added to the signal, although the overall signal power to the noise power ratio is the same in the scope of a packets. The probability to determine the proper sampling instances can be also found in the same figure with the dotted curve. As in the previous discussion on the characteristic function, the system with roll-off factor 0.8 provides the most obvious difference on the characteristic function, so the resulting probability curve as shown in Fig. 4-20 dotted curve is also correlated to the characteristic function. It is found in this case that the most probably calculated sampling phases provides the best system performance, i.e. the smallest SNR to reach 8% packet error rate. The case with a Butterworth filter has a performance promising the similar results, except the performance curve difference on different sampling instance and the calculated best sampling instance probability curve.

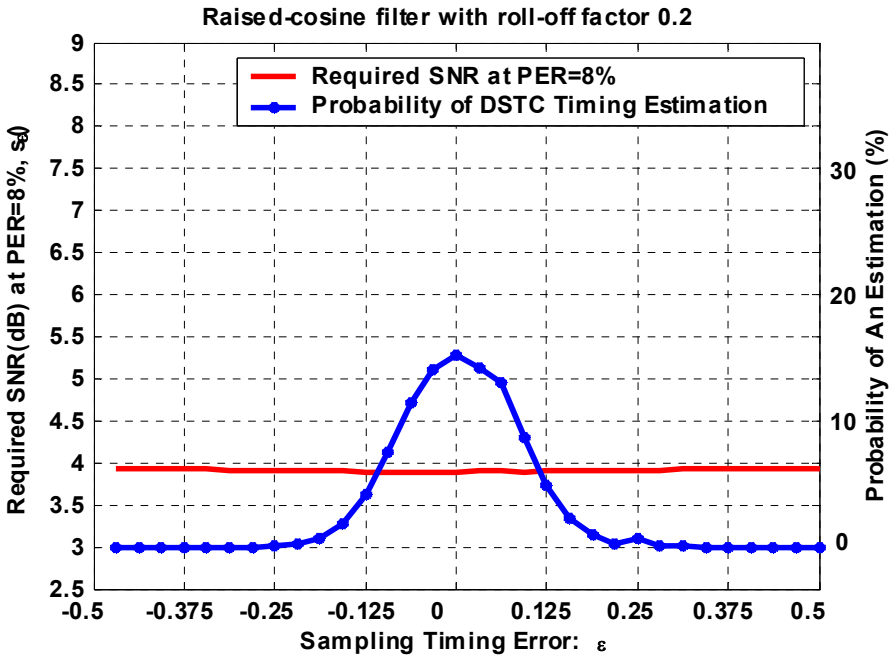


Fig. 4-18. System performances on a corresponding sampling instance and the determined sampling-timing probability with DSTC algorithm in the RC function condition

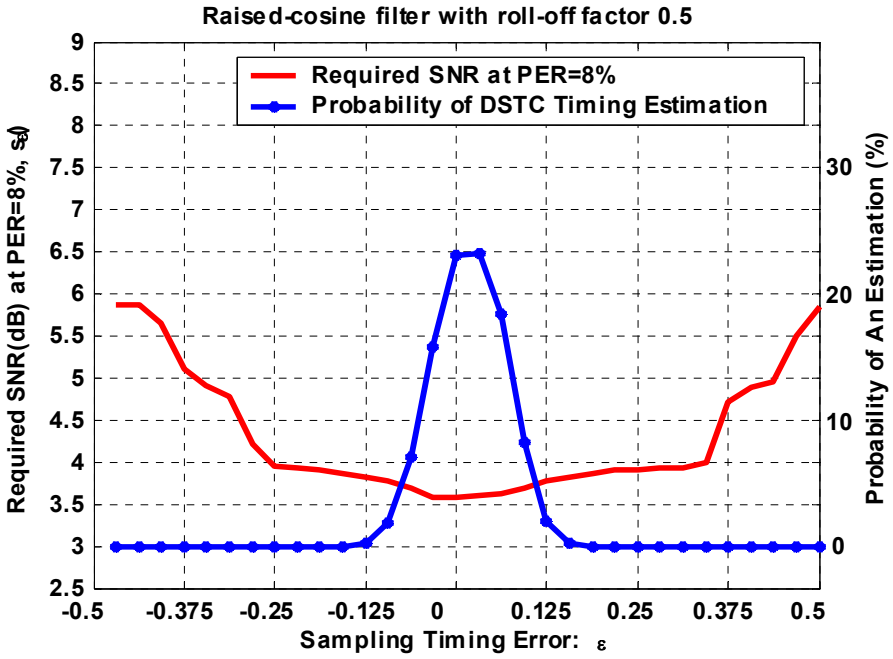


Fig. 4-19. System performances on a corresponding sampling instance and the determined sampling-timing probability with DSTC algorithm in the RC function condition

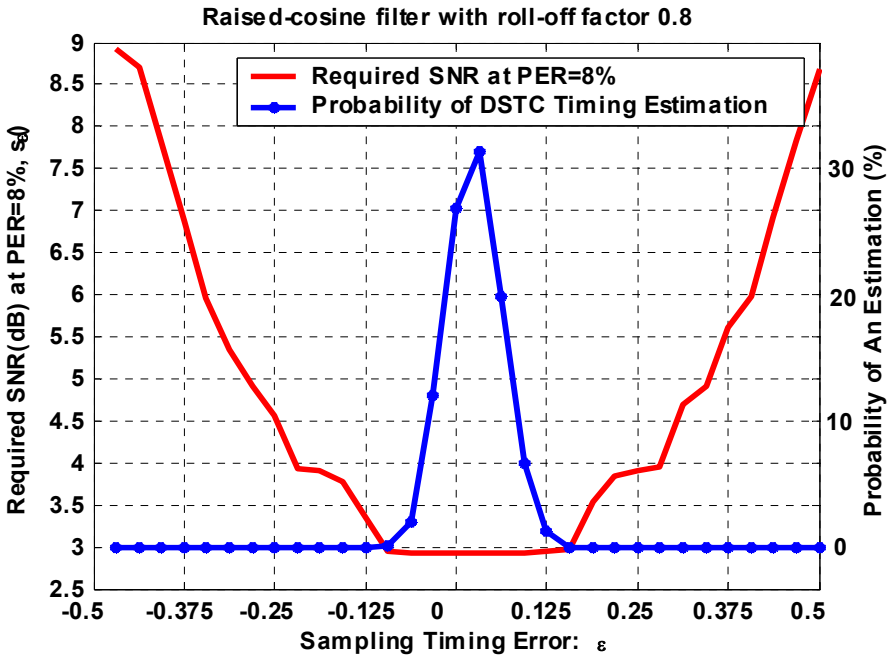


Fig. 4-20. System performances on a corresponding sampling instance and the determined sampling-timing probability with DSTC algorithm in the RC function condition

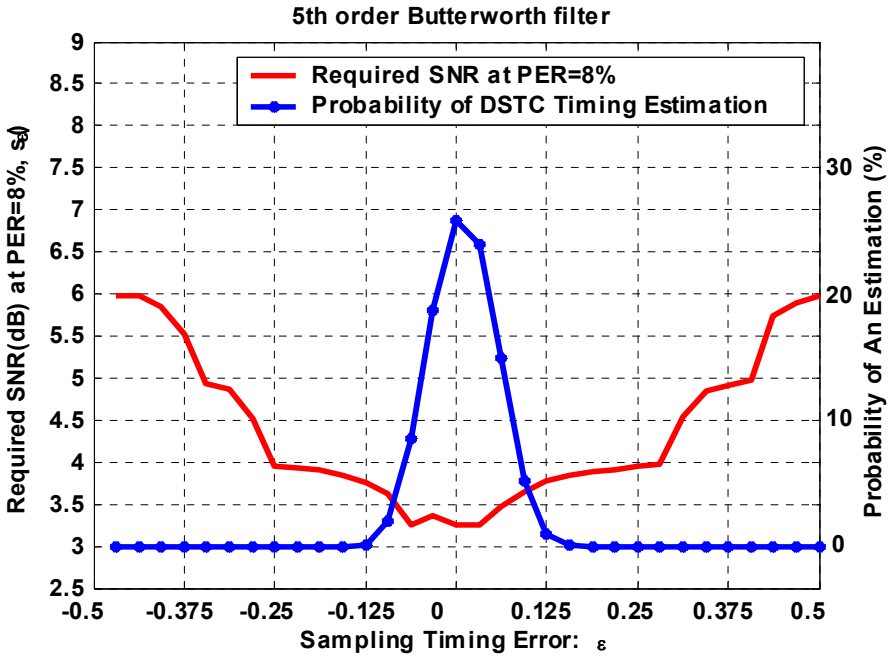


Fig. 4-21. System performances on a corresponding sampling instance and the determined sampling-timing probability with DSTC algorithm in the Butterworth function condition

Figs. 4-22 and 4-23 shows an example of the decoded QPSK symbol constellation with the best and worst sampling instances, respectively. The evaluation

case applies a raised cosine filter with roll-off factor 0.5 at SNR 7dB for clearer performance recognition. The best-sampled constellation in Fig. 4-22 has much more condensed signal distribution than that in Fig. 4-23 from the worst signal samplings.

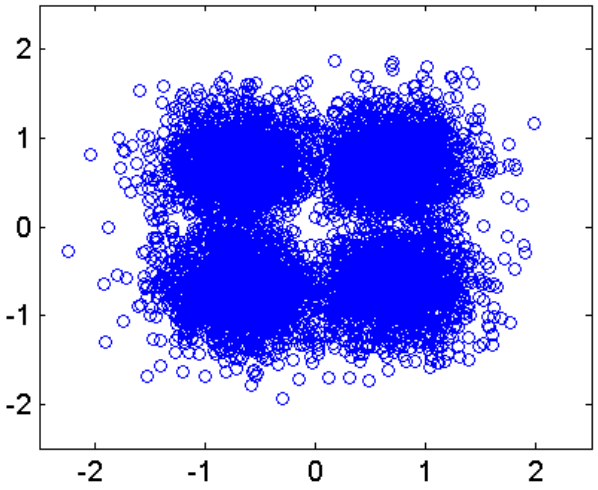


Fig. 4-22. The decoded QPSK symbol constellation with the best sampling instance in β=0.5 raised-cosine filter condition

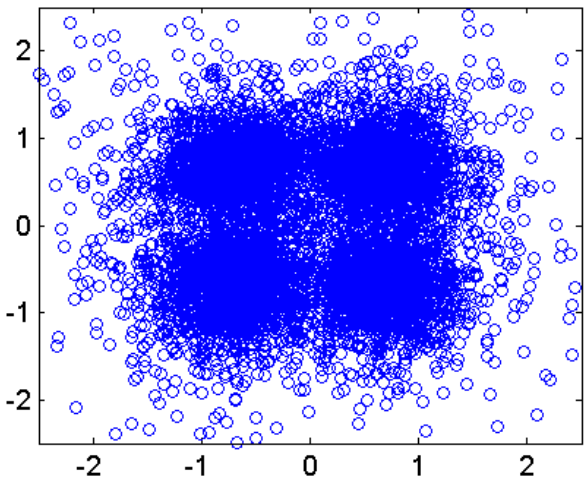


Fig. 4-23. The decoded QPSK symbol constellation with the worst sampling instance in β=0.5 raised-cosine filter condition

The system performance is illustrated in Fig. 4-24 using a two-time interpolation scheme. The interpolation is achieved by taking twice samples with signals averaged, and is then proceeded by the data decoding. The sampling phase is simulated by 32 possible partitions. The simulated phase is fixed at a certain value as an initial phase. Then the rest of the packet is decoded by the identical phase position. So, the overall performance is done by taking the initial phase pair of {ε/T, (ε/T+1/2T)} with ε=0, 1/32, 2/32, …, 15/32. The equivalent system filter is also assumed with the reference filters, i.e. sinc filter, raised-cosine filter, and Butterworth filter. The simulated system performance is shown in Fig. 4-24. Since the sampling phase over a packet is fixed and the selected initial phase is a random variable, it is reasonable to assume the targeted initial phase as a uniform distribution. Accordingly, each performance curve in Fig. 4-24 comes from the averaged performance with equally probably initial phase. The system with sinc filter and low roll-off factor raised-cosine filter provide better packet error rate performance. This is due to the two-time sampled signals that can average and reduce the noise power level for a better signal quality decoding. On the contrary, the performance with the roll-off factor 0.8 raised-cosine filter requires 4.59dB SNR to reach the acceptable performance. The interpolation in this case does not benefit because the other additional sample signal may contribute unnecessary interference or noise on the original desired signals, and the additional interference or noise may have much more power level that can not be averaged even two or more samples are taken together. Note that this performance is the result from the expectation value. This implies that the performance in a specific sampling phase may result in a smaller SNR value than 4.59dB to reach the required performance, but this also implies that most of the cases require more than 4.59dB for the corresponding system performance. Although the resulted system curve is the outcome in average, it

reflects a fact that the system performance is not robust and not stable due to the variation in the performance.

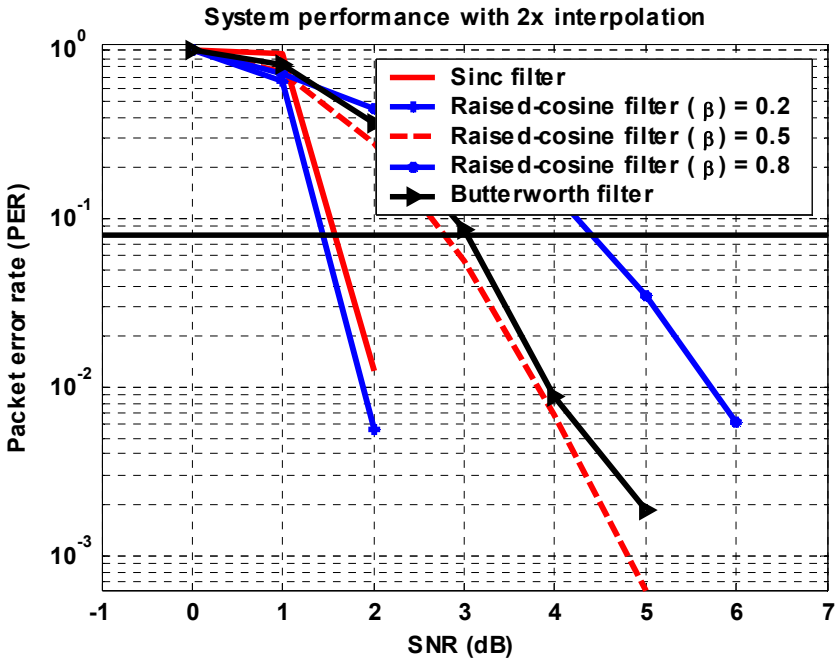


Fig. 4-24. System performance with 2-time interpolation scheme

Table 4-1 summarizes the required SNR value to reach a 8% PER level in terms of the proposed DSTC and the 2x interpolation approach. If the equivalent system filter is an ideal sinc function, the required SNR with DSTC performs worse than that with interpolation. With reasonable system filter designs, say a 0.5 roll-off factor, the proposed DSTC has only about 0.69dB SNR loss with only half sampling frequency and a robust and stable system decoding performance. When a 0.8 roll-off factor is applied to the system design, the system with DSTC outperforms that with interpolation. The DSTC provides a stable decoding performance with 2.92dB SNR to reach 8% PER, but the interpolation only requires higher SNR values but also has poorer system stability. Another example with Butterworth has an about 0.3dB SNR loss for the tradeoff among sampling frequency, system stability, and system

performance. The discussion on the power consumption with the reduced sampling frequency may be further directed to chapter 6 for detailed illustration.

TABLE 4-1. SYSTEM PERFORMANCE SUMMARY WITH DSTC AND 2X INTERPOLATION

Equivalent Filters	SNR with DSTC (dB)	SNR with 2x interpolation (dB)
Sinc	3.9251	1.93
Raised-cosine (β=0.2)	3.8948	1.89
Raised-cosine (β=0.5)	3.6166	2.9
Raised-cosine (β=0.8)	2.9244	4.59
Butterworth	3.3418	3.02

In hardware realization, there is finite resolution for controllable sampling timing. So, a sub-optimum ε_{subopt} solution of Eq. (4-23) can be expressed by

$$\varepsilon_{subopt} = \left.\frac{kT_s}{l}\right|_{k=K_{opt}} = \arg \max_{\substack{k=0\sim(l-1)\\ l\in\square}} \sum_{n=0}^{N-1} \left| r_{kT_s/l}[n] \right|^2 \tag{4-25}$$

where N=128 in the case of MB-OFDM UWB. This means how close ε_{opt} and ε_{subopt} can be is limited by the hardware finite resolution. The value of variable l determines three important tradeoffs: (i) the performance loss when an incorrect $\varepsilon_{subopt,err}$ is made with a non-zero offset index.

$$\varepsilon_{subopt,err} = \varepsilon_{subopt} - \hat{\varepsilon} = (K_{opt} + offset)T_s / l \tag{4-26}$$

where $\hat{\varepsilon}$ is the final decision; (ii) the PTCG hardware capability giving a lead or lag clock phase offset with resolution T_s/l; (iii) the necessary number of OFDM symbols for the MASS search. So, any clock sampling error may introduce some SNR losses at 8% PER. In the following, the discussion will determine the required clock tuning phases according to the three design constraints (or tradeoffs).

(a) Allowable performance loss

The determination of phase number results in different system performances. When only a single clock phase is available for selection, it depends on probability to sample a signal at the best sampling instance. This presents a large variance of system performance and results in unstable link quality of wireless transmission. On the other hand, it is also possible to design a clock source that provides as many phases as possible for selection to drive the sampling circuit. Therefore, the best sampling instance can be obtained when the sampling position is well-calculated. However, a large number of provided PTCG phases largely increase the difficulty in designing the clock source, especially in the high-speed applications. Accordingly, the tradeoff exists between the design challenge of the PTCG circuits and the allowable of system performance loss. This relationship between the PTCG phase number and the corresponding SNR to reach an 8% packet error rate is illustrated in Fig. 4-25. The simulation condition applies a raised-cosine filter with roll-off factor 0.8 as the equivalent filter responses. This filter results in the best and worst performance SNR=2.92 and SNR=8.93, respectively, at PER=8% as shown in Fig. 4-20. In average, it is found that a single phase provided by the PTCG provides an expected SNR=4.82dB for PER=8%. When the PTCG is designed in 32 phase number, a required SNR is 2.92dB to this performance level. However, it is not necessary to design so many phases since a phase number 8 provides almost similar performance level as that with 32 phases. If fewer number than eight will result in an increased performance loss, the PTCG is designed with the phase number eight, providing a reasonable performance loss with only 0.1dB SNR. This also enables the capability in the PTCG circuit designs in a high speed system such as MB-OFDM UWB system.

Accordingly, this measures the necessary PTCG phase number when designing the DSTC algorithm accompanied with the PTCG circuit design.

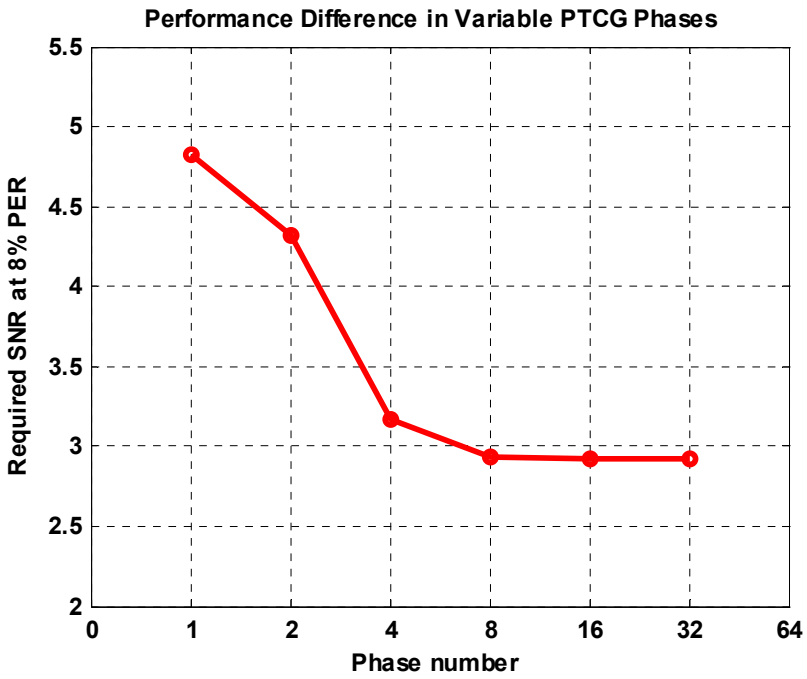


Fig. 4-25. Resulted system performance in variant PTCG phase number

(b) PTCG hardware design capability

The PTCG design includes a phase-locked loop (PLL) and a multi-phase generator (MPG). The PLL has the role of generating a clock source with required driving frequency. Then, the MPG further takes the definite frequency source for multiple phase generations so that each clock phase is equally separated in timing domain. Those circuits are designed and implemented in an all digital cell-based approach, including both of the all-digital PLL (ADPLL) [53] and the all-digital MPG (ADMPGC) [53]. So, the output frequency is generated by concatenating delay cells to target the required frequency. Then the delay cells dominate the frequency accuracy and the possible ADMCG phase separation resolution. In other words, the

number of separation phases in each clock period will be dominated by the delay cell property. In the MB-OFDM UWB system, the signal bandwidth is 528MHz. So, the baseband clock frequency should be no less than 528MHz (no more than 1.89ns in period). The delay cells from the standard-cell library have the fundamental inverters as delay cells that have a delay in the order of 100ps. Considering the process-voltage-temperature (PVT) variations, the delay may be scaled to twice or half, so the fundamental inverter delay may range from 50ps~200ps for every possible operation condition. In the evaluation of proper number of clock phases in each period, the upper bound of ADMCG phase number is eight if a power-of-two phase number is taken into considerations, so each phase is separated by 1.89ns/8=236.25ps. When 16 phases are designed, each phase will be spaced by 1.89ns/16=118.37ps. This exceeds the resolution that can be provided by a fundamental inverter cell. Consequently, the PFTCG will take an 8-phase design for the clock generation in the point of view of hardware implementation.

(c) Necessary OFDM symbols for DSTC convergence

The computation of MASS value will determine the alternation direction of the PTCG clock phase. The search of the best sampling search can be achieved by a linear or binary approach. A linear search is done by exhausted computation of each OFDM symbol for the MASS comparison so that the PTCG clock phase approaches the forward or backward step by step. In other words, an exhausted best sampling search requires a total of l OFDM symbols for energy computation if a total of l PTCG phases are designed. On the other hand, a binary search of the best sampling instance is done by taking M/2 phase step for timing search, where the M is the phase number

of remaining unsearched phases on a specific moving direction. The binary search requires $\log_2(l)$ steps for the best timing allocation.

In the exploration of the required sampling resolution, the worst condition should be the case for discussion. So, the best sampling timing search is assumed to be applied with the linear search of the most time-consumed algorithm. In the MB-OFDM UWB evaluation platform, the preamble used for the DSTC search is the 21-repeated sync preamble. Conventionally, the 21-repeated synchronization preamble is used for the automatic gain controlling, packet detection, carrier frequency offset estimation and compensation, etc. This implies that some of those 21 preamble symbols are used for the baseline timing synchronization and frequency synchronization. Therefore, a reasonable estimated remaining preamble symbols can be half of the total symbol number, i.e. 21/2 = 10.5 preamble symbols. In other words, the design PTCG phase resolution should be no more than 10.5, otherwise the linear search of DSTC timing search will fail to work. In this reference design, the suggested number of PTCG resolution would be eight according to this design constraint.

From the three mentioned design constraints, tradeoffs and the overall system performance profile, it is proper to divide each clock period into 8 controllable clock phases, i.e. l=8, because this sampling phase number results in reasonable SNR improvement or loss. Also, a clock resolution in this high frequency rate is shown to be realizable [53]. In timing error searches, there are sufficient 21 OFDM symbols for 8-phase MASS computation. In other words, the maximum absolute-squared-sum can be always found within 8 searches in this case.

Each sample period is planned to be divided into eight phases, for example, as shown in Fig. 4-26, for the finite hardware resolution and limited CF value degradation.

Therefore, the optimal sampling timing from these eight positions always corresponds to a CF value that approaches the maximum value.

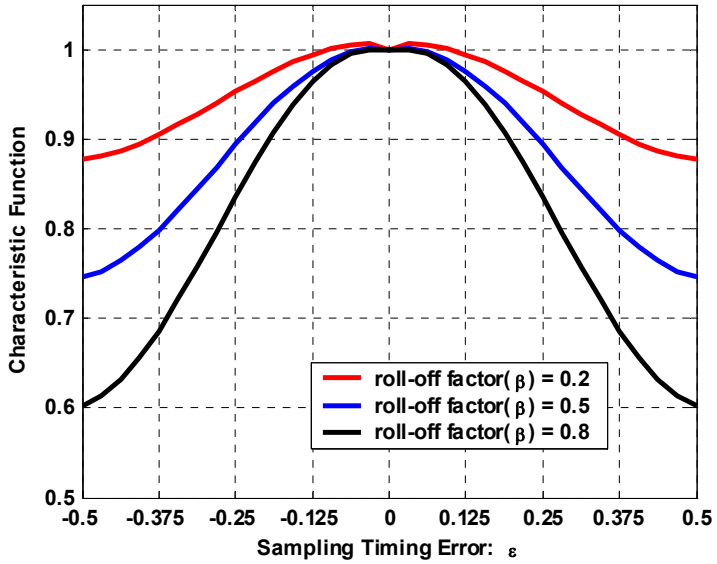


Fig. 4-26. CF function to the corresponding sampling timing error

4-5 Summary

This chapter proposes the dynamic sampling-timing control scheme to search the best sampling instance with reduced sampling frequency, signal symbol rate. For the corner case evaluations, the sinc function, raised-cosine with roll-off factor 0.2~0.8, and Butterworth are applied for the system performance illustrations. A characteristic function is utilized as a indicator function for the proper sampling position search. The simulation results reveal that the DSTC with symbol-rate sampling can outperform the interpolation scheme under the β=0.8 rasied-cosine filter environment. Considering the finite hardware resolution, it is shown that each sampling period can be divided into eight phases for the best sampling instance selection. With the other

corner filter conditions, a reasonable SNR loss can be regarded as the implementation loss whereas a more robust and stable system is obtained with the DSTC algorithm at reduced sampling frequency.

Chapter 5:

All-Digital Hysteresis-Based Clock Generator

5-1 Background and Overview

A clock generator stays active all the time because digital signal process requires clock trigger edge for computation. This circuit usually remains active even if a system is not in operation. An always-on operation implies that circuit continuously consumes both of the dynamic and static power. As the power from data computation and signal transformation is getting lower and lower, the amount of clock-generation power becomes obvious. State-of-the-art clock generators with analog design approaches consume the power in the order of 1mW to 10mW with large area occupation and poor process portability. Although the (cell-based) digital clock generator provides a reduced power, it still remains a power higher than 100μW. This disables portable devices for long-duration applications.

Accordingly, this chapter addresses a low-rate clock source design with an all-digital circuit approach in the sub-100μW power consumption. A clock source requires variable delay generation elements, and this hysteresis-based clock generator focus on the delay cell innovation in the architecture and circuit level improvement. The design goals of those delay elements are to provide a variable propagation delay elements with most economic area and power consumption. The role of this hysteresis clock generator is introduced as shown in Fig. 5-1.

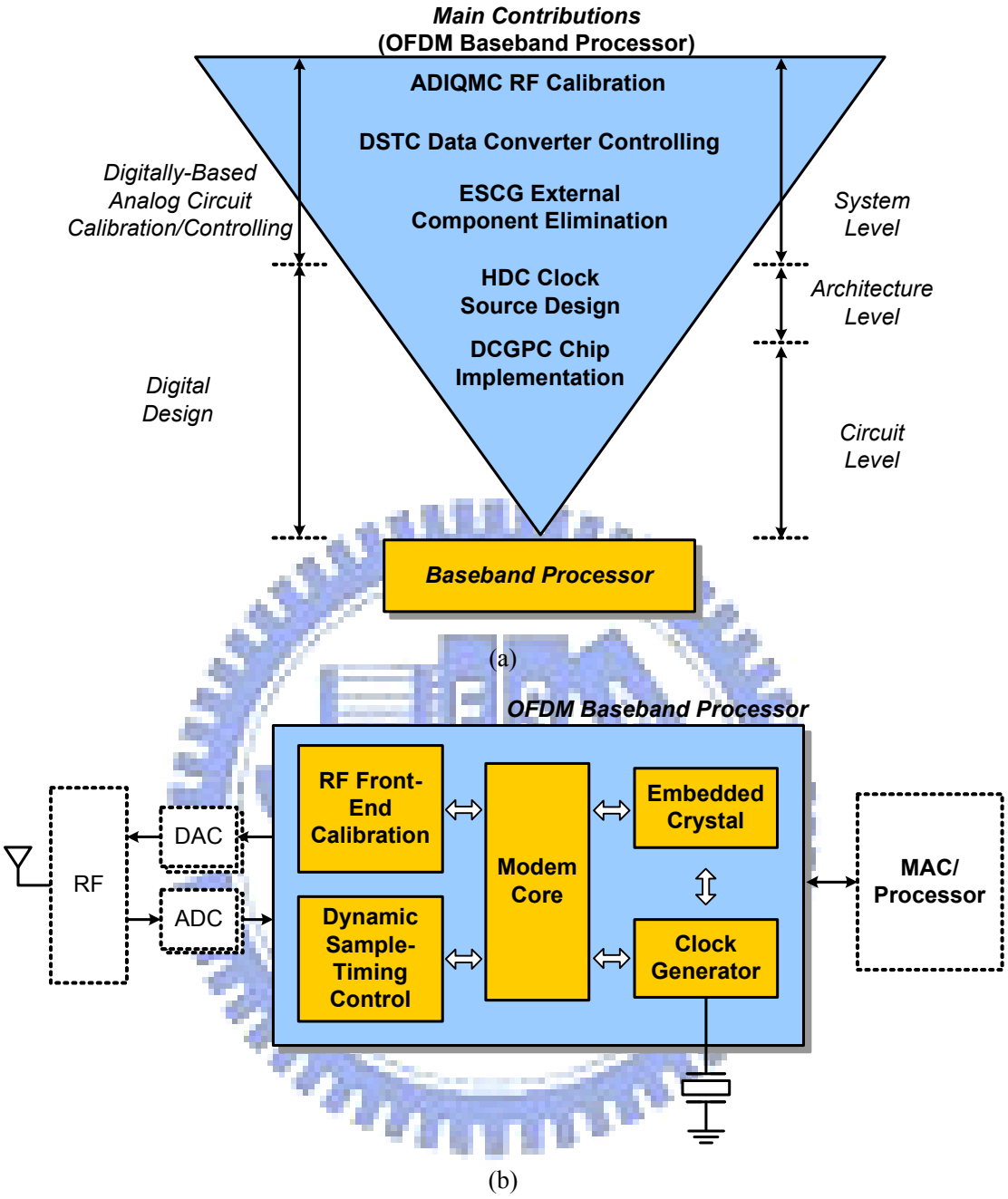


Fig. 5-1. The role of the dynamic sample-timing control in the power and data proximity scheme

Digitally-controlled oscillator (DCO) is a key module to the designs of all-digital phase-locked loops (ADPLL) [61][62], all-digital delay-locked loops (ADDLL) [63], and all-digital multi-phase clock generators (ADMCG) [38][63] that are becoming more and more widely used in SoC applications and system-level integrations. Instead of the utilizations of voltage-controlled oscillators (VCO) in the analog-based PLLs,

which have difficulty in charge-pump designs, leakage minimization, and tradeoffs among supply voltage, gain, and bandwidth as circuit process moves toward deep submicron technology, the DCO possesses the merits of easier porting between different circuit processes, voltage scaling, and the power minimization. Moreover, the feature of the all-digital approach minimizes the control and integration efforts.

The power consumption, however, is a major design challenge in a DCO design. It is found that the DCO power, depending on variant operating frequencies, occupies 50%~70% power of the target circuits [38][64]. Moreover, state-of-the-art DCO designs have two major drawbacks: (i) the absolute DCO power increases and (ii) the DCO occupies higher power ratio in the target circuits, as the operating frequency becomes lower. Therefore, this confines the uses of the DCO in low frequency applications, especially in the power-critical or battery-less systems [65].

The DCO has been proposed in several architectures. The current-starved DCO [66] changes delays by modifying supply current that provides high delay resolution but also features high static power consumption. The LC-tank DCO [67] requires dedicated layout design, although a high delay resolution is maintained. Consequently, standard cell based DCOs have been proposed for better design portability. Straightforward delay elements, buffers/inverters [61] and or-and-inverter (OAI) [63] logic cells, present high power and poor linearity with insufficient delay resolution. The digitally-controlled varactor (DCV) has good delay resolution, but the power is still unacceptable. Therefore, the hysteresis delay cell (HDC) was proposed [52] for the tradeoffs between power and delay resolution, which was the first use of HDCs in a DCO design. The HDC was used to generate a delay range equal to the one in a multiple of inverters, in a simple topology, instead of cascading lots of inverters. This

previous HDC, however, does not possess better power feature than an inverter. Consequently, this work addresses (i) the proposal of a HDC set (on-off, cascade, and nested) with low power features and (ii) a power-of-two delay stage DCO (P2-DCO) which is easily achieved by the proposed HDC set. These two features accordingly overcome the challenge in DCO power reduction, especially in a sub-100MHz design.

5-2 The P2-DCO Architecture

The power-of-two digitally-controlled oscillator (P2-DCO) is designed that every segment in the delay line has a delay in the power-of-two descending order. So, each segment performs a propagation delay either half of previous segment or twice of the next one. Fig. 5-2 illustrates the architecture of the P2-DCO that is partitioned in a coarse-tuning stage and two fine-tuning stages. The coarse-tuning stage applies hysteresis delay cells (HDC) as essential delay elements in variant topologies (on-off, cascade, and nested). According to the HDC delays that cover a specific range, they are further defined as very-large-scale HDC (VLHDC), large-scale HDC (LHDC), medium-scale HDC (MHDC), and small-scale HDC (SHDC), in terms of delays.

The coarse-tuning stage is composed of VLHDCs and LHDCs, and multiplexers are used to determine if a VLHDC or a LHDC is in the signal propagation path or not. Moreover, an AND logic gate is used to block an input signal transition when the VLHDC or the LHDC is not selected. Both the VLHDC and LHDC can be internally sized and concatenated for different delay generation.

The MHDC and SHDC constitute the first fine-tuning stage. Both the MHDC and SHDC are able to switch the propagation delay internally, instead of the use of multiplexers. In the second fine-tuning stage, also the final delay tuning stage, a MOS

gate capacitor (MGC) is applied to generate variant combinations of output loadings for delay fine tunings. The gate capacitance is also arranged in the power-of-two ordering style by increasing a transistor gate width or combining transistors in a multiple of fingers.

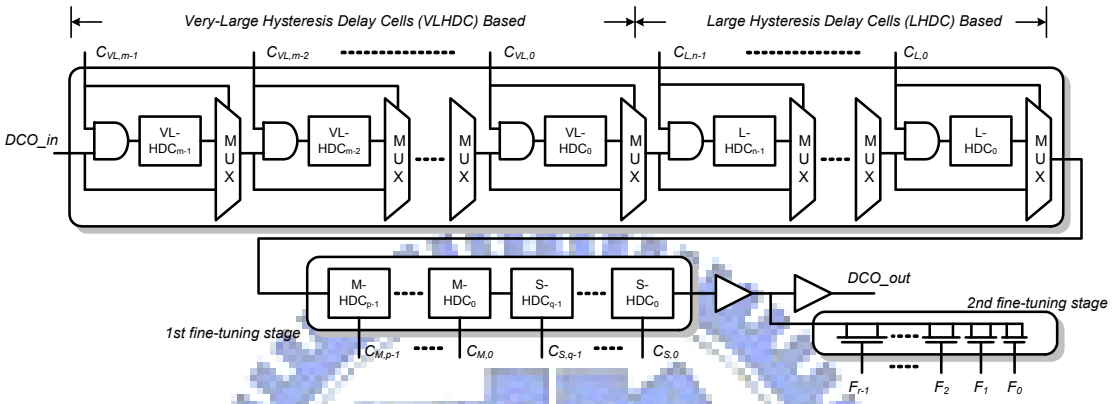


Fig. 5-2. The power-of-two delay stage DCO block diagrams

5-3 Coarse Tuning Delay Cells

The coarse-tuning stage contains two circuit forms, LHDC and VLHDC, as shown in Fig. 5-3. The LHDC (or VLHDC) are designed to generate a delay that is several tens (or hundreds) times larger than a minimum-sized inverter in the same manufacturing process. This is achieved by increasing output rise-time or fall-time and at the same time avoiding large short current sink in the next stage to maintain the low power purpose. This is achieved by the use of Schmitt-trigger cells with the hysteresis phenomenon.

5-3-1 Large-Scale Hysteresis Delay Cell (LHDC)

A LHDC is designed by an inverter chain internally cascaded with a header or a footer cell as shown in Fig. 5-3(a). The degeneration form of the LHDC can be found

in the low power Schmitt-trigger architecture [70]. The internal voltage V_n and V_p are expressed as

$$\begin{cases} V_n\,|_{MP1=ON} = \dfrac{V_{in}}{R_n+1} + \dfrac{R_n V_{SS} + V_{t,n}(R_n-1)}{R_n+1} \\ V_p\,|_{MN1=ON} = \dfrac{V_{in}}{R_p+1} + \dfrac{R_p V_{DD} - |V_{t,p}|(R_p-1)}{R_p+1} \end{cases} \tag{5-1}$$

where the $R_n=(k_{n1}/k_{n2})^{1/2}$ and $R_p=(k_{p1}/k_{p2})^{1/2}$ with the transconductance k_n and k_p for a NMOS and a PMOS, respectively. The MOS threshold is denoted by V_t. It can be found that the node V_p is equal to VDD when the transistor MP1 is operated at ON state. As a result, the internal delay chain of a LHDC is equivalently regarded as a voltage scaling with a supply voltage $VDD'=VDD-V_n|_{MP1=ON}$ or $VDD'=V_p-VSS|_{MN1=ON}$. Therefore, an inverter propagation delay (t_p) in the internal delay chain is expressed by the first-order approximation

$$t_p \approx \sum_{s=0}^{S-1} \frac{C_L}{2VDD'}\left(\frac{1}{k_{p,s}} + \frac{1}{k_{n,s}}\right) \tag{5-2}$$

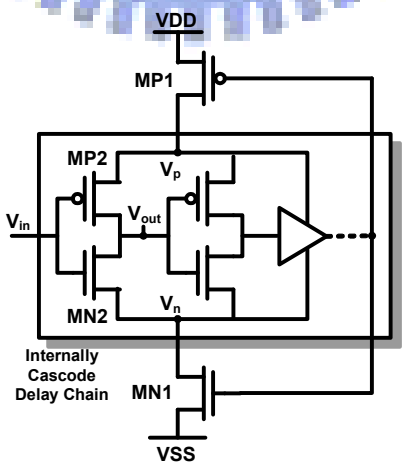
where C_L is the output loading appeared in each inverter output node. The $k_{n,s}$ and $k_{p,s}$ denote the transconductance in the s-th inverter, and the capital S represents the total number of inverters in the LHDC. Due to the hysteresis property, the LHDC does not cause large short current sink when the input signal behaves a slow rise- or fall-time transition.

5-3-2 Very Large-Scale Hysteresis Delay Cell (VLHDC)

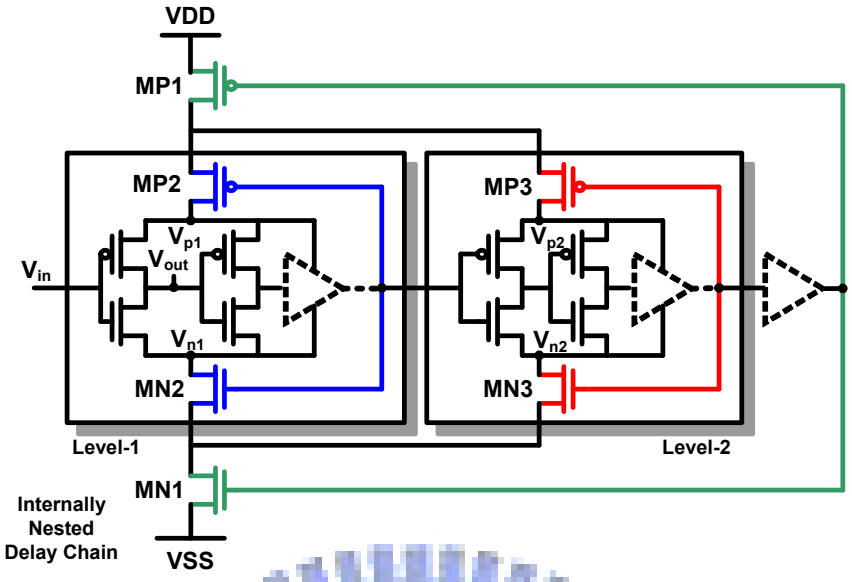
The VLHDC is designed by a nested cascaded LHDC as shown in Fig. 5-3(b). This VLHDC provides several hundreds times cell delay of a minimum size inverter. The static behavior of the VLHDC is stated as follows. Assume the input voltage V_{in} has a transition from low to high. Then the input voltage propagates to the output of

the Level-1 delay block. This also turns on the transistor MN2 and disables MP2. When this input transition propagates to the output level-2 delay block, the transistor MN3 is also turned-on. The output signal of the final-level delay block may directly enable the MN1 or turn on the MN1 after an optional buffer delay chain. This can control the propagation delay of an input change. Note that the V_{n1} and V_{n2} are isolated by two transistors cascaded before the MN2 and MN3 are turned on. This implies that the propagation delay in each nested level is balanced. This has the advantages that the signal propagation in each level block can be operated in the lowest *VDD'* (*VDD'*=*VDD*-V_{n1} or *VDD*-V_{n2}) as long as the threshold voltage is small enough, and guarantees the VLHDC can be nested deeper with each level block performs the similar propagation delays.

The calculation of the propagation delay is on a similar basis of the LHDC circuit, except the footer cell (MN1) and the header cell (MP1). Therefore, the derivation of V_{n1} and V_{n2} can be referred to Eq. (5-1) that R_n is modified to the equivalent transconductance of {MN1 and MN2} or {MN1 and MN3}. This gives new V_{n1} and V_{n2} values, resulting in the propagation delay calculated from Eq. (5-2).



(a)

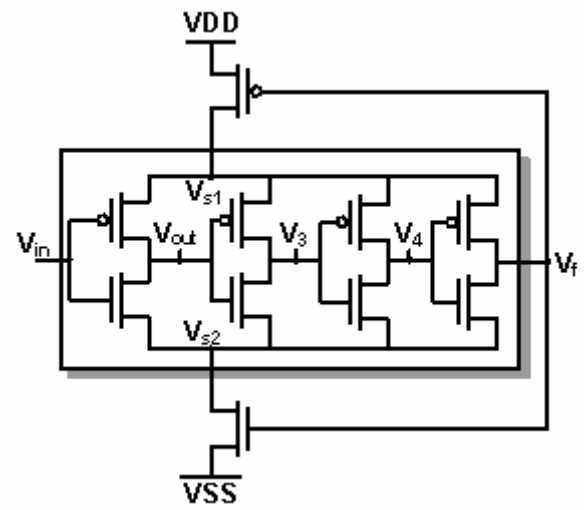


(b)

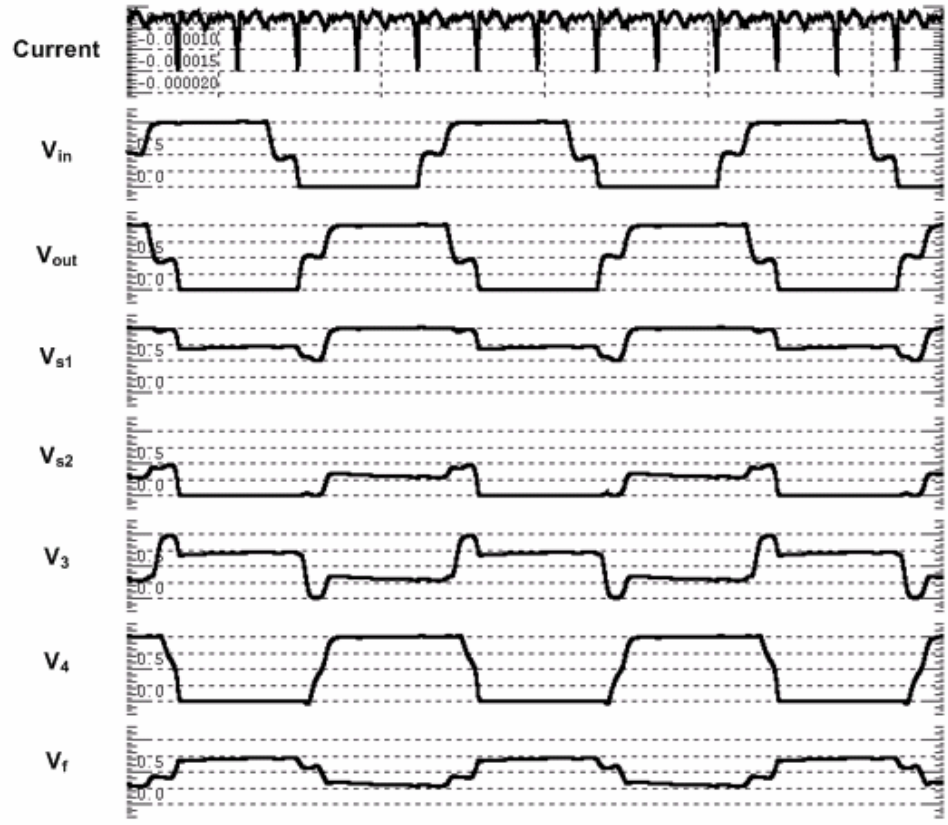
Fig. 5-3. The proposed delay cells (a) large-scale hysteresis delay cell (LHDC); (b) very-large-scale hysteresis delay cell (VLHDC)

Fig. 5-4 illustrates the fastest LHDC cell schematic, defined as LHDC0, and the corresponding waveform behavior. The LHDC0 shown in Fig. 5-4(a) is equivalent to a dual inverter cascaded with a PMOS header and a NMOS footer. During the propagation of input signal to output, the V_{s1} and V_{s2} nodes provide the necessary pull-high and pull-down voltages as depicted in Fig. 5-4(b). When the output is tied to logic high, the V_{s1} provides the necessary voltage level whereas the V_{s2} concatenated to the NMOS footer cell has a floating voltage level. The signal level eventually propagates to the final stage that has the output signal, V_f, feedback to the header and footer cell for the charge and discharge path controlling. This signal level of this feedback node is kept floating centered at VDD/2 voltage level. This only provides sufficient turn-on and turn-off voltage for the header and footer cells. With those properties, the propagation delay from input to output has rather large value so that it can perform a long delay compared to a conventional inverter cell. The current profile of LHDC0 can also be found in the waveform plot. The current is in the scale of

10μA, and the peak value occurs at the rising or falling edge of both the input and output signals.



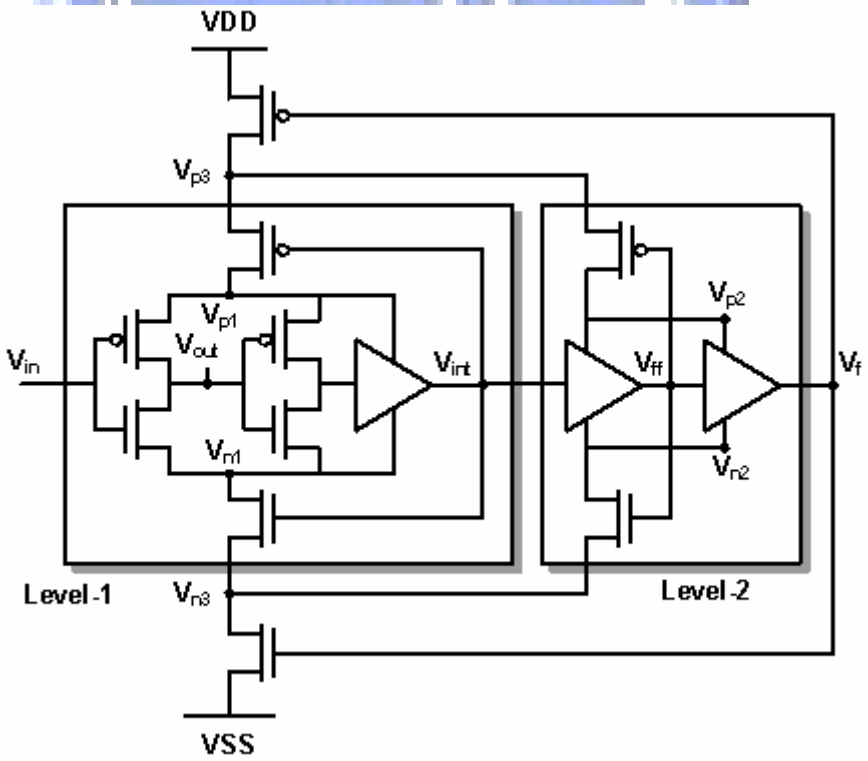
(a)



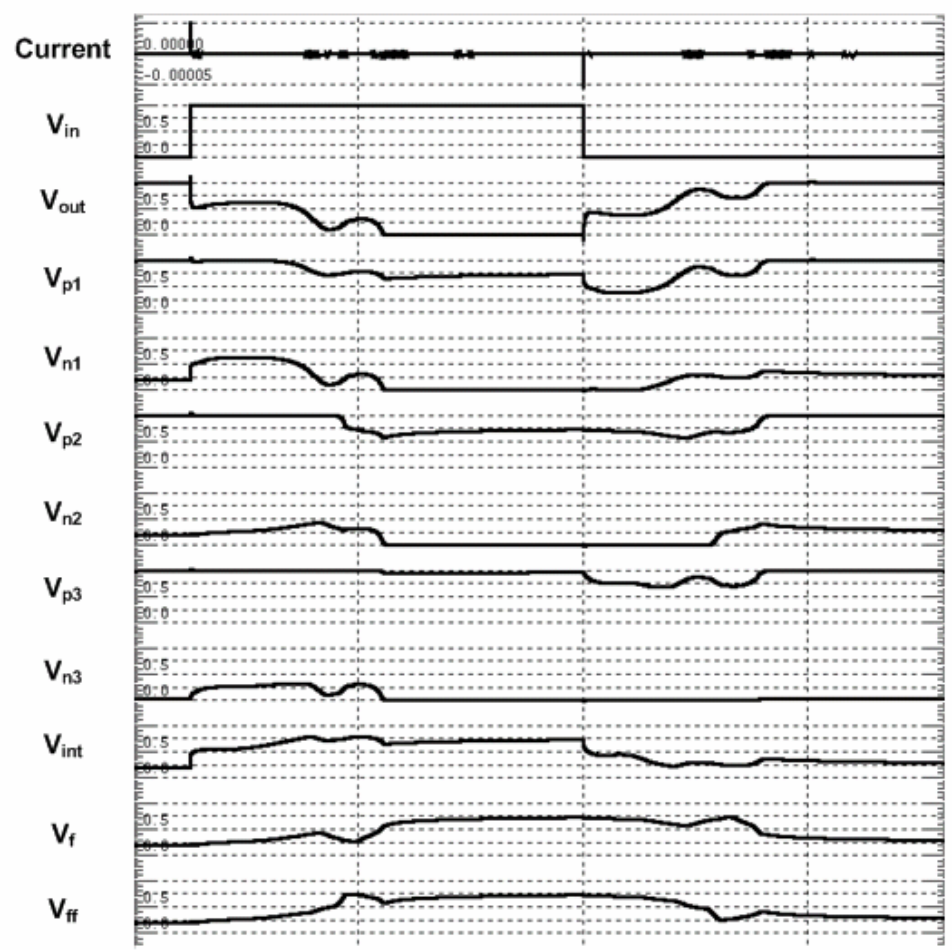
(b)

Fig. 5-4. The example case (a) LHDC0 schematic (b) LHDC0 generated waveforms

Fig. 5-5 illustrates the smallest VLHDC cell that is defined as VLHDC0. This VLHDC0 is equivalently composed of four buffer cells with serial cascaded header and footer cells as shown in Fig. 5-5(a). The logic behavior from V_{in} to V_{out} is equal to an inverter. The internal nodes providing charge and discharge level (V_{p1}~V_{p3} and V_{n1}~V_{n3}) are in order changed to floating, tied-high, or tied-low, according to the input signal transitions. The floating nodes for header and footer cell controlling are used to turn on or turn off the corresponding charge and discharge paths. The overall current sink is also illustrated. The peak current is about 50μA occurred at the input signal transitions, and the rest time of signal propagation has current profile in the order of 1μA, providing an overall current in sub-1μA scale.



(a)



(b)

Fig. 5-5. The example case (a) VLHDC0 schematic (b) VLHDC0 generated waveforms

5-4 Fine Tuning Delay Cells

The fine delay tuning is achieved by two stages. The first stage is composed of MHDC and SHDC that generate delays about 0.01~10 times of a minimum sized inverter. Both the MHDC and SHDC perform the hysteresis phenomenon. The second fine-tuning stage is designed by the MOS gate capacitance (MGC) for sub-pico-scale delay tuning.

5-4-1 Medium/Small-Scale Hysteresis Delay Cell

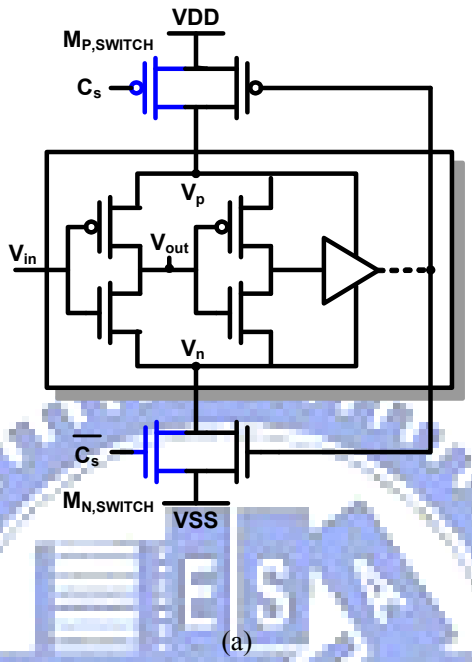
The MHDC and SHDC is designed on a Schmitt-trigger circuit basis, as shown in Fig. 5-6. When both transistors $M_{P,SWITCH}$ and $M_{N,SWITCH}$ are in the turn-off state, the MHDC and SHDC degenerates to a conventional Schmitt-trigger-based delay cell [70]. When the HDCs are operated in the Schmitt-trigger mode, the hysteresis phenomenon appears, and provides a longer propagation delay. As the $M_{P,SWITCH}$ and $M_{N,SWITCH}$ are switched to the turned-on state, a direct charge or discharge path exists in the output node, resulting in a normal inverter behavior. Consequently, the on-off HDC has its naming from the on-off behavior of the switch-transistors. In other words, the switch transistor determines if the circuits perform the Schmitt-trigger behavior or not, resulting in a hundred pico-second delay difference.

The delay analysis can be found from the hysteresis or inverter behavior. When the switch transistor is turned-on, the MHDC in Fig. 5-6(a) (cascade inverters) and SHDC in Fig. 5-6(b) (an inverter with equivalent half W/L) perform similar delay propagation. When the circuits turn into the Schmitt-trigger mode, the internal node voltage and propagation analysis for the MHDC can be found in Eq. (5-1). Furthermore, the V_n and V_p of the SHDC in Fig. 5-6(b) is expressed [71] as

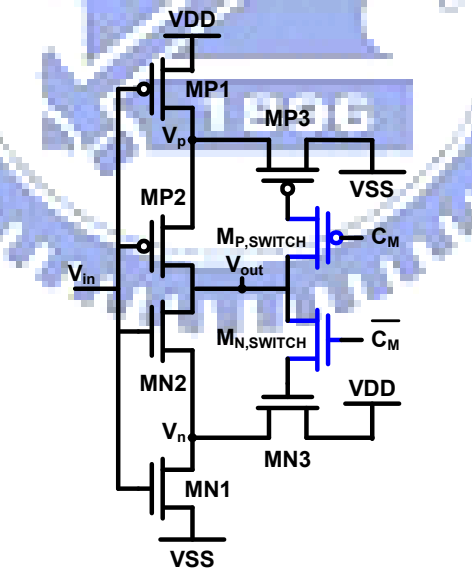
$$\begin{cases} V_n = V_{DD} - V_{t,n} - R_n(V_{in} - V_{t,n}) \\ V_p = R_p(V_{DD} + V_{t,p} - V_{in}) - V_{t,p} \end{cases} \tag{5-3}$$

where $V_{t,n}$ and $V_{t,p}$ are the threshold voltage of a NMOS and PMOS, respectively. The effective propagation delay by voltage scaling $VDD'=VDD-V_n$ provides smaller delay than that of the MHDC. As a result, these MHDC and SHDC cells provide exclusively two delay values for adjustment. This delay generation concept by maintaining or destroying the hysteresis property can be applied to every possible

Schmitt-trigger design form. This work only illustrates the discussed two forms for the consideration of power consumption and delay range.



(a)

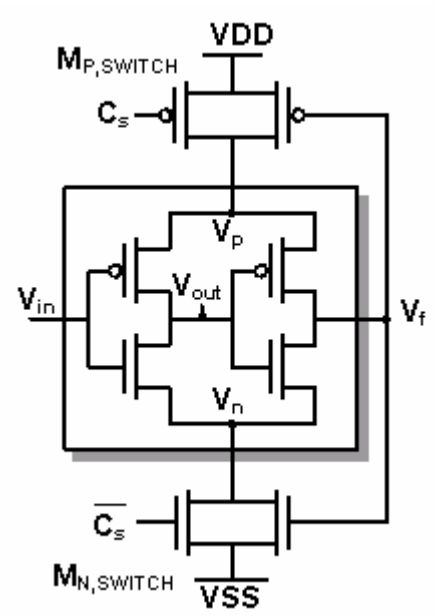


(b)

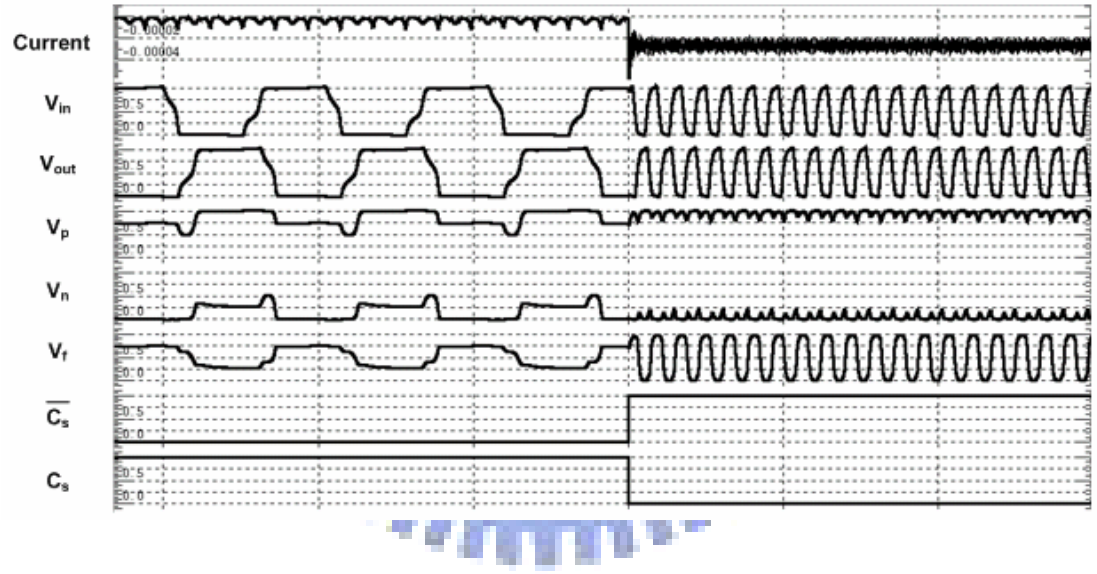
Fig. 5-6. The proposed delay cells (a) medium-scale hysteresis delay cell (MHDC); (b) small-scale hysteresis delay cell (SHDC)

Fig. 5-7 demonstrates a MHDC cell with the smallest design scale. This is defined as MHDC0 with the schematic shown in Fig. 5-7(a). As the switch transistors are turned off, the MHDC0 degenerates to hysteresis mode with the behavior like the type in LHDC. The corresponding waveforms are shown in Fig. 5-7(b). When the switch transistors are turned on, this MHDC0 becomes a normal buffer with dual cascaded inverters that can be defined as the inverter mode. The delay resolution comes from the delay difference between the hysteresis mode and inverter mode. Accordingly, a delay overhead exists in the delay chain if the MHDC0 is placed in a certain delay path. The current profile in the hysteresis mode and inverter mode is also shown. The current sink in the hysteresis mode promises the values from the LHDC0 that is in the level of 10μA scale. When the operation is changed to the inverter mode, the current rises to about 30 μA.

An example of SHDC cell is also shown in Fig. 5-8. The schematic in Fig. 5-8(a) is also composed of a hysteresis topology in addition to the broken path for SHDC degenerated to a conventional inverter cell. Similarly, the delay resolution also comes from the delay difference between the hysteresis and inverter modes as illustrated in Fig. 5-8(b). Accordingly, the delay in the inverter mode is also considered as the overhead in a delay path. This current level is a little higher than that of a MHDC0 cell. The current sink in the hysteresis mode is around 30 μA, and a similar level of current sink is in the inverter mode.



(a)



(b)

Fig. 5-7. The example case (a) MHDC0 schematic (b) MHDC0 generated waveforms

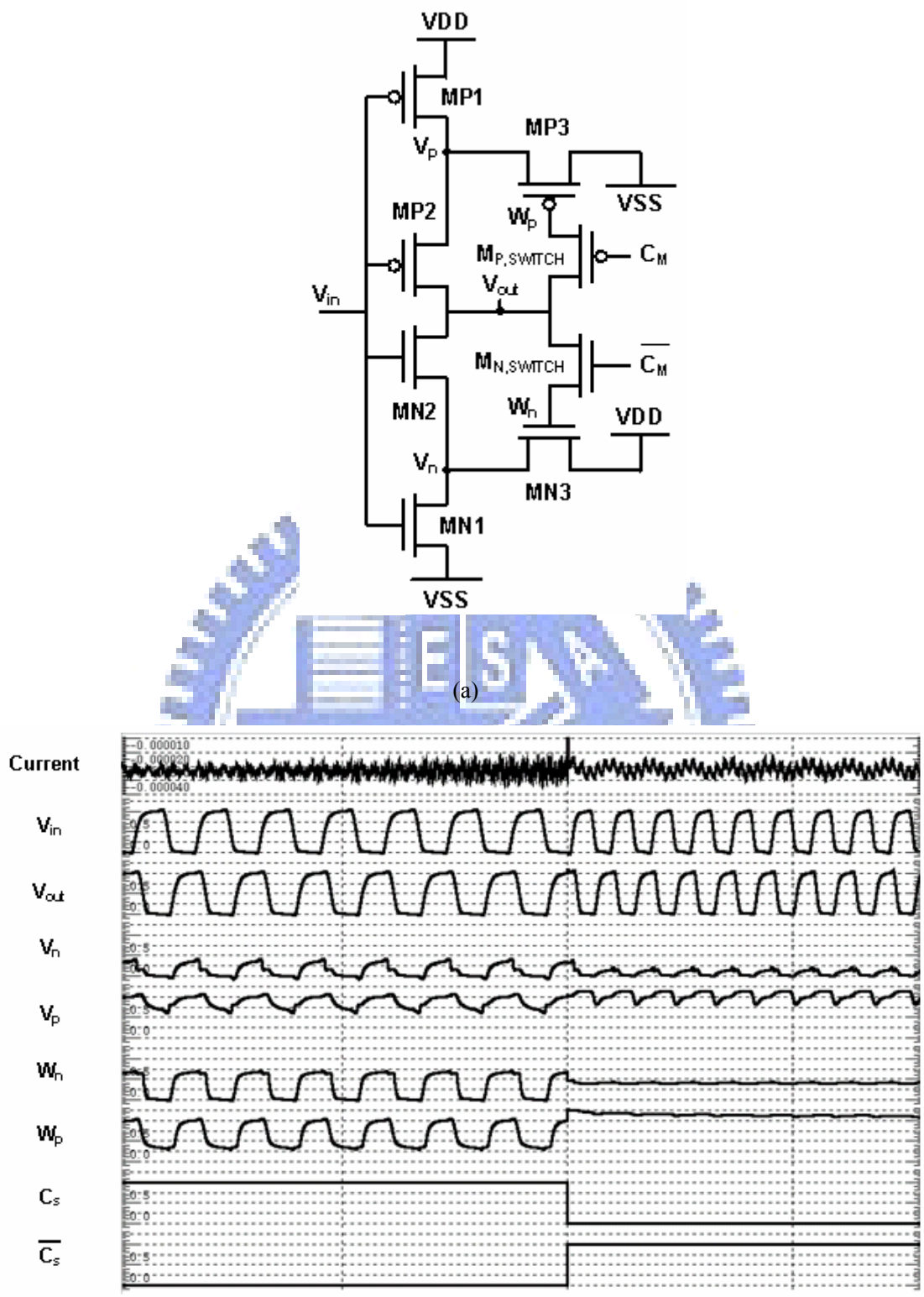


Fig. 5-8. The example case (a) MHDC0 schematic (b) MHDC0 generated waveforms

5-4-2 MOS Gate Capacitance (MGC)

The MGC provides a sub-pico-second delay resolution for final stage fine tuning. The delay is generated by the use of a MOS gate capacitor. The MGC is placed at the output node of the last stage in the delay chain as an extra output loading. Consequently, a digitally-controlled code that is provided to the MGC slightly changes the output delay, resulting in a high resolution P2-DCO design.

5-5 Simulation Results and Comparisons

The proposed delay cells are evaluated in the design of the P2-DCO operating at 5MHz and 200MHz, respectively. The circuit process is 90nm standard CMOS technology. The rest evaluations are simulated using the HSPICE simulator, and the comparisons are done by rebuilding the published approaches under the same circuit process.

The features of the P2-DCO are listed in Table 5-1. The delay range of each cell is provided by a slightly modification of transistors' sizes. The property of the power-series delay chain illustrates that each delay segment provides an approximately twice delay of the next delay stage and half delay of the previous one. Consequently, the P2-DCO enables the covering a period range from 0.1ps to 132ns in this design.

The power in the coarse-tuning stages is in the range of 0.29~25.66μW. The first fine-tuning cell has the power about 0.1μW, and the second fine-tuning MGC provides the delay resolution 0.1ps. Compared to the most commonly-used coarse-tuning cell (an inverter or tri-state buffer [52][63][68]), the proposed VLHDC and LHDC at least achieve power reduction by 97.33% and 93.31%, respectively. In

the hundred-pico-second tuning range, the MHDC and SHDC enables about 75.85% power reduction when compared to the equivalent delay-scale approach (HDC [52]). The second fine-tuning delay is achieved by an added-on output loading in an inverter's output. Therefore, the power of the fine-tuning cell is measured from the incremental power compared to a pure inverter power. The simulation shows that the MGC consumes the incremental power about 0.1μW, which is only 2.16% and 4.5% of the published long-delay DCV and short-delay DCV approaches [52][68], respectively.

The power and delay characteristics of each delay cell are imply the overall DCO power performance. The DCO dynamic power $P_{d,DCO}$ is proportional to total consumed energy in each delay cell divided by total delay, and a general expression is given by

$$P_{d,DCO} \propto \frac{\sum_k (D_k \cdot P_{d,k})}{\sum_k D_k} = \frac{\sum_k (D_k \cdot P_{d,k})}{T/2} = 2\sum_k (R_k \cdot P_{d,k}) \quad (5\text{-}4)$$

where D_k is the propagation delay of each delay cell that corresponds to the dynamic power $P_{d,k}$. The delay ratio R_k is defined by a cell delay over the period T. Note that the DCO power $P_{d,DCO}$ is not a function of its operating frequency, because only a single cell in the delay chain is activated at every instance rather than whole cells swing together. For instance, the VLHDC in Table 5-1 provides the largest delay ratio R_k when used in the delay path. Moreover, the power feature of each proposed delay cell is listed, which is measured by continuously switching the cell output for the charge and discharge power calculation.

The P2-DCO is composed of the SHDC~VLHDC and MGC. Table 5-2 illustrates the P2-DCO features and comparisons with the linear-DCO approach [52]. The delay line in the linear-DCO requires 2048 (and 32) inverters at frequency 5MHz (and 200MHz)* to achieve the target delay (half period). Accordingly, it requires 2048 (and 32) NAND logic gates and 2048 (and 31) multiplexers for delay path gating and selection, respectively. On the other hand, the P2-DCO requires only eight (and four) delay segments in the first coarse-tuning stage. Consequently, only eight (and four) AND logic gates, and eight (and six) multiplexers are required for the delay generation. Assume minimum size is applied to all logic gates (inverter: W/L= 0.6μm/80nm; NAND: W/L= 1.2μm/80nm; AND: W/L=1.4μm/80nm; Multiplexer: W/L=3.0μm/80nm), and the total required W/L is also summarized. It is found the total area is saved by 98.9% (and 36.4%). This area reduction also implies the static power saving, especially in a deep-submicron process. It is found that the P2-DCO achieves 93.67% (and 16.7%) static power reduction. In the dynamic power exploration, it is again referred to Eq. (5-4) that $P_{d,k}$ and R_k determine the total dynamic power. The linear-DCO regardless of operating at 5MHz or 200MHz utilizes the same logic cells (unchanged $P_{d,k}$), and the used inverters, NAND gates, and multiplexers are increased in the same ratio (unchanged R_k). As a result, the simulated dynamic power does not change too much (150μW at 5MHz 355ns/ and 140μW at 200MHz).

In the P2-DCO case, however, the 200MHz P2-DCO consumes 40μW due to fewer multiplexer used and less power density of VHDC~SHDC. When the P2-DCO is operated in the 5MHz case, the dynamic power is largely reduced to 5μW. This is because a low-frequency P2-DCO applies mainly a LHDC or even a VLHDC in the delay path that provides a much smaller $P_{d,k}$ and larger R_k, resulting in a tremendous

power reduction, as shown in Fig. 5-9. Moreover, the required delay stage and multiplexers in P2-DCO are proportional to O(log2(D)) to achieve the target delay D compared to that in the linear-DCO, which is proportional to O(D) and O(2^D) for the delay stage and multiplexers, respectively. Moreover, the multiplexers used for the delay path selection are also largely shrunk. The challenges of designing a P2-DCO are to guarantee a monotonic delay behavior when the control word increases. Therefore, every later delay stage is carefully sized to be about half delay than the previous one in both the best and worst process-voltage-temperature corner cases. Since the MGC provides a linear behavior, it is used for the fine-tuning to guarantee the DCO is able to cover every desired delay value. Finally, the overall comparison to the state-of-the-art DCOs are shown in Table 5-3. The designed P2-DCO requires 17-bit control word length, operating in the frequency range 1MHz~250MHz. The LSB of the control word provides an about 0.05ps delay resolution. Note that the proposed P2-DCO DO NOT NEED any control word decoding, since the delay path selection is already designed in the format of two's complement or, in other words, the power-of-two delay stages. With this proposed approach, the PS-DCO provides the least power consumption (5μW@5MHz, 40μW@200MHz) in the state of the art.

TABLE 5-1. DELAY CELL SUMMARIES AND COMPARISONS

	Design Basis		Delay Res.(ns)	Power(μW)	Normalize Power
Coarse Tuning	Std. Cell	INV[63]	0.1	46.18	1
	Nested HDC	$VLHDC_3$	66.86	0.34	0.74%
		$VLHDC_2$	30.004	0.45	0.97%
		$VLHDC_1$	15.01	1.07	2.32%
		$VLHDC_0$	7.33	1.2	2.60%
	Cascode HDC	$LHDC_0$	3.666	3.14	6.80%
1^{st}-stage Fine tuning	Std. Cell	HDC[52]	0.12	106.25	1
	On-off HDC	$MHDC_0$	1.788	14.76	13.89%
		$SHDC_2$	0.734	29.62	27.88%
		$SHDC_1$	0.378	25.05	23.58%
		$SHDC_0$	0.204	22.62	21.29%
2^{nd}-stage Fine tuning	Std. Cell	DCV-LD[52]	0.02	23.14	1
		DCV-SD[52]	0.01	13.87	59.94%
	MOS gate cap.	MGC	0.1~50f	0.5	2.16%

TABLE 5-2. DCO SUMMARIZES AND COMPARISONS

	Linear DCO [52]		Proposed P2-DCO	
	200MHz	5MHz	200MHz	5MHz
Delay Cell W/L	173.6μm	2996μm	84.96μm	425.04μm
Multiplexer W/L	93μm	6141μm	6μm	24μm
Misc. W/L	N/A	N/A	8.92μm	11.2μm
Total W/L	266.6μm	9137μm	99.88μm	460.24μm
Static Power	0.155μW	3.13μW	0.186μW	0.2μW
Dynamic Power	140μW	150μW	40μW	3μW

TABLE 5-3. COMPARISONS TO THE STATE OF THE ART

	This Work	TCAS2'07 [52]	TCAS2'05 [68]	JSSC'05 [66]	JSSC'03 [63]	JSSC'04 [61]
Process	90nm CMOS	90nm CMOS	0.35μm CMOS	0.18μm CMOS	0.35μm CMOS	0.35μm CMOS
Supply Voltage (V)	1	1	3.3	1.8	3.3	3
Control Wordlength	17	15	15	5	12	7
Operation Range (MHz)	1-250	191-952	18-214	413-485	45-510	152-366
LSB Resolution (ps)	0.05	1.47	1.55	2	5	10-150
Control Decoding	NOT-Required	Required	Required	Required	Required	Required
Power Consumption	5μW(5MHz) 40μW(200MHz)	140μW (200MHz)	18mW (200MHz)	170-340μW (static only)	50mW (500MHz)	12mW (366MHz)

5-6 Summary

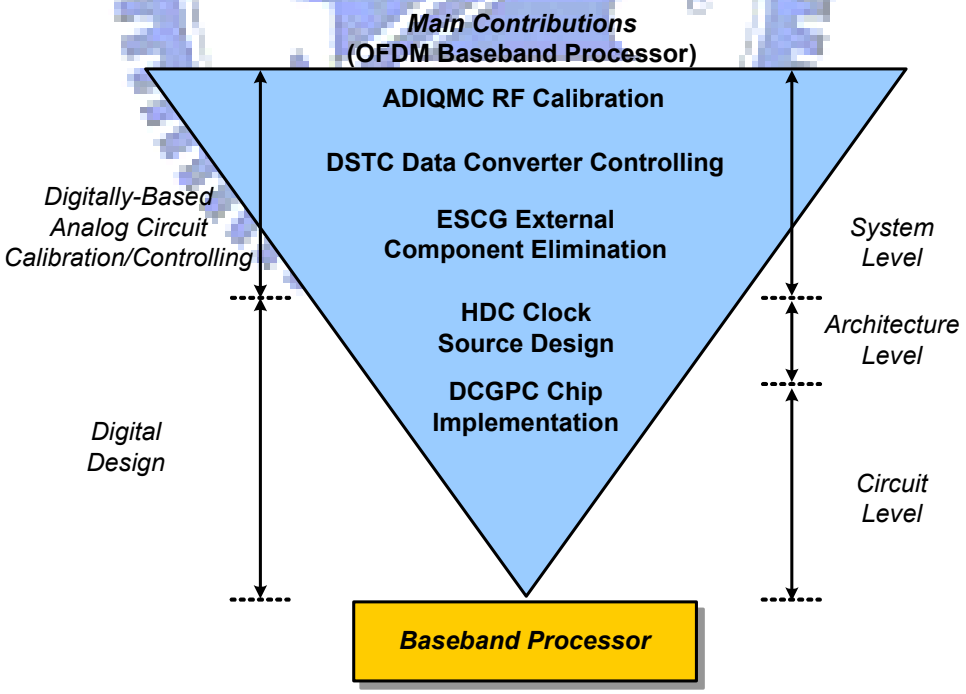
This chapter proposes several topologies for hysteresis delay cell schemes that are applied to the digital control oscillator circuit design. The HDC cell provides low power profile that is benefited especially in the low frequency large delay applications. The hysteresis delay cells are proposed in terms of SHDC, MHDC, LHDC, and VLHDC four topologies. Those proposed HDC cell reduces the power from 72.12% to 99.26% compared to the conventional used standard cells. The designed DCO targets on the low frequency range, say sub 50MHz. In the designed 5MHz operation frequency, the dynamic is saved by 98%, and the area is saved by 94.96%.

Chapter 6:

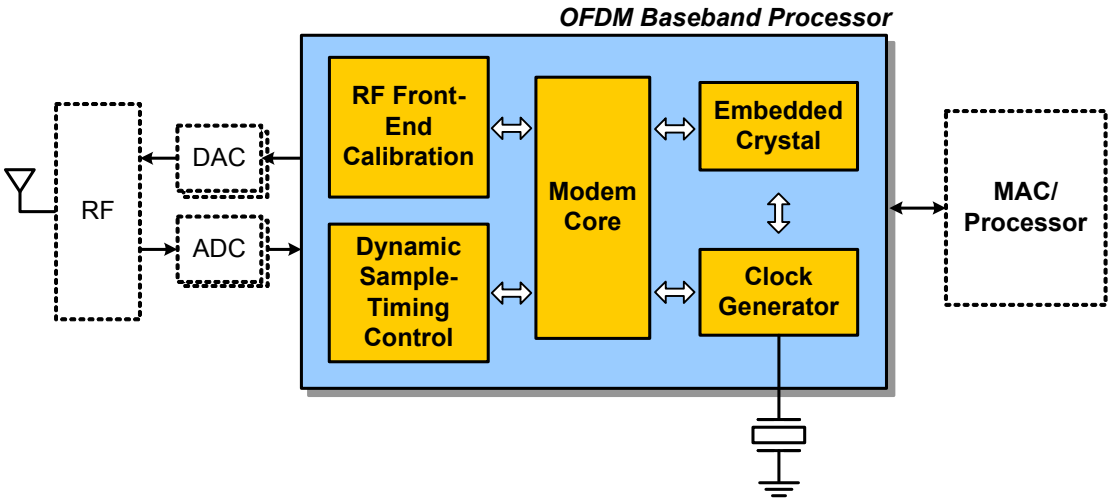
Case Study

6-1 Introduction

The evaluations of the proposals from previous chapters are achieved by the high-speed multi-band OFDM (MB-OFDM) ultra-wideband (UWB) baseband processor or an in-house designed Wireless-Body-on-The-Chip (WiBoC) platform for the wireless body area network (WBAN) applications, which aim at micro-level power consumption and highly integration capability.



(a)



(b)

Fig. 6-1. The role of the chip implementation in the power and data proximity scheme (a) design hierarchy; (b) design building blocks

Beside the implementation of the signal-processing-based ADIC RF calibration and DSTC computation, this part will take some more transistor-level implementation approach to achieve the micro-power target as illustrated in Fig. 6-1. This techniques will also applied to the whole baseband processor for the maximum power saving.

6-2 Case 1: MB-OFDM UWB baseband processor

6-2-1 Baseband Modem Designs

The baseline signal modulation and demodulation are illustrated in Fig. 6-2. In the transmitter side, the signal bit stream from the media access control (MAC) layer is first encoded by the forward error control (FEC) code. The output of FEC encoder is represented as bit stream, too. The mapper block takes every one bit or two bits to modulate them into a BPSK or QPSK symbols, depending on the transmitted data rate. Then some pilot tones are inserted into this symbol stream so that the receiver side may use the pre-known information for timing or frequency synchronization.

Afterwards, an inverse discrete Fourier transformation (IDFT) function block takes the complete symbol stream for the OFDM modulation. Before the digital-to-analog conversion (DAC), the OFDM symbols are reshaped by a pulse shaping block that may perform upsampling digital filtering for spectrum issues or reduce the peak-to-average power ratio (PAPR) by some pre-distortion signal processing. Then, the data converted analog waveforms are carried out by the RF front-end circuits.

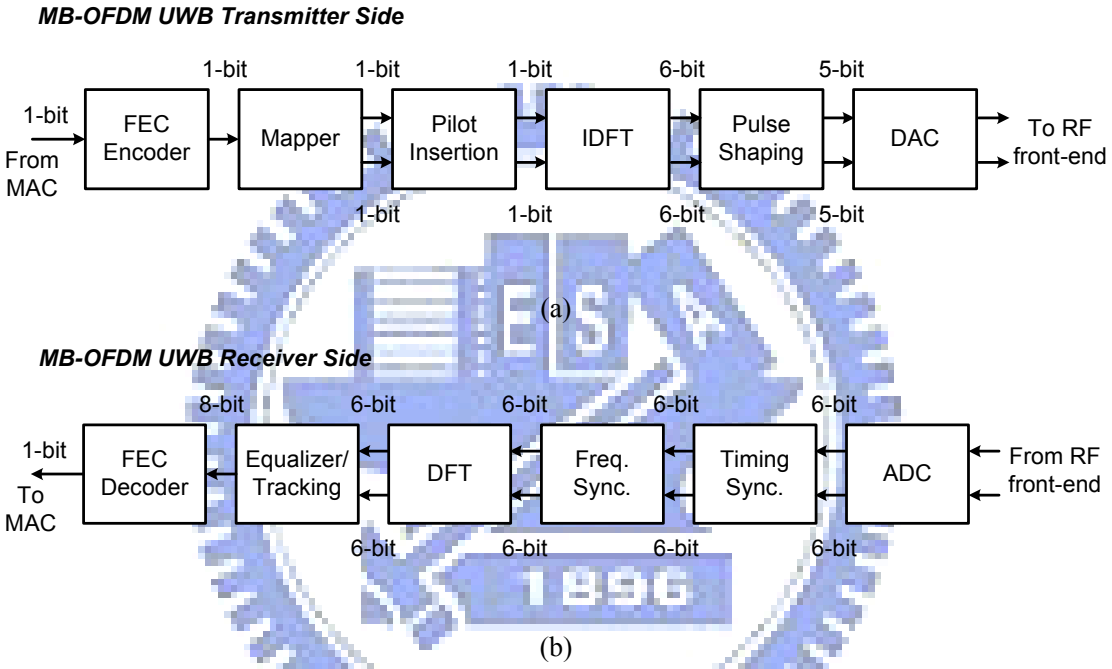


Fig. 6-2. Block diagrams in the MB-OFDM WUB transceiver (a) transmitter (b) receiver

On the contrary, the receiver side applies a timing synchronization block after analog-to-digital conversion circuits that receive analog waveforms from the RF front-end circuits. This timing synchronization block detects when a desired packet comes so that the following decoding mechanism may wake up for signal demodulation. Moreover, the timing synchronization may also be in charge of generating the best symbol stream that can be provided for the later signal decoding. After the timing synchronization, the corrected recognized symbols are further calibrated by a frequency synchronization block. This frequency error may come from

any non-ideal circuit implementation and mismatches between a transmitter and a receiver in either a RF circuit or a baseband circuit that may present in terms of a carrier frequency offset (CFO) or sampling clock offset (SCO) phenomenon. Next, the time-domain calibrated symbols are transformed to the frequency domain by a discrete Fourier transformation (DFT) circuit. The frequency-domain signals are composed of primitive information signal and the channel effects. So, the equalizer is applied to estimate the channel information and compensate the channel response. Although the equalized signals are good enough for later bit-stream decoding, the SCO effects slowly distorts the incoming signals. Consequently, a tracking mechanism is applied to guarantee the stability of the decoding quality after the equalization. Finally, the FEC decoder outputs the primitive information.

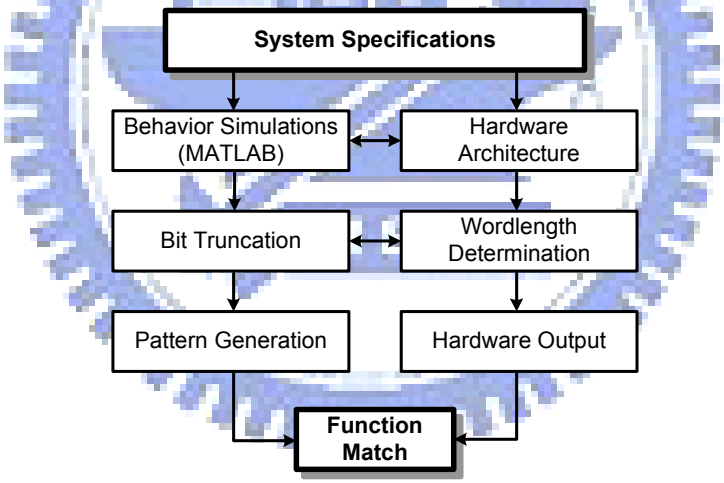


Fig. 6-3. Developments and verifications between system behavior and hardware implementation

The signal flow of Fig. 6-2 requires the definition of bit length (word length) of each building block operation so that the hardware may be implemented in the corresponding complexity and performance requirements. The determination of bit length is in accordance with the system performance in which an acceptable SNR loss is allowed for the hardware bit length reduction. The total allowable SNR loss is no

more than 3dB in the whole implementation flow. This 3dB design budget is dispread to every possible building block. An in-depth discussion of the quantization evaluations and measurements can be further directed to for complete simulation result disclosure. The brief verification relationship is shown in Fig. 6-3. Based on this baseline modulation and demodulation processor, the added contributions are placed on this platform for the illustration.

According to the baseline signal flow shown in Fig. 6-2 and the proposed contributions DSTC and ADIC RF calibration, the block diagram for this proposal is illustrated in Fig. 6-4. This shows the proposed half-duplex UWB-based modem. The whole baseband system is driven by the clock generated from an all-digital PLL embedded in the chip, and this all-digital PLL generates 528MHz and 1056MHz clock sources from an external 33MHz crystal. In order to make the radio signal easier satisfying power spectrum mask, the baseband signal go through a digital filter with 2x processing rate, i.e. 1056MHz, and sampled by 5-bit DACs before analog circuits. In receiver side, a clock rate with only 528MHz is applied to 5-bit ADCs to prevent from extra ADC power consumption due to higher sampling frequency. To guarantee the signal integrity of sampled data, this 528MHz clock source of ADCs is selected from an all-digital multi-phase generator (MPG), which generates 8 even-delay clock sources in 1.8939ns (1/528MHz), by the dynamic sample-timing controller (DSTC). Moreover, clock drift due to TX/RX clock frequency inconsistency is corrected in clock drift tracking. Furthermore, sampled signals are calibrated in digital circuits with I/Q mismatch effect due to non-balanced RF circuits. This mismatch can be detected with gain error < 1dB and phase error < 10 degree. The other standard compliance parameters of ±25ppm carrier frequency offset (CFO) and sampling clock offset (SCO) can be estimated and compensated. The parallel

architecture is also applied in OFDM modem. A 128-point parallel pipelined (I)FFT and division-free channel equalizer are exploited to achieve high throughput requirement.

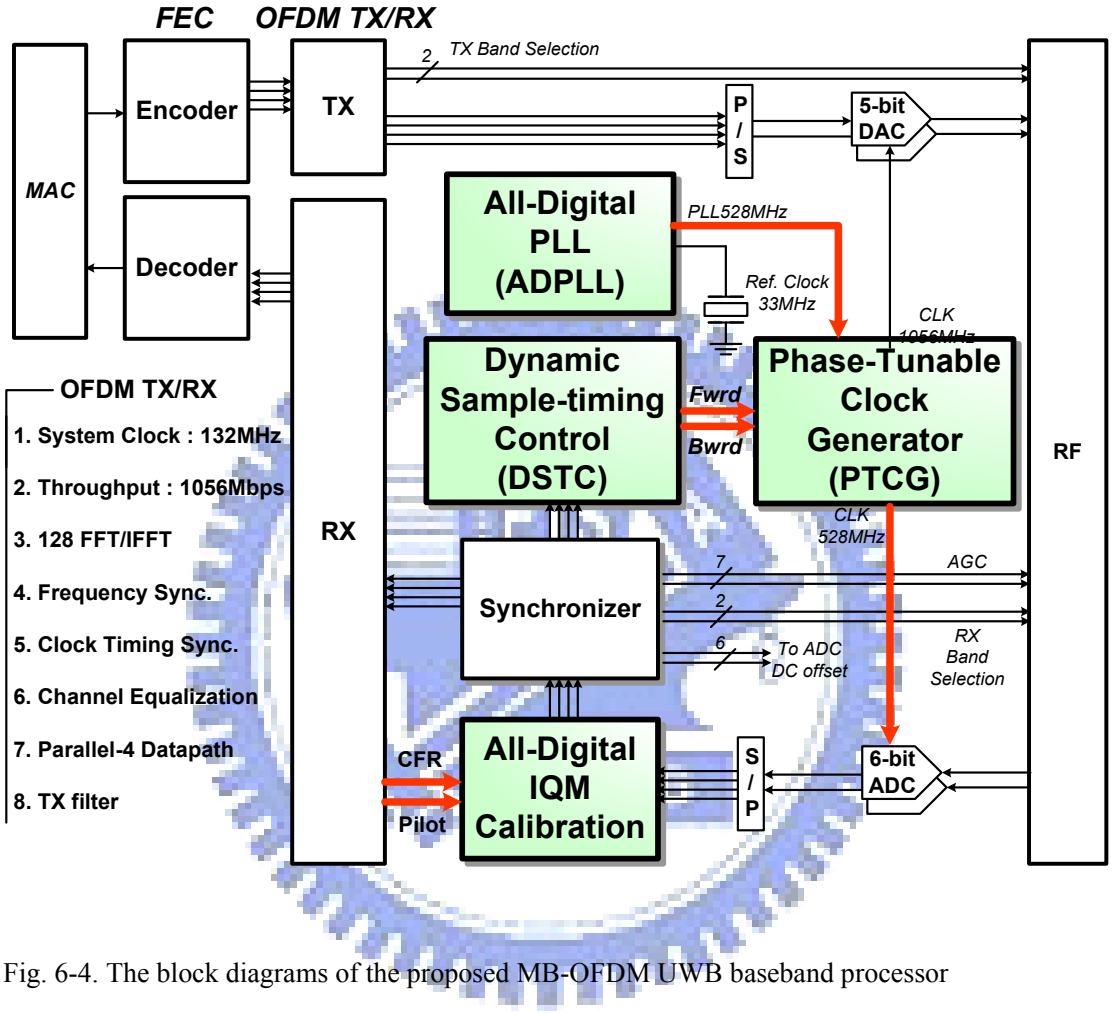


Fig. 6-4. The block diagrams of the proposed MB-OFDM UWB baseband processor

The parallel-four data-path is globally applied to this baseband processor. Due to the high signal bandwidth, say 528MHz, the fundamental clocking speed is operated at the same 528MHz frequency. This high frequency operation approaches the speed boundary of the logic computation or numeric calculation without pipelining in present technology process. This results in the architecture of parallel-four baseband architecture. Accordingly, the timing synchronizer, frequency synchronizer, (I)DFT, and channel equalizer have to correspond to the designed architecture. The

exploration of parallel-four architecture is also disclosed in the work in detail. This results in the parallel-four architecture in the DSTC and ADIC RF calibration designs that are regarded as the main focuses of this work. Thus in the following, only the ADIC RF calibration and DSTC will be explored more in the literature.

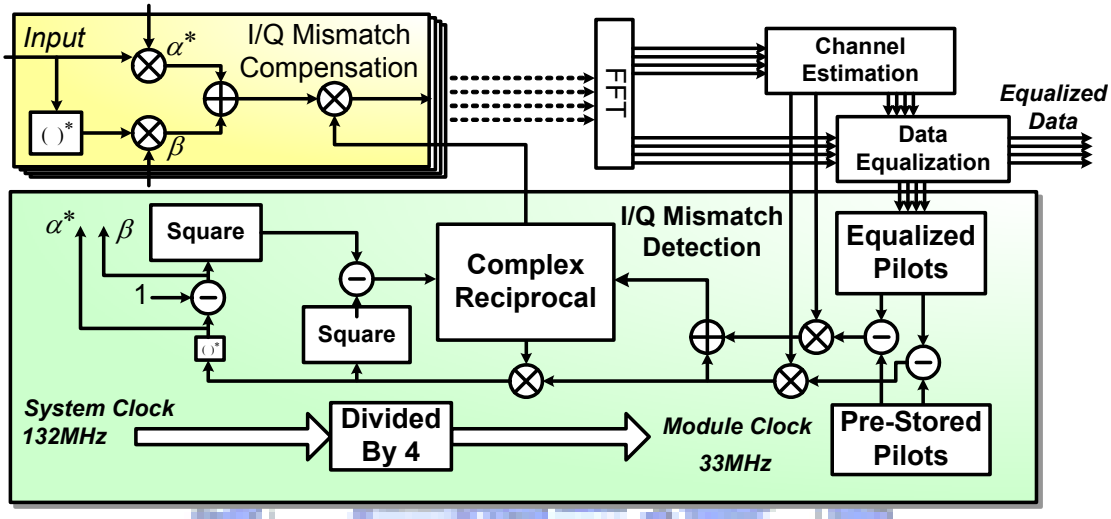


Fig. 6-5. The proposed wideband adaptive ADIC I/Q mismatch calibration scheme

Fig. 6-5 shows the architecture of ADIC RF calibration circuit. With IQM effects, each OFDM subcarrier is interfered by the one from the symmetric index in spectrum, and the gain and phase values are thus distorted, resulting in non-square QPSK constellation. By this digital signal-process-based calibration, the transceiver automatically separates subcarrier interference and compensates signal distortion. To extract gain and phase errors, distorted pilots from two spectrum symmetric indices are subtracted from clean pilot values. Then the differences are compensated by estimated CFR, which is also IQM distorted. Therefore, a complex reciprocal is applied to eliminate this non-ideal channel estimation effect, and extracts the error parameters. For lower hardware cost, this reciprocal is also shared with IQM compensation circuit. The solvable IQM range with signals clipped by the 6-b I/Q

ADC can be up to 2dB gain and 20 degree phase. The ADIC RF calibration is achieved mainly by the signal process and the error function calculation. The efforts of the hardware implementation are to design a speed-achievable building block for the gain and phase error calculation.

The overall DSTC operation is illustrated in Fig. 6-6. It guarantees ADC operating at signal Baud rate without loss of signal integrity. The control circuit takes preamble and determines whether the data from ADC is sampled at the eye-open positions, and a corresponding *Forward* or *Backward* command is sent to ADMPG. The resulting ADC-driving clock then comes earlier or later by ±236.7ps. Note that any decision to ADMPG is made during band transitions. This guarantees each OFDM symbol is sampled from the same clock phase. To satisfy the high throughput requirement, the parallel-4 architecture is exploited. The input signals are compared, and the differences are accumulated. The accuracy of difference accumulation is easily influenced by CFO effect and quantization word-length. To avoid CFO problem, an inner-product correlation is applied for any signal comparisons. This also results in reduced complexity due to calculation in real number, and signal word-length can be enhanced under such a high throughput requirement, resulting in more accurate accumulation. Moreover, it is unnecessary to sum up all difference values. As long as any overflow or underflow flag occurs, a forced-decision can be made to control the ADMPG. This effectively reduces 50% hardware cost and computation time of this high speed and high resolution accumulator, resulting in lower power consumption. This circuit consumes 1.9mW, which occupies only 6.8% of total chip power.

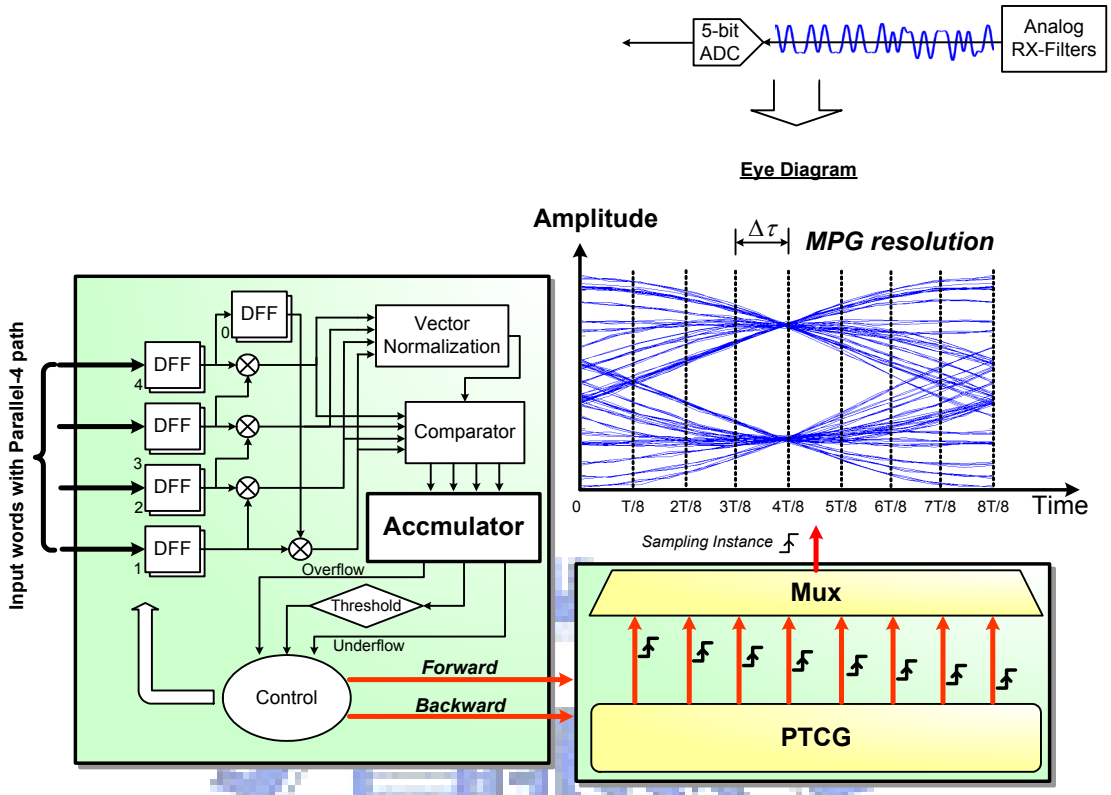


Fig. 6-6. DSTC block diagram and operation architecture

6-2-2 Phase-Tunable Clock Generator

An all-digital phase-tunable clock generator (PTCG) provides eight clock sampling candidates for phase selection, and outputs a specific one according to the ε_{opt} calculated in Eq. (4-23). This PTCG phase-tuning is achieved within a few cycles, and a clock output during this tuning period is glitch-free. Fig. 6-7 presents the proposed PTCG, which primarily consists of an ADPLL, a time-to-digital converter (TDC), and a cell-based delay line. Initially, the ADPLL is locked to the target frequency with the period T_{REF}. This generated clock is used as a reference source for multi-phase clock generation.

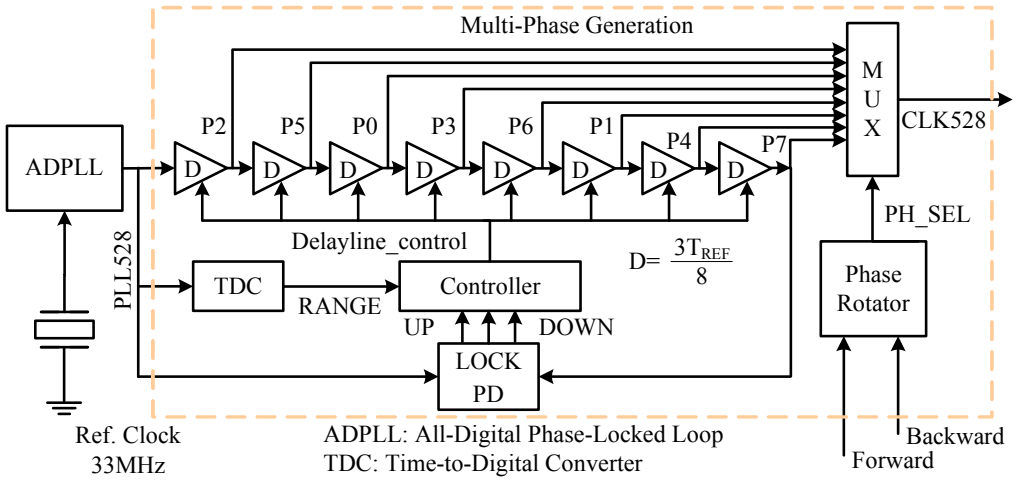


Fig. 6-7. The proposed phase-tunable clock generator (PTCG)

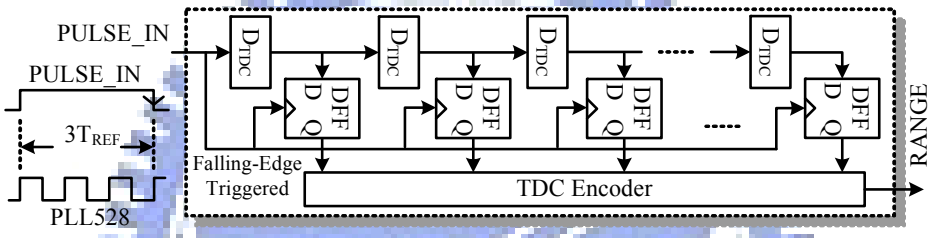


Fig. 6-8. The proposed time-to-digit converter (TDC) in the PTCG

In the earlier DLL-based multi-phase clock generation approach [53], the TDC enables a delay line locked to a single clock period (T_{REF}), giving a $T_{REF}/8$ in each delay stage. In a high-speed cell-based DLL design, however, maintaining such a short delay and a high resolution simultaneously is difficult. Thus, in this design, the TDC measures three periods and makes the DLL lock to $3\times T_{REF}$. After the DLL is locked, each delay stage presents a $3\times T_{REF}/8$ delay. Hence the minimum delay constraint for each delay stage (D) is extended to three times its original value. Moreover, the numbers in the numerator and denominator of the delay fraction 3/8 are not divisible by each other. As a result, the generated phase $P_{n|n=0\sim7}$ after each delay cell presents a unique fraction of the period.

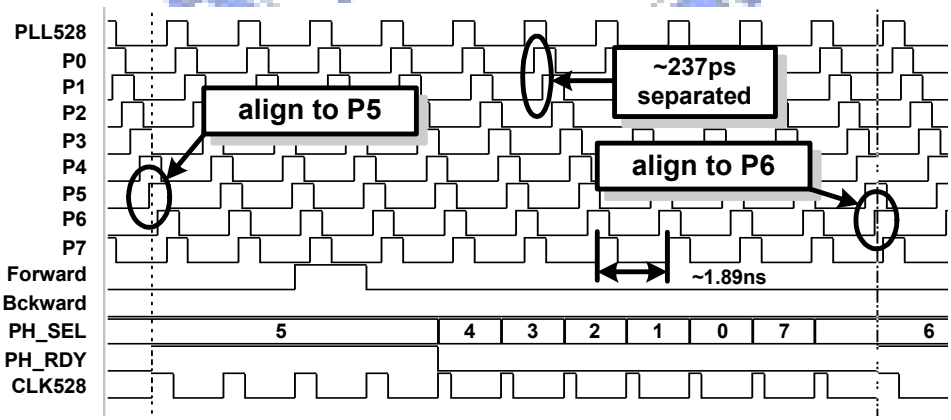
Fig. 6-8 shows the proposed TDC design architecture. The TDC takes the input PLL528 from the ADPLL. From this PLL528, a PULSE_IN signal is internally generated with a pulse width of $3T_{REF}$ as the TDC delay line input. A flip-flop is inserted between each pair of delay elements (D_{TDC}) in the delay line to latch data. The trigger event of all the flip-flops occurs at a PULSE_IN falling edge, and a latched data vector is encoded in a variable RANGE to the PTCG controller. According to the RANGE, the controller determines whether the periods of both PLL528 and PULSE_IN are correctly generated to avoid a false lock in this loop. Then, the PD of the PTCG continues fine-tuning the delay of the delay elements to improve the accuracy of the output phase position.

An example is shown here. The delay between the PLL528 and P0 is $3\times(3T_{REF}/8) = 9\times T_{REF}/8$. Therefore, the P0 phase shift to the PLL528 is $T_{REF}/8 = \{(9\times T_{REF}/8)$ modulus $T_{REF}\}$. The clocks P0~P7 are generated accordingly. This PTCG takes the estimated timing error ε, represented by Forward or Backward, from the DSTC to select a proper clock phase for ADC sampling. To avoid glitches in CLK528, a Forward command is converted cyclically to several Backward commands by a glitch-free controller, say a phase rotator block.

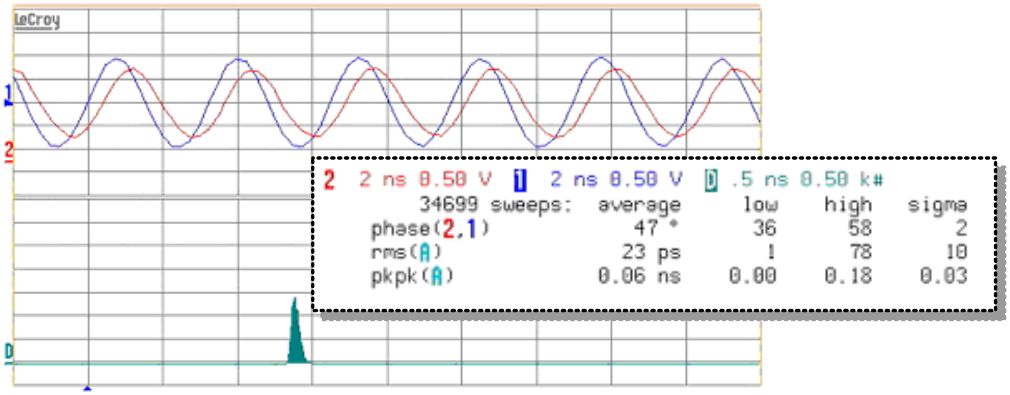
6-2-4 Simulation and Experimental Results

The proposed DSTC and PTCG are evaluated in a multi-band OFDM (MB-OFDM) based UWB system with low-density-parity-check (LDPC) code for error correction [54]. The signal bandwidth occupies 528MHz with QPSK and OFDM modulations, and the maximum data rate 480Mbps is selected for following simulations. The hardware circuits are designed in 0.13um standard CMOS process.

Fig. 6-9 shows both the simulated and measured waveforms from the PTCG design. This PTCG provides eight clock phases operating at 528MHz, and each consecutive phase is separated by about 237ps. As shown in Fig. 6-9(a), the output CLK528 is initially aligned to P5. When a command Forward is asserted, the selected output clock phase from the multiplexer (PH_SEL) counts down to zero and cyclically rotates back to P7 and P6. As the targeted clock phase is reached, a phase ready signal (PH_RDY) is activated to denote that the clock is updated from a new phase. To further explain the conversion of the Forward into several Backwards commands, P5 is again assumed to be initially selected as the system clock (CLK528), and the value of PH_SEL changes at the rising edge of the system clock, say P5. If CLK528=P5 is directly updated to CLK528=P6 before the rise of P6, a glitch may occur. Conversely, a change in CLK528 from P_n to P_{n-1} can avoid this glitch problem, except for the duty cycle change of CLK528 in the phase change intervals. The waveform in Fig. 6-9(b) plots the phase P_n and P_{n+1}. The measured RMS and P_k-P_k jitters are 30ps and 101ps, respectively.



(a)



(b)

Fig. 6-9. Generated PTCG waveforms: (a) the simulated waveforms and (b) the measured waveforms

To illustrate the glitch phenomenon, for example, at the instance of PH_SEL=5 to PH_SEL=6 as illustrated in Fig. 6-10, we have the value CLK528=P5 as shown in the brackets *(1)*. After PH_SEL is changed to 6, a logic-0 in P6 *(2)* push the CLK528 to zero. Afterward during the period of PH_SEL=6, the CLK528 follows the waveform appeared in P6 *(3)* and *(4)*. To prevent from this glitch, a Backward command guarantees a non-glitch behavior during the phase changes.

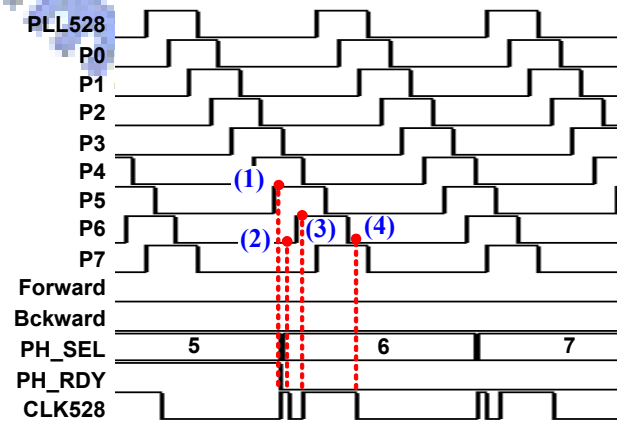


Fig. 6-10. The illustrations of a glitch generation in improper forward and backward controlling

The resulting PTCG power is 10.9mW [38] in the 0.13μm standard CMOS process. Fig. 6-11 and Table 6-1 presents both the performance and the power reduction in this work. The scheme herein offers an improvement of approximately 1.7dB SNR over that of the 2× interpolation method. In this MB-OFDM UWB system, the symbol-rate is 528MHz, and the 2× interpolation scheme requires a sampling rate of 1056MHz in the ADC circuits. The estimated power reduction is from 160mW×2 to 70mW×2 (for both I and Q paths) if the ADC circuits in [55] are taken into account. When the baseband processor power 31.2mW [38] is included, this reduced sampling rate results in a baseband power saving of (160×2-70×2+31.2)mW / (160×2+31.2)mW ≒ 40% if the ADC [55] is calculated together as shown in Fig. 6-11.

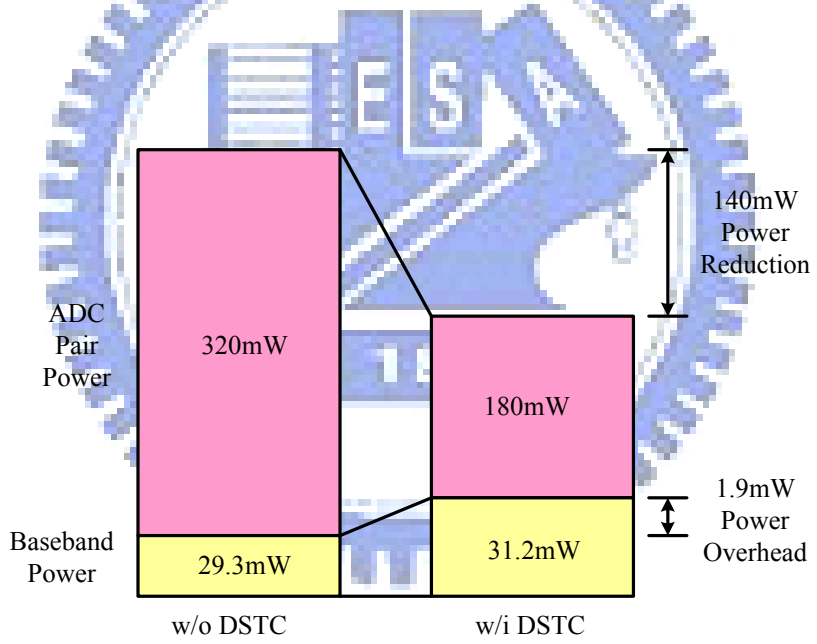


Fig. 6-11. The power reduction and overhead with DSTC

TABLE 6-1. SUMMARY OF POWER REDUCTION

	2× Oversampling Timing Sync.	This Work (DSTC+PTCG)
ADC Sampling Rate	1056MHz	528MHz
ADC Power (I+Q paths) [55]	160mW × 2	70mW × 2
Timing Sync. Circuits	High-rate interpolation computation	DSTC(1.9mW) PTCG(10.9mW)

This ADC power reduction from the reduced sampling frequency is roughly a general case. To clarify this, a list of ADC power from both the commercial product and academic papers is summarized. Those ADC chips from the industry, 10-bit and 8-bit ADCs, are shown in Table 6-2 and Table 6-3, respectively. The academic research result is shown in Table 6-4. The power consumption of those selected chips is illustrated in Fig. 6-12 with the supply voltage normalized to 3V. Moreover, the ADC power in Table 6-4 is further normalized to bit number = 8. This power-bit normalization is according to the equation (6-1) and (6-2).

$$FOM = Power / (2^{bit} * F_S) \quad \text{---------- for Nyquist ADCs} \qquad (6\text{-}1)$$

$$FOM = Power / (2^{bit} * 2 * ERBW) \quad \text{---------- for non-Nyquist ADCs} \qquad (6\text{-}2)$$

where F_S and ERBW represent the sampling frequency and effective resolution bandwidth, respectively. We apply a first-order least-square algorithm to find a curve for the data fitting. It is found that the ADC power consumption is reduced by 56.26% and 76.8% of 8-bit and 10-bit ADCs, respectively, and 51.2% of academic ADCs when the sampling rate is reduced to the half. These three power reduction ratios, 56.26%, 76.8%, and 51.2%, are comparable to the result (160mW×2-70mW×2)/(160mW×2) = 56.25% from the reference [38].

TABLE 6-2. A LIST OF 10-BIT ADC POWER

Industry 10-bit ADC circuits					
Part Number	Throughput (SPS)	Supply	Power (W)	Normalized Supply	Normalized Power (W)
LTC1850	1.25M	+5V	40m	+3V	14.4m
LTC2230	170M	+3.3V	890m	+3V	735.54m
LTC2231	135M	+3.3V	660m	+3V	545.45m
LTC2232	105M	+3.3V	475m	+3V	392.56m
LTC2233	80M	+3.3V	366m	+3V	302.48m
LTC2234	135M	+3.3V	630m	+3V	520.66m
LTC2236	25M	+3V	75m	+3V	75m
LTC2237	40M	+3V	120m	+3V	120m
LTC2238	65M	+3V	205m	+3V	205m
LTC2239	80M	+3V	211m	+3V	211m
LTC2240-10	170M	+2.5V	445m	+3V	640.8m
LTC2241-10	210M	+2.5V	585m	+3V	842.4m
LTC2242-10	250M	+2.5V	740m	+3V	1065.6m
LTC2250	105M	+3V	320m	+3V	320m
LTC2251	125M	+3V	395m	+3V	395m

TABLE 6-3. A LIST OF 8-BIT ADC POWER

Industry Device 8-bit ADC circuits					
Part Number	Throughput (SPS)	Supply	Power (W)	Normalized Supply	Normalized Power (W)
AD9283-100	100M	+3V	120m	+3V	120m
AD9054A-135	135M	+5V	700m	+3V	252m
AD9054A-200	200M	+5V	781m	+3V	281.16m
AD9481	250M	+3.3V	618.8m	+3V	511.41m

TABLE 6-4. ADCS REPORTED IN ACADEMIC PAPERS

Reference Paper	Throughput (SPS)	Bit	Supply	Power (W)	Normalized Bit	Normalized Supply	Normalized Power (W)
[72]	1.6G	8	+1.8V	1.4	8	+3V	1958.3m
[73]	600M	8	+1.8V	200m	8	+3V	555.6m
[74]	220M	10	+1.2V	135m	8	+3V	540m
[74]	110M	10	+1.2V	90m	8	+3V	360m
[75]	1G	11	+1.2V	250m	8	+3V	826.5m
[76]	800M	11	+1.3V	350m	8	+3V	985.9m
[55]	1200	6	+1.5V	160m	8	+3V	1137.8m

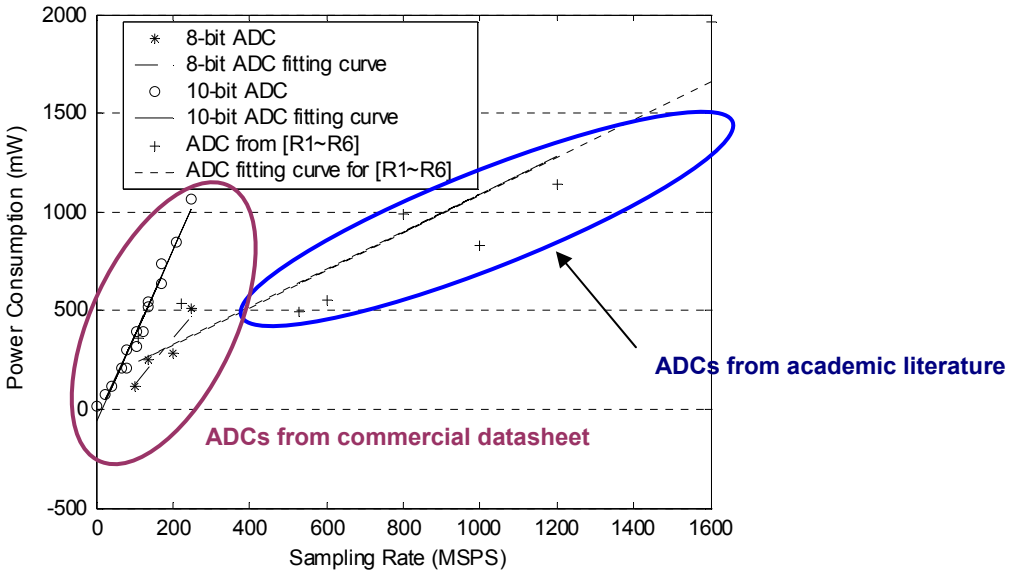


Fig. 6-12. Pie chart of RX signal power

Therefore, the overall hardware performance may be further summarized. Note that the proposed symbol-rate synchronization method requires both the DSTC and PTCG circuits for timing calculation and clock generation that consume the power of 1.9mW and 10.9mW, respectively. They occupy 6.09% and 34.93% of the baseband chip power, respectively, as illustrated in Fig. 6-13. This PTCG provides the necessary

clock source that is mandatory in a wireless system. This building block is not considered as an overhead circuit since it only slightly changes the clock generation behavior from a single clock phase to multiphase clock signals. As a result, the only overhead of the computation circuits may be regarded as the DSTC. The DSTC is required when the symbol-rate sampling is performed for ADC power saving. It is calculated that the DSTC circuit occupies 6.09% of the baseband chip. Fig. 6-14 presents a microphoto of this baseband test chip. The DSTC is designed in the synchronizer part. The PTCG includes both the multiphase clock generator and the all-digital phase-locked loop for clock generation. Table 6-5 shows the summary of this test chip [38].

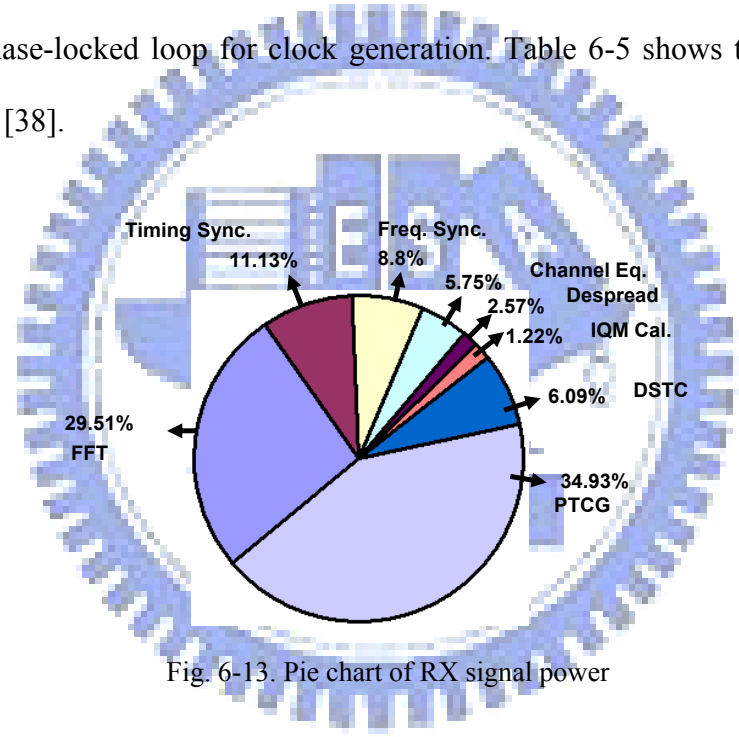


Fig. 6-13. Pie chart of RX signal power

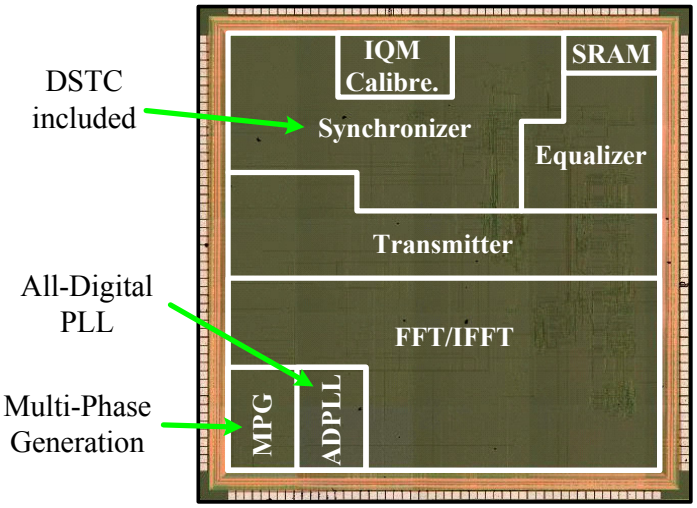


Fig. 6-14. Micro-photo of the test chip in 0.13 μm standard CMOS technology

TABLE 6-5. THE IMPLEMENTATION AND FUNCTION SUMMARY

Technology	Std. 0.13um CMOS 1.2V core, 3.3V I/O
Die Size	3.975mm×3.980mm
Package	280-pin CQFP
Transistor Count	2.25M
Max. Data Rate	480Mb/s
Core Power @ 480Mb/s (TX/RX)	15.8/31.2mW
PTCG Resolution	236.7ps

Finally, an emulation platform is applied to demonstrate the decoded QPSK symbols in the receiver side. The output shown in the serial data analyzer (SDA) corresponds to the decoding output of the manufactured silicon chip. As a result, the decoded QPSK symbols illustrated in a constellation map can be found in the Fig. 6-15. The chip testing of this MB-OFDM UWB work is achieved by the Agilent 93000 tester for logic pattern testing and power measurements as illustrated in Fig. 6-16.

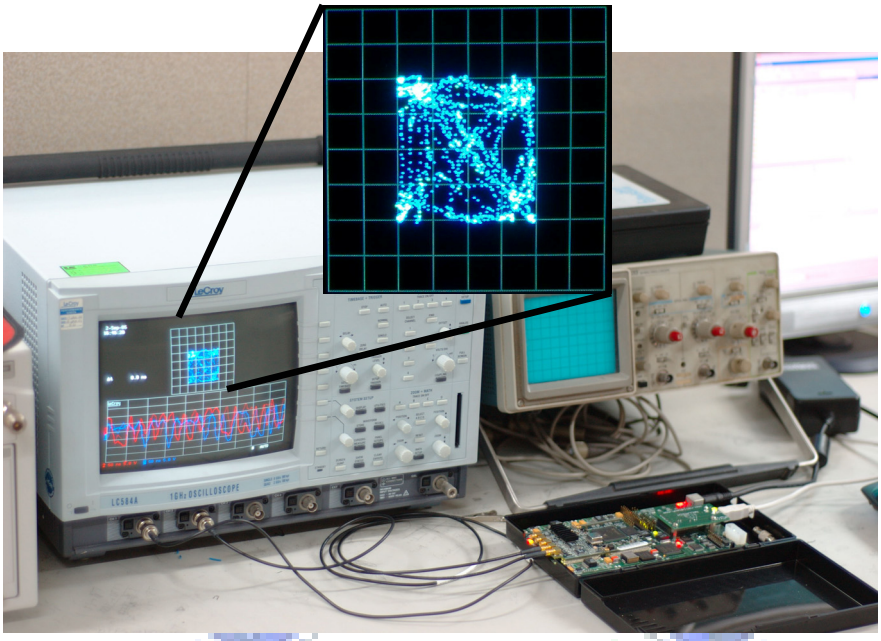


Fig. 6-15. The decoded constellation example

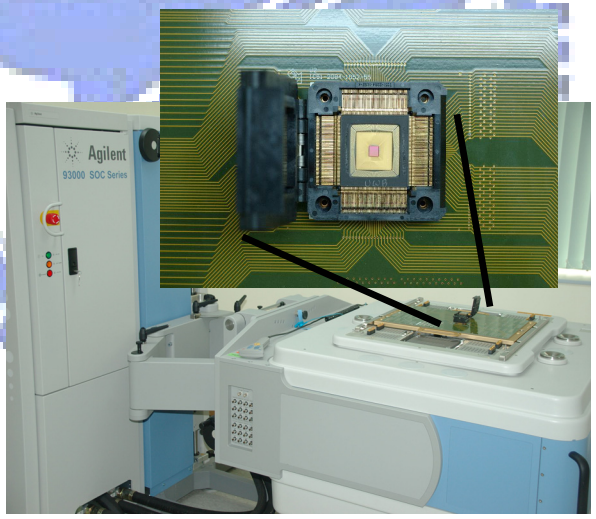


Fig. 6-16. Chip testing platform

6-3 Case 2: WBAN WiBoC baseband processor

6-3-1 Low Power Design Flow

The low power design flow is applied to the WiBoC baseband processor implementation. So, this implementation flow will be illustrated first before a further explanation of the designs of the baseband processor.

The baseline flow of a digital cell-based circuit design can be described in the hardware description language (HDL) register transfer level (RTL) description, logic synthesis for circuit mapping, (automatic) place and route (APR) for layout design, formal checks for logic consistency, timing analysis, implementation checks in terms of design-rule-check (DRC) and layout-versus-schematic (LVS) checks. For a more flexible implementation for different power budget designs, a low power design flow, say voltage and power planning, is introduced into this work as a standard implementation approach. Therefore, the resulted timing and power consumption will be met at the balance for this low-rate and small duty-cycle (active/inactive ratio) hardware design. The applied low power flow includes the variable voltage-domain implementation. Moreover, in the deep-submicron circuit process, the leakage power occupies a large ratio of the total power, so the power gating scheme is definitely included to minimize the leakage power in the inactive circuits. As a result, the power-domain planning is also considered in the whole chip organization so that every building block may be active or inactive dynamically accompanied with the voltage applied or not. To achieve the voltage and power domain organization, the circuit synthesis and APR are the main parts in the designs, and they will be focused in the following discussion.

(a) Voltage-Domain and Power-Domain Circuit Synthesis

The planning of voltage-domain and power-domain partitions requires the timing library files to provide the necessary timing information in every possible operation conditions, ex: supply voltage, environment temperature, and manufacturing process. As a result, an N-voltage-domain partition requires N set of timing library, and each of them defines the best and worst operation conditions for corner timing calculations. In the circuit synthesis, the possible voltage domains are first specified, and each voltage domain defines what building blocks or modules are included in the voltage domain. After the mappings between voltage domains and design modules in the forms of HDL RTL, each voltage domain is required to assign a set of timing library to achieve the target timing in the operation conditions. This is illustrated in Fig. 6-17. During the synthesis, the constraints of clocking-speed, interference constraints, and switching or leakage power should be specified. Therefore, the synthesizer will report the timing, area, and power information of the design netlist, and the mapped netlist is generated in accordance with the desired voltage and timing constraints.

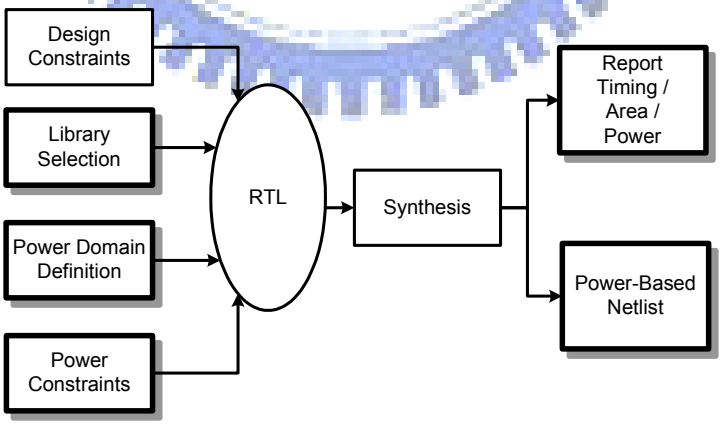


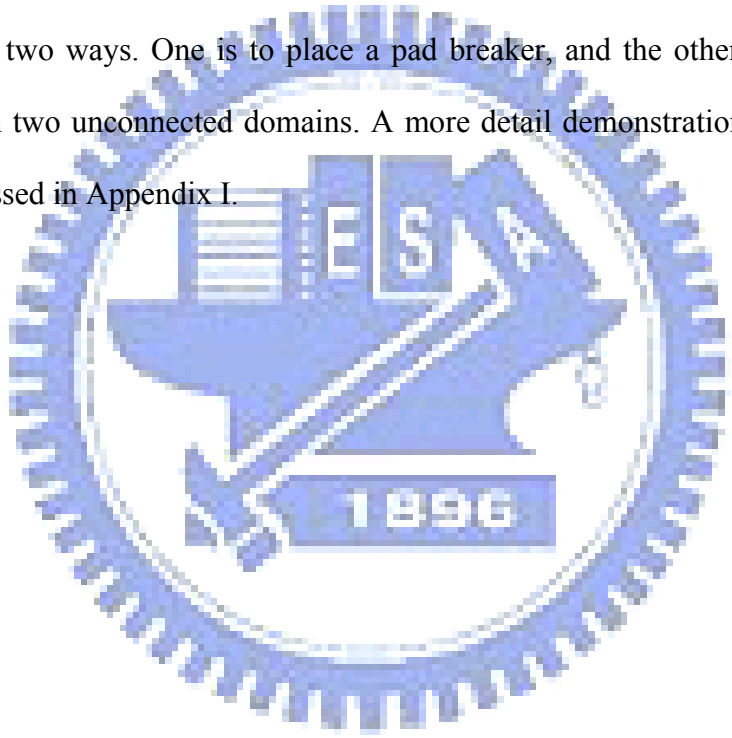
Fig. 6-17. Circuit synthesis in the low-power design flow

(b) Voltage-Domain and Power-Domain Circuit Automatic Place-and-Route

The synthesized netlists with specific mapping libraries are used for circuit layout designs. A preparation of corresponding timing library is also required for the APR process. Those are used to re-calculate the timing information of the circuits after detail wire routings between end-points to end-points. The constraint descriptions are also necessary for the layout process. Moreover, the process characteristics have to be provided since the property of each foundry process may vary to each other.

The main design part in the APR flow is the power-domain planning instead of the voltage-domain partitions that are done in the synthesis stage. So, the floor-planning has to specify the location and geometry size of each power domain. Each power-domain may vary in terms of voltages, always-on, or on-off behaviors. If a pair of power domain is operated at different voltage level, a level shifter has to be inserted to provide the physical voltage level transformation. When a power-domain is operated in possible active or inactive conditions, the power gating cells are inserted to cut off the supply current paths for minimizing circuit sleeping current. The isolation cell is necessary when an always-on domain is not intended to be interfered by the unknown signals from the power-off domain. Thus, an isolation cell is placed between power-off domain and always-on domain so that this cell isolates the unknown signals from the power-off domain and provides a preset definite signal level to the target operation modules. The ordering of operation flow is briefly described in Fig. 6-18. The extra circuits from level shifters and power gating cells contribute additional circuit loading and propagation delays. Moreover, the driving capability of the level shifter and power gating cells will destroy the overall timing

behavior if not carefully designed. After the placements and insertions of level shifters and power gating cells, the conventional APR flow is applied, i.e. logic cell placements, pre clock tree synthesis (pre-CTS), CTS, post-CTS, global connection routing, and deep-submicron signal integrity re-synthesis and re-routing. When it is necessary to measure each power domain supply current separately, the power pads are to provide their own power domain without connections with the power pads for the other power domains. Accordingly, the input, output, and power pad designs are subject to modify. The approaches to disconnect the power pads for different power domain have two ways. One is to place a pad breaker, and the other is to cut filler pads between two unconnected domains. A more detail demonstration of this design flow is discussed in Appendix I.



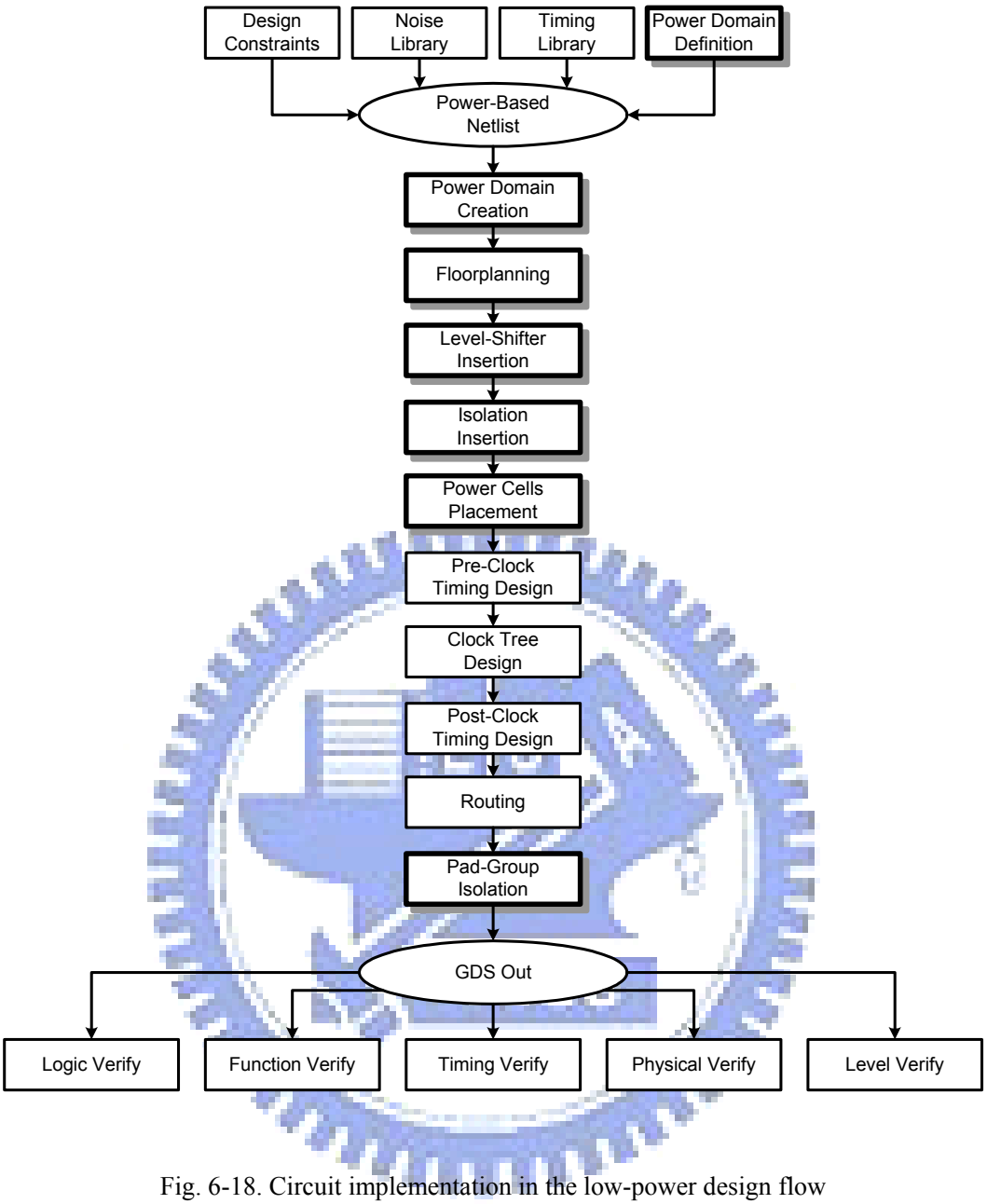


Fig. 6-18. Circuit implementation in the low-power design flow

Here shows some example topologies of a level shifter, an isolation cell, and a power gating cell. Fig. 6-19 illustrates a level shifter design. The basic ideal of the level transformation is that a pair of inverters powered by V1 provides signals to another pair of inverters which are powered by a voltage V2. An inverter normally changes its state when an input level reaches Vdd/2. In the level shifter assuming a level is going to be transferred from low voltage (V1) to high voltage (V2), it is possible that a transition level V1/2 is much less than another transition level V2/2 of

the inverter powered by V2. This will results in a failure of level shifting. Accordingly, it is necessary, for example, to provide PMOS headers that cut off the power path of an inverter to be able to sense the threshold voltage. This added header definitely provides an additional MOSFET resistor, and this will result in a non-V2 high level in an output. So, the later cascaded inverter and buffers are used to guarantee a correct signals level as well as sufficient output driving ability.

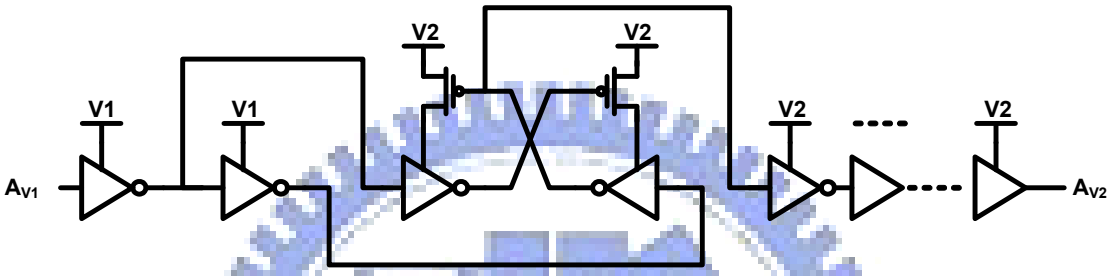


Fig. 6-19. The example circuit of a level shifter

An example isolation circuit topology is shown in Fig. 6-20. The isolation cell is simple but important in a correct power planning design. When an active-low enable signal (E) applied to the cell, the signal level in the path from A to Z is transparent. On the other hand, when the domain in the left-hand side is powered off, the signal A may possibly generate an unknown level that may affect the normal operation in the always-on circuits. Accordingly, a high-level voltage is applied to the enable signal (E) when the power-off domain becomes sleep. Therefore, another transmission gate becomes active to bypass the ground level to the output Z, guaranteeing a definite signal level provided to the active domain. Note that a PMOS header is also concatenated to the interface inverter. This is due to an unknown signal level A may result in a short current path in the interface inverter. This will destroy the motivation of leakage saving in turning off some inactive design modules.

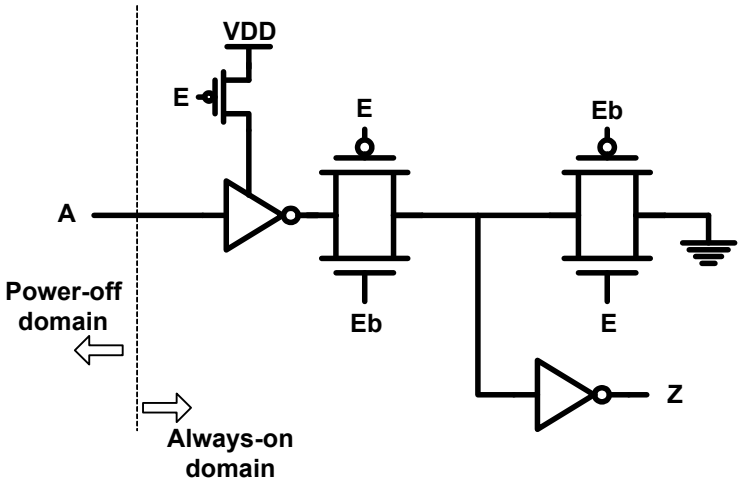


Fig. 6-20. The example circuit of an isolation cell

Fig. 6-21 shows a conceptual topology of a power gating cell. When the SLEEP signal turns on the MOSFET transistor, the operation current is provided from VDD to Virtual_VDD so that the descendant circuits are powered on for activity. On the contrary, a turned-off MOSFET transistor cuts off the power path so that a minimum static current will leak to the descendant modules connected on Virtual_VDD. The exploration of the transistor for power gating can be seen in Appendix II that an in-depth discussion on the power gating cell is provided. It reveals some properties and behaviors of a NMOS or a PMOS power gating cell as well as a header or a footer power gating cell.

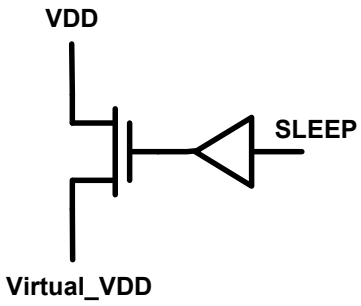


Fig. 6-21. The example circuit of a power gating cell

6-3-2 MT-CDMA Baseband Processor

The following designs are based on the discussed low power flow. Fig. 6-22 shows the proposed ubiquitous personal healthcare inspector (uPHI) wireless sensor node (WSN). This transmitter may connect with variant possible sensor categories and achieve a maximum 143kbps data rate for maximum 10-WSN coexistence, providing large interference-rejection capability and better system reliability. Because uPHI-WSN/CPN communicates with a data rate much higher than a human body's signal rate in this work, a WSN stays asleep for most of time (sleep-phase) and transmits data in a burst mode (active-phase). Therefore, leakage power minimization is emphasized for this long-sleep operation. When the electrocardiogram (ECG) signal is considered as a body signal source with sampling rate 16-bit 500-samples/s, a 2048x16-bit SRAM is designed in a WSN. This SRAM size reaches optimum leakage saving efficiency, resulting in a 6.96% active-sleep duty cycle. The sampled signals from the sensor are modulated by QPSK with 16-point IFFT, and the subcarrier allocation follows the conjugate-symmetric rule to further reduce 50% DAC and front-end circuit area and power. Then, the baseband signal is transmitted with 5M chip/s. In the CPN of receiver side, the wideband ADIC IQM calibration circuit is provided to compensate the gain and phase distorted signals. Also, a DSTC is also applied for best sample timing search with the aid of the PTCG circuit, which provides 5MHz 8-phase even spaced clock phases for selection. Each clock phase is separated by 25ns.

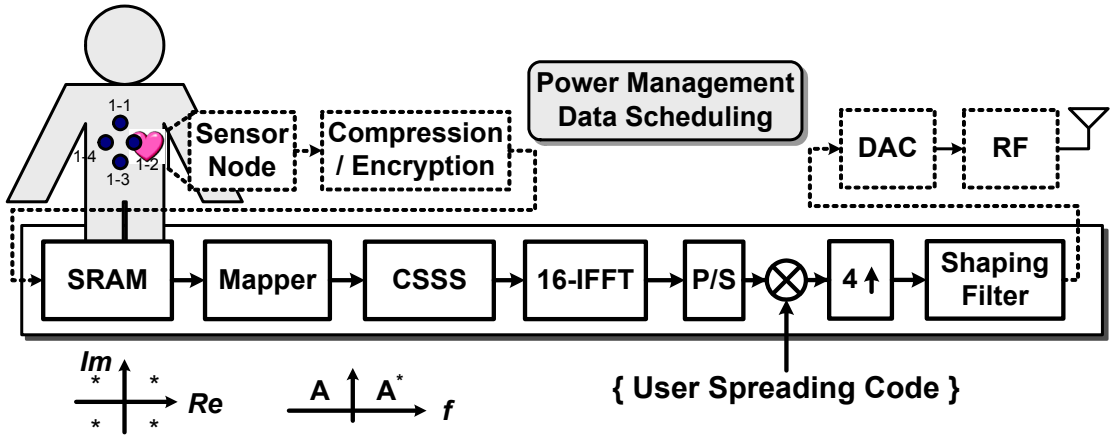


Fig. 6-22. The block diagram of the MT-CDMA baseband transmitter

The reason to emphasize the duty cycle is that the SRAM usually takes quite a long time to store body signals due to body's low information rate. Thus, the modulator stays idle for a long time and wastes lots of power due to the leakage current. To decide this duty cycle and minimize the leakage power, we first define a parameter as leakage saving efficiency, LSE. This LSE is formulated to represent leakage power reduction ratio as expressed by

$$LSE(w) = \frac{MP \times T_{off}}{MP \times T_{off} + SP \times (T_{off} + T_{on})} \tag{6-3}$$

Let the modulator leakage power and SRAM leakage power be defined as MP and SP respectively. Ton and Toff stand for WSN active-phase and sleep-phase, respectively. Thus this LSE gives the ratio of the leakage power in sleep-phase to the overall circuit power, as shown in Fig. 6-23. Because the modulator is designed to be able to turn off the power during the sleep-phase, this LSE becomes an indicator of power consumption which can be saved. The determination of the SRAM size can be explained as follows. As the SRAM size is enlarged, it takes longer time to gather and store the sampled body signals. Due to the non-sleep fact of the SRAM operations, a

larger SRAM size also implies a larger area of SRAM that may contribute the leakage current at the same time. The modulator is also required to take longer time to complete each signal transmission due to larger amount of data source. The LSE indicator is looking for the optimum codeword size that the WSN may take minimum leakage power to transmit each information bit. In other words, the balance between the always-on SRAM leakage and the burst-on modulator leakage is found. This trade-off between the SRAM and modulator leakage power are represented as the LSE indicator curve as illustrated in Fig. 6-24. It is found that the most efficient SRAM size is about 3000x16 (bit). For easier modulator controlling, a size consist of a power-of-two amount is preferred. Accordingly, a 2048x16 (bit) SRAM is selected as the MT-CDMA buffer space for the body signal storage.

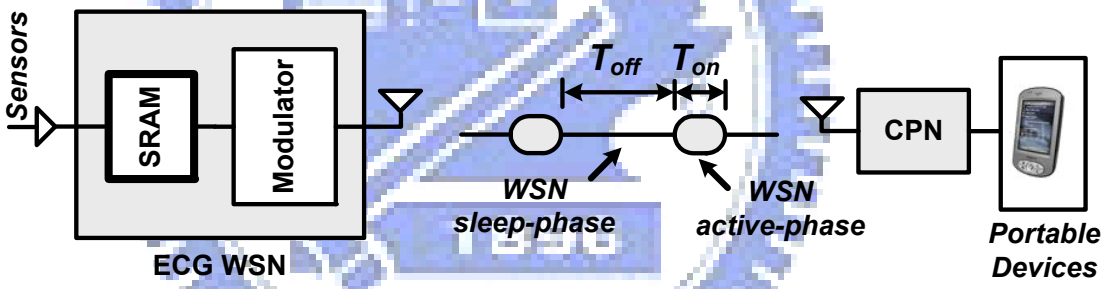


Fig. 6-23. An illustration on the sleep and active phases in a WSN-CPN transmission link

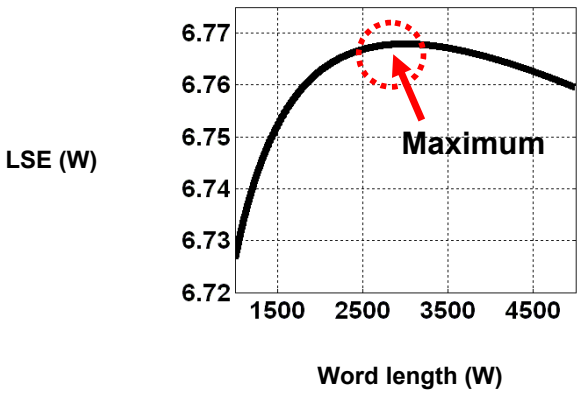


Fig. 6-24. The leakage saving efficiency to the SRAM word length size

Fig. 6-25 shows the brief block diagram in a MT-CDMA WSN design, including main functional blocks, MVTCMOS, MSV domains, and DCG-PGC. In the sleep-phase, the SRAM continuously stores the sensed body-signals. As the SRAM free-space approaches full, the MT-CDMA modulator is powered-on (active-phase) to modulate those signals via main function blocks, including constellation mapper, conjugate-symmetric frequency-domain spreading, IFFT, and time-domain user-code spreading (Fig. 6-22). To minimize the dynamic power consumed in the active-phase, the supply voltage for the modulator is scaled from 1.2v to 0.8v, which is implemented in a low-Vt cells to enable low voltage supply operation, resulting in 60.89% dynamic power reduction. To further reduce the modulator's leakage power consumed during the sleep-phase, the column-style NMOS DCG-PGC is distributed between the global VCC and local virtual-VCC(VCCV) as a power controlling switch to cut off any possible leakage current path, resulting in 99.92% leakage power reduction. In the always-on power domain, only low-rate operation components are implemented, including both SRAM and control unit, which consumes more leakage power than dynamic. Therefore, low-leakage (high-Vt) cells are selected for this domain. Between these two power domains we insert level-shifter for correct signal level and isolation cells for tie-high/low signal level when the signal source comes from a power-off domain.

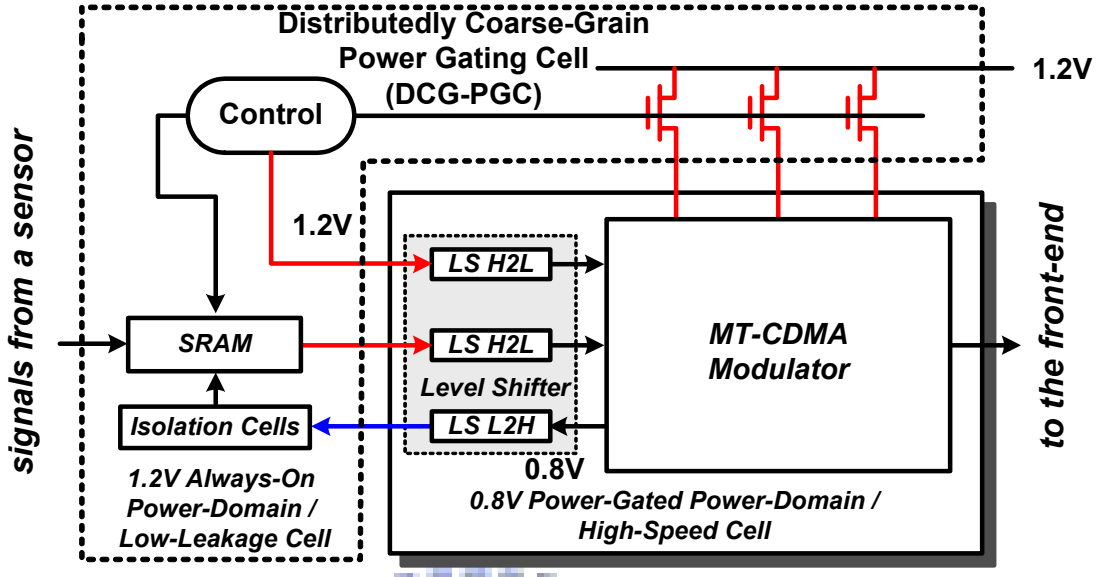


Fig. 6-25. Abstract view of the circuit block partitions in terms of power domains

Fig. 6-26 shows the CPN architecture. A DSTC is applied to enable ADC circuits sampling incoming signals with the symbol rate and maintain the sampled signal integrity. This is achieved by a PTCG, which consists of an ADDLL providing 8-phase even-spaced clock phases for selection. This DSTC approach prevents ADC circuits from sampling data with Nyquist rate, saving 43.75% ADC power. To further improve the system reliability and signal decoding quality, a wideband adaptive I/Q-mismatch calibration is applied with 2dB gain error (GE) and 20^{o} phase error (PE) calibration range [38][65].

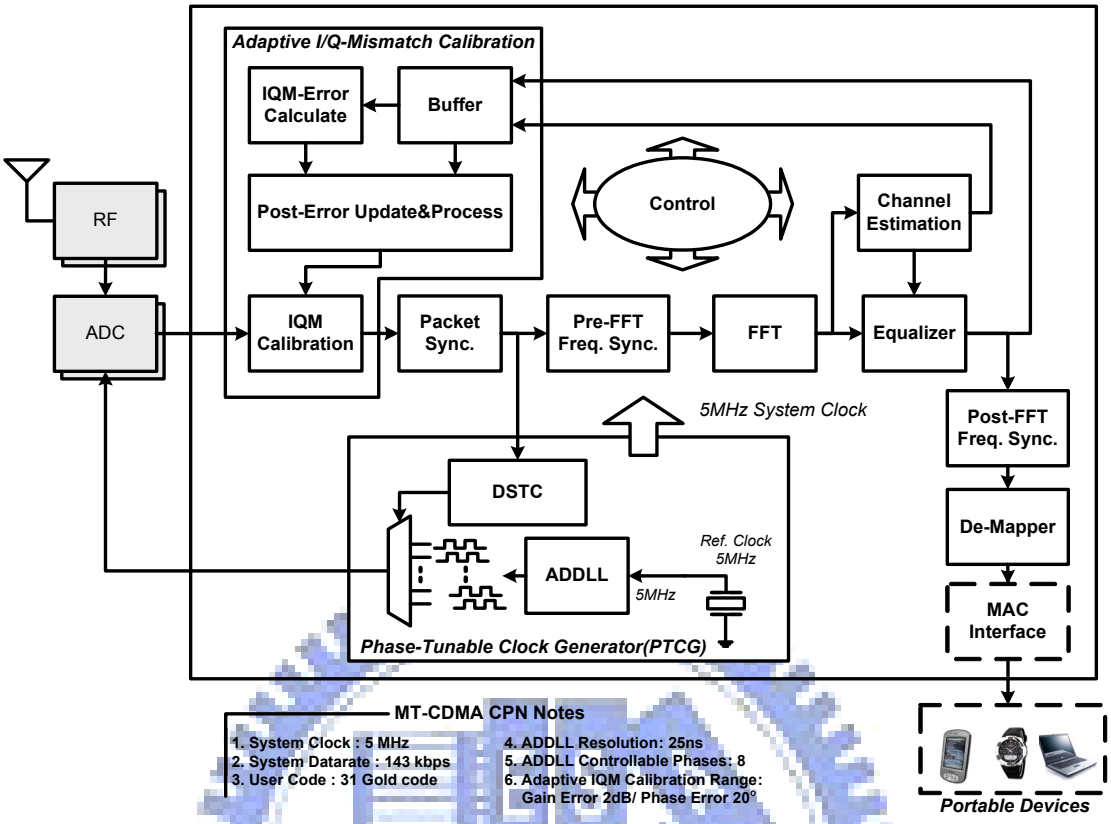


Fig. 6-26. The block diagram of the MT-CDMA demodulator in the CPN circuit

A more detail illustration of Fig. 6-26 is shown in Fig. 6-27 and Fig. 6-28. The CPN continuously detects the possible in-coming signals. In other words, it is an always-on non-sleep circuit. So, it is not suitable to apply the power gating approach in the CPN side. For possible power reduction, voltage scaling is applied to the whole circuit. Moreover, digitally-aided calibration is also considered to balance the design effort among the front-end, data-converter, and baseband circuits. These include the proposed adaptive I/Q mismatch calibration for performance improvement and dynamic sample-timing control for power reduction. In the dynamic sample-timing control, it enables the ADC circuits sampling signals in the symbol rate rather than the Nyquist rate to reduce the ADC power due to the lower sampling frequency. To maintain the sampled signal integrity, the DSTC is capable of providing 8 different

sampling phases for selection to drive ADC circuits. This mechanism starts right after the packet is detected from the short preamble field. Then the rest of the short preamble is fed to the phase search block to find out if this sampling phase is best or not in terms of sampled quality. If not, then a lead or lag command is sent to a phase-tunable clock generator for a different clock phase selection. Therefore, a better sampling instance is decided, and this also guarantees good qualities for later sampled signals. A more detail discussion on the DSTC may be further referred to section 6-2 for the MB-OFDM baseband processor design.

The CPN design also includes the wideband ADIC IQM calibration circuits, as illustrated in Fig. 6-28. In the adaptive I/Q mismatch calibration block, it compensates the remaining gain and phase errors from the front-end circuits in an all-digital manner. This mechanism starts after the timing synchronization completes. This calibration circuit is divided into two parts, one is estimation and another is compensation. In the estimation part, it takes and correlates the estimated channel response and equalized preamble from the preamble-1 and preamble-2 fields. These two fields have an odd and an even phase symmetric properties, respectively. The correlated results are stored and mutually divided. Then a signal gain and an image gain are calculated accompanied with a step size to achieve the adaptive loop. The signal gain and also the image gain are functions of gain and phase errors. Therefore, these two parameters are sent to the compensation block to compensate and extract the image interference in the incoming signals.

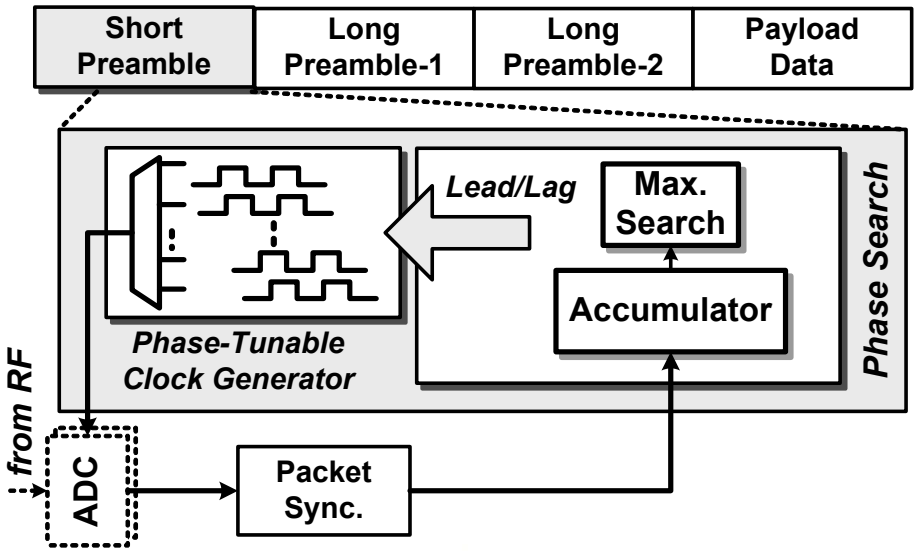


Fig. 6-27. The DSTC algorithm applied to the MT-CDMA demodulator in the CPN side

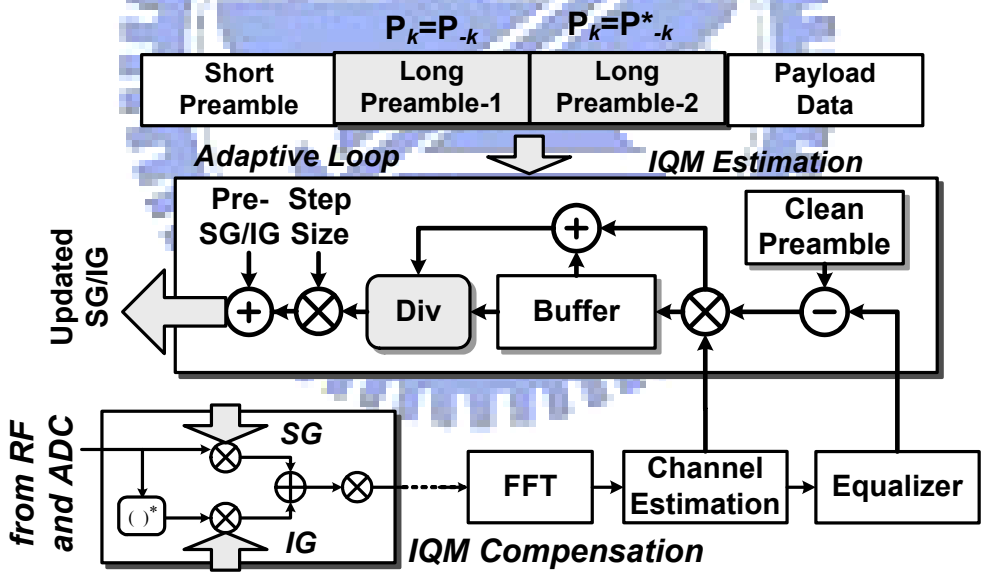


Fig. 6-28. The adaptive ADIC I/Q mismatch calibration applied to the MT-CDMA demodulator in the CPN side

Fig. 6-29 shows the MT-CDMA modulator power profile during active-to-sleep and sleep-to-active phases. In the sleep phase, the modulator sinks only 15.2nA with

the proposed DCG-PGC design, resulting in 99.92% leakage reduction compared to the non-DCG-PGC approach. The averaged simulation current consumed 95.8uA and 18.89uA in the active-phase and sleep-phase, respectively. The turned-on time takes 9.16ns for VDDV to restore to the stable voltage level, as shown in Fig. 6-30.

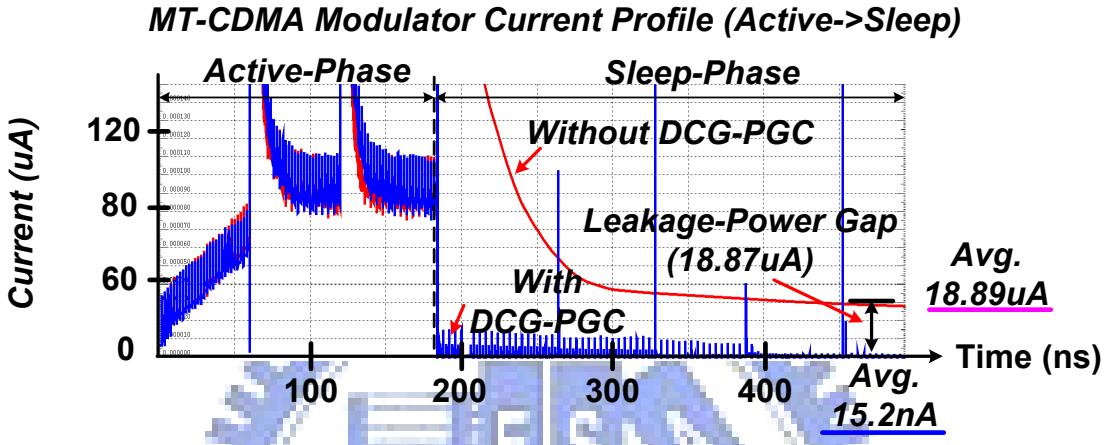


Fig. 6-29. The current profile of the MT-CDMA modulator in the active and sleep phases

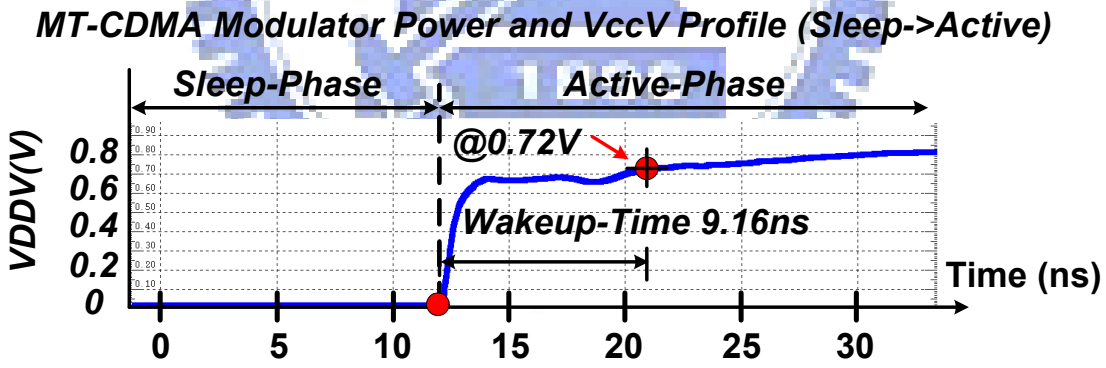


Fig. 6-30. The virtual VDD profile from sleep phase to active phase

Table 6-6 and Fig. 6-31 provide the area percentage of each building block or module in the CPN side. Since this MT-CDMA has a de-spreader synchronizer operating at 5MHz frequency that are 31 times higher than that of baseband signal demodulation processing operating at 5MHz/31 frequency, resulting in a higher area percentage

occupied in the synchronization part (USYNC module), say about 55%. The DSTC operation is included in the synchronization part. The ADIC IQM calibration occupies an about 7.12% of the total area.

TABLE 6-6. THE AREA OF THE MT-CDMA CPN CIRCUIT

Module	Area(um^2)	Percentage (%)
URX	517189	100
USYNC	279662	55
UCFO	38127	7.37
UCHANNEL_EST	57959	11.2
UPHASE_RECOVERY	52285	10.11
UFFT16_DIT	43971	8.5
UEQ	5909	1.14
UIQM	36841	7.12

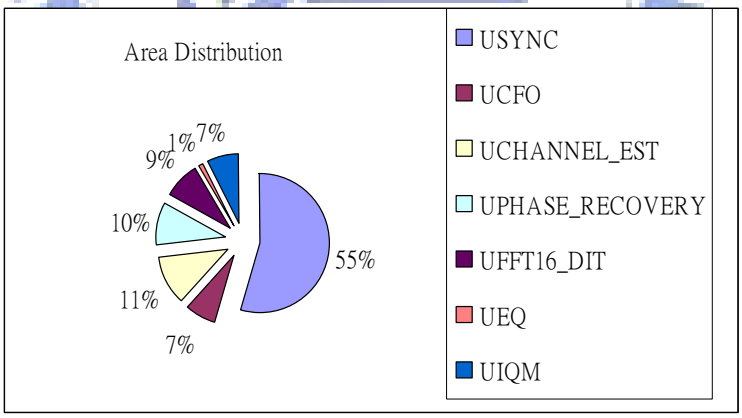


Fig. 6-31. The pie chart of the area percentage of a MT-CDMA demodulator in a CPN circuit

Table 6-7 and Fig. 6-32 also reveal the power distribution of the whole CPN chip. It is also found that the synchronization part (USYNC) also occupies the most power

percentage of the total CPN chip, say 83%. The wideband ADIC IQM calibration consumes a small portion, about 1.58%, of total power.

TABLE 6-7. THE POWER OF THE MT-CDMA CPN CIRCUIT

Unit = nW	Leakage	Dynamic	Total	Percentage (%)
URX	162704	1971789	2134493	100
USYNC	92272	1640411	1732683	83
UCFO	10642	79071	89713	4.2
UCHANNEL_EST	17177	84845	102022	4.78
UPHASE_RECOVERY	15801	46131	61932	2.9
UFFT16_DIT	13245	53504	66749	3.12
UEQ	1620	7565	9185	0.43
UIQM	11178	22587	33765	1.58

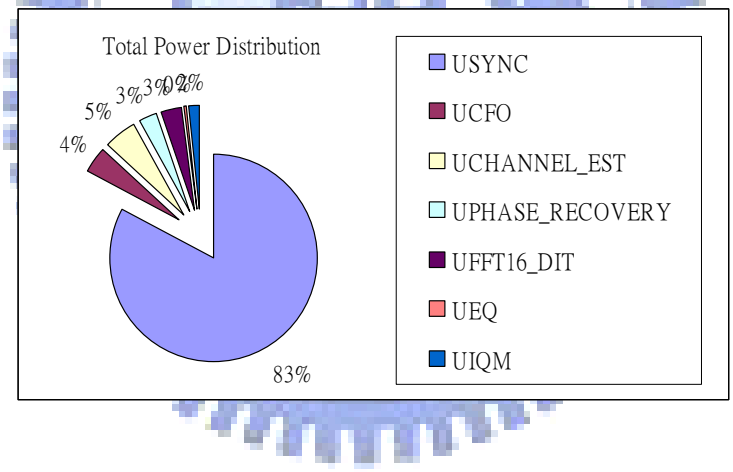


Fig. 6-32. The pie chart of the power percentage of a MT-CDMA demodulator in a CPN circuit

As to the dynamic and leakage power ratio, the statistics are shown in Fig. 6-33 and Fig. 6-34. In the applied 0.13μm circuit process, the static power occupies less than 10% power the total chip power. The leakage versus the dynamic power is shown in Fig. 6-34 in terms of the designed modules.

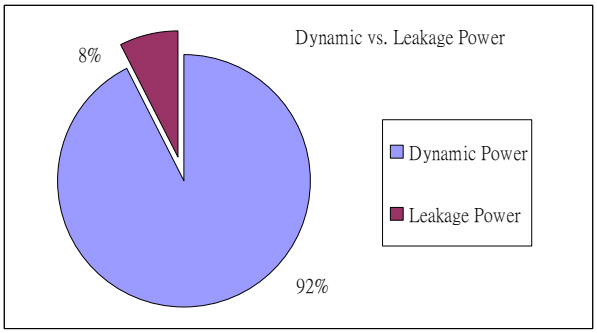


Fig. 6-33. The pie chart of the power percentage of a MT-CDMA demodulator in a CPN circuit in terms of dynamic power and leakage power

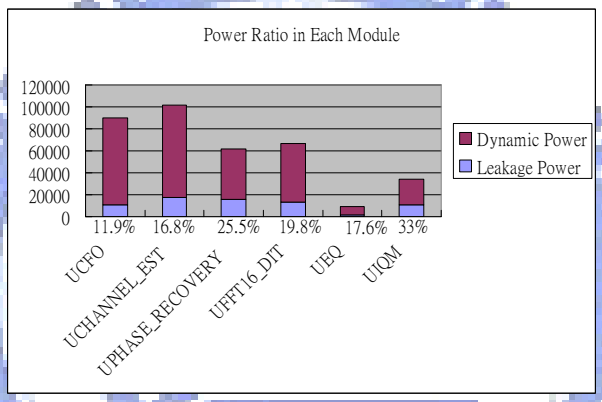
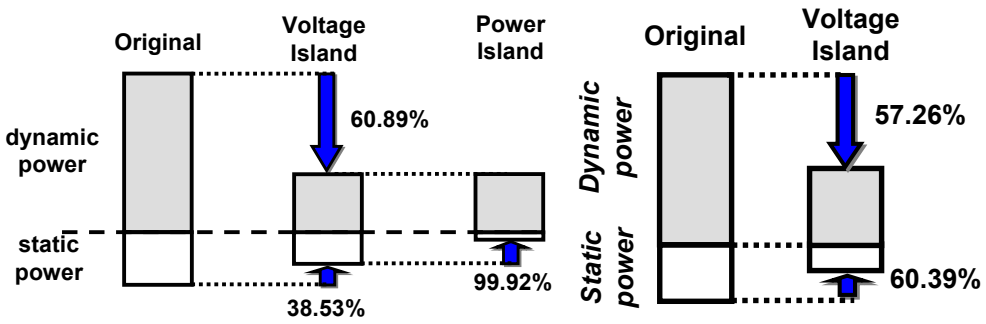


Fig. 6-34. The bar chart of the dynamic and leakage power in each operation module

So, the power reduction is shown in Fig. 6-35 in terms of dynamic and static power. By the voltage island approach, both dynamic and static power consumptions are reduced by 60.89% and 38.53%, respectively. With the power island approach, static power is further reduced by 99.92%. The circuit consumes leakage power in most of the time because this system is operated in a small system duty cycle, say 6.96%. Therefore, this static power reduction plays an important role. So, these power reductions meet the body area network's low power requirements in the WSN side. In the CPN side, a voltage island is applied to scale the supply voltage from 1.2v to 0.8v, resulting in a 57.26% dynamic power and 60.39% static power reduction.



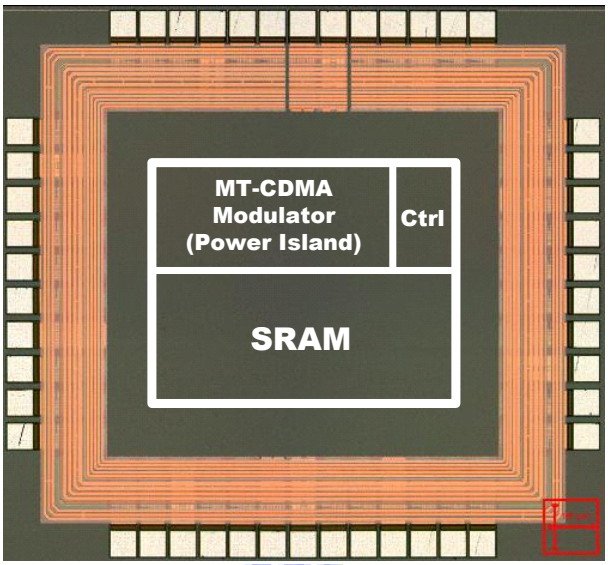
(a) (b)

Fig. 6-35. The power reduction in the (a) WSN and (b) CPN

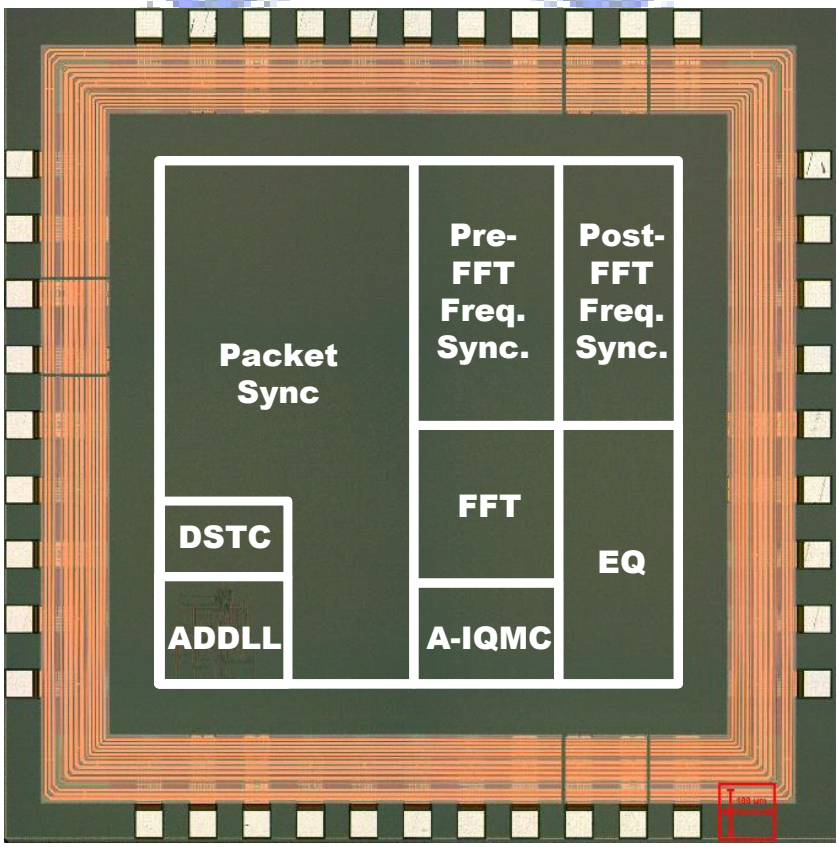
TABLE 6-8. THE MT-CDMA TRANSCEIVER CHIPSET SUMMARY

Item	Features
Technology	0.13μm High-Speed/ Low-Leakage CMOS
Max. Data Rate	143kbps
Max. Signal Bandwidth	5MHz
Die Size	1252μm x 1358.8μm (WSN) 1842μm x 1842μm (CPN)
Measure Core Power	21μW @ 0.8V (WSN) 566.4μW @ 0.8V (CPN)
ADIC IQM Error Tolerance Gain Error / Phase Error	2dB / 20°
PTCG Phase Number	8

The proposed MT-CDMA WBAN baseband transceiver is fabricated in 0.13μm 1P8M CMOS process. Table 6-8 shows the chip summary and Fig. 6-36 shows the chip micro-photo. The MT-CDMA is designed in the proposed uPHI system for 10-WSN/CPN 1-meter reliable coexistence. For enduring monitoring, the WSN consumes 21uW with 60.89% dynamic and 99.92% leakage power reduction (total 90.91% power reduction in a 6.96% duty cycle) by the proposed duty-cycle control with power island approach. Fig. 6-37 illustrates the chip measurement scenario.



(a)



(b)

Fig. 6-36. Micro-photo of the WSN and CPN chip set in 90nm standard CMOS technology

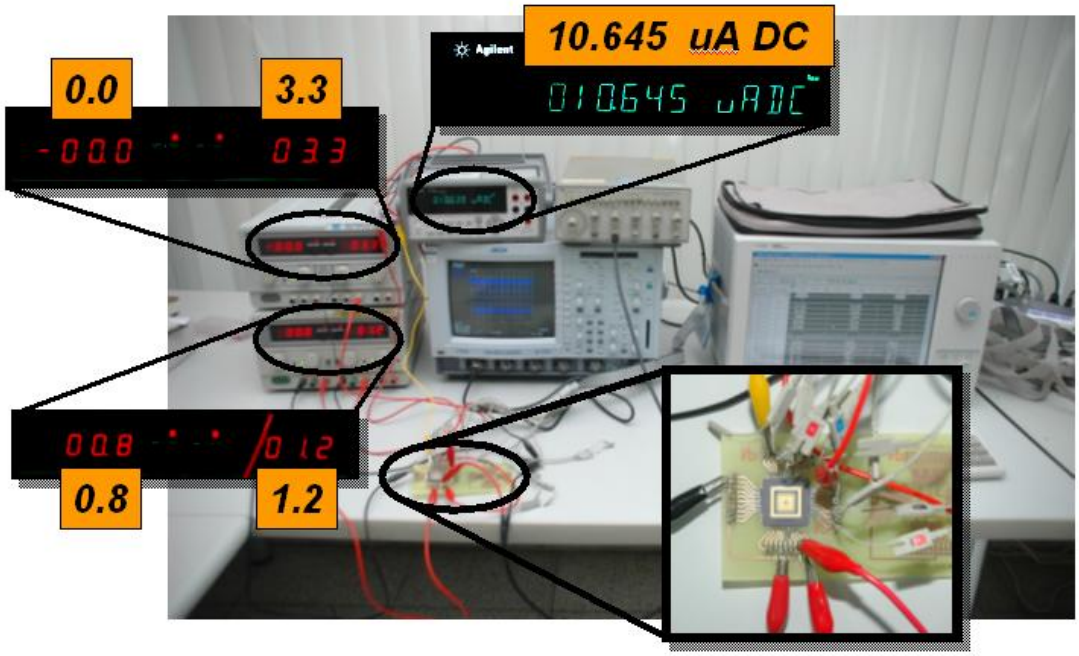


Fig. 6-37. Testing environment for the MT-CDMA modem test chips

6-3-3 Dual Mode WiBoC OFDM/MT-CDMA Baseband Processor

The second version of the WBAN baseband processor is named as wireless body on a chip (WiBoC). The proposed WiBoC platform contains a WSN and a CPN that are attached on human body skin and integrated in a portable device, respectively. The system block diagram and behavior time-line are illustrated in Fig. 6-38. A register-based FIFO is designed in the WSN that is used to accumulate body signals from an internally integrated temperature sensor or an external readout sensor. The memory size and clocking speed are optimized for and aimed at the ECG signal that are regarded as the most complex signals among body information sources. Compared to the baseband processing speed, the WSN takes much longer time accumulating body signals. This results in the WSN-CPN pair staying inactive for most of time and awake in burst for data transmission. The baseband processor provides both

MT-CDMA and OFDM modes for selection, and the transmission behavior is shown in Fig. 6-38(b) [3].

The clock sources in the WSN and CPN are implemented by a phase-frequency tunable clock generator (PFTCG). It is used to adjust the generated clock phase and frequency automatically for better system performance and reduced power consumption. An embedded temperature sensor is integrated together. Each block in both the WSN and CPN is designed for a specific power-voltage domain for low-power management.

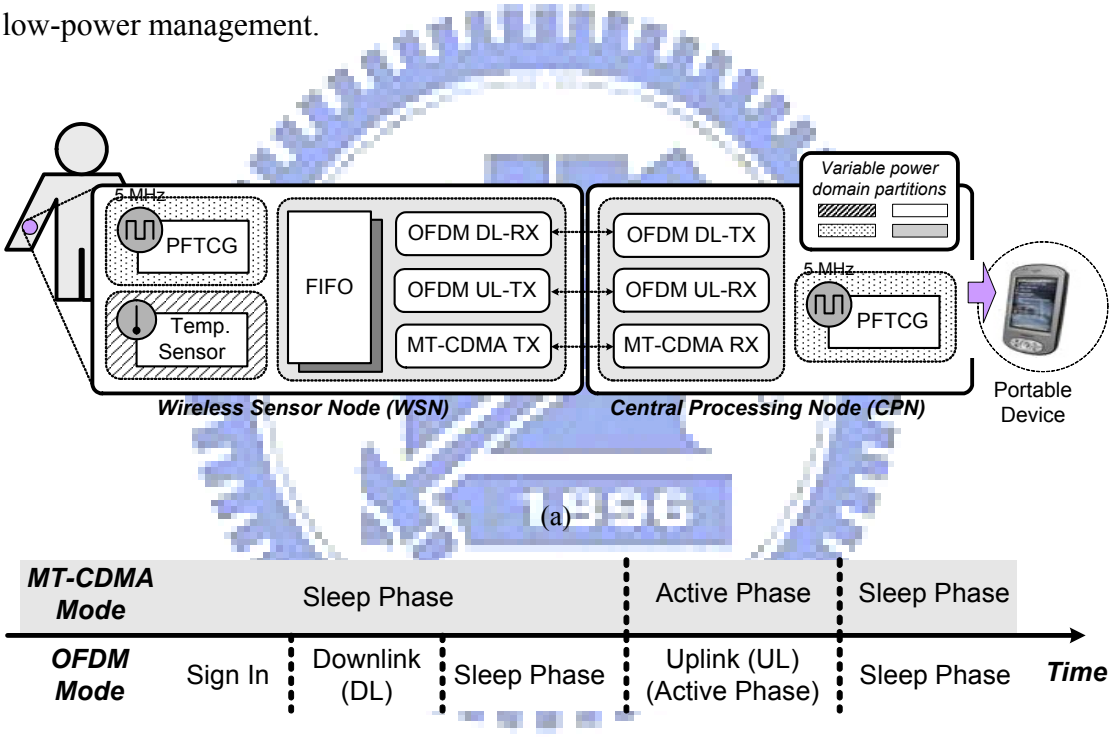


Fig. 6-38. The dual-mode baseband transceiver with (a) abstract view of functional blocks and (b) behavior time-line

This chipset is designed with power-domain partitions for voltage scaling, multi-supply voltage (MSV), and power gating to achieve extreme low power consumption as illustrated in Fig. 6-39.

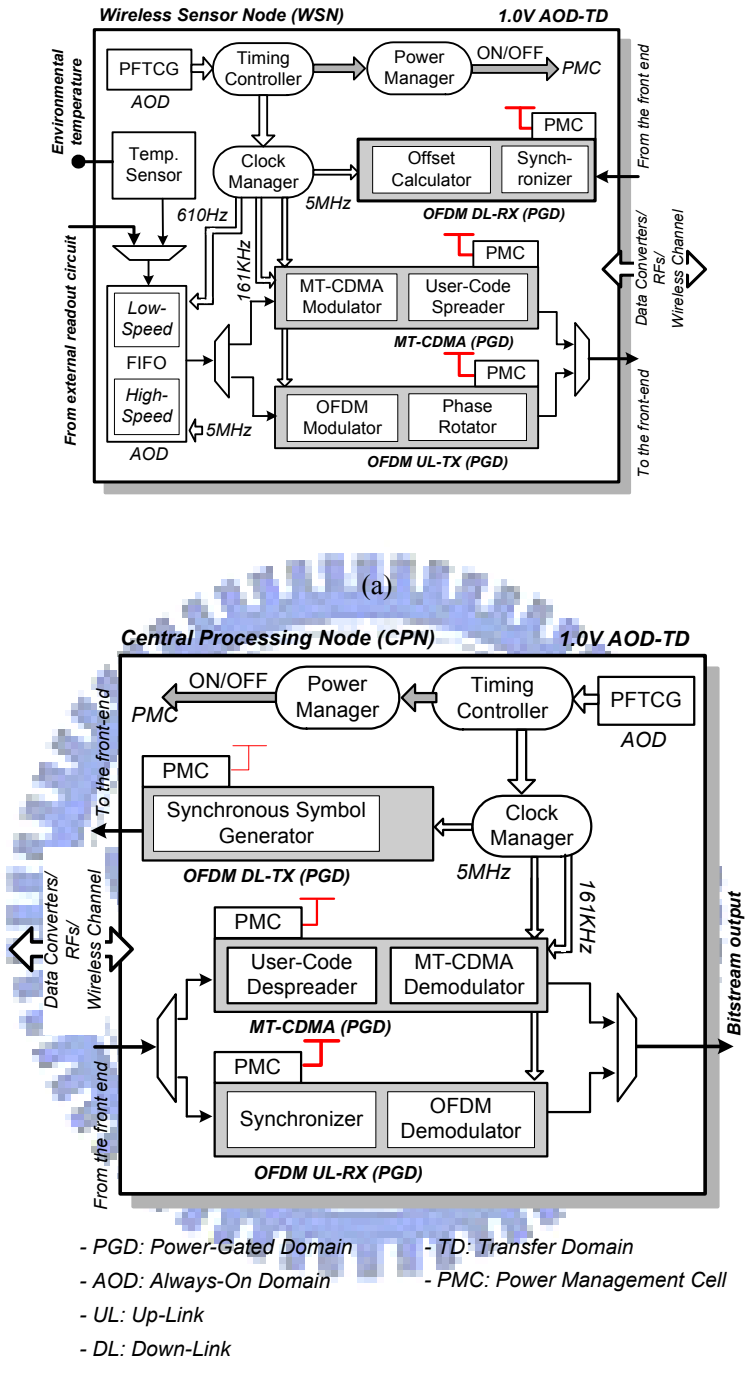


Fig. 6-39. The transceiver with power domain planning (a) wireless sensor node (WSN); (b) central processing node (CPN)

With the voltage scaling and multi-supply voltage techniques, the system is partitioned into 12 power domains with possible different voltage supplies. According

to the required operating speed and the achievable functionality, the supply voltage 0.5V is provided globally to every functional block, except special function blocks and transfer-domain (TD) that are operated at 1.0V to interface with I/O pads. Furthermore, every power domain is not necessary to be activated together. So, the other inactive domains can be switched into sleep phase for most leakage power saving. This active-sleep behavior is achieved by a power management cell (PMC) that contains a distributed coarse-grain power gating cell (DCG-PGC) [65] and an isolation cell shown in Fig. 6-40. The power manager sends commands to the PMC to turn ON/OFF the power-gated domain (PGD). The timing diagram is shown in Fig. 6-41. When an OFF signal is asserted, the isolation cell first de-activates by pulling high the signal in the AOD side. After that, the DCG-PGC shuts the virtual VDD off. Therefore, the unknown signal from the power-off domain will not affect the other domain. The PMC behavior is in the reverse way when a domain goes to active state. On the other hand, if a hardware block always stays active, its power will not be gated and is referred as always-on domain (AOD).

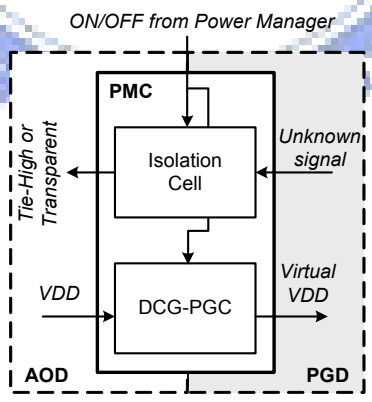


Fig. 6-40. The power management cell (PMC)

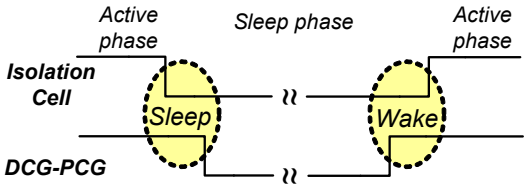


Fig. 6-41. The power management control sequence

In addition, the chipset has several clock domains to drive different sequential circuits. For the MT-CDMA block, a clock of 1/31 time of the original frequency is needed. Besides, a low frequency to drive the sensor is necessary. Therefore, an embedded clock generator provides the 5MHz clock source, and a clock manager unit is designed for frequency synthesis. The synthesized frequency outputs 5MHz, 161kHz, and 610Hz clocks to cover all possible requirements.

(a) Wireless Sensor Node

Fig. 6-39(a) shows details of the proposed WSN design as well as the power domain partition. The partition contains three PGDs, including 0.5V OFDM DL-RX, 0.5V MT-CDMA, and OFDM 0.5V UL-TX. The AODs include 1.0V PFTCG, 0.5V FIFO, and the other control circuits used for the 1.0V TD.

There are total three operation modes in the WSN, MT-CDMA TX, OFDM DL-RX, and OFDM UL-TX, to support the dual mode transmission and pre-calibration. First, in the MT-CDMA TX mode, FIFO stores the sensed signals whereas the MT-CDMA transmitter is idled in the sleep phase. When the stored data in low-speed FIFO is full, the MT-CDMA transmitter is waked to transmit those signals in the active phase. The 161KHz and 5MHz clocks are used for modulation and user code spreading respectively. Second, in the OFDM DL-RX mode, the

OFDM receiver is synchronized to the downlink training symbols and calculates the frequency offset for pre-calibration. The 5MHz clock is used for the OFDM receiver block as well as the OFDM transmitter block. Lastly, when WSN operates in the OFDM UL-TX mode, the OFDM transmitter can also be separated into two phases. The OFDM transmitter is in active phase when transmitting the data and in sleep phase when waiting for the sensed data storing. The frequency offset is pre-calibrated by the digital data distortion and tuning the frequency generated from PFTCG. In these modes, only the corresponding PGD is waked up, the other PGDs are turned off to save the leakage power.

A temperature sensor is also integrated in the WSN. The measured temperature or external sensor data is stored in the register-based FIFO. The FIFO is designed by a register approach instead of an SRAM basis because the supply voltage of a register can be reduced to 0.5V or less, which is difficult for a SRAM to achieve due to the use of an embedded sense amplifier. Furthermore, the biomedical signal is highly correlated in time domain so that a FIFO has benefits in the minimum switching power consumption, resulting in both reduced dynamic and leakage power for body-oriented signal storage. The total size of FIFO is 1024x8 bits that are further equally divided into two banks. One of the FIFO banks is driven by the 610Hz clock, which is synchronous to the sensor data. The other bank operates at 5MHz and delivers the data to the baseband modulator. The low speed bank collects data in longer period until it is full. As the content of the low speed bank is full, the bank dumps all its content to the high speed bank and can continue on collecting the data without any loss.

(b) Central Process Node

The CPN contains three PGD partitions, including 0.5V OFDM DL-TX, 0.5V MT-CDMA, and 0.5V OFDM UL-RX. Two AODs of 1.0V PFTCG and the other control circuits at 1.0V are applied, as shown in Fig. 6-39(b).

There are three operation modes, MT-CDMA RX, OFDM DL-TX, and OFDM UL-RX, in CPN. First, when CPN operates in the MT-CDMA RX mode, the received data from the front-end is directed to the MT-CDMA receiver block. The data is first de-spread by the 31-chip user code followed by the MT-CDMA demodulator. The synchronizer of MT-CDMA is able to calculate a better sampling phase for the PFTCG. Second, in OFDM DL-TX mode, the OFDM DL-TX broadcasts synchronous symbols and the content of the synchronous symbols is adjustable depending on the user selection. Last, in the OFDM UL-RX mode, the received data is switched to the OFDM uplink receiver where the synchronization block is first encountered followed by the OFDM demodulation block. When CPN is in one of the operation modes, the corresponding PGD is activated and the others are in sleep phase. The rest block of CPN is PFTCG, which generates a 5MHz clock with 8 different phases for synchronization. This clock signal is sent to the clock manager unit, where a 5MHz clock is bypassed to all the three blocks and a 161KHz clock is generated for the MT-CDMA demodulator.

(c) RSD Frequency Pre-Calibration

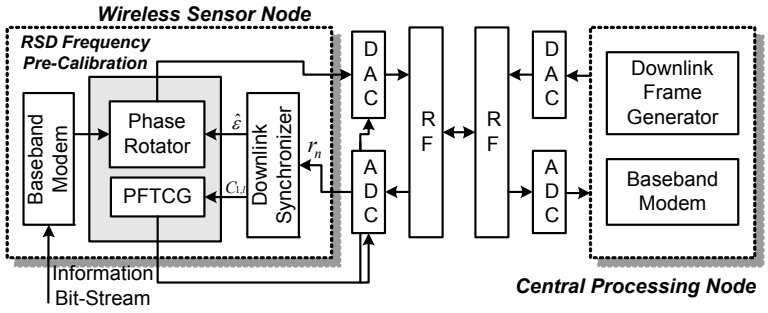


Fig. 6-42. The baseband transceiver with RSD frequency pre-calibration

The OFDM symbols are pre-calibrated with the estimated carrier frequency offset (CFO) and sampling clock offset (SCO) via the rotator-and-synthesizer driven (RSD) frequency pre-calibration, as shown in Fig. 6-42, where the frequency information is from the downlink synchronizer. The downlink synchronizer estimates CFO and SCO from the downlink frame. The phase rotator rotates the data by the estimated CFO value before the data are transmitted. A phase-frequency tunable clock generator (PFTCG) generates an accurate clock which is adjusted by the estimated SCO. The benefits of providing phase tuning capability are disclosed in [64] (for power reduction). This PFTCG is used to adjust the generated clock phase and frequency automatically for better system performance and reduced power consumption. Therefore, the baseband clock will be accurately tuned by the generator and the SCO effect will be reduced. In the down-link process, the CFO between the WSN and CPN is estimated by the expression

$$z = \sum_{n=0}^{N-1} r_{n+N} \cdot (r_n)^* = \sum_{n=0}^{N-1} r_n e^{j2\pi\varepsilon} \cdot (r_n)^* = e^{j2\pi\varepsilon} \sum_{n=0}^{N-1} |\, r_n \,|^2 \qquad (6\text{-}4)$$

where r_n is a periodic transmitted down-link frame [9], N is the length of the preamble, and z is the inner product of consecutive two preambles. The ε is the added CFO value, and the estimated CFO is computed via

$$\hat{\varepsilon} = (1/2\pi)\tan^{-1}(z) \tag{6-5}$$

The remaining received and ready-for-transmitted data will be compensated by this estimated value.

The SCO value is estimated by the pilot information in preambles. These preambles after channel equalization and CFO compensation are transformed to frequency domain to perform SCO estimation [3]. The behavior of the clock offset can be modeled as

$$\theta_{l,k} = C_{l,0} + C_{l,1}k \tag{6-6}$$

where k is the index of the subcarrier, and $\theta_{l,k}$ is the phase rotation of the data at k_{th} carrier in l_{th} preamble. The coefficient $C_{l,0}$ means the CFO value. The slope $C_{l,1}$ is used to estimate SCO.

The SCO effect on these pilots can be described as the following matrix form

$$KC_l = \theta_l \tag{6-7}$$

where $K = \begin{bmatrix} 1 & k_1 \\ 1 & k_2 \\ : & : \\ : & : \\ 1 & k_m \end{bmatrix}$, $C_l = \begin{bmatrix} C_{l,0} \\ C_{l,1} \end{bmatrix}$, and $\theta_l = \begin{bmatrix} \theta_{l,k_1} \\ \theta_{l,k_2} \\ : \\ : \\ \theta_{l,k_m} \end{bmatrix}$

We can obtain the $C_{l,1}$ in the preamble phase rotation by least square algorithm.

$$C_l = (K^T K)^{-1} K^T \theta_l \tag{6-8}$$

According to the estimated value in (6-8), the PFTCG is able to alter its generated frequency to reduce the sampling rate mismatch from the CPN side.

(d) PFTCG Architecture

The proposed architecture is shown in Fig. 6-43. The PFTCG is composed of two main parts: (i) 5MHz-frequency clock generation from the reference clock and (ii) multi-phase clock generation from the generated 5MHz clock source. The phase-frequency detector (PFD) and digital-controlled oscillator (DCO) are used for 5MHz clock generation. Furthermore, the DCO is also designed with 8 delay buffers, and each buffer provides $T_{FREF}/8$ delay time, resulting in 8 clock signals with equal-spaced $T_{FREF}/8$ between *Phase_N* and *Phase_(N-1)*. Then the selected clock from these 8 sources is picked up via the phase-selection. In order to dynamically generate the clock with variable frequencies and phases, the estimated frequency error FE and phase error PE are sent to the controller and phase-selection multiplexer, respectively. From this architecture, the correct frequency is generated by the closed loop of PFD, controller, and the phase_0 in the DCO. When this loop reaches steady state, the DCO is able to divide the total delay in 8 partitions with different clock phases.

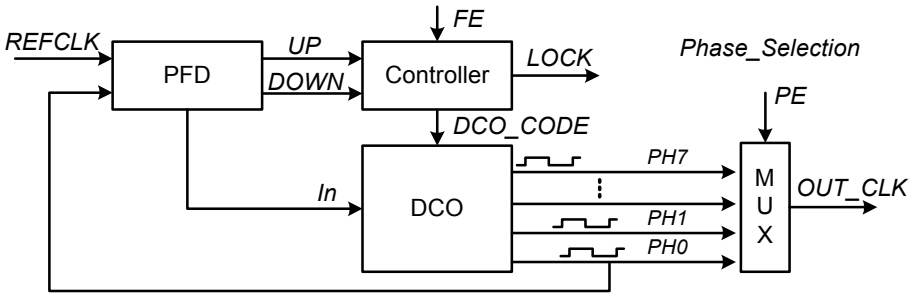


Fig. 6-43. The proposed PFTCG architecture

The control loop of this architecture is depicted in Fig. 6-44. In the beginning of clock generation and locking loop, the PFD generates an UP or DOWN command to modify the delay in the tracking loop. When a new DCO code is calculated, then the present DCO and PFD control signals are first cleared and then updated to the latest DCO code. The behavior of clear→update rather than directly update is to prevent the loop from frequency and phase divergence. When this loop achieves the lock state, the resulting clock frequency corresponds to the desired 5MHz clock, which is regarded as the coarse tuning loop. In order to match the signal sampling frequency from the transmitter (SCO may come from TX or RX itself), another fine-tuning loop is applied to approach the TX clock frequency according to the information $\hat{\xi}$. Then the SCO is minimized to the resolution provided by the delay hardware.

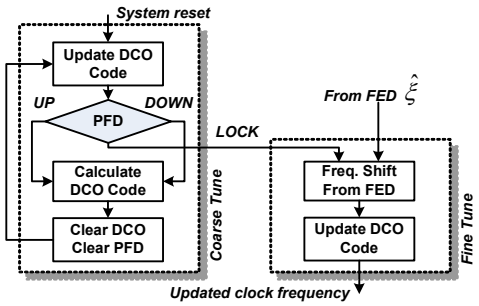


Fig. 6-44. The control loop of the PFTCG circuits

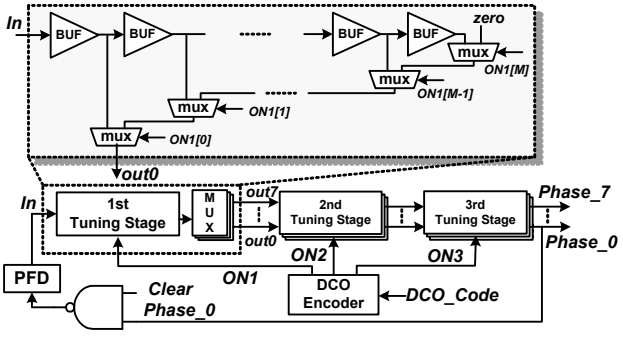


Fig. 6-45. The DCO block diagram

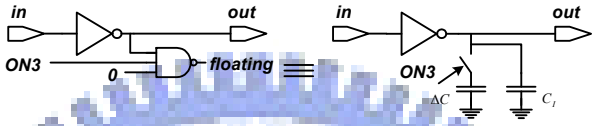


Fig. 6-46. The fine-tuning delay stage

The PFD design follows the circuit topology proposed in [63][64]. In the DCO design as shown in Fig. 6-45, it is composed of 3 tuning stage to meet the wide-range delay resolution from several tens of nanoseconds to the ten-pico-second scale. In order to provide 8 phases from the generated 5MHz clock source, the buffers in the 1st tuning stage divide the total delay into a multiple of 25ns in each delay segment. Moreover, the 2nd tuning stage provides the delays to compensate delay changes due to the process-voltage-temperate (PVT) variations. The circuit topology in the 2nd tuning stage follows the 1st one except the delay resolution.

In the 3rd tuning stage, it provides the highest delay resolution, i.e. least timing delay. This stage is used to slightly move the frequency of the generated clock to approach the TX's clock frequency. Furthermore in the 1st tuning stage, the clock signals between every buffer in the delay line are connected to 8 multiplexer groups, and each multiplexer group selects a clock signal with $T_{FREF}/8$ to each other and forms the vector out0~out7. Then every out_N signal is fine-tuned individually by the 2nd and

3rd stage. The SCO between TX and RX is assumed to be 150ppm @ 5MHz, so the frequency variation is 750Hz, corresponding to the tuning range of PFTCG ±30ps. To achieve this resolution, the loading variation of NAND logic-gate capacitance is applied as shown in Fig. 6-46 [68]. The 3-input NAND is selected with one input node tied to zero to cut off the path of NMOS and PMOS from ground and voltage supply, respectively. Then the on-off behavior from ON3 decides if an additional capacitance ΔC appeared in the output node of the delay cells, resulting in the change of charge and discharge in the desired delay resolution.

In the beginning of the RESET trigger, the PFTCG starts to converge to the generated clock to 5MHz until the LOCK signal appeared. During this time, it is found that the CLEAR_DCO signal is sent frequently to update the loop to a new delay path. After this, the circuit enters the steady state. When the PFTCG is required to change the frequency from the control signal $\hat{\xi}$ (corresponding to the signals TUNE_VALID and TUNE_CODE), the resulting clock then has an updated frequency. In the Fig. 6-47 shows 8 even-spaced clock waveforms in the steady state. Each pair of waveforms has about 25ns delay. When looking into the exact delay spacing, the percentage between each phase slot is 10%, 10%, 10%, 12%, 14%, 14%, 14%, and 15% of one period from Phase_0 to Phase_7.

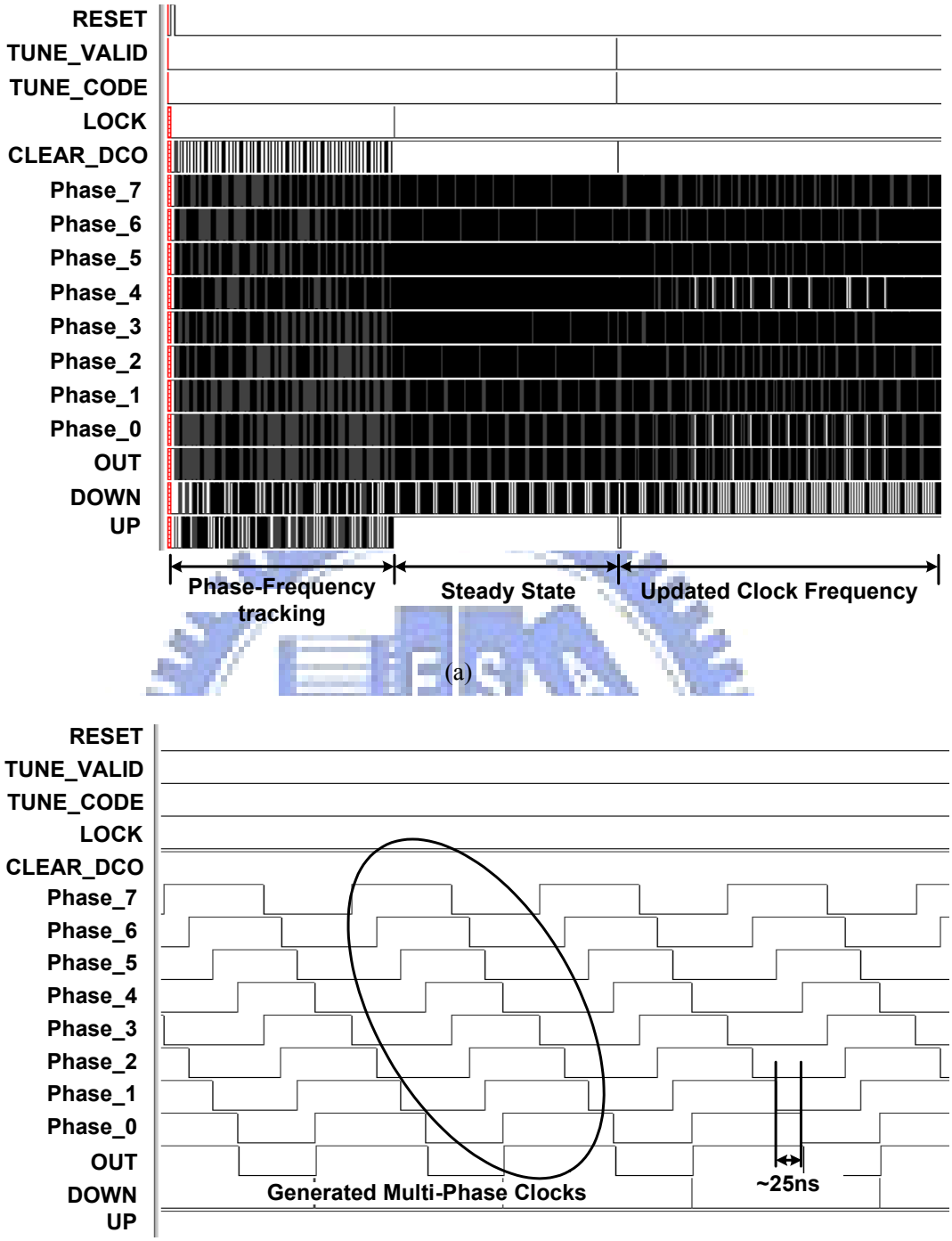


Fig. 6-47. The generated waveforms from the PFTCG (a) operation overview (b) multi-phase waveforms

This PFTCG is implemented in the standard process 90nm high threshold voltage (SPHVT) CMOS technology. The generated clock frequency and phase number are

5MHz and 8 phases, respectively. The lock-in time is designed within 128 cycles. The delay cell resolutions of 1^{st} ~ 3^{rd} tuning stage in the DCO circuit are 37.16ns, 1.16ns, and 18ps, respectively. With the scaled 0.8V and SPHVT CMOS, the power consumes 77.56μW with maximum RMS jitter 62ps. In the area of this PFTCG, the main part is the DCO circuits, largely from the delay cells to constitute the 25ns delay in each delay phase. In the rest of the area, it mainly comes from the control circuits because the long delay line has multiple of delay stage to control and it requires lots of circuits to decode the control signals. This PFTCG is integrated in a test system for system verification with the PFTCG area 125μm x 252μm.

The proposed WiBoC baseband transceiver chipset is fabricated in 90nm 1P9M CMOS standard process, where both devices of high- and regular-threshold voltages (SPHVT and SPRVT) are applied in this design. The measurement instruments include a constant-temperature oven, LeCroy LC584A, and a current-meter with resolution of 100pA.

The PFTCG is an always-on building block that continuously consumes both dynamic and static power. Therefore, it is implemented in the high threshold-voltage device for static current saving. The generated clock frequency and phase number are 5MHz and 8 phases, respectively. Four generated phases (PH0, PH2, PH4, PH6) are shown in Fig. 6-48. The measured RMS and peak-to-peak jitter is 145ps and 340ps, respectively. The power consumption is 145.8μW at 5MHz frequency and 1V power supply.

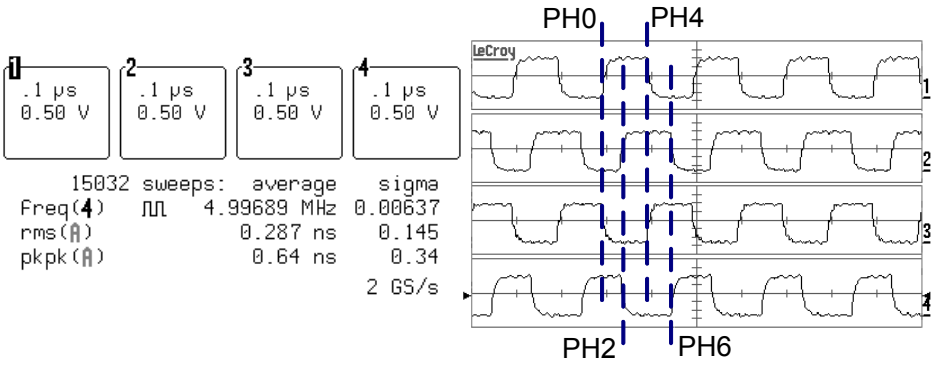


Fig. 6-48. Clock phases from the PFTCG circuits

TABLE 6-9. CHIP CORE POWER IN THE DUAL-MODE WSN AND CPN CHIPSET

WSN		CPN	
Total Modulator	5.52µW	DL-TX	3.94µW
		UL-RX	520µW
		MT-RX	490µW
FIFO+TS	289.5µW	N/A	N/A
PFTCG	145.8µW	PFTCG	145.8µW

The building blocks in this chip are tended to be designed with individual groups of power pads. This enables the power consumption in some of the blocks measured separately. Table 6-9 shows the measured core power consumption in the corresponding power domain.

The power-domain is turned on by the DCG-PGC. The OFDM DL-TX building block is used for the illustration of the current profile between active and sleep states. This current profile is generated by concatenating a resistor (51k ohm) in the way of core power path for clear instrument observation, and the voltage between this resistor's two sides is shown in Fig. 6-49. As the ENABLE signal is activated, the OFDM DL-TX domain is turned on, and more current is drawn (current = (measured voltage)/51kohm) that corresponds to µ-level power consumption.

This WiBoC improves the system data rate from 143kbps to 4.85Mbps. This largely reduces the system working duty cycle (the percentage of circuit-active time). The transmission power is reduced from previous proposal 21μW to this work 5.52μW, resulting in 73.7% efficiency improvement in baseband circuit processing. Fig. 6-50 shows the micro chip photos. Each bold-rectangular denotes a separate power domain with the rest region as the transfer domain for I/O-pad interfaces. Table 6-10 summarizes the features of this work.

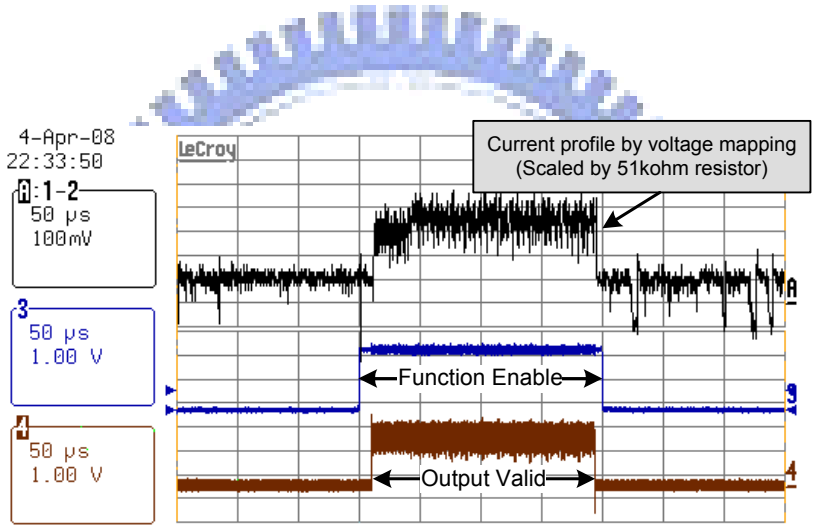


Fig. 6-49. Current profile between the sleep and active phases

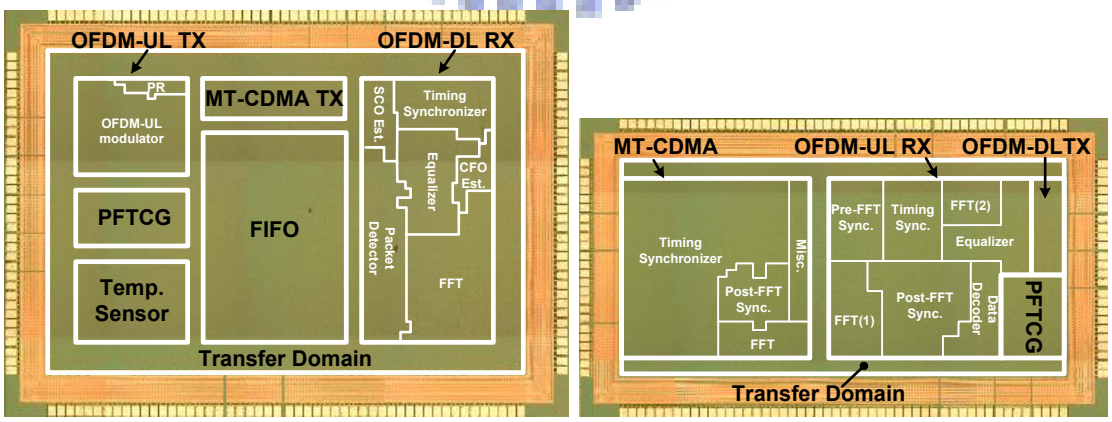
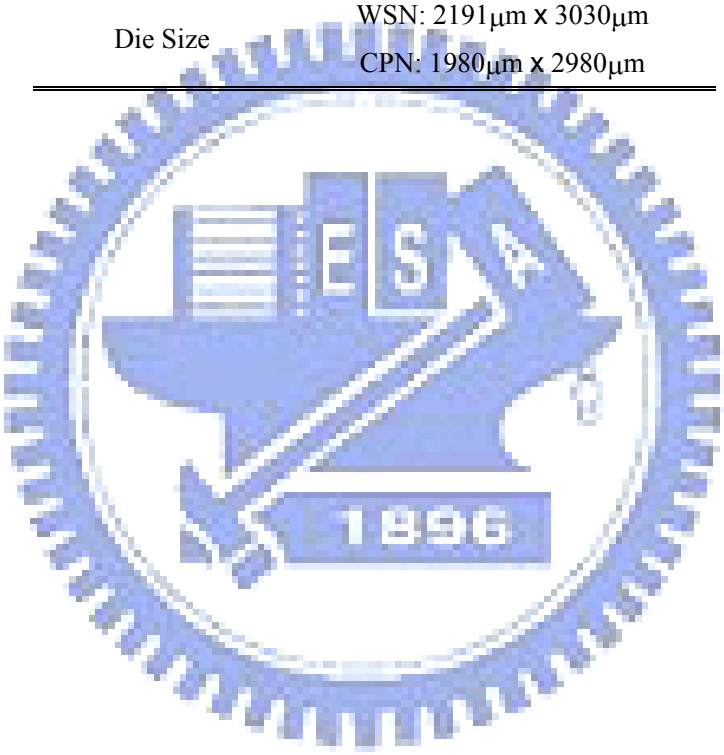


Fig. 6-50. Micro-photo of the dual mode test chip in 90nm standard CMOS technology

TABLE 6-10. THE DUAL-MODE TRANSCEIVER CHIP SUMMARY

Technology	Standard 90nm SPHVT/SPRVT CMOS
Max Data Rate	4.85Mbps (OFDM) 143kbps (MT-CDMA)
Temperature Sensor Accuracy	Error < 0.3°C (35~40°C)
PFTCG	8 Phases Generations RMS Jitter 145ps
Die Size	WSN: 2191μm x 3030μm CPN: 1980μm x 2980μm



Chapter 7:

Conclusion and Future Work

7-1 Conclusion

The design challenges in more Moore and more than Moore are explored in this work, proximity data communications. Here, Table 7-1 summarizes the contributions in this work.

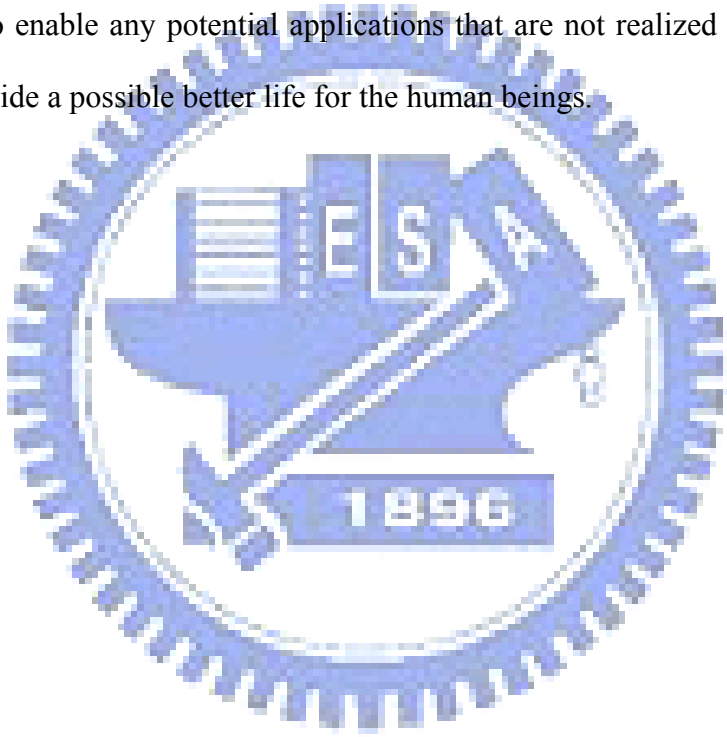
TABLE 7-1. THE SUMMARY OF THIS WORK

ADIQMC	Narrow band error function Wideband dual properties Wideband error function
DSTC	Symbol-rate synchronization Optimum sampling-instance search Collaboration with PTCG
HDC Clock Generator	Delay cells use with HDC Power-of-two delay line architecture HDC topology designs
Baseband Core Design	Low-power design flow

In the near future, the applications will approach both of the more Moore and more than Moore trends at the same time. Consequently, this work provides several schemes with reduced power and improved performance that may cover several items in the spectrum of more transistors or more heterogeneous integrations. With this work, a possible beyond-Moore scenario may be achieved with the foundation of the power and performance efforts in this work.

7-2 Future Work

The external components, for example a crystal, disable a highly integration of a single chip design. However, an elimination of crystal results in difficulty in accurate synchronization in the communications operations. Accordingly, a proposal with the embedded silicon crystal generator (ESCG) is on-going developed for the elimination of an external crystal to achieve the goal of the single chip. With this scheme, both ends of more transistors and more heterogeneous integrations become solid complete. This will also enable any potential applications that are not realized nowadays. This will also provide a possible better life for the human beings.



Appendix I:

Voltage-Power Domain Designs

In the beginning of chip designs, the power domain and voltage domain are defined first. Fig. A1-1 illustrates the WiBoC CPN design and the module groupings. Different colors indicate different domains in terms of voltage level or power behavior.

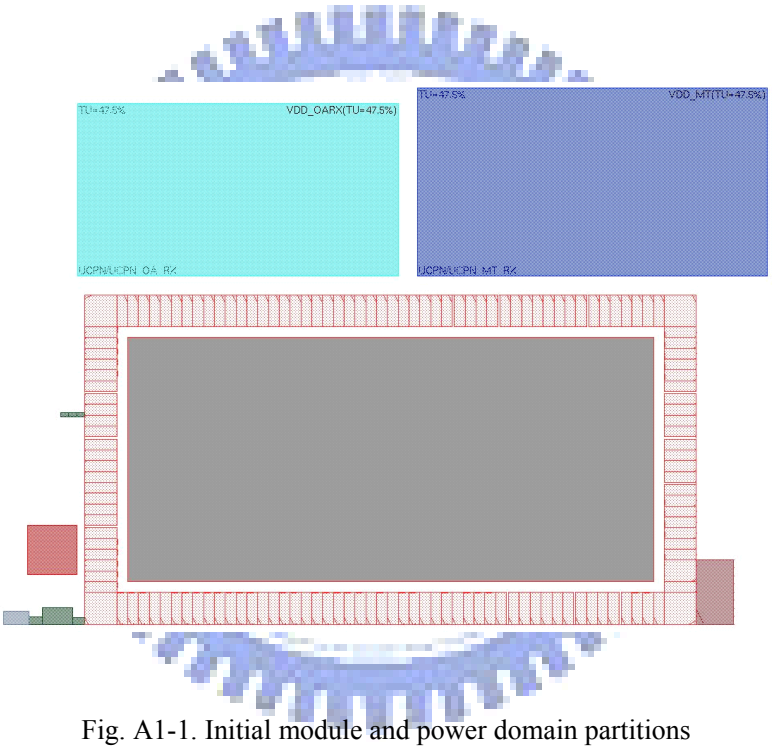


Fig. A1-1. Initial module and power domain partitions

Each domain is then placed in the designed partitions as shown in Fig. A1-2. Note that a transfer domain exists in the rest of power-domain partitions to interface with the I/O pad for a proper level transformation. Moreover, the I/O data pad and also the I/O power pad are grouped so that each power domain can be powered on individually for convenient measurement and behavior monitoring. The power gating cells are located in certain domains to enable the power-switch capability. The gating cells are

placed as stripes to be attached with the stripe power lines. These positions match the power designs as a bridge between power VDD and virtual VDD.

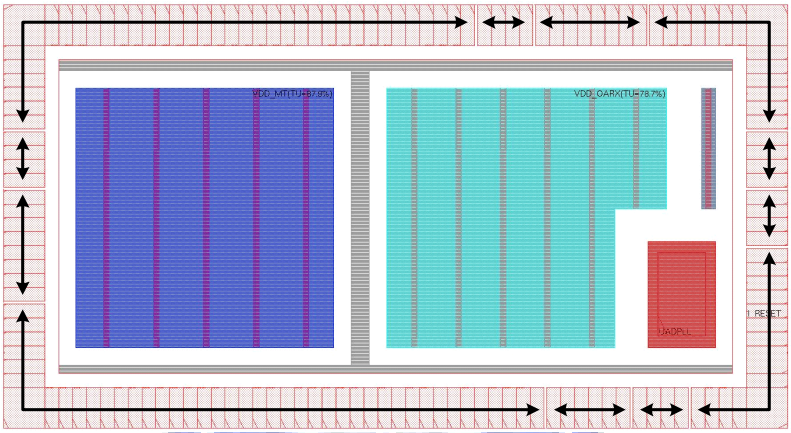


Fig. A1-2. The floor planning in the scope of voltage and power domain partitions

Fig. A1-3 illustrates the result after power planning. The power pads attach to the corresponding power rings around their power domains. The power stripes cross each power domain follow the locations of power gating cells. In this step, the power gating cell successfully connects the power VDD and the virtual VDD nodes.

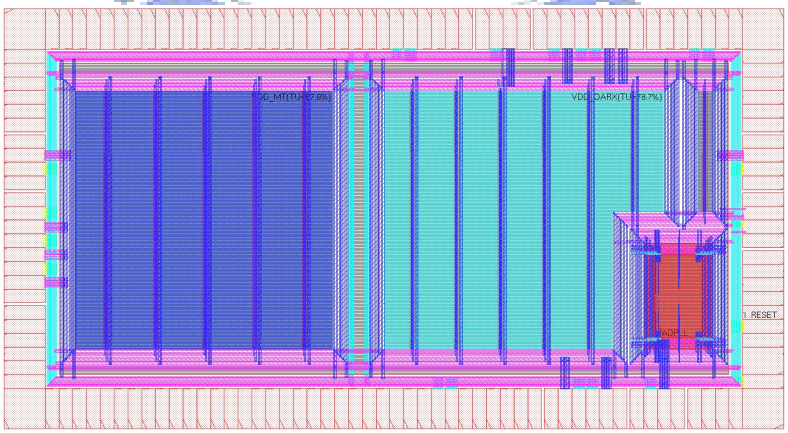


Fig. A1-3. The results of power planning

After the completeness of power planning, the standard cells are placed to the corresponding modules, in addition to the level shifter cells, as shown in Fig. A1-4. Those level shifters are placed around the module boundary to interface with the transfer domain that may pass the signals to the I/O pads or the other power domains with different voltage levels or power behaviors.

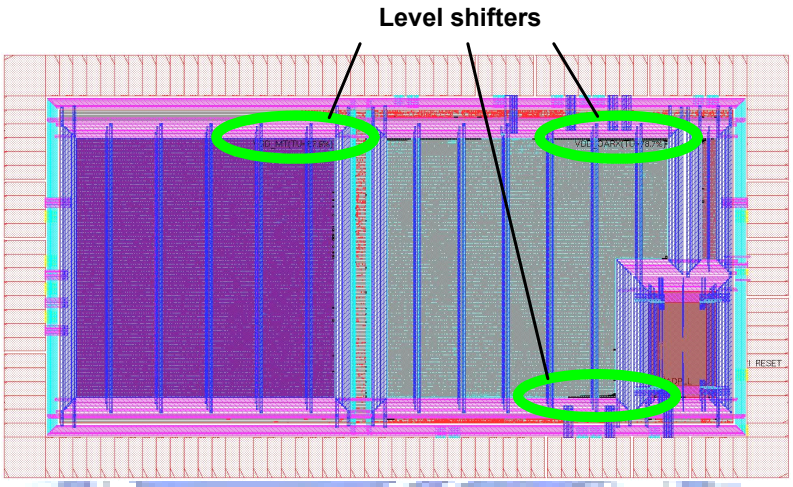


Fig. A1-4. Standard cell placement in addition to the level shifter insertions

The next step after the level shifter insertions is the isolation cell placements as illustrated in Fig. A1-5. The isolation cells are normally placed in the transfer domain that is the always-on domain. So, this domain provides the no-sleep power line to the isolation cells to guarantee the output signals providing a specific tie-high or tie-low voltage level.

The rest of the APR design follows depends on the design specifications in terms of timing, signal integrity, logic behaviors, etc. The final scope of the chip with the bonding pad is shown in Fig. A1-6.

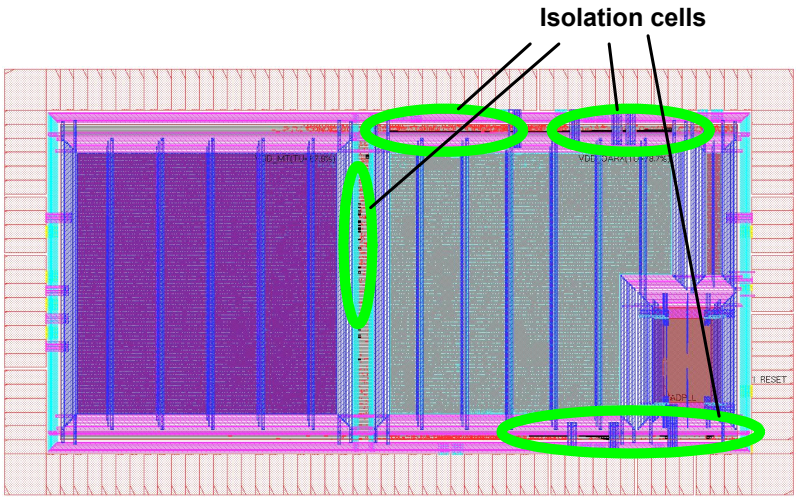


Fig. A1-5. Standard cell placement in addition to the isolation cell insertions

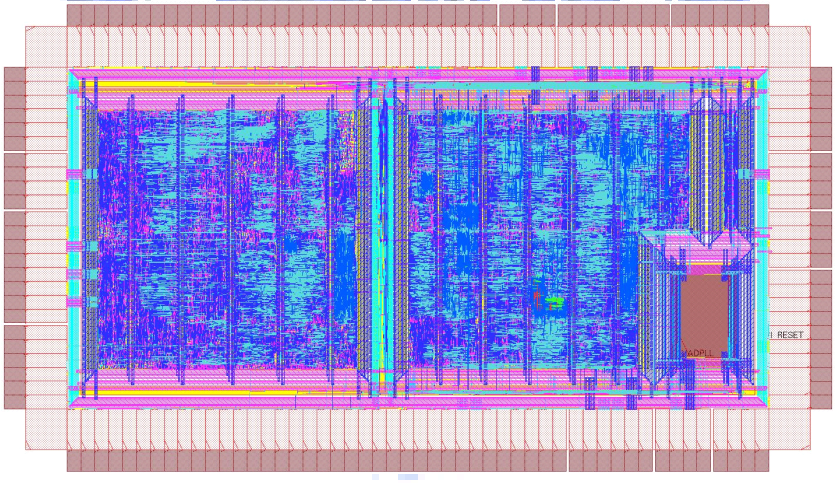


Fig. A1-6. Final chip view with bonding pads attached

Appendix II:

Power Gating Cell Exploration

A2-1 Introduction

Leakage power plays a crucial role in the deep sub-micron CMOS technology. The operation current leaks in both active and sleep phases. To reduce this amount, a multi-threshold CMOS (MTCMOS) technique [77] has been reported to apply transistors with different threshold voltage (V_{TH}) in different timing paths. Circuits with lower V_{TH} implies higher computing speed and also higher leakage power consumption. This approach effectively reduces the static current whenever the circuits are in full-speed operations or stay in an idle state. However, the unsolved static current of the idle circuits may cause dramatic power waste, shrinking the lifetime of batteries in portable devices. As a result, power gating approaches are further applied to cut off any possible paths from power sources to leakage victim devices.

Existing power gating techniques cover two mainstreams, fine grain and coarse grain schemes. In the fine-grain power-gating approach [78], power gating cells (PGC), either a header (between the VDD and a logic core) or a footer (between a logic core and the VSS) or both of them, are inserted into each standard cell, isolating the static current path from VDD to VSS. In other words, every standard cell has an additional port for the PGC control. This methodology has the advantage of unchanged automatic EDA design flows whereas it requires the redesigned standard-cell libraries. Moreover, this extra control-pin occupies routing space,

largely increasing the routing complexity. On the other hand in the coarse-grain design scheme, PGCs are placed outside standard cells, and each PGC supplies the operation current to cells depending on the driving ability itself. This has been shown to achieve about an order leakage saving more than that of fine-grain schemes. At the same time, the area and power overheads are tremendously reduced. The difficulties of the coarse-grain design approach are the increased complexity in the design methodology and circuit verification, and the most critical problem is to guarantee the unchanged functionality after PGC insertion. Previous work, the super cut-off CMOS (SCCMOS) [79], was proposed to perform picoampere current per logic gate in the stand-by mode with PMOS header (PMOSH) as power switches. It applies p-type header CMOS (PHCMOS) with overdriven gate voltage to be the power switches. To improve circuit wake-up time by the use of non-overdriven single VDD, the zigzag super cut-off CMOS (ZSCCMOS) [80] was proposed with a particular phase-forced flip-flop pair as the pipeline stage. This has difficulties in connecting those pipeline stages with the automatic place-and-route (APR) implementation flow [69].To ease the design efforts by the APR flow, the single-low-VDD CMOS (SLVCMOS) [78] technique was developed with PMOSH-PGC concentrated and combined outside a core design. To achieve the purpose of single power supply in the ZSCCMOS and SLVCMOS designs, several voltage-boosting techniques like bootstrap and charge pump with the aid of level detectors are applied.

For the benefits of reduced leakage current, larger current driving force, faster circuit wake-up time, smaller area-power overhead, smaller IR-drop variation, and higher power integrity in a core design, a charge-pumped NMOS header (CP-NMOSH) is analyzed and verified in this paper. To distinguish the PGC fundamental characteristics between a NMOS and a PMOS, section II presents a

numerical analysis of current and voltage-drop behaviors. In section III, the proposed CP-NMOSH is designed and discussed for leakage reduction, and also the logic-core performance indices mounted under PGCs in the operation mode is described. Finally, this work is concluded in section IV.

A2-2 Power Gating Cell Fundamental Exploration

A2-2-1 Header vs. Footer

The use of a power switch by a header or a footer with a NMOS or a PMOS depends on the overall chip floorplanning and performance considerations. Existing literature has reported that a footer power switch is less effective than a header one for leakage reduction because static current may leak out from VDD to CMOS substrate even if the ground path is cut off. As a result, we focus on the header power gating scheme in this paper, and discuss the difference between NMOS- and PMOS-header designs.

Before a deeper analysis, we compare the operation behavior between PMOSH, which is applied in both SCCMOS and SLVCMOS, and the desired NMOSH. In Fig.A2-2, it is found that the PMOS is turned on and off with the gate voltage switched to VSS and VDD+V_{OV}, respectively, with the overdriven voltage V_{OV} for further leakage reduction in the sleep mode. Based on these two voltage levels, VDD and VDD+V_{OV}, we are going to illustrate the NMOSH and PMOSH performance indices, and show that the selection of NMOSH scheme performs better than the PMOSH as used in the SCCMOS and SLVCMOS schemes.

A2-2-2 NMOS-Header vs. PMOS-Header

The PGC behavior is modeled as a resistor when it is turned on, acting as a gate between a VDD power rail and a virtual VDD (VDDV) power line. The VDDV value is required as approach the VDD voltage as possible because a higher voltage drop implies a larger power overhead dissipated in the PGC and smaller current driving force, and also unexpected timing in a logic function. This is going to be illustrated in terms of the transconductance in an active MOSFET. According to the square-law model, the current of a NMOS in the triode region is approximately proportional to

$$I_N \propto \mu_N C_{OX} \frac{W}{L}[(V_{GS} - V_{TN})V_{DS} - \frac{1}{2}V_{DS}^2] \quad \text{(A2-1)}$$

where μ_N is the electron mobility, C_{OX} is the oxide capacitance, W and L are the width and length of a MOSFET, respectively. V_{TN} is the NMOS threshold voltage. V_{GS} and V_{DS} represent the voltage differences of gate-source and drain-source, respectively. Fig. A2-2 shows the configuration of header-style PGCs. In a power-gating design, the correlation of voltage drop (VDD-VDDV) and driving current (I_N) is concerned. We may further rewrite (A2-1) as

$$I_N \propto \mu_N C_{OX} \frac{W}{L}[(V_{OV} + \Delta V - V_{TN})\Delta V - \frac{1}{2}\Delta V^2] \quad \text{(A2-2)}$$

where $\Delta V = V_{DS}$, V_{OV} is the overdriven voltage relative to the VDD level, and $V_{GS} = V_{OV} + \Delta V$. Therefore, the transconductance of this NMOS PCG can be derived by the derivative of (A2-2) with respect to ΔV.

$$g_{m,N} = \frac{\partial I_N}{\partial \Delta V} \propto \mu_N C_{OX} \frac{W}{L}(V_{OV} + \Delta V - V_{TN}) \quad \text{(A2-3)}$$

To compare with the PMOS PCG, the transistor's current is derived in a similar way except covering both the saturation and triode region.

$$I_P \propto \begin{cases} \mu_P C_{OX} \dfrac{W}{L}[(V_{SG}-|V_{TP}|)V_{SD}-\dfrac{1}{2}V_{SD}^2] \\ \qquad\qquad (triode \quad region) \\ \mu_P C_{OX} \dfrac{W}{L}(V_{SG}-|V_{TP}|)^2 \quad (saturation \quad region) \end{cases} \tag{A2-4}$$

where μ_P is the hole mobility. We may further rewrite (A2-4) with V_{SG} and V_{SD} replaced by VDD and ΔV, respectively.

$$I_P \propto \begin{cases} \mu_P C_{OX} \dfrac{W}{L}[(VDD-|V_{TP}|)\Delta V-\dfrac{1}{2}\Delta V^2] \\ \qquad\qquad (triode \quad region) \\ \mu_P C_{OX} \dfrac{W}{L}(VDD-|V_{TP}|)^2 \quad (saturation \quad region) \end{cases} \tag{A2-5}$$

In the PMOSH scheme, the change of VG below VSS level has only slight increase of the I_P current. Moreover as discussed in *Part A*, PMOSH has applied the second overdriven voltage for an improved leakage power saving. Therefore, we ignore the possible third voltage for driving PMOS gate below the VSS level for a fair comparison between NMOS and PMOS schemes. So, the transconductance of a PMOS transistor is

$$g_{m,P} = \frac{\partial I_P}{\partial \Delta V} \propto \begin{cases} \mu_P C_{OX} \dfrac{W}{L}(VDD-|V_{TP}|-\Delta V) \\ \qquad\qquad (triode \quad region) \\ 0 \qquad\qquad (saturation \quad region) \end{cases} \tag{A2-6}$$

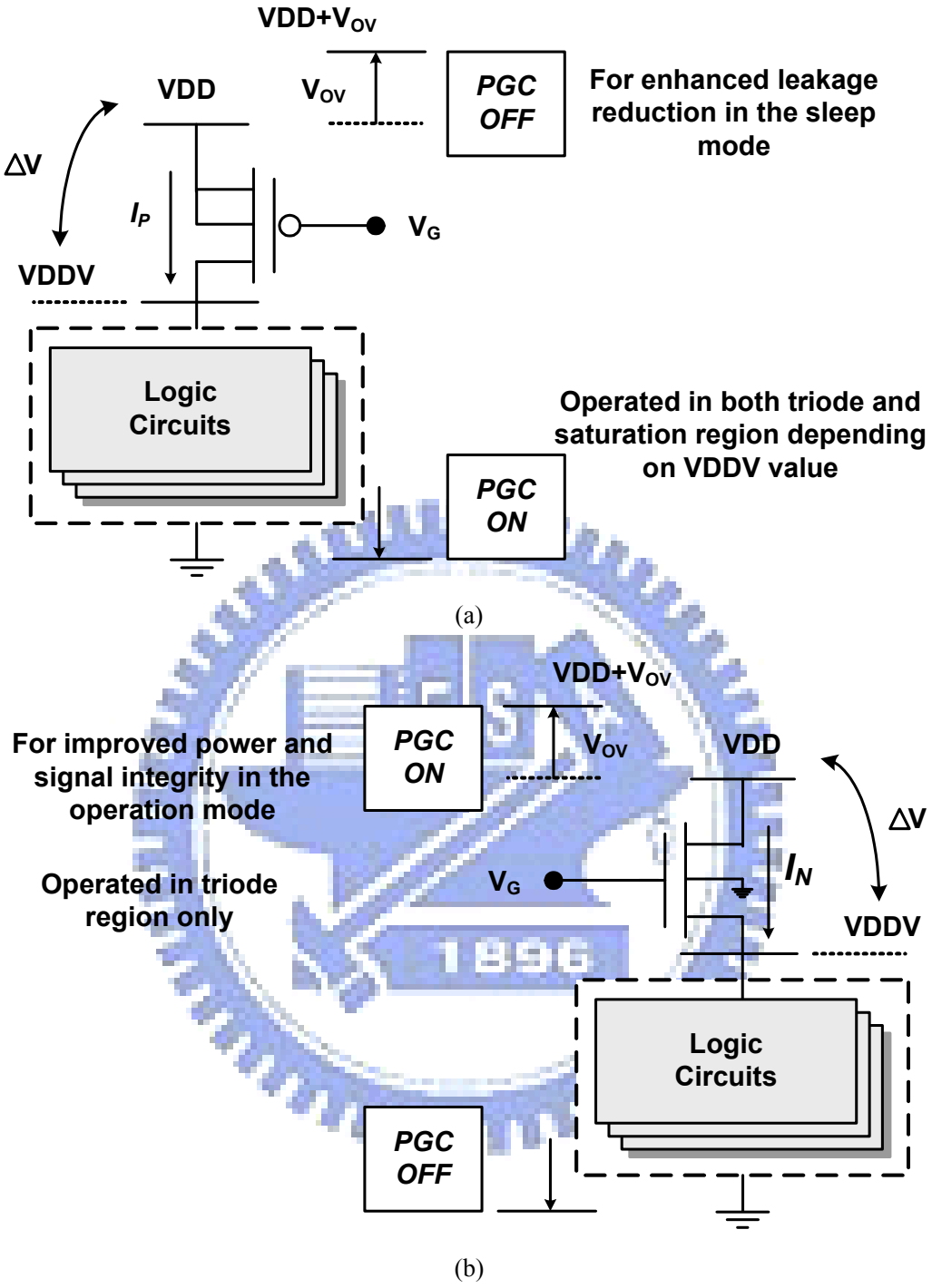
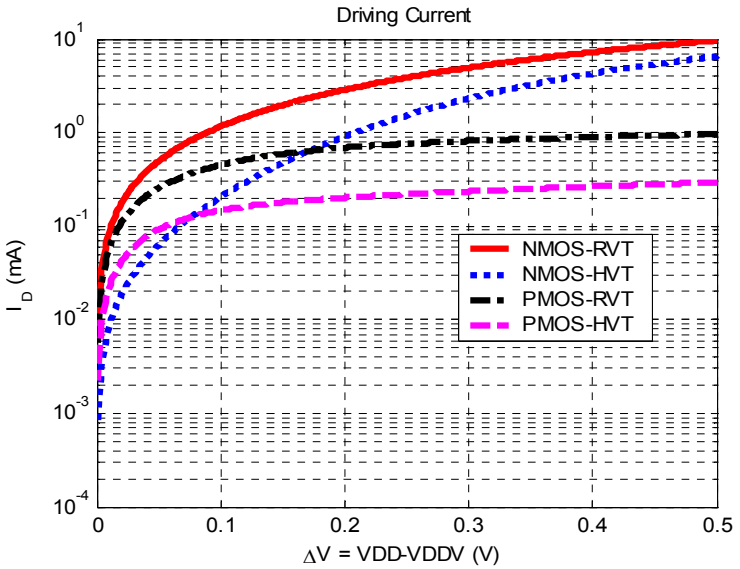


Fig. A2-2. Power gating cell operation mechanism (a) PMOSH (b) NMOSH

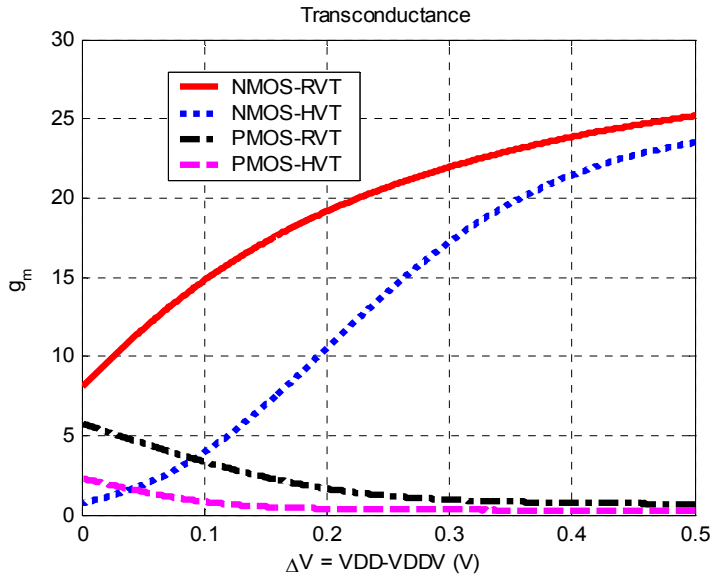
In comparison of I_N and I_P, there are two main differences and thus impacts to the mounted logic cells. First, I_N is able to provide a larger driving current with a proper selection of the overdriven V_{OV} value whereas I_P current behavior is fixed when the VDD value is determined. Second, when logic cells are activated from the

stand-by mode, i.e. $\Delta V = VDD$ to $\Delta V = 0$, the restored current of I_P covers both the saturation and triode region whereas I_N is only in the triode region. This implies that the saturated I_P does not provide a larger current value when the voltage gap between VDD and VDDV becomes larger, whereas I_N from a NMOS does. Furthermore, the mobility value of μ_N is more than twice of μ_P, and this again guarantees that NMOS PGC is capable of providing larger driving current. To illustrate the driving current of NMOSH and PMOSH PGCs, the circuits are based on 90nm CMOS technology, and VDD and V_{OV} are designed in 0.5V and 0.4V [78], respectively. The NMOSH and PMOSH are sized in the same length and width, say 80nm and 0.6um for evaluations. As a result, Fig.A2-3 shows the current and transconductance curves. In the current plot, the curves reflect the provided current pulling the VDDV from the stand-by level to VDD with different MOS threshold voltage, regular-V_T (RVT) and high-V_T (HVT). In the RVT-NMOS and PMOS curves, it is found that the driving current of RVT-NMOS is about an order higher than that of RVT-PMOS when $\Delta V = 0.5V$. This means RVT-NMOS provides 10x current at circuit's wakeup instance. When the voltage drop ΔV approaches zero, the value becomes 1.3x difference, and the RVT-NMOS current still remains higher than RVT-PMOS. Basically, the region around $\Delta V = 0$ implies the loaded circuits are active, so the current reflects the ability that the PGC can afford when a sudden large current is required without a voltage drop. On the other hand in the region around $\Delta V = 0.5V$, it reflects that the circuits are in the sleep status, and the driving current corresponds to the provided value for circuit wakeup. As a result, it is shown that the I_D value of the RVT-NMOS over $\Delta V = 0 \sim 0.5V$ is larger than that of RVT-PMOS. This means a RVT-NMOS PGC provides better driving ability than a PMOS PGC either in active or sleep state. In the HVT-NMOS and PMOS, both of them has poorer driving force in terms of provided current than the RVT-NMOS and PMOS. If we look at the transconductance as shown

in Fig. A2-3(b), it is also found that the RVT-NMOS possesses a higher g_m value over the whole ΔV range. From the I_D and g_m plots, we are able to confirm the use of RVT-NMOS as a power gating cell. In the following discussion and comparison, we denote the RVT-NMOS and RVT-PMOS as NMOS and PMOS for simplicity.



(a)



(b)

Fig. A2-3. NMOS:VD(0.5V)+VG(0.9V) and PMOS:VS(0.5V)+VG(0V) (a) driving current (b) transconductance

A2-3 Power Gating Cell Fundamental Exploration

Previous discussion confirms the utilization of NMOSH and PMOSH with overdriven V_{OV} for further leakage reduction and enhanced current driving ability, respectively. The purpose of adding power gating cells is to reduce the leakage current when circuits are not in operations whereas maintaining the signal and power integrity when circuits are in normal working conditions. Therefore in the following, these two design schemes, NMOSH and PMOSH, are explored in terms of leakage level and current driving abilities, respectively.

A2-3-1 Leakage Characteristics

The characteristics of leakage current in a NMOSH and a PMOSH are first simulated and summarized in the Table A2-1 and Table A2-2. The environmental conditions are defined in two process-voltage-temperature (PVT) extreme corners, say fast-0.55V-125^{0}C (best) and slow-0.45V-0^{0}C (worst) cases. The gate and body voltages are applied with reversely 0~0.9V to look for the minimum leakage values for both design schemes in each corner condition. For a NMOSH, VB and VG are swept from 0~ -0.9V, and for a PMOSH, VB and VG are swept from 0.5~ (0.5+0.9)V. Each variable is simulated with voltage step 0.05V. In the worst case, the NMOS sinks minimum 7.65pA at VG=-0.05V and VB=-0.65V, and the PMOS sinks minimum 6.75pA at VG=0.65V and VB=0.1V. With these biased voltages for minimum current, however, the operation PVT conditions may change due to unexpected manufacturing variation and environmental conditions. Then the leakage current under these pre-fixed VG and VB becomes 14.46nA and 90.47nA for a NMOSH and a PMOSH, respectively, when PVT moves to the opposite extreme case, say best case. Although the minimum leakage of a NMOSH in a certain case

consumes a little higher current than PMOSH, it becomes lower when PVT changes for both directions of extreme cases (best -> worst or worst -> best). The possible leakage variation range for a NMOSH is 7.65pA~14.46nA, which is much lower than that for a PMOSH, say 6.75pA~90.47nA. On the other hand, the SLVCMOS (PMOSH) approach provides an overdriven gate voltage VG=0.9V, so it is more likely for the gate and body voltages close to VG=0.65V and VB=0.1V in a huge system-on-a-chip silicon, resulting in possible maximum leakage increase.

For least leakage variation, we confirm the utilization of a NMOSH as a power gating cell for power saving. To generate the reversely-biased VG and VB voltages, a charge-pumped NMOSH (CP-NMOSH) scheme is proposed as depicted in Fig. A2-4 with the control sequences as shown in Fig. A2-5. In the active phase (T1), the logic circuits are in operations with currents provided by the power gating cell (M0). M4 passes an overdriven 0.9V to the VG_{M0}. M1 and M3 charge the capacitor (C0), so the voltage difference of C0 is 0.9V-$V_{TH,M3}$. The NMOS M5 disconnects the M0's gate and body, so the VB_{M0} is increased to $V_{TH,M3}$. In other words, the current driving ability of a NHCMOS is further improved.

When the logic circuits turn into sleep phase (T2), M4 first cuts off the path between power supply and VG_{M0}. Then M5 is first turned on to share the charge between VB_{M0} and VG_{M0}, whereas keeping M1 turned on to provide the necessary charge for VB_{M0} and VG_{M0} balances. After M1 is turned off, M2 is turned on in a burst to shift C0's reference voltage from 0.9V to $V_{TH,\,M2}$. As a result, both VG_{M0} and VB_{M0} are reversely biased. From sleep phase to active phase, M5 should disconnect VG_{M0} and VB_{M0} first, then the rest necessary transistors could be turned on again in an arbitrary ordering. Note that the transistors required in the charge-pumped circuit

are designed in high-V_{TH} PMOS (M1~M4) due to two reasons. First, there are no further biased voltages provided for these transistors except a 0.9V overdriven voltage. So only a PMOS with VG=0.9V provides good enough leakage isolation. Second, these transistors provide only biased voltage to M0 rather than a current driving ability, so a high-V_{TH} transistor could perform less leakage current. The only NMOS (M5) used is to provide good connection between VG_{M0} and VB_{M0}. Those transistors, M1~M5, are implemented in minimum sizes. The capacitor applied here is designed from MOS transistors, providing a several tens fF-scale capacitance. With proper selections of RVT/HVT NMOS and PMOS transistors, the power gating cell performs both good driving ability and little leakage consumption.

To evaluate the leakage reduction performance, an inverter chain composed of 1677 minimum-sized inverters is applied as shown in Fig. A2-6. Under 0.5V supply voltage, this inverter chain constitutes a delay about 200ns. To maintain the same delay, the PGCs with equivalent W/L=12um/80nm are used. During the sleep mode, the leakage current is summarized in Table A2-3 with different PGC schemes (SCCMOS: VG=0.5V; SLVCMOS: VG=0.9V; NMOSH: VG=0V; CP-NMOSH: VG & VB are charge-pumped biased). It is found that the leakage level for SLVCMOS varies in a wide range. With the proposed charge-pumped gate-body biasing, the CP-NMOSH sustains a small enough leakage level and keeps the total leakage in the nano-scale rather than diverges to micro-scale, which is comparable to the whole chip leakage current without PGC schemes.

A2-3-2 Performance Evaluations

To see the performance indices for NMOSH and SLVCMOS, the same testing circuit in Fig. A2-6 is used. To evaluate the PGC with the circuit loads, the plot of

delay penalty vs. power switch width is shown in Fig. A2-7. For the test of the delay penalty, we apply a rectangular pulse as an input of the inverter chain, and it is found that the NMOSH has a delay penalty of 7% less than the SLVCMOS approach in the same switch width. Similarly, the PGC with equivalent W/L= 12um/80nm is used for the following evaluations, which maintains the 200ns delay of this inverter chain. The restored time is shown in Fig. A2-8. Following the definition for system restored time [6], it includes (1) the VDDV level from 50mV to 450mV (10% and 90% of VDD) and (2) the setup time of the circuit load from VDDV=450mV to V_{OUT} = 50mV or 450mV (±10% of VDD or VSS level), where V_{OUT} is the circuit load's output voltage.

In Fig. A2-8(a), the VDDV restored time with NMOSH and SLVCMOS are 15ns and 68ns, respectively. Fig. A2-8(b) shows the circuit load's setup time of 6ns and 9ns with NMOSH and SLVCMOS, respectively. Therefore, the restored time reaches 268.8% reduction including both VDDV and circuit's setup time. Furthermore, the required energy for a PGC from sleep to active state is summarized in Table A2-4. It is shown that NMOSH requires only 26.5pJ whereas PMOSH takes 96.6pJ, resulting in a 72.6% reduction.

In order to maintain the functionality in logic sequential circuits, we have to keep the voltage variation of power rails (VDDV) in standard cells as small as possible. Any VDDV variations cause the change of computing time of a logic cell. In nowadays sequential design philosophy, the setup and hold time violations are prevented by computation speedup or buffer insertion under the assumption that the voltage of power rails in each logic cell rises or falls together. If the assumption does not hold, the system function correctness becomes much more difficult. In other words, PGC insertion with improper MOS sizing may cause different IR-drops in

different logic cells, resulting in malfunction to the overall system. To see the features of a NMOSH and a SLVCMOS in terms of IR-drop and current sink, we apply different number of inverters (min. size) connected in parallel, and trigger those inverters at the same time by a continuous rectangular waveform. Then, the maximum IR-drop of virtual VDD and the maximum affordable current sink is depicted in Fig. A2-9. It is found that NMOSH not only provides larger current but also keep a smaller IR-drop. This again guarantees the utilization of a NMOSH as the power gating cell for system functionality and leakage savings.

TABLE A2-1. MINIMUM LEAKAGE SEARCH WITH COMBINATIONS OF VG AND VB

	NMOSH-PGC		PMOSH-PGC	
PVT conditions	Minimum current	[VG,VB] @ min. current	Minimum current	[VG,VB] @ min. current
Fast/0.55V/125^{0}C	121.96pA	[-0.3V, -0.9V]	96.78pA	[0.9V, 1.4V]
Slow/0.45V/0^{0}C	7.65pA	[-0.05V, -0.65V]	6.75pA	[0.65V, 0.1V]

Power gating cell (PGC) W/L = 0.6um/80nm @ 90nm standard process
NHCMOS consumes a little high leakage then PHCMOS

TABLE A2-2. LEAKAGE VARIATIONS WITH UNCHANGED [VG,VB] BUT CHANGED PVT

	NMOSH-PGC		PMOSH-PGC	
Changed PVT conditions	Changed current	Unchanged [VG,VB]	Changed current	Unchanged [VG,VB]
Slow/0.45V/0^{0}C	17.34pA	[-0.3V, -0.9V]	24.39pA	[0.9V, 1.4V]
Fast/0.55V/125^{0}C	14.46nA	[-0.05V, -0.65V]	90.47nA	[0.65V, 0.1V]

Power gating cell (PGC) W/L = 0.6um/80nm @ 90nm standard process
PHCMOS may consume much higher leakage than NHCMOS after changed PVT conditions with unchanged pre-designed [VG,VB]

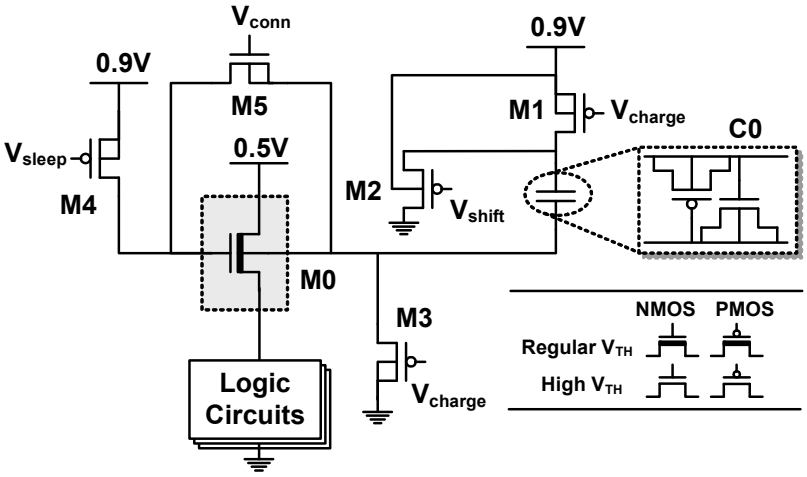


Fig. A2-4. The proposed charge-pumped NHCMOS (CP-NHCMOS).

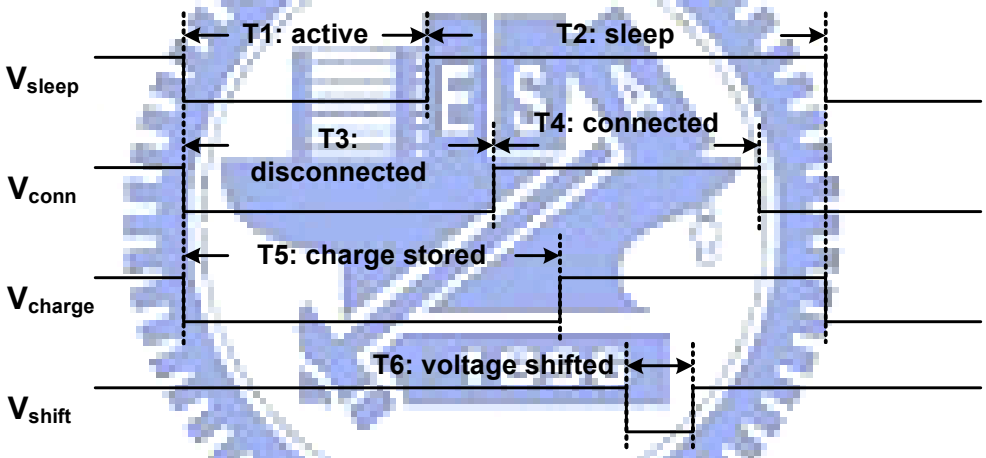


Fig. A2-5. The control signals and the corresponding timing order.

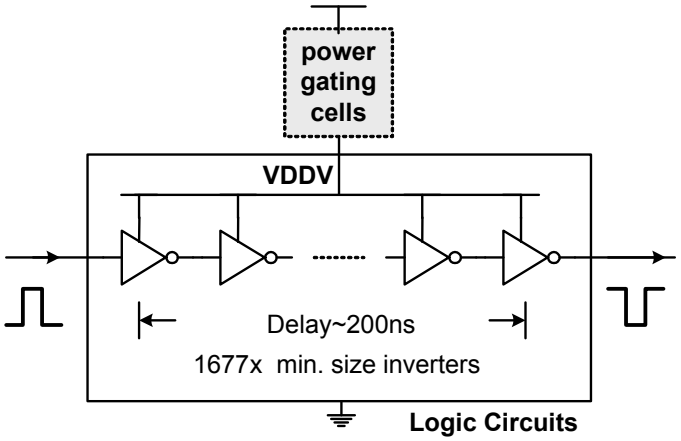


Fig. A2-6. Test circuit for performance evaluations

TABLE A2-3. LEAKAGE CURRENT SUMMARY IN DIFFERENT DESIGN SCHEMES

		Leakage current (A)	
		Worst case	Best case
SCCMOS	PGC only	15.6u	1.48n
SLVCMOS	PGC	3.42n	1.33n
	Aided circuits	Not reported*	
NMOSH	PGC only	2.71u	1.40n
Proposed	PGC	654.1p	122.1p
CP-NMOSH	Aided circuits	5.71n	87.8p

PGC W/L = 12um/80nm @ 90nm standard process
PGC: power gating cell
Worst case: process/voltage/temperature: fast/0.55V/125^{0}C
Best case: process/voltage/temperature: slow/0.45V/0^{0}C
*: The relative circuit sizes of both SLVCMOS PGC and aided circuits are not reported.

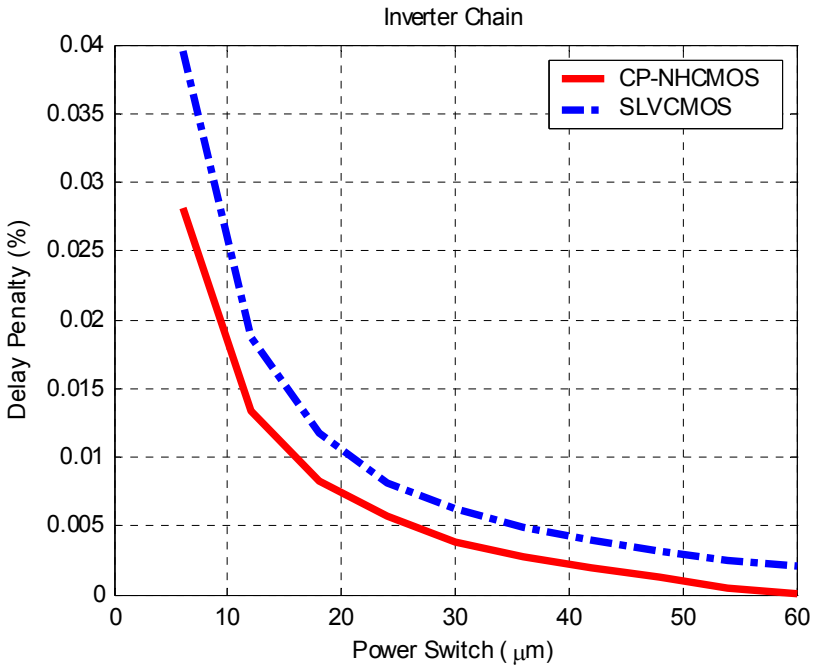
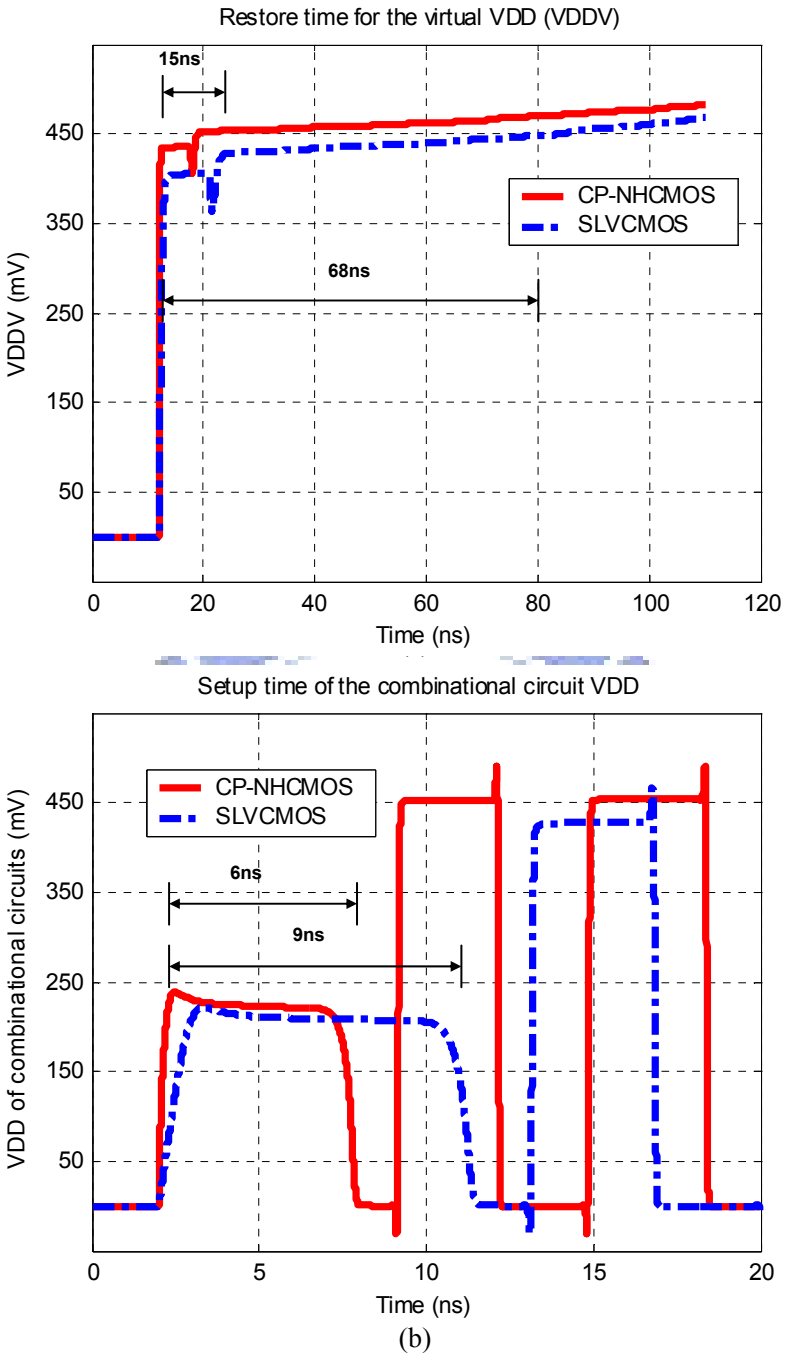


Fig. A2-7. Delay penalty vs. power switch size

TABLE A2-4. REQUIRED ENERGY OVERHEAD FROM SLEEP STATE TO ACTIVE STATE

	Energy	Normalized
SLVCMOS	96.6pJ	100%
CP-NHCMOS	26.5pJ	27.43%



(b)

Fig. A2-8. Restored time of virtual VDD (VDDV)

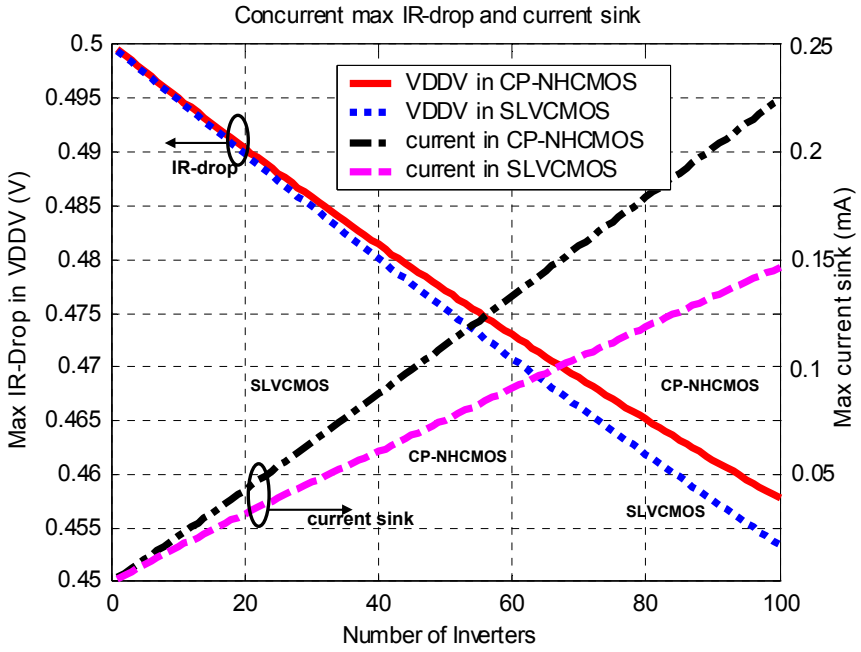


Fig. A2-9. Restored time of virtual VDD (VDDV)

TABLE A2-5. IR-DROPFROM VDD (0.5V) TO VDDV

	Avg	Normalized	P2P	Normalized
SLVCMOS	13.38mV	100%	5.05mV	100%
CP-NHCMOS	8.92mV	66.67%	1.8mV	35.64%

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