國 立 交 通 大 學

電子工程學系 電子研究所碩士班

碩士論文

形成矽化鎳時在矽化鎳與矽接面處離子活化相關研究

Research of Dopant Activation at the Interface between Nickel Silicide and Silicon during Nickel Silicide Formation

研 究 生：楊志祥　　Student：Chih-Hsiang Yang

指導教授：張國明 博士　　Advisor：Dr. Kow-Ming Chang

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摘要

在先進互補式金氧半導體元件裡，當接觸尺寸縮小至奈米等級，源極及汲極的接觸電阻也會隨之增加。因此，金屬矽化物的技術應用在源極及汲極已經被開發用來同時降低接觸電阻及接面寄生電阻。在奈米金氧半場效電晶體的製造中，矽化製程是必須的，為了抑制源極及汲極的超淺接面形成所產生的短通道效應。所以，是否具有與矽基材完好介面特性的金屬矽化物，是在製造奈米尺寸的元件時重要的製程考量。在本論文中，我們主要探討離子佈植入矽化鎳再經由後續不同條件的退火製程後，所呈現出的活化量及電特性的研究。吾人結合離子佈植入矽化鎳和固態磊晶再成長的概念來達到低溫在介面處的高活化特性，此結果和吾人準備的傳統高溫退火試片相比較，發現在550度時的片電阻值即可與傳統高溫所得之片電阻值相當，此外，透過I-V和C-V的量測結果，我們可以對我們所製作的接面做理想因子和介面活化濃度的推算，總和所有的實驗結果，此低溫活化的特性是很有潛力取代傳統的高溫退火已獲得高活化的製程。

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Abstract

In advanced CMOS devices, as contact dimensions scale down to nanometer range, contact resistance of source and drain is increased correspondingly. As a result, the technique of metal silicides for poly gate and source/drain has been developed to reduce the contact resistance and the parasitic junction resistance as well. In nanometer MOSFET fabrication, this silicidation process requires considering to suppress short channel effect (SCE) when forming the ultra shallow source and drain junction. Therefore, metal silicides owning a perfect interfacial property with Si above an ultra-shallow junction is considered as a critical module toward the realization of nano-scale CMOS. In the thesis, we want to know the amount of activation and electro-characteristics by different thermal process. The experiments shows that nickel silicide interface dopant activation improved by two-step rapid thermal annealing (RTA)

process. We combined the concept of implant into silicide (IIS) and solid phase epitaxial regrowth (SPER) to lowering the process temperature. Compared with the conventional samples, the results for doping interface had nice sheet resistance at RTA 550℃. By means of I-V and C-V method, we could also discuss the ideality factor and interface dosage. The overall results can promote the low temperature activation and have the potential to replace conventional high temperature anneal.

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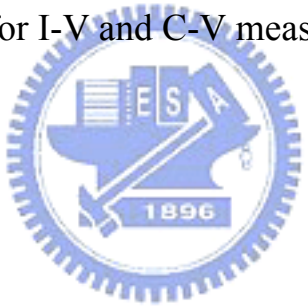

Figure Captions

Chapter 1

Introduction

1.1 General background

In order to improve the performance and packing density of metal-oxide-semiconductor (MOS) integrated circuit, the device dimension has been scaled down to nanometer region. In nanometer complementary metal - oxide- semiconductor (CMOS) circuit with gate length down to 0.1 μm, the parasitic resistance of gate, source and drain region will increase. Those result in the increase of RC time delay and more power dissipation with integrated circuit.

In past years, many people made effort to develop a new technology for reducing parasitic resistance to improve the device and circuit performance. Nowadays, the metal-silicide-related technology has become an integral part of nanometer devices for reducing the parasitic resistance in order to improve the devices and circuit performance. The major advantages of metal silicides can be grouped as follows:

(1) Their low resistivity for gate and interconnect applications

(2) Easy formation by self-aligned technology without any extra mask and compatible with conventional CMOS process.

Where the self-aligned silicide (salicide) process is widely used in MOS manufacturing to reduce the sheet resistance and contact resistance of the gate polysilicon [1]. In nanometer MOSFET fabrication, this silicidation process requires considering to suppress short channel effect (SCE) when forming the ultra shallow source and drain junction. Therefore, metal silicides owning a perfect interfacial property with Si above an ultra-shallow junction that is considered as a critical module toward the realization of nano-scale CMOS. Additionally, as the oxide thickness scaling down with the device dimensions, the gate oxide reliability will also be a concern for the silicided gate process.

Numbers of silicides have been discussed to use to improve device performance, such as $TiSi_2$, $CoSi_2$, $MoSi_2$ and NiSi. Some of silicides, $TiSi_2$, $CoSi_2$ and NiSi, have been used for device fabrication. Moreover, different silicides show different characteristics. Some properties have good merits for device fabrication, but others would negatively affect the integrity circuit processes.

Titanium disilicide ($TiSi_2$) has been the most commonly used metal-silicide in ULSI process, because its low resistivity and relatively high thermal stability. In addition, Ti is very effective at reducing native oxide in contacts, because of the high solubility of oxygen in Ti [2,3]. There are two phases of $TiSi_2$, corresponding to different crystal structures; a base-centered orthorhombic C49 structure and a face-centered orthorhombic C54 structure [4]. The C49 phase forms first and has a high resistivity(60-300 μ ohm-cm) whereas the C54 phase has low resistivity(13-35 μ ohm-cm) so that $TiSi_2$ must be phase transformation from C49 phase to C54 phase [5,6]. However, as line width shrinks below 0.2 μm, the width is not enough for C49-$TiSi_2$ to

convert to C54-$TiSi_2$ completely (even at the temperature above 800 ℃), and the silicide agglomeration temperature limit is about 950 ℃. Bridging phenomenon is also a problem of $TiSi_2$ process. During the silicidation of Ti/Si system, the Si atom is the dominant diffusing species. This facilitates the problem of bridging in the MOSFET salicide structure, silicidation may occur on the sidewalls, as shown in Fig.1.1. The possibility of Silicide bridge forming between the gate and source or drain increases when the physical dimensions of the device decrease. As a consequence, there is an increasing need for new silicide material suitable for nanometer CMOS devices.

Cobalt disilicide ($CoSi_2$) is a promising alternative to $TiSi_2$ for salicide applications [6,7]. The resistivity and thermal stability of $CoSi_2$ are similar to those of $TiSi_2$, but the sheet resistance of $CoSi_2$ is relatively insensitive to decreasing line width, unlike $TiSi_2$ [6,7]. In addition, $CoSi_2$ can be used as a diffusion source to form shallow junctions [7]. However, $CoSi_2$ have two major drawbacks. First, the formation of $CoSi_2$ consumes a relatively larger amount of Si to achieve an equivalent silicide sheet resistance than other silicides, as show in Table.1.1. The non-uniform $CoSi_2$/Si interface or Co spike will lead to the larger junction leakage [8,9]. Large silicon comsuption will restrict the vertical scaling for $CoSi_2$ to achieve shallow junction and not compatible with the SOI process. Second, surface cleaning is more critical; since Co does not reduce an interfacial oxide as Ti does, the existence of the interfacial oxide will affect the $CoSi_2$ formation severely increase the contact resistance. Third, cobalt is not compatible to SiGe process, which is the main method to increase the device mobility.

The Nickel monosilicide (NiSi) which shows improved performance with respect to the three limitations presented above is the candidate to replace the $CoSi_2$. Four main advantages of NiSi are listed below:

(1) Reduced thermal budget

(2) Low Si consumption

(3) Formation controlled by Ni diffusion

(4) Low resistivity phase formation possible on SiGe

Multiple factors contribute to the ease of formation of the low resistivity NiSi with low thermal budget such as the high solubility of Ni in Silicon [10,11]. Ni also has a considerably large diffusivity in Si than Co at low temperature [12]. Once low resistivity NiSi is formed, it does not have to anneal further and reach the NiSi phase. The lower Si content of NiSi compared to $CoSi_2$ is also an advantage. There are two reasons contribute to the lower consumption of Si. The first one is the lower silicon density of NiSi compared to $CoSi_2$. This alone allows for a reduction in Si consumption by more than 10%. Second, since the resistivity of NiSi (~13-14 μ ohm-cm) is lower than that of $CoSi_2$ (~18 μ ohm-cm), the NiSi silicide films can be considerably thinner for the same sheet resistance. Those factors combined typically lead to a reduction in Si consumption of about 35%.

Besides the silicon consumption, bridging phenomenon during silicide formation is also an important issue. In the case of NiSi, silicidation proceeds by the diffusion of metal into the Si. So it can effectively reduce the bridging phenomenon. Recently, in order to reduce the poly depletion effect, metal gate is adapted to the VLSI manufacturing again. Since the

work function of NiSi can be modulated by doping different dopants such like boron, phosphorous, and arsenic [13], this property makes the NiSi suitable for nanometer CMOS technology. In addition, the film stress of NiSi is also much lower than that of $TiSi_2$ and $CoSi_2$. Because of above advantages, nickel monosilicide has received more attention over the last years.

1.2 Motivation

The rapid advance of integrated circuit technology has moved the minimum feature size into nanometer region. In the nano-device generation, the reliability and performances of CMOS have suffered some problems which about gate-leakage and poly depletion. In order to improve these problems, it is a tendency to choose new materials. Metal/high-k gate stack technology is a promising structure since it provides both low gate-leakage and minimal poly depletion effect [14]. Although Metal/high-k gate stack technology will be the mainstream technology in the future, as shown in Fig.1.2, there are still some drawbacks need to be overcome. The one of these is thermal reliability for high-k dielectric.

Hf-silicate which is the most plausible near-term candidate for high-k dielectric. However, it can not tolerate high temperature process, because that high-k dielectric will crystallize under high temperature process. With the high-k dielectric crystallization, the gate-leakage current will increase dramatically. Since the thermal reliability is playing an important role for Metal/high-k gate stack technology, it is why that NiSi will be chosen to the metal gate material. NiSi attributed to the low temperature process window.

However, it needs high temperature annealing to achieve high implanted dopant activation in the S/D region when adapted gate first (self-aligned) process. The threshold voltage (Vt) adjustment in the gate region also needs high level dopant activation (high thermal budgut).

In parallel with the gate dielectric engineering to improve the high-k dielectric‘s thermal reliability, we are interesting in the project about low temperature activation. If the process temperature after gate dielectric formation can be lowered, the high-k dielectric crystallized problem in process integration can also be minimized. We combined the concept of implant into silicide (IIS) and solid phase epitaxial regrowth (SPER) to lowering the process temperature. These two methods lower the dopant activation temperature through the concept of change the surface energy of silicon and pile up the dopant concentration by dopant segregation (IIS) and/or higher the solubility of the dopant in Si through the Si re-crystallization process. Details about these two methods with our experiment will be discussed in the following chapters.

1.3 Organization of the Thesis

In this thesis, we concentrate our efforts on the activation of B and P implant through silicide by RTA process. In chapter 1, brief introduction metal-silicide technology history evolution and the motivation of this thesis are mentioned. In chapter 2, find the optimized recipe to forming nickel monosilicde. In chapter 3, first overview of metal-silicide technology is given to describe the various applications and process technologies. Second the process flow of fabrication will be described. In chapter 4, the detail

discussion of characteristics includes physical properties, electrical properties and doping concentration extraction. In chapter 5 is conclusions and chapter 6 is future works.

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Chapter 2

Formation of nickel silicide

2.1 Introduction

With the lower formation temperature and lower silicon consumption, nickel silicide overcomes some limitations of cobalt silicide, and provides a scaling ability to push the device into the 30 nm technology range. For successful process integration, key material feathers and formation limitations need to be understood to minimize adverse effects on the electrical characteristics of device. A two step RTA process was shown to provide an optimal integration of NiSi technology [1]. Under the two step process, in this chapter, we would compare the sheet resistance of silicide on crystal silicon by different Ni deposition system, and select the better one as our starting deposition source in the following experiments. Also, as being a metal gate material, we compared the silicide sheet resistance formed on different a-Si source. Four point probe was adapted to measure the sheet resistance, SEM cross-sectional image would be inspected the silicide thickness, and using AFM to compare silicide roughness.

2.2 Sheet resistance test

Before the experiment begins, determining the best recipes for silicide formation is necessary. First of all, the Ni deposition source must be decided. P-type (100) oriented Si wafers was prepared for the silicide formation substrate. After a standard RCA clean process, we deposited Ni 20 nm with Dual E-Gun Evaporation System and Sputtering System respectively. Both samples were then rapid thermal annealed (RTA) at 350℃/400℃ with different time duration in N_2 ambient to form nickel silicide, the recipes listed in Table.2.1. The unreacted Ni film was selectively etched using SPM solution of (H_2SO_4 : H_2O_2 = 3 : 1) at 75~85 ℃ for 45 sec. The sheet resistance measurement results of the remaining silicide were shown in Fig.2.1. Then, we chosen the temperature which in the NiSi formation process window, 550℃ 50sec, as a second RTA process temperature [2], the sheet resistance was shown in Fig.2.2. From the results of Fig.2.1 and Fig.2.2, it shows that the lower sheet resistance of nickel silicide is the nickel deposited with the Dual E-Gun Evaporation System so that the Ni deposition for following experiment was decided by using Dual E-Gun Evaporation System.

Moreover, based on the result of Fig.2.1, it shows that the sheet resistance for the samples annealed at 350℃ was higher than those annealed at 400℃. It is because that 350℃ is not enough to forming NiSi completely, but it can be utilized by second RTA process to transform the silicide from Ni_2Si to NiSi. The second RTA process can lower sheet resistance effectively. In addition, excessive silicidation also must be concerned because it was found that the junction leakage measured on diode structures consisting of a large number of small active area islands [3,4] was greatly impoved by a reduction

of the first RTA thermal budget. As a result, the excessive silicidationcan can be reduced in a 2-step Ni-silicide process with reducing the thermal budget of the first RTA step. From the above mention, we would use 350℃ 30 sec for the first step RTA being the experiment recipe.

In order to fabricate the fully silicide gate stack MOS capacitor structure, we will test the sheet resistance which use different a-Si source to react with Ni. A 300 nm oxide was thermally grown on the p-type (100) oriented Si wafer, and following a 50 nm thick a-Si was deposited using PECVD and HDPCVD, respectively. After a standard RCA clean process, 20 nm nickel was deposited using Dual E-Gun Evaporation System**.** Samples were then rapid thermal annealed (RTA) at 350℃ for different time duration in N_2 ambient to form nickel silicide, the recipes listed in Table.2.2. The unreacted Ni film was selectively etched using a solution of H_2SO_4 : H_2O_2 = 3 : 1 at 75~85 ℃ for 45 sec. The results were shown in Fig.2.3(a). Then, we chosen the temperature which in the NiSi formation process window, 550℃ 50sec, as a second RTA process temperature, as shown in Fig.2.3(b). From the results of Fig.2.3(a) and Fig.2.3(b), the lower sheet resistance of nickel silicide is formed by the PECVD System so that the a-Si deposition which was used for fully silicide gate material.

2.3 SEM cross sectional view inspection

In order to identify the real thickness of the as-deposited Ni film and the NiSi layer formed, scanning electron microscope (SEM) was used for cross sectional view inspection. Fig.2.4 and Fig.2.5 shows SEM images of NiSi

layer formed by RTP annealing at 350℃ for different Ni deposition source by Dual E-Gun Evaporation System and Sputtering System, respectively.

The SEM image of silicide formed for gate stack technology was shown in Fig.2.6, it is formed by PECVD deposited a-Si with Dual E-Gun Evaporation System deposited Ni.

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Chapter 3

Characterization of Boron/Phosphorous Implanted To Silicide by Subsequence Thermal Process

3.1 Introduction

As device dimension is scaled down to deep submicron, not only the size of gate electrode is shrunk, but also the vertical dimension of doped source/drain regions must be scaled to avoid device punch through and short channel effects. In the past, PN junctions were formed by dopant ion implantation into Si substrate followed by high temperature furnace annealing for dopant activation and implantation damage annihilation. However, channeling effect and high temperature dopant diffusion limit the formation of shallow junction. This is particularly important for the p^+n junction because boron is a light element and diffuses fast in silicon. In recent years, many advanced junction formation techniques have been studied using low energy ion implantation, low temperature annealing, and rapid thermal annealing process. These new methods are briefly reviewed as follows **:**

(1) Pre-amorphization of silicon substrate before dopant implantation

Pre-amorphization has been widely used to control the channeling behavior of implanted dopant atoms. After the pre-amorphization of the silicon substrate surface layer, dopant implantation was performed followed

by crystal regrowth and annealing process for the junction formation. Many heavy atoms have been used as pre-amorphization species, such as Si [1] and Ge. [2-3] Solid phase epitaxial (SPE) scheme can be used to regrow the crystal from the amorphous layer at a temperature as low as 550 ℃ [4]. The growth rate depends on the element used for pre-amorphization as well as the dopant implanted following the pre-amorphization. A careful annealing process is needed to annihilate the massive defects and dislocation induced by the pre-amorphization.

(2) Elevated source/drain structure

This method is to raise the source/drain regions by depositing a polysilicon (poly-Si) or amorphous silicon (α-Si) film or growing a selective epitaxial Si or SiGe layer[5-6]. Deposition of poly-Si/α-Si film on the source/drain regions needs an additional lithographic step to define the elevated regions, while the selective epitaxial growth of silicon on the source/drain regions does not need such an additional lithographic step. The elevated source/drain regions made with selective epitaxial growth (SEG) provide a sacrificial layer for silicide formation and an alternative approach for the salicide process. However, the SEG scheme needs a high deposition temperature to obtain good crystallinity in the epitaxial layer. The fact that high temperature process deteriorates the device performance is the main disadvantage of this method[7].

(3) Low energy ion implantation [8-10]

This is an extension of the conventional ion implantation technique. The implantation energy is lower than 1 keV and the implantation dose is typically from 1×10^{14} to 5×10^{14} cm^{-2}. The major disadvantage of this method

is that no commercial implantation system of such a low energy ion beam is available for high throughput mass production with reasonable cost.

(4) IIS/ITM technique

The implant into silicide (IIS) and implant through metal (ITM) processes have been investigated for shallow junction formation. The IIS/ITM process consists of implanting dopants into/through silicide or metal layer and the subsequent thermal annealing to form a silicide-contacted shallow junction [11-14]. The IIS scheme in particular is of much benefit to the formation of shallow junction. This is because metal silicides have a larger nuclear stopping power than silicon for the implanted dopant ions and thus can reduce the channeling effect; in addition, the junction formed by the IIS scheme can be almost free of implant damage, which is mostly confined in the silicide layer. Thus, the post-implant annealing temperature can be lowered while shallow junctions with superb characteristics can be obtained. Moreover, the silicided junction is conformal to the silicide/silicon interface, and thus the possibility of junction penetration by the silicide is reduced.

The need for high-activation, diffusionless junctions and low temperature process for advanced gate stacks have promoted further research in shallow junction formation. Because solid phase epitaxial regrowth(SPER)[15-17] works on the principle that dopants in an amorphous region will activate to a level above the equilibrium solid solubility during crystalline regrowth. Temperature even below 600℃ allow regrowth, and thus activation, with negligible dopant diffusion[18]. In this thesis, we would combine the dopant pile-up characteristic of IIS at interface and the ability of SPER to achieving the formation of N+/P and P+/N shallow junction.

3.2 Experiment

Because the experiment will need to remove the NiSi to measuring the sheet resistance which could obtain the silicide/Si interface dopant activation, we had to get the silicide etched solvent(HNO_3 : NH_4F : H_2O= 4 : 1 : 50) selectivity of silicide to Si. We prepared the p-type (100) oriented Si wafers to form the NiSi and then used SEM to measure the silicide thickness was around 20nm which as shown in Fig.2.5. Before silicide etching test, we measured the sheet resistance of p-type (100) wafer and had formed silicide wafer by four-point probe. Then, we used the silicide removed solvent to etch silicide and took the duration which sheet resistance value up to the p-type (100) wafer value to be the silicide complete removed duration, 60sec. We took the silicide removed solvent to etched p-type (100) wafer for 30min and inspected the etched thickness by AFM, as shown in Fig.3.1 to obtaining the etching rate of silicide removed solvent to p-type (100) wafer. From the experiment, we got the etching selectivity of NiSi/Si substrate was 100 : 1. In the follow-up experiment, we would take the over etching time for 30s to conform the silicide removed completely because of the high etching selectivity.

The sheet resistance experiment samples for the four-point probe measuring structure included experimental and comparison samples. First, experimental and comparison samples were fabricated on p-type/n-type (100) oriented Si wafers. After a standard RCA clean process. Then, a 350 nm isolation oxide was grown on the wafer by wet oxidation at 1000℃ for 35 min. The active regions were defined by the photolithography and etched by BOE (buffered oxide etchant) solution. Then, experimental samples were standard cleaned again to fully remove the contamination.

Following, a 20 nm Ni deposited on the wafer in a Dual E-Gun Evaporation system with a base pressure of less than 5×10^{-6} torr, using a Ni target in vacuum ambient with a deposition rate of about 0.7- 1.0 Å/sec. After the Ni film deposition, the samples were rapid thermal annealed (RTA) at 350℃ for 30 sec in N_2 ambient to form NiSi. The unreacted Ni film was selectively etched using a solution of H_2SO_4 : H_2O_2 = 3 : 1 at 75~85 ℃ for 45 sec. Then, the sample of NiSi were implanted with BF_2^+ / P^+ ions at an energy of 50 and 30 keV to a dose of $5\times10^{15}cm^{-2}$. After ion implantation, followed by rapid thermal anneal (RTA) at 400 to 650℃ for 30 / 60 sec in N_2 ambient for the activation dopant, as shown in Fig.3.2. Process recipe is listed in Table.3.1. Because the selectivity of silicide to Si is large enough, NiSi was removed by silicide etched solvent(HNO_3 : NH_4F : H_2O= 4 : 1 : 50) for 90sec that included overetching 20sec. After above process, the samples were coated the Al 500nm by thermal coater, and used photolithography to define the four-point probe measuring pads. Comparison samples were also standard cleaned again to fully remove the contamination. Following, a 20 nm screen oxide was grown on the wafer by dry oxidation at 950℃ for 30 min. Then, the sample were implanted with BF_2^+ / P^+ ions at an energy of 28 and 43 keV to a dose of $5\times10^{15}cm^{-2}$. After ion implantation, first, removed screen oxide by BOE and following by rapid thermal anneal (RTA) at 600 to 950℃ for 30 / 60 sec in N_2 ambient for the activation dopant, as shown in Fig.3.3. Process recipe is listed in Table.3.2. After above process, the samples were coated the Al 500nm by thermal coater, and used photolithography to define the four-point probe measuring pads. The last step is sintering for 400℃ 10min by furnace for both experimental and comparison samples.

We would also prepare the P+/N and N+/P junction samples of silicide contact for I-V and C-V electrical properties measurement. The samples prepared steps were the same as the above mentioned experimental samples. The different step with the experimental samples was we had not to remove silicde contact and needed to coat Al 500nm at backside. The fabricated process was shown in Fig.3.4 and process recipe is listed in Table.3.1 with the 2nd RTA duration is only 60s.

3.3 References

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Chapter 4

Physical Properties and Electrical Characteristics of Boron/Phosphorous Implanted Through Silicide

4.1 Compare conventional dopant activation and 2-step RTA result of IIS dopant activation

From the data of sheet resistance, we could obtain the result which about dopant activation ability of different situation. In the experimental samples, we used four-point probe to measure the sheet resistance is because that the accuracy of Spreading Resistance Profiling(SRP) in the shallow junction is not enough. So we used four-point probe structure to measure the sheet resistance of experimental and comparison samples and compared them. In order to measure the sheet resistance of shallow junction dopant activation, we must remove the silicide and the method is mentioned in chapter 3. The result of measurement was shown in Fig.4.1(a)(b) and we can obtain that when annealing temperature increased, the sheet resistance would decrease. This method does measure the bulk junction activation so we would get the results of Fig.4.1**.** The following we compared were the different implanted dopant samples. Because the solubility of phosphorous and electron mobility was higher than boron, the measured sheet resistance of phosphorous implanted was supposed to lower than boron implanted, theoretically. And the graphics was shown in Fig.4.2(a)(b)**,** we could prove that the hypothesis

was correct.

From above results, we could observe that the value of IIS N-sub samples was decreased at 450℃. We speculated that it might be due to the counter doping so that we would make a experiment to verify it. We prepared a sample set which used N-sub wafer to form silicide and implanted BF_2 then annealed by RTA at 400℃ 5/15/30/60 s, respectively. The following were that removed silicide and coated Al then measured the sheet resistance, and the results was shown in Fig.4.3**.** According to the results of experiment, we could obtain the counter doping effect did occur at 400℃ 10s so the hypothesis of counter doping was not a main reason. The another opinion which we supposed was the RTA process would affect the grain regrowth so that the overetching of removing silicide would have an influence on sheet resistance measurement.

Because the silicide removed overetching time would maybe affect the doping Si substrate, we would want to know the relationship of overetching time with sheet resistance. We prepared a P-sub sample to form silicide and selected a 2nd RTA recipe, 550℃ 60s, after implanted phosphorous. Then, we used silicide removed solvent to etching it and measured the sheet resistance. The relationship of sheet resistance was :

$$R_S = \frac{\rho}{T - \alpha t} \Rightarrow \frac{1}{R_S} = \frac{1}{\rho}(T - \alpha t) \qquad (1)$$

$$T : thickness, \alpha : etch\ rate, t : time$$

The graphic was reciprocal sheet resistance versus etchin time, as shown in Fig.4.4**.** We obtained that silicide overetching would affect the sheet resistance and were sure that the silicide was removed. Because the relation of reciprocal resistance versus etching time was linearity, we could also

calculate effectively the sheet resistance which without overetching time by this relationship and could know that the doping density was uniform.

4.2 I-V measurement

The experiment recipes of these samples prepared for this measurement was shown in Table.4.1. The I-V graphics were shown in Fig.4.5 and Fig.4.6. The measuring sweep voltage for N-sub samples was form 2V to -2V and P-sub was -2V to 2V. From the I-V curve, we could calculate the ideality factor by :

$$
\begin{aligned}
& I = I_S\left(e^{\frac{qV}{kT}} - 1\right) \\
& \Rightarrow I = I_S e^{\frac{qV}{kT}} \quad as\ qV >> kT \\
& \Rightarrow n = \frac{q}{kT}\frac{\partial V}{\partial(\ln J)}
\end{aligned}
\tag{2}
$$

The current range which we used to extrapolate ideality factor was 0.4V to 0.04V for N-sub samples and -0.4V to -0.04V for P-sub samples. The ideality factor results for N and P samples were shown in Fig.4.7(a)(b) and the ideality factor for N samples had a tendency from low temperature anneal to high temperature but the P samples does not. The ideality factor would be affected by four factors : (1)contact resistance (2) generation-recombination current (3)substrate series resistance (4)high level injection. The ideality factor affected analysis for our experiment would be important. For the contact resistance, because our high implanted dosage, the

MS interface would turn from schottky contact to ohmic contact[1]. Because the substrate series resistance related to the bulk resistance, the N-sub samples would better than the P-sub samples but it does not the main reason. And the extrapolated current range does not the high level injection region so this does not dominate reason. In our opinion, the dominated factor might be due to the defect induced generation-recombination current. We could find the relationship by the Ion-Ioff current graphics. We took the Ion at 1/-1V and Ioff at -2/2V, the results was shown in Fig.4.8(a)(b). The Ioff is the reverse bias current and the reverse bias current is related to the Space Charge Region(SCR). The defects in SCR would provide generation-recombination center to affect the reverse current and ideality factor. For N-sub samples, the ideality factor was more and more lower, it is due to the high temperature anneal would recover the defects and the P+/N and N+/P interface moved away from the MS interface. Moreover, high temperature anneal would also activate the implanted bulk dopant so the N-sub samples had this tendency. In addition, the ideality factor of P-sub samples would affect apparently by the defects so the ideality factor of P-sub does not have a good tendency.

4.3 C-V measurement

4.3.1 C-V measurement introduction

The capacitance-voltage(C-V) measurement was a method which could calculate dopant activation that silicide dopant segregation and pile-up at interface. In this part, the measured capacitance was depletion-layer capacitance and the model was shown in Fig.4.9**.** The depletion-layer

capacitance per unit area is defined as $C_D=dQ_D/dV=\varepsilon_S/W_D$, where Q_D is the incremental depletion charge on each side of the junction(total charge is zero) upon an incremental charge of the applied voltage dV. For one-side abrupt junctions, the capacitance per unit area is given by :

$$C_D = \frac{\varepsilon_S}{W_D} = \sqrt{\frac{q\varepsilon_S N}{2}}(\psi_{bi} - V - \frac{2kT}{q})^{-1/2} \qquad (3)$$

where V is positive/negative for forward/reverse bias. Rearrange the above equation leads to :

$$\frac{1}{C_D{}^2} = \frac{2}{q\varepsilon_S N}(\psi_{bi} - V - \frac{2kT}{q})$$

$$\frac{d(1/C_D{}^2)}{dV} = -\frac{2}{q\varepsilon_S N} \qquad (4)$$

It is clear from Eqs.4 that by plotting $1/C^2$ versus V, a straight line should result from a one-sided abrupt junction(Fig.4.10). The slope gives the impurity concentration of the substrate(N), and the extrapolation to $1/C^2=0$ gives (Ψ_{bi}-2kT/q). The interface doping density can be calculate by the equations[2] :

$$N = -\frac{2dV}{q\varepsilon_S d(1/C_D{}^2)} \qquad (5)$$

$$\psi_{bi} = \frac{kT}{q}\ln\frac{N_A N_D}{n_i{}^2}$$

$$\Rightarrow N_A = \frac{n_i{}^2}{N_D}e^{\psi_{bi}q/kT} \ \ and \ \ N_D = \frac{n_i{}^2}{N_A}e^{\psi_{bi}q/kT} \qquad (6)$$

4.3.2 Results and Discussion

The C-V graphics were shown in Fig.4.11 and Fig.4.12. From C-V measurement, we used Eqs.5 to calculate the average substrate dopimg density and by plotting $1/C^2$ versus V to obtain Ψ_{bi}. The results of Ψ_{bi} was shown in Fig.4.13(a)(b) and then combined Eqs.5 and Eqs.6 to obtain the doping density P+ and N+ region, as shown in Fig.4.14(a)(b). From above results, we could prove it again that when the annealing temperature was increasing, the doping density were more and more lower was due to the junction went away from interface. Moreover, the dopant activation was started to activate from the pile-up interface of MS. The phenomenon could also be explained that the C-V measurement was measure the junction interface. Because away from the MS interface, the measured result would exhibit the junction interface characteristic so that the higher temperature annealing showed the lower doping density.

4.4 SIMS

We took the IIS N-sub and P-sub samples with 2^{nd} RTA 650℃ 60s for SIMS analysis. The graphics was shown in Fig.4.15(a)(b)**.** From the SIMS graphics, we could observe the N-sub sample which had two boron peak. The first peak might be the dopant segregation at interface pile-up and the second peak might be the implanted dosage peak. It means that for N-sub sample the implanted energy was maybe too large. According to this result, we could have an another evidence to explain that the ideality factor of N-sub samples does better than P-sub samples. Because the measured I-V characteristic might be the second peak PN junction and at higher annealing temperature would cause dopant activation which excepted interface region

so that the ideality factor was better than the P-sub samples. Another is the boron activated ability was higher than phosphorous. Moreover, the reverse bias current would also decrease, the reason was also the PN junction which we measured was away from the more defects MS interface. The SIMS for P-sub did have the result which we expected. It had the shallow junction characteristic and the pile-up just at the MS interface. The result could also explain why the ideality factor and reverse bias current were not good.

4.5 References

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Chapter 5

Conclusions

In this thesis, we have been investigated the activation of B and P implant into silicide (IIS) by RTA process. With the device scale down, the shallow junction would be important because shallow junction formation can effectively suppress short channel effect(SCE). Based on the IIS dopant segregation pile-up at interface and SPER, our experiment would achieve the high dosage activation and do not use high temperature annealing. We could find the best recipes for the device fabrication in the future. In the first part experiment, regardless of N and P-sub samples at 550℃ annealing that are all had better sheet resistance which compared with conventional high temperature annealing. In spite of overetching time was taken for 30s, the sheet resistance values also closed to the conventional samples. In second part experiment, we would use another method to measure the activation condition. By the C-V and I-V measurement, we could realize the interface dopant distribution and the integrity of P/N or N/P junction. All in all, we achieved our purposes by means of the experiment and the results were beneficial.

Chapter 6

Future Work

In order to improve the shallow junction properties, we could make some experiments to revise it in the future. We could use Spreading Resistance Profiling(SRP) to check the junction depth and the doping density. According to the actuality junction depth, we could also know that our fabricated junction does conform to the shallow junction condition or not. In addition, we could also find the optimum value of annealing temperature. As long as the doping activation density can attain our expectation at more lower annealing temperature, we can replace the high temperature fabrication.

	Resistivity (μΩ-cm)	Silicidation Temperature (℃)	Silicon Consumption	Moving Species	Film Stress (dyn/cm2)
$TiSi_2$	12-15	800-950	0.9× T	Si	1.5×10^{10}
CoSi	-	375-500	0.91× T	Si	-
$CoSi_2$.	18	550-900	1.04× T	Co	1.2×10^{10}
NiSi	15-16	350-700	0.82× T	Ni	6×10^{9}
$NiSi_2$	35-50	700-850	-	Ni	-

T stands for thickness of silicide formed

Table.1.1 Comparison the characteristics of Ti, Co and Ni silicides.

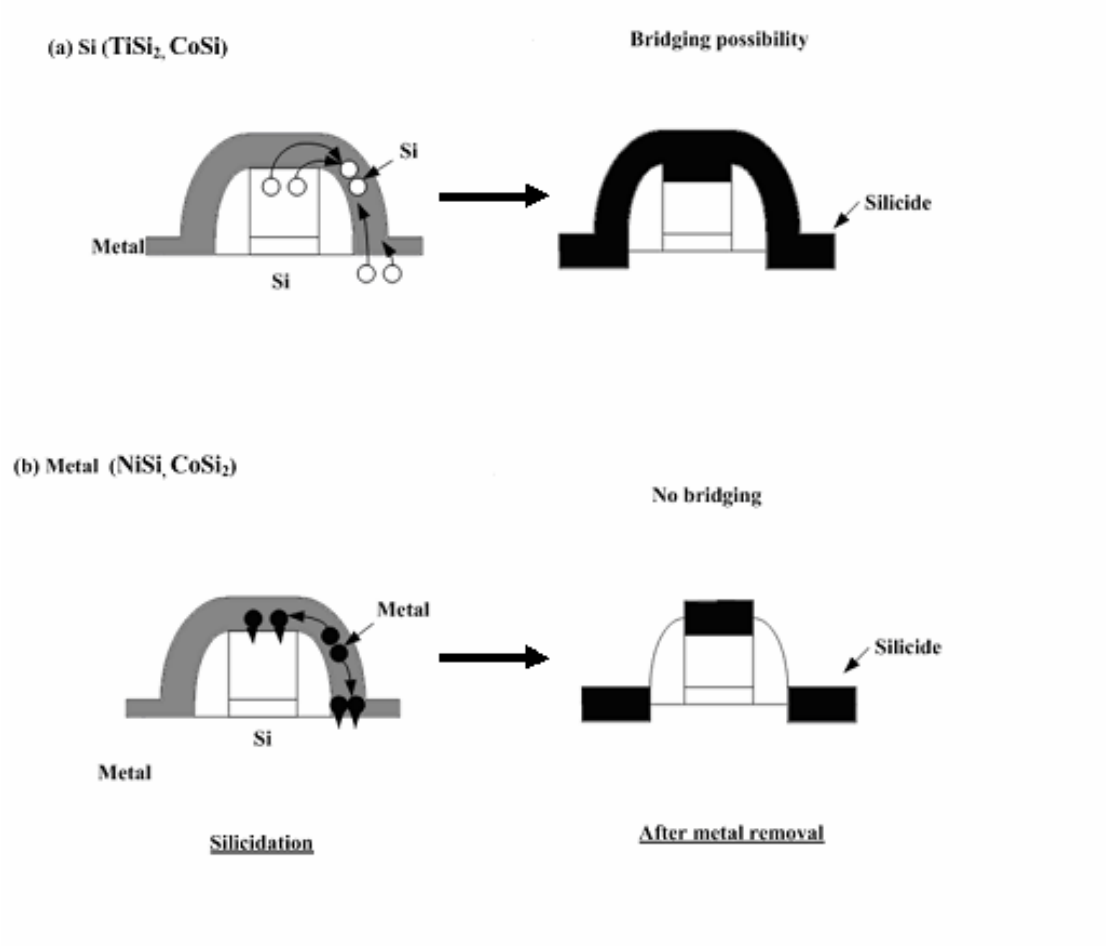


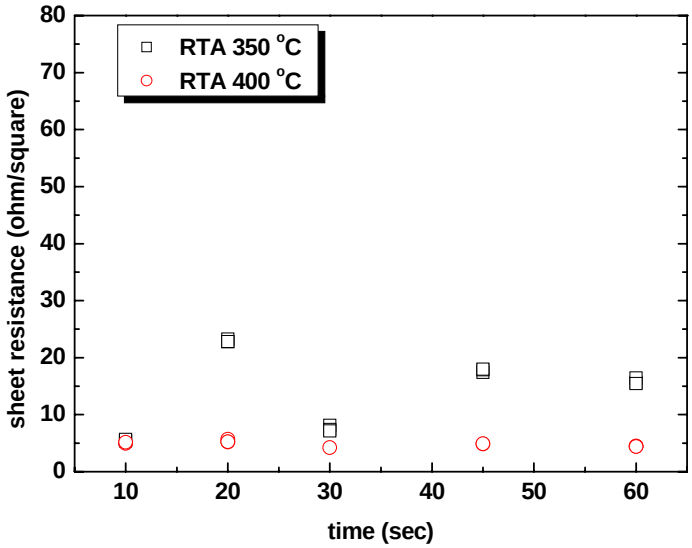
Fig.1.1 With/without bridging phenomenon of metal silicides.

Process Name	P856	P858	Px60	P1262	P1264	P1266	P1268	P1270
1st Production	1997	1999	2001	2003	2005	2007	2009	2011
Process Generation	0.25μm	0.18μm	0.13μm	90 nm	65 nm	45 nm	32 nm	22 nm
Wafer Size (mm)	200	200	200/300	300	300	300	300	300
Inter-connect	Al	Al	Cu	Cu	Cu	Cu	Cu	?
Channel	Si	Si	Si	Strained Si	Strained Si	Strained Si	Strained Si	Strained Si
Gate dielectric	SiO_2	SiO_2	SiO_2	SiO_2	SiO_2	High-k	High-k	High-k
Gate electrode	Poly-silicon	Poly-silicon	Poly-silicon	Poly-silicon	Poly-silicon	Metal	Metal	Metal

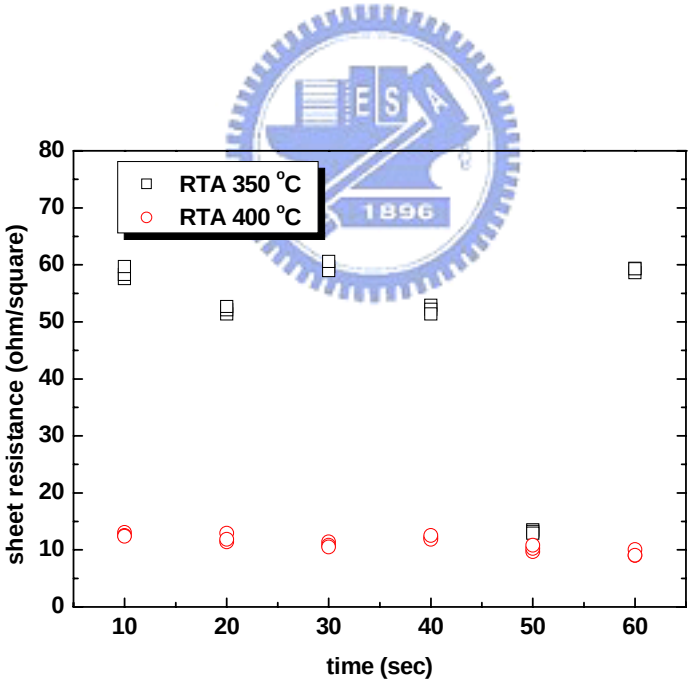
Introduction targeted at this time

Subject to change

Fig.1.2 Continuation of Moor's Law from intel's high-k/metal gate announcement (2003)

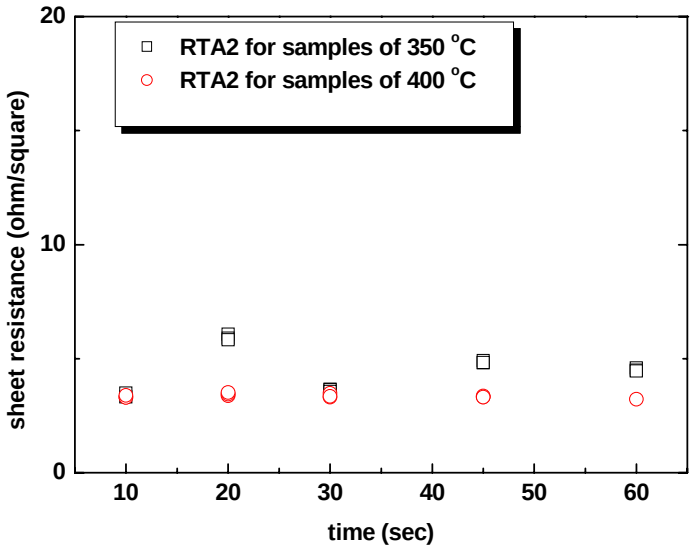


(a)

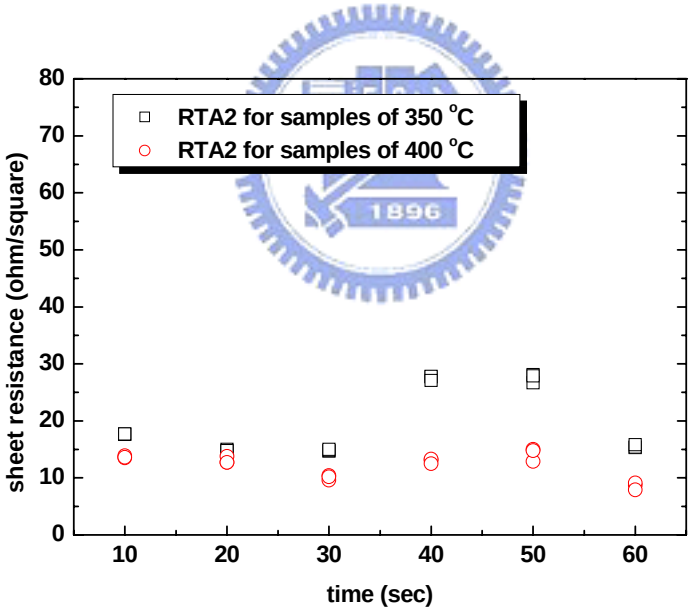


(b)

Fig.2.1 Results of nickel silicide sheet resistance: (a) Dual E-Gun Evaporation System (b) Sputtering System

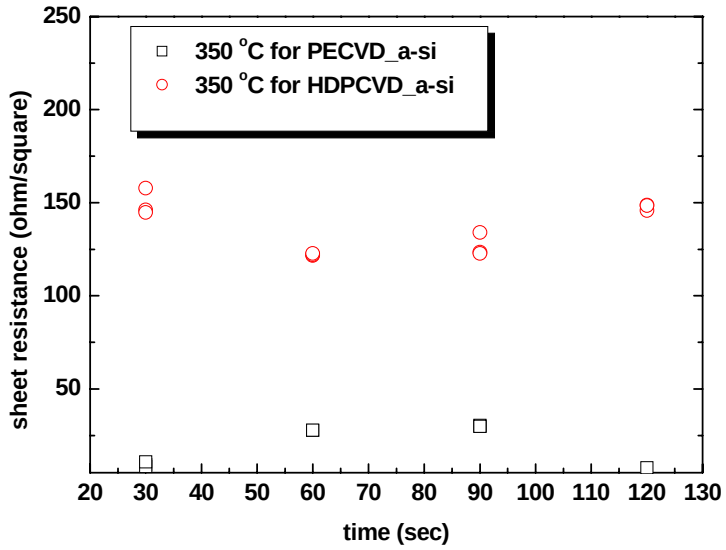


(a)

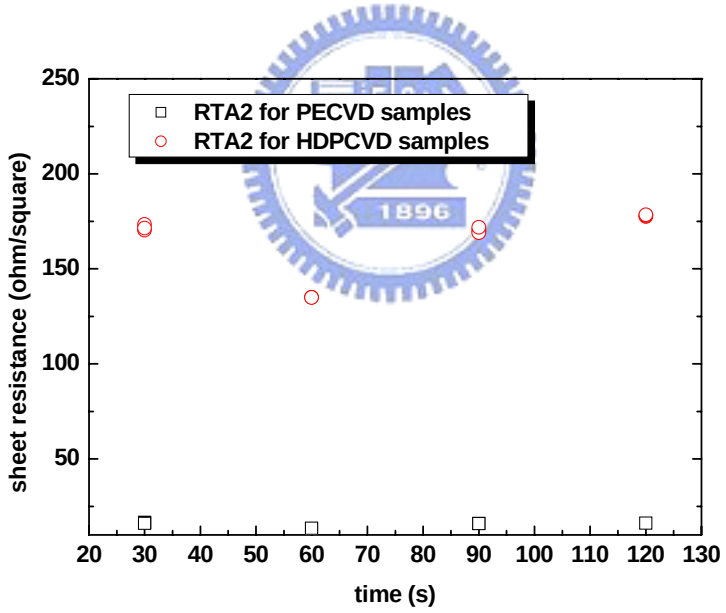


(b)

Fig.2.2 Results of RTA2, 550℃ 50sec, treatment to forming NiSi: (a) Dual E-Gun Evaporation System (b) Sputtering System



(a)



(b)

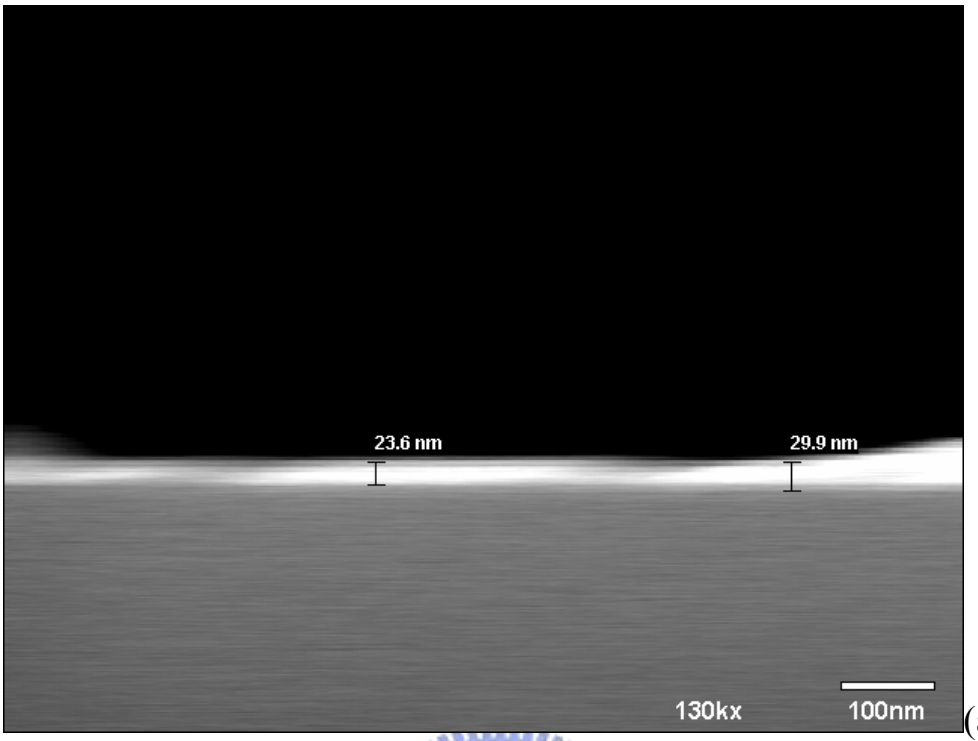
Fig.2.3 Results of nickel silicide sheet resistance: (a)first RTA 350℃ with different time for PECVD and HDPCVD a-Si samples (b)all samples were treated by second RTA 550℃ 50sec

	1st RTA	2nd RTA
E-gun Ni	350/400℃ 10/20/30/45/60s	550℃ 50s
Sputter Ni	350/400℃ 10/20/30/40/50/60s	

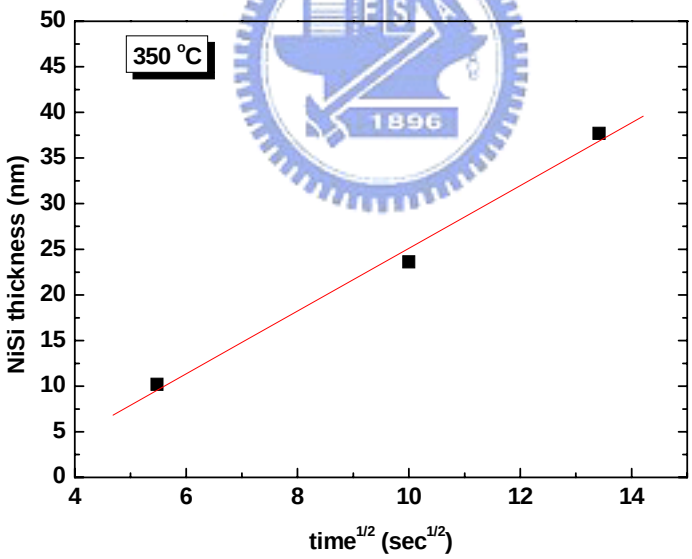
Table.2.1 The recipes of Nickel silicide formation for different Ni deposition system

	1st RTA	2nd RTA
PECVD a-Si	350℃ 30/60/90/120s	550℃ 50s
HDPCVD a-Si		

Table.2.2 The recipes of Nickel silicide formation for different a-Si deposition system

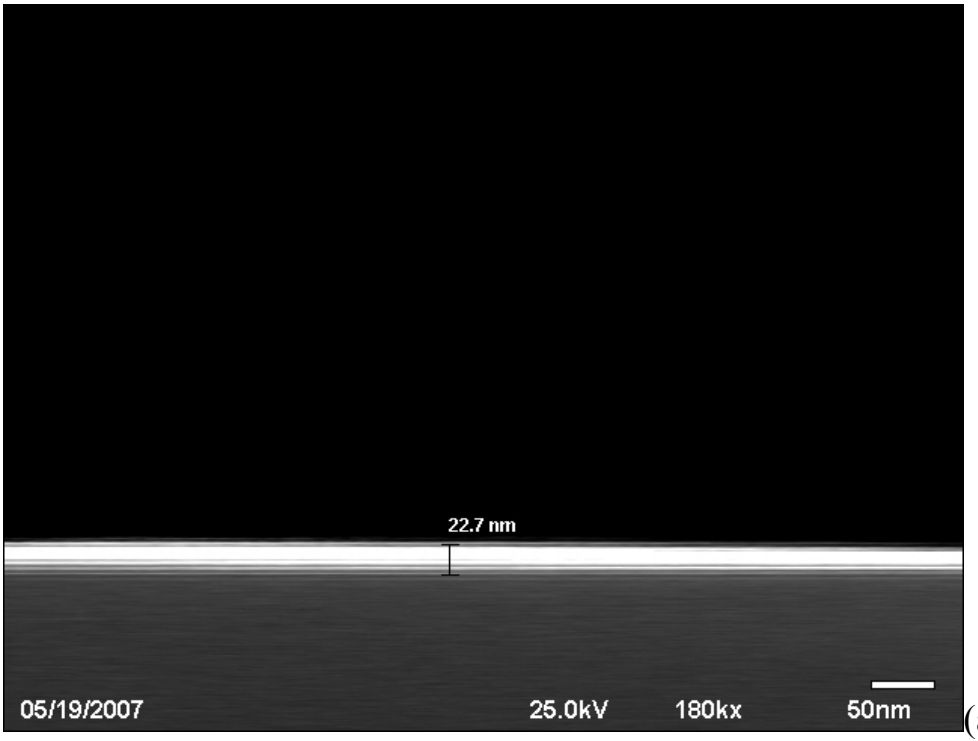


(a)

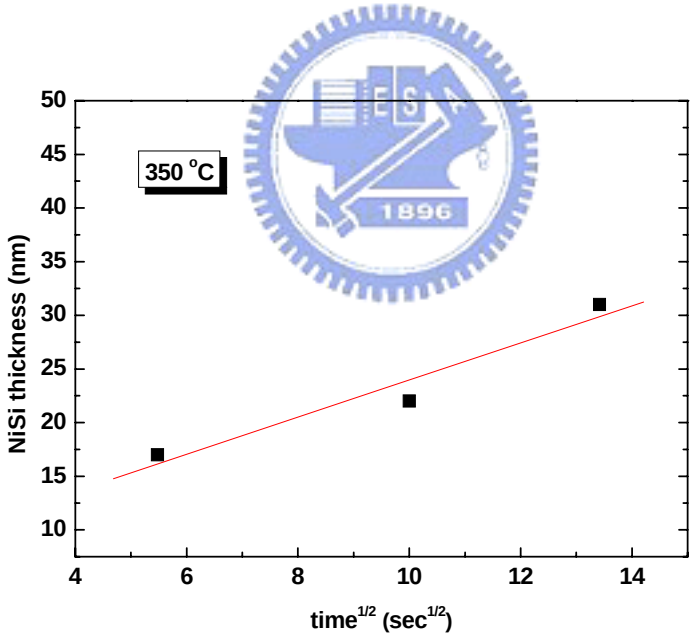


(b)

Fig.2.4 (a)SEM image for nickel silicide which was formed by Sputtering System Ni with single crystalline Si (b)silicide thickness versus square root of time



(a)



(b)

Fig.2.5 (a)SEM image for nickel silicide which was formed by Dual E-Gun Evaporation System Ni with single crystalline Si (b)silicide thickness versus square root of time

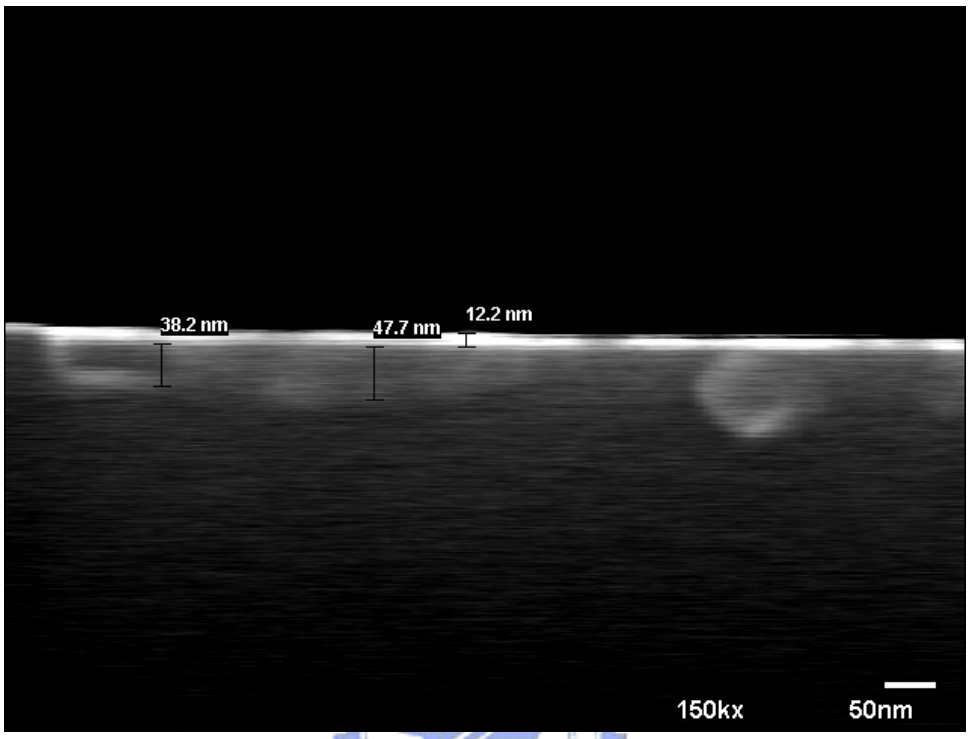


Fig.2.6 SEM image of nickel silicide which was formed by Dual E-Gun Evaporation System Ni with PECVD deposited a-Si

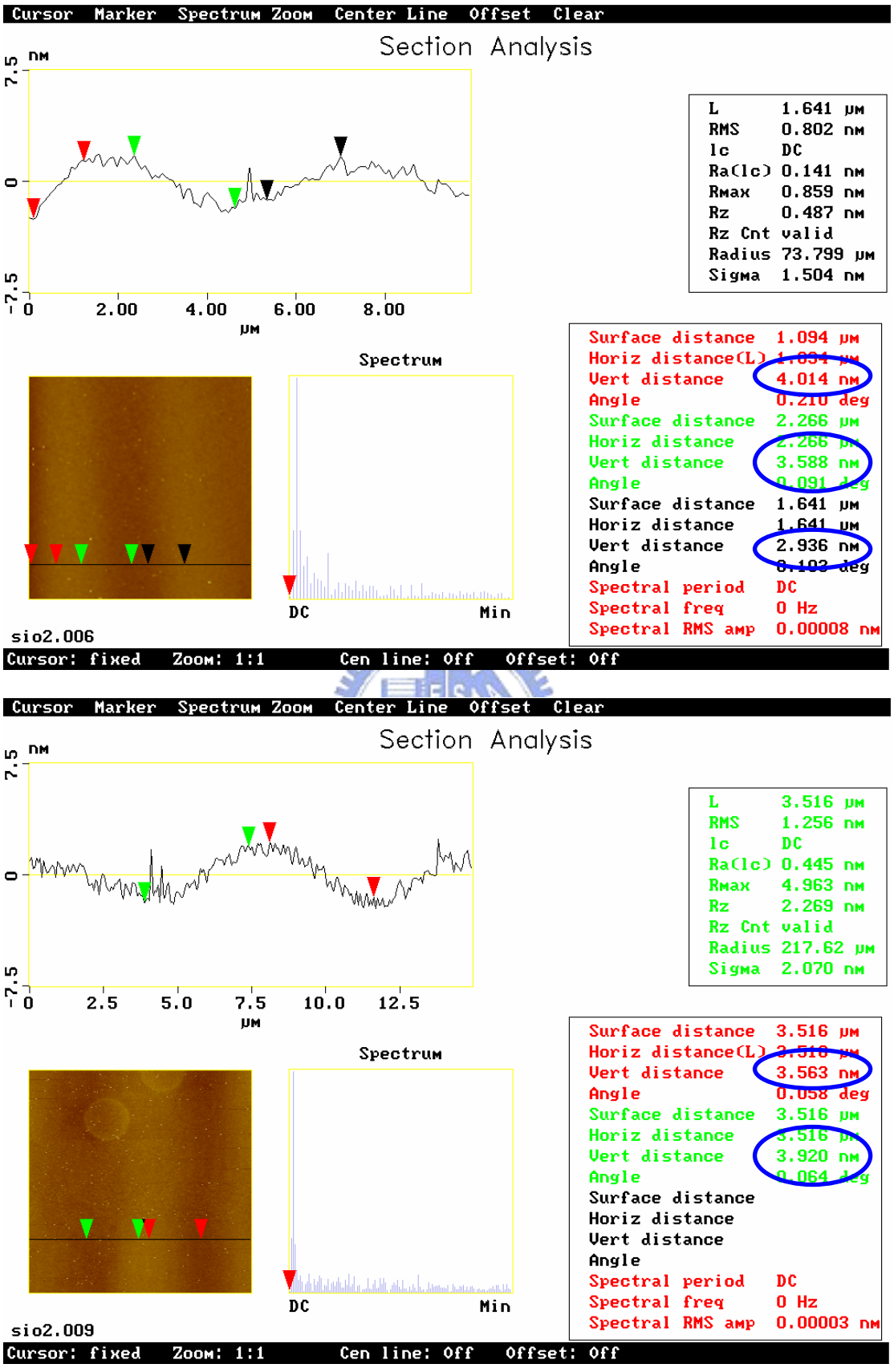
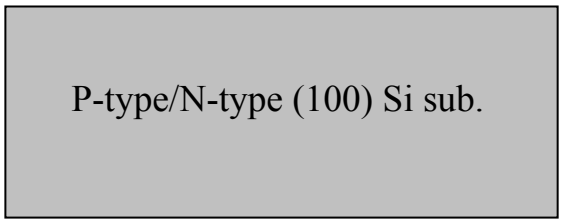
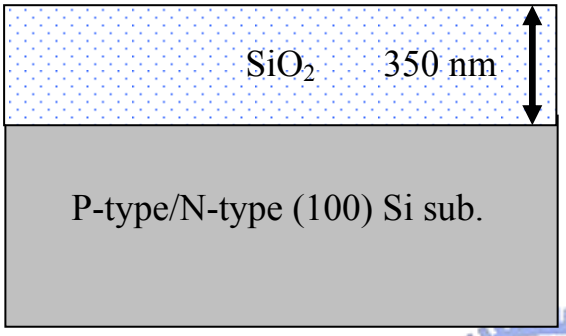


Fig.3.1 AFM inspection image of Si substrate etched by silicide etching solvent for 30min

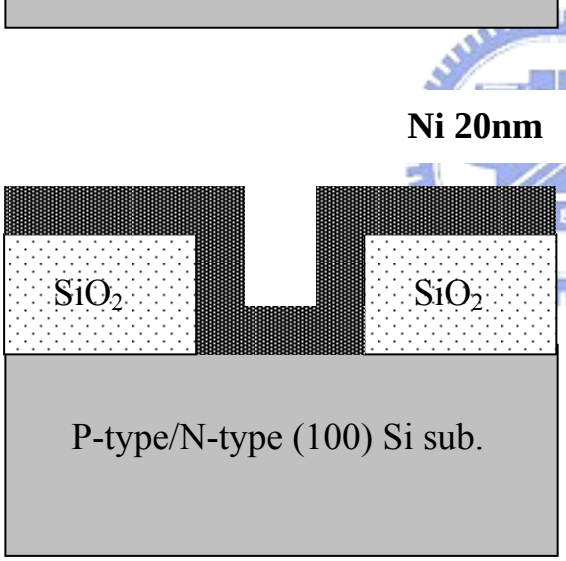
Process flow of experimental samples



● RCA clean

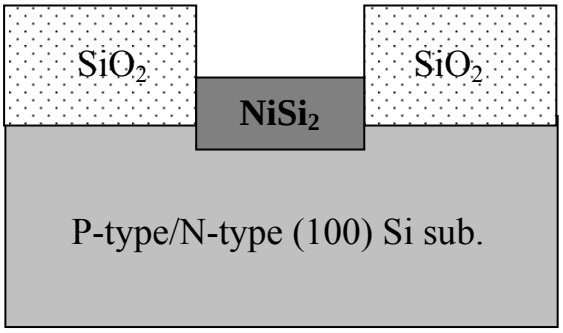


● Thermal wet oxidation 350 nm



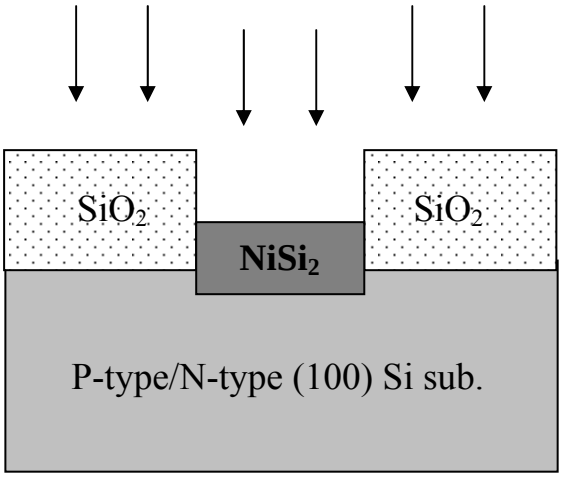
● Define active region (100 μm x 300 μm)

● Ni film 20nm deposited by E-gun

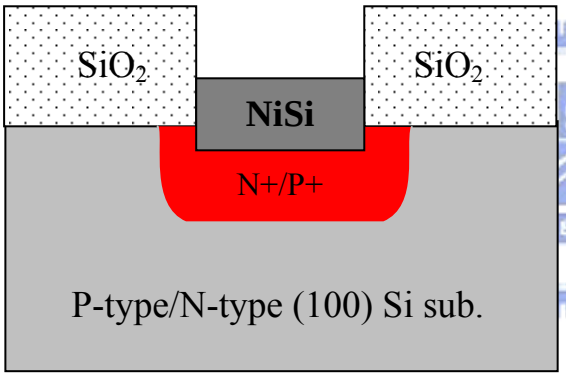


● Silicidation by 1st RTA (350℃ 30s)

● Selectively etch (H_2SO_4 : H_2O_2 = 3 : 1) 45 sec for unreact Ni

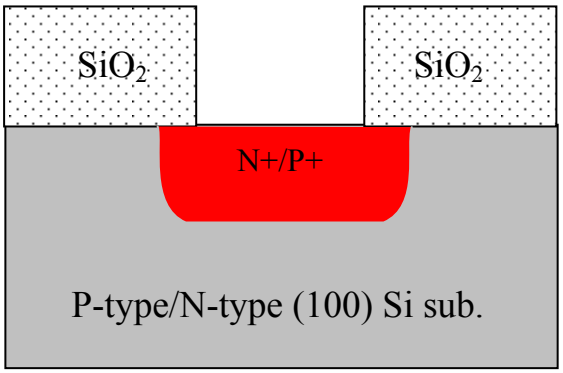


● BF_2 / Phosphorous ion implantation



● Activation and junction formation by 2^{nd} RTA

(400 ~ 650℃)



● Remove silicide by etching solvent (HNO_3 : NH_4F : H_2O= 4 : 1 : 50) 90sec

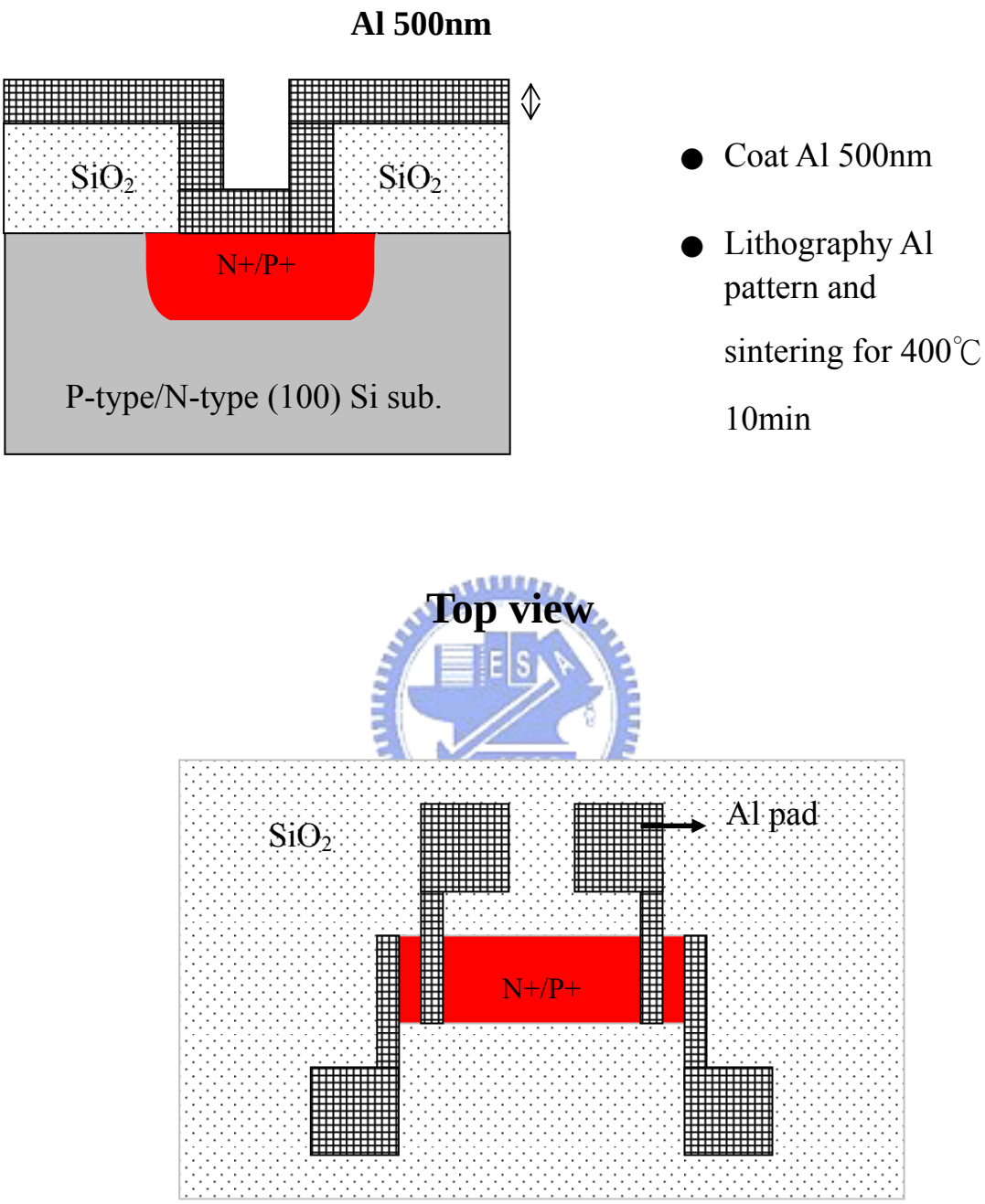
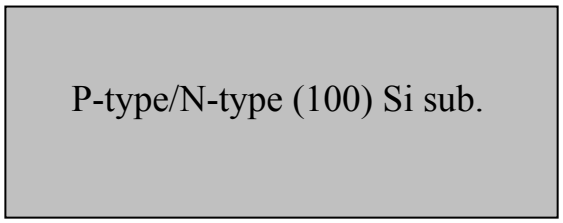
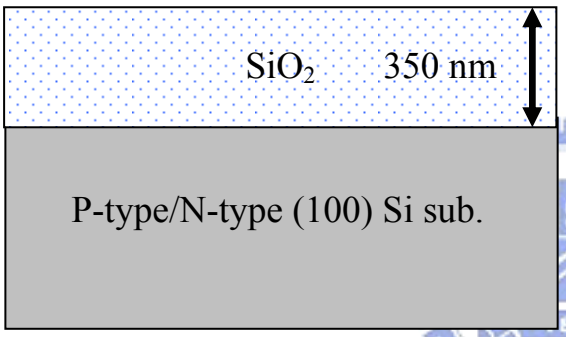


Fig.3.2 Process flow of P+N and N+/P junction by IIS scheme

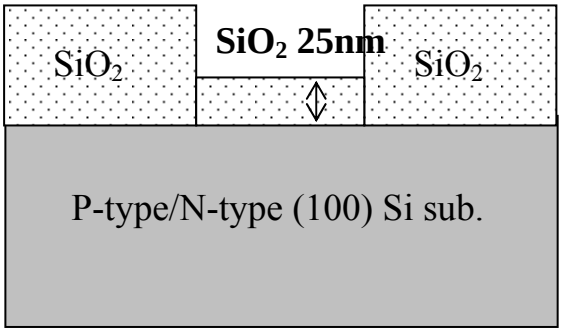
Process flow of comparison samples



● RCA clean



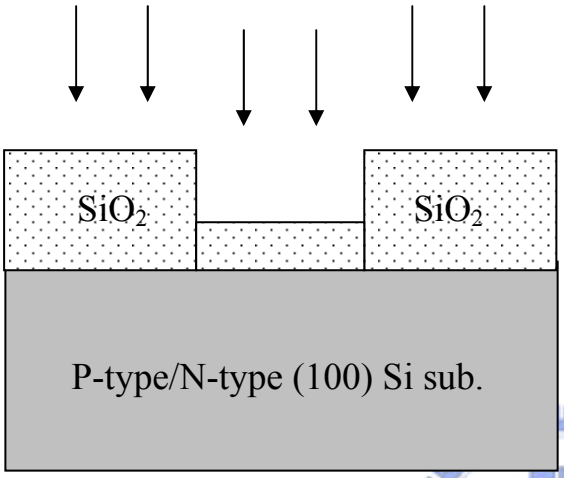
● Thermal wet oxidation 350 nm



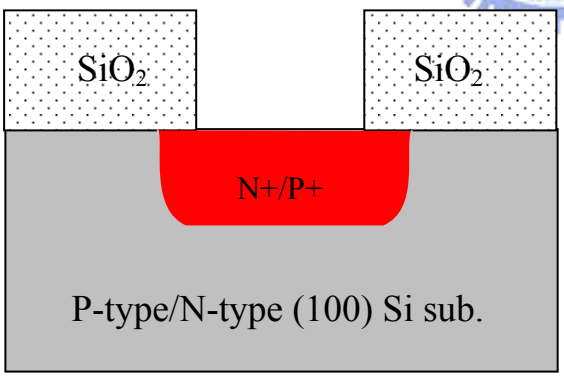
● Define active region

(100 μ m x 300 μ m)

● Thermal dry oxidation 25 nm for screen oxide



● BF_2 / Phosphorous ion implantation



● Remove screen oxide

● Activation and junction formation by RTA

(600 ~ 950℃)

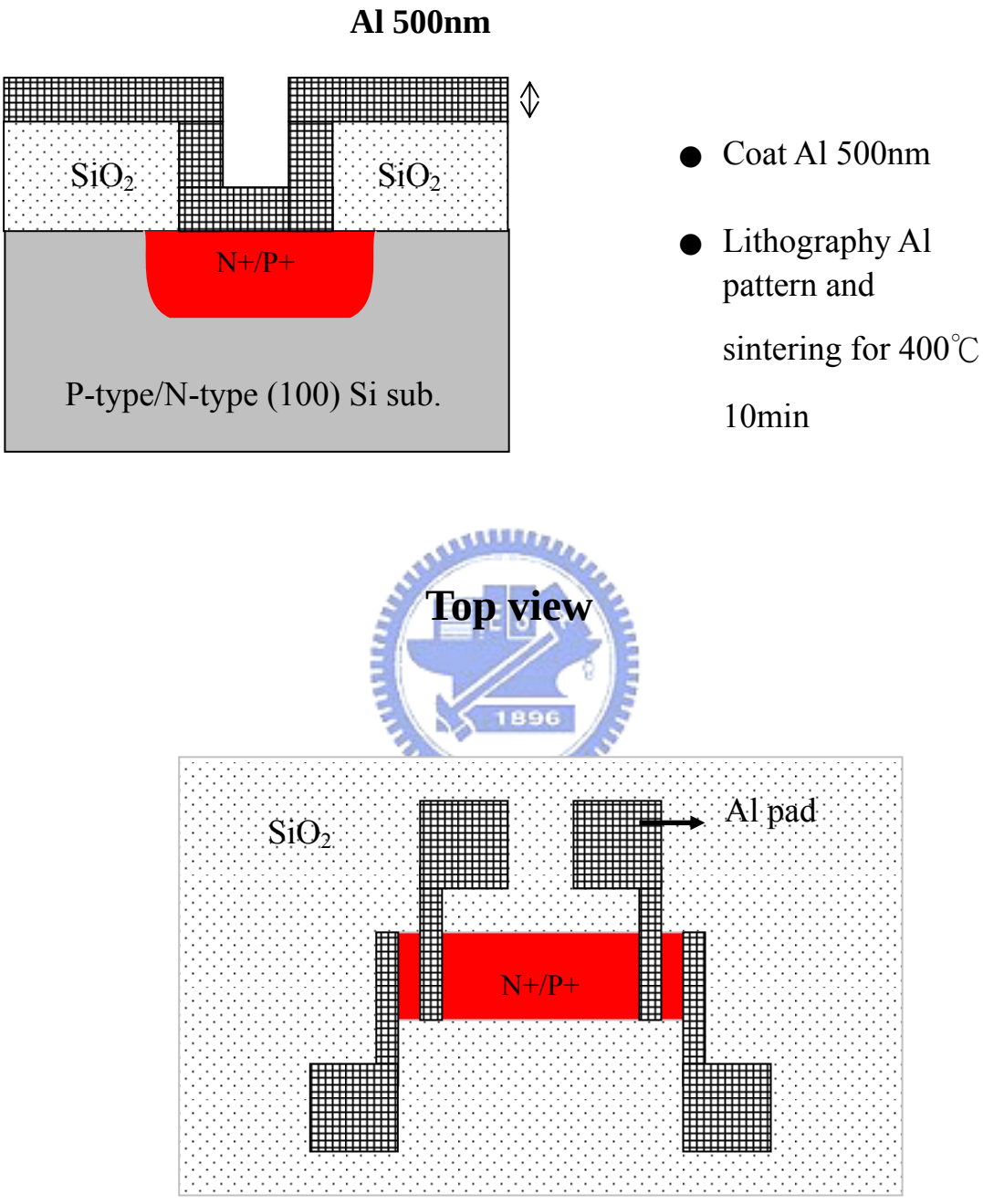


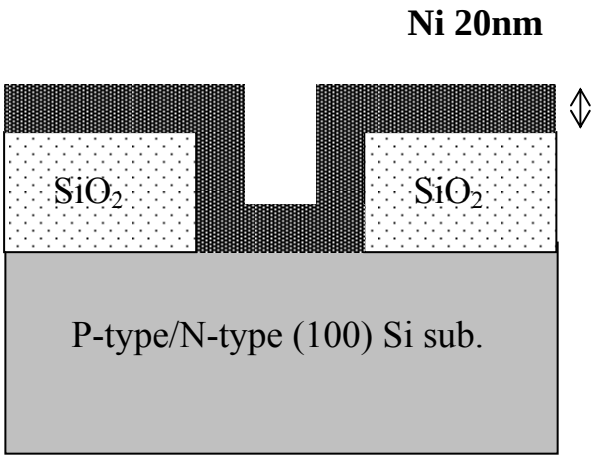
Fig.3.3 Process flow of P+N and N+/P junction for comparison samples scheme

	Implanted ion	1st RTA	2nd RTA
P substrate	**P^+/30 kev/5E15**	**350℃/30 sec**	**400 ~ 650℃ 30 / 60 sec**
N substrate	**BF_2^+/50 kev/5E15**	**350℃/30 sec**	**400 ~ 650℃ 30 / 60 sec**

Table.3.1 Process recipe of P+N and N+/P junction by IIS scheme.

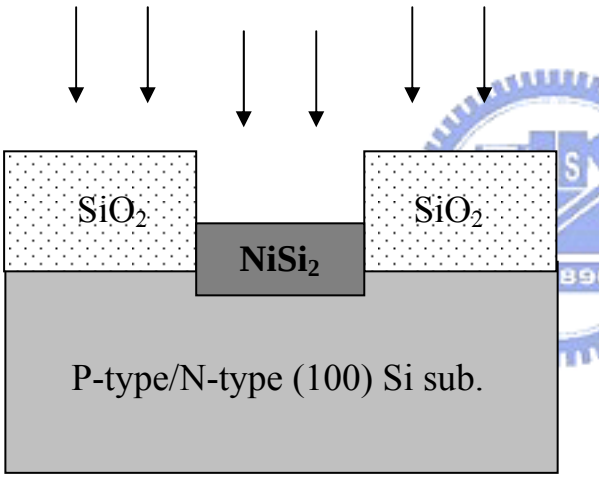
	Implanted ion	RTA
P substrate	**P^+/28 kev/5E15**	**600 ~ 950℃ 30 / 60 sec**
N substrate	**BF_2^+/43 kev/5E15**	**600 ~ 950℃ 30 / 60 sec**

Table.3.2 Process recipe of P+N and N+/P junction for comparison samples scheme.



- RCA clean
- Thermal wet oxidation 350 nm
- Define active region

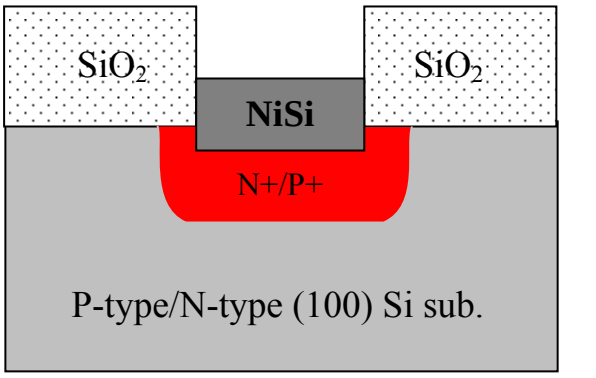
  (300 μ m x 300 μ m)
- Ni film 20nm deposited by E-gun



- Silicidation by 1st

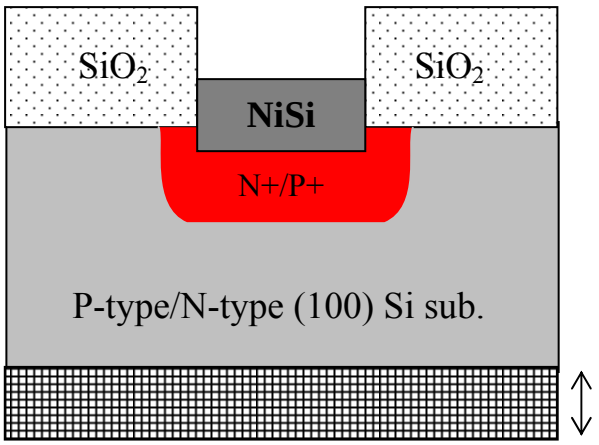
  RTA (350℃ 30s)
- Selectively etch

(H_2SO_4 : H_2O_2 = 3 : 1)
45 sec for unreact Ni
- BF_2 / Phosphorous ion implantation



- Activation and junction formation by 2nd RTA

  (400 ~ 650℃)



● Coat Al 500nm at backside

Al 500nm

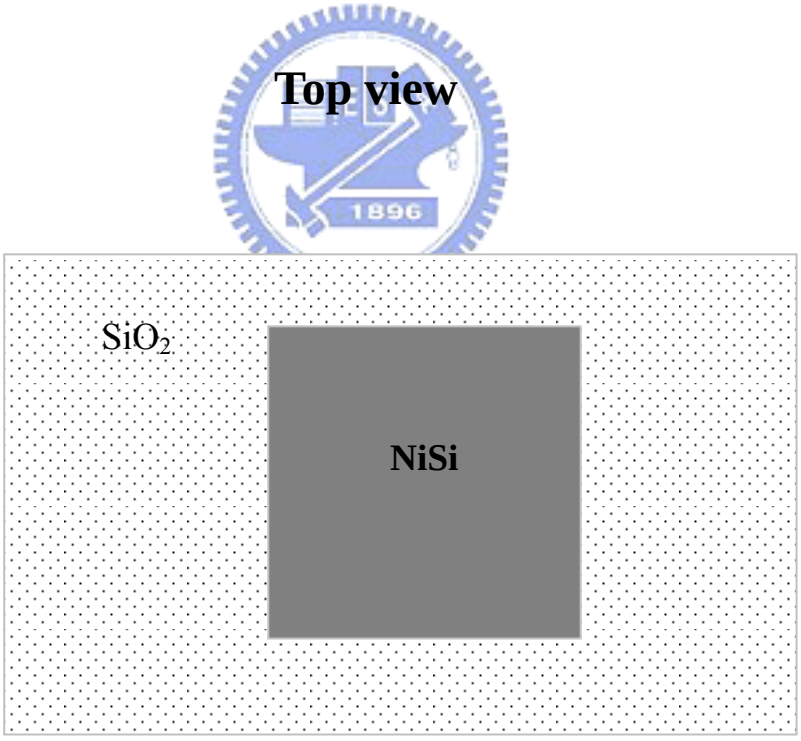
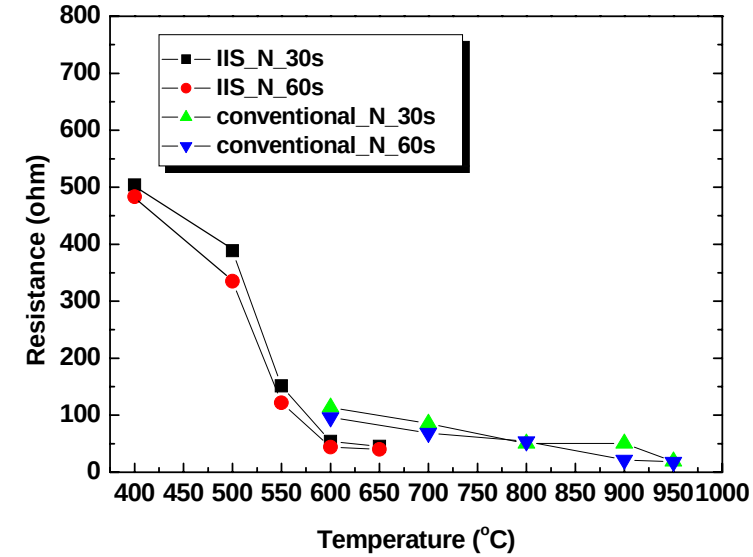
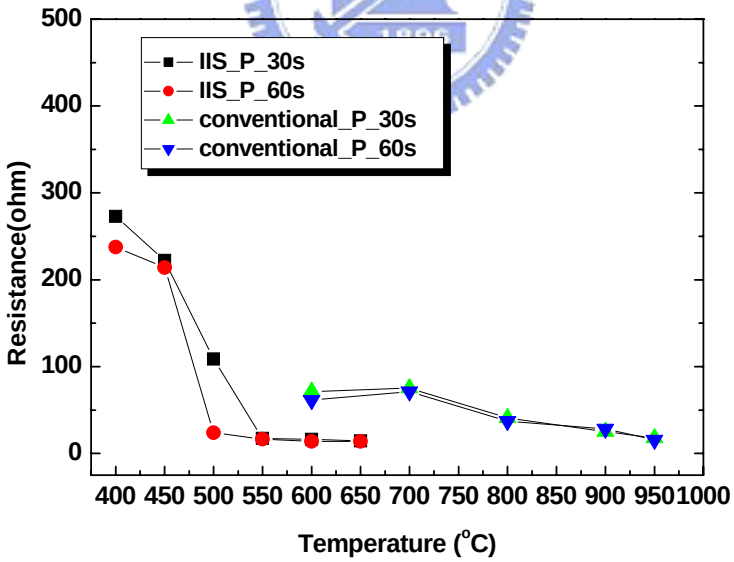


Fig.3.4 Process flow of P+/N and N+/P junction samples of silicide contact for I-V and C-V electrical properties measurement.

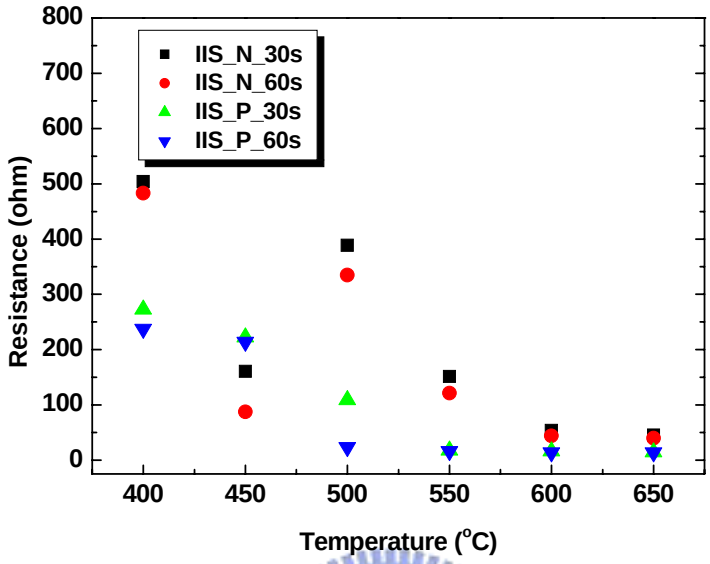


(a)

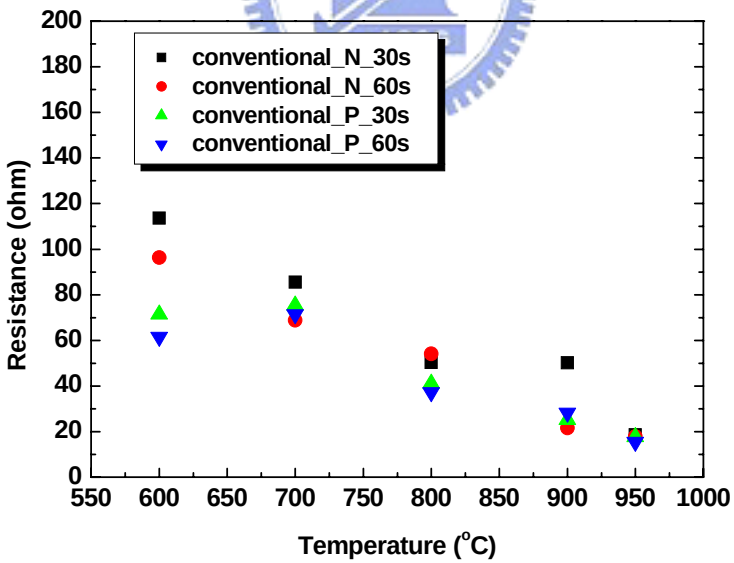


(b)

Fig.4.1 The IIS samples compared with conventional high temperature anneal (a) N-sub Si implanted BF_2 (b) P-sub Si implanted Phosphorous



(a)



(b)

Fig.4.2 The comparison of different Si-sub implanted different dopant (a) IIS samples compared (b) conventional high annealing samples compared

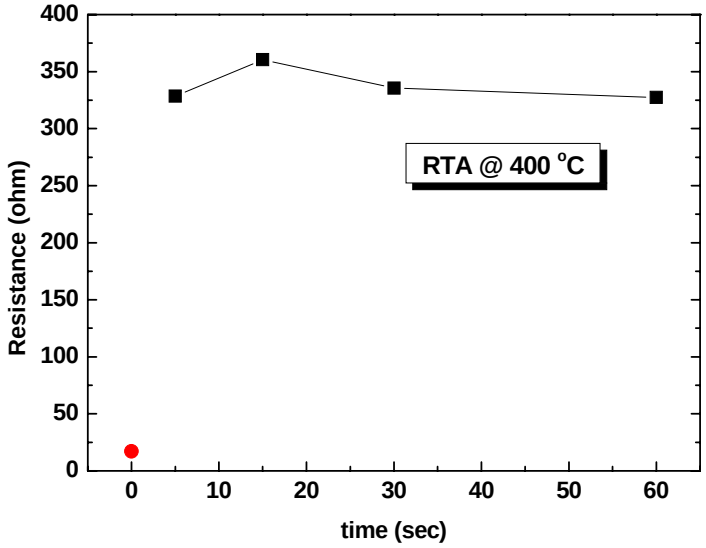


Fig.4.3 The experiment of counter dopingwas N-sub wafer to form silicide and implanted BF_2 then annealed at 400℃ 5/15/30/60s, respectively.

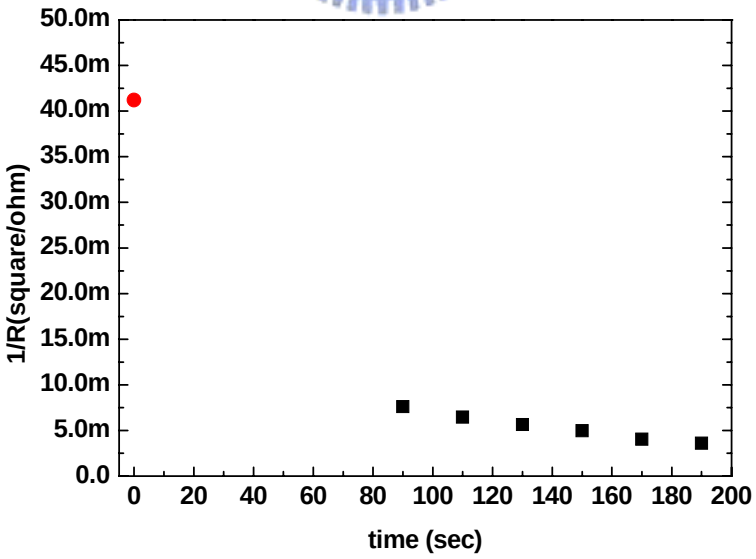


Fig.4.4 The relationship of doping Si-sub etching time versus reciprocal resistance.

	Implanted ion	1st RTA	2nd RTA
P substrate	**P^+/30 kev/5E15**	**350℃/30 sec**	**400 ~ 650℃ 60 sec**
N substrate	**BF_2^+/50 kev/5E15**	**350℃/30 sec**	**400 ~ 650℃ 60 sec**

Table.4.1 Recipes of IIS for I-V and C-V measured experiment

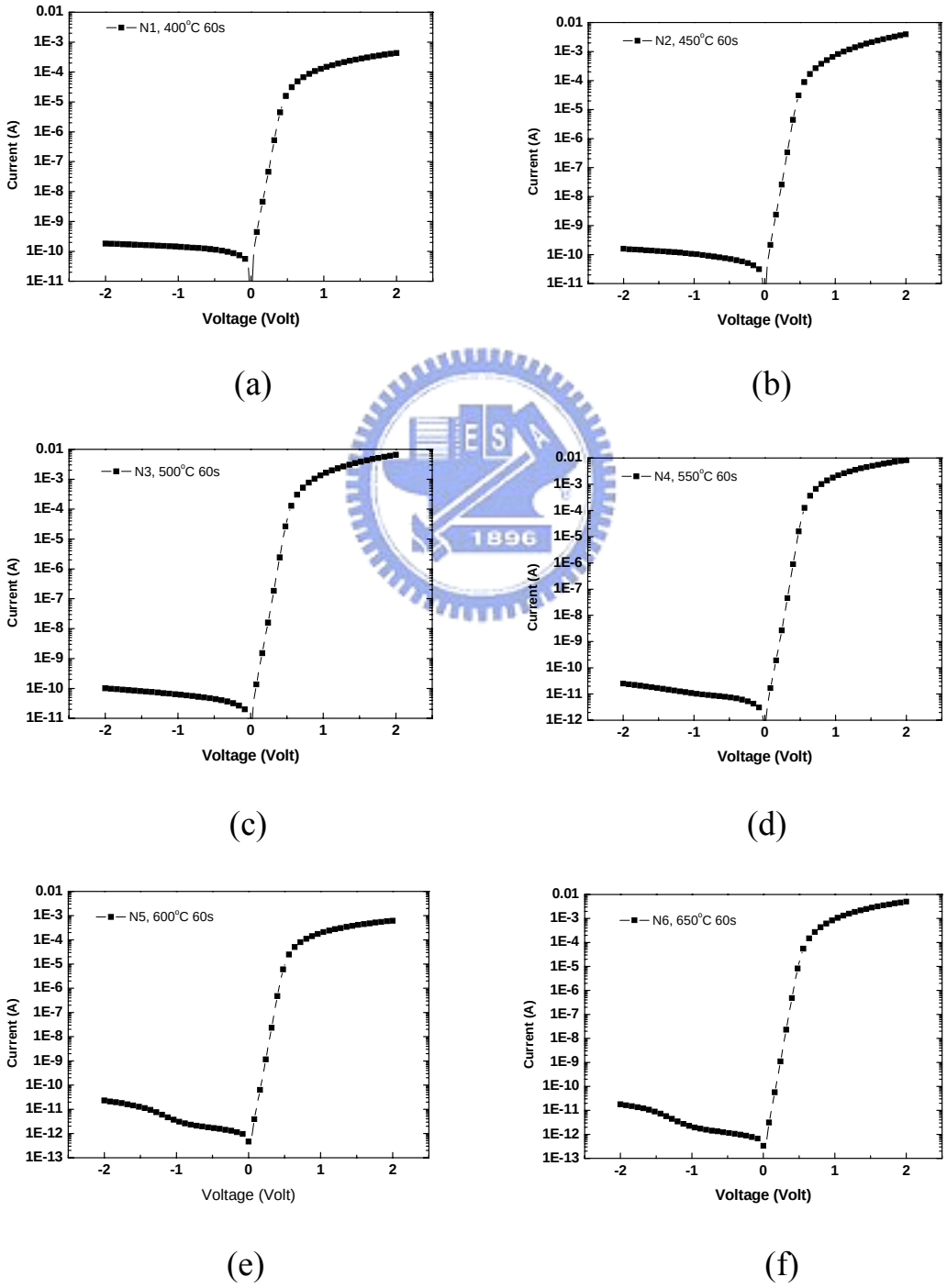


Fig.4.5 (a)~(f) I-V graphics for IIS N-sub samples

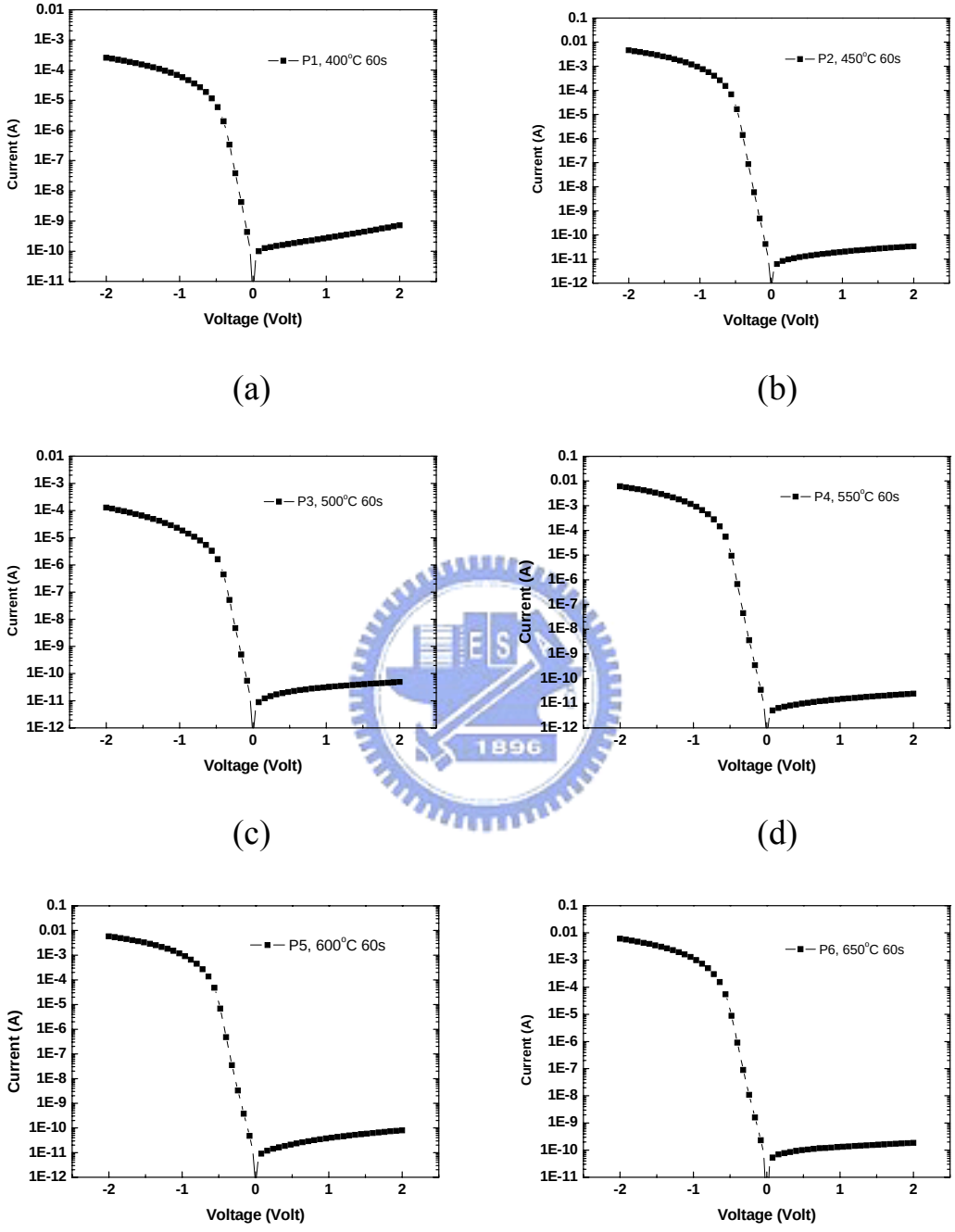
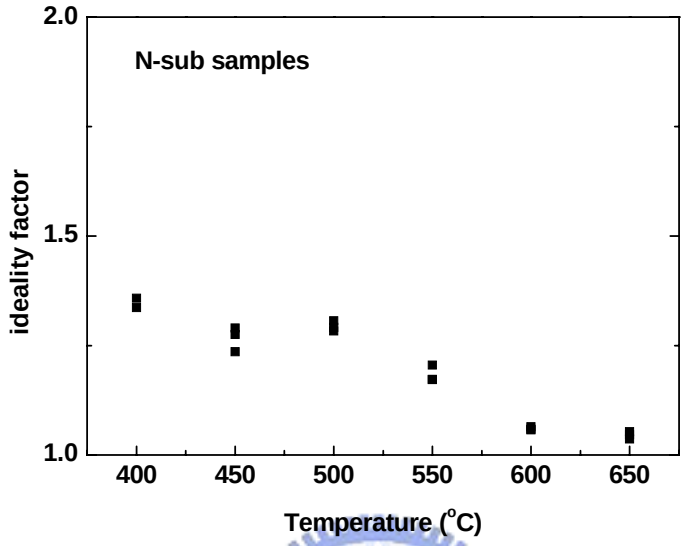
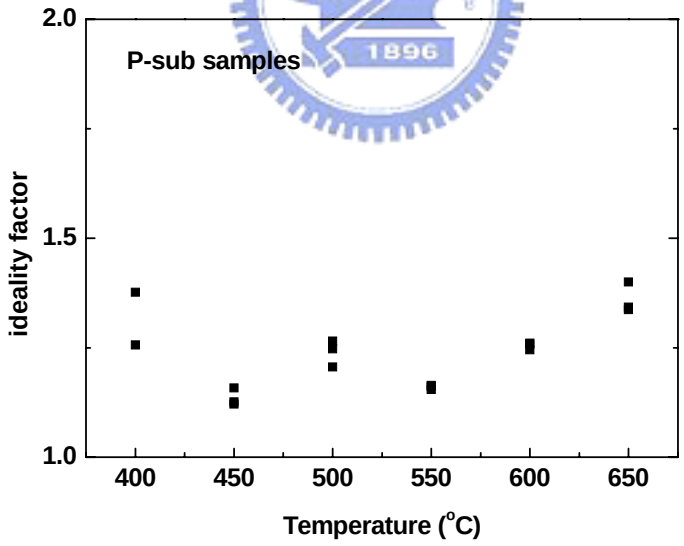


Fig.4.6 (a)~(f) I-V graphics for IIS P-sub samples

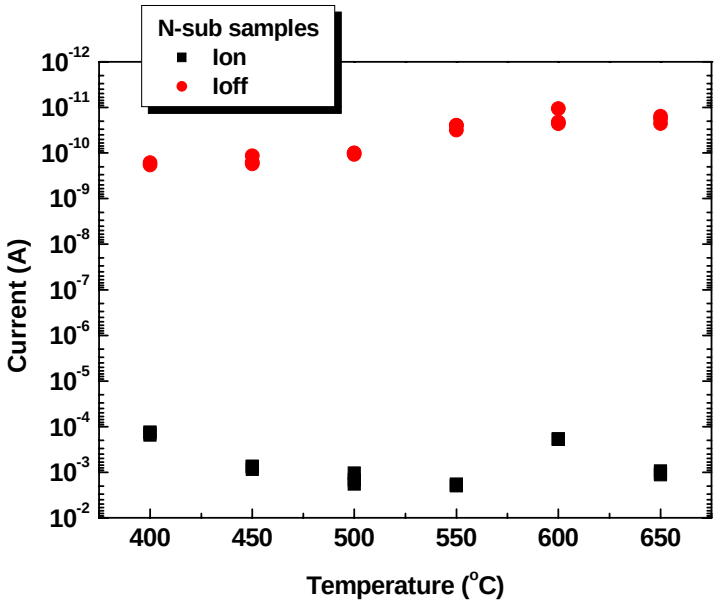


(a)

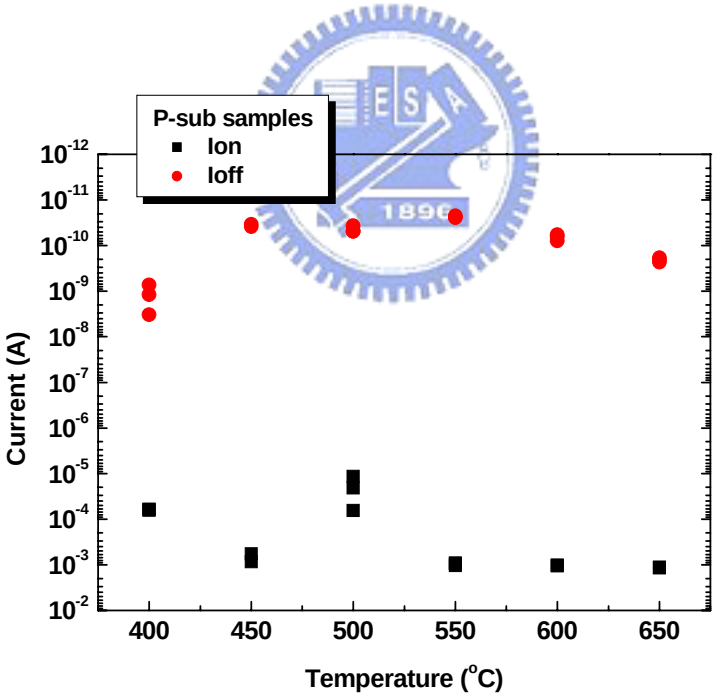


(b)

Fig.4.7 ideality factor (a)N-sub samples (b)P-sub samples



(a)



(b)

Fig.4.8 Ion-Ioff relation graphics(a)N-sub samples (b)P-sub samples (Ion : Forward bias at 1V and Ioff : Reverse bias at 2V)

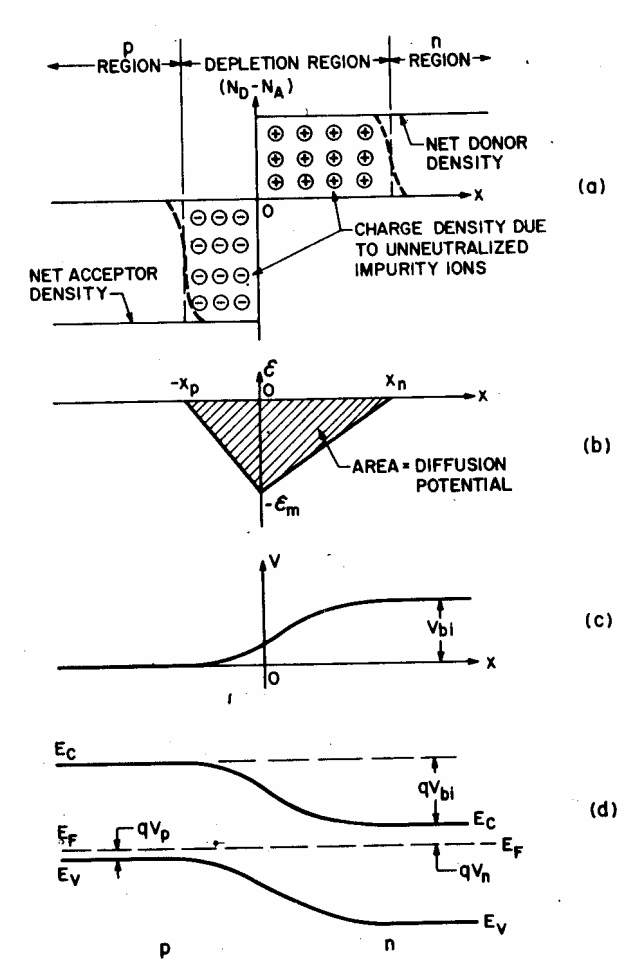


Fig.4.9 Abrupt p-n junction in thermal equilibrium. (a)Space-charge distribution. Dashed lines indicate corrections to depletion approximation. (b)Electric-field distribution. (c)Potential distribution where Vbi(Ψ_{bi}) is the built-in potential. (d)energy-band diagram.

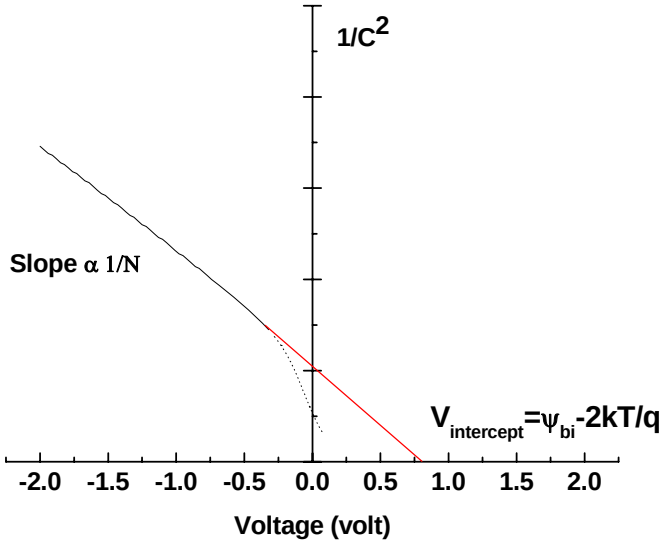


Fig.4.10 A $1/C^2$-V plot can yield the built-in potential and doping density N.

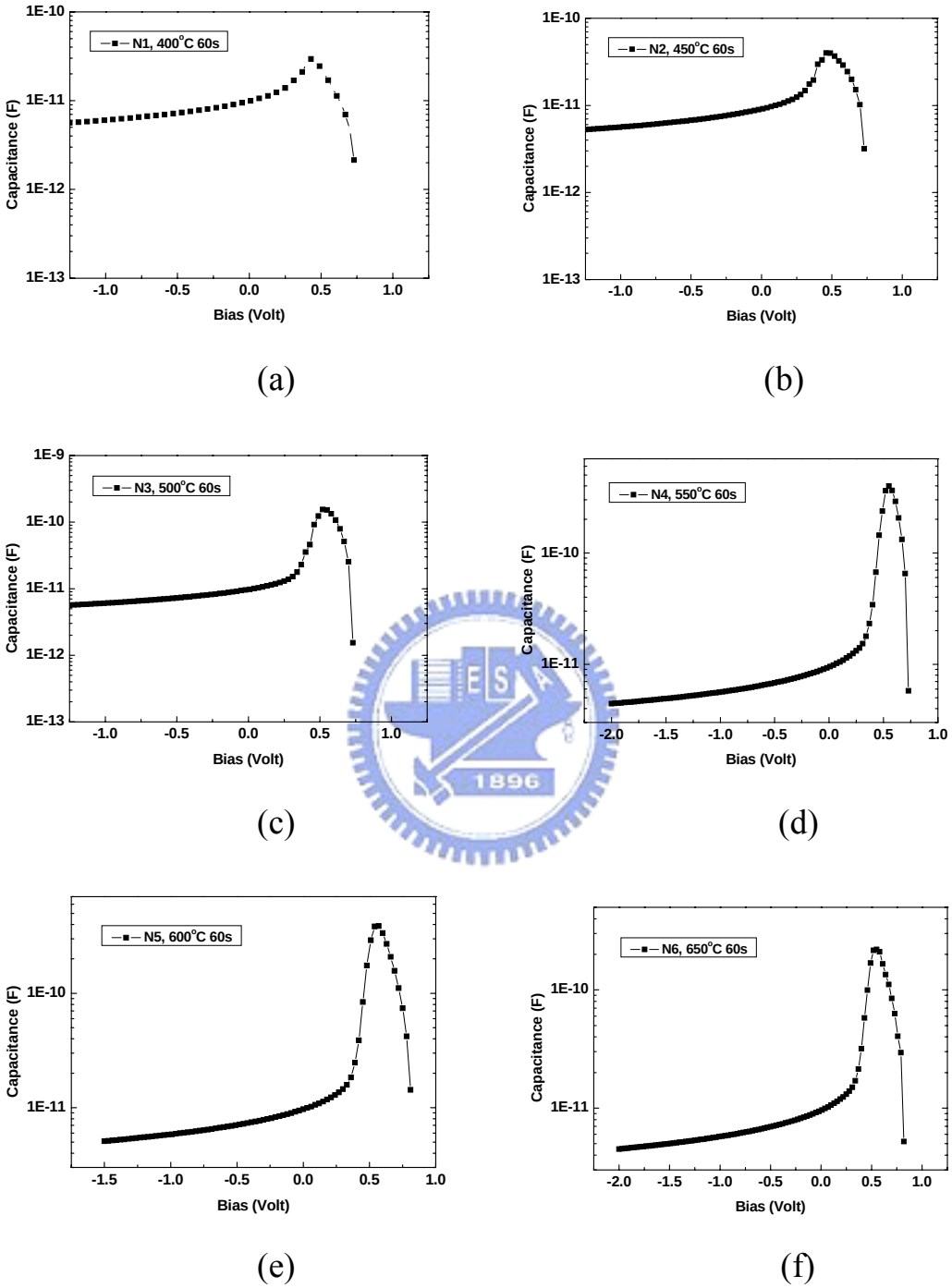


Fig.4.11 (a)~(f) C-V graphics for IIS N-sub samples

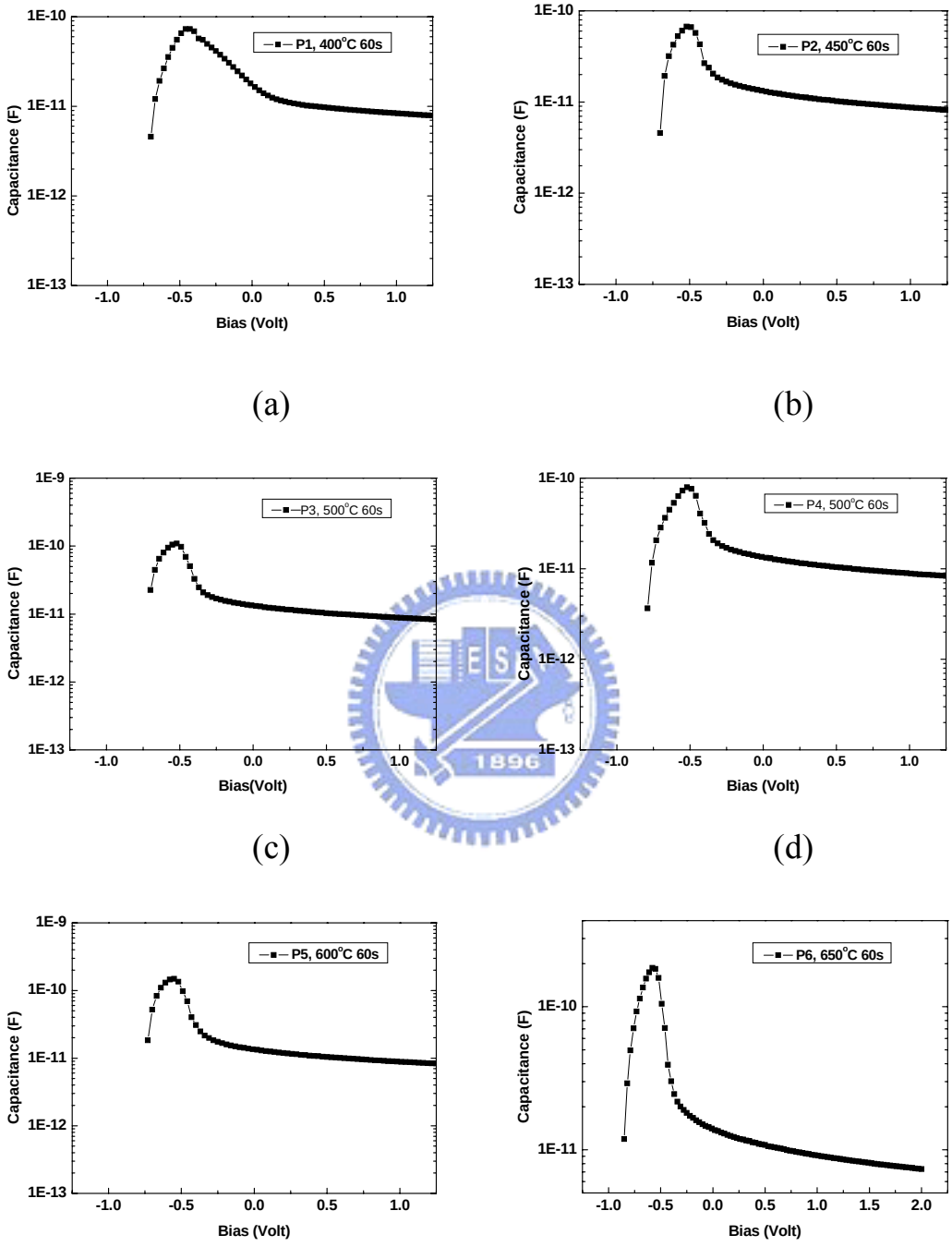
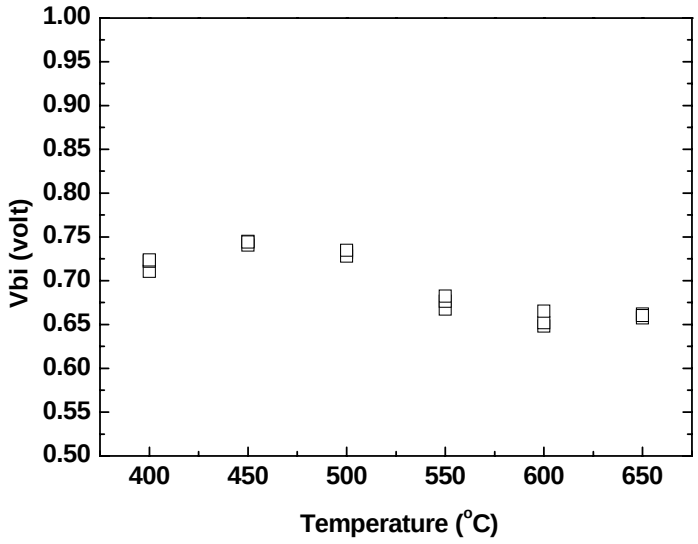
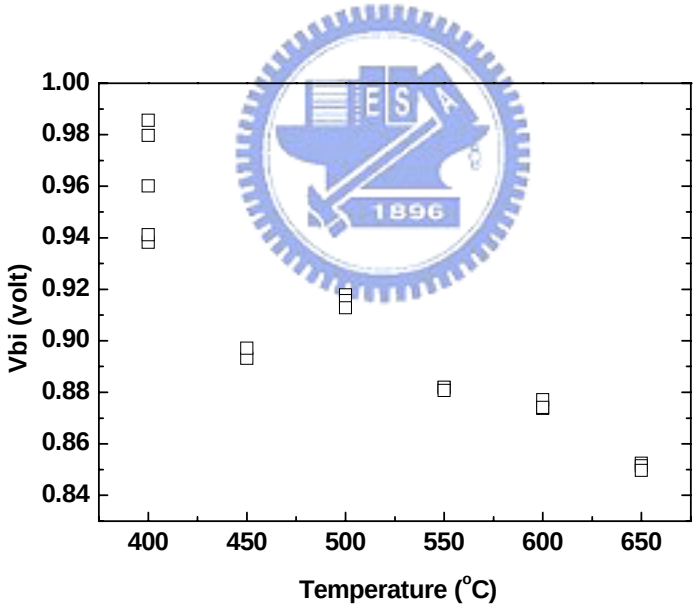


Fig.4.12 (a)~(f) C-V graphics for IIS P-sub samples

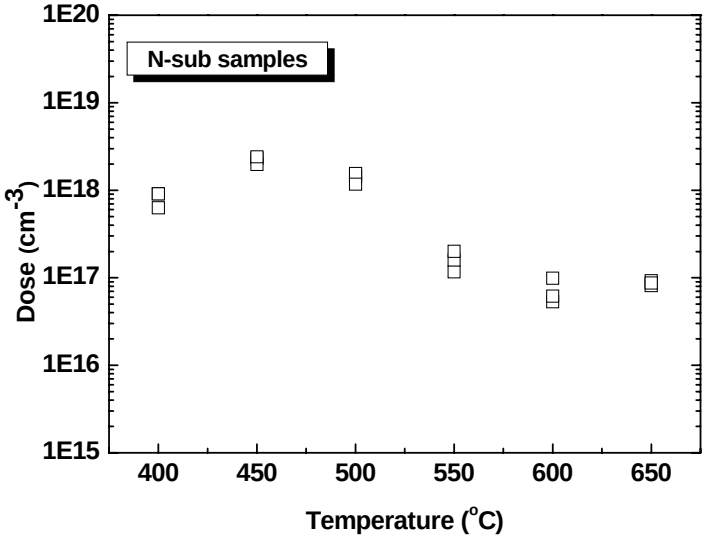


(a)

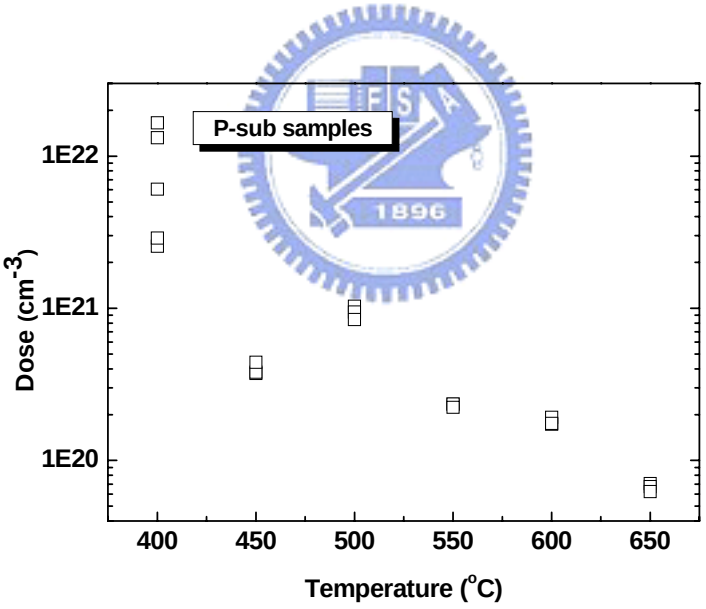


(b)

Fig.4.13 Ψ_{bi} (a)N-sub samples (b)P-sub samples

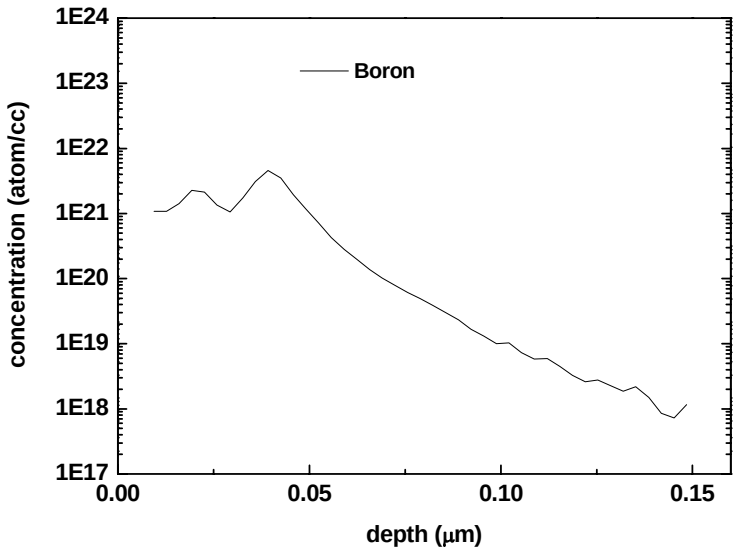


(a)

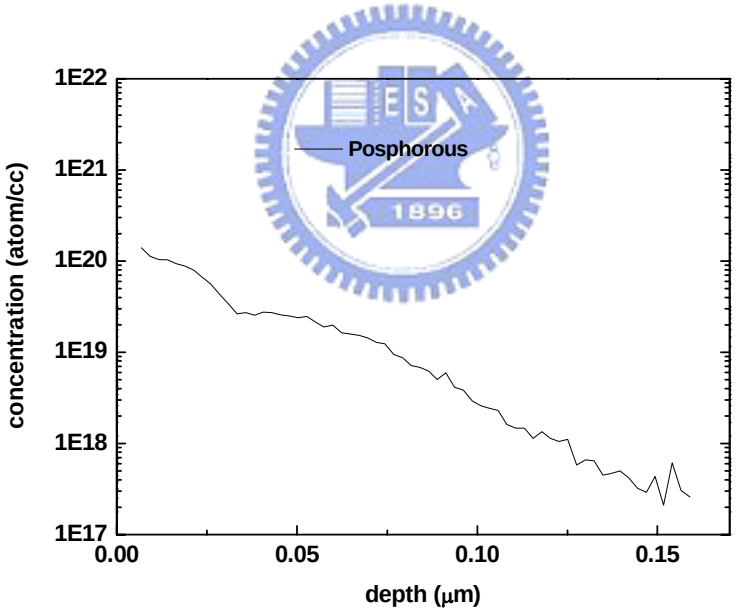


(b)

Fig.4.14 The dopant activation density of IIS at MS interface (a)Boron doping density for N-sub samples (b)Phosphorous doping density for P-sub samples



(a)



(b)

Fig.4.15 SIMS analysis for IIS samples 2nd RTA 650℃ 60s (a)Boron distribution of N-sub sample (b)Phosphorous distribution of P-sub sample

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（民國 94 年 9 月~民國 96 年 7 月）

碩士論文：形成矽化鎳時在矽化鎳與矽接面處離子活化相關研究

Research of Dopant Activation at the Interface between Nickel Silicide and Silicon during Nickel Silicide Formation