國 立 交 通 大 學

電子工程學系　電子研究所

碩　士　論　文

利用電流模式的 24-GHz 互補式金氧半傳送器前端電路

A 24-GHz CMOS Current-Mode Transmitter Front-End

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中華民國九十七年十月

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碩士論文

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摘要

具有高操作頻率高傳輸速率的通訊系統已被視為次世代通訊系統的主軸。在最近幾年,24-GHz 附近的頻帶中,已有許多頻帶如 24.05–24.25-GHz 的 ISM-band 及 22–29 GHz 被 FCC 釋出作為汽車雷達應用等用途。

此論文中介紹利用電流模式來實現一個操作在 24 GHz 的傳送器前端電路。此傳送器包含了升頻混波器以及功率放大器等電路並且使用了 0.13-μm CMOS 技術來設計並製造。藉由電流模式來實現升頻混波器以及功率放大器，使得大訊號操作的傳送器電路不會受限於 0.13-μm CMOS 的 1.2 V 供應電壓。

此傳送器前端電路包含了升頻混波器以及功率放大器等電路,已被模擬、實現於 1.05 mm^2 的晶片面積、以及量測。根據量測結果，此電路由於佈局時的錯誤、EM、製程以及溫度效應的考慮沒有詳盡，使得增益降至 11.5 dB。然而，從修改後的模擬結果與其它所發表的傳送器電路比較可知，此電路操作在較低的供應電壓下，仍有較好的線性度。因此，電流模式的電路非常適合用在低供應電壓的製程，尤其是高整合度、低成本的 CMOS 製程。

A 24-GHz CMOS Current-Mode Transmitter Front-End

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Abstract

In the next-generation wireless communication, high data rate transmission with a high operating frequency is expected to be realized. Over the past few years, the 24.05–24.25-GHz Industrial, Scientific, and Medical (ISM) band, 22–29 GHz band provided by Federal Communications Commission (FCC) for the operation of vehicular radar have been released.

In this thesis, a 24-GHz current-mode transmitter front-end is presented. The proposed transmitter which consists of an up-conversion mixer and a power amplifier is designed using 0.13-μm CMOS technology. By adopting the current-mode approach for design mixer and power amplifier, the large-signal operated transmitter circuit can be implemented under the typical supply voltage 1.2-V of 0.13-μm CMOS technology.

The proposed transmitter front-end, including a mixer and a power amplifier, is simulated, fabricated with a chip size of 1.05 mm^2, and measured. Because of the layout mistake, and the effects such as EM, corner and temperature which are not carefully

considered before fabrication, the measured power gain decreases to 11.5 dB. Comparing the results of the re-design transmitter with other proposed transmitter circuits, however, the current-mode transmitter can have better linearity under lower supply voltage. Therefore, current-mode circuits are suitable for low supply voltage technology, especially for high-integrated low-cost CMOS technology.

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于　風城交大

９７年　秋

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CHAPTER 1

INTRODUCTION

1.1 Background

Recently, the research on radio-frequency integrated circuits (RFICs) in higher frequencies have been accelerated since the frequency spectra below 10 GHz have gradually become crowded by massive requirements of data transmission from the modern wireless applications such as Bluetooth, wireless local area network (WLAN) and ultra-wideband (UWB), etc. Many researchers investigate RF transceiver front-end circuits in 24 GHz because higher operating frequency can provide more bandwidth. In addition, the 24.05–24.25-GHz Industrial, Scientific, and Medical (ISM) band [1], 22–29 GHz band provided by Federal Communications Commission (FCC) for the operation of vehicular radar [2]–[3], and the 24-GHz band plan as shown in Fig. 1.1 [4] are released.

In RF transmitter front-end, key components such as up-conversion mixers and power amplifiers (PAs) have been reported in many CMOS designs [5]–[7]. Nevertheless, in standard CMOS technologies, the active devices have poor inherent characteristics comparing to GaAs and SiGe, and the passive components such as planar inductors have higher losses from lossy substrate. These inherent characteristics seriously degrade the performance of the transmitter front-end circuits. Although the output power of the transmitter can be increased by utilizing multiple parallel transistors to implement power amplifiers [5], the power-added efficiency (PAE) remains the same in such a structure. To improve the PAE, several design techniques

have been proposed. By using the special structure of transmission line and additional algorithms, the PAE of a RF CMOS PA can be improved to around 10% [6]–[7].

Besides, the degraded voltage headroom is another challenge. This challenge causes by the decrease of the supply voltage with the scaling and improvement of CMOS technology. The reduction in the supply voltage of modern CMOS technologies originated by the aggressive downscaling of MOS devices has many prominent effects on the characteristics of monolithic CMOS circuits including high packing density, small device parasitic, high device speed, and low power consumption. Unlike supply voltage, the threshold voltage of MOS devices, however, is reduced at a rather slower pace, as shown in Fig. 1.2. As a result, reduced dynamic range and small effective gate-source voltage critically affect the performance of RF circuit implemented by CMOS technologies, particularly those that employ cascode structures.

It is well known that CMOS current-mode circuits have many intrinsic advantages over voltage-mode counterparts including wide bandwidth, tunable input impedances, high slew rates, less susceptible to power and ground fluctuations [8]–[9], low power dissipation, and the most important – lower supply voltage requirement. These characteristics make current-mode circuits particularly attractive for multi-Gbps data communications [10]–[11]. It is because the impedances of internal nodes in current-mode circuits are smaller than those in voltage-mode circuits and the voltage swings at internal nodes are resultant smaller. The signal information, instead of voltage swing in voltage-mode circuit, is mainly carried with the time-varying current signals. Consequently, current-mode circuits can be designed under small voltage headroom. With the above advantages, current-mode RF circuits are capable of

operating in low supply voltage and have great potential in the design of CMOS RF front-end in the advanced nanometer CMOS technologies.

1.2 Motivation

This research focuses on a 24-GHz transmitter front-end implemented by CMOS technology. This research also focuses on the novel current-mode approach for designing and implementing this 24-GHz transmitter circuit.

Because of the applications released in 24-GHz frequency range, many researchers are attracted to design high-performance and low-cost wireless applications in this frequency band with advanced CMOS technologies. As mentioned above, however, CMOS technology has limitation of low supply voltage. That is why traditional commercial implementation of wireless transceivers typically utilizes a mixture of technologies in order to implement a high-performance, completed system. Nevertheless, considering the cost and integration capability, CMOS technology is still the most suitable choice for designing RF circuits.

For CMOS technology, the difficulty is to implement a good-performed RF system with low supply voltage constraints. As the CMOS technology is scaled down to nanometer nodes, the supply voltage is gradually reduced to around or even below 1 V. The lower the supply voltage it becomes, the smaller voltage headroom it leaves and the poorer linearity it performs in the design of CMOS RF circuits. The required linearity for transmitter front-end circuit is much higher than that for receiver front-end because of its high power level and resultant large-signal operation is needed. However, low supply voltage constraint and resultant smaller voltage swing directly conflicts with the linearity requirements. That is one of the reasons that more and more

transmitter front-end circuits are implemented by other technologies such as GaAs but most of receiver circuits are still realized by CMOS technologies so far. Furthermore, for traditional topologies of RF circuit such as cascoded structures, the lower supply voltage for advanced CMOS technology in the future will not be capable to bias each transistor to a correct biasing point. Because of the advantages of current mode circuit, it has a chance to avoid the limitation of low supply voltage. Besides, when dealing with signal processing, it is easy to perform the function of summation by simply connecting the signal paths together without additional amplifiers. Thus power consumption can be further reduced. Therefore, a current-mode approach is adopted for designing RF transmitter front-end circuit.

1.3 Main Results and Thesis Organization

In this work, the mixer and power amplifier are designed by current-mode circuits. The up-conversion mixer is realized by current-operated self-switching mixer. A 2-stage current-mirror amplifier is proposed for the current-mode power amplifier. Besides, this is the first work in current-mode transmitter for 24-GHz applications. By using the current-mode approach instead of voltage-mode in RF circuit designs, the limitation of lower supply voltage of advanced CMOS technology can be overcome.

The post-sim results of the re-design circuit show that the impedance matching for IF, LO, and RF ports are –5.7, –13.3, and –13.7 dB, respectively. Power gain is 25.2 dB with the LO frequency of 23.9 GHz and IF frequency of 100 MHz. OP_{1dB} is 7.2 dBm and OIP3 is 15 dBm. Power consumption is 314.4 mW from 1.2 V power supply. The performance of stand-alone power amplifier shows it has 22-dB power

gain, 11.9-dBm IP_{1dB}, 22-dBm OIP3, 5.5% PAE at 1-dB compression point, and 22.9% peak PAE.

The measurement results show that the measured impedance matching for IF, LO, and RF ports are –1.4, –2.6, and –15.8 dB, respectively. The measured power gain is 11.5 dB with the LO frequency of 21.9 GHz and IF frequency of 100 MHz. Measured OP_{1dB} is –9.5 dBm and OIP3 is 4 dBm. The total power consumption is 238.4 mW from 1.2-V power supply. Comparing to other voltage-mode work [6][23][24], the proposed current-mode transmitter has better linearity and lower power dissipation under lower supply voltage. The experimental results and comparisons show that current-mode circuits are suitable for low supply voltage technology, especially for advanced CMOS technology.

The thesis is divided into five chapters. Chapter 1 introduces the background, motivation and main results of this research. Chapter 2 will discuss the concept of current-mode and the published current-operated RF front-end circuits.

The current-mode transmitter front-end of this thesis will be presented at Chapter 3. Design consideration of the transmitter front-end is discussed in Section 3.1. Then the power amplifier, up-conversion mixer, and the transmitter front-end design procedures are presented in Section 3.2.1, 3.2.2, and 3.2.3, respectively. Post-simulation results are shown in Section 3.3.

The chip microphotograph, measurement setup, experimental results, revised post simulation and re-design will be included in Chapter 4. Finally, the conclusions and future work will be presented in Chapter 5.

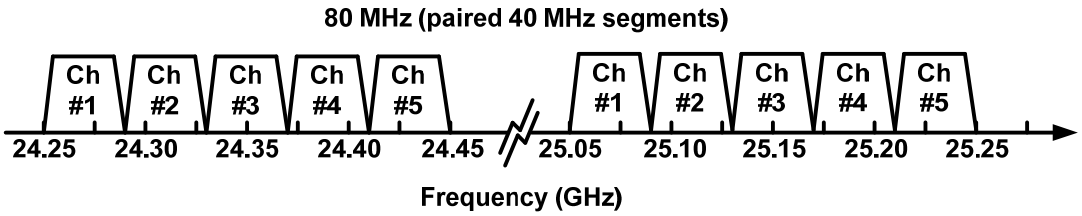


Fig. 1.1 24-GHz service band plan release by FCC.

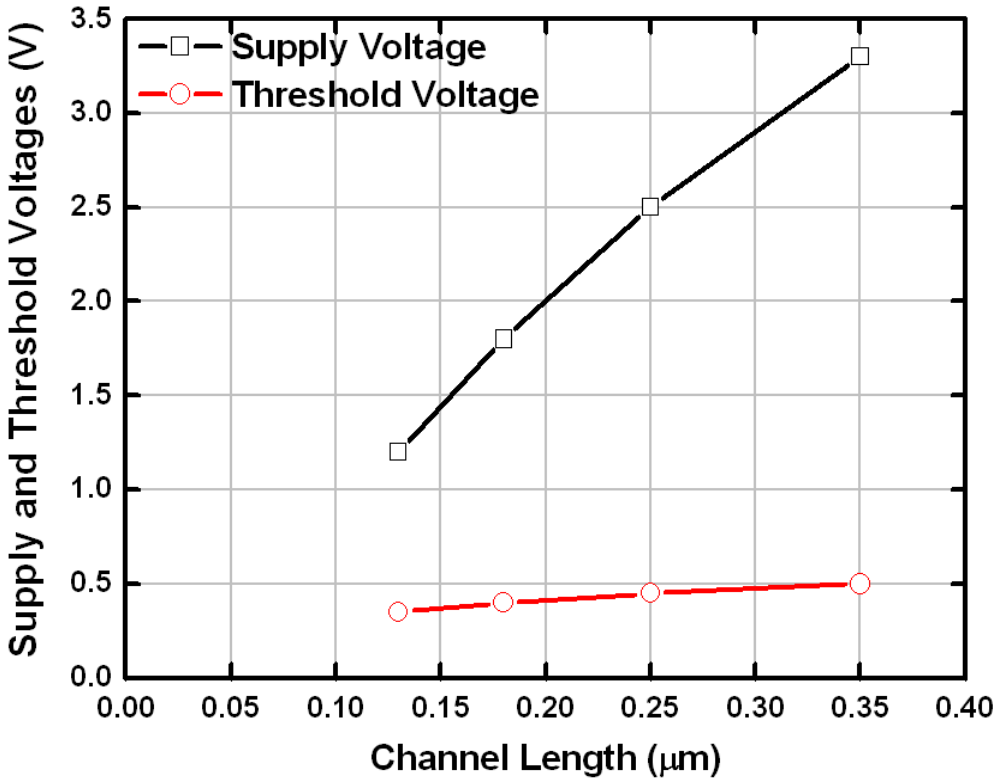


Fig. 1.2 Supply voltage (V_{DD}) and threshold voltage (V_{TH}) trends

CHAPTER 2

REVIEW ON CMOS CURRENT-MODE RF FRONT-END

2.1 CMOS Current-Mode RF Receiver Front-End

A current-mode receiver front-end is proposed in [12], as shown in Fig. 2.1–Fig. 2.2. The current-mode low-noise amplifier (LNA) is shown in Fig. 2.1. In order to adopt current-mode methodology, the first stage is a transconductance stage which makes an I-V conversion. The converted current signal then passes the current-mirror amplifier for second stage. Besides, this proposed LNA also adopts capacitive feedback match for input matching network in order to minimize the noise figure and maximize power gain simultaneously. The current-mode mixer shown in Fig. 2.2 is realized by current-operated self-switching mixer. This current-mode receiver has the advantages of low supply voltage and low power consumption.

Current-mode related down-conversion mixers are in [13]–[14]. These two mixers are proposed with a novel concept for realizing mixing function by current-mode operation. The schematic for general concept of these two mixers are given by Fig. 2.3. By using current inputs instead of voltage inputs, all series-connected transistors can be replaced by parallel-connected transistors in order to reduce the number of the cascode transistors. The detailed equations derived in [13] show that the differential output current ($i_{IF+} - i_{IF-}$) is proportional to the multiplication of i_{RF} and i_{LO}. Thus the mixing function can be done by this operation. Because of non-cascode structure, this current-mode mixer has the capability of low supply voltage operation.

Schematic shown in Fig. 2.4 is another current-mode receiver proposed in [15]. This proposed circuit modifies the receiver shown in Fig. 2.5 [16]. Since the circuit in Fig. 2.4 suffers from the problems of less degree of freedom for optimization and enough supply voltage is required for cascode structure. The modified current-mode receiver avoids these limitations by separating LNA from the tail current source in the mixer. Because only the RF current output from LNA to mixer, the bias currents for the LNA and the mixer are separated. The separated bias allows independent optimization for the noise in these two blocks. Besides, the headroom requirements are also relaxed in this circuit because the tail current source in the mixer does not govern the linearity.

Another current-mode receiver front-end including a LNA and a down-conversion mixer is shown in Fig. 2.6 [17]. This proposed current-mode LNA is consisted of a two-stage cascaded current mirror to amplify current signal. By adding diode-connected PMOS to reduce effective supply voltage shown in Fig. 2.7, this LNA can be operated correctly by lower than 1.2 V, the typical supply voltage for 0.13-μm CMOS technology. It means this proposed topology has potential for designed RF circuits by advanced CMOS technology in the future.

The concept of this proposed current-mode down-conversion mixer comes from square law. The conceptual block diagram of this proposed current-mode down-conversion mixer is depicted in Fig. 2.8. This mixer is composed of a current summing circuit, a current squaring circuit, and a band-pass filter (BPF). The RF input current signal

$$i_{lna} = I_{LNA}\cos\omega_{RF}t$$

from the current-mode LNA and the LO input current signal

$$i_{lo} = I_{LO}\cos\omega_{LO}t$$

from the off-chip LO signal generator are summed in advance through the current summing circuit. The summed current signal

$$i_{sum} = (i_{lna} + i_{lo}) = (I_{LNA}\cos\omega_{RF}t + I_{LO}\cos\omega_{LO}t)$$

are sent to the following current squaring circuit which results in the square components of i^2_{lna} and i^2_{lo} and the multiplication component $i_{lna} \times i_{lo}$. The multiplication component of two current input signals provides the function of double-sideband mixing. Through the double-sideband mixing, the received 24-GHz signal is converted to 5 GHz which is the lower sideband (LSB) and 43 GHz which is the upper sideband (USB) with the LO signal at 19 GHz. Following the current squaring circuit is the BPF which is capable of frequency selectivity. In this receiver design, the center frequency of the BPF is designed at 5 GHz so that the targeted LSB can be obtained and the unwanted USB can be attenuated. Fig. 2.9 shows the current summing circuit. Two common-gate transistors M_8 and M_9 operated in the saturation region function as current buffers. Due to the advantage of current-mode signal processing, the adding function can be realized by wired connection without any extra circuits. Thus the current signals $i_{out,lna}$ from LNA circuit and $i_{in,lo}$ from off-chip LO signal generator are summed by directly connecting the drains of M_8 and M_9 together. The conceptual circuit of other parts is implemented as shown in Fig. 2.10. A current-mirror structure is adopted so that the squaring function can be realized by the transistor's square law. The following band-pass filter is implemented by a LC tank that can filter out all frequency of signal except desired 5-GHz band. The detailed operational principles of the current summing circuit and the current squaring circuit are described in [17]. This current-mode receiver has the advantage of smaller power

dissipations and can be operated in low supply voltage. Besides, this current-mode receiver front-end also has better linearity performance.

According to these current-mode receiver front-end circuits illustrated above, no cascoded transistor is needed except the diode-connected transistors which are for reducing the effective supply voltage. Thus current-mode approach is a suitable solution for insufficient headroom problem caused by lower supply voltage of advanced technologies.

2.2 CMOS Current-Mode RF Transmitter Front-End

The transmitter front-end, o the other hand, consists of up-conversion mixer and power amplifier. Like the receiver front-end, the up-conversion mixer can also be realized by square-law or self-switching concept.

The current-mode up-conversion mixer proposed in [18] is the same concept of square-law as down-conversion mixer proposed in [17] but double-balance structure. Because of the advantage of current approach, the summing function is realized by directly wired connection. Thus a huge number of amplifiers or other extra circuits are preserved and the lower power consumption and smaller chip area are achieved.

Another up-conversion mixer at RF frequency of 2 GHz proposed in [19] adopts current-operated self-switching concept that the mixing function can be implemented under lower supply voltage. The detailed concept will be explained in chapter 3.

A current-mode power amplifier which is implemented by standard 0.13-μm CMOS technology is proposed in [20]. Because the specifications are different for preamplifiers and power amplifiers, this current-mode power amplifier is similar but

not completely the same with the preamplifier. First, two n-type current-mirror stages are adopted and current feedback is removed because of the PAs' high power gain requirement. Second, according to the required high output power, DC current of output stage cannot be reduced. Thus the low-power design proposed in [21] is not suitable for power amplifier. Besides, because of the serious parasitic by large transistors' size at high frequency, a neutralized method is implemented by current-mode power amplifier in [20]. This proposed current-mode power amplifier consists of two-stage cascaded current-mirror structure, two neutralized L_{GD} between gate-drain for both stages, and load-pull analysis for output transformation network (output matching network). This CMOS power amplifier can perform saturated output power as large as 20 dBm. Besides, it also shows that no cascode are necessary for implementing power amplifier by current-mode approach. Therefore, these current-mode circuits show that it is possible to implement CMOS transmitter front-end by current-mode approach.

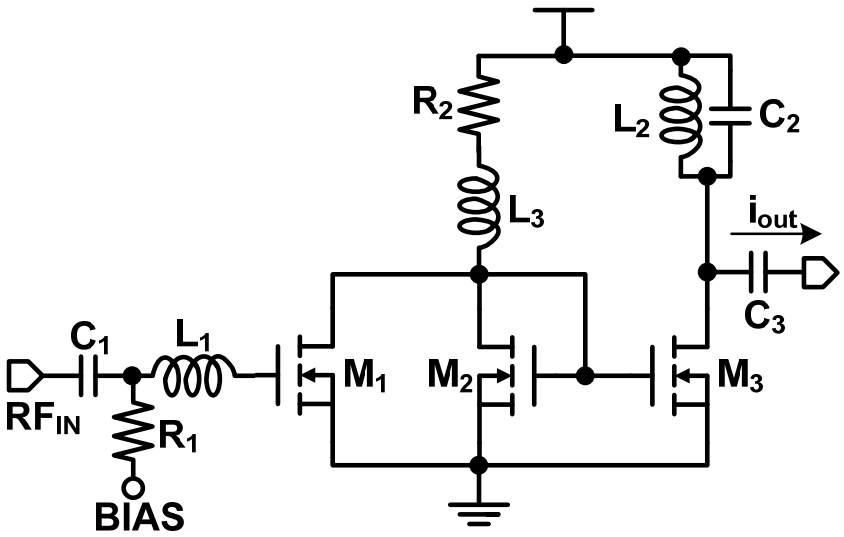


Fig. 2.1 Schematic for current-mode LNA in [12]

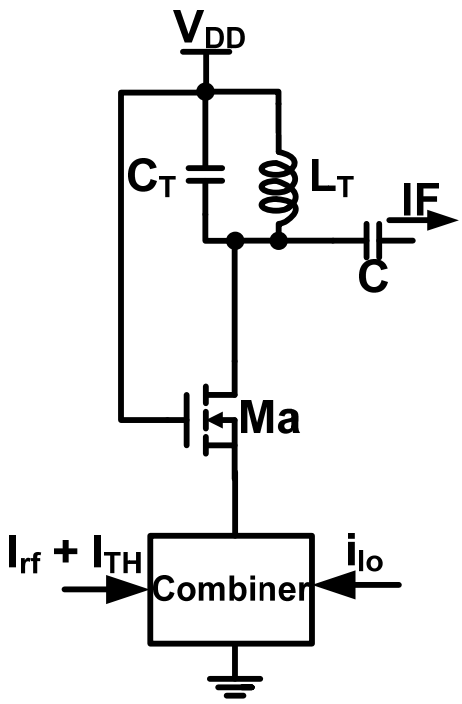


Fig. 2.2 Schematic for current-mode mixer in [12]

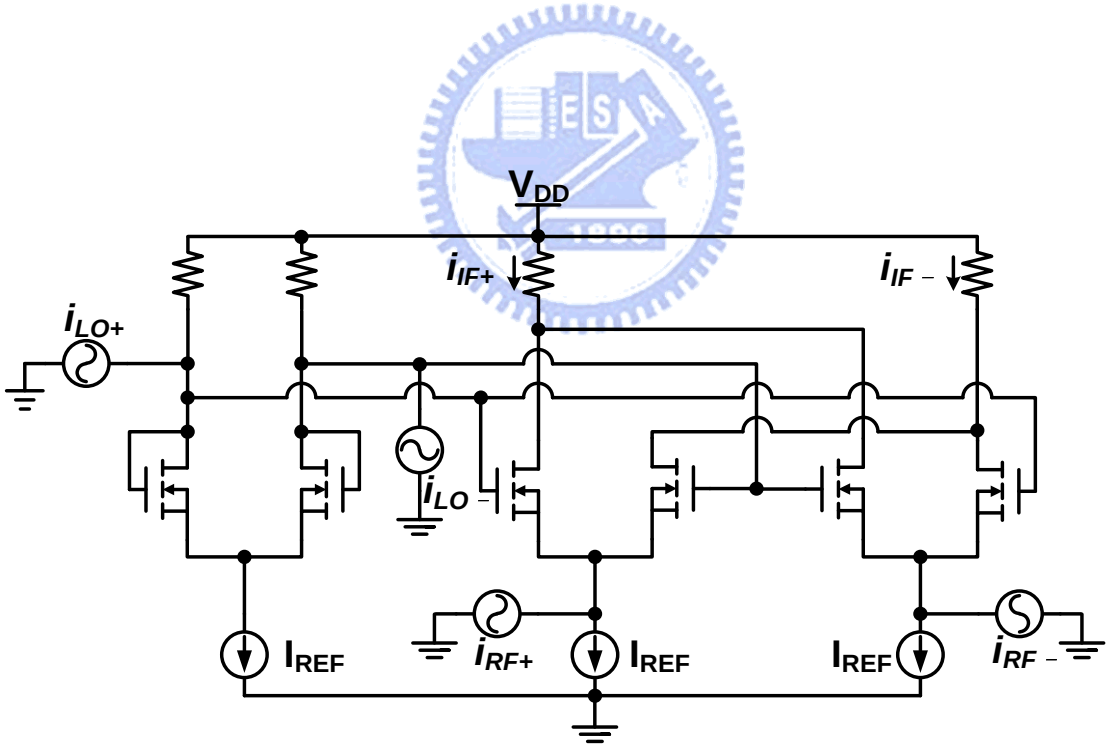


Fig. 2.3 Schematic for general concept in [13]–[14]

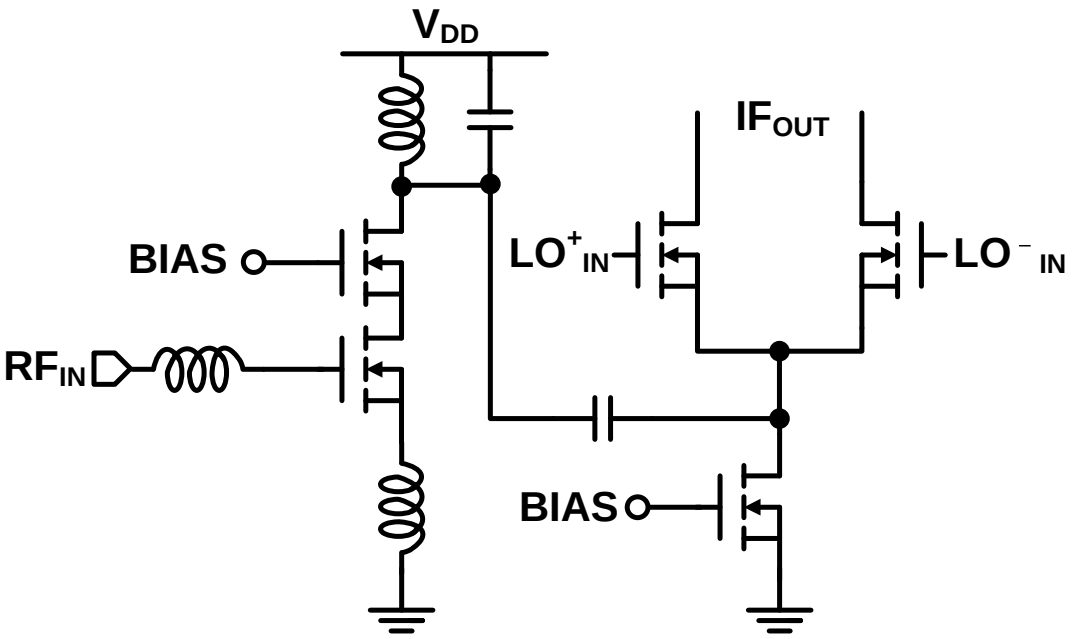


Fig. 2.4 Current-mode direct-conversion receiver proposed in [15]

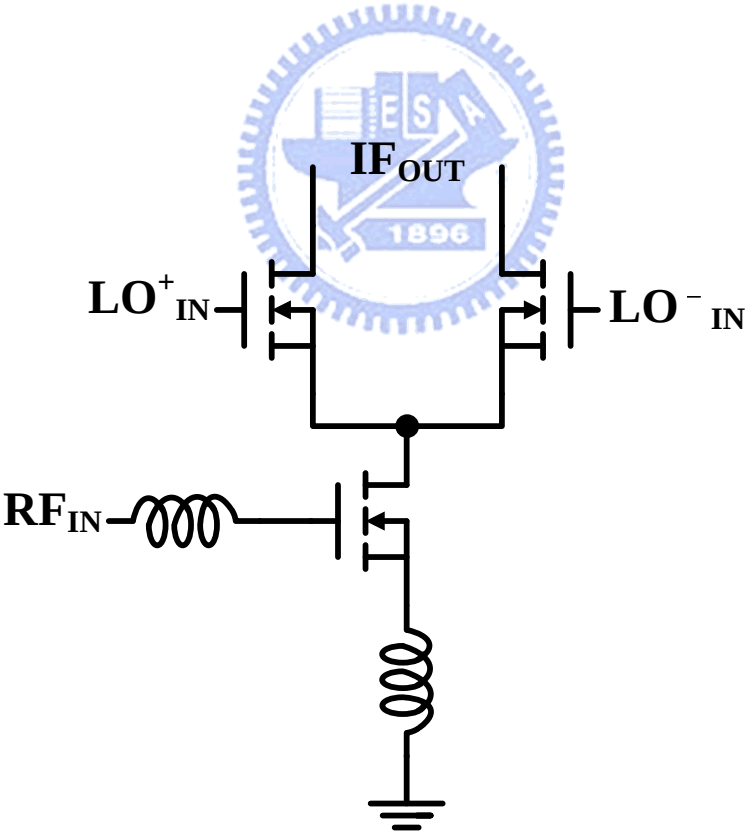


Fig. 2.5 Direct-conversion receiver proposed in [16]

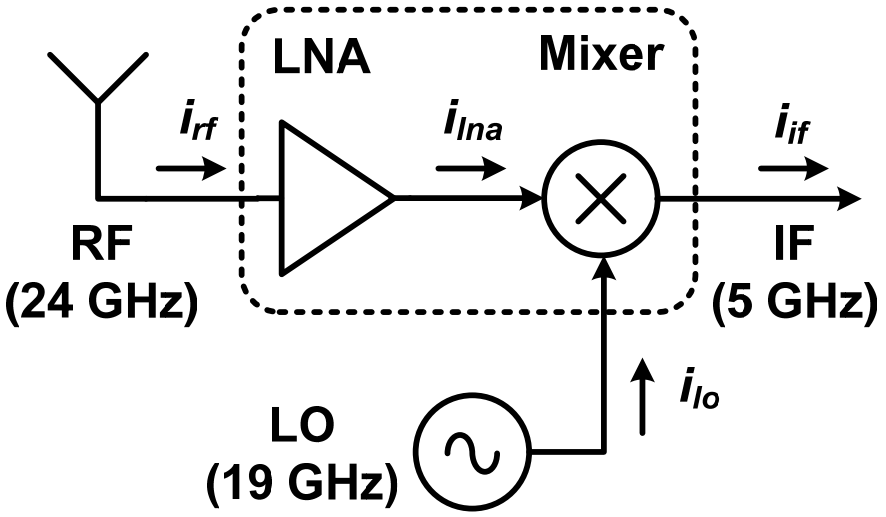


Fig. 2.6 Involved block diagram of proposed receiver front-end in [17]

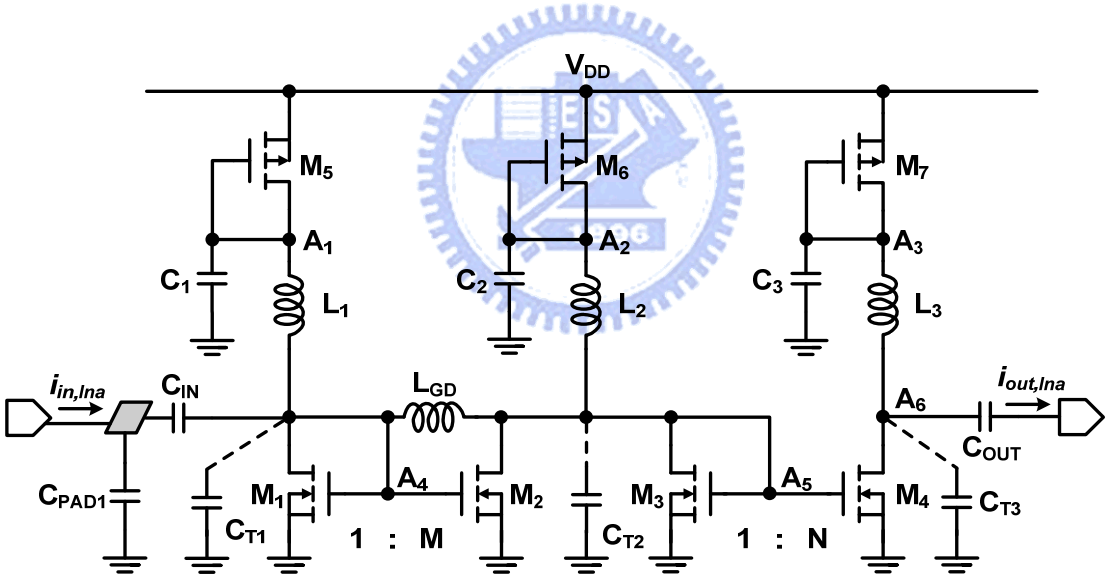


Fig. 2.7 Schematic of proposed LNA in [17]

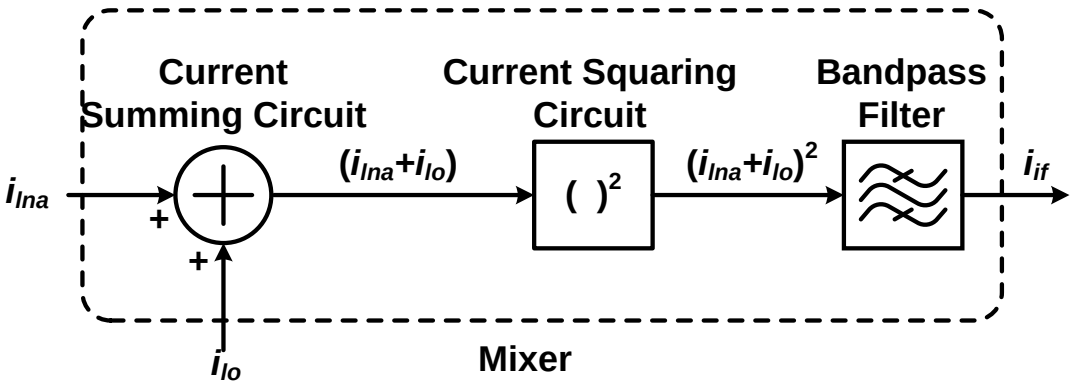


Fig. 2.8 Conceptual diagram of proposed down-conversion mixer in [17]

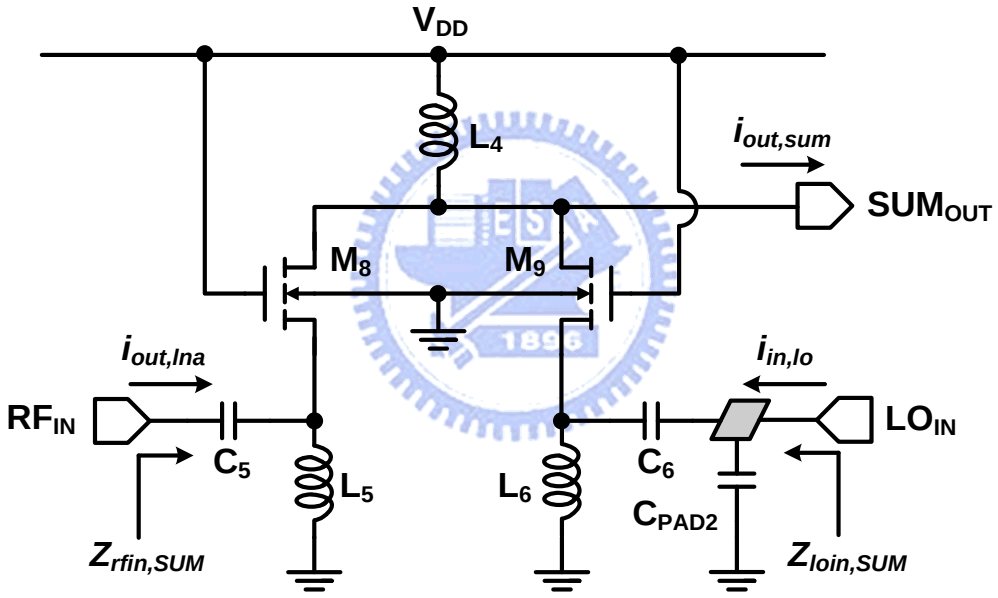


Fig. 2.9 Summing circuit of proposed down-conversion mixer in [17]

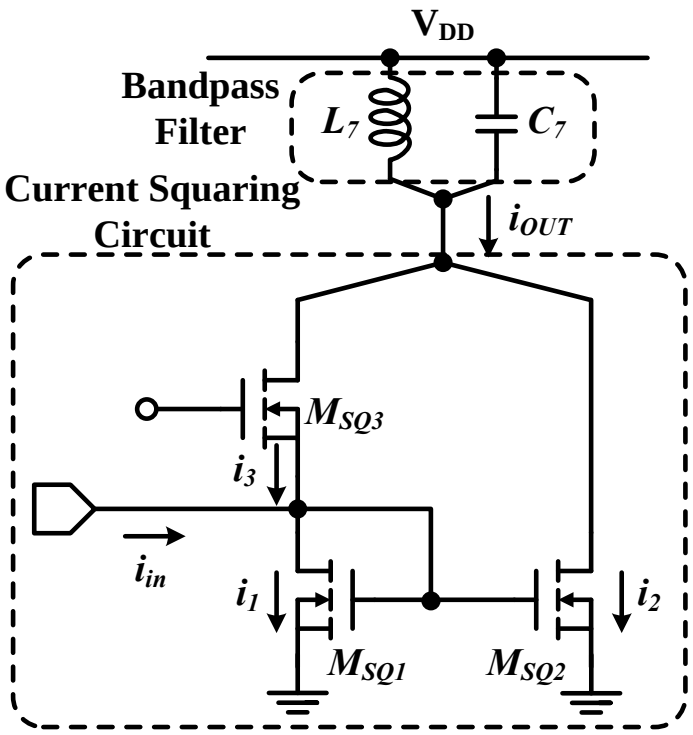


Fig. 2.10 Squaring circuit and band-pass filter of proposed down-conversion mixer in [17]

CHAPTER 3

CIRCUIT DESIGN AND SIMULATION RESULTS

3.1 Design Consideration

In this research, as shown in Fig. 3.1, a current-mode transmitter front-end included an up-conversion mixer and a power amplifier is realized with 0.13-μm CMOS technology. The designed mixer is implemented by the current-operated self-switching concept in order to compromise with the typical supply voltage of 1.2 V for standard 0.13-μm CMOS technology. The power amplifier which is also realized by current-mode concept consists of two stages to provide larger than 20-dB power gain. The 1st-stage of power amplifier amplifies the RF signal comes from designed mixer to drive the 2nd-stage of power amplifier. The 2nd-Stage is designed to have capability to provide enough signal swing that the required output power can be achieved. The specification of the designed transmitter front-end is to output more than 10-dBm output power at 24 GHz.

3.2 Circuit Design

3.2.1 Up-Conversion Mixer

The concept of the current-operated self-switching up-conversion mixer comes from [19]. The concept diagram of the designed mixer is shown in Fig. 3.2. Two current signals of IF and LO are summed together. The summed current signal is then passed through the self switch. This switch is called self switch because the summed current signal is not only its input but its control signal. Therefore, the switch is turned

on if the level of the summed current signal is larger than turn-on threshold current I_{TH} of the switch. Therefore, only the current signal larger than I_{TH} is appeared at the output of the switch. The fully balance structure which is composed of Path-A and Path-B is selected to eliminate non-ideal effect. Consequently, the mixing function can be achieved, and it can be applied to realize a differential up-conversion mixer.

The operation principle in terms of waveform for this designed mixer is illustrated in Fig. 3.3. According to the Fig. 3.2, the input signals are one low-frequency current signal IF (i_{if+} or i_{if-}) and one high-frequency current signal LO (i_{lo+} or i_{lo-}) in each path, as shown in Stage-I in Fig. 3.3. The adding signal ($i_{if+} + i_{lo+}$ or $i_{if-} - i_{lo-}$) shown in Stage-II is the linear combination of these two current signals. The output signals of self switch (i_{rf1} and i_{rf2}) are given by the Stage-III. Because of the characteristics of the self switch, the specific period of waveform that their amplitudes are larger than the I_{TH} will be remained and pass through the self switch. After linear combined these two signals, the mixing function can be done as shown in Stage-IV. Larger (Fig. 3.4) or smaller I_{TH} (Fig. 3.5) will produce worse performance. The extremely case is shown in Fig. 3.6. The switches always turn off or turn on and the resultant output is eliminated. Therefore, the biasing condition must be carefully considered in order to guarantee the I_{TH} level the same as in Fig. 3.3.

The detailed description is derived in (3.1)–(3.8). The Path-A and Path-B signals in Stage-I are shown in (3.1)–(3.2), respectively. In (3.1), A is the amplitude of the IF signal, ω_{IF} is the frequency of the IF signal, B is the amplitude of LO signal, and ω_{LO} is the frequency of the LO signal. The adding signals in Stage-II are (3.3)–(3.4). After the adding signals of IF and LO go through the self switch, the output signals of the switch, $i_{rf1}(t)$ and $i_{rf2}(t)$, can be regarded as the adding signals multiplied by repeating 1,0,1,0,... pulse with the LO signal cycles. After Fourier transforming, $i_{rf1}(t)$ in Stage-III can be

expressed as (3.5) where the IF and LO signals are given by (3.1). Similarly, signal $i_{rf2}(t)$ in path-B can be expressed by (3.6). Thus the adding signal $i_{rf}(t)$ (= $i_{rf1}(t)$ + $i_{rf2}(t)$) in Stage-IV can be expressed by (3.7), just like the mixing waveform $i_{rf}(t)$ illustrated in Fig. 3.3. After output LC tank, the output signal remains only the mixing term in (3.8). According to the equations above, it is obvious that this mixing concept can be implemented in current-mode operation.

$$i_{if+}(t) = A\sin\omega_{IF}t, \quad i_{lo+}(t) = B\sin\omega_{LO}t \tag{3.1}$$

$$i_{if-}(t) = A\sin(\omega_{IF}t+\pi), \quad i_{lo-}(t) = B\sin(\omega_{LO}t+\pi) \tag{3.2}$$

$$i_{if+}(t)+i_{lo+}(t) = A\sin\omega_{IF}t + B\sin\omega_{LO}t \tag{3.3}$$

$$i_{if-}(t)+i_{lo-}(t) = A\sin(\omega_{IF}t+\pi) + B\sin(\omega_{LO}t+\pi) \tag{3.4}$$

$$\begin{aligned} i_{rf1}(t) &= (A\sin\omega_{IF}t + B\sin\omega_{LO}t)\times\frac{2}{\pi}\left(\frac{\pi}{4}+\sin\omega_{LO}t+\frac{1}{3}\sin 3\omega_{LO}t+\text{H.O.T.}\right) \\ &= \frac{1}{2}(A\sin\omega_{IF}t + B\sin\omega_{LO}t)+\frac{2B}{\pi}\sin^2\omega_{LO}t+\frac{2A}{\pi}\sin\omega_{IF}t\sin\omega_{LO}t+\text{H.O.T.} \end{aligned} \tag{3.5}$$

$$\begin{aligned} i_{rf2}(t) &= \left[A\sin(\omega_{IF}t+\pi)+B\sin(\omega_{LO}t+\pi)\right] \\ &\quad\times\frac{2}{\pi}\left[\frac{\pi}{4}+\sin(\omega_{LO}t+\pi)+\frac{1}{3}\sin 3(\omega_{LO}t+\pi)+\text{H.O.T.}\right] \\ &= -\frac{1}{2}(A\sin\omega_{IF}t + B\sin\omega_{LO}t)+\frac{2B}{\pi}\sin^2\omega_{LO}t+\frac{2A}{\pi}\sin\omega_{IF}t\sin\omega_{LO}t+\text{H.O.T.} \end{aligned} \tag{3.6}$$

$$i_{rf}(t) = \frac{4A}{\pi}\sin\omega_{IF}t\sin\omega_{LO}t+\frac{4B}{\pi}\sin^2\omega_{LO}t+\text{H.O.T.} \tag{3.7}$$

$$\frac{4A}{\pi}\sin\omega_{IF}t\sin\omega_{LO}t \tag{3.8}$$

The circuit realization is given by Fig. 3.7–3.9. I-V transfer and current-adding circuits are shown in Fig. 3.7. I-V transfer-function for IF and LO signals are implemented by PMOS (M_1) and NMOS (M_2), respectively. Because of the current-mode operation, these two current signals are added at the drain terminal of M_1 and M_2 (node A_1) in a wired-OR manner without any extra circuits. Comparing to two common-source NMOS, the DC current can be re-used and resultant power consumption of whole transmitter front-end can be lower. The self-switching function is realized by M_3 in Fig. 3.8, where the $i_{if+}(t)$ and $i_{lo+}(t)$ are given in (3.1) and I_{IFB}/I_{LOB} is the DC current of IF/LO.

The source terminal of the transistor M_3 is also connected to this terminal. I_{IFB} and I_{LOB} are set to $I_{IFB} = -I_{LOB}$ so that M_3 is turned off when $i_{if+}(t)$ and $i_{lo+}(t)$ are not applied. This condition means $I_{TH} = 0$ in Fig. 3.2 and Fig. 3.3. Furthermore, M_3 is turned on when IF and LO signals are input and $i_{if+}(t) + i_{lo+}(t) > 0$. This indicated that the transistor M_3 detects the polarity of $i_{if+}(t) + i_{lo+}(t)$ and is switched on by the polarity. In this way, the current adding and self-switching circuits is realized using current-mode operations.

Because of the characteristics of self-switching transistor M_3, any drifted I_{TH} level result in the V_{GS} of switch transistor M_3 will affect its characteristic and degrade the performance of this mixer as shown in Fig. 3.4–Fig. 3.6. Thus some extra circuits are adopted in order to fix the biasing point of the internal node A_1. The negative feedback is realized by OPAMP, as shown in Fig. 3.9.

The schematic of the designed mixer is shown in Fig. 3.10. The IF and LO frequency are 100 MHz and 23.9 GHz, respectively, in this designed mixer. $M_{1,4}$ and $M_{2,5}$ are operated in the saturation region and functioned as transconductors that transform the voltage signals of IF and LO into current signals. For maximizing

conversion gain, "$V_{DD}/2$" is chosen for V_{A1} and V_{A2}, the DC bias of the internal nodes A_1 and A_2. The gate biasing points for these four transconductors are chosen by the optimal linearity for each of them. The gate-to-source voltage of M_3 and M_6, V_{GS3} and V_{GS6}, are designed to equal to their respective threshold voltage V_{TH3} and V_{TH6} such that the characteristic of self switch can be achieved. Because the different value of V_{GS}, no matter higher or lower, will reduce amplitude of output RF signal, the V_{GS} of M_3 and M_6 must be fixed. The DC biases V_{B1} and V_{B2} are carefully designed in order to achieve the condition of $V_{GS}=V_{TH}$. Besides, two operational amplifiers (OPAMPs) with the configuration of differential input single-ended output shown in Fig. 3.11 are used to implement negative feedback loops so that the DC bias of the internal nodes V_{A1} and V_{A2} are virtual short to the biasing voltage V_{REF}. Therefore, the DC biasing points of the sources of M_3 and M_6 can be fixed, and the voltage of V_{REF} is chosen as $V_{REF}=V_{B2}-V_{TH3,6}$. The schematic and the results for simulating this feedback loop are shown in Fig. 3.12 and Fig. 3.13, respectively. According to Fig. 3.13, the phase margin of this loop is large than 50^o.

For transconductors $M_{1,4}$ and $M_{2,5}$, larger size of them can provide larger transconductance. In RF systems, however, serious parasitic effect comes up with large transistor's size. For low-IF or direct conversion receiver front-end circuits, it can be resonated out simultaneously by only one inductor because the frequency of input signals RF and LO are almost the same. Unfortunately, this situation will never occur in transmitter front-end unless the impractical specification that IF and LO frequencies are exactly equal to half of the RF frequency. That is, the IF and LO frequencies are too different to simultaneously resonate out the parasitic capacitance at nodes A_1 and A_2 simultaneously. Therefore, large transistor provides large transconductance, but a huge and un-removable parasitic capacitance is also donated to the circuit. Because

any parasitic capacitance can be regarded as an equivalent short path for high frequency, it may degrade RF signal by leakage RF signal to ground. The optimized sizes of these four transistors are determined by largest amplitude of current signals after I-V conversion.

In order to provide lower impedance that the adding signal of IF and LO can easily flow into self-switching circuit, the dimension of self-switching transistors M_3 and M_6 are designed as large as possible. However, just like the transconductance transistors, these self-switching transistors are suffered from the same situation that large size can provide lower impedance for adding signal but serious and un-removable parasitic problem at their source terminals. The sizes of these two transistors are optimized by the largest current amplitude of RF signal at output node of mixer.

The LO input matching network is composed of R_1, R_2, $XFMR_2$, C_3, and the parasitic capacitance of the LO input pad C_{PAD3}. Input matching network for 100-MHz IF signal is not integrated on chip. Instead, as shown in Fig. 3.14, two off-chip biased-tees (C_1, C_2, L_1 and L_2) and an off-chip transformer ($XFMR_1$) are required during measurement. The inductor L_3 and parasitic capacitance at output node, drain terminals of M_3 and M_6, are implemented for output LC tank that functions as a filter and only passes desired RF signal to power amplifier.

The voltage headroom required at the nodes A_1 and A_2 is "$2\times V_{DSAT} +\Delta V$", which ΔV is signal voltage swing. It is the same as the nodes B_1 and B_2 in conventional Gilbert mixer shown in Fig. 3.15. In Gilbert mixer, however, the output node is high impedance node and directly proportional to its conversion gain. Thus the voltage swing at the output node of Gilbert mixer must be large. In designed current-operated self-switching mixer, the node A_1 and A_2 are low impedance nodes because that the

sizes of M_3 and M_6 are large enough so that the current signal can pass though them. Because the signal information is mainly carried by the current swing, the voltage swing is much smaller that that in Gilbert mixer. That is, the required ΔV is much smaller than that in Gilbert mixer. Comparing with the conventional Gilbert mixer, consequently, the designed current-operated self-switching mixer has better linearity if the supply voltage is the same, or supply voltage can be reduced if the linearity specification is the same. Thus the self-switching mixer in current-mode approach has great potential to operate in low supply voltage in advanced nanometer CMOS technology.

3.2.2 Power Amplifier

As to power amplifier, the most critical node is its output because high output power and resultant large voltage and current swing are required. Large output power which implies to large DC bias means the reliability such as metal current density must be considered. Besides, large voltage and current swing which implies to large-signal operation must be considered instead of small-signal operation. Therefore, for RF systems' power amplifiers, the output impedance transformation networks (output matching networks) are always implemented by load-line or load-pull analysis instead of traditional conjugate match.

The traditional conjugate match can provide maximal power transfer only under the condition of no current and voltage swing limitation. It is always true for small-signal operation. That is why most of RF systems, such as receiver, adopt traditional conjugate match for their matching networks. However, transmitter front-end, especially for output of power amplifier, is large-signal operation. It is because that power amplifiers always produce high output power, the current or voltage swing always reaches the limitation of its supply. Therefore, instead of

traditional conjugate match, the output matching networks of power amplifiers are usually determined by two methods – load-line or load-pull.

A quantitative description is given by Fig. 3.16 for the difference of optimal load if the voltage and current swing are limited. For traditional conjugate match, the load resistance R_L is chosen to equal to R_S. If the voltage and current swing are limited, however, it is clear that the "V_{MAX}/I_{MAX}" load resistance have maximal output power than any other load resistance.

The load-line analysis on a common-source transistor I-V curve is illustrated in Fig. 3.17. The load-line shown by black color is the optimal load resistance determined by load-line analysis. It is obvious that the load-line has maximal output power under this voltage and current swing limitation. Any load resistance which is smaller than the optimal resistance will have the same current swing but smaller voltage swing and resultant smaller output power. Any load resistance which is larger than the optimal resistance will have the same voltage swing but smaller current swing and resultant smaller output power. The hand-calculated procedure for load-line analysis can be accessed through (3.9)–(3.10). The transistors' sizes (in terms of DC current) and optimal load resistance can be calculated as long as the required output power is given.

$$P_{OUT,MAX} = \frac{1}{2}\left(V_{DC} - V_{knee}\right) I_{DC} \tag{3.9}$$

$$R_{L,OPT} = \frac{V_{DC} - V_{knee}}{I_{DC}} \tag{3.10}$$

From the figures and equations of load-line analysis above, it is not difficult to notice that load-line analysis can be used for quickly determining optimal load resistance, but not reactance. Because load-line analysis bases on I-V curve, the junction parasitic effect is exclusive. That is, only the real part of the load impedance (Z_L) can be determined by this analysis, the effect of imaginary part cause by the parasitic effect of the circuit will be completely neglected. Unfortunately, the parasitic effect induce lose for high frequency signal. Besides, the larger size of the transistor it is, the parasitic effect is worse and cannot be ignored.

Comparing to load-line, load-pull analysis can be used to determine the load impedance Z_L, both real and imaginary part, of power amplifiers. The load-pull analysis, shortly, is to sweep Z_L to see how PAs perform. The analysis procedure is： First, add a load tuner at the output of power amplifier. Second, sweep the value of load tuner (Z_L) to see the difference of output power (P_{OUT}) and PAE. Because of each point on Smith chart is a reflection coefficient, and the reflection coefficient and impedance are one-to-one mapping for 50-ohm characteristic impedance, the swept data can be used to construct constant P_{OUT} and constant PAE contours. Third, choose one reflection coefficient (load impedance) on Smith chart by trade-off between constant P_{OUT} and constant PAE contours. Using load-pull analysis to determine Z_L has several advantages. Because the constant P_{OUT} and PAE contours are drawn on the same Smith chart, it is easy and obvious to trade-off between them. Besides, because of the one-to-one mapping characteristic, both real and imaginary part of Z_L can be determined as soon as the trade-off point has been chosen.

Another difficulty for designing power amplifier is the parasitic effect. Because high output power is required, a cumbersome size of each transistor and resultant seriously parasitic effect are inevitable. Large parasitic capacitance C_{GD} provides a

short path between input and output at high frequency in common-source amplifier. Therefore, a resonated inductor (L_{RES}) must be used between these two nodes shown in Fig. 3.18 for resonating parasitic capacitance C_{GD} and improving reverse isolation.

The small-signal model for a common-source amplifier is shown in Fig. 3.19. Because the S-parameter S12 is desired, input phasor E_2 is placed at port 2 (drain).

According to the definition of S12 shown in (3.11) [22], the term "V_{O1}/E_2" can be expressed by (3.12). Although (3.11) and (3.12) can show the effect for value of Z_X, it is not obvious. In order to further simplify this equation, the matched condition at output node is assumed. This condition is always true for RF systems. The S22 of common-source amplifier can be calculated through (3.13) to (3.14). α and β are the substituted variables for the numerator and denominator in (3.13), respectively. Under the matched condition, the condition "$Z_{O2}\beta=\alpha$" can be derived as shown in (3.15). Thus (3.12) can be further simplified by this derived condition and the final result for S12 of common-source amplifier is shown in (3.16).

For a traditional common-source amplifier, Z_X is "$1/j\omega C_{GD}$" and S12 will become (3.17). Thus larger the transistor size it is, larger the value of parasitic capacitance C_{GD} it has and worse the reverse isolation it becomes. For extremely case of infinitely large C_{GD} value, the S12 will become the equation shown in (3.18) and equal to 1 (or 0 dB) in general for RF circuits (for $Z_{O1} = Z_{O2} = Z_O = 50$ ohm, general case in RF circuits). 0-dB S12 means this circuit has no any reverse isolation or the equivalent circuit for this two-port network is short circuit. It is reasonable because the infinitely large C_{GD} provides a zero-impedance short path between port-1 and port-2.

If the resonated inductor L_{RES} is adopted and placed between gate-drain, the impedance Z_X in (3.16) will become (3.19). Thus S12 can be zero as long as the

condition in (3.20) is achieved. That is the reason why a resonated inductor is always adopted for large-sized common-source amplifier.

$$S12 \equiv 2 \times \frac{\sqrt{Z_{O2}}}{\sqrt{Z_{O1}}} \times \frac{V_{O1}}{E_2} \tag{3.11}$$

$$\frac{V_{O1}}{E_2} = \frac{Z_{O1}Z_{GS}Z_{DS}}{Z_{O2} \times \left[\left(g_m Z_{O1} Z_{GS} Z_{DS} \right) + \left(Z_X Z_{O1} + Z_X Z_{GS} + Z_{O1} Z_{GS} \right) + \left(Z_{O1} Z_{DS} + Z_{GS} Z_{DS} \right) \right] + Z_{DS} \times \left(Z_X Z_{O1} + Z_X Z_{GS} + Z_{O1} Z_{GS} \right)} \tag{3.12}$$

$$Z_{T2} = \frac{Z_{DS} \times \left(Z_X Z_{O1} + Z_X Z_{GS} + Z_{O1} Z_{GS} \right)}{\left(g_m Z_{O1} Z_{GS} Z_{DS} \right) + \left(Z_X Z_{O1} + Z_X Z_{GS} + Z_{O1} Z_{GS} \right) + \left(Z_{O1} Z_{DS} + Z_{GS} Z_{DS} \right)} \tag{3.13}$$

$$S22 \equiv \frac{Z_{T2} - Z_{O2}}{Z_{T2} + Z_{O2}} = \frac{\alpha - Z_{O2}\beta}{\alpha + Z_{O2}\beta} \tag{3.14}$$

$$S22 \to 0 \Rightarrow Z_{O2}\beta = \alpha \tag{3.15}$$

$$S12 \equiv 2 \times \frac{\sqrt{Z_{O2}}}{\sqrt{Z_{O1}}} \times \frac{V_{O1}}{E_2} = \left(2 \times \frac{\sqrt{Z_{O2}}}{\sqrt{Z_{O1}}} \right) \times \frac{Z_{O1}Z_{GS}Z_{DS}}{Z_{O2}\beta + \alpha}$$

$$= \left(\frac{\sqrt{Z_{O2}}}{\sqrt{Z_{O1}}} \right) \times \frac{Z_{O1}Z_{GS}Z_{DS}}{Z_X \left(Z_{O1}Z_{DS} + Z_{GS}Z_{DS} \right) + Z_{O1}Z_{GS}Z_{DS}} \tag{3.16}$$

$$S12 = \left(\frac{\sqrt{Z_{O2}}}{\sqrt{Z_{O1}}} \right) \times \frac{Z_{O1}Z_{GS}Z_{DS}}{\left(\frac{1}{j\omega C_{GD}} \right) \times \left(Z_{O1}Z_{DS} + Z_{GS}Z_{DS} \right) + Z_{O1}Z_{GS}Z_{DS}} \tag{3.17}$$

$$S12 \approx \frac{\sqrt{Z_{O2}}}{\sqrt{Z_{O1}}} \tag{3.18}$$

$$Z_X = j\omega L_{RES} // \frac{1}{j\omega C_{GD}} = \frac{j\omega L_{RES}}{1-\omega^2 L_{RES} C_{GD}} \tag{3.19}$$

$$\text{if } \omega^2 L_{RES} C_{GD} = 1 \Rightarrow Z_X \to \infty \Rightarrow S12 \to 0 \tag{3.20}$$

For RF system, an ideal inductor is equal to a short path for DC because its impedance is "jωL". Therefore, as long as the resonated inductor is implemented, a blocking capacitor is always used for blocking unnecessary DC path. This blocking capacitor, C_B, comes from the consideration during measurement. The cable inherent resistance between probe and DC power supply is around 3 ohm. It's not a serious issue for small-signal systems such as receiver front-end. However, for hundreds milli-ampere transmitter front-end, it may cause milli-volt or even several volts drop during measurement. Because such voltage drop may downgrade internal biasing points by different levels, DC current may be sunk into unexpected path when measurement. In order to avoid this phenomenon, a capacitor must be added to block DC current from stage to stage.

Fig. 3.20 is the equivalent network between gate-drain of common-source transistor. Because C_B is used for DC blocking, its value is much larger than parasitic capacitance C_{GD} and the resonating frequency of L_{RES} and C_B is much lower than the resonating frequency of L_{RES} and C_{GD}. After the resonating frequency of L_{RES} and C_B, the series L_{RES} and C_B can be equivalent to an inductance L'_{RES} and its value is shown in (3.21). Therefore, the equivalent network between gate and drain can be express in Fig. 3.21. The impedance between gate and drain in Fig. 3.21 is given by (3.22). Thus

if the inductance value must be chosen to satisfy the condition in (3.23), the parasitic capacitance can be resonated and the reverse isolation can be improved.

$$L'_{RES} = L_{RES} - \frac{1}{\omega^2 C_B} \tag{3.21}$$

$$j\omega L'_{RES} // \frac{1}{j\omega C_{GD}} = \frac{j\omega L'_{RES}}{1-\omega^2 L'_{RES} C_{GD}} \tag{3.22}$$

$$\omega = \frac{1}{\sqrt{L'_{RES} C_{GD}}} \tag{3.23}$$

Shown in Fig. 3.22 is the designed 2-stage cascaded current-mode PA that has been published by the present author [20]. The proposed PA consists of two cascaded current-mirror amplifiers to amplify the current signal.

By (3.9)–(3.10), the transistors' dimensions and optimal load resistance can be roughly predicted by hand calculation. Two stages are adopted for the budget of PA's output power and power gain. Because the biasing is fixed to V_{DD}, the variable for transistor itself is size. The transistor's size of output stage (2^{nd}-stage) is determined by the required output power. The size of driving stage (1^{st}-stage) is determined by the required power gain which amplifies mixer output signal to the level of input signal required by PA's 2^{nd}-stage.

Three on-chip inductors, L_4–L_6, are used to resonate out the parasitic capacitance of the drain (that is, node B_1, B_2, and B_3). Because of large transistors and resultant seriously parasitic capacitance, two on-chip inductors, L_7 and L_8, are used to resonate out the gate-drain parasitic capacitance $C_{GD,M8}$ and $C_{GD,M10}$ of transistors M_8 and M_{10}, respectively.

The inductors L_4 and L_5, which are used for resonating parasitic capacitance of the internal nodes of power amplifier (B_1 and B_2), are determined and simulated with core circuit of power amplifier during the load-pull analysis. So if the performance of these resonated inductors is affected by the output impedance transformation network, which is determined by load-pull analysis, then these inductors have to be modified after the output impedance transformation network has been implemented. However, the chosen Z_L and its corresponding transformation network are for previous circuit – core circuit of PA with non-modified inductors, load-pull analysis has to be simulated again for modified inductors. Because load-pull analysis has to be simulated again as long as any part of circuit is modified, iterative simulations may be needed to determine the values of resonated inductors and output impedance transformation network. For iterative procedure, it is endless if it is not convergent. From this point of view, the better way is to increase reverse isolation so that these resonated inductors need no any modification when the output impedance transformation network is connected to the circuit. That is the reason why both two inductors (L_7 and L_8) are used between gate-drain for both stages of PA.

Two capacitors, C_4 and C_5, are adopted to cut out unnecessary DC paths provided by L_7 and L_8. R_3 is used for stability consideration. In fact, both M_8 and M_{10} could form Colpitts oscillators. First stage is stable because node B_2 is low-impedance node. However, node B_3 is high impedance at low frequency. Therefore, R_3 is designed to

decrease the loop gain of Colpitts oscillator. The sweep value of R_3, shown in Fig. 3.23, shows the larger value of R_3 can further degrade the loop gain and more stable. This figure also shows the node B_3 is high impedance before it becomes negative resistance. Considering the process variation, 5-ohm R_3 is chosen. It is realized by 6-μm length, 2-μm width, 5-paralleled poly resistor and degrades power gain less than 1 dB. Its effect, in terms of k and b factor, is shown in Fig. 3.24–3.25.

The output impedance transformation network determined by load-pull analysis is composed of C_6, L_9, L_{10}, and the parasitic capacitance of the output pad C_{PAD4}.

In order to minimize chip area, internal nodes such as PA's input (connected to mixer) and the node between PA's 1st and 2nd stage are not implemented any matching networks. Instead, shunt inductors are adopted to resonate out the parasitic capacitance of these nodes. Because any parasitic capacitance is equivalent as a short path for high frequency, it may degrade RF signal by leakage RF signal to ground. The output node, however, is connected to external 50-ohm impedance probe during measurement. Therefore, output transformation network is needed and implemented by load-pull analysis. Fig. 3.26 is the constant P_{OUT}, constant PAE contours and the chosen Z_L by trade-off between them. Fig. 3.27 is the impedance transformation network, which transfers 50-ohm port to chosen Z_L determined by the load-pull analysis. The transferred load impedance seen by power amplifier is shown in Fig. 3.28.

3.2.3 Transmitter Front-End

Shown in Fig. 3.29 is the integrated current-mode transmitter front-end which consists of a differential current-operated self-switching mixer that up-convert the signal from IF to RF according to LO signal and a 2-stage cascaded current-mode power amplifier. Two shunt inductors at the inter-stage node of mixer-PA are merged

into one inductor which has the same value and higher quality factor. Beside this inductor, the dimensions and functions of other components are the same as mention in section 3.2.1 and 3.2.2. The summary tables for dimension, value, and DC bias are given by Table 3.1 and Table 3.2.

The effective schematic diagram which includes routing effect after layout is shown in Fig. 3.30. High-frequency electro-magnetic (EM) effect of routing has been simulated individually by 3-D EM-simulated EDA tool which is called as High Frequency Simulation Software (HFSS). There are several sections, such as the inter-stage of mixer–PA, the terminals of two L_{GD}s, and the gate between master- and slave-end of PA's 2^{nd}-stage. The routing effect of inter-stage node comes from the distance between mixer and power amplifier. Others are connected by long wire because of the guard-ring of L_{GD}. These wire connections are longer than $\lambda/10$ that their EM effect can not be neglected, thus they are simulated by HFSS and modeled by the S2P file (2-port network). The other one is the input port of IF signal. Two two-port network consist of wire connect from the gate of M_1 to IF+ PAD for Path-A and M_4 to IF– PAD for Path-B. Although these two transmission lines do not connect to each other, they are simulated EM analysis together because of the short distance between them. Therefore, the four-port network in terms of S4P is placed between the IF input PAD and gate of the input PMOS. The last one is the three-port network consists of a shunt inductor (L_9) and a series inductor (L_{10}) at the output of power amplifier. Output transformation network, which includes C_6, this three-port network, and the parasitic capacitance of output PAD C_{PAD4}, can transfer 50-ohm impedance of output port to desired impedance shown in Fig. 3.27. The procedure and model view for EM analysis are illustrated in Fig. 3.31 and Fig. 3.32. Dimension for all EM-simulated components are summarized in Table 3.3.

3.3 Post-Simulation Results

The 24-GHz integrated current-mode transmitter is designed in 0.13-μm 1P8M CMOS technology with IF frequency of 100 MHz and LO frequency of 23.9 GHz. The performance is simulated by EDA tool which is called as Advanced Design System (ADS). From the supply voltage of 1.2 V, the current consumption of the differential self-switching up-conversion mixer and current-mode PA are 15.7 mA and 259.8 mA, respectively. The total power dissipation is 330.5 mW. Fig. 3.33–Fig. 3.36 show the post-simulation performance of mixer with the loading equaled to the PA's input impedance.

Fig. 3.33 is S-parameter S11, S22, and S33 for return loss of IF input, LO input, and RF output, respectively. This mixer has S11 of –8.9 dB at 100 MHz, S22 of –16.4 dB at 23.9GHz, and S33 of –5.6 dB at 24 GHz.

Fig. 3.34 is constructed by –30-dBm fixed IF input power and sweeping LO input power to see the performance of the conversion gain. Because the nonlinear effect of M_2 and M_5 when LO input power is too large, the conversion gain will be degraded. From this figure, it's obvious that the chosen 4-dBm LO input power can provide optimal conversion gain for this mixer.

The linearity and conversion gain with 4-dBm LO input power are illustrated in Fig. 3.35 and Fig. 3.36. It shows the conversion gain is around 1dB, input 1-dB compression point (IP_{1dB}) is –12 dBm, and output 1-dB compression point (OP_{1dB}) is –12 dBm in Fig. 3.35. This figure also shows the mixer is a double-side band (DSB) mixer, so the signal at the frequency of LO + IF (upper-side band, USB) and LO – IF (lower-side band, LSB) will be produced and inject into power amplifier. Fig. 3.36 shows the performance of 2-tone test. Post-simulation results show this mixer has input

third-order inter-modulation intercept point (IIP3) of 1 dBm and output third-order inter-modulation intercept point (OIP3) of 1 dBm.

The S-parameter, P_{OUT} and PAE versus input power (P_{IN}), and IIP3 and OIP3 of 2-stage cascaded power amplifier presented by post-simulation are illustrated in Fig. 3.37, Fig. 3.38, and Fig. 3.39, respectively. According to Fig. 3.37, the stand-alone current-mode PA has S11 of –4.9 dB, S12 of –54.7 dB, S21 of 21.7 dB, and S22 of –9.5 dB at 24 GHz. "P_{OUT} versus P_{IN}" and "PAE versus P_{IN}" curves in Fig. 3.38 show this power amplifier has 21.7-dB power gain. For 1-tone test, this power amplifier has IP_{1dB} of –5 dBm, OP_{1dB} of 15.6 dBm, and 12.3 % PAE at 1-dB compression point. The maximum PAE is 27.7 % at the input power of 7 dBm and output power of 18.4 dBm. P_{OUT} v.s. P_{IN} and PAE v.s. P_{IN} of 2-tone test has also been simulated because of double-side band mixer. In order to correspond to mixing function, the frequencies for 2-tone test signals are LO + IF and LO – IF. For 2-tone test, its IP_{1dB} is –10 dBm, OP_{1dB} is 10.6 dBm, and the PAE at 1-dB compression point is 3.8 %. The maximum PAE for 2-tone simulation is 9.7 % which is for input power of 4 dBm and output power of 14.3 dBm. Fig. 3.39 shows this PA has IIP3 of –2 dBm and OIP3 of 21 dBm in 2-tone simulation.

The post-simulation results for transmitter front-end are shown in Fig. 3.40–3.44. From Fig. 3.40, the post-simulation results show this transmitter front-end has S11 of –8.9 dB at 100 MHz, S22 of –16.4 dB at 23.9 GHz, and S33 of –9.5 dB at 24 GHz for mixer's IF input, LO input, and PA's output, respectively. Fig. 3.41–3.42 illustrate the LO input power and frequency versus output power with –30-dBm IF input. Based on these two figures, 4-dBm and 23.9-GHz LO input signal can perform largest conversion gain.

Under the conditions for largest conversion gain, the linearity and conversion gain are illustrated in Fig. 3.43 and Fig. 3.44. It shows the power gain of this transmitter front-end is 25.2 dB contributed by both mixer and power amplifier. IP_{1dB} is –15 dBm, and OP_{1dB} is 9.1 dBm according to Fig. 3.43. Because of the double-side band of this mixer, the output power performs the same level with the performance of 2-tone test for stand-alone power amplifier. Fig. 3.44 shows the performance of 2-tone test for whole transmitter front-end circuit. Post-simulation results show this integrated circuit has IIP3 of –5 dBm and OIP3 of 20 dBm. Table 3.4 and Table 3.5 give the performance summary of mixer, power amplifier, and integrated transmitter front-end.

Table 3.1 Summary of device value

	Dimension (μm)
M_1	2.5*28/0.13
M_2	2.5*12/0.13
M_3	2.5*20/0.13
M_4	2.5*28/0.13
M_5	2.5*12/0.13
M_6	2.5*20/0.13
M_7	1.2/0.13
M_8	2.5*20*2/0.13
M_9	1.2/0.13
M_{10}	2.5*20*7/0.13
$M_{OP,P1}$	2*2/0.13
$M_{OP,P2}$	2*2/0.13
$M_{OP,N1}$	2*8/0.13
$M_{OP,N2}$	2*8/0.13
$M_{OP,TAIL}$	2*18/0.13

	Value
$XFMR_1$	off-chip
$XFMR_2$	478 pH
L_1–L_2	off-chip
L_{34}	215 pH
L_5	65 pH
L_6	215 pH
L_7	1.24 nH
L_8	165 pH
L_9	104 pH
L_{10}	47 pH

	Value
R_1–R_2	99 ohm
R_3	5 ohm
C_1–C_2	off-chip
C_3	88 fF
C_4	993 fF
C_5	3.08 pF
C_6	431 fF
C_{PAD1}–C_{PAD4}	30 fF

Table 3.2 Summary of DC bias

	Bias
$V_{G,OP}$ (V)	0.5
V_{REF} (V)	0.6
V_{B1} (V)	0.8
V_{B2} (V)	0.95
V_{DD} (V)	1.2
$V_{D,PA1}$ (V)	1.2
$V_{D,PA2}$ (V)	1.2
$V_{D,PA3}$ (V)	1.2

Table 3.3 Dimension summary of transmission line

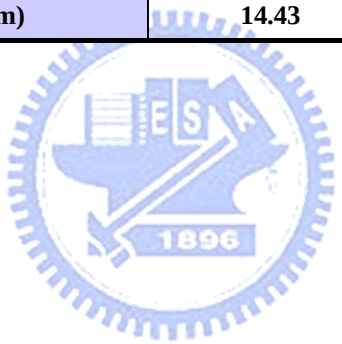
Transmission Line	Width (μm)	Length (μm)
$S2P_1$	6	60
$S2P_2$	3	20
$S2P_3$	3	20
$S2P_4$	6	100
$S2P_5$	3	30+45
$S2P_6$	6	40
L_5	9	210
L_9 (S3P)	6	150+150
L_{10} (S3P)	18	250

Table 3.4 Summary of original post-sim results1

		Post-Sim (Original)
Technology		0.13-μm CMOS
Supply Voltage (V)		1.2
IF (GHz)		0.1
LO (GHz)		23.9
RF (GHz)		24
Power (mW)	Mixer	18.8
	Power Amplifier	311.7
	Total	330.5

Table 3.5 Summary of original post-sim results2

		Post-sim (Original)	Targets
Mixer	Conversion Gain (dB)	1	>0
	OP_{1dB} / IP_{1dB} (dBm)	–12 / –12	-
	P_{OIP3} / P_{IIP3} (dBm)	1 / 1	-
Power Amplifier	Gain (dB)	21.7	>20
	OP_{1dB} / IP_{1dB} (dBm)	15.57/ –5	-
	P_{OIP3} / P_{IIP3} (dBm)	21 / –2	-
	PAE@P_{1dB} (%)	12.26	-
	Peak PAE (%)	27.73	-
	Max. P_{OUT} (dBm)	18.41	>10
TX Front-End	S11 / S22 / S33 (dB)	–8.9 / –16.4 / –9.5	-
	Gain (dB)	25.16	>20
	OP_{1dB} / IP_{1dB} (dBm)	9.08 / –15	-
	P_{OIP3} / P_{IIP3} (dBm)	20 / –5	-
	Max. P_{OUT} (dBm)	14.43	>10



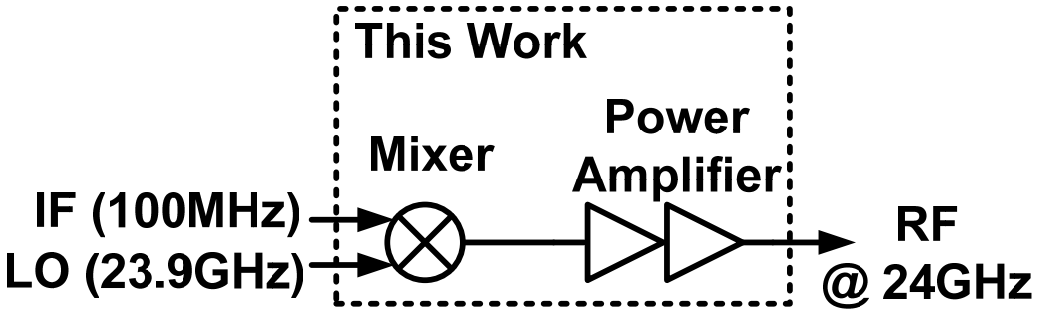


Fig. 3.1 Block diagram of the designed transmitter front-end

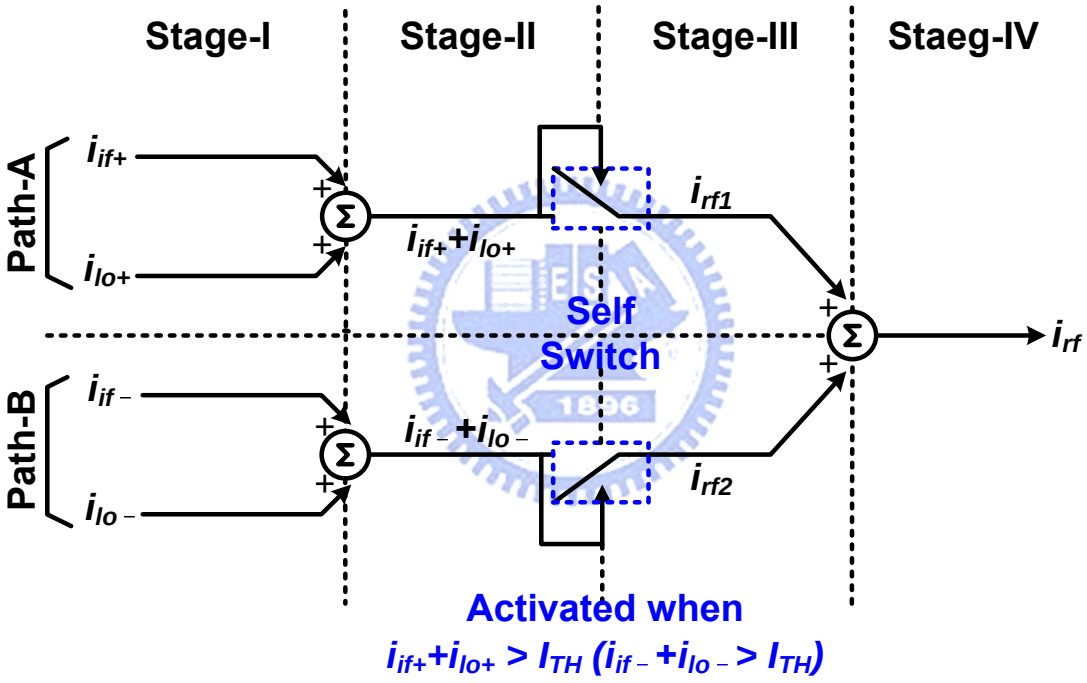


Fig. 3.2 Conceptual diagram of the designed mixer

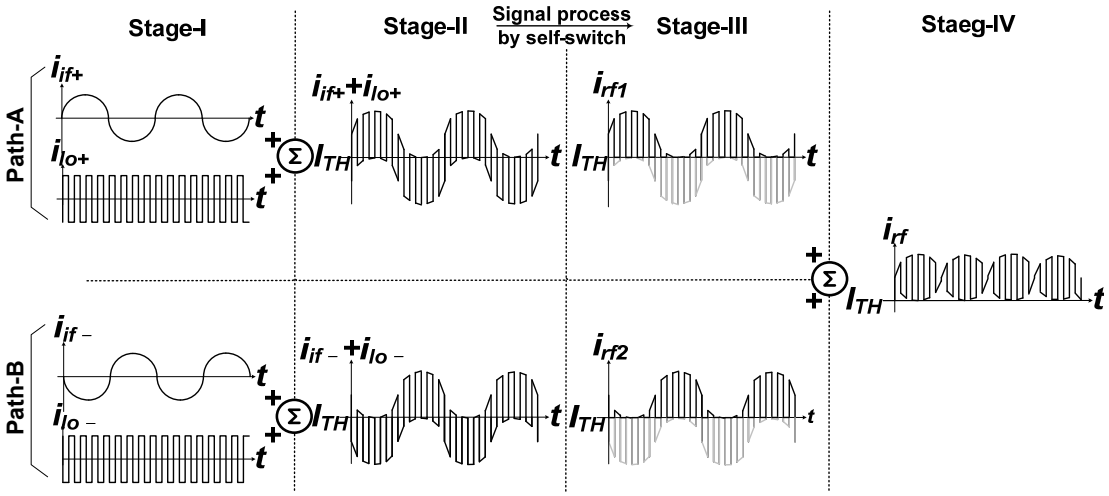


Fig. 3.3 Basic operational principle for designed mixer

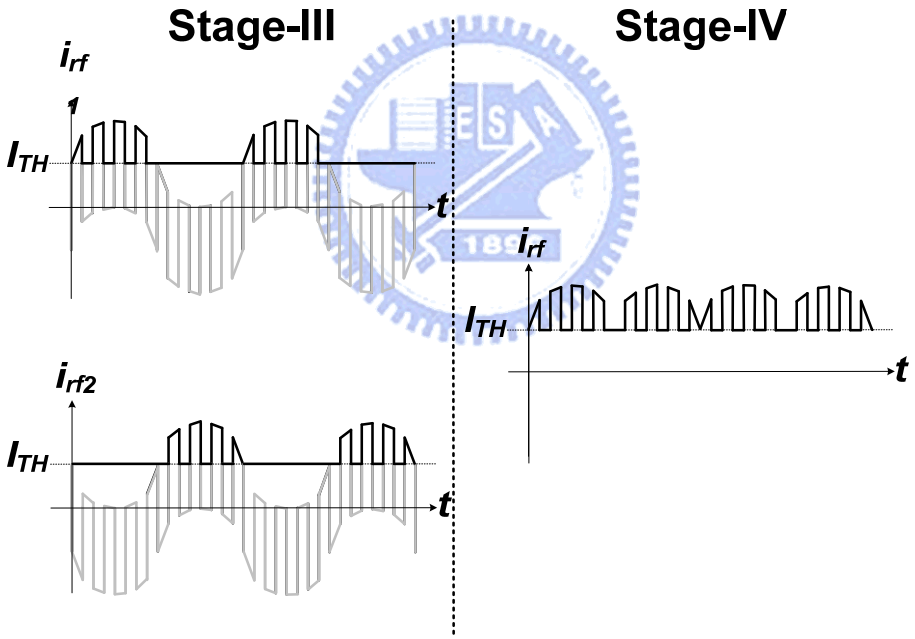


Fig. 3.4 Output waveform for larger I_{TH}

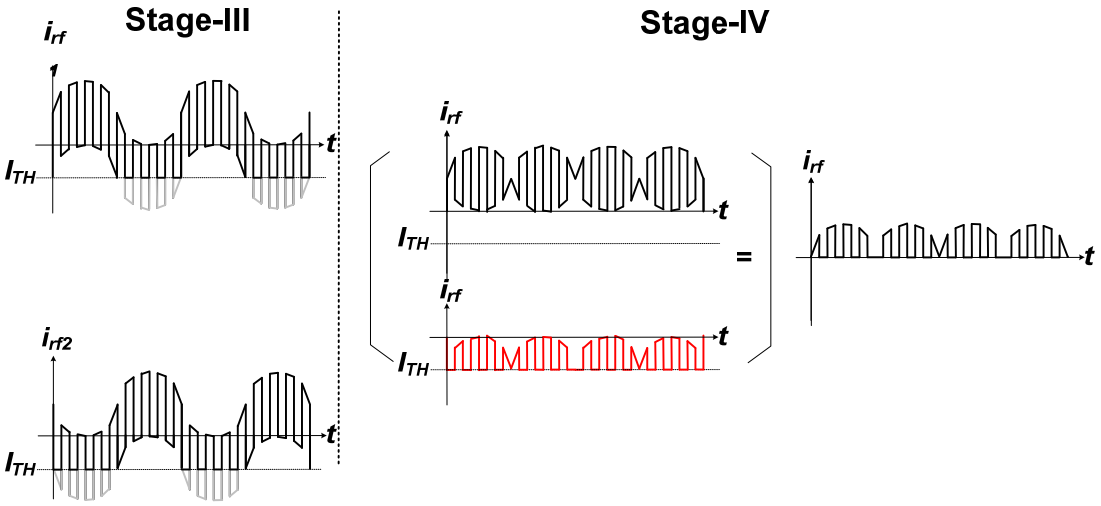


Fig. 3.5 Output waveform for smaller I_{TH}

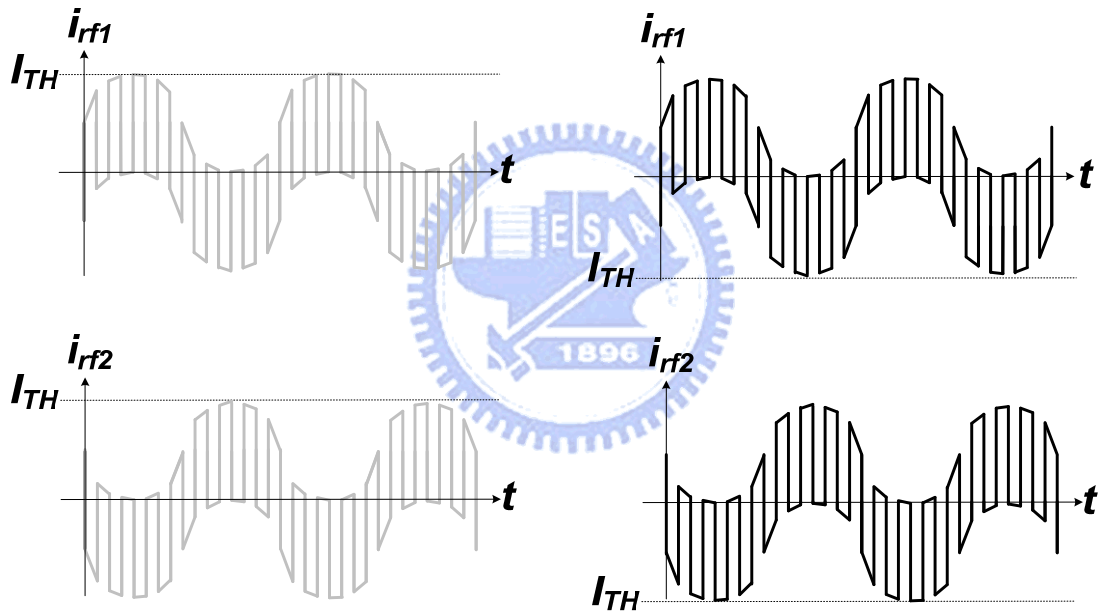


Fig. 3.6 Output waveform for extremely large or small I_{TH}

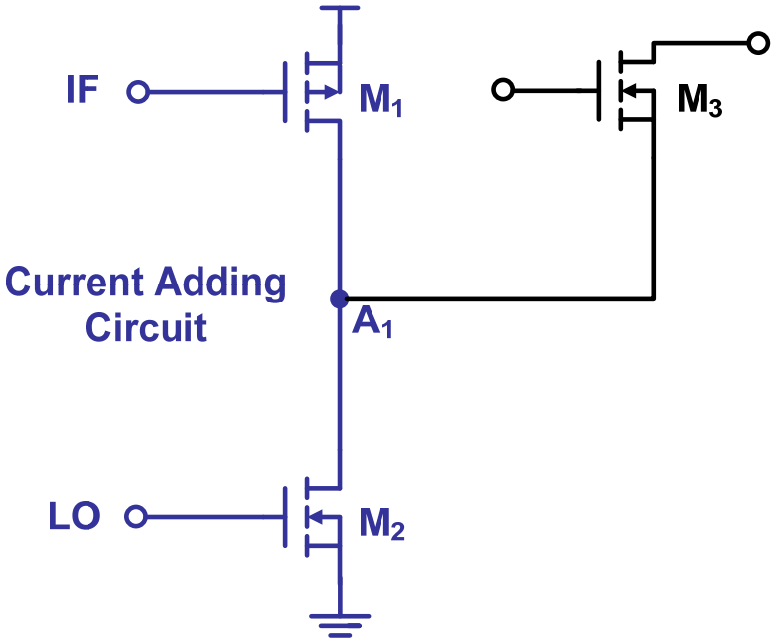


Fig. 3.7 Circuit realization for current-adding circuit

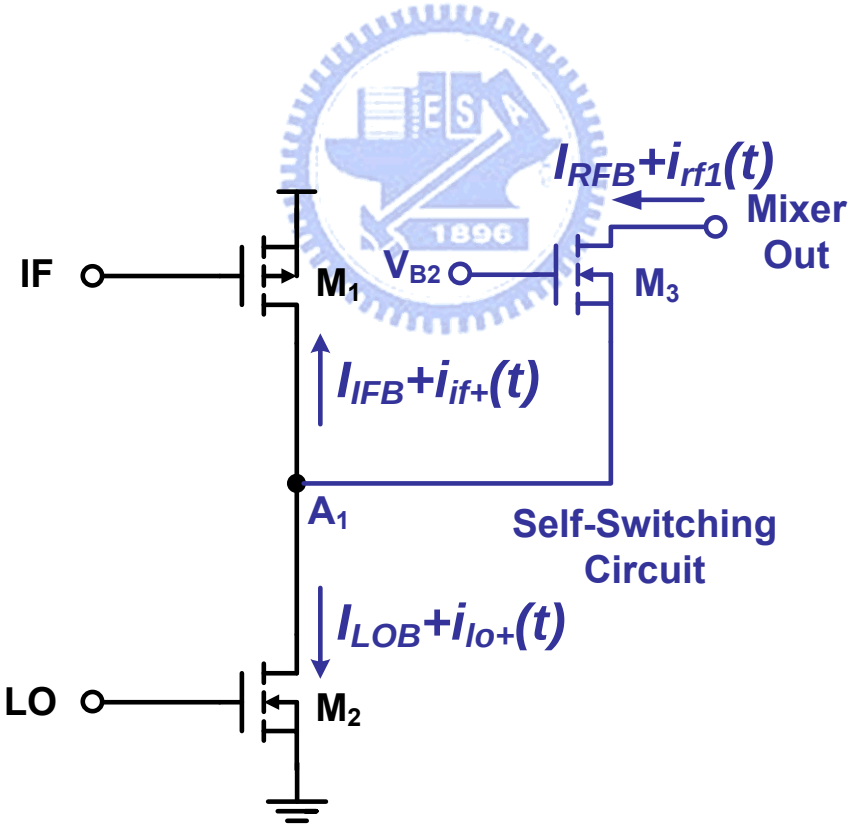


Fig. 3.8 Circuit realization for self-switching circuit

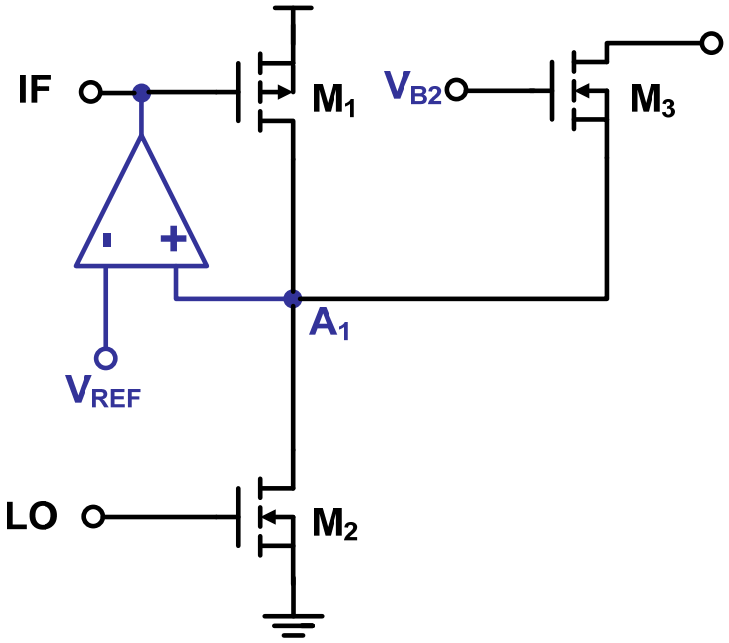


Fig. 3.9 Circuit realization for negative feedback by OPAMP

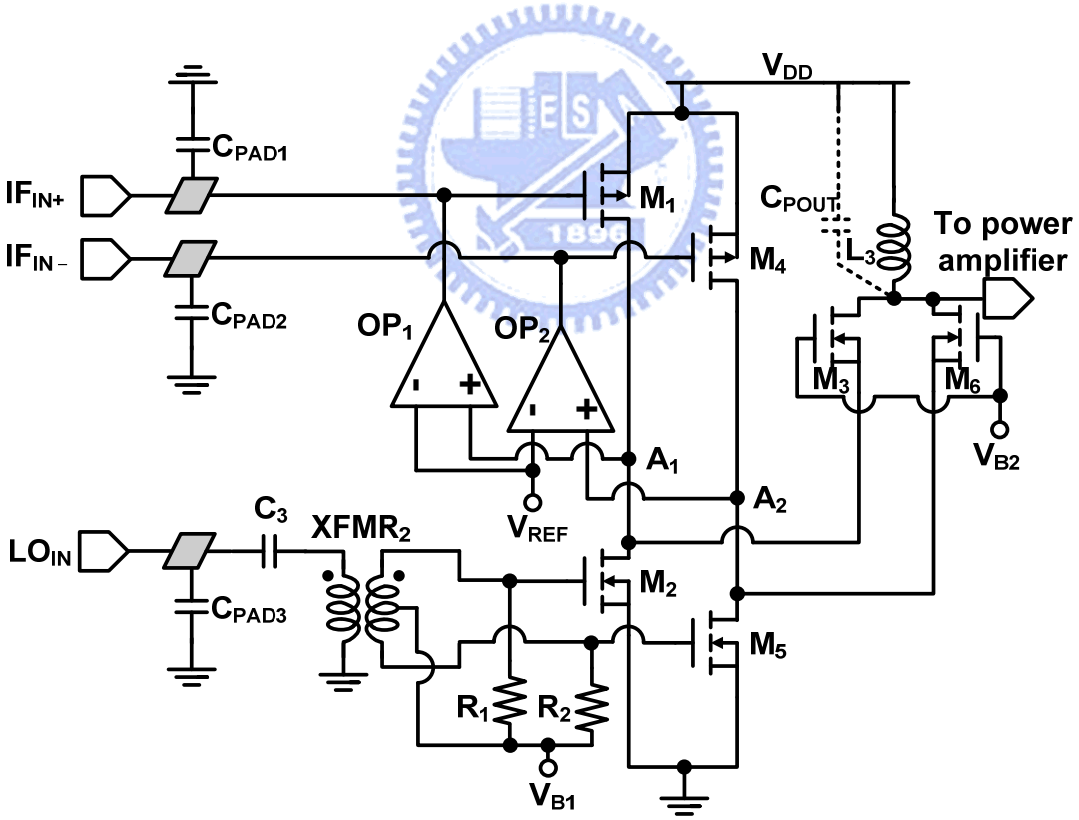


Fig. 3.10 Schematic of the designed mixer

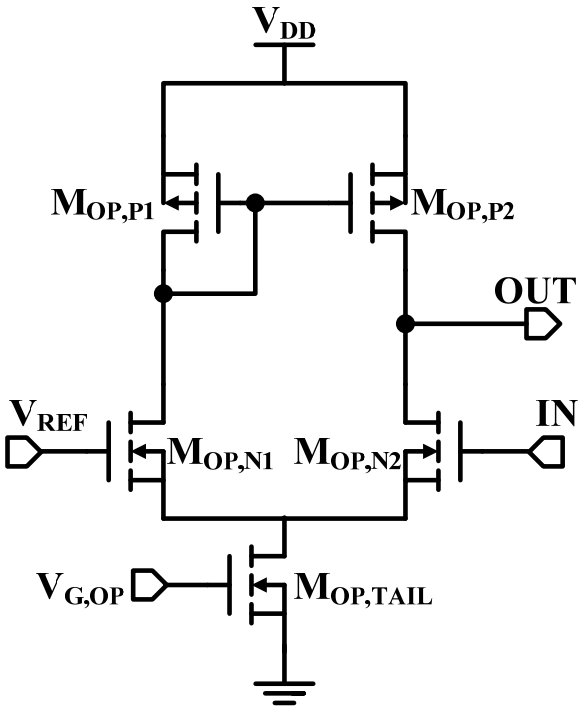


Fig. 3.11 Schematic of the OPAMPs

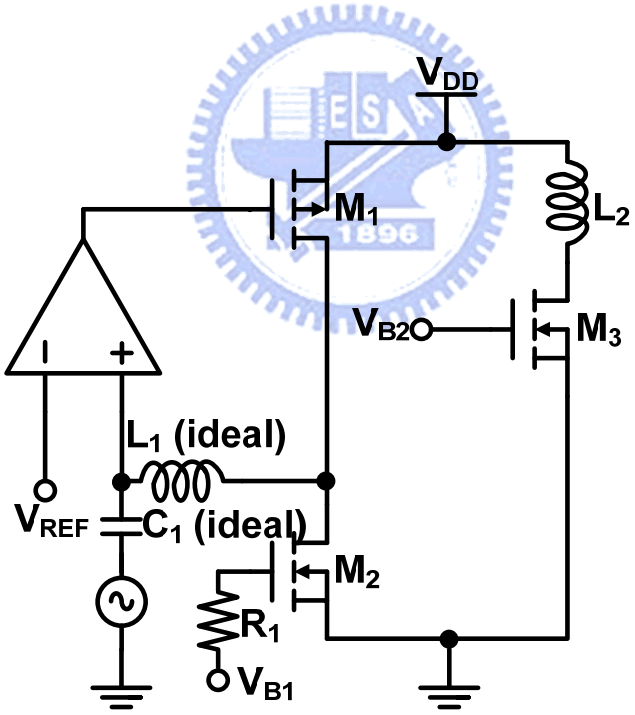


Fig. 3.12 Schematic for simulating the characteristic of the feedback loop

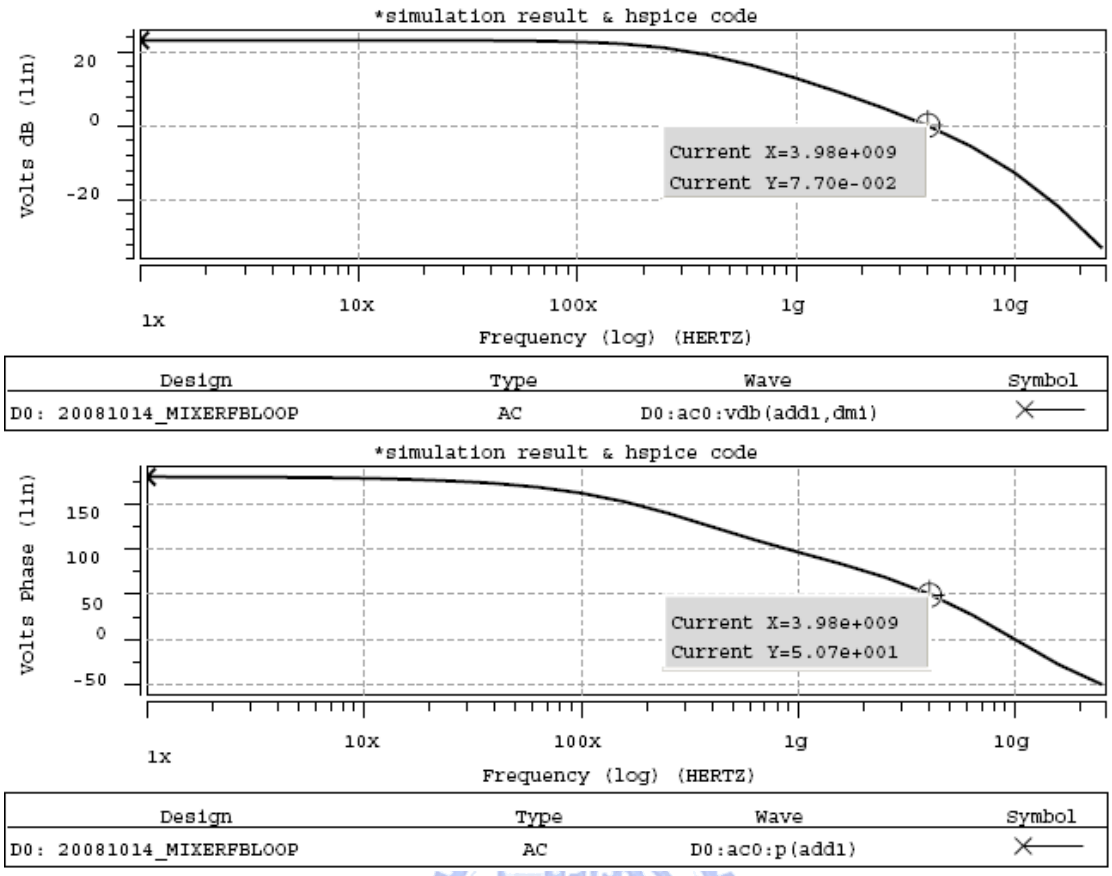


Fig. 3.13 Simulation results for the characteristic of the feedback loop

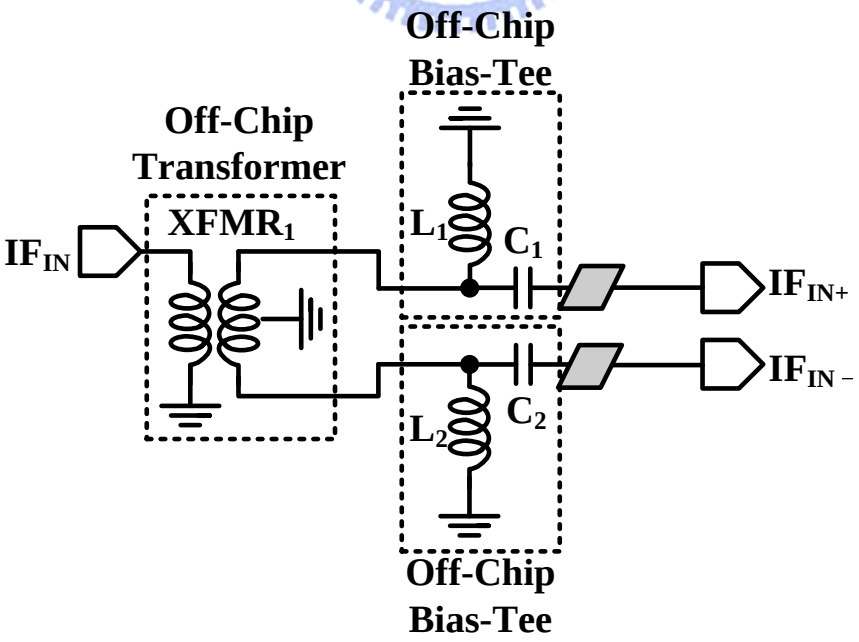


Fig. 3.14 Input matching network for IF signal

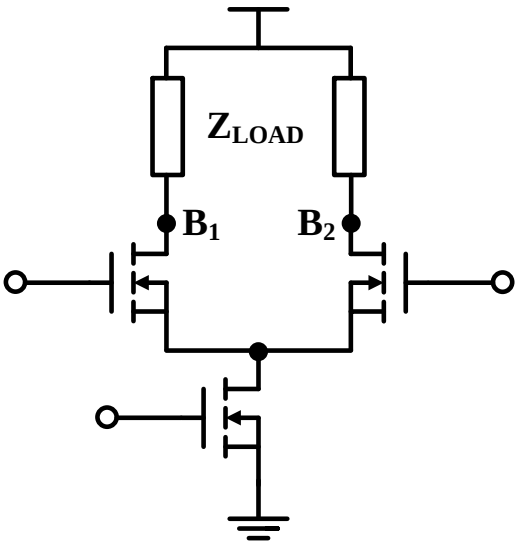


Fig. 3.15 Schematic of Gilbert mixer

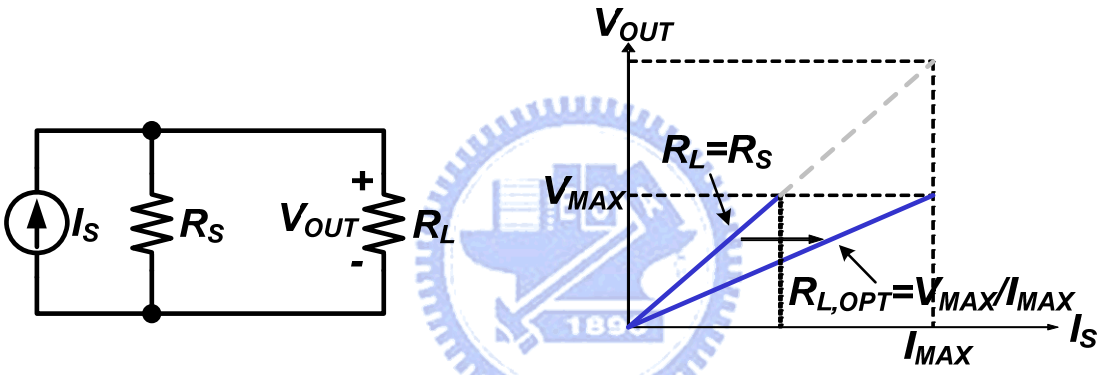


Fig. 3.16 Effect for optimal load when swing is limited

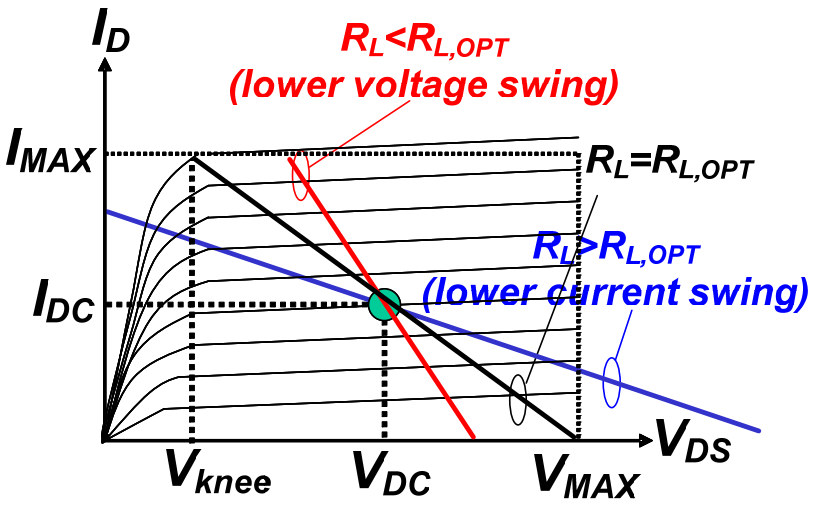


Fig. 3.17 Optimal load resistance determined by load-line analysis

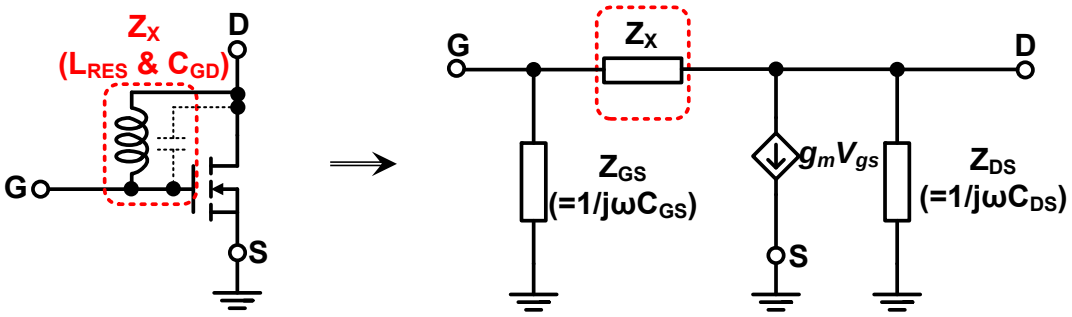


Fig. 3.18 Neutralization for resonating parasitic capacitance C_{GD}

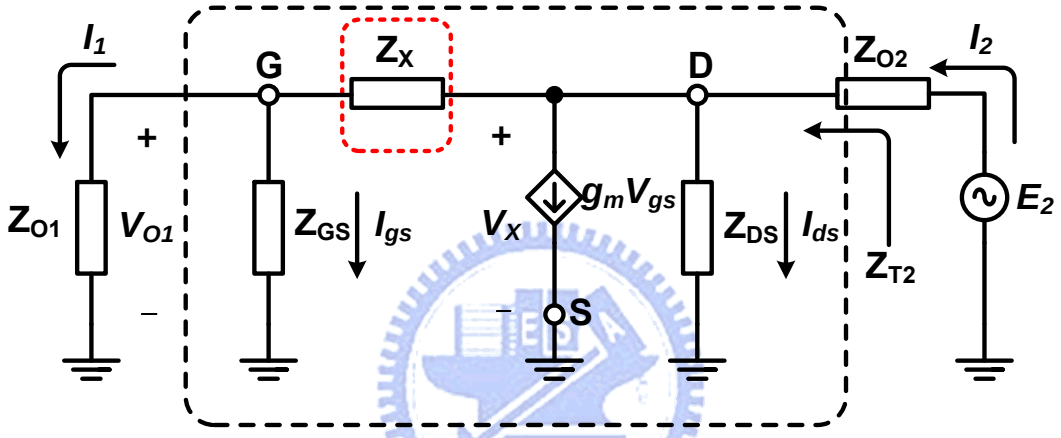


Fig. 3.19 Small-signal model of common-source transistor.

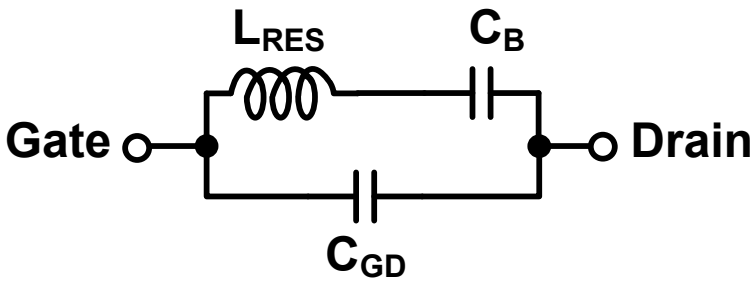


Fig. 3.20 Equivalent network between gate-drain of common-source transistor.

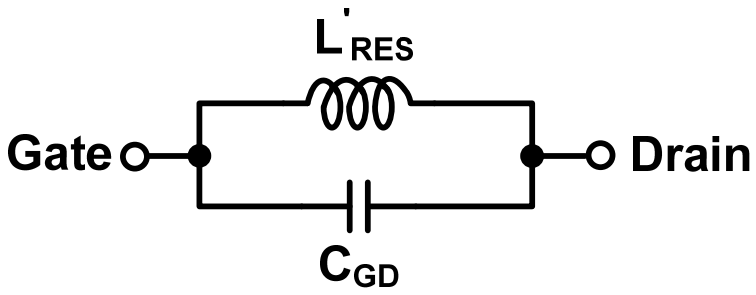


Fig. 3.21 Equivalent network between gate-drain of common-source transistor.

(L'_{RES} is the equivalent inductance of L_{RES} and C_B)

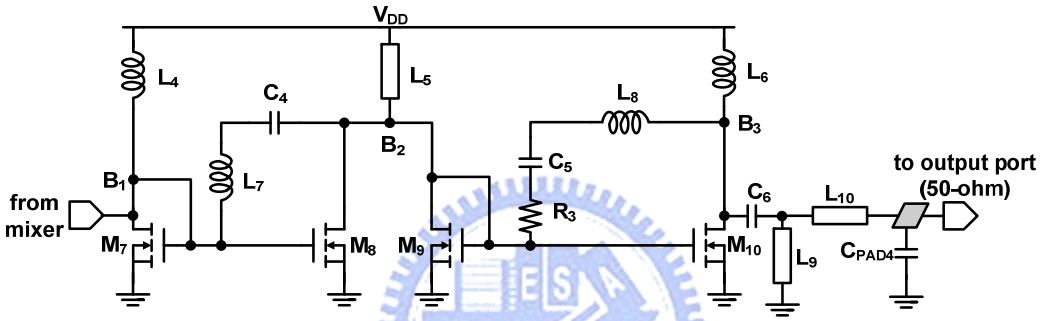
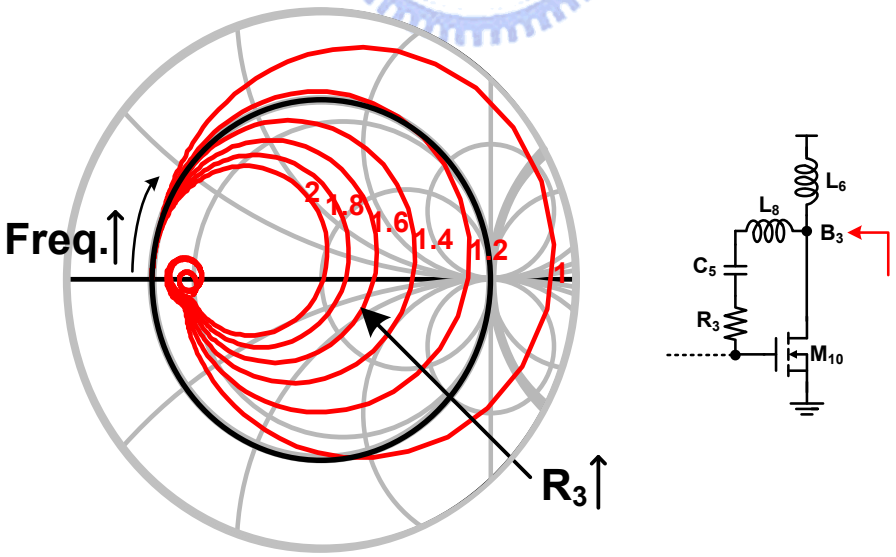


Fig. 3.22 Schematic of designed power amplifier



R_3=1–2 ohm
step=0.2 ohm
Frequency : 0.01–40 GHz

Fig. 3.23 Sweep value of R_3

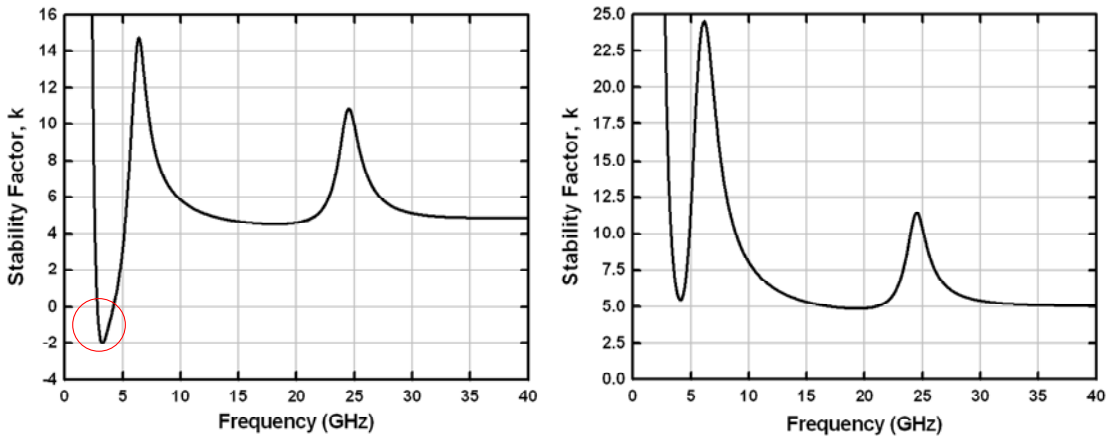


Fig. 3.24 Stability factor (k factor) without and with R_3

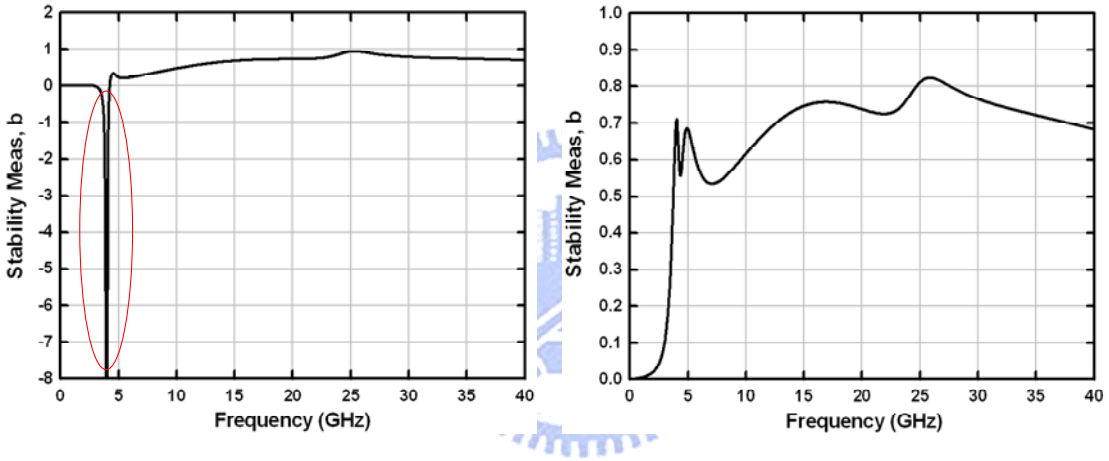


Fig. 3.25 Stability meas (b factor) without and with R_3

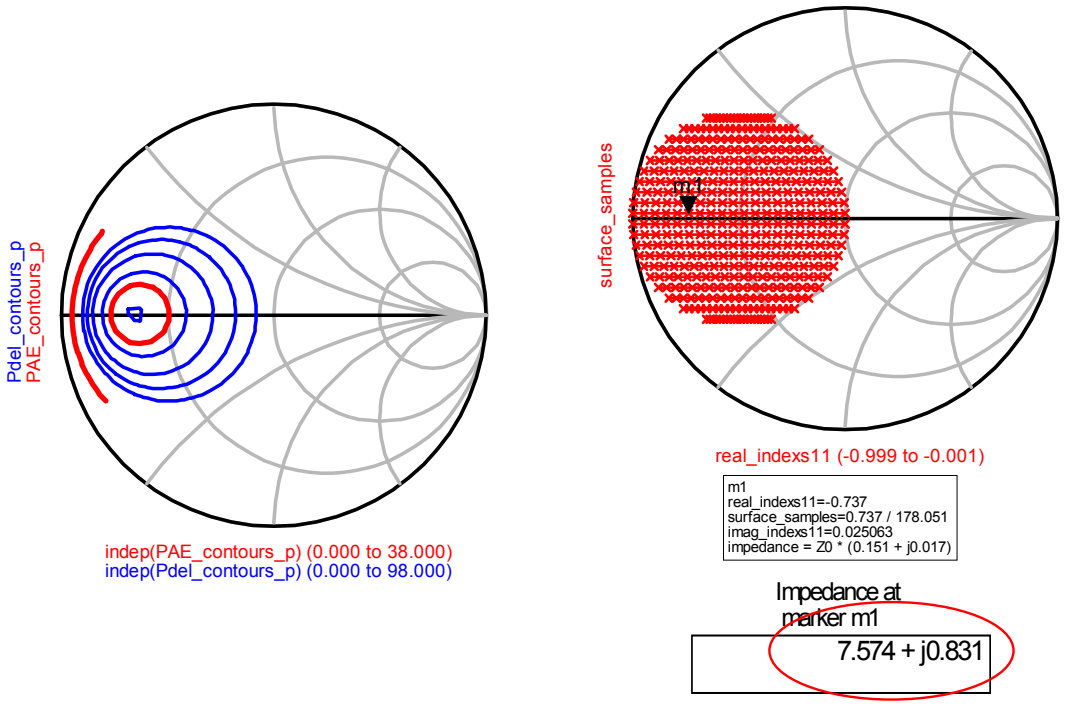


Fig. 3.26 Constant P_{OUT}, constant PAE contours and the chosen Z_L

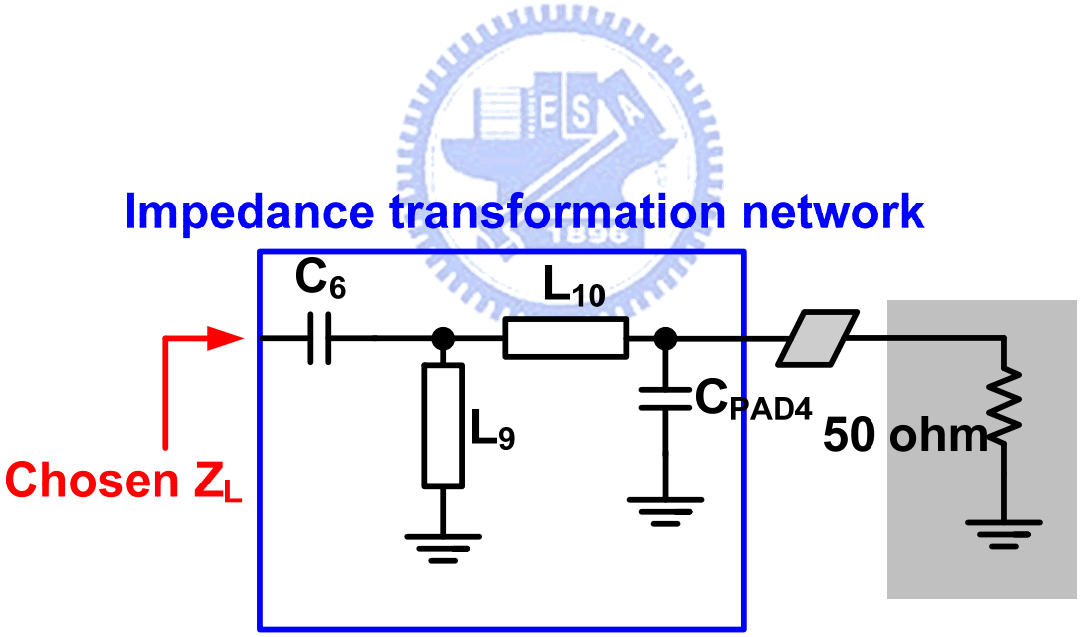


Fig. 3.27 Impedance transformation network of power amplifier

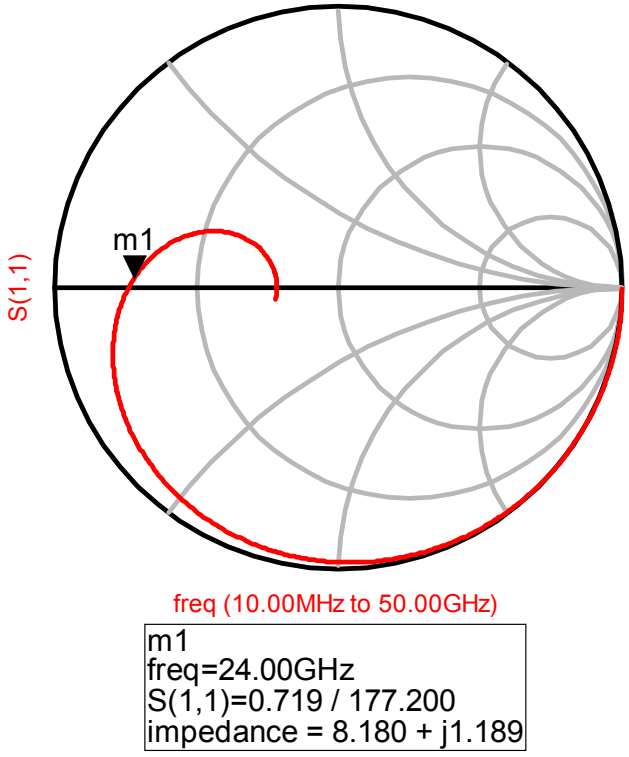


Fig. 3.28 Load impedance transferred by transformation network

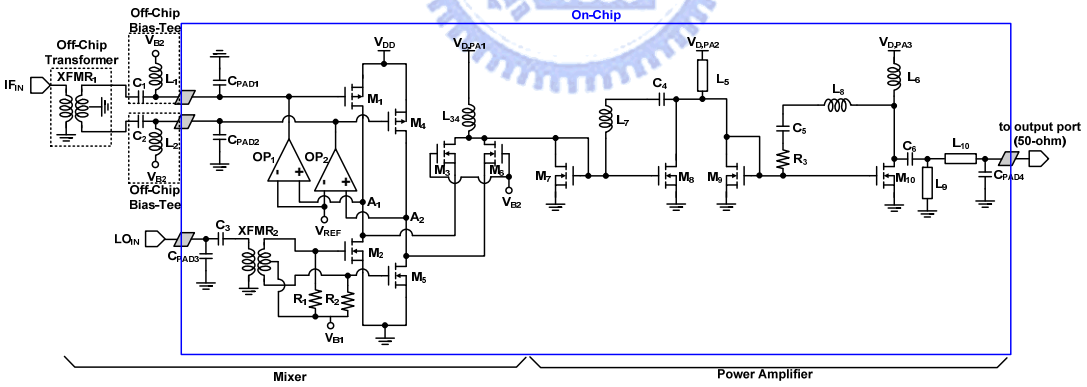


Fig. 3.29 Schematic of designed current-mode transmitter front-end

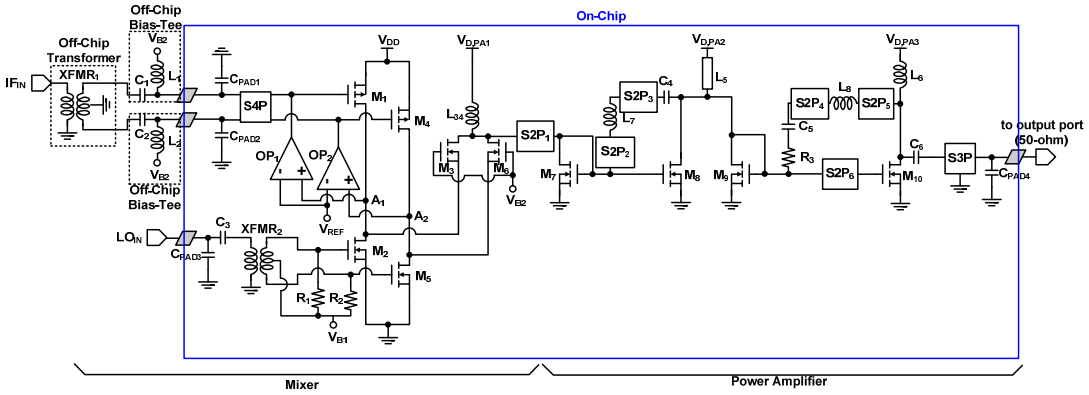


Fig. 3.30 Schematic of designed current-mode transmitter front-end

(with parasitic routing effect)

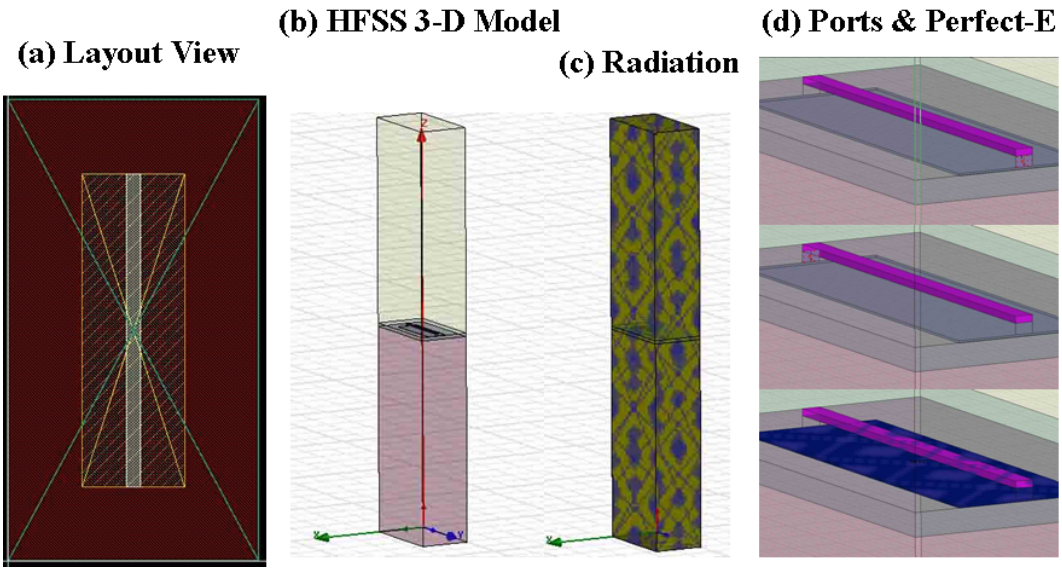


Fig. 3.31 Layout, 3-D model and setting for EM analysis (2-port networks)

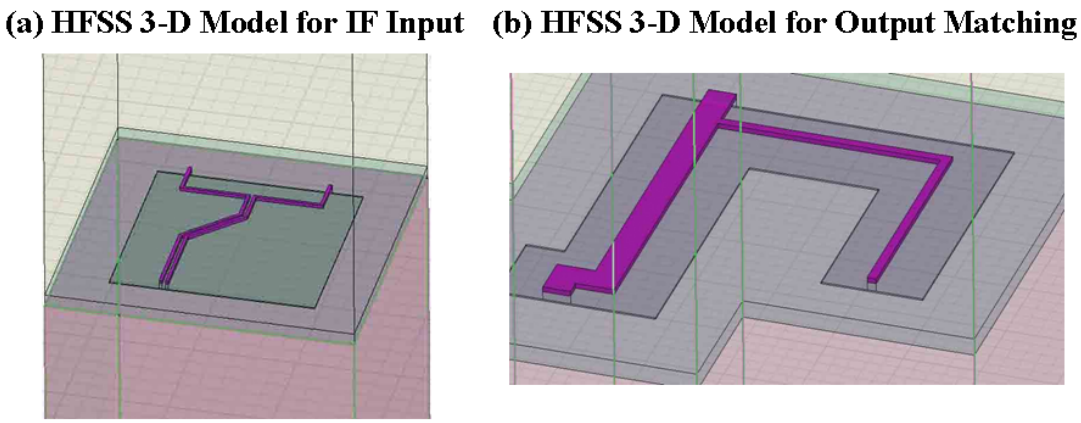


Fig. 3.32 Layout, 3-D model and setting for EM analysis (3- and 4-port networks)

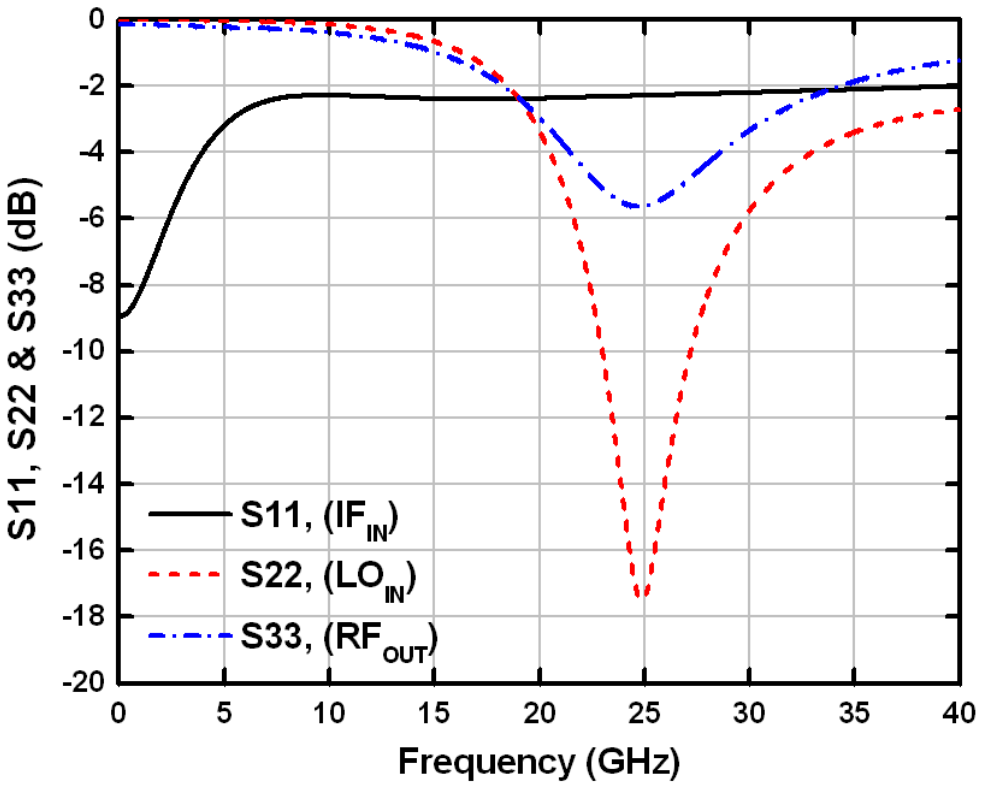


Fig. 3.33 S-parameter of stand-alone mixer

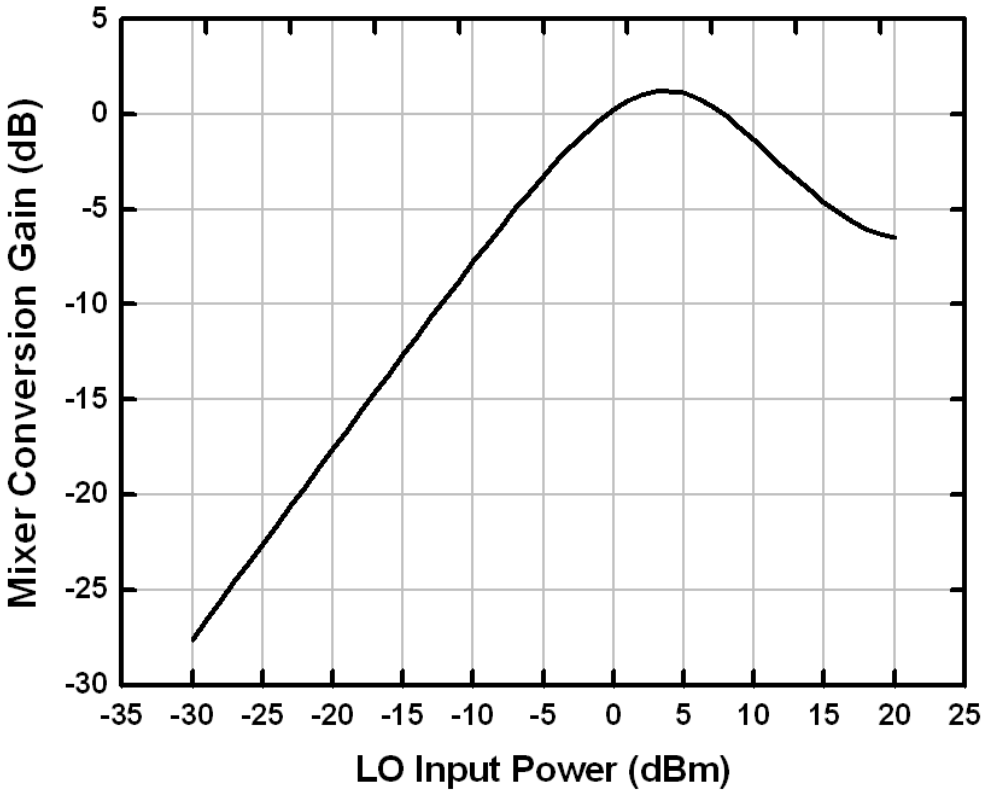


Fig. 3.34 Sweep LO power for stand-alone mixer

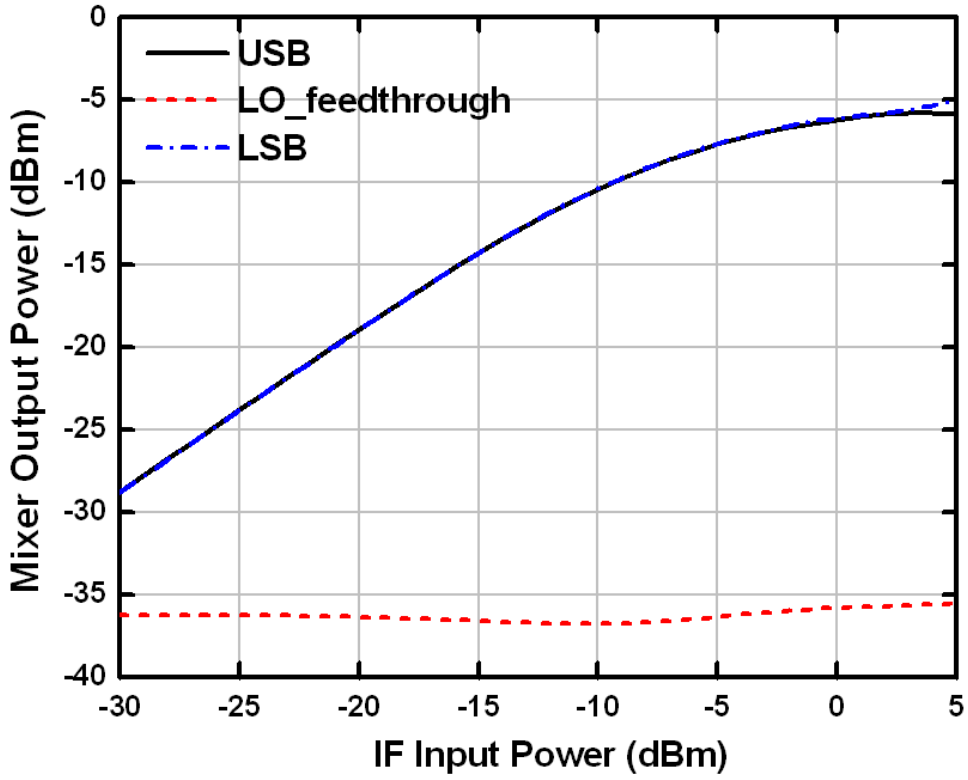


Fig. 3.35 1-tone test for stand-alone mixer

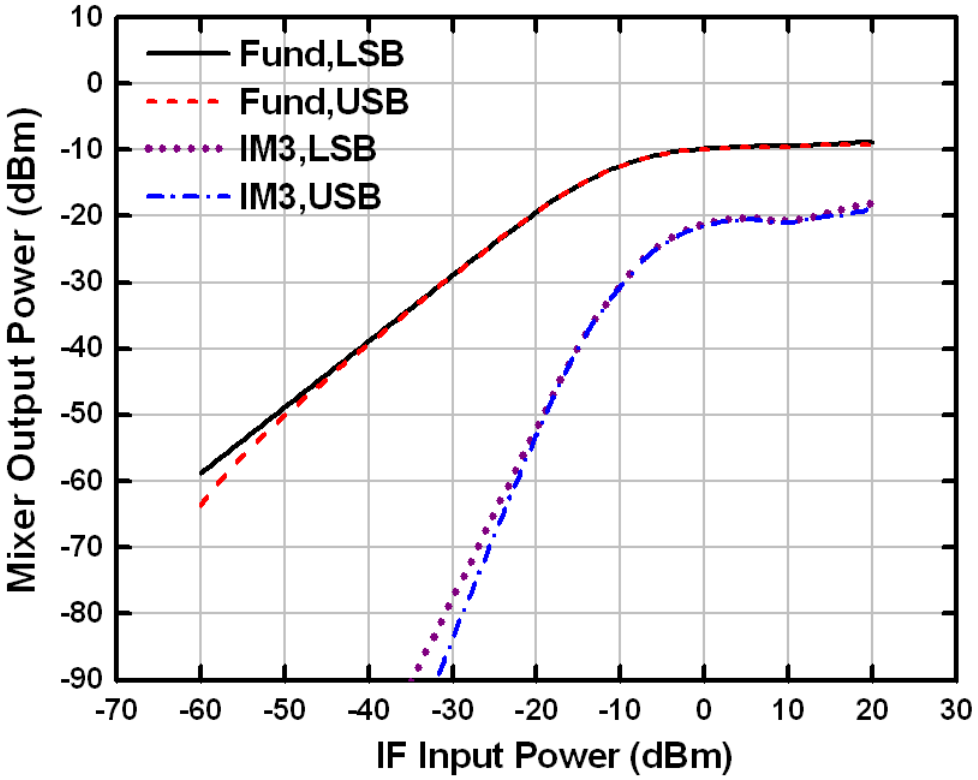


Fig. 3.36 2-tone test for stand-alone mixer

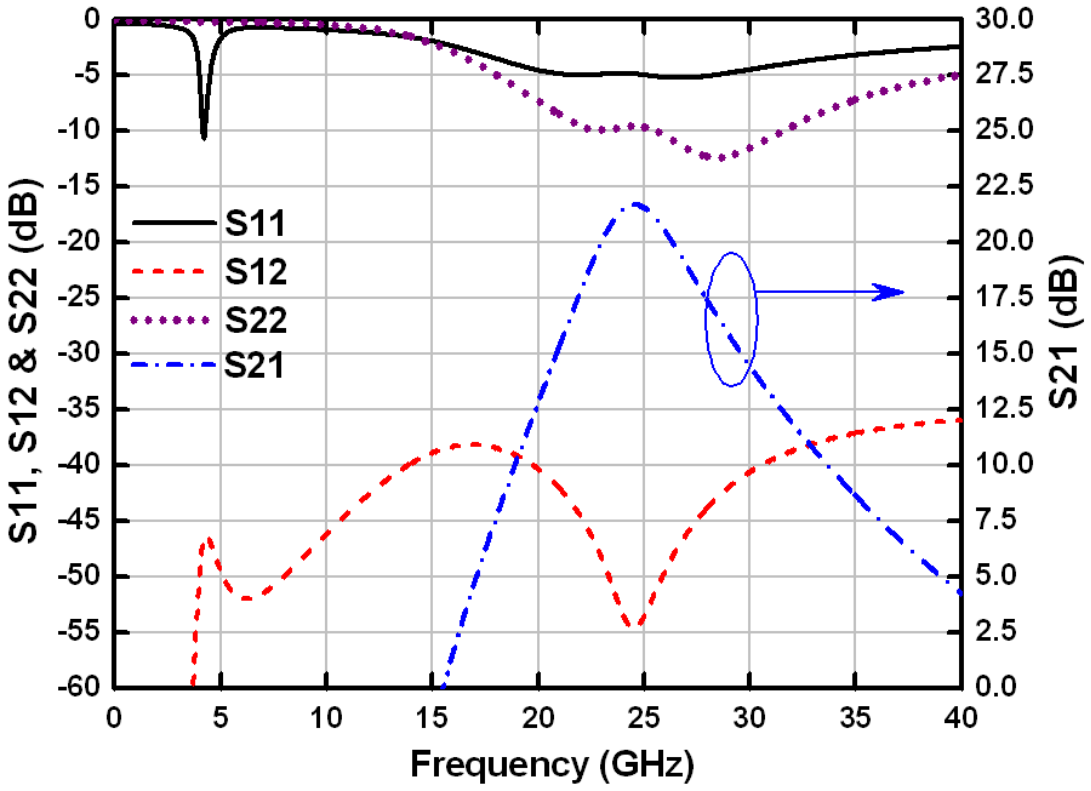


Fig. 3.37 S-parameter of 2-stage current-mode power amplifier

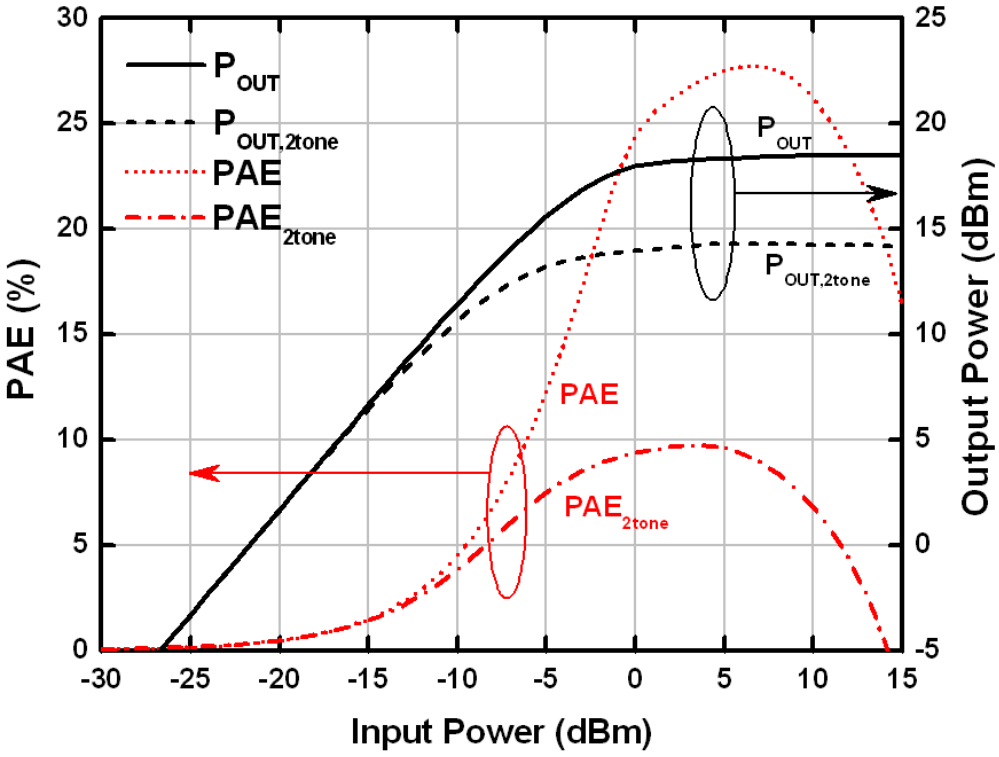


Fig. 3.38 P_{OUT} versus P_{IN} and PAE versus P_{IN} for 2-stage current-mode power amplifier

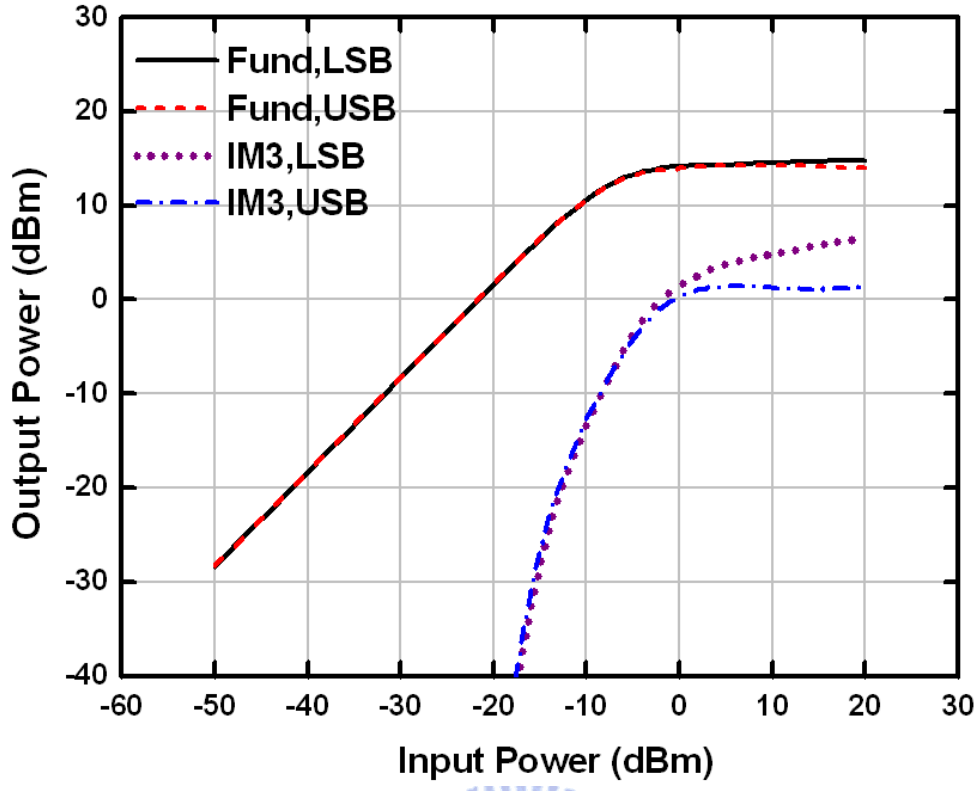


Fig. 3.39 2-tone test for 2-stage current-mode power amplifier

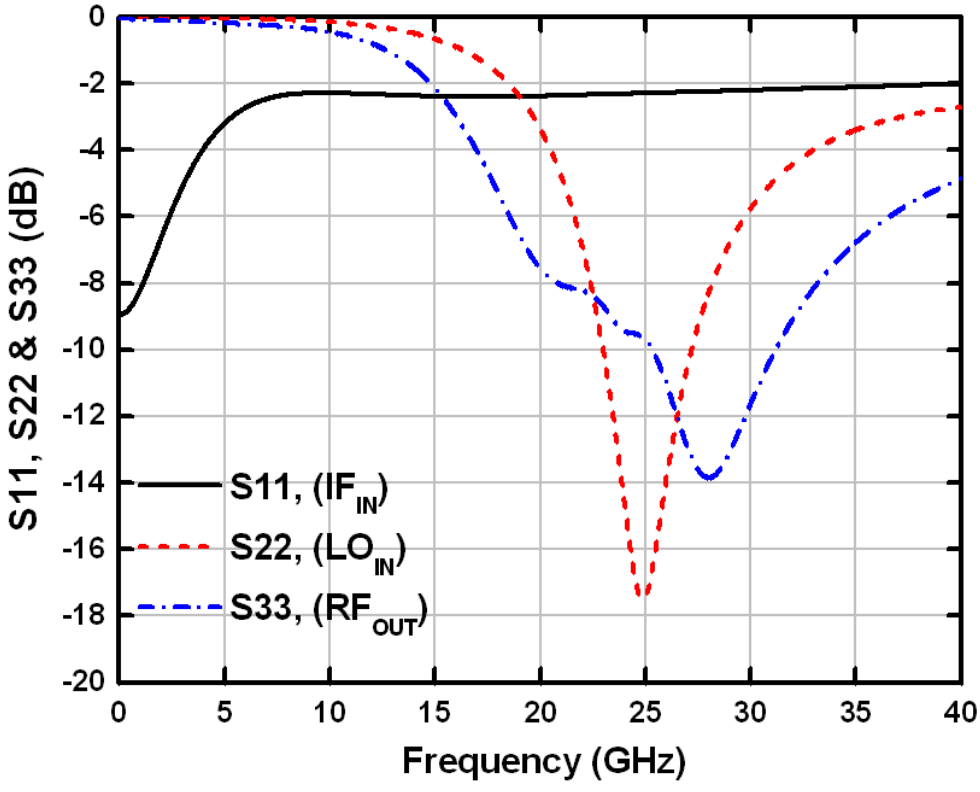


Fig. 3.40 S-parameter of designed transmitter front-end

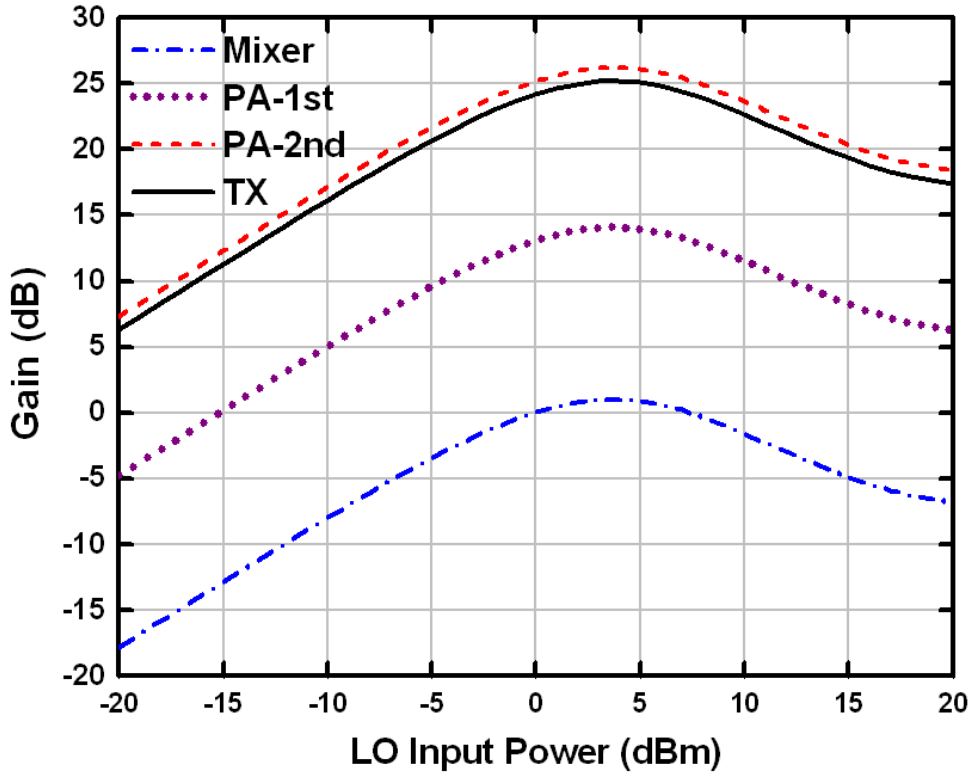


Fig. 3.41 Sweep LO power for designed transmitter front-end

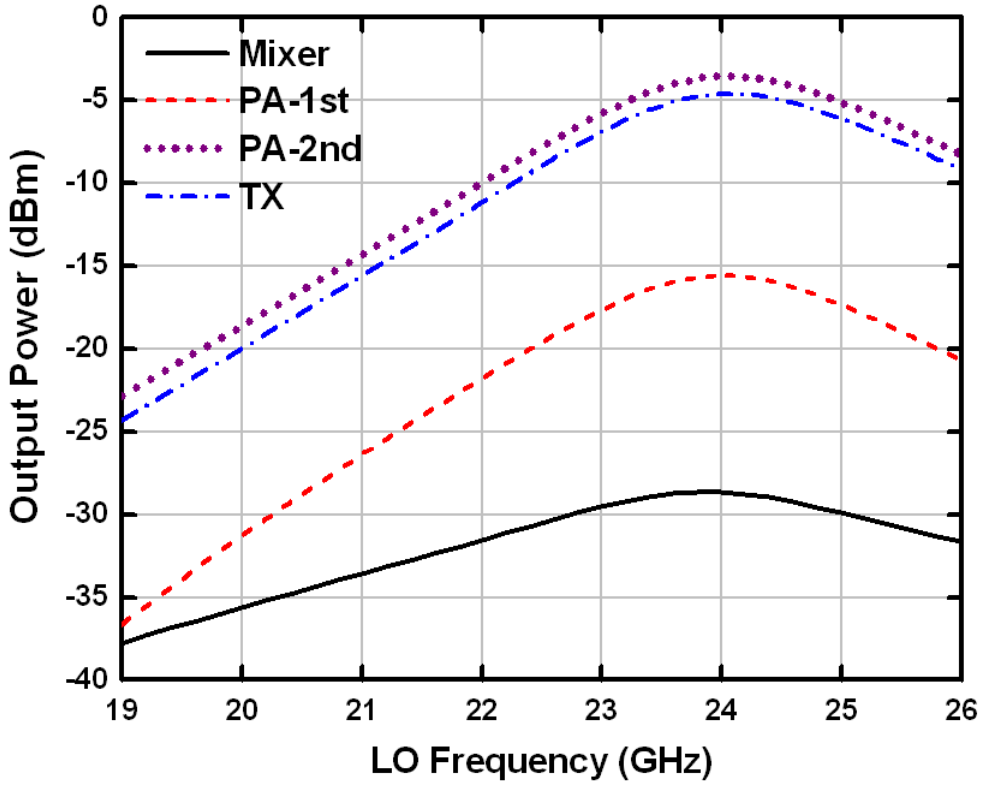


Fig. 3.42 Sweep LO frequency for designed transmitter front-end

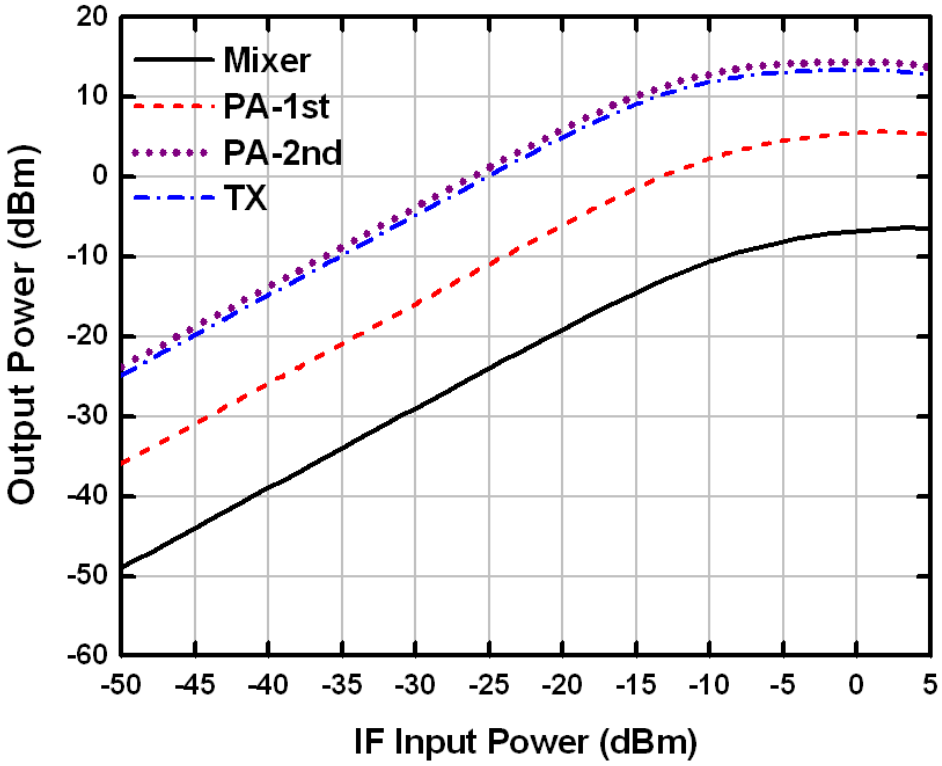


Fig. 3.43 1-tone test for designed transmitter front-end

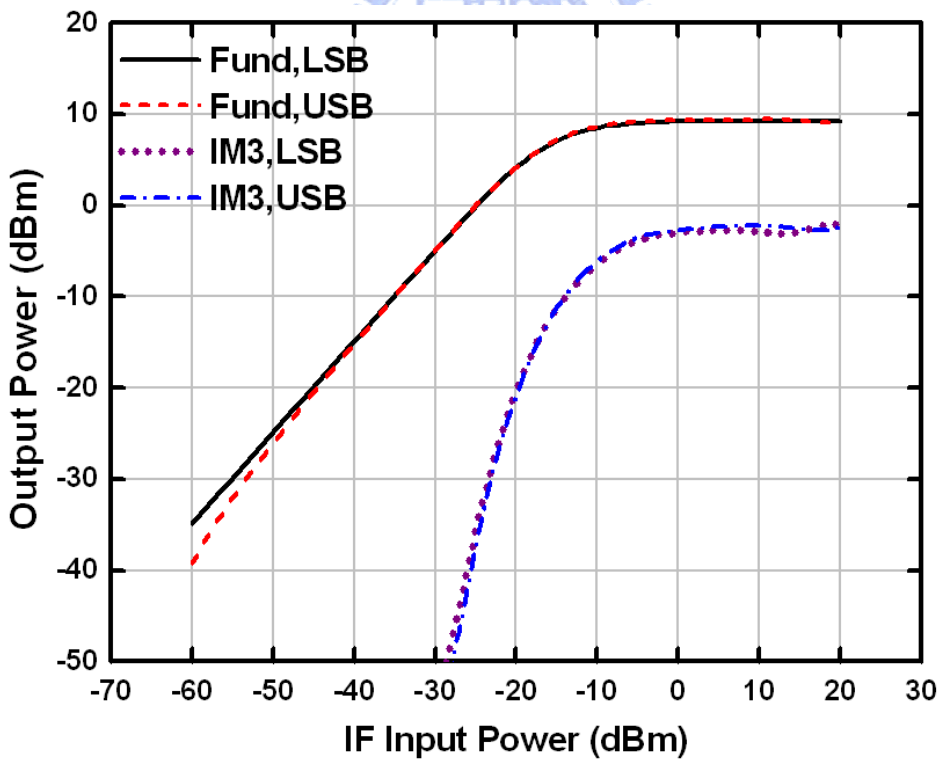


Fig. 3.44 2-tone test for designed transmitter front-end

CHAPTER 4

EXPERIMENTAL RESULTS

4.1 Chip Layout Descriptions

Because of the performance in Table 3.5 can achieve the targets. This proposed current-mode transmitter circuit is tape-out and fabricated by 0.13μm 1P8M CMOS technology. The chip microphotograph for the proposed transmitter front-end is given by Fig. 4.1 where the total chip area, including testing PADs, is 0.92 mm × 1.14 mm. The path from inductor to transistor is minimized in order to minimize impact on its quality factor. The parasitic inductance and capacitance of inevitable metal line are considered and pre-simulated in advance. Because of the differential structure of the designing mixer, symmetric style is adopted for mixer layout. The power line cell consisted of metal layers 1^{st}, 3^{rd}, 5^{th}, and 7^{th} for ground and metal layers 2^{nd}, 4^{th}, 6^{th}, and 8^{th} for V_{DD} is used in layout. These power line cells can provide power line between DC pad and core circuits and enough metal density at the same time. Besides, because the cell has bypass capacitance between each two layers, it also can provide enough bypass path between V_{DD}/bias to ground.

4.2 Measurement Setup

The measurement setup is shown in Fig. 4.2. This proposed transmitter front-end has been on-wafer measured. Two Infinite GSGSG-100 probes are used for differential signal PADs. One 6-pin DC probe card with 100-μm pitch and one 3-pin DC probe card with 150-μm pitch are used for DC PADs. Besides, because of the off-chip

components are needed at the IF input PAD, a Mini-Circuit ZFSCJ-2-1 transformer and two Anritsu V255 Bias-Tees are adopted. The S-parameter of the proposed transmitter front-end is measured by Agilent E8364B PNA. For linearity measurement, two Agilent E8257D signal generators are required for IF and LO input signal, and Agilent E4448A spectrum analyzer is used for measured output spectrum.

4.3 Experimental Results

Because the LO signal will increase the gate biases of M_2 and M_5. If mismatch occurs, the drain biases of these two transistors will be different. In this proposed current-operated self-switching mixer, mismatch will result in large I_{TH} or small I_{TH} and degrade desired signal. In order to check the mismatch, the OPAMPs are turned off and the gates of M_1 and M_4 are biased through Bias-Tees at the beginning. The figure of different DC bias versus DC current is shown in Fig. 4.3. It is obvious that this circuit does not suffer from mismatch problem.

The measured results of the proposed transmitter front-end are given by Fig. 4.4–Fig. 4.10. The S-parameter of the transmitter front-end shows in Fig, 4.4–Fig. 4.6. Near the IF, LO, and RF frequency, the S11 at 100 MHz, S22 at 23.9 GHz, and S33 at 24 GHz are –1.4 dB, –3.3 dB, and –6.3 dB, respectively. Because the center frequency drifts to 22 GHz in measured results, –2.6-dB S22 at 21.9 GHz and –15.8-dB S33 at 22 GHz has also been measured.

The measured results of sweep LO input power and input frequency are given in Fig. 4.7–Fig. 4.8 with –30-dBm, 100-MHz IF signal. The LO input power in measurement cannot larger than 15 dBm because of the equipment limitation, as shown in Fig. 4.7. By comparing with the simulation results, it is obvious that the

required LO input power is increased from 4 dBm to 9 dBm. The center frequency of the transmitter is drifted from 24 GHz to near 22 GHz.

Under this conditions, the 1-tone and 2-tone test for linearity are shown in Fig. 4.9 and Fig. 4.10, respectively. In 1-tone test, the cable loss of 2.5 dB at IF port and 4.8 dB at both LO and RF ports are calibrated already. Besides, 9-dBm, 21.9-GHz LO and 100-MHz IF are adopted for input. The measured results for 1-tone test shows that the proposed transmitter front-end has 11.5-dB power gain, –20-dBm IP_{1dB}, and –9.5-dBm OP_{1dB} shown in Fig. 4.9.

For 2-tone test, the cable loss at LO and RF ports are the same as the 1-tone test. However, because the two tones IF must be input to the transmitter, extra cables and off-chip components such as power combiner and adaptor must be used. Therefore, the total loss of IF input is increased to 9 dB. The LO input power is 9 dBm and LO input frequency is 21.9 GHz, the same as the condition in 1-tone test. The frequencies for IF are 75 MHz and 125 MHz. The measured results for 2-tone test illustrated in Fig. 4.10 shows the measured IIP3 is –5 dBm and OIP3 is 4 dBm. The summary and comparison table with other transmitter-related papers are given by Table 4.1.

4.4 Discussion

It is obvious that the measured results are quite different from the results shown in post simulation. From Table 4.1, it is clear that the degraded measurement results can not achieve the targets. The performance degradation can be categorized into three parts. One of them is the required LO input power becomes higher. Others are the degradation of the power gain and the drift of the center frequency. After re-checking

the circuit and design procedure, few mistakes are found. The detailed explanation will be introduced as follows.

The Increment of the Required LO Input Power

The Smith charts given by original post-simulation and by measurement are given by Fig. 4.11. It is clear that the Smith chart given by post-simulation is matched to near 50 ohm. However, the measured result shows that the LO input matching is located on the 50-ohm circle at the desired frequency but lacks for series capacitance. After re-check the layout of the designing transmitter, a mistake of missing capacitor has been found. This mistake comes from doing the LVS process. Because the on-chip transformer at the LO input port is re-drawn and cannot be found in the symbol provided by the TSMC, the transformer must be removed or disconnected during the LVS process. That is, this transformer and the following series capacitor were floated at that time. Nevertheless, the mistake occurred because that only the transformer had been replaced but not the following capacitor after the LVS process. The original placement of the series capacitor in schematic and layout and the difference between the LO input match with and without this capacitor are shown in Fig. 4.11. This mistake will increase the reflection at the LO input. In order to obtain the same level of LO input power in core circuit, the signal generator must be provided larger power than simulation at the LO input PAD. That is the reason why LO input power required during the measurement is much higher than that in post-simulation.

The Degradation of the Power Gain and the Frequency Drift

In general, the frequency drift comes from the parasitic effect. Because the parasitic effect had been considered for long metal line as shown in Fig. 3.30–Fig. 3.32, it is possible to underestimate the parasitic effect of other nodes. Therefore, the revised

post-simulation has been done by considering full chip EM effect and simulated by HFSS. The layout view and 3-D model in HFSS are shown in Fig. 4.12. Besides, the DC current in measurement is much lower than original one. Because this phenomenon is usually caused by higher temperature or worse corner, an infrared thermometer is used for temperature measurement. The result in Fig. 4.13 shows that the chip temperature is about 72^{o}C. According to the parameters reported by CIC, on the other hand, the circuit characteristic is SS corner. Therefore, the DC currents for different temperature and SS corner are simulated and given by Table 4.2. It is obvious that the measured DC current matches to the DC current under the conditions of SS, 75^{o}C. Thus the revised post simulation is done by setting the simulation conditions of SS, 75°C, layout mistake, and replacing each SNP file produced by EM simulation in HFSS.

Revised Post-Simulation Results

The revised simulation results, comparing with the original post-simulation results and measurement results, are shown in Fig. 4.14–Fig. 4.20. The comparison of S11, S22, and S33 are given by Fig. 4.14–Fig. 4.16. The S-parameter of revised post-simulation is similar to the measured one. The sweep LO input power and input frequency are shown in Fig. 4.17–Fig. 4.18. The required LO input power increases to 9 dBm and the center frequency drifts to 22 GHz, the same with the measured results. Comparing to the original post-simulation, it is obvious that the 1-tone and 2-tone test shown in Fig. 4.19–Fig. 4.20 of revised post-simulation results close to the measured results. The summary and comparison table are given by Table 4.3. According to the revised post-sim results, the required LO input power is the same as measured LO input power. Besides, the center frequency in revised post-sim results is also the same

as the center frequency in measurement. Although the gain of revised circuit is also degraded, it still has 4-dB difference from measured gain.

4.5 Re-Design

Because several factors such as the parasitic effect simulated by Fig. 3.30–Fig. 3.32, corner, and temperature are underestimated, the performance is quite degraded in measurement and revised post-sim results. Therefore, the purpose of the re-design circuits is to match the original targets but under the revised conditions.

Under the worse conditions, the DC current, transistor's g_m, linearity, and power gain are degraded. Therefore, not only the passive components, the dimensions of active components have to be modified to improve the performance. The components which have modified their dimensions are shown by red color in Fig. 4.21, the summary of these dimensions are given by Table 4.4.

The performance of the re-design version, including the detailed EM simulation of modified layout in Fig. 4.22, SS or TT corner, and 75^{o}C temperature, are simulated. The results of re-design version, comparing with original targets and revised post-sim results, are shown in Fig. 4.23–Fig. 4.36.

The S-parameter shown in Fig. 4.23–Fig. 4.25 express the S-parameter of re-design is similar to original one except S33. S33 comes from the output of the power amplifier and determines by the load-pull analysis. Because the sizes of the transistors in 2-stage PA have been rearrange, the optimized load impedance determined by load-pull is different from original one. It is obvious that the required LO input power and frequency in Fig. 4.26–Fig. 4.27 are equal to the original design.

The 1-tone and 2-tone tests, given by Fig. 4.28–Fig. 4.29, show that the power gain and the linearity of the re-design are almost the same as the original.

The performances under the TT corner, 75°C temperature also have been simulated and expressed by Fig. 4.30–Fig. 4.36. Because the DC currents are larger than the DC current in SS corner, the results are almost the same with the SS corner except the power gain and saturated output power. The performances for all corners are shown in Fig. 4.37–Fig. 4.43.

The summary and the comparisons are given in Table 4.5 and Table 4.6. Comparing to other voltage-mode power amplifier in Table 4.5, it shows the proposed current-mode power amplifier has better OP_{1dB} and OIP3 under lower supply voltage. Comparing to other voltage-mode transmitter circuits in Table 4.6, the proposed transmitter front-end circuit has lower supply voltage. Although the total power consumption is larger than other works, this proposed transmitter front-end can deliver 16.8-dBm output power, which is quite larger than others. Under the same output power level, therefore, this proposed current-mode transmitter can have lower power consumption than voltage-mode transmitter circuits.

From the original design, the V_{REF} is chosen for maximizing conversion gain. For transmitter front-end circuits, however, the signal comes from base station and can be large. Thus the mixers' conversion gain in transmitter is not necessary to be very large. On the other hand, however, the linearity requirement is strict. From Fig. 4.44 and Table 4.7, it is obvious that the 0.6-V V_{REF} can obtain maximized conversion gain and the 0.4-V V_{REF} can have best OP_{1dB}. Therefore, the 0.4-V V_{REF} should be chosen for designing up-conversion mixer in the future.

The 1-tone test by different LO input power of proposed transmitter front-end is shown in Fig. 4.45. For small IF level, 4-dBm LO input power has maximal conversion gain. It is also the original design consideration. For large IF level, however, 6-dBm or even 8-dBm can deliver higher output power. Considering the real case in transmitter front-end, the large IF signal should be adopted and resultant large LO input power should be chosen in the future.

Table 4.1 Summary of measurement results

		Post-Sim (Original)	Measurement	Targets
Technology		**0.13-μm CMOS**		**-**
Methodology		**Current-Mode**		**-**
Supply Voltage (V)		**1.2**		**-**
IF (GHz)		**0.1**	**0.1**	**0.1**
LO (GHz)		**23.9**	**21.9**	**23.9**
RF (GHz)		**24**	**22**	**24**
Power (mW)	**Mixer**	**18.8**	**7.3**	**-**
	Power Amplifier	**311.7**	**231.1**	**-**
	Total	**330.5**	**238.4**	**-**
TX Front-End	**S11 / S22 / S33 (dB)**	**–8.9 / –16.4 / –9.5**	**–1.4 / –2.6 / –15.8**	**-**
	Gain (dB)	**25.2**	**11.5**	**>20**
	OP_{1dB} / IP_{1dB} (dBm)	**9.1 / –15**	**–9.5 / –20**	**-**
	P_{OIP3} / P_{IIP3} (dBm)	**20 / –5**	**4 / –5**	**-**
	Max. P_{OUT} (dBm)	**14.4**	**–2.5**	**>10**

Table 4.2 DC consumption for different corners and temperatures

	I_{VDD} (mA)	I_{VDPA1} (mA)	I_{VDPA2} (mA)	I_{VDPA3} (mA)
TT, 25°C	**15.26**	**1.04**	**58.1**	**201**
SS, 25°C	**5.72**	**0.616**	**48.9**	**169**
SS, 50°C	**5.58**	**0.605**	**47.4**	**164**
SS, 75°C	**5.42**	**0.6**	**46**	**159**
SS, 100°C	**5.22**	**0.599**	**44.6**	**154**
Measurement	**5.3**	**0.84**	**45**	**147**

Table 4.3 Summary of revised post-sim results

		Post-Sim (Original)	Measurement	Post-Sim (Revised)	Targets
IF (GHz)		0.1	0.1	0.1	0.1
LO (GHz)		23.9	21.9	21.9	23.9
RF (GHz)		24	22	22	24
Power (mW)	Mixer	18.8	7.3	6.9	-
	Power Amplifier	311.7	231.1	246.6	-
	Total	330.5	238.4	253.5	-
TX Front-End	S11 / S22 / S33 (dB)	–8.9 / –16.4 / –9.5	–1.4 / –2.6 / –15.8	–13.2 / –2.3 / –5.4	-
	Gain (dB)	25.2	11.5	15.5	>20
	OP_{1dB} / IP_{1dB} (dBm)	9.1 / –15	–9.5 / –20	–0.5 / –15	-
	P_{OIP3} / P_{IIP3} (dBm)	20 / –5	4 / –5	9 / –5	-
	Max. P_{OUT} (dBm)	14.4	–2.5	7.1	>10

Table 4.4 Dimensions summary of the re-design version

	Dimension (μm)
M_1	2.5*28/0.13 → 2.5*40/0.13
M_2	2.5*12/0.13 → 2.4*14/0.13
M_8	2.5*20*2/0.13 → 2.5*20*3/0.13
$M_{OP,P1-2}$	2*2/0.13 → 1.5*2/0.13

	Value
L_{34}	215 pH → 69 pH
L_5	215 pH → 67 pH
L_7	1.24 nH → 563 pH
L_9	104 pH → 128 pH

	Value
C_3	88 fF → 79 fF
C_6	431 fF → 399 fF

Table 4.5 Comparison with voltage-mode power amplifier

	Post-Sim (Revised)	Post-Sim (Re-Design)		[6] *JSSC 2005*
Technoogy	**0.13-μm CMOS**			**0.18-μm CMOS**
Methodology	**Current-Mode**			**Voltage-Mode**
Topology	**2-Stage Current Mirror Amplifier**			**2-Stage Cascode Common-Source Amplifier**
Supply Voltage (V)	**1.2**			**2.8**
Conditions	**SS, 75°C**	**SS, 75°C**	**TT, 75°C**	**-**
Power Consumption	**246.6**	**294.3**	**349.9**	**280**
Gain (dB)	**16.6**	**22**	**22.1**	**6**
OP_{1dB} (dBm)	**12.7**	**11.9**	**14.1**	**11**
P_{OIP3} (dBm)	**23**	**22**	**24**	**14**
PAE@P_{1dB} (%)	**7.8**	**5.5**	**7.9**	**-**
Peak PAE (%)	**19.6**	**22.9**	**23.9**	**6.5**
Max. P_{OUT} (dBm)	**16.6**	**16.6**	**17.1**	**14.5**

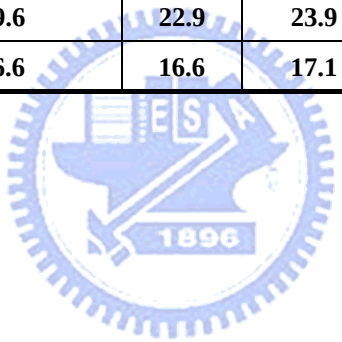


Table 4.6 Comparison with voltage-mode transmitter circuits

		Post-Sim (Revised)	Post-Sim (Re-Design)		[23] *RFIC Symp. 2005*	[24] *JSSC 2008*
Technoogy		**0.13-μm CMOS**			**0.13-μm CMOS**	**0.13-μm CMOS**
Methodology		**Current-Mode**			**Voltage-Mode**	**Voltage-Mode**
Topology		**Self-Switching Mixer + 2-Stage Current Mirror Amplifier**			**Double-Balanced Gilbert Mixer + 2-Stage Fully Differential Pre-Amp**	**Double-Balanced Gilbert Mixer + 4-Stage Fully Differential Cascode CS Pre-Amp + Differential Class-E PA**
Supply Voltage (V)		**1.2**			**1.5**	**1.2 and 1.5**
Conditions		**SS, 75°C**	**SS, 75°C**	**TT, 75°C**	**-**	**-**
IF (GHz)		**0.1**	**0.1**	**0.1**	**3.4**	**3.4**
LO (GHz)		**21.9**	**23.9**	**23.9**	**13.6**	**13.6**
RF (GHz)		**22**	**24**	**24**	**17**	**24**
Power (mW)	**Mixer**	**6.9**	**20.1**	**26.9**	**18**	**-**
	Power Amplifier	**246.6**	**294.3**	**349.9**	**75**	**-**
	Total	**253.5**	**314.4**	**376.8**	**93**	**118**
TX Front-End	**S11 / S22 / S33 (dB)**	**–13.2 / –2.3 / –5.4**	**–5.7 / –13.3 / –13.7**	**–3.3 / –13.1 / –14.1**	**-**	**-**
	Gain (dB)	**15.5**	**25.2**	**26**	**4**	**-**
	OP_{1dB} (dBm)	**–0.5**	**7.2**	**10**	**4.2**	**-**
	P_{OIP3} (dBm)	**9**	**15**	**23**	**13**	**-**
	Max. P_{OUT} (dBm)	**7.1**	**14.3**	**16.8**	**-**	**7**
Chip Area (mm^2)		**1.05**			**0.5**	**2.2**

Table 4.7 Summary table of V_{REF} versus mixer performance

V_{REF} (V)	0.3	0.4	0.5	0.6	0.7
Gain (dB)	–3	–2.3	–0.5	1.7	–0.3
IP_{1dB} (dBm)	2.9	2.9	–2.9	–12.9	–11.4
OP_{1dB} (dBm)	–0.8	–0.3	–4.2	–12.1	–12.8

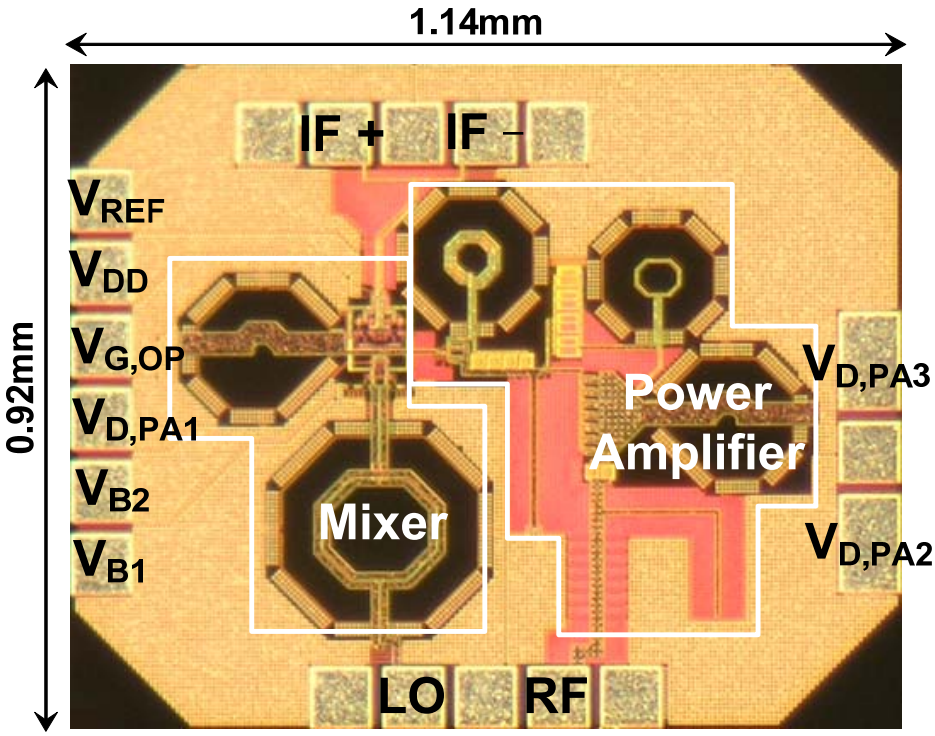


Fig. 4.1 Chip microphotograph of the proposed transmitter front-end

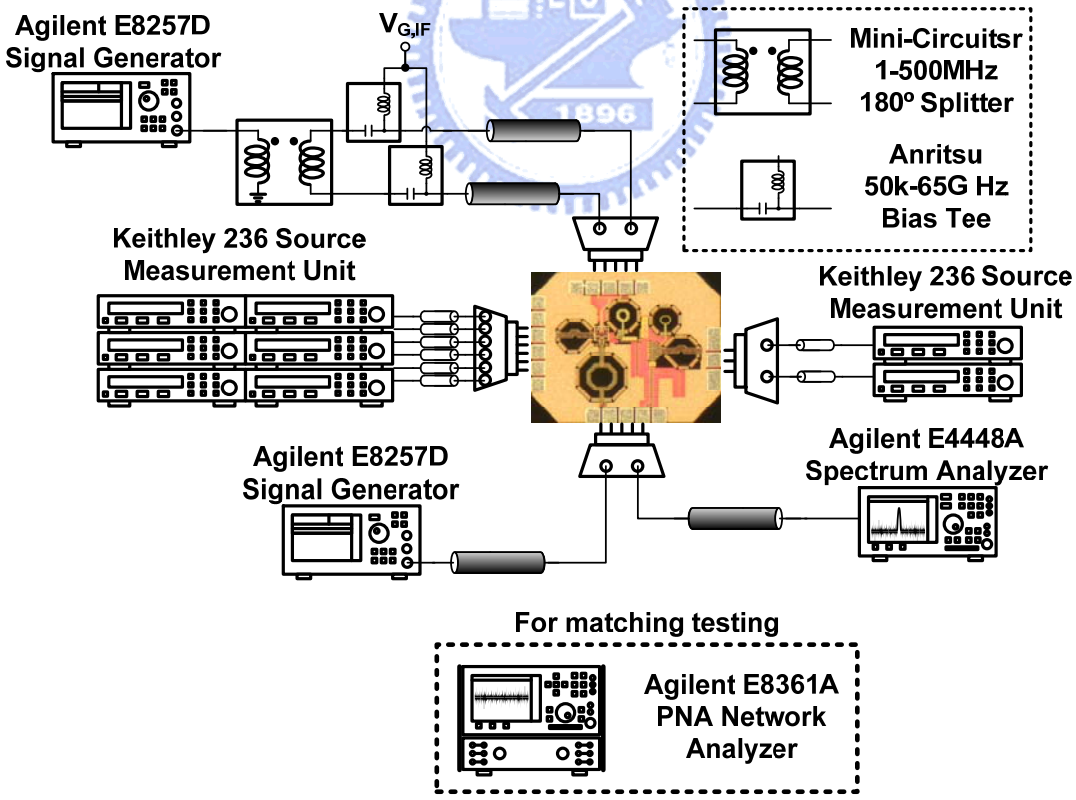


Fig. 4.2 Measurement setup for the proposed transmitter front-end

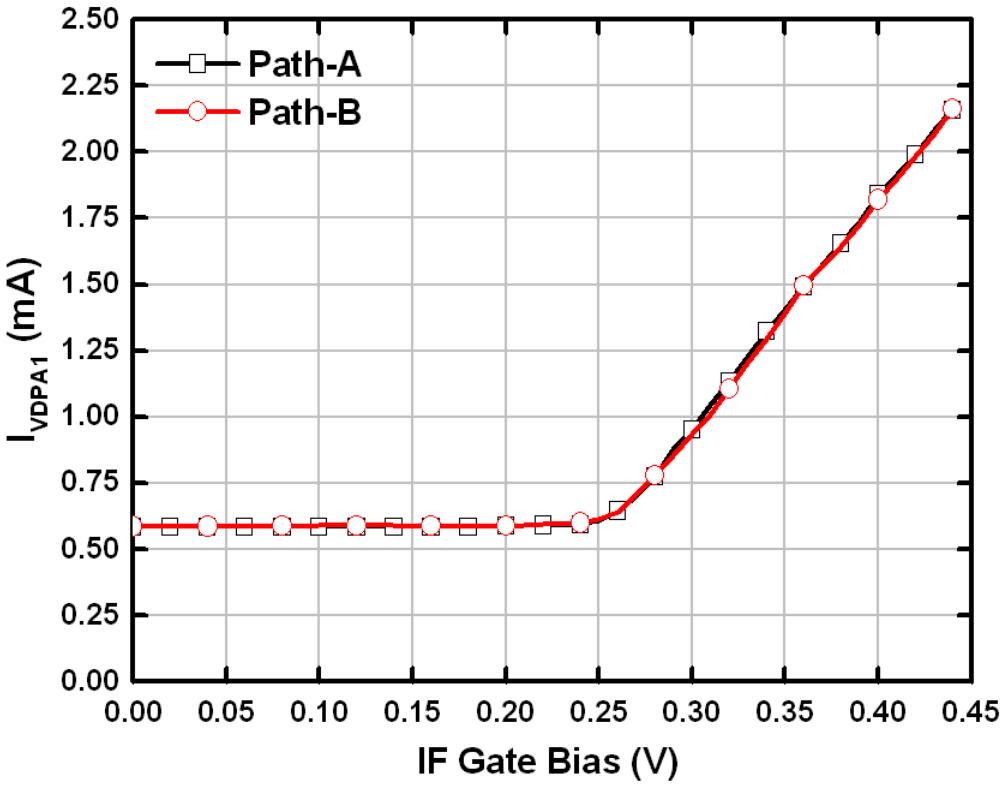


Fig. 4.3 Sweep IF gate bias through Bias-Tees for checking mismatch

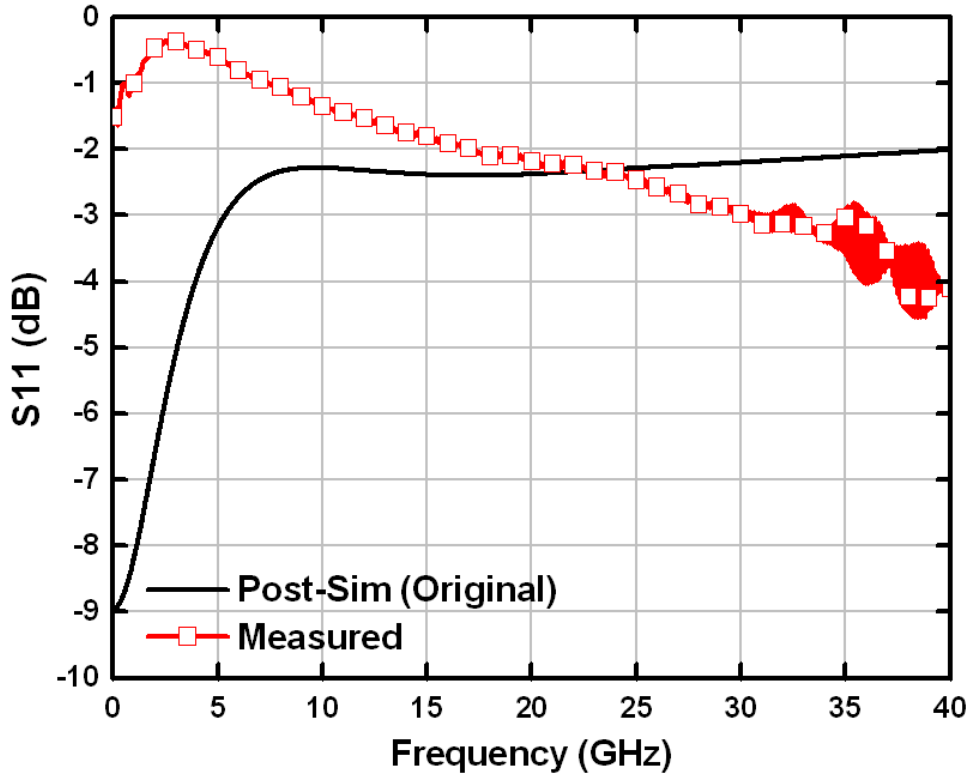


Fig. 4.4 Measured S11 of proposed transmitter front-end

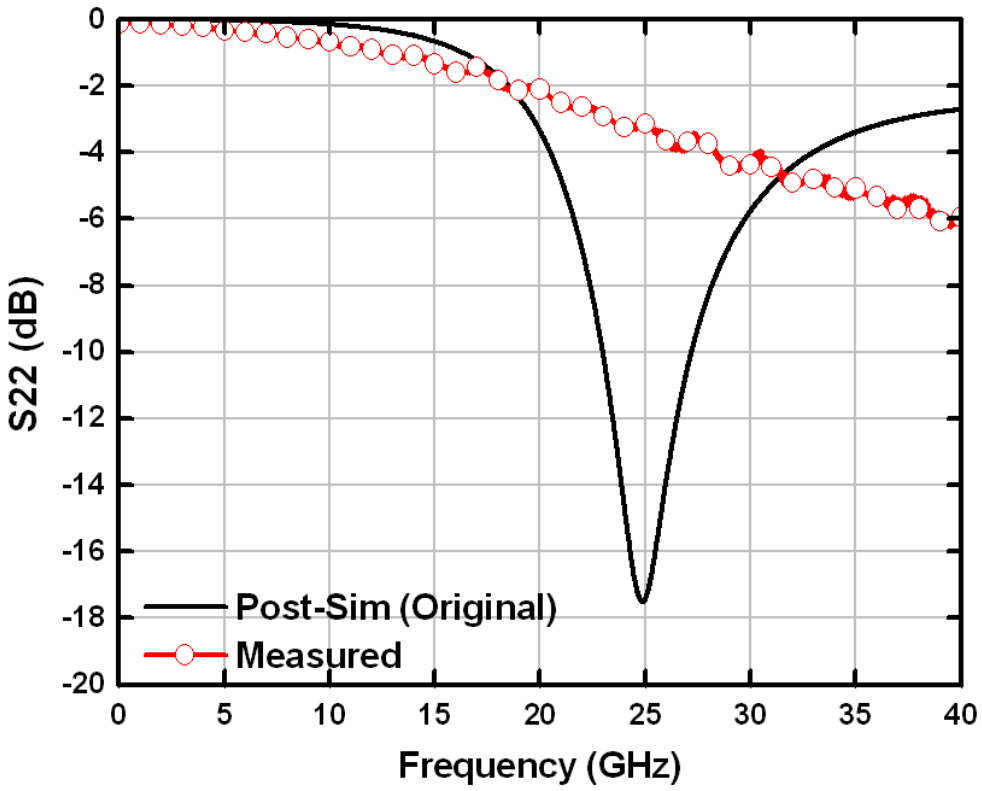


Fig. 4.5 Measured S22 of proposed transmitter front-end

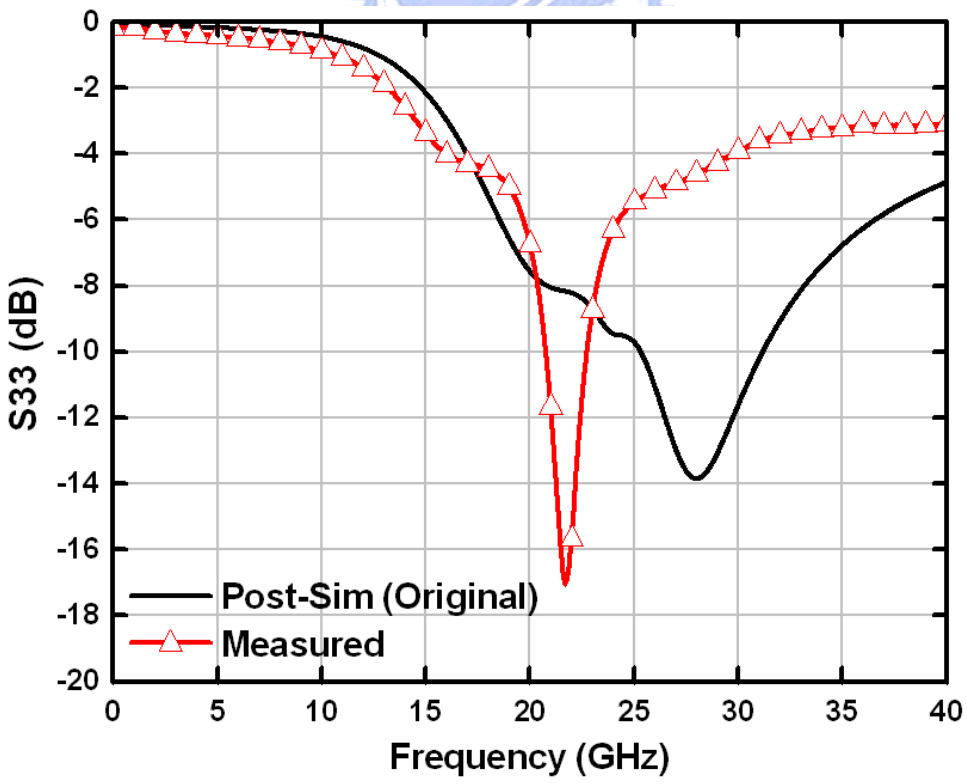


Fig. 4.6 Measured S33 of proposed transmitter front-end

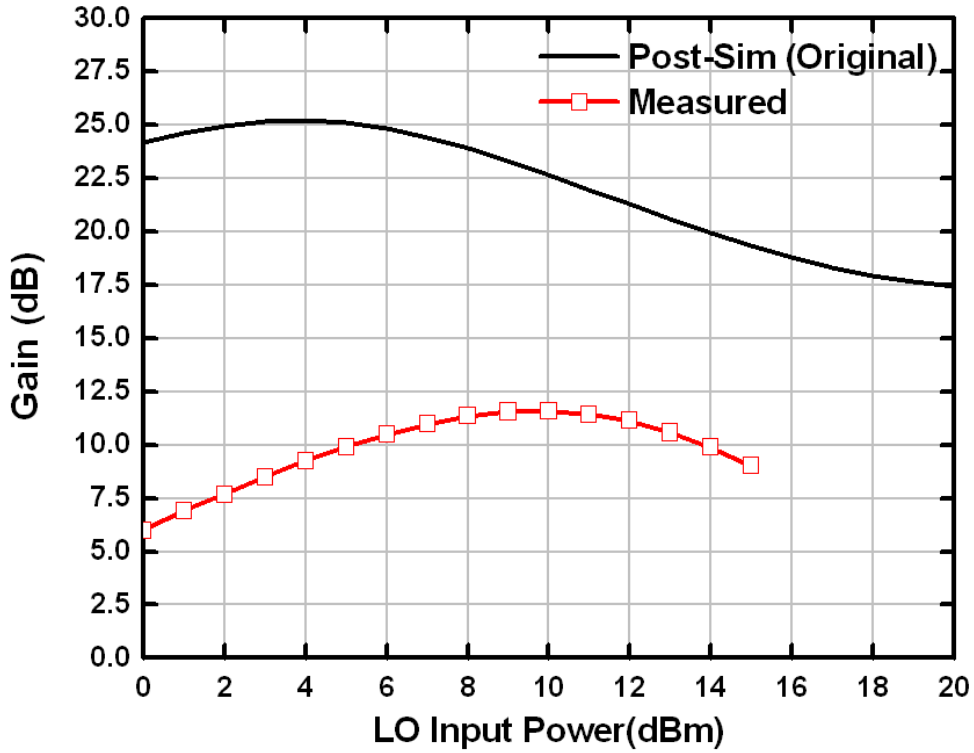


Fig. 4.7 Measured gain versus LO input power for proposed transmitter front-end

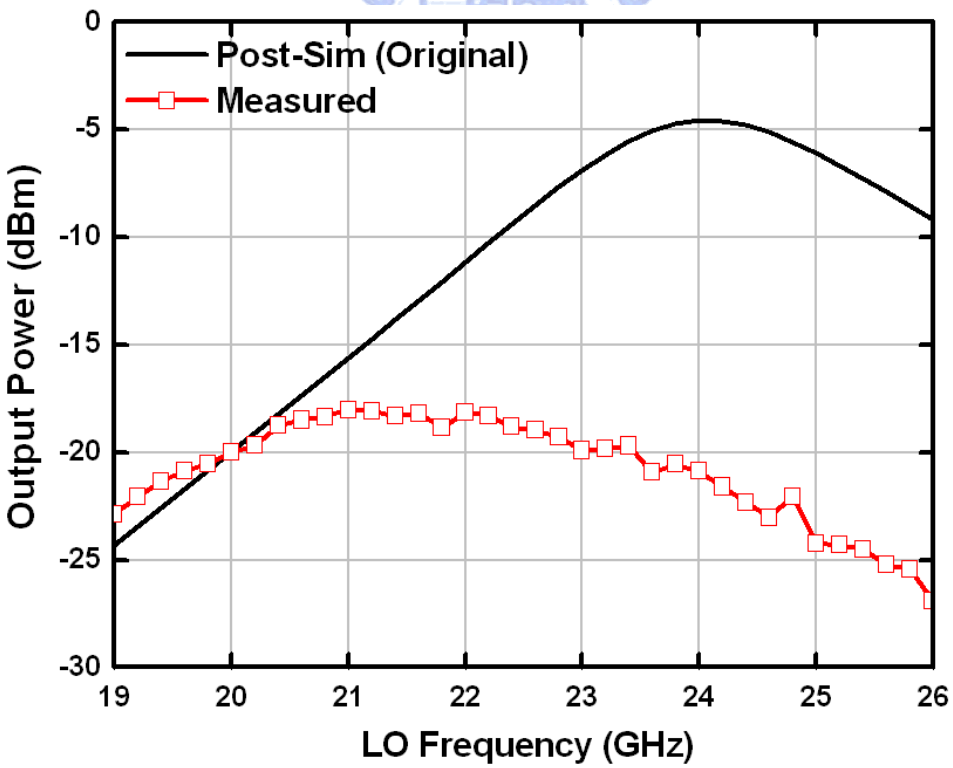


Fig. 4.8 Measured output power versus LO input frequency for proposed transmitter front-end

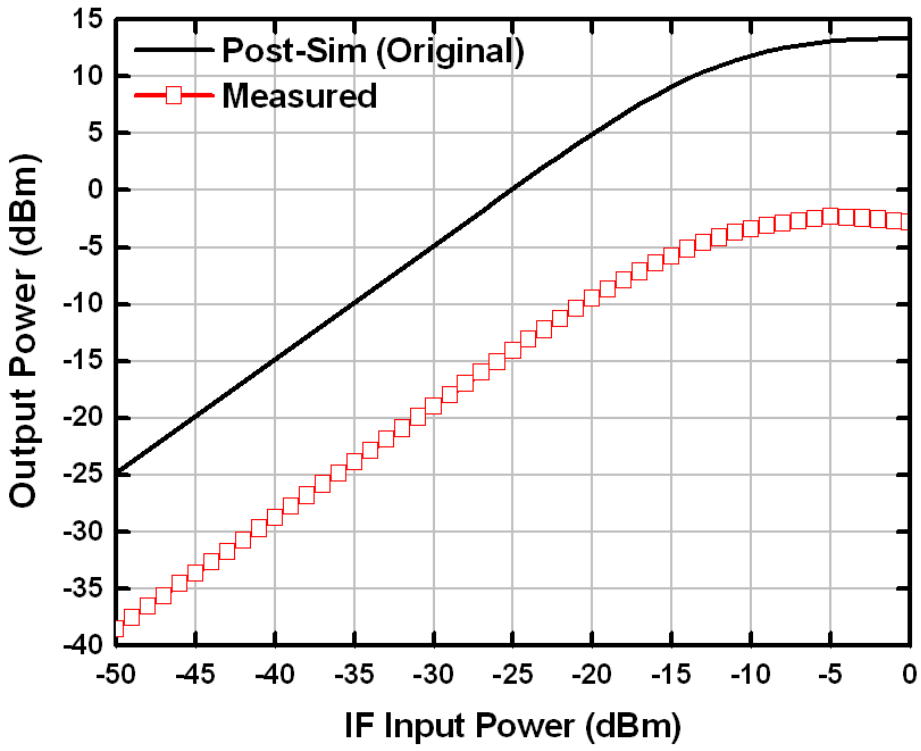


Fig. 4.9 Measured output power versus IF input power (1-tone) for proposed transmitter front-end

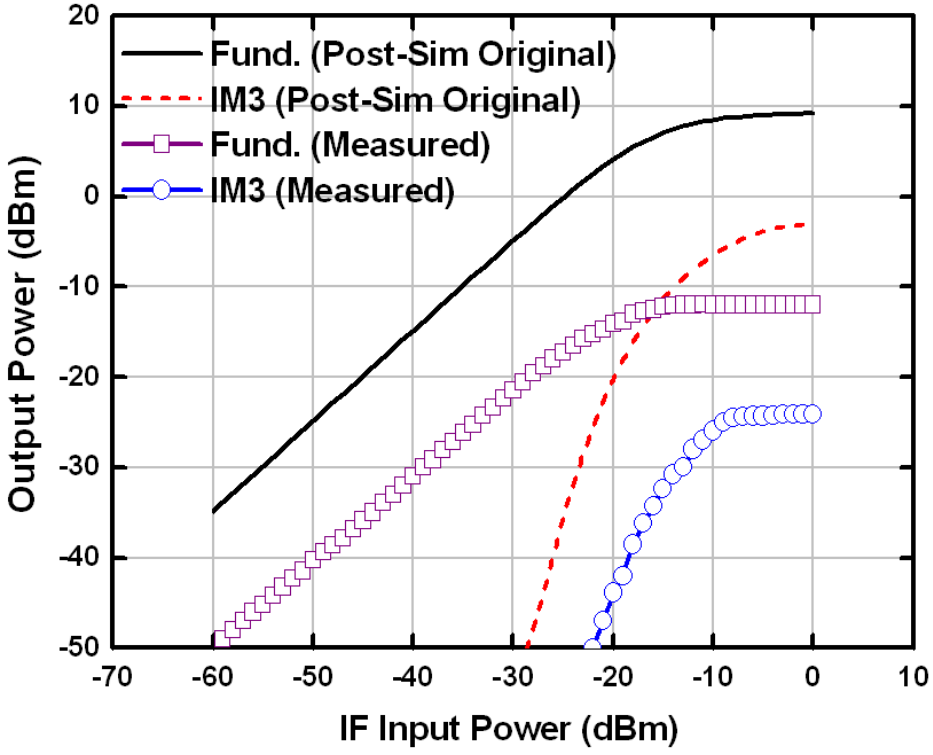


Fig. 4.10 Measured output power versus IF input power (2-tone) for proposed transmitter front-end

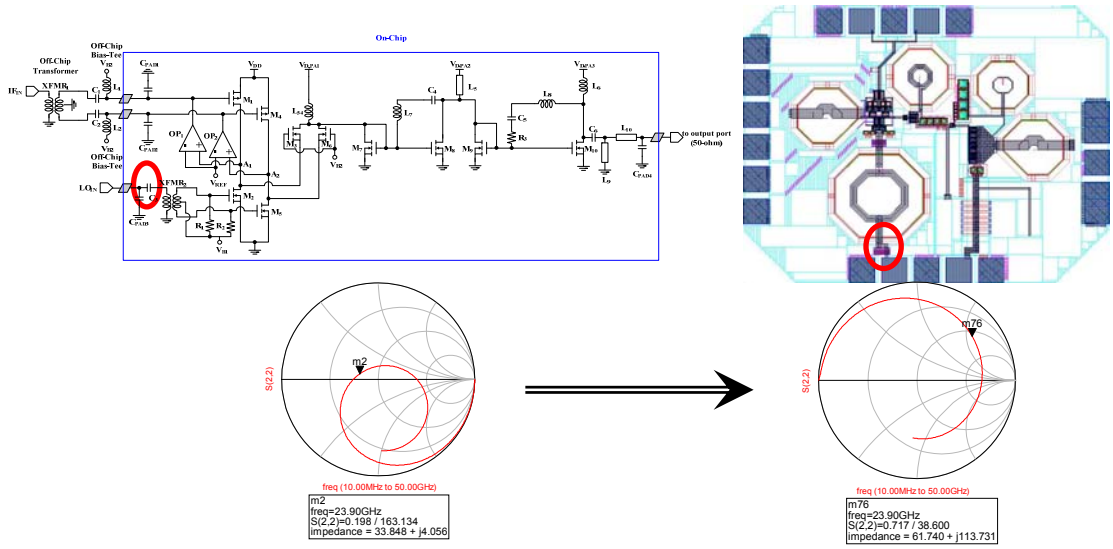


Fig. 4.11 Missing capacitor and the effect in terms of Smith chart

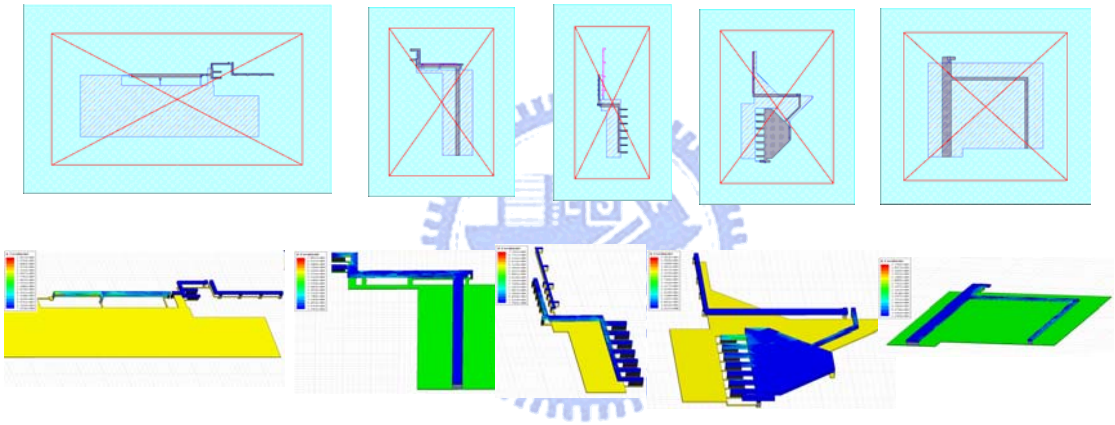


Fig. 4.12 Layout view and 3-D model in HFSS for revised post-simulation

Fig. 4.13 Temperature measurement

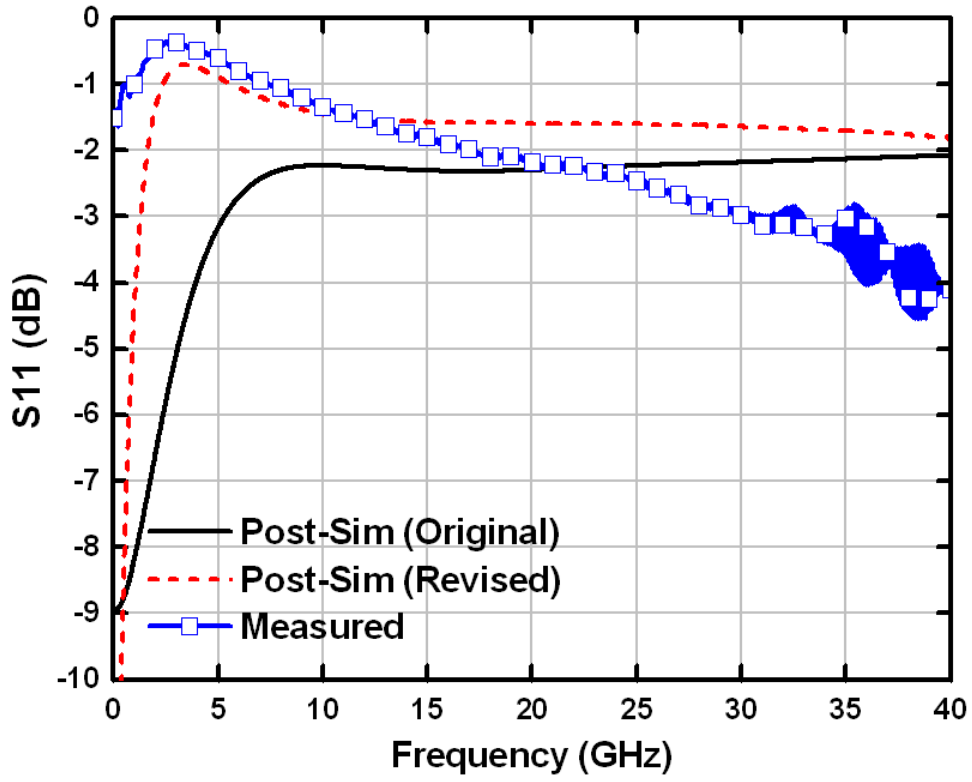


Fig. 4.14 S11 of revised post-sim comparing with original post-sim and measurement

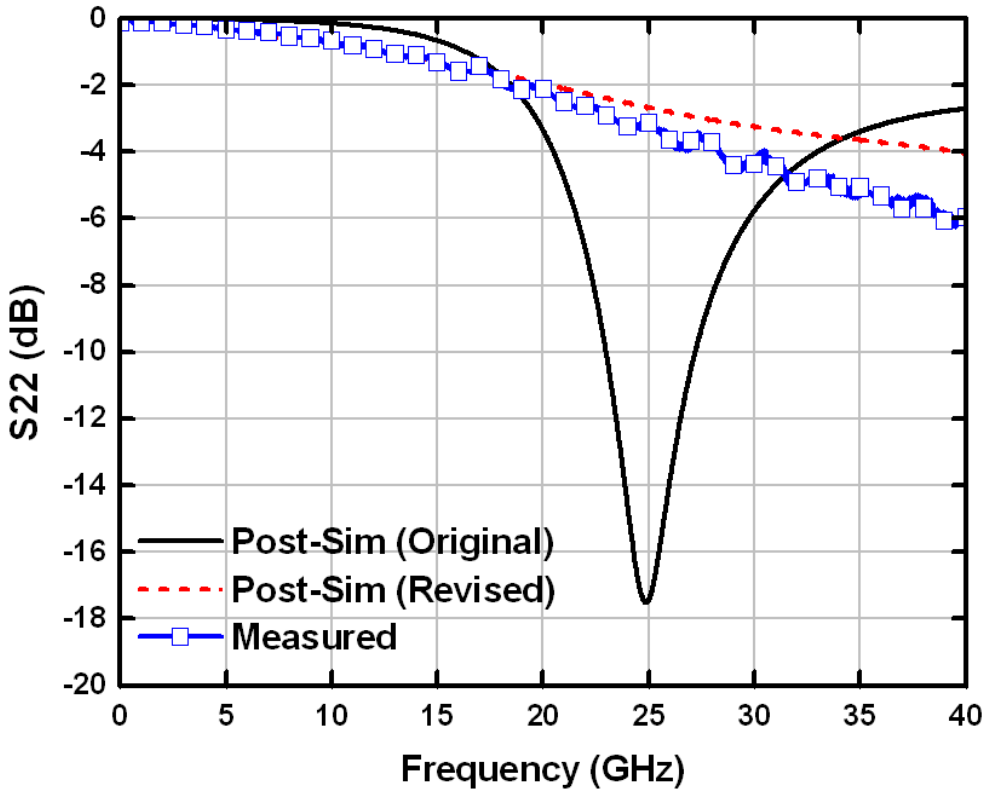


Fig. 4.15 S22 of revised post-sim comparing with original post-sim and measurement

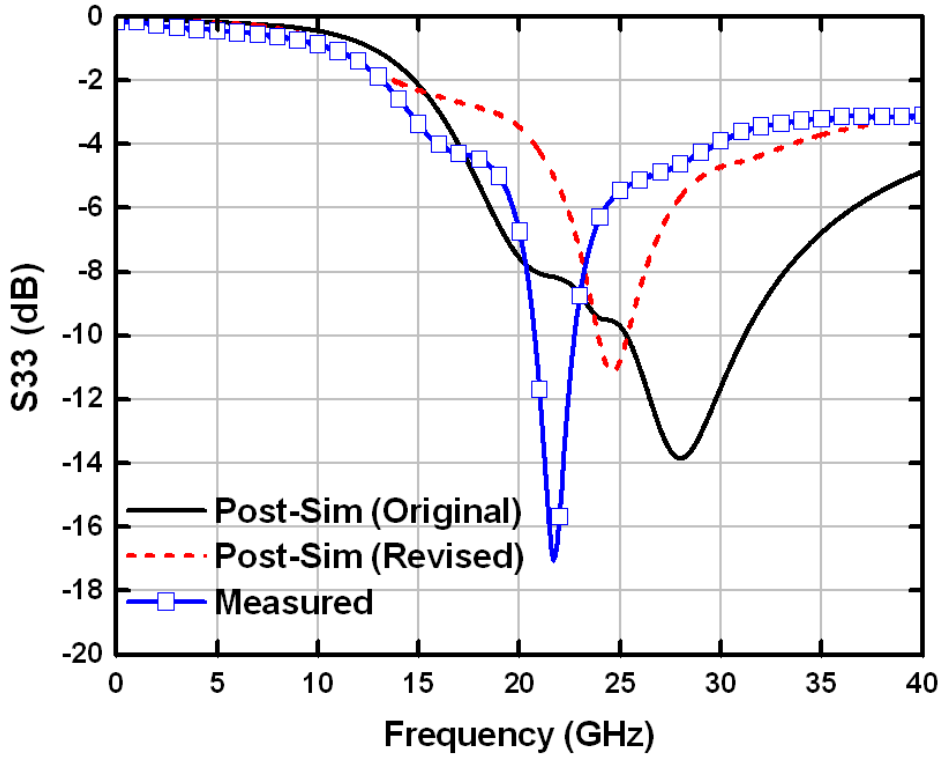


Fig. 4.16 S33 of revised post-sim comparing with original post-sim and measurement

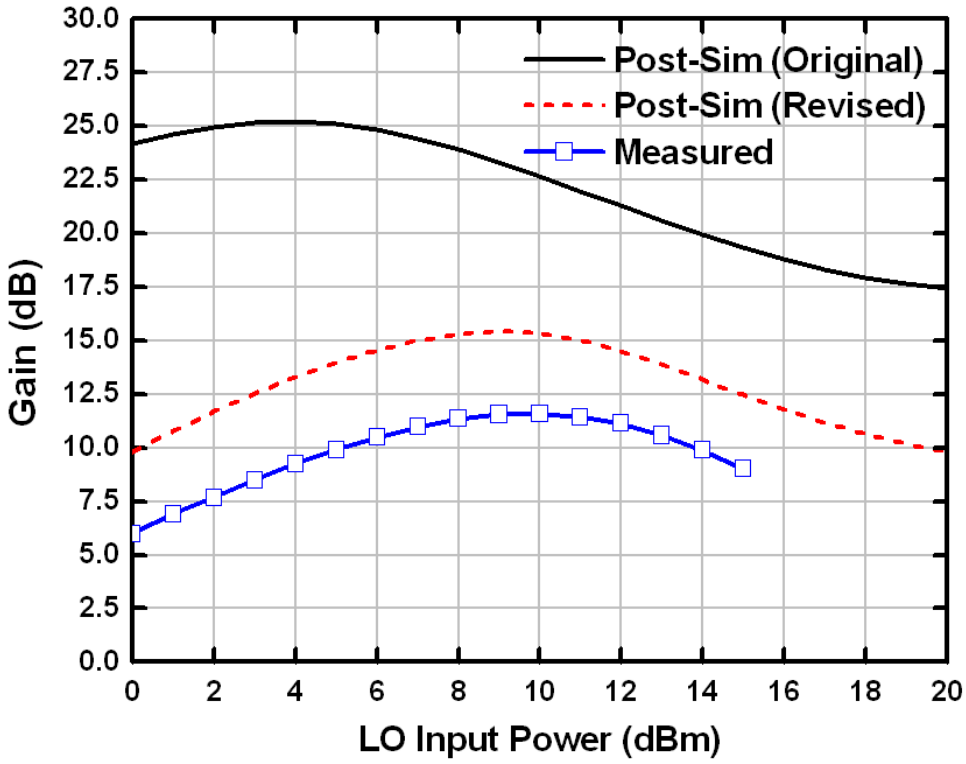


Fig. 4.17 Sweep LO power of revised post-sim comparing with original post-sim and measurement

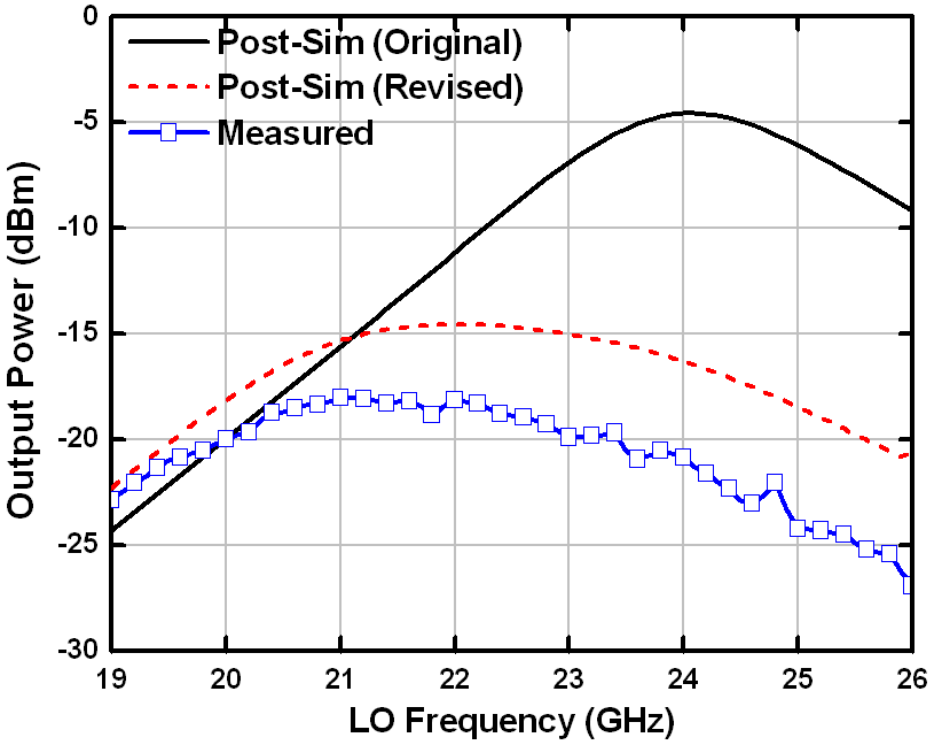


Fig. 4.18 Sweep LO frequency of revised post-sim comparing with original post-sim and measurement

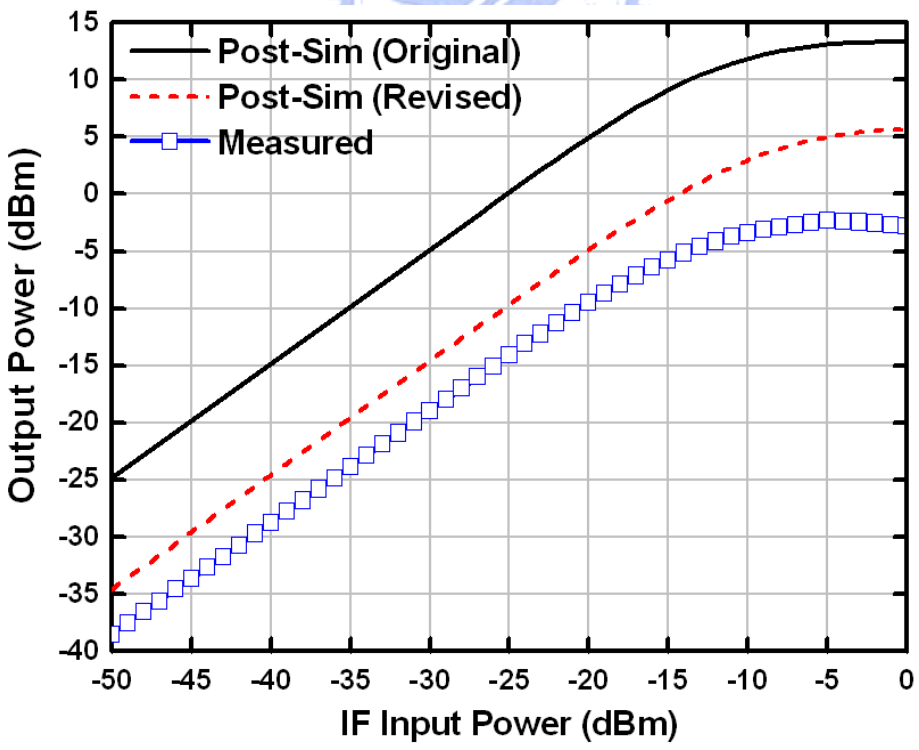


Fig. 4.19 1-tone test of revised post-sim comparing with original post-sim and measurement

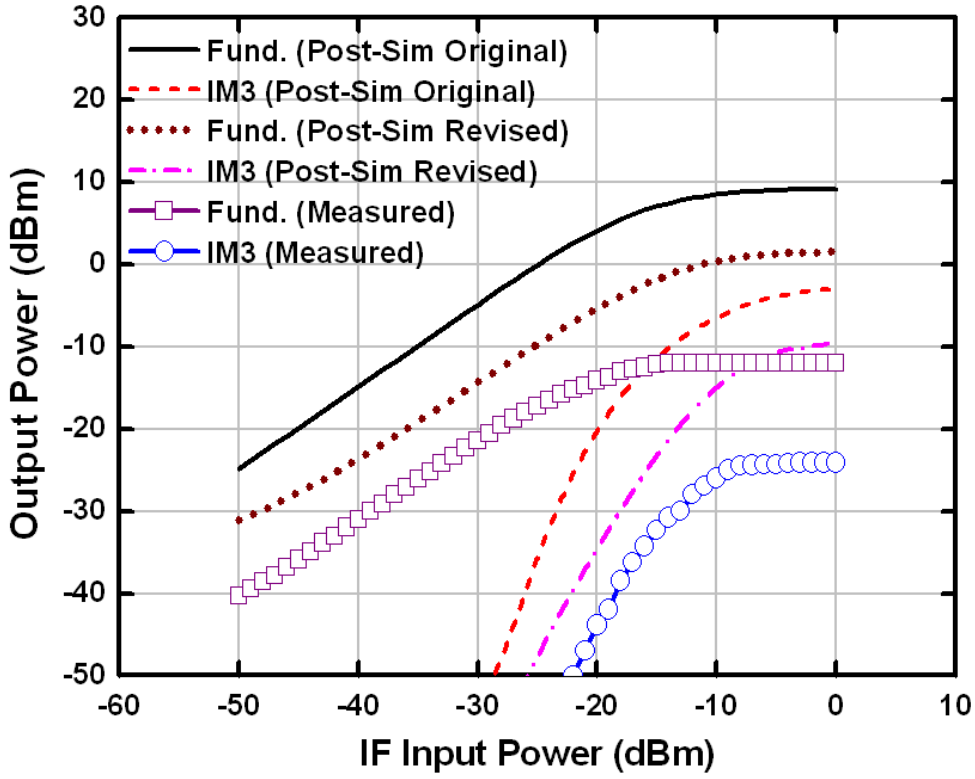


Fig. 4.20 2-tone test of revised post-sim comparing with original post-sim and measurement

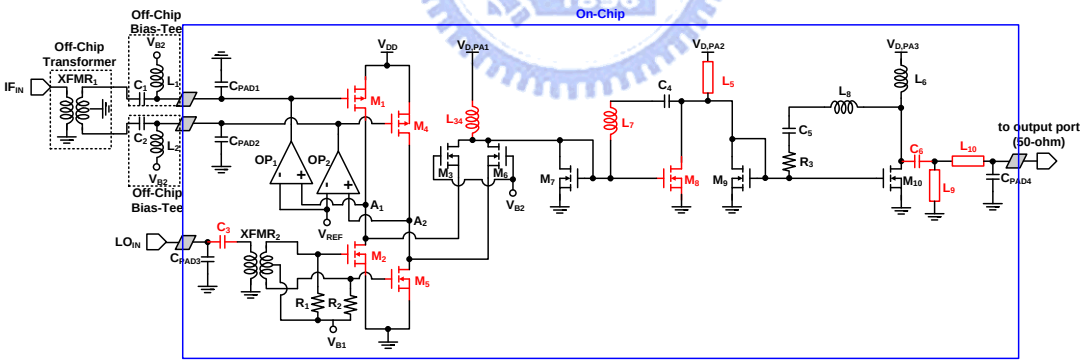


Fig. 4.21 Change components' dimensions for re-design

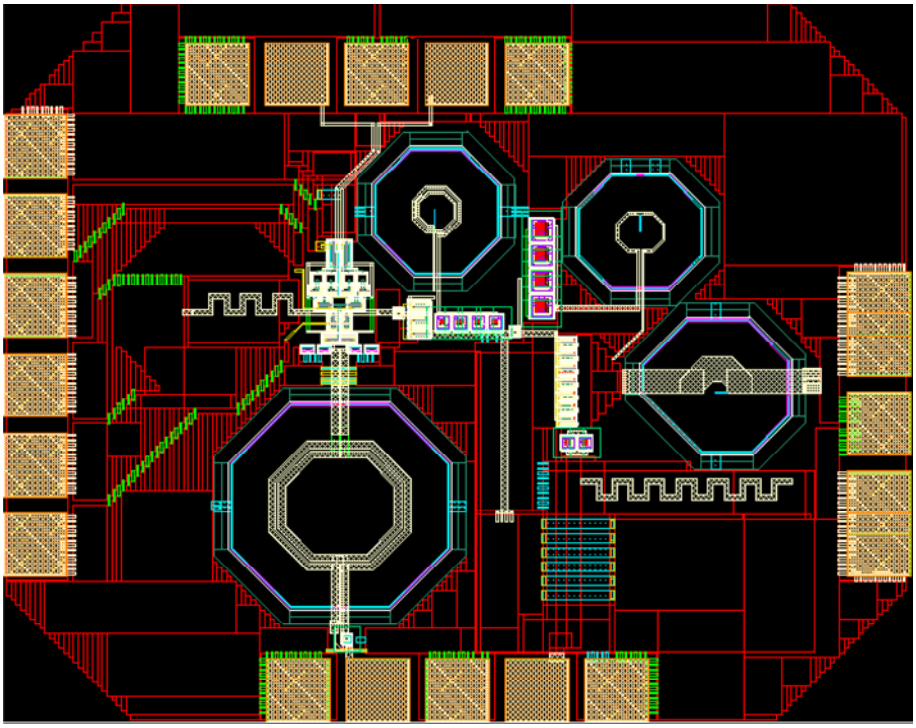


Fig. 4.22 The modified layout for re-design transmitter

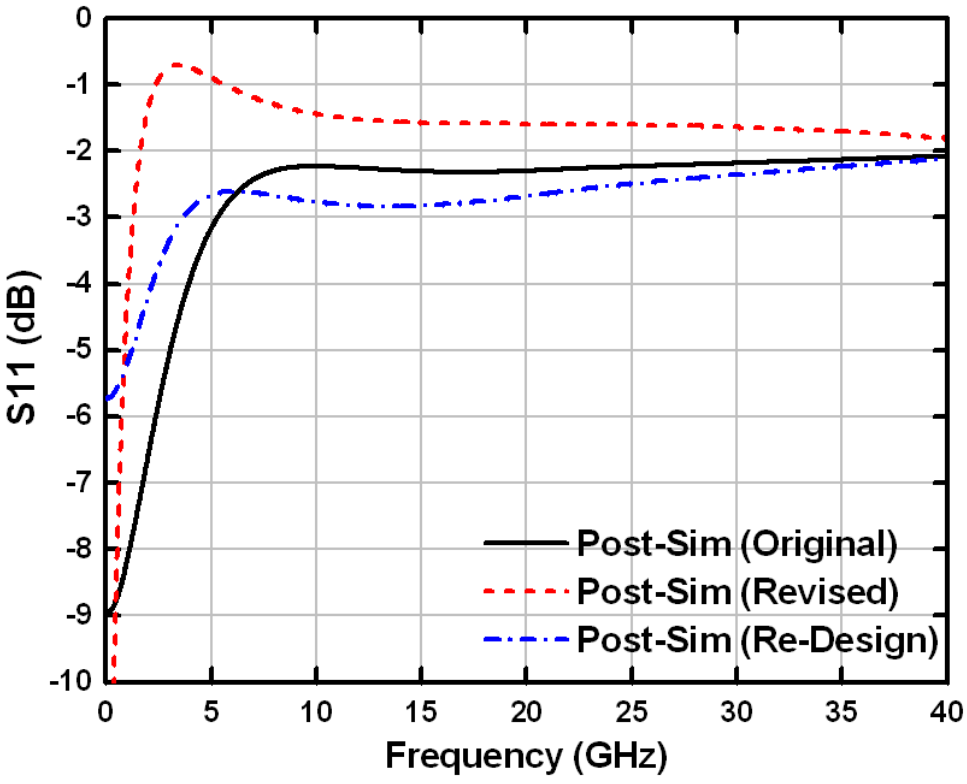


Fig. 4.23 S11 of re-design (SS, 75°C) comparing with original and revised post-sim

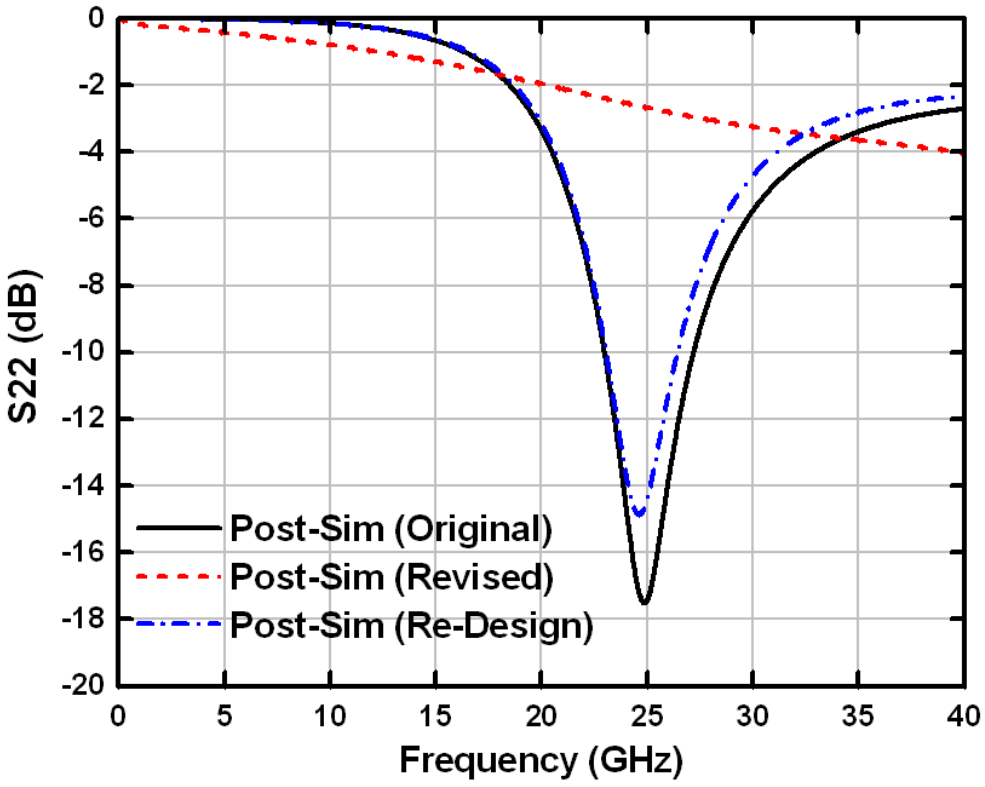


Fig. 4.24 S22 of re-design (SS, 75°C) comparing with original and revised post-sim

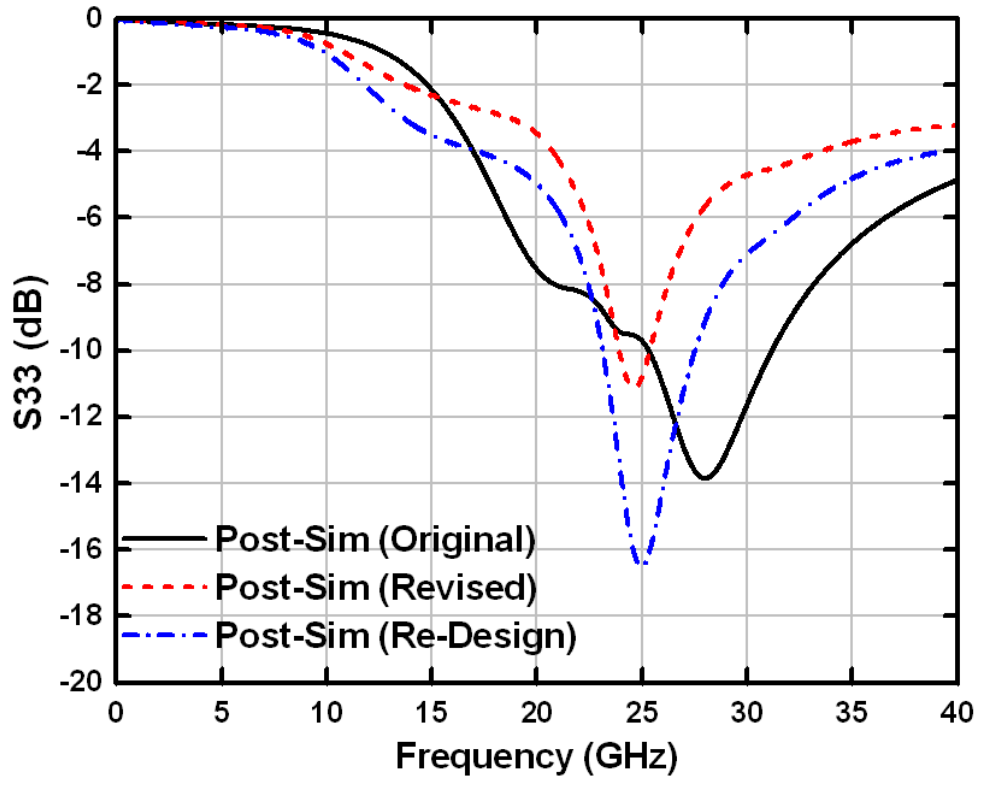


Fig. 4.25 S33 of re-design (SS, 75°C) comparing with original and revised post-sim

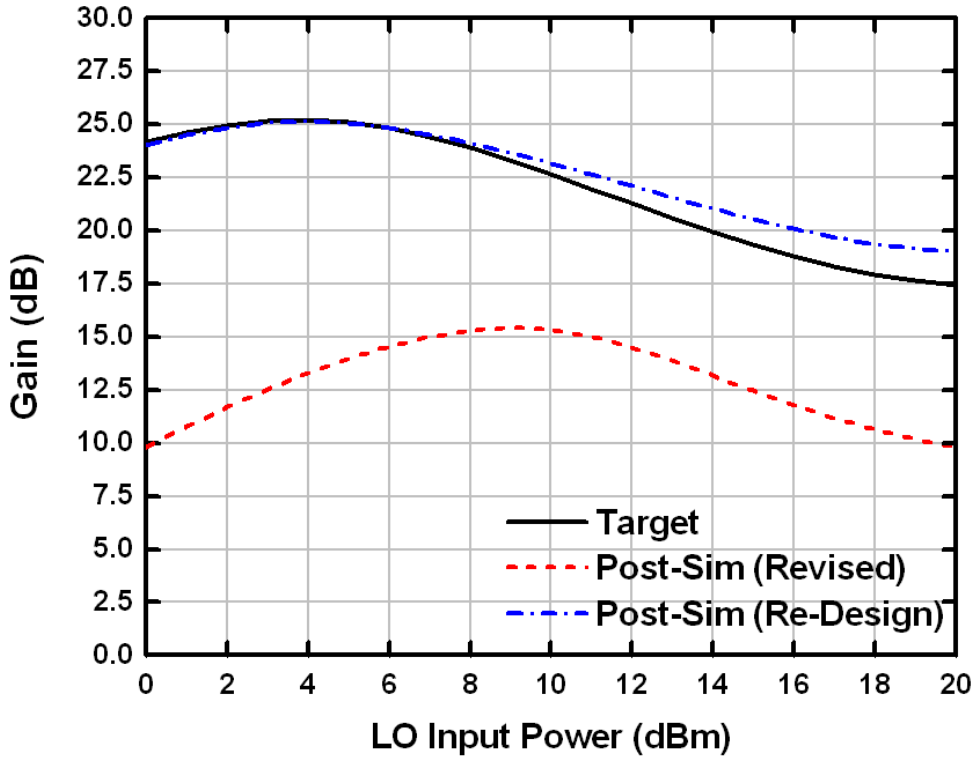


Fig. 4.26 Sweep LO power of re-design (SS, 75°C) comparing with original and revised post-sim

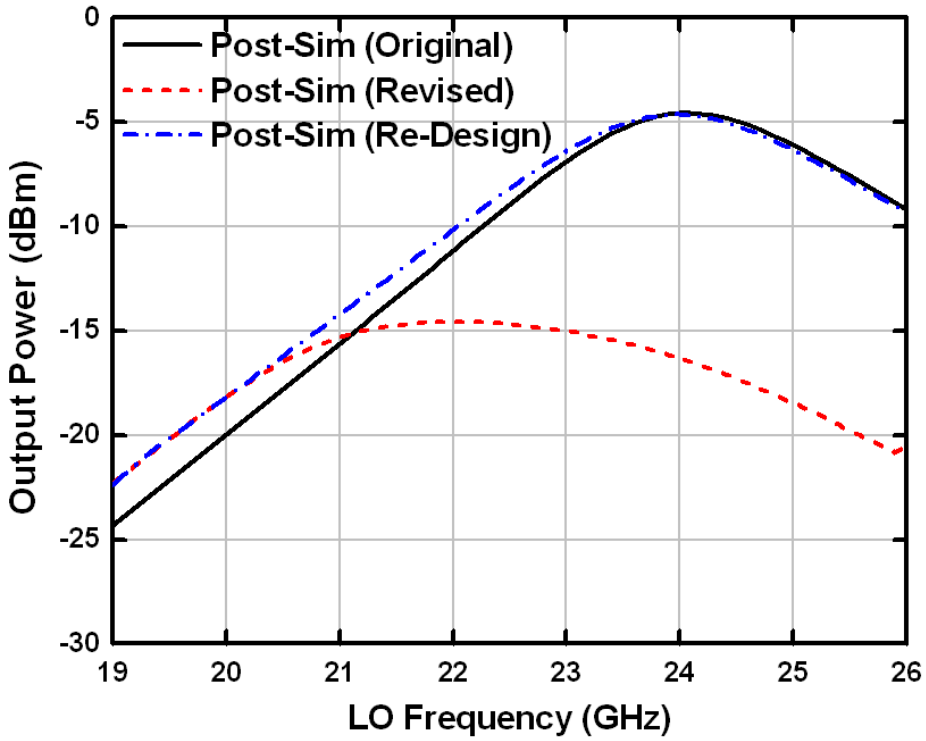


Fig. 4.27 Sweep LO frequency of re-design (SS, 75oC) comparing with original and revised post-sim

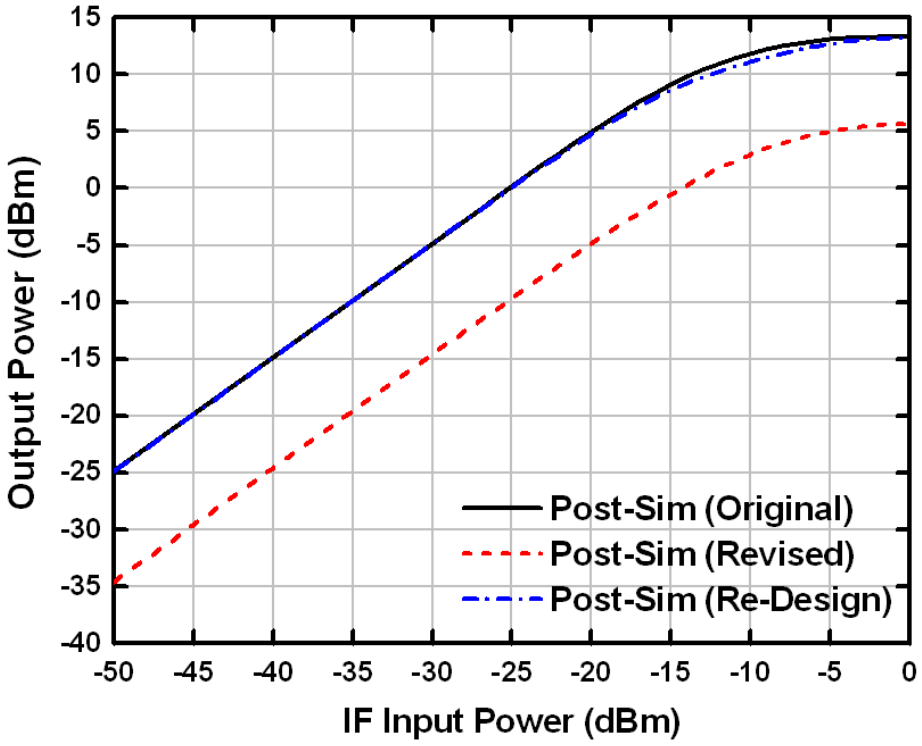


Fig. 4.28 1-tone test of re-design (SS, 75°C) comparing with original and revised post-sim

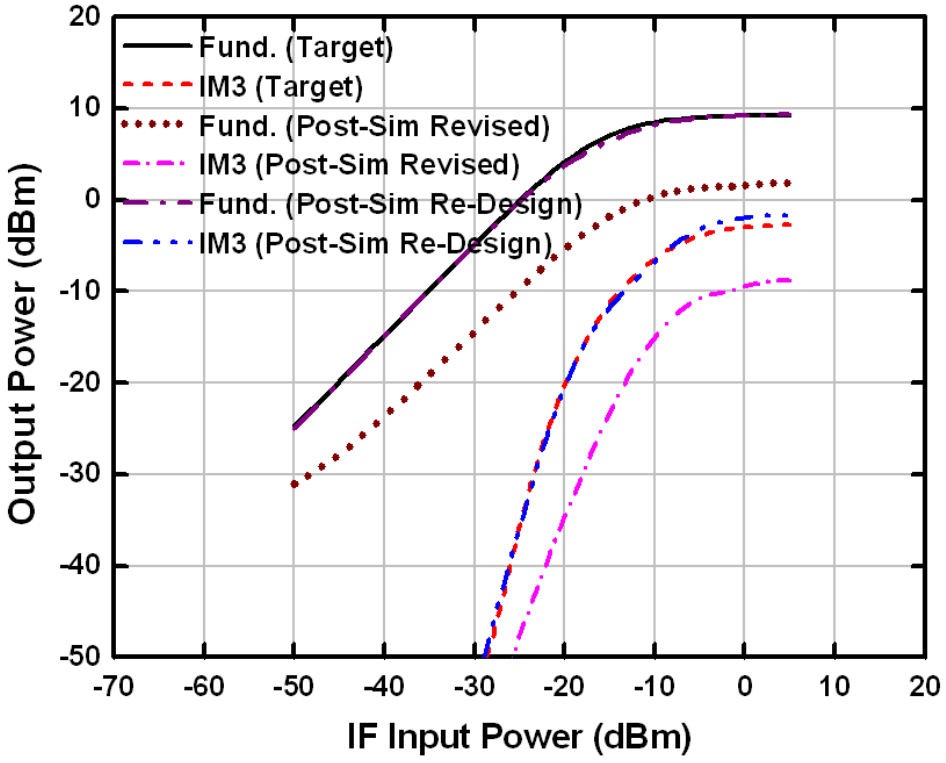


Fig. 4.29 2-tone test of re-design (SS, 75°C) comparing with original and revised post-sim

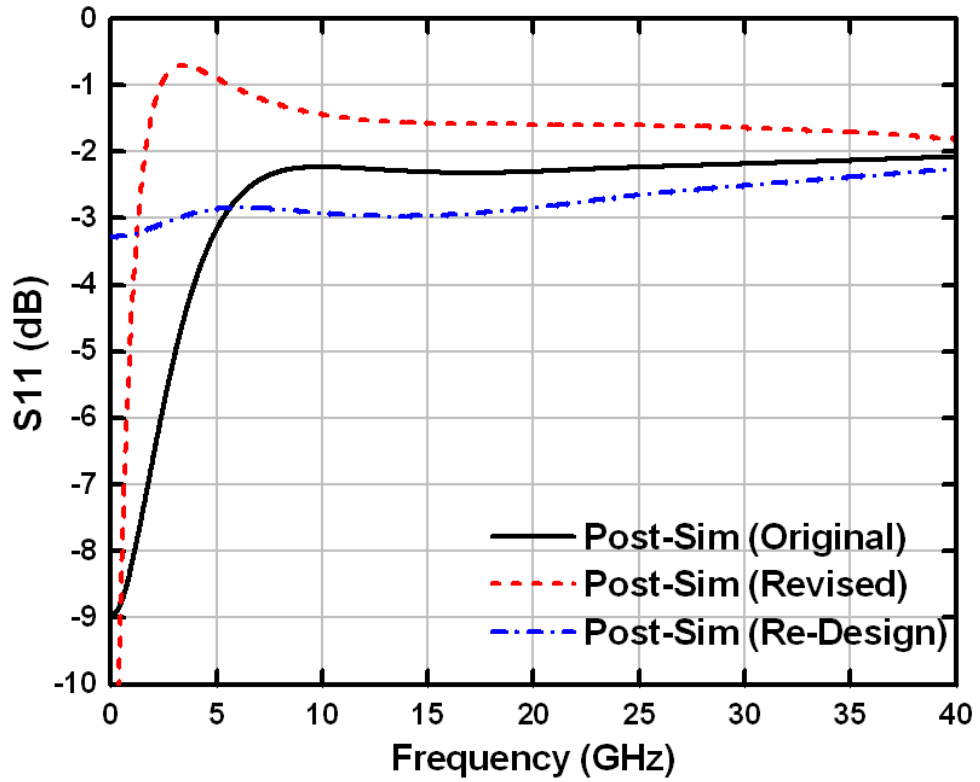


Fig. 4.30 S11 of re-design (TT, 75°C) comparing with original and revised post-sim

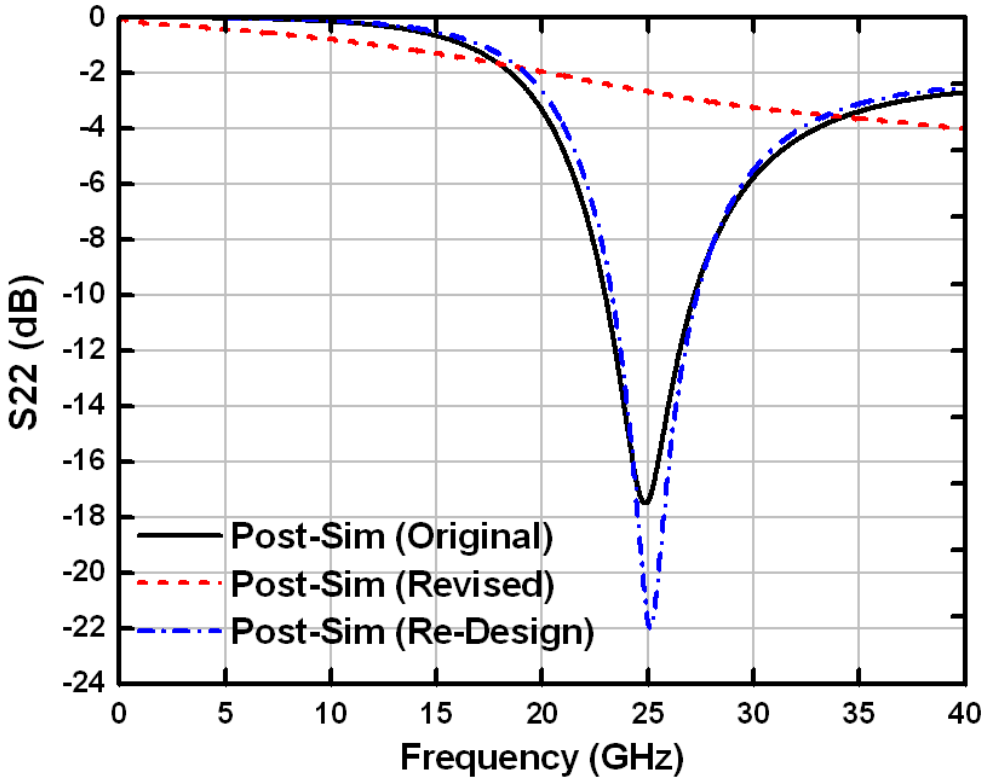


Fig. 4.31 S22 of re-design (TT, 75°C) comparing with original and revised post-sim

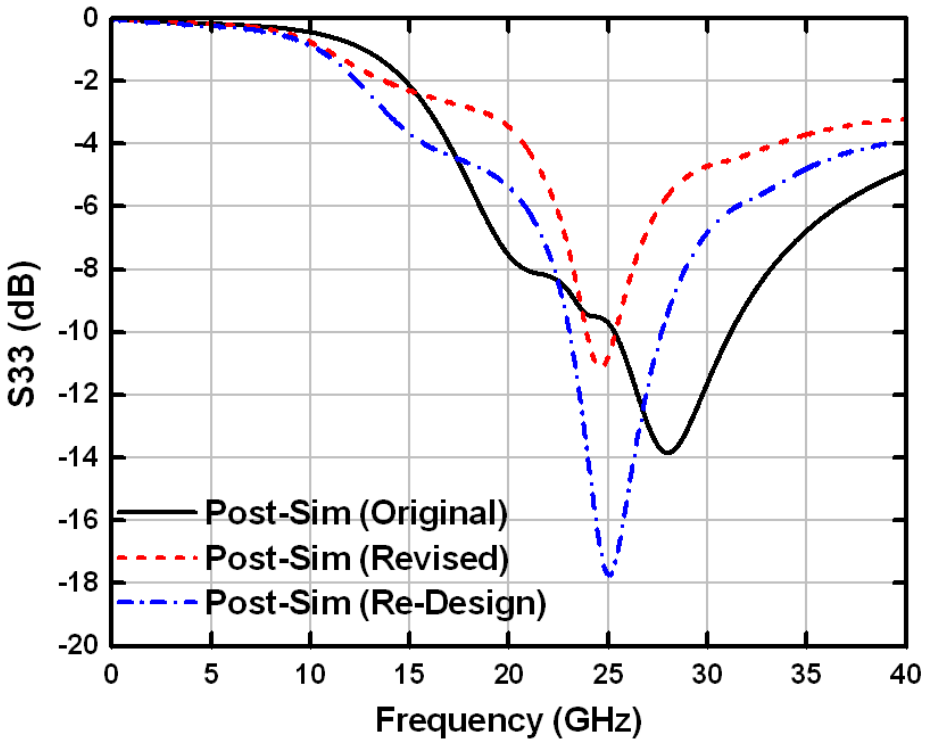


Fig. 4.32 S33 of re-design (TT, 75°C) comparing with original and revised post-sim

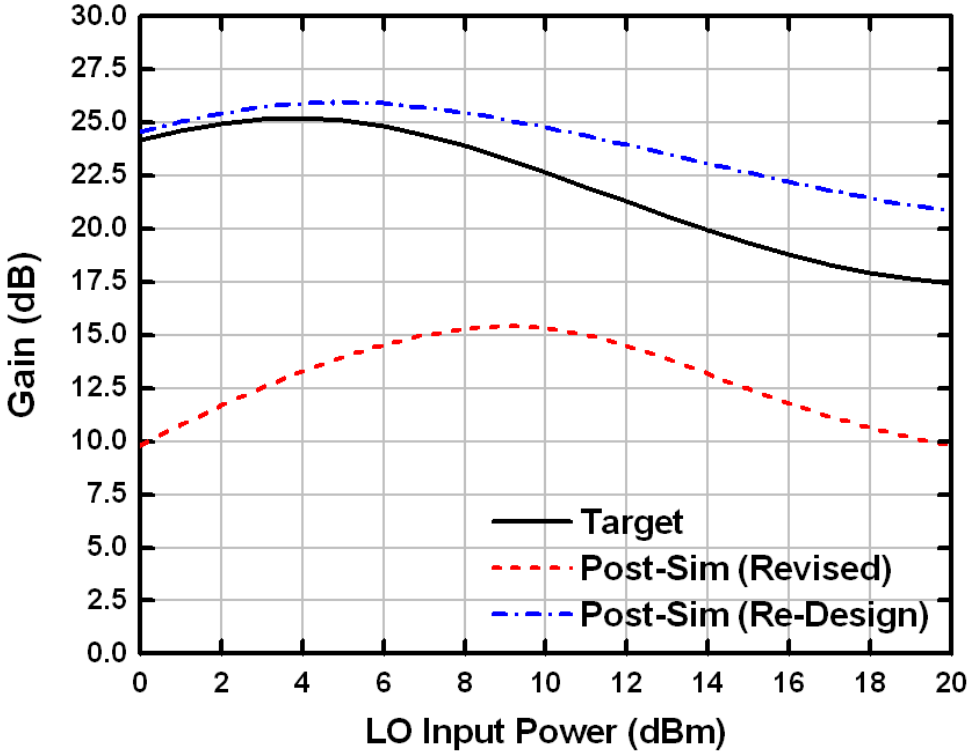


Fig. 4.33 Sweep LO power of re-design (TT, 75°C) comparing with original and revised post-sim

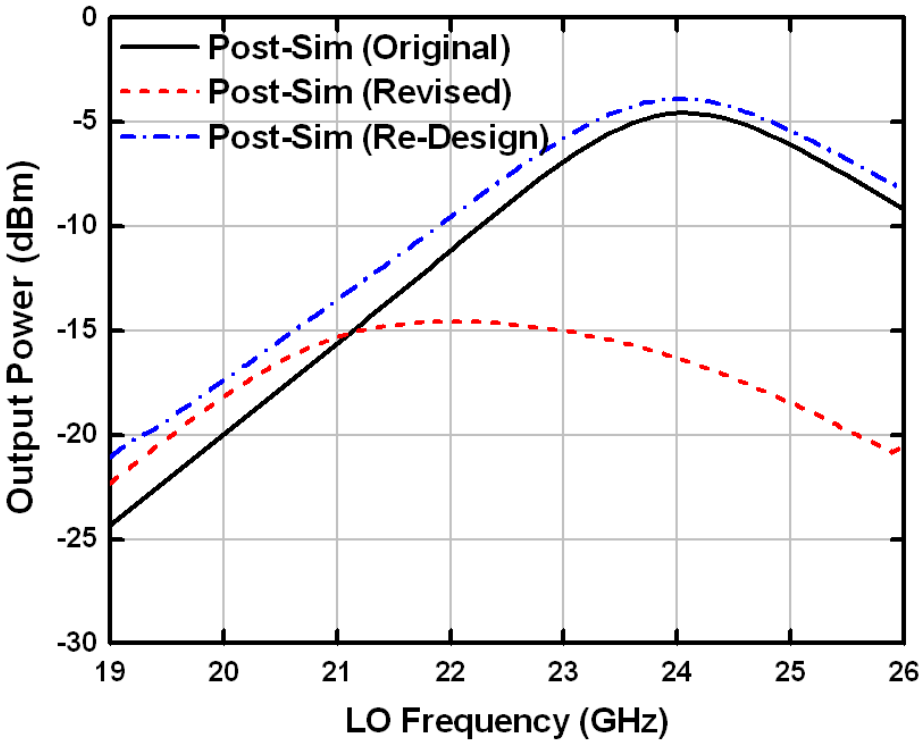


Fig. 4.34 Sweep LO frequency of re-design (TT, 75°C) comparing with original and revised post-sim

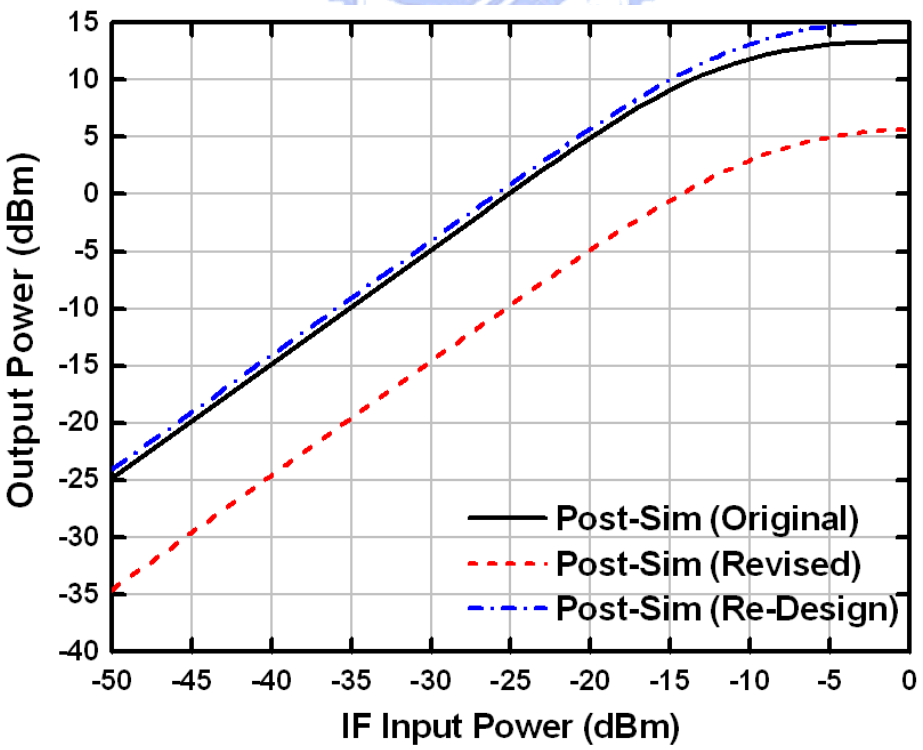


Fig. 4.35 1-tone test of re-design (TT, 75°C) comparing with original and revised post-sim

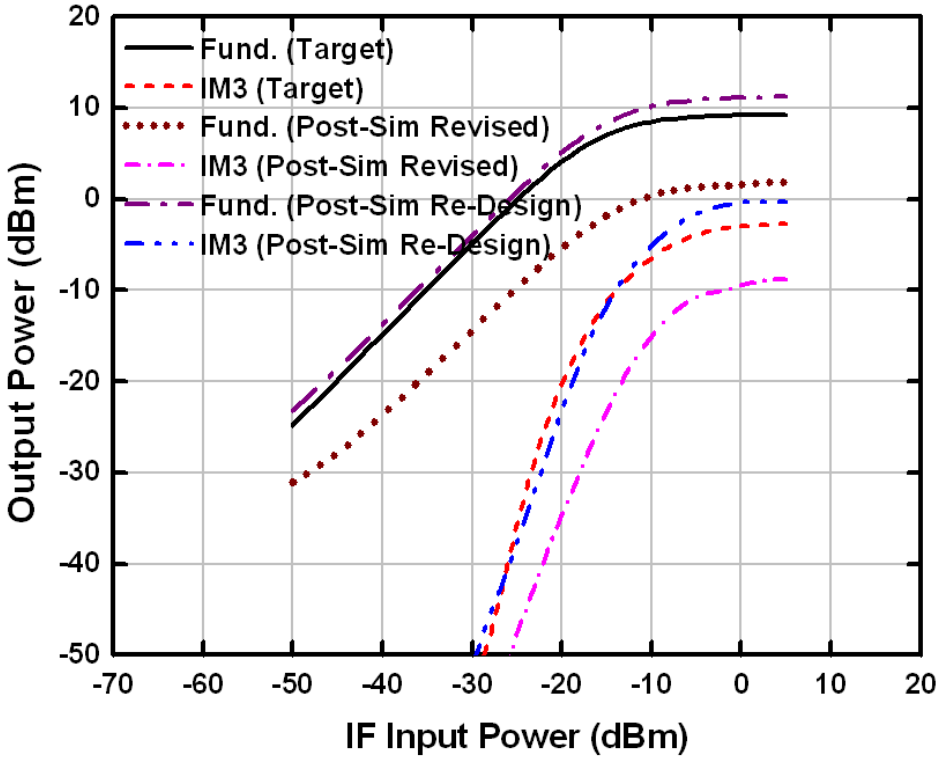


Fig. 4.36 2-tone test of re-design (TT, 75°C) comparing with original and revised post-sim

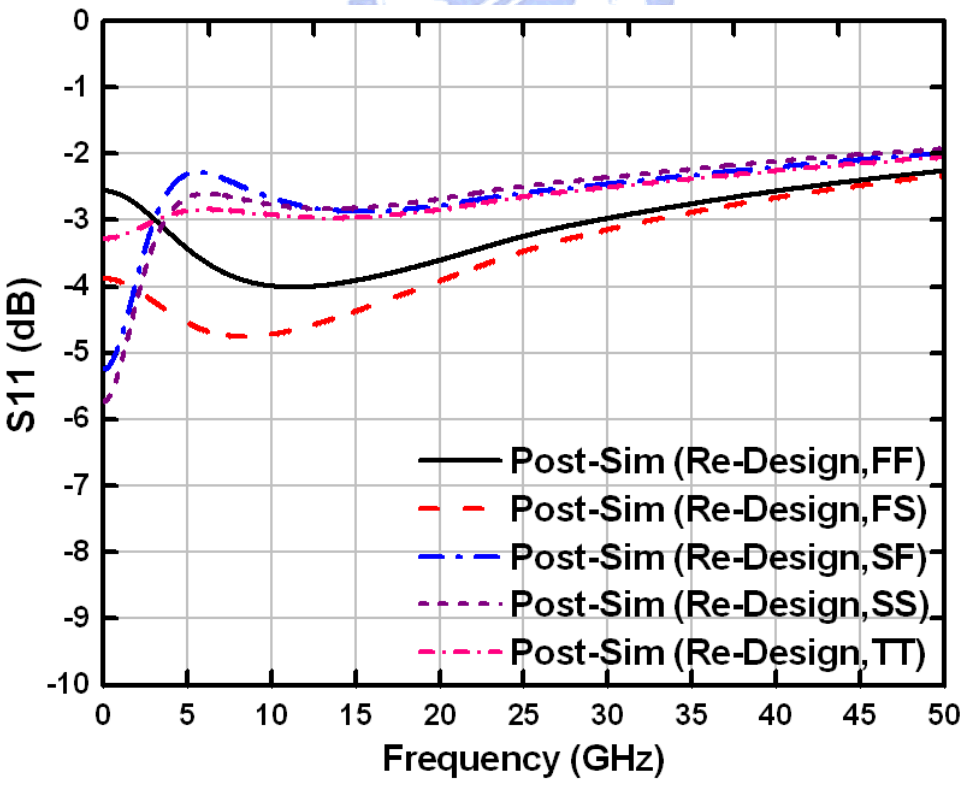


Fig. 4.37 S11 of re-design circuit in FF, FS, SF, SS, and TT corners

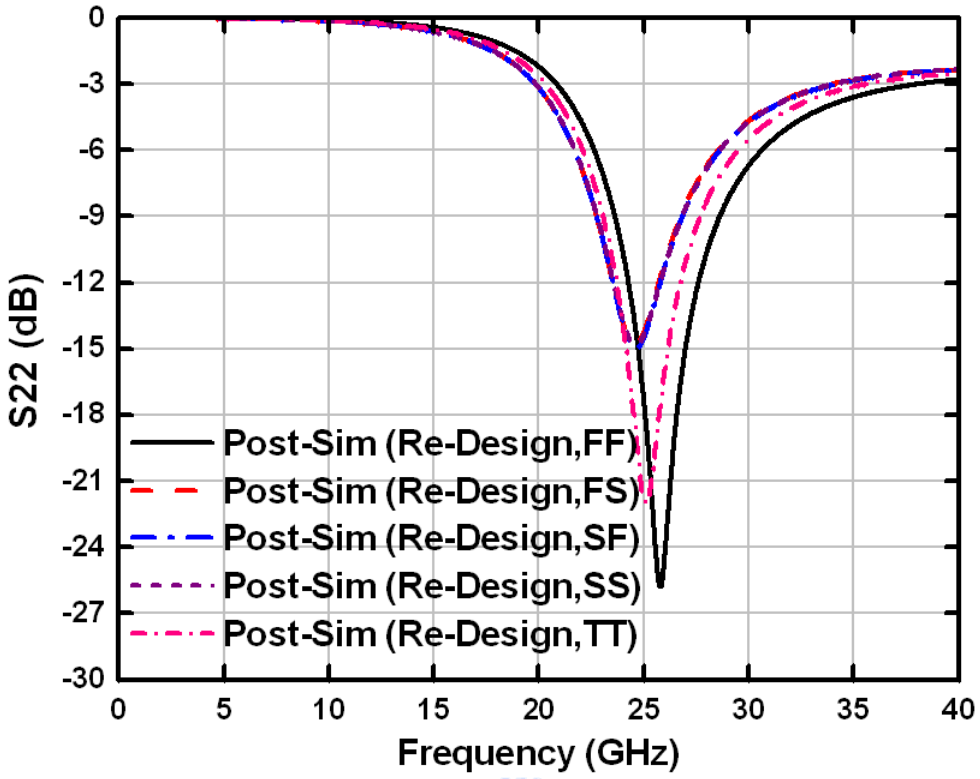


Fig. 4.38 S22 of re-design circuit in FF, FS, SF, SS, and TT corners

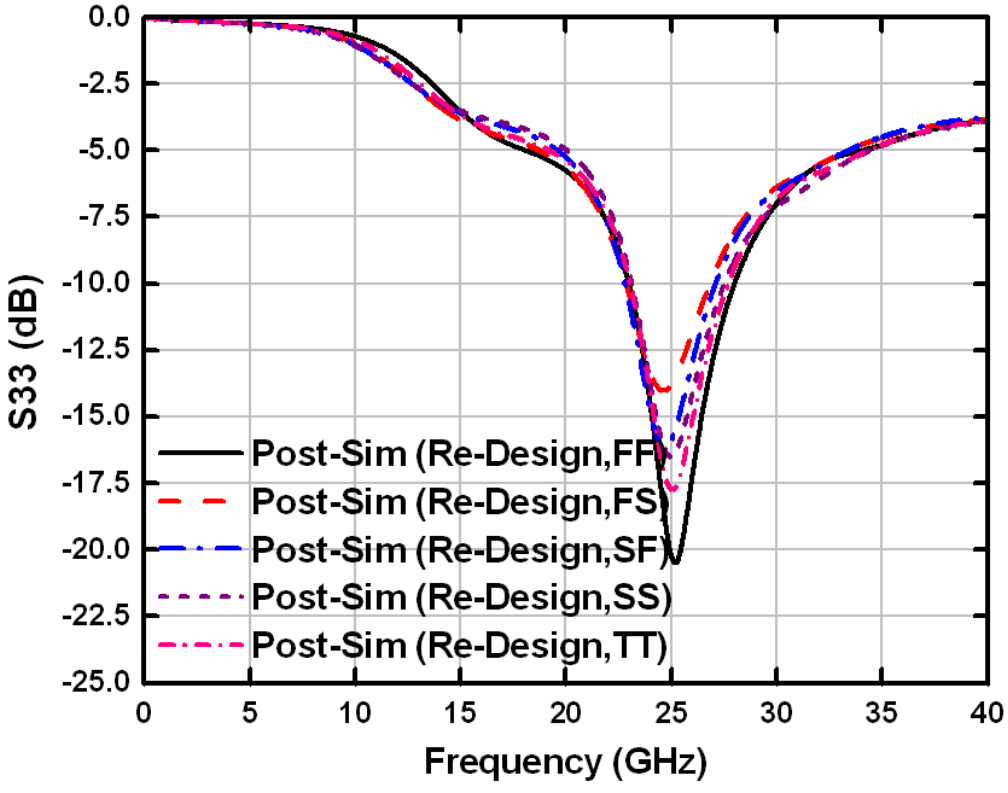


Fig. 4.39 S33 of re-design circuit in FF, FS, SF, SS, and TT corners

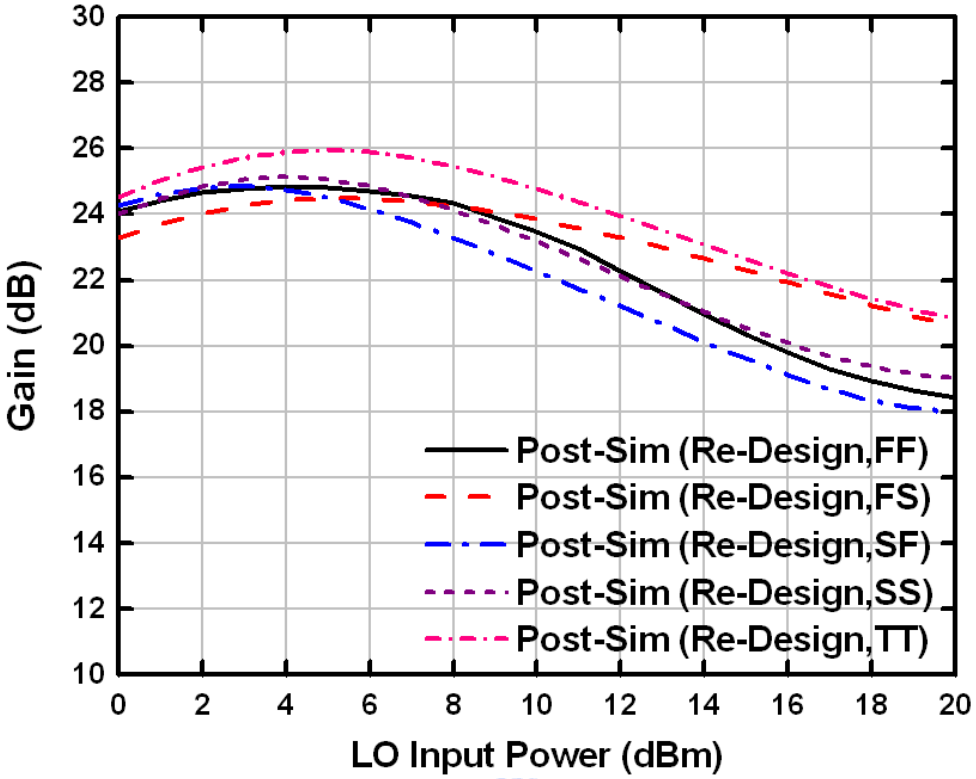


Fig. 4.40 Sweep LO power of re-design circuit in FF, FS, SF, SS, and TT corners

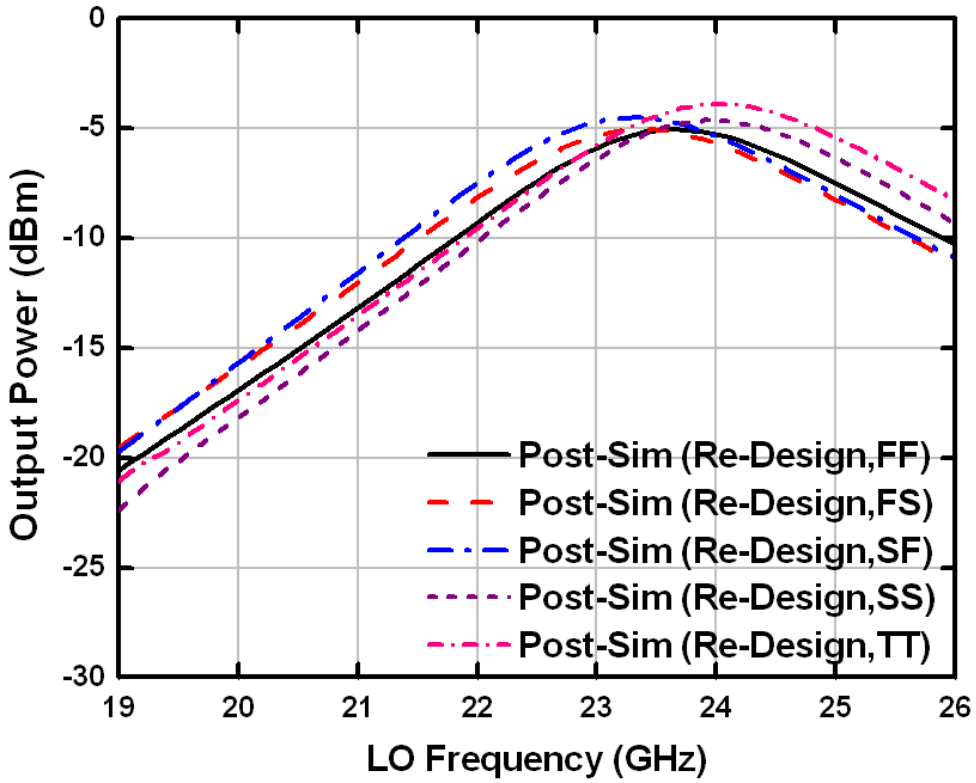


Fig. 4.41 Sweep LO frequency of re-design circuit in FF, FS, SF, SS, and TT corners

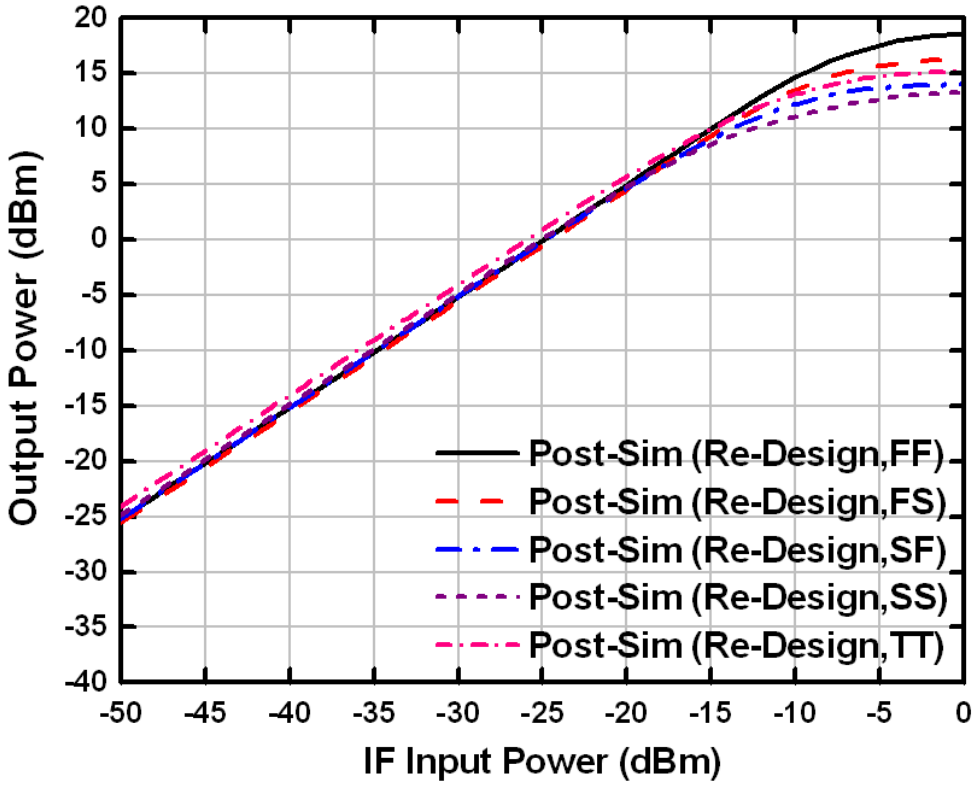


Fig. 4.42 1-tone test of re-design circuit in FF, FS, SF, SS, and TT corners

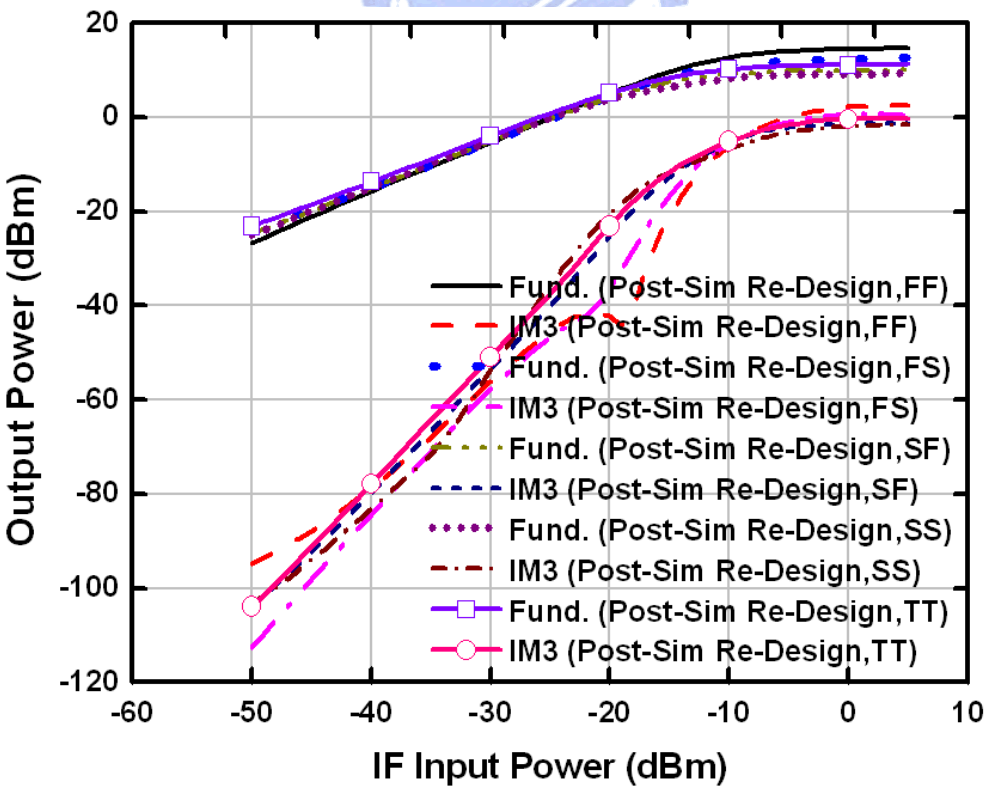


Fig. 4.43 2-tone test of re-design circuit in FF, FS, SF, SS, and TT corners

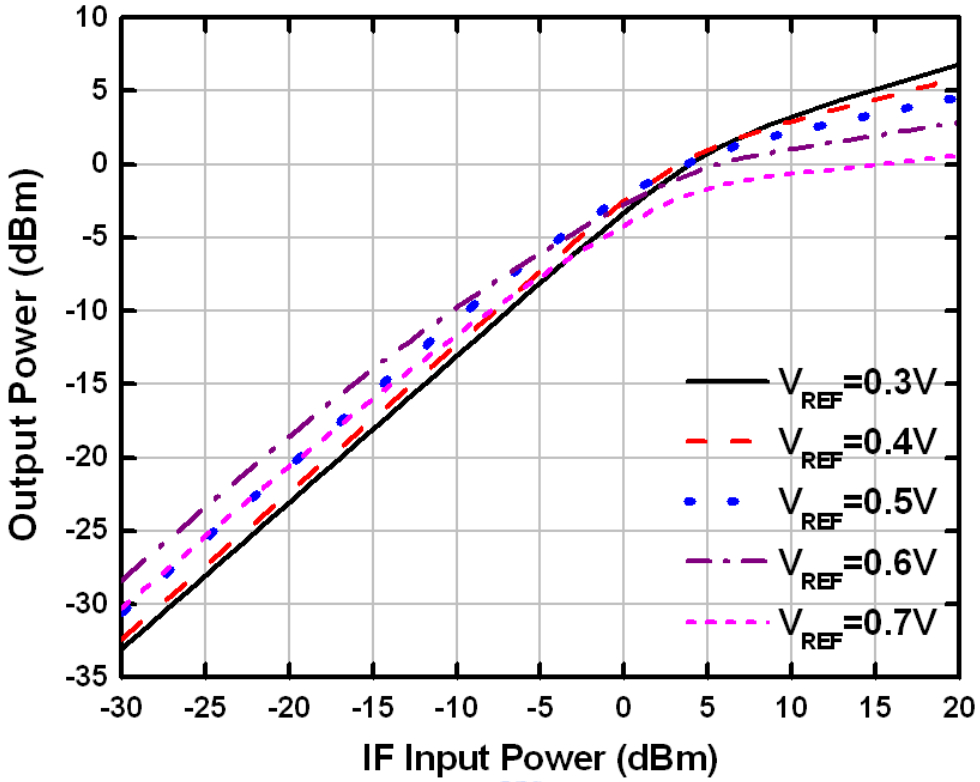


Fig. 4.44 1-tone test by different V_{REF} of proposed mixer

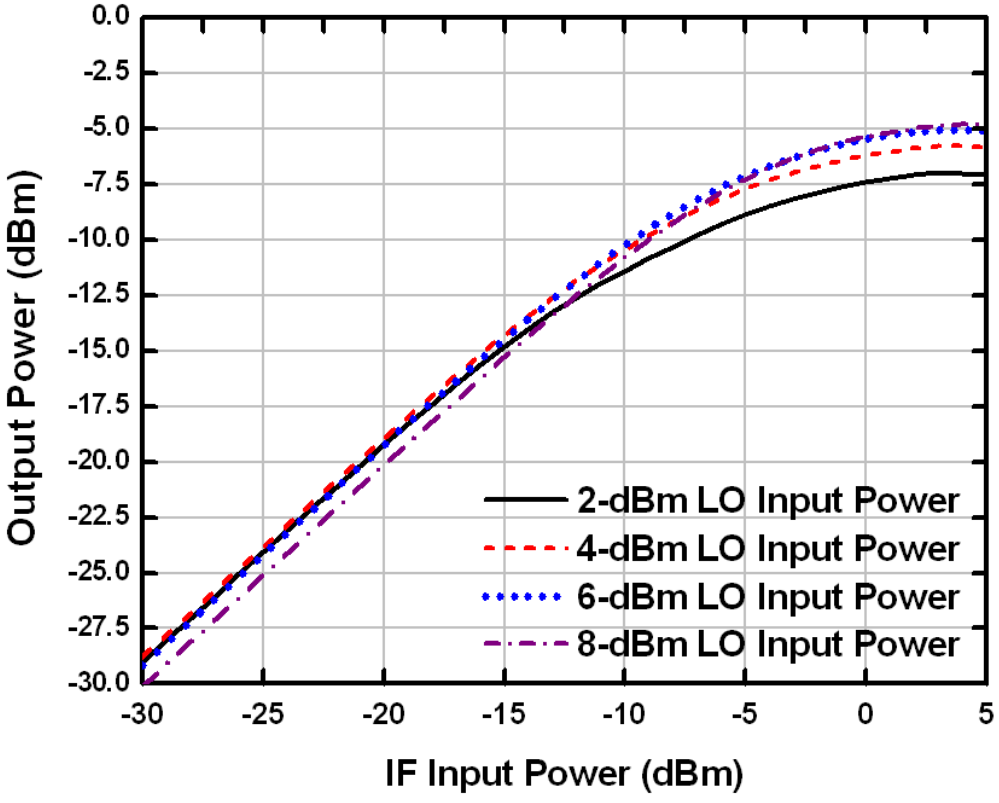


Fig. 4.45 1-tone test by different LO input power of proposed transmitter circuit

CHAPTER 5

CONCLUSIONS AND FUTURE WORK

5.1 Conclusions

In this research, a 24-GHz transmitter front-end is implemented by 0.13μm 1P8M CMOS technology. This 24-GHz transmitter front-end is realized by current-mode methodologies where the power amplifier is realized by two-stage current-mirror amplifier and the mixer is realized by current-operated self-swing mixer. This is the first work in current-mode transmitter including a mixer and a power amplifier for 24-GHz applications.

Because of the layout mistake and incorrect post simulation procedure, performance is seriously degraded. Measurement results show that the measured impedance matching for IF, LO, and RF ports are –1.4, –2.6, and –15.8 dB, respectively. The measured power gain is 11.5 dB with the LO frequency of 21.9 GHz and IF frequency of 100 MHz. OP_{1dB} is –9.5 dBm and OIP3 is 4 dBm. Power consumption is 238.4 mW from 1.2 V power supply.

After carefully considering these effects, the re-design post-sim results show that this proposed transmitter front-end has 25.2-dB power gain, 7.2-dBm OP_{1dB}, and 15-dBm OIP3 under SS corner. For TT corner, the power gain is 26 dB, OP_{1dB} is 10 dBm, and OIP3 is 23 dBm. From the re-design post-sim results, the power amplifier has 11.9-dBm IP_{1dB}, 22-dBm OIP3, and 22.9% peak PAE.

Comparing with other voltage-mode power amplifier, this current-mode power amplifier has better OP_{1dB} and OIP3 under lower supply voltage. Furthermore, the proposed current-mode transmitter has lower power dissipation under the same output power level. According to the experimental results, therefore, current-mode circuits are suitable for low supply voltage technology, especially for advanced CMOS technology.

5.2 Future Work

Because the problem of frequency drift is occurred in measurement results, the re-design version is moved to 24 GHz by careful whole chip EM simulation. This re-design transmitter circuit will be tape-out and measured in the future.

Besides, the 1-tone and 2-tone simulation results for power amplifier in Fig. 3.38 show the double-side band mixer compress the PA's gain, linearity and efficiency. Therefore, quadrature structure will be designed in order to improve the efficiency and release the linearity required in the future.

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