

# CONTENTS

<b>ABSTRACT (CHINESE)</b> .....	<b>i</b>
<b>ABSTRACT (ENGLISH)</b> .....	<b>iii</b>
<b>ACKNOWLEDGEMENT</b> .....	<b>v</b>
<b>TABLE CAPTIONS</b> .....	<b>viii</b>
<b>FIGURE CAPTIONS</b> .....	<b>ix</b>
<b>Chapter 1 Introduction</b> .....	<b>1</b>
1.1    MOTIVATION .....	1
1.1.1 <i>LCD Industry and LTPS Technology [1], [2]</i> .....	1
1.1.2 <i>System-on-Panel Displays</i> .....	2
1.1.3 <i>The Advantages of the SOP LTPS TFT-LCD Displays</i> .....	4
1.1.4 <i>Future Application of “Input Display” [6]</i> .....	7
1.2    THESIS ORGANIZATION .....	9
<b>Chapter 2 Background Knowledge of Thin-Film Transistor</b>	
<b>Liquid Crystal Displays</b> .....	<b>10</b>
2.1    LIQUID CRYSTAL DISPLAY STRUCTURE.....	10
2.1.1 <i>Material and Display Theory of Liquid Crystal [7], [8]</i> .....	10
2.1.2 <i>Liquid Crystal Display Module Structure</i> .....	13
2.1.3 <i>Equivalent Model of Dot in each Pixel Cell</i> .....	14
2.2    DRIVING METHOD IN TFT-LCD PANEL .....	17
2.2.1 <i>Driving Method</i> .....	17
2.2.2 <i>Gamma Correction</i> .....	20
2.3    PERIPHERY CIRCUIT BLOCK .....	22
2.3.1 <i>Scan Driver Circuit</i> .....	23
2.3.2 <i>Data Driver Circuit</i> .....	24
<b>Chapter 3 Novel Digital-to-Analog Converter with Gamma</b>	
<b>Correction for On-Panel Data Driver</b> .....	<b>25</b>

3.1	INTRODUCTION .....	25
3.2	DIGITAL-TO-ANALOG CONVERTERS [11]-[14].....	25
3.2.1	<i>R-String DAC with Switch Array Decoding</i> .....	25
3.2.2	<i>R-String DAC with Binary-Tree Decoding</i> .....	26
3.2.3	<i>R-String DAC with Digital Decoding</i> .....	27
3.2.4	<i>Charge-Redistribution DAC</i> .....	28
3.2.5	<i>Multiple R-String DAC [15]</i> .....	29
3.2.6	<i>Resistor-Capacitor Hybrid DAC</i> .....	30
3.2.7	<i>Current-Steering DAC</i> .....	31
3.3	NOVEL FOLDED R-STRING DAC WITH GAMMA CORRECTION .....	33
3.3.1	<i>Design of Gamma Correction</i> .....	33
3.3.2	<i>Circuit Description</i> .....	37
3.3.3	<i>Simulation and Verification</i> .....	40

## **Chapter 4 On-Panel Analog Output Buffer for Data Driver**

### **with Consideration of Device Characteristic**

#### **Variation ..... 45**

4.1	INTRODUCTION .....	45
4.2	DEVICE CHARACTERISTIC VARIATION IN LTPS TECHNOLOGY .....	46
4.3	ON-PANEL ANALOG OUTPUT BUFFER .....	48
4.3.1	<i>Source Follower Analog Output Buffer [26]</i> .....	48
4.3.2	<i>Unity-Gain Output Buffer with an OPamp</i> .....	50
4.3.3	<i>Proposed Output Buffer with Suppressing Device Variation</i> .....	53
4.4	EXPERIMENTAL RESULTS .....	57
4.5	DISCUSSION .....	62
4.6	SUMMARY .....	63

## **Chapter 5 Conclusion and Future Works..... 64**

5.1	CONCLUSION.....	64
5.2	FUTRUE WORKS.....	65

## **REFERENCES ..... 67**

## **VITA 70**

## TABLE CAPTIONS

Table 3.1 The comparisons of many kinds of the digital-to-analog converter circuits. .....	32
Table 3.2 The pixel voltage corresponded to each gray level with gamma of 2.2.....	34
Table 3.3 The resistance values of R-string for gamma correction design.....	35
Table 3.4 The modified resistance values of R-string for gamma correction design...	36
Table 3.5 The voltage values in ideal condition, R-string ladder, and this proposed DAC corresponded to each gray level. Unit: volt.....	41
Table 4.1 Summary of the simulated circuit performances of the output buffer in Fig. 4.6.....	52
Table 4.2 Mobility variation for n-channel and p-channel TFTs at different stress conditions. ....	53
Table 4.3 The summary and comparison of the simulated circuit performances of the output buffer in Fig. 4.6 and Fig. 4.8. ....	56



## FIGURE CAPTIONS

Fig. 1.1	System integration roadmap of LTPS TFT-LCD.....	2
Fig. 1.2	Basic concept of pixel memory technology. ....	3
Fig. 1.3	(a) The schematic illustration of the “sheet computer” concept and (b) a CPU with an instruction set of 1-4 bytes and an 8b data bus on glass substrate....	4
Fig. 1.4	The roadmap of LTPS technologies leading toward the realization of sheet computers. ....	4
Fig. 1.5	Schematic cross-section view of the structure of a LTPS complementary metal oxide semiconductor (CMOS). LDD = lightly doped drain.....	5
Fig. 1.6	(a) Comparison of an amorphous silicon TFT-LCD module and (b) a low-temperature polycrystalline silicon TFT-LCD module. ....	6
Fig. 1.7	The comparison of new SOP technology product and conventional product. The new 3.8” SOP LTPS TFT-LCD panel has been manufactured by SONY corp. in 2002. ....	6
Fig. 1.8	Future application of “Input Display”.....	7
Fig. 1.9	The principle and structure of the photo-sensing display. ....	8
Fig. 1.10	The system architecture and image-capturing finger of this new touch-panel. ....	8
Fig. 2.1	Phases of liquid crystal materials versus temperature. ....	10
Fig. 2.2	(a) A couple of polarizers with 90° phase error. (b) A couple of polarizers with liquid crystals.....	11
Fig. 2.3	The structure of a TN-LCD (a) while light is passing, and (b) while light is blocked. a: polarizer; b: glass substrate; c: transparent electrode; g: orientation layer; e: liquid crystal; f: illumination. ....	12
Fig. 2.4	The transmitted luminance versus the normalized voltage ( $V_{LC}/V_0$ ) across the LC cell for the normally white mode and the normally black mode.....	13
Fig. 2.5	The cross section structure of TFT-LCD panel.....	14
Fig. 2.6	The basic layout and cross section of an AMLCD sub-pixel. ....	14
Fig. 2.7	The equivalent circuit of a TFT in the sub-pixel with voltages, currents, and parasitic capacitances. ....	15
Fig. 2.8	The layout view of a TFT-LCD sub-pixel: (a) $C_s$ on common mode and (b) $C_s$ on gate mode. ....	16
Fig. 2.9	The equivalent circuit of a TFT-LCD sub-pixel: (a) $C_s$ on common mode and (b) $C_s$ on gate mode. ....	16
Fig. 2.10	The polarity inversions of TFT-LCD panel.....	18
Fig. 2.11	The operation waveform of direct driving method.....	19

Fig. 2.12	The operation waveform of AC modulation driving method. ....	19
Fig. 2.13	The operation of the gamma correction for the normally white TN type LCD panel. HVS: human visual system. ....	20
Fig. 2.14	The input digital code vs. pixel voltage curve of data driver in TFT-LCD panel. ....	21
Fig. 2.15	The block diagram of the entire TFT-LCD panel circuits. ....	22
Fig. 2.16	The entire addressing system in detail. ....	23
Fig. 2.17	The basic diagram of scan driver circuit. ....	23
Fig. 2.18	The basic diagram of data driver circuit. ....	24
Fig. 3.1	A 6-bit R-string DAC with switch array decoding. ....	26
Fig. 3.2	A 6-bit R-string DAC with binary-tree decoding. ....	26
Fig. 3.3	A 6-bit R-string DAC with digital decoding. ....	27
Fig. 3.4	The charge-redistribution DAC. ....	28
Fig. 3.5	A 6-bit multiple R-string DAC. ....	29
Fig. 3.6	(a) The spikes of the DAC, and (b) the output waveform of the DAC with spikes reduction method. ....	30
Fig. 3.7	The resistor-capacitor hybrid DAC. ....	31
Fig. 3.8	The current-steering DAC. ....	32
Fig. 3.9	The transform function of display system. ....	33
Fig. 3.10	The voltage vs. transmission curve of the liquid crystal in CPT process. ...	34
Fig. 3.11	The gray level vs. pixel value curve in the voltage divider of R-string. ....	35
Fig. 3.12	The GL vs. pixel value curve in the modified voltage divider of R-string. ...	36
Fig. 3.13	The folded R-string DAC with segmented digital decoders. ....	37
Fig. 3.14	The operation illustration of the 6-bit folded R-string DAC with segmented digital decoders. ....	38
Fig. 3.15	The comparison of the transistors number of the decoders between the conventional and proposed 6-bit R-string DAC. ....	39
Fig. 3.16	The simulation result of this 6-bit folded R-string DAC with segmented digital decoders in 8- $\mu\text{m}$ technology. ....	40
Fig. 3.17	The GL vs. output voltage curves in ideal condition, R-string ladder, and this proposed DAC. ....	41
Fig. 3.18	The definition of the differential non-linearity. ....	42
Fig. 3.19	The definition of the integral non-linearity. ....	42
Fig. 3.20	The simulation result of this 6-bit folded R-string DAC with segmented digital decoders in 3- $\mu\text{m}$ technology. ....	43
Fig. 3.21	The GL vs. output voltage curves in ideal condition, R-string ladder, and this proposed DAC in 3- $\mu\text{m}$ technology. ....	43
Fig. 4.1	Variation on threshold voltage ( $V_{\text{TH}}$ ) of 120 LTPS n-type TFTs in different	

	locations on LCD panel. ....	47
Fig. 4.2	The device characteristic variations of LTPS p-type TFTs in different gate bias. ....	47
Fig. 4.3	(a) The conventional source follower output buffer and (b) its output waveforms at different input voltages.....	48
Fig. 4.4	The Monte Carlo simulation results of the conventional source follower output buffer. ....	49
Fig. 4.5	(a) The source follower output buffer with $V_{TH}$ compensation method and (b) Monte Carlo simulation results of this source follower output buffer. ....	49
Fig. 4.6	The class-A analog output buffer with N-TFTs input stage. ....	51
Fig. 4.7	The simulated frequency response of the class-A analog output buffer with N-TFTs input stage in open-loop condition.....	52
Fig. 4.8	The class-A analog output buffer with P-TFTs input stage.....	54
Fig. 4.9	The simulated frequency response of the class-A analog output buffer with P-TFTs input stage in open-loop condition. ....	55
Fig. 4.10	The photographs of the class-A output buffers with (a) N-TFTs input stage and (b) P-TFTs input stage. ....	57
Fig. 4.11	The setup illustration for slew rate and output swing measurement with DC probing station. ....	58
Fig. 4.12	The setup illustration for unity-gain bandwidth measurement with DC probing station. ....	59
Fig. 4.13	The proposed analog output buffer under the PCB with wire bonding and the measurement setup illustration with the wire bonding glass substrate samples. ....	59
Fig. 4.14	The measured output waveforms of the class-A output buffers with (a) N-TFTs input stage and (b) P-TFTs input stage about slew rate and output swing. ....	60
Fig. 4.15	The measured output waveforms of the class-A output buffers with (a) N-TFTs input stage and (b) P-TFTs input stage about unity-gain bandwidth. ....	60
Fig. 4.16	The slew rate and output swing of the class-A output buffer with N-TFTs input stage, which are measured from 13 samples on glass substrate.....	61
Fig. 4.17	(a) Circuit and signal-timing diagram of the analog output buffer with the offset compensation technique. (b) The measurement result of this analog output buffer with the offset compensation technique under 50-kHz square wave with a swing of 2-to-8 V. ....	62
Fig. 4.18	The proposed class-A output buffer with P-TFTs input stage using for pixel array in TFT-LCD panel.....	63

Fig. 5.1 The architecture of the DAC circuit combined with analog output buffer with input offset compensation method in TFT-LCD panel.....65

Fig. 5.2 A class-B analog output buffer with device variation suppressing technique.....66

