Chapter 3

Novel Digital-to-Analog Converter with Gamma Correction for On-Panel Data Driver

3.1 INTRODUCTION

As last chapter description, we know that there is a nonlinearity relationship between luminance and human visual system. For this reason, a data driver with gamma correction is necessary in TFT-LCD panel. The Data driver mainly contains shifter register, data latch, level shifter, digital-to-analog converter (DAC) and analog output buffer. DAC is used convert the digital RGB signal to analog gray level. It is an important and essential part in the driving system of TFT-LCD panel. In this chapter, the analysis and comparison of the many kinds of DAC circuits will be introduced particularly. Moreover, a novel DAC with gamma correction for on-panel data driver will be proposed and verified in this chapter.

3.2 DIGITAL-TO-ANALOG CONVERTERS [11]-[14]

3.2.1 R-String DAC with Switch Array Decoding

Fig. 3.1 shows a 6-bit R-string DAC circuit. The architecture of this DAC requires no digital decoders. This conventional R-string DAC is familiar in general LCD data drivers, because this architecture is simple and suitable for gamma correction design. However, the area of switch array is becoming larger and larger due to the high resolution DAC. The loading at the output node (Vout) is also becoming larger due to the huge switch array.

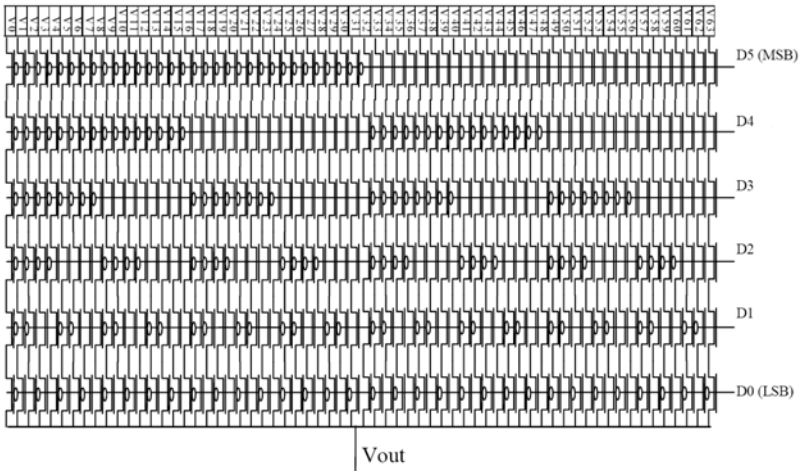


Fig. 3.1 A 6-bit R-string DAC with switch array decoding.

3.2.2 R-String DAC with Binary-Tree Decoding

Fig. 3.2 is a 6-bit R-string DAC with binary-tree decoding. This architecture also requires no digital decoders. In opposition to the R-string DAC with switch array decoding, this R-string DAC with binary-tree decoding has less transistors in the decoding circuits. Nevertheless, the speed of this circuit is limited by the delay through the switch network. The timing skew among the switch-controlling signals can cause large glitches at Vout. This circuit also has larger RC-type loading at the output node (Vout) due to the binary-tree switches.

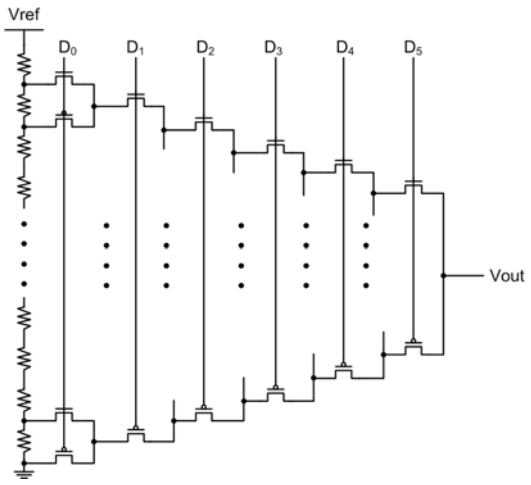


Fig. 3.2 A 6-bit R-string DAC with binary-tree decoding.

3.2.3 R-String DAC with Digital Decoding

In a higher-speed implementation, logic can be used for the decoder. Fig. 3.3 is a 6-bit R-string DAC with digital decoding. The loading of the output node can be reduced by the digital decoder, because the output node is only connected to one column of analog switches. Therefore, the operational speed of DAC using digital decoding is faster than DAC using binary-tree decoding. This architecture is also more suitable for gamma correction design because it is easy to produce different sections in resistor string. However, the area and complexity of decoder are larger and larger due to the high resolution DAC. For this reason, this R-string DAC with digital decoding is not suitable for integrating the data driver in the high resolution TFT-LCD panels.

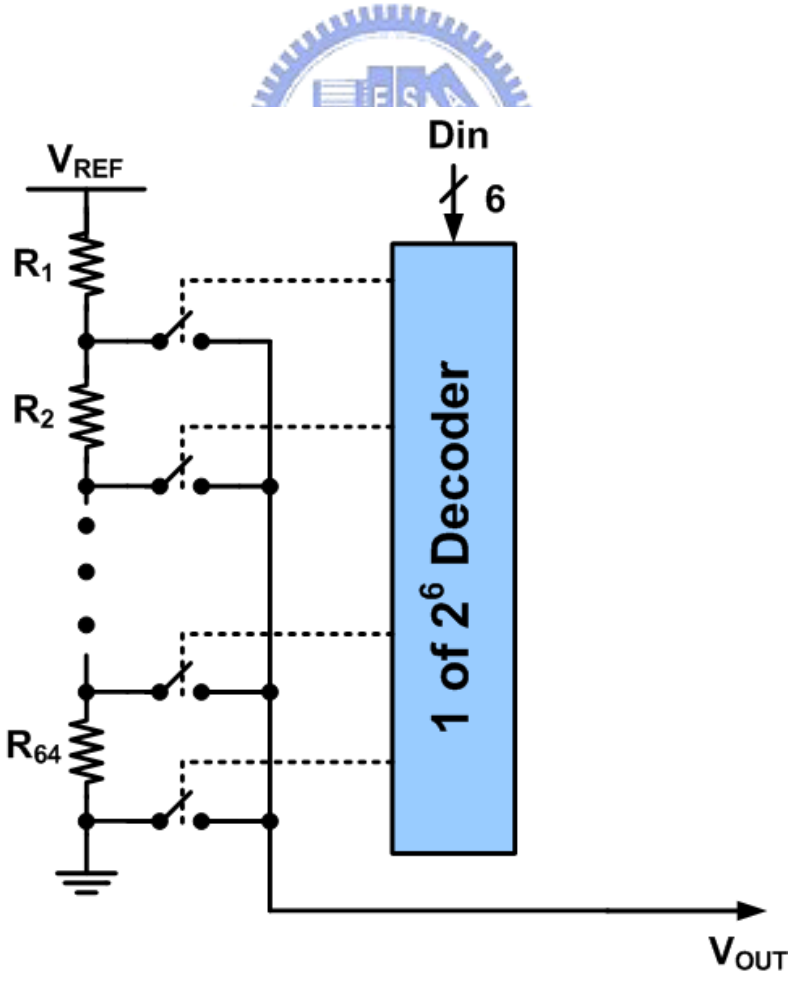


Fig. 3.3 A 6-bit R-string DAC with digital decoding.

3.2.4 Charge-Redistribution DAC

As shown in Fig. 3.4, it is a charge-redistribution DAC. The basic idea here is to simply replace the input capacitor of a switched-capacitor (SC) gain amplifier by programmable capacitor array (PCA) of binary-weighted capacitors. In this circuit, it has two phases. In first phase (ϕ_1), all capacitor bottom plates are connected to a reference voltage and top plates are connected to ground. During second phase (ϕ_2), capacitor bottom plates are connected to a reference voltage or ground according to logic high or logic low in codes. By this operation, the voltage level in output terminal can be determined by a formula which is shown in follow:

$$V_o = V_{ref} \times \frac{C}{2^N C + C_p} \times \sum_{i=0}^{N-1} b_i 2^i \qquad (3 - 1)$$

Where b_i is the bit number in input code, N is the total bit number and C_p is top plate parasitic capacitance. This circuit structure has some advantages better than the resistor-string DAC. First, the process matching for capacitor is better than resistor string. Second, charge-redistribution DAC can save more power because it has no DC path in the circuit. However, it has a big problem in LCD panel application. That is, this method is very difficult to achieve gamma correction. In other word it cannot compensate the inherent characteristic of liquid crystal.

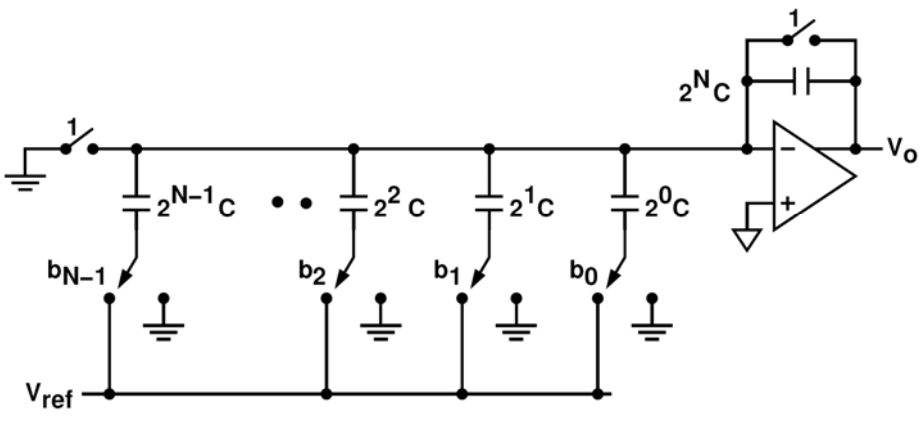


Fig. 3.4 The charge-redistribution DAC.

3.2.5 Multiple R-String DAC [15]

In this variation, a second tapped resistor string is connected between two adjacent nodes of the first resistor string (voltage reference), as shown in Fig. 3.5. In the shown 6-bit example, the three MSBs determine which two adjacent nodes of the first resistor string. The second resistor string linearly interpolates between the two adjacent voltages from the first resistor string. Finally, the output is determined by the lower LSBs. This approach requires only $2x2^{N/2}$ resistors, making it suitable for higher-resolution, low-power applications. This approach also has guaranteed monotonicity. During the signal transformation process, the spikes generated in the DAC (as shown in Fig. 3.6 (a)) are significantly related to the quality of display because the spikes would lead to the unstable displaying and redundant power consumption. Therefore, effective spikes reduction in the DAC becomes a critical topic for display systems. In this architecture, the bit with least signal variation (the higher bits) is arranged closely to output node. By this method, the spikes of the DAC can be reduced obviously, shown in Fig. 3.6 (b).

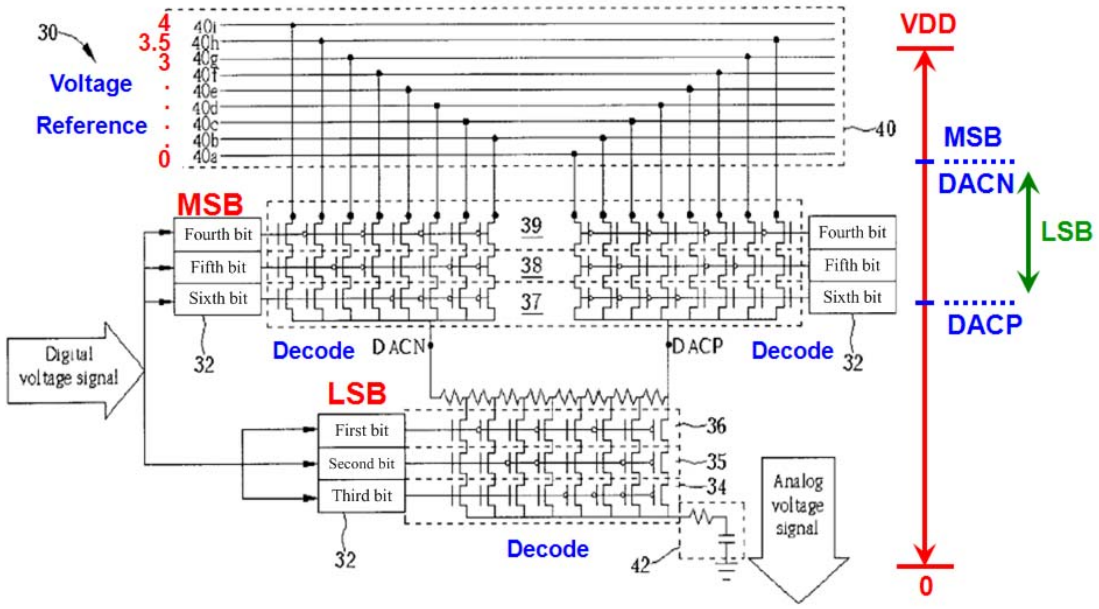
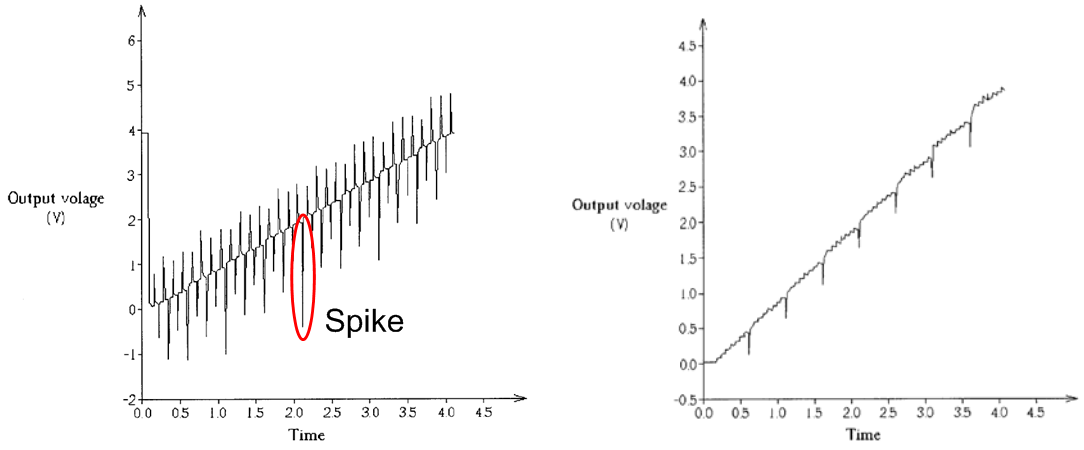


Fig. 3.5 A 6-bit multiple R-string DAC.



(a) (b)

Fig. 3.6 (a) The spikes of the DAC, and (b) the output waveform of the DAC with spikes reduction method.

3.2.6 Resistor-Capacitor Hybrid DAC

The benefits and drawbacks of resistor-string DAC and charge-redistribution DAC have been discussed previously. In order to get their benefits and exclude the drawbacks in the DAC, a hybrid structure has been proposed in Fig. 3.7. In this circuit, the upper bits are adopted in resistor-string architecture and the lower bits are employed the charge-redistribution structure. There are two phases in this circuit operation. In first phase (ϕ_1), all capacitor bottom plates are connected to ground. During second phase (ϕ_2), capacitor bottom plates are connected to a reference voltage V_1 or connected to the other reference voltage V_2 which is according to logic high or logic low in input codes. Furthermore, a formula about this circuit is shown in below:

$$V_o = \frac{V_{ref}}{2^M} \times \sum_{i=0}^{M-1} b_{i+L} 2^i + \frac{1}{2^M} \times \frac{V_{ref}}{2^L} \times \sum_{j=0}^{L-1} b_j 2^j = \frac{V_{ref}}{2^N} \times \sum_{i=0}^{N-1} b_i 2^i \qquad (3 - 2)$$

Where M is the total bit number in resistor-string DAC, L is the total bit number in charge-redistribution DAC and N is the total bit number in this DAC (N = M + L).

This hybrid structure can achieve high performance in operational speed, die area, and power consumption. Besides, it is also suitable in gamma correction DAC.

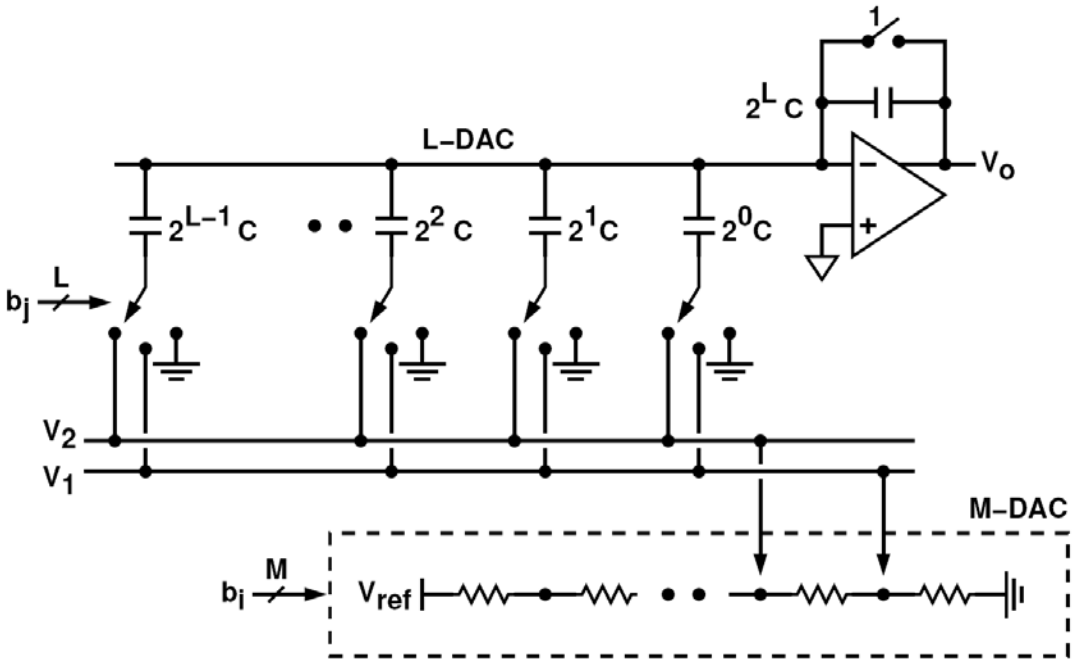


Fig. 3.7 The resistor-capacitor hybrid DAC.

3.2.7 Current-Steering DAC

Current-steering DAC is very similar to resistor-based converter, but is intended for higher-speed application due to the current type. The basic idea is to switch currents to either the output or to ground, as shown in Fig. 3.8. Here, the total output current is sum of the currents which are selected, as shown below:

$$I_o = I \times (b_{N-1} \cdot 2^{N-1} + b_{N-2} \cdot 2^{N-2} + \cdots + b_1 \cdot 2^1 + b_0 \cdot 2^0) \qquad (3 - 3)$$

This output current is converted to a voltage through a resistor (R_F). Although, this circuit has potentially large glitches due to timing skews and the monotonicity in this DAC is not guaranteed. But, we can reduce the glitches and provide the guaranteed monotonicity by using the thermometer decoding method.

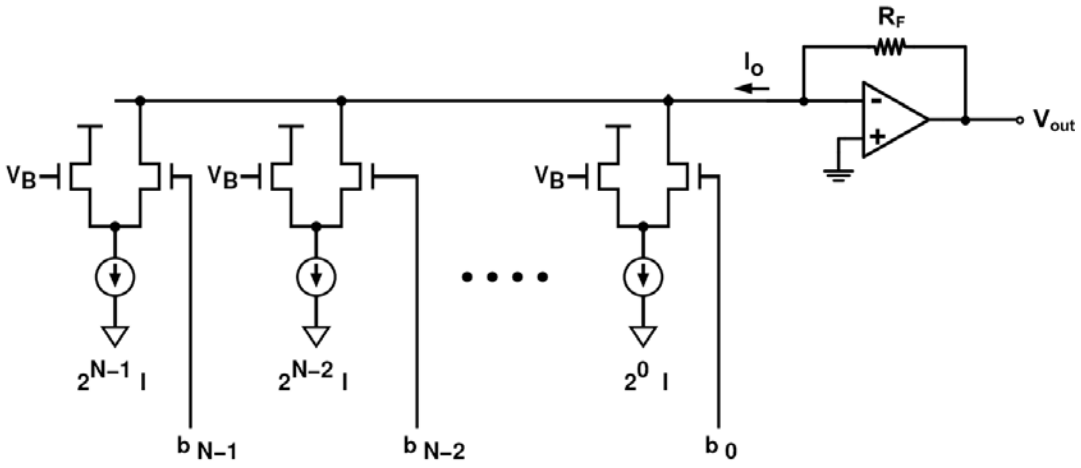


Fig. 3.8 The current-steering DAC.

From previous description and analysis, we can summarize a table about many kinds of the DAC circuits, as shown in Table 3.1. In this table, we can clearly find the characteristics of those DAC, like: suitable for gamma correction design, operation speed, power consumption, area, and the complexity of design and layout.

Table 3.1

The comparisons of many kinds of the digital-to-analog converter circuits.

Circuit Type	γ Correction	Speed	Power	Area	Complexity
R-DAC with switch array decoder	Best	Poor	Normal	Poor	Easy
R-DAC with binary-tree decoder	Best	Normal	Normal	Normal	Easy
R-DAC with digital decoder	Best	Good	Normal	Normal	Medium
Charge-redistribution DAC	Poor	Good	Best	Normal	Medium
Multiple R-DAC	Good	Good	Poor	Best	Medium
Hybrid R-C DAC	Good	Good	Good	Good	Hard
Current-steering DAC	Poor	Best	Poor	Normal	Hard

3.3 NOVEL FOLDED R-STRING DAC WITH GAMMA CORRECTION

3.3.1 Design of Gamma Correction

From previous chapters, we know that there is a nonlinearity relationship between luminance and human visual system. For this reason, the gamma correction design is necessary in TFT-LCD panel. The display transfer function is shown in Fig. 3.9. The nonlinearity between gray level domain and luminance domain can be corrected by gamma correction design. For a 6-bit gamma correction design, the transform function about this system can be express as following:

$$\frac{T(GL)-T_{\min}}{T_{\max}-T_{\min}}=(GL/63)^{\gamma} \tag{3 - 4}$$

$$T(GL)=(T_{\max}-T_{\min})(GL/63)^{\gamma}+T_{\min} \tag{3 - 5}$$

$$L(GL)=T(GL)\cdot K_{backlight} \tag{3 - 6}$$

$$L(GL)=(L_{\max}-L_{\min})(GL/63)^{\gamma}+L_{\min} \tag{3 - 7}$$

From above formula, the transform function between transmission and gray level is shown in equation (3 - 5).

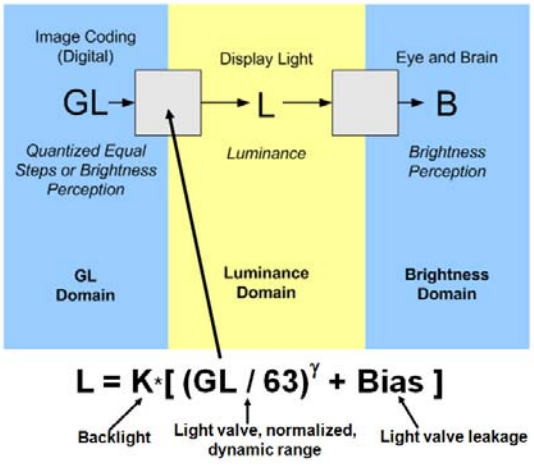


Fig. 3.9 The transform function of display system.

Fig. 3.10 shows a voltage versus transmission curve of the liquid crystal in CPT process. From this figure, we can know this liquid crystal is a normally white TN-type liquid crystal. We can calculate the pixel voltage with gamma value of 2.2 by using the transform function in equation (3 - 5) and the V-T curve of this liquid crystal. The pixel voltage corresponded to each gray level is shown in Table 3.2.

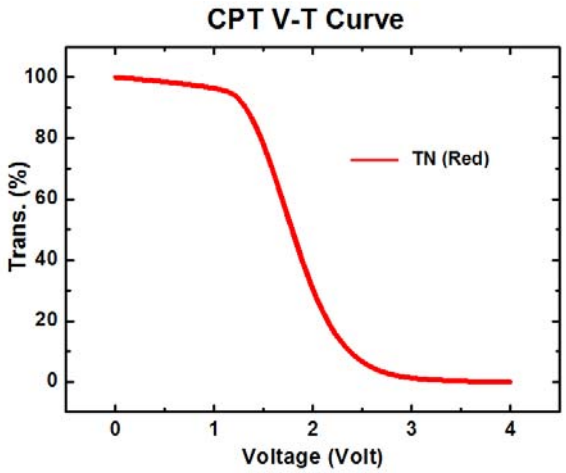


Fig. 3.10 The voltage vs. transmission curve of the liquid crystal in CPT process.

Table 3.2

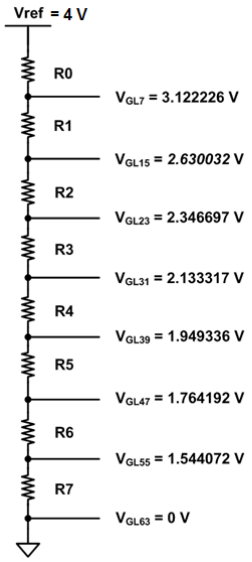
The pixel voltage corresponded to each gray level with gamma of 2.2.

GL	T%	Vp (V)	GL	T%	Vp (V)	GL	T%	Vp (V)	GL	T%	Vp (V)
0	0	***4***	16	4.903597	***2.5879***	32	22.53101	***2.109766***	48	54.97706	***1.74***
1	0.011001	***3.9***	17	5.60323	***2.548154***	33	24.10913	***2.086728***	49	57.52838	***1.71465***
2	0.050549	***3.758902***	18	6.354045	***2.510975***	34	25.74568	***2.063205***	50	60.14296	***1.688701***
3	0.123344	***3.613312***	19	7.156632	***2.47524***	35	27.44104	***2.04***	51	62.82105	***1.66249***
4	0.232264	***3.457736***	20	8.011554	***2.441479***	36	29.19553	***2.017145***	52	65.5629	***1.635021***
5	0.379476	***3.327016***	21	8.919351	***2.408688***	37	31.00949	***1.994362***	53	68.36876	***1.606405***
6	0.56674	***3.217753***	22	9.88054	***2.376906***	38	32.88325	***1.971823***	54	71.23888	***1.576317***
7	0.795548	***3.122226***	23	10.89562	***2.346697***	39	34.81713	***1.949336***	55	74.17349	***1.544072***
8	1.067207	***3.035698***	24	11.96508	***2.317437***	40	36.81144	***1.926691***	56	77.17283	***1.50949***
9	1.382879	***2.959477***	25	13.08937	***2.289892***	41	38.86649	***1.90363***	57	80.23715	***1.471855***
10	1.743616	***2.892731***	26	14.26895	***2.261672***	42	40.98257	***1.881031***	58	83.36666	***1.42963***
11	2.150377	***2.83195***	27	15.50426	***2.234607***	43	43.16	***1.858031***	59	86.56159	***1.382006***
12	2.604051	***2.774818***	28	16.79571	***2.208712***	44	45.39904	***1.834985***	60	89.82217	***1.324149***
13	3.105462	***2.723289***	29	18.14372	***2.182949***	45	47.69999	***1.81194***	61	93.14862	***1.249646***
14	3.655379	***2.675385***	30	19.54869	***2.157501***	46	50.06313	***1.788369***	62	96.54116	***1.1297***
15	4.25453	***2.630032***	31	21.01099	***2.133317***	47	52.48873	***1.764192***	63	100	***0***

As shown in the Table 3.2, we can find each target pixel value. The voltage-dividing method of the resistor string is adopted. First, we divide this R-string ladder into 8 interval values fitting to the target pixel value. Then, we divide each section of R-string into 8 the same sub-interval R-string. The value of each resistor in this R-string is designed in the Table 3.3 and the simulation result of the voltage divider of R-string is shown in Fig. 3.11.

Table 3.3

The resistance values of R-string for gamma correction design.



R0	*43.9k*	R1	*24.6k*	R2	*14.15k*	R3	*10.65k*
R00	5.4875k	R10	3.075k	R20	1.76875k	R30	1.33125k
R01	5.4875k	R11	3.075k	R21	1.76875k	R31	1.33125k
R02	5.4875k	R12	3.075k	R22	1.76875k	R32	1.33125k
R03	5.4875k	R13	3.075k	R23	1.76875k	R33	1.33125k
R04	5.4875k	R14	3.075k	R24	1.76875k	R34	1.33125k
R05	5.4875k	R15	3.075k	R25	1.76875k	R35	1.33125k
R06	5.4875k	R16	3.075k	R26	1.76875k	R36	1.33125k
R07	5.4875k	R17	3.075k	R27	1.76875k	R37	1.33125k
R4	*9.2k*	R5	*9.25k*	R6	*11k*	R7	*77.2k*
R40	1.15k	R50	1.15625k	R60	1.375k	R70	9.65k
R41	1.15k	R51	1.15625k	R61	1.375k	R71	9.65k
R42	1.15k	R52	1.15625k	R62	1.375k	R72	9.65k
R43	1.15k	R53	1.15625k	R63	1.375k	R73	9.65k
R44	1.15k	R54	1.15625k	R64	1.375k	R74	9.65k
R45	1.15k	R55	1.15625k	R65	1.375k	R75	9.65k
R46	1.15k	R56	1.15625k	R66	1.375k	R76	9.65k
R47	1.15k	R57	1.15625k	R67	1.375k	R77	9.65k

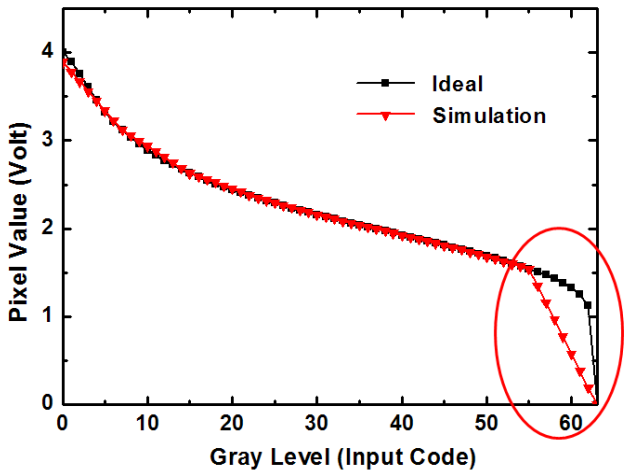
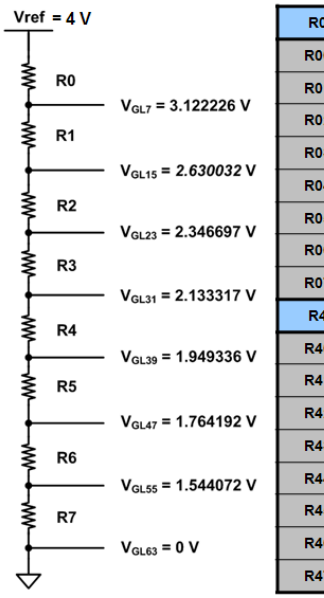


Fig. 3.11 The gray level vs. pixel value curve in the voltage divider of R-string.

From above simulation result, we can see that the pixel values of last 8 bits are not fit to the ideal values. This is because of the same interval in the last 8-bit section is not suitable for this design. The modified R-string ladder is designed in Table 3.4 and the simulation result of the voltage divider of R-string is shown in Fig. 3.12. As shown in the simulation result, we can find that all pixel values are fitter to the ideal values due to the modified R-string ladder.

Table 3.4

The modified resistance values of R-string for gamma correction design.



R0	43.9k	R1	24.6k	R2	14.15k	R3	10.65k
R00	5.4875k	R10	3.075k	R20	1.76875k	R30	1.33125k
R01	5.4875k	R11	3.075k	R21	1.76875k	R31	1.33125k
R02	5.4875k	R12	3.075k	R22	1.76875k	R32	1.33125k
R03	5.4875k	R13	3.075k	R23	1.76875k	R33	1.33125k
R04	5.4875k	R14	3.075k	R24	1.76875k	R34	1.33125k
R05	5.4875k	R15	3.075k	R25	1.76875k	R35	1.33125k
R06	5.4875k	R16	3.075k	R26	1.76875k	R36	1.33125k
R07	5.4875k	R17	3.075k	R27	1.76875k	R37	1.33125k
R4	9.2k	R5	9.25k	R6	11k	R7	77.2k
R40	1.15k	R50	1.15625k	R60	1.375k	R70	2.96k
R41	1.15k	R51	1.15625k	R61	1.375k	R71	2.96k
R42	1.15k	R52	1.15625k	R62	1.375k	R72	2.96k
R43	1.15k	R53	1.15625k	R63	1.375k	R73	2.96k
R44	1.15k	R54	1.15625k	R64	1.375k	R74	2.96k
R45	1.15k	R55	1.15625k	R65	1.375k	R75	2.96k
R46	1.15k	R56	1.15625k	R66	1.375k	R76	2.96k
R47	1.15k	R57	1.15625k	R67	1.375k	R77	56.48k

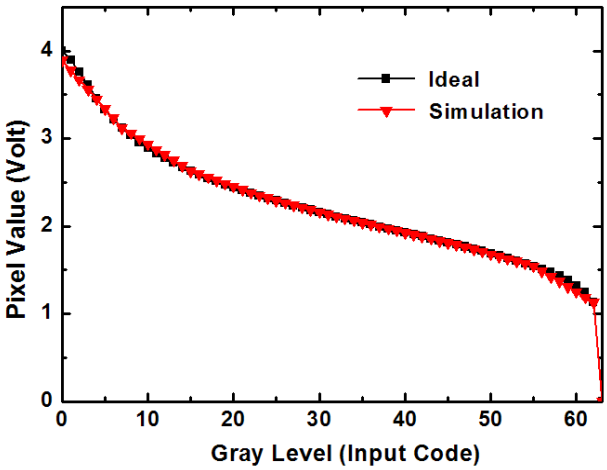


Fig. 3.12 The GL vs. pixel value curve in the modified voltage divider of R-string.

3.3.2 Circuit Description

From above discussions, we know that the R-string DAC with digital decoding is a valid technique for reducing the loading of the output node. It also has a simple structure for layout floorplan and suitable for gamma correction design. But this architecture has too large area of the decoder in high resolution DAC. For this reason, we have proposed a new architecture to reduce the area of the decoder. The transistor number of the decoder is not linearly increased but exponentially increased with the growing of the bit number. Therefore, we divided a decoder into two decoders to reduce the area of the decoder. The folded R-string DAC with segmented digital decoders is shown in Fig. 3.13. The area of the decoders in the 6-bit DAC can be reduced to about one sixth by using this segmented architecture.

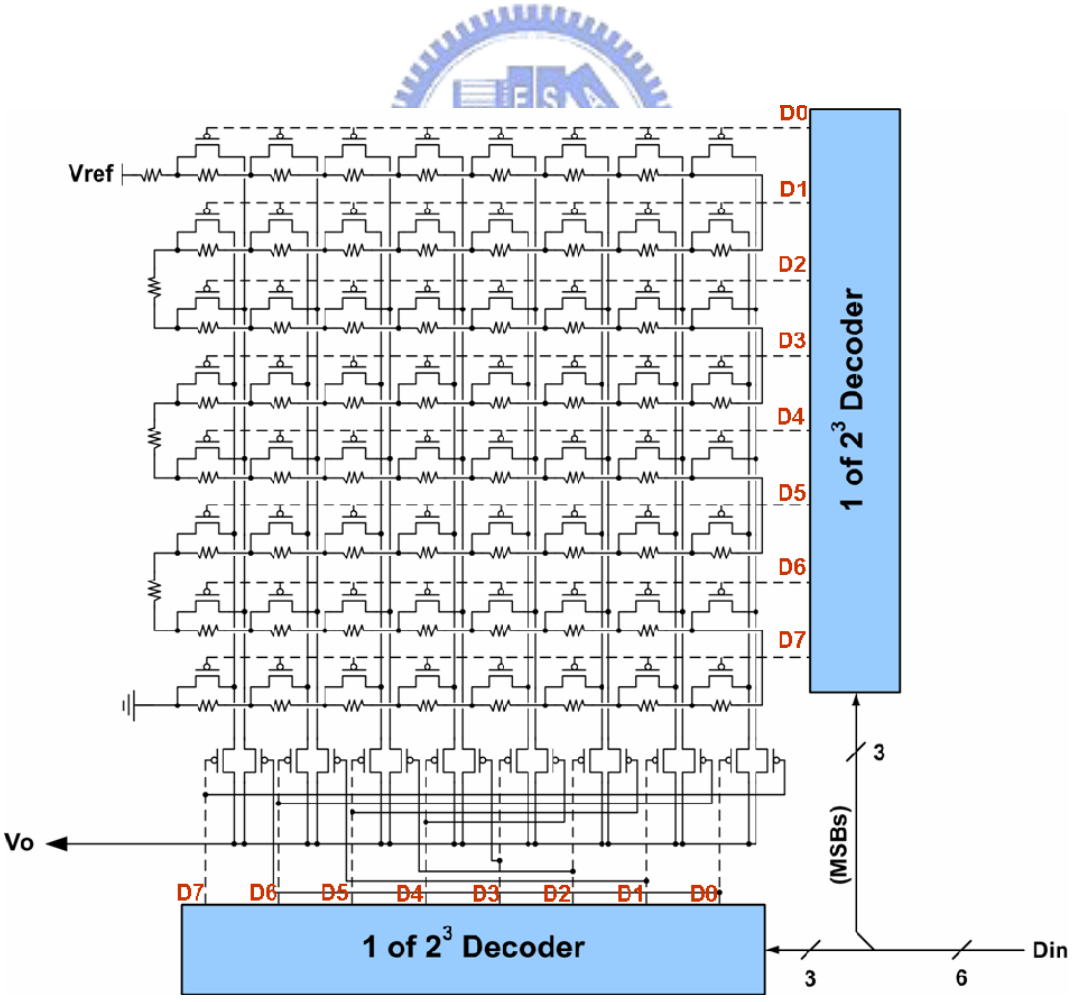


Fig. 3.13 The folded R-string DAC with segmented digital decoders.

In this work, we propose a novel digital-to-analog converter with gamma correction for on-panel data driver in LTPS technology. The purpose of low dimension and low complexity can be achieved by this architecture of the folded R-string DAC with segmented digital decoders. This DAC is composed of folded R-string, switch array, two segmented decoders, and reordering decoding circuit. The operating illustration of this 6-bit folded R-string DAC with segmented digital decoders is shown in Fig. 3.14. For example, when the input signal Din is 000000, this input signal will be segmented into two parts (MSBs and LSBs). The MSBs (000) and the LSBs (000) of the input signal are assigned to high-bit decoder and low-bit decoder, respectively. The output signal (D0) of the low-bit decoder will turn on the switches Ms08, Ms18, and their signal paths because its input is 000. In the same way, the output of high-bit decoder will turn on the top row of the switch array.

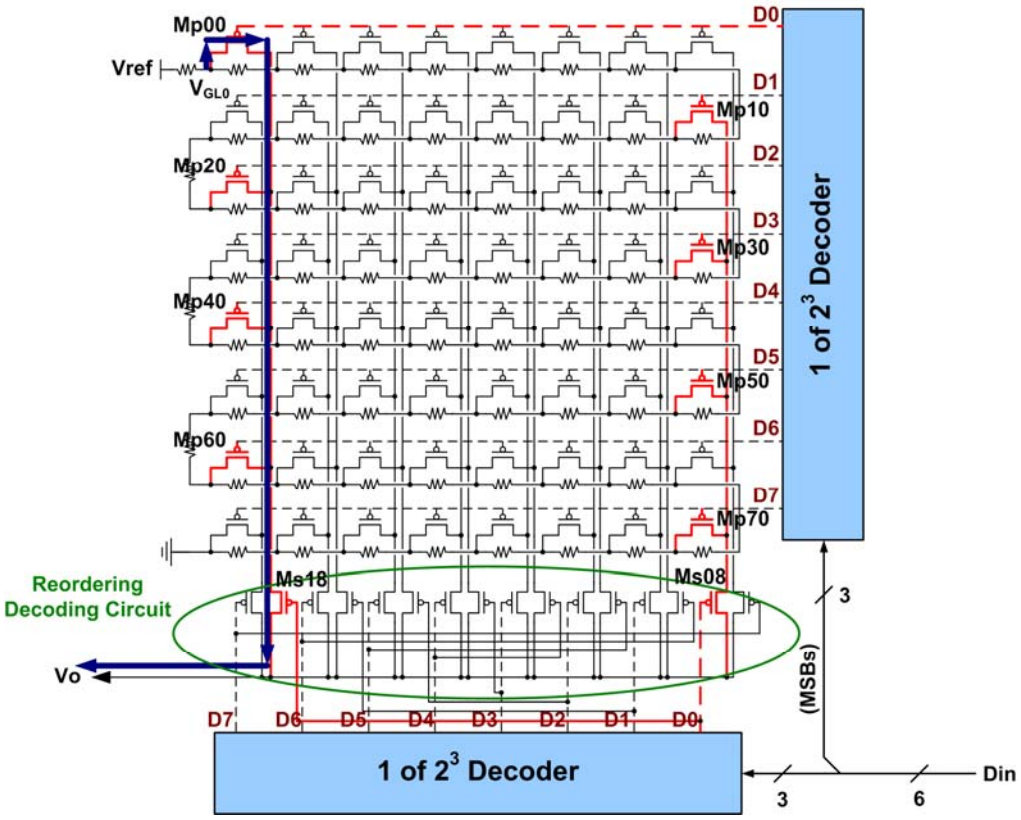


Fig. 3.14 The operation illustration of the 6-bit folded R-string DAC with segmented digital decoders.

With a resistor-string approach, the DAC has guaranteed monotonicity since any section on the resistor string must has a low voltage than its upper, neighbor section. It also has higher accuracy because the accuracy of the R-string DAC is dependent on the ratio of resistors, not dependent on absolute resistor values [16]. Furthermore, the area of the R-string DAC can be reduced by using the folded R-string and the segmented digital decoders. The reordering decoding circuit can simplify the decoder circuit. The partial decoding function is replaced by the signal paths routing of the reordering decoding circuit. For this reason, the fundamental decoders can be used for the segmented digital decoders. Fig. 3.15 is shown that the transistors of the decoders can be decreased from 780 to 124 in 6-bit DACs. The area of the R-string DAC can be effectively reduced to about one sixth by using this proposed architecture. This proposed 6-bit folded R-string DAC with segmented digital decoders is also more suitable for gamma correction design in TFT-LCD panel.

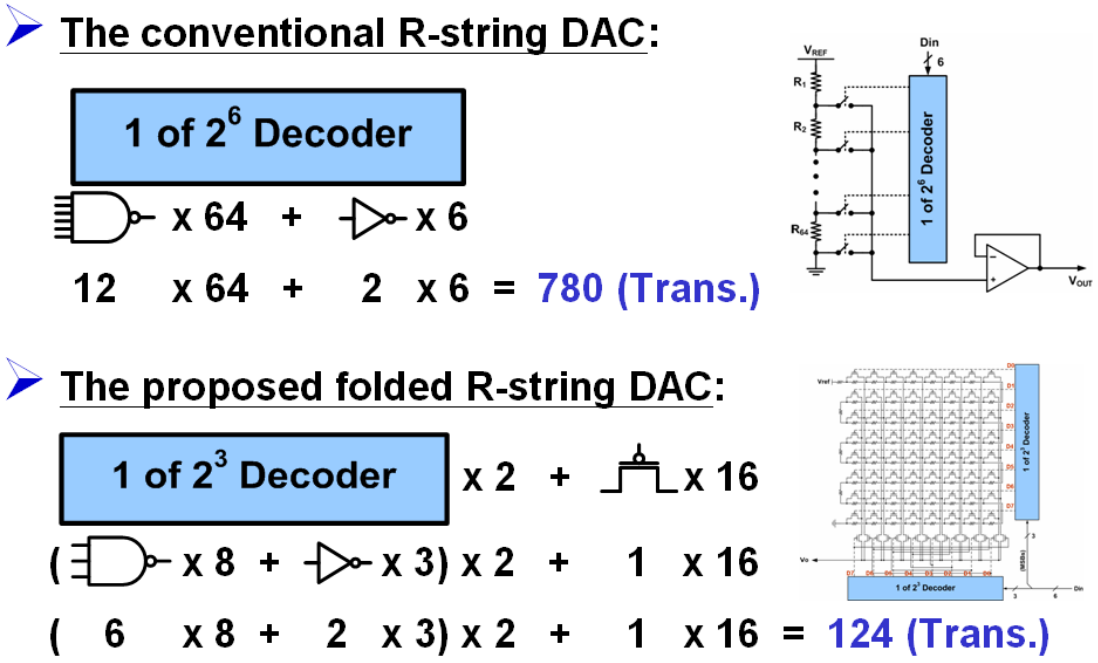


Fig. 3.15 The comparison of the transistors number of the decoders between the conventional and proposed 6-bit R-string DAC.

3.3.3 Simulation and Verification

According to previous sections in this chapter, we can get whole architecture of this 6-bit R-string DAC (as shown in Fig. 3.13) and all resistance values of R-string for gamma correction design (as shown in Table 3.4). This proposed 6-bit folded R-string DAC with segmented digital decoders has four voltage sources: V_{DD} = 6 V, V_{SS} = -2 V, V_{ref} = 4 V, and GND = 0 V. The first two voltage sources are used for digital decoders. The rest of voltage sources are used for R-string ladder. This proposed DAC has been successfully verified in 8-μm LTPS technology. The simulation result of this DAC, assigned a series of digital input codes from 000000 (0) to 111111 (63) at 100-kHz operation frequency, is shown in Fig. 3.16. The average power consumption of the proposed DAC is 82.047 μW and the average current through R-string is 20.007 μA. From above results, we know that the power consumption is dominated by the R-string ladder in this proposed 6-bit DAC.

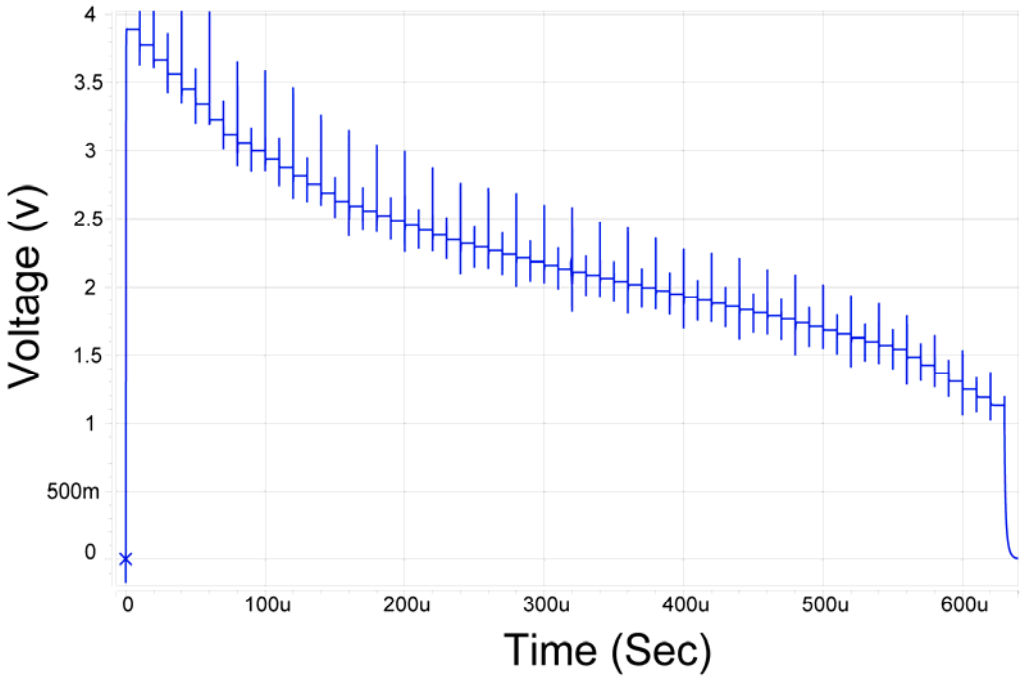


Fig. 3.16 The simulation result of this 6-bit folded R-string DAC with segmented digital decoders in 8-μm technology.

Table 3.5 and Fig. 3.17 show the voltage values and the GL vs. output voltage curves in ideal condition, R-string ladder, and this proposed DAC.

Table 3.5
The voltage values in ideal condition, R-string ladder, and this proposed DAC corresponded to each gray level. Unit: volt.

GL	Ideal	R-String	R-DAC	GL	Ideal	R-String	R-DAC	GL	Ideal	R-String	R-DAC	GL	Ideal	R-String	R-DAC
0	4	3.89	3.89	16	2.588	2.594	2.594	32	2.11	2.111	2.111	48	1.74	1.737	1.737
1	3.9	3.78	3.781	17	2.548	2.559	2.559	33	2.087	2.088	2.088	49	1.715	1.709	1.71
2	3.759	3.671	3.671	18	2.511	2.524	2.524	34	2.063	2.065	2.065	50	1.689	1.682	1.682
3	3.613	3.561	3.561	19	2.475	2.488	2.488	35	2.04	2.042	2.042	51	1.662	1.654	1.654
4	3.458	3.451	3.451	20	2.441	2.453	2.453	36	2.017	2.019	2.019	52	1.635	1.627	1.627
5	3.327	3.341	3.341	21	2.409	2.417	2.417	37	1.994	1.996	1.996	53	1.606	1.599	1.599
6	3.218	3.232	3.232	22	2.377	2.382	2.382	38	1.972	1.973	1.973	54	1.576	1.572	1.572
7	3.122	3.122	3.122	23	2.347	2.347	2.347	39	1.949	1.95	1.95	55	1.544	1.544	1.544
8	3.036	3.06	3.06	24	2.317	2.32	2.32	40	1.927	1.926	1.926	56	1.509	1.485	1.485
9	2.959	2.999	2.999	25	2.29	2.293	2.293	41	1.904	1.903	1.903	57	1.472	1.426	1.426
10	2.893	2.937	2.937	26	2.262	2.267	2.267	42	1.881	1.88	1.88	58	1.43	1.367	1.367
11	2.832	2.876	2.876	27	2.235	2.24	2.24	43	1.858	1.857	1.857	59	1.382	1.308	1.308
12	2.775	2.814	2.814	28	2.209	2.213	2.213	44	1.835	1.834	1.834	60	1.324	1.248	1.248
13	2.723	2.753	2.753	29	2.183	2.187	2.187	45	1.812	1.811	1.811	61	1.25	1.189	1.189
14	2.675	2.691	2.691	30	2.158	2.16	2.16	46	1.788	1.788	1.788	62	1.13	1.13	1.13
15	2.63	2.63	2.63	31	2.133	2.134	2.134	47	1.764	1.764	1.765	63	0	0	0.0052

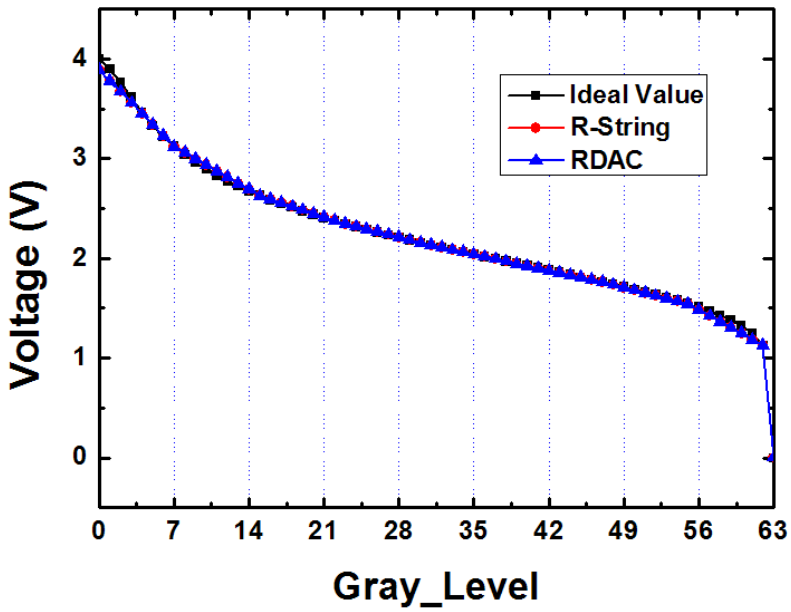
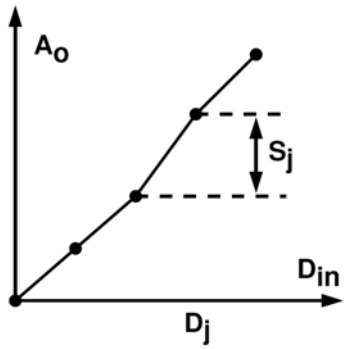


Fig. 3.17 The GL vs. output voltage curves in ideal condition, R-string ladder, and this proposed DAC.

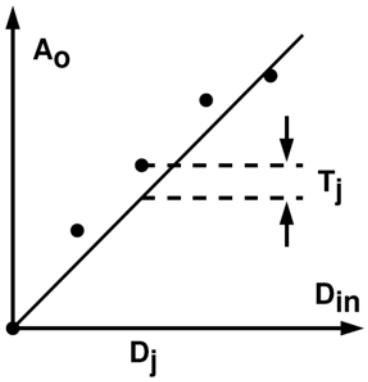
The differential non-linearity (DNL) and integral non-linearity (INL) are important specification of the data converter circuits except offset error and gain error. The definitions of DNL and INL are shown in Fig. 3.18 and Fig. 3.19 [17]. "Δ" is defined as least significant bit (LSB) in the data converter. However, there is a thing should be emphasized. The LSB is not a constant value in the nonlinear system, like this proposed DAC with gamma correction design. For this reason, if the difference between the bit itself and adjacent upper bit is named Diff (N+1) and that between the bit itself and adjacent lower bit is named Diff (N-1), the LSB in nonlinear system is defined as the less one among Diff (N+1) and Diff (N-1). From the simulation result in Table 3.5, we can find that the DNL and INL in this proposed 6-bit DAC almost equal to 0.



$$DNL(D_j) = \frac{S_j - \Delta}{\Delta} \quad (LSB)$$

$$\Delta = \frac{A_{FS}}{2^N}$$

Fig. 3.18 The definition of the differential non-linearity.



$$INL(D_j) = \frac{T_j}{\Delta} \quad (LSB)$$

$$\Delta = \frac{A_{FS}}{2^N}$$

Fig. 3.19 The definition of the integral non-linearity.

This proposed architecture also has been successfully verified in 3-μm LTPS technology. The simulation results are shown in Fig. 3.20 and Fig. 3.21. Based on Fig. 3.20, we can find that the spikes of this DAC can be obviously reduced by the advanced technology. This is because the clock feed-through can be greatly reduced due to the shorter length dimension of transistor.

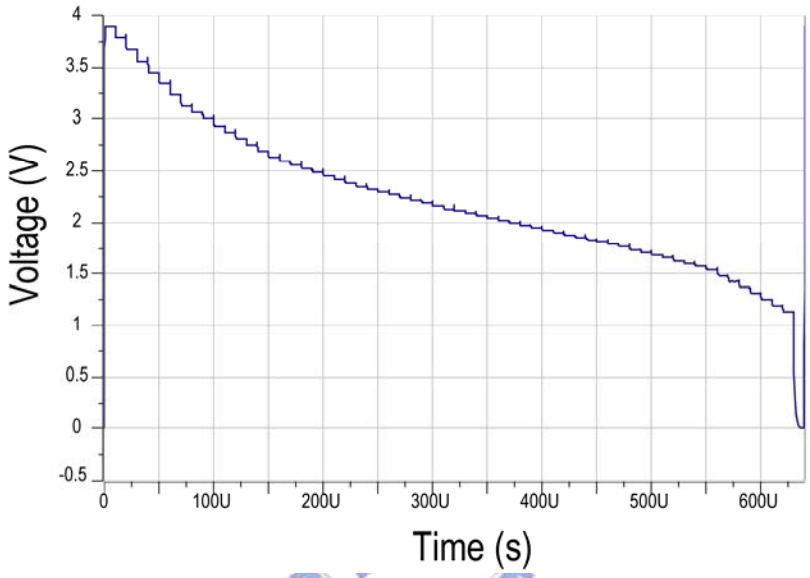


Fig. 3.20 The simulation result of this 6-bit folded R-string DAC with segmented digital decoders in 3-μm technology.

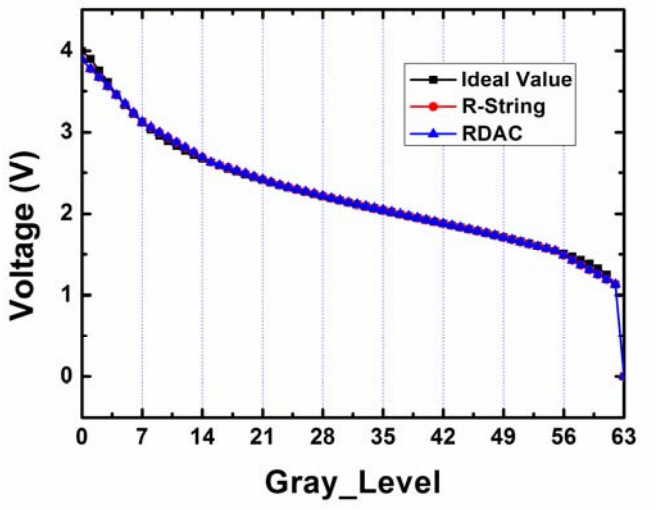


Fig. 3.21 The GL vs. output voltage curves in ideal condition, R-string ladder, and this proposed DAC in 3-μm technology.

In summary, a novel 6-bit folded R-string DAC with gamma correction has been successfully verified in 8-μm and 3-μm LTPS technology. By using the folded R-string and segmented digital decoders, the area of the R-string DAC can be effectively reduced to about one sixth. Furthermore, this architecture is also more suitable for gamma correction design and many kinds of LTPS process. Although, there is only a discussion for normally white TN-type liquid crystal in this chapter. This proposed architecture is also suitable for many kinds of gamma value and normally white (or black) TFT-LCD panel by modifying the R-string value and the decoder architecture.