Chapter 5

Conclusion and Future Works

5.1 CONCLUSION

A novel 6-bit folded R-string DAC with gamma correction for on-panel data driver has been proposed in chapter 3. This proposed DAC has been successfully verified in 8-μm and 3-μm LTPS technology. By using the folded R-string and segmented digital decoders, the area of the R-string DAC can be effectively reduced to about one sixth and the complexity of circuit can be simplified. Furthermore, this architecture is also more suitable for gamma correction design and many kinds of LTPS process. Although, there is only a discussion for normally white TN-type liquid crystal in this thesis. This proposed architecture is also suitable for many kinds of gamma value and normally white (or black) TFT-LCD panel by modifying the R-string value and the decoder architecture.

In chapter 4, a class-A output buffer with device variation suppressing technique in LTPS technology has been proposed and verified in 8-μm LTPS technology. The output buffer with P-TFTs input stage can be operated at 50-kHz operation frequency with at least 1-to-9 V output swing under V_{DD} of 10 V and V_{SS} of 0 V. The slew rate of this proposed output buffer is 1.961 V/μs. The device characteristic variation has been successfully suppressed by replacing the critical part of analog circuits by the P-TFTs. The proposed output buffer with P-TFTs input stage can be used in the on-panel data drivers to provide a uniform brightness and high resolution display.

5.2 FUTRUE WORKS

Although the proposed 6-bit folded R-string DAC in this thesis are successfully designed and verified in LTPS technology. The accuracy of the data driver is determined by DAC circuit combined with analog output buffer. Even though the DAC has high accuracy, the data driver also has not enough accuracy with a low accuracy analog output buffer. This is because that the analog output buffer has large input offset voltage. For this reason, the input offset voltage of the analog output buffer will become a serious issue in data drivers. Fig. 5.1 shows a valid input offset compensation method [20]. In this circuit, the pre-charge buffers first execute rapid charging or discharging of the data-line with respect to the analog signal voltage of the R-DAC. After that, the R-DAC output, which is a signal voltage precisely determined by the reference string resistance, is connected directly to the data-line. By using this method, the offset of the pre-charge buffers can be neglected in this operation mode of the proposed DAC. Furthermore, since the pre-charge buffers carry most of the power load required to charge the data-line, static current through the reference string resistance can be kept to a minimum.

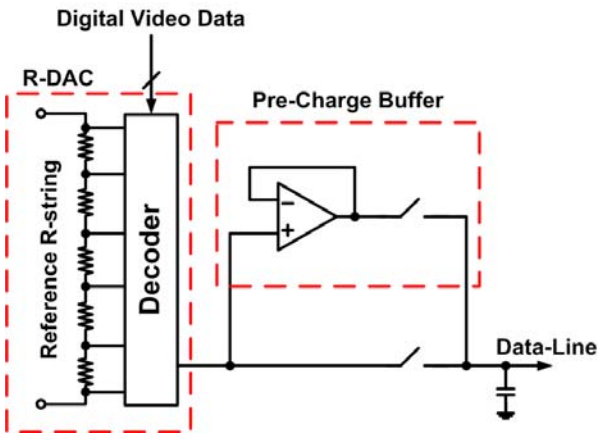

Fig. 5.1 The architecture of the DAC circuit combined with analog output buffer with input offset compensation method in TFT-LCD panel.

In addition, the power dissipation must be minimized while displays are used toward portable applications. The analog output buffer is a critical design to achieve the low power dissipation on TFT-LCD panels. In chapter 4, we propose a class-A output buffer with device variation suppressing technique in LTPS technology. But, the class-A output buffer has a drawback which is less power efficiency. This is because this kind of output buffer always has a DC current path. If we can replace the output stage of the OP amp by class-B or class-AB output stage, the power consumption of analog output buffer will be reduced effectively [29]. For example, Fig. 5.2 shows a class-B analog output buffer with device variation suppressing technique.

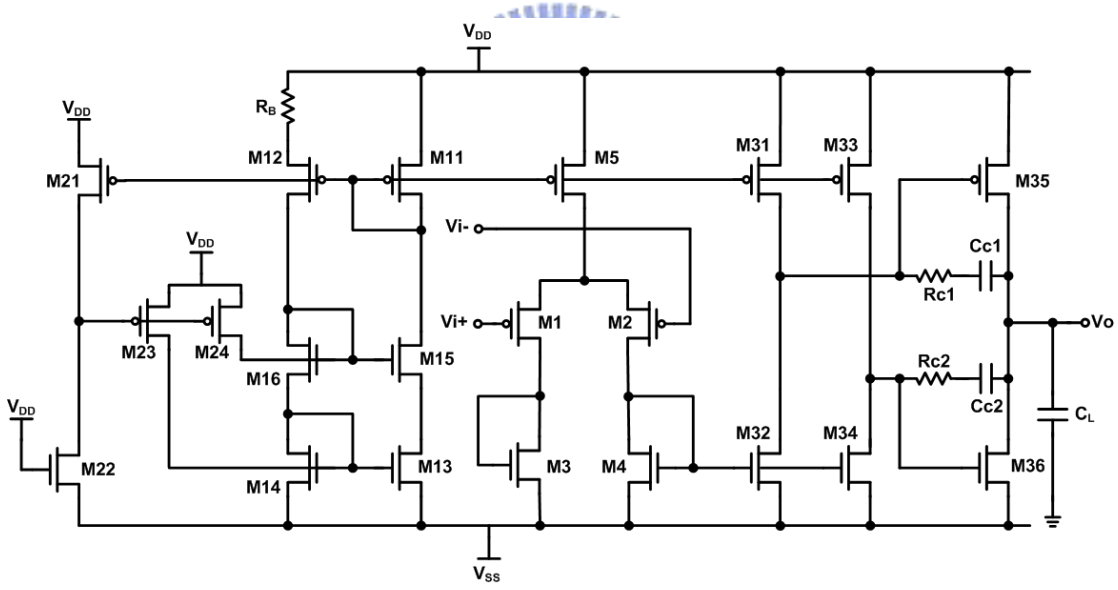

Fig. 5.2 A class-B analog output buffer with device variation suppressing technique.