國 立 交 通 大 學

電子工程學系　電子研究所碩士班

碩　士　論　文

低功率數位式自我校正鎖相迴路

Low Power Digital Phase Locked Loop with Self-Calibration

研 究 生：張巧伶

指導教授：陳巍仁

中華民國九十七年十一月

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碩士論文

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摘要

頻率合成器(Frequency Synthesizer)對於通訊晶片，無論是無線射頻傳輸介面或者高速的序列傳輸介面中，都扮演著非常重要的腳色，影響整個通訊晶片的性能甚大。隨著製程的進步，深次微米(Deep-submicrometer)的互補金氧半(CMOS)製程已廣泛地被應用於數位電路上，使得數位電路得以實現高度密集化、低成本與低功率消耗等需求。類比電路在低電壓的環境下，運作不易，不只增加設計上的難度，也使得類比電路無法隨著製程的演進，降低功率消耗。近年來，有些研究紛紛提出了數位控制振盪器(Digital Controlled Oscillator)的概念，藉由數位訊號來控制振盪器的振盪頻率，其中充電汞、迴路濾波器等的類比電路皆以數位電路取代，配合數位控制振盪器，使得整個迴路得以全數位化，較易操作在低電壓的工作環境下，使整體的功率能夠下降。

本作品實現一個具有低功率數位式自我校正頻率合成器，使用聯電 90nm 1P9M 互補金氧半製程實現，且適用於生物感測器(Bio-sensor)上的收發機(transceiver)，中央頻率為 1.4GHz，預計功率消耗低於 1mW；相位雜訊在距離載波頻率 1MHz 時小於-100dBc/Hz。此外，為兼顧低功率操作與性能穩定之雙重條件，本電路可依據 PVT 的變化自動調整硬體結構，以達到自我校準與操作性能之最佳化。

Low Power Digital Phase Locked Loop with Self-Calibration

Student: Chiao-Ling Chang Advisor: Wei-Zen Chen

Department of Electronics Engineering & Institute of Electronics

National Chiao-Tung University

Abstract

The frequency synthesizer is the key element use for both up-conversion and down-conversion of radio signals, and it also affects the performance of the whole transceiver. Along the progress of the deep-submicron CMOS process, the digital circuits could be implemented more integrative, and reduce the cost and the power consumption of the system. But analog circuits are difficult to operate with lower supply voltage and integrate with digital circuits. In the recent years, some researchers proposed the concept of the digital control oscillator (DCO), and the output frequency could be controlled by the digital codes. If we replace the charge-pump and the filter into digital loop filter, the whole PLL could be digitalized by replacing the charge-pump and the filter into digital loop filter, and the PLL could be operated with low voltage and lower down the power consumption.

This thesis proposes a low power digital phase locked loop with self-calibration circuits. The chip has been implemented in UMC 90nm 1P9M CMOS process and could be used on the transceiver of the Bio-sensor. The

center frequency of the RF output is 1.4GHz, and the expected phase noise at 1MHz offset is below -100dBc/Hz. The prospective total power consumption is lower than 1mW. A DCO calibration circuit is added to suppress the PVT variation and increase the stability of this loop.

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感謝神終於等到這一刻了，歷經了一番掙扎，終於完成了這部拙作。在此也感謝陳巍仁教授在這些日子以來，辛勤的教導與勉勵，才有現在的成果，雖然有點久，但在學期間也學了不少的東西，獲益良多。謝謝我們的大學長台祐，在這段期間的支持與協助。

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張巧伶 17, Nov, 2008

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Chapter 1 Introduction

1.1 Motivation

In the recent year, people could live over seventy years or longer. Health care has become a popular issue in the whole word. Recent technological advances in sensors, low-power microelectronics and miniaturization, and wireless networking enable the design and proliferation of wireless sensor networks capable of autonomously monitoring and controlling environments. A number of these devices has the advantage of allowing patient movement without tethering the patient to a bedside monitor with a hard-wired connection and can be integrated into a Wireless Body Area Network (WBAN), a new enabling technology for health monitoring.

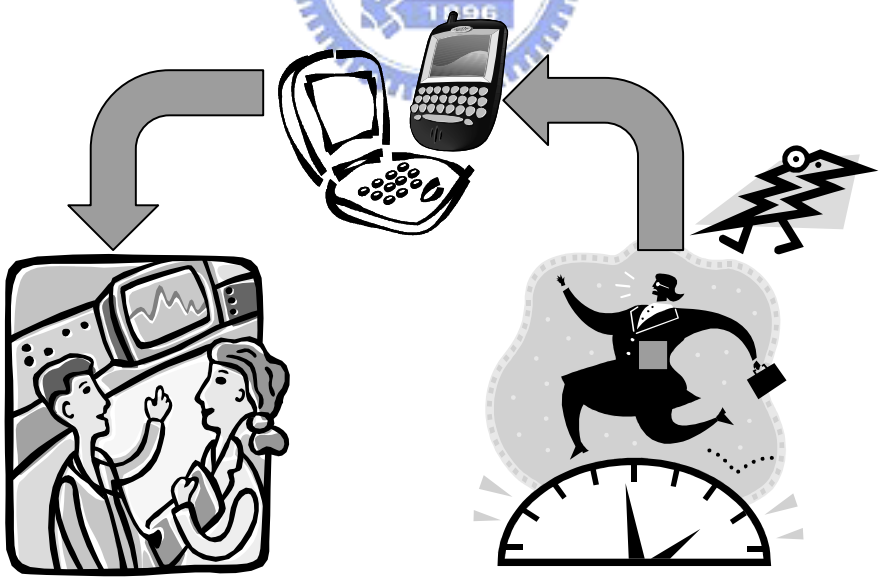


Fig. 1-1 WBAN concept

The concept of WBAN is shown in Fig. 1-1. People can carry a tiny sensor all around without staying beside the monitor. The sensor could get vital signals, such as electrocardiogram (ECG), and transfer the relevant data to a personal

digital assistant (PDA) or a personal computer (PC) through a wireless personal area network implemented using ZigBee (802.15.4) [1] or Bluetooth (802.15.1) [2]. Those devices allow an individual to closely monitor changes in body's vital signs which can provide feedback to help maintain an optimal health status, and these systems can even alert medical personnel when life-threatening changes occur.

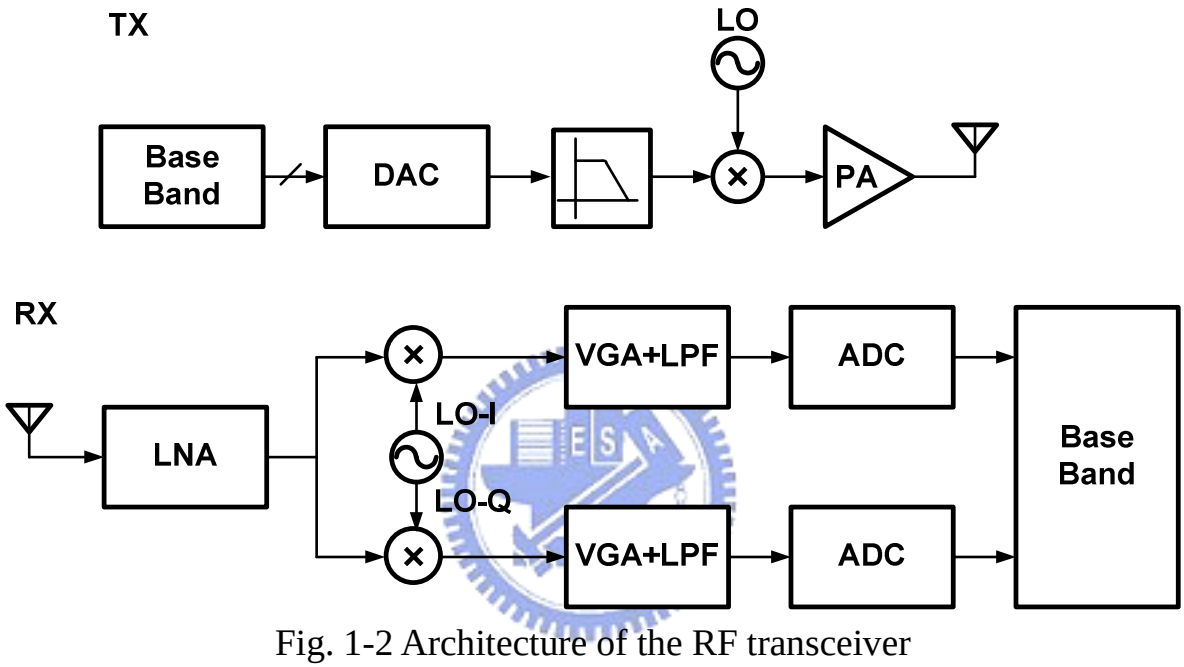


Fig. 1-2 Architecture of the RF transceiver

In this application, a radio frequency (RF) transceiver is necessary for delivering the signal between sensors and local hard ware. The architecture of the RF transceiver is shown in Fig. 1-2. The operation of transceiver is as following. Baseband signal converts to analog signal with a digital-to-analog converter (DAC). Up-conversion mixer mixes carrier frequency generated by local oscillator (LO) and analog signal filtered by low pass filter. The antenna of the transmitter (TX) transfers RF signal which is amplified with power amplifier (PA). The antenna of the receiver (RX) receives the RF signal and delivers to a low noise amplifier (LNA) to amplify the received signal. RF signal is converted to baseband signal with a mixer and LO. A variable gain amplifier (VGA) and

low pass filter (LPF) is used for amplifying the received signal and filtering the noise produced by higher frequency, and then the output baseband signal is converted to digital signal with an analog-to-digital converter (ADC).

Frequency synthesizer is a key element in transceiver and is generally implemented by phase-locked loop (PLL). A sub-μW PLL is necessary for reducing the power consumption of the whole system. The central frequency for ZigBee (IEEE 802.15.4) or Bluetooth is about 2.4GHz, which might be interfered by other application, such as 802.11 a, b, g. Federal Communication Commission (FCC) has voted to adopt new rules establishing a service for wireless medical telemetry devices [3]. The Wireless Medical Telemetry Service (WMTS) report and order sets aside the frequencies of: 1395 to 1400 MHz and 1429 to 1432 MHz for primary or co-primary use by eligible wireless medical telemetry users. This action creates frequencies where medical telemetry will enjoy protection against interference from other in-band RF sources and reduce power consumption by lower central frequency.

We propose a low power PLL with self-calibration in this thesis. The specification of this proposed PLL is shown in Table 1-1.

Table 1-1 Specification of the proposed PLL

Parameter	Value
Process	UMC 90nm
Output Frequency	1.4GHz
Reference Frequency	4MHz
Supply Voltage	1V
Power Dissipation	<1mW
Phase Noise @ 1MHz	<-100dBc/Hz
Resolution	<20ppm

1.2 Overview of Thesis

The organization of this thesis is as follows. In Chapter 2, we propose a new architecture of low power PLL. We give a behavior model and an analyze method for the new architecture in Chapter 3. We implement each block in Chapter 4. Experimental results are provided in Chapter 5 and this thesis is concluded following a discussion in Chapter 6.

Chapter 2 Architecture

2.1 Prior Art

Emerging wireless sensor network applications call for radio architectures where size and current consumption are major design criteria. Many studies [4]-[6] have been carried out on frequency synthesizer based on a charge-pump PLL [7]. The basic concept of charge-pump PLL is shown as Fig. 2-1.

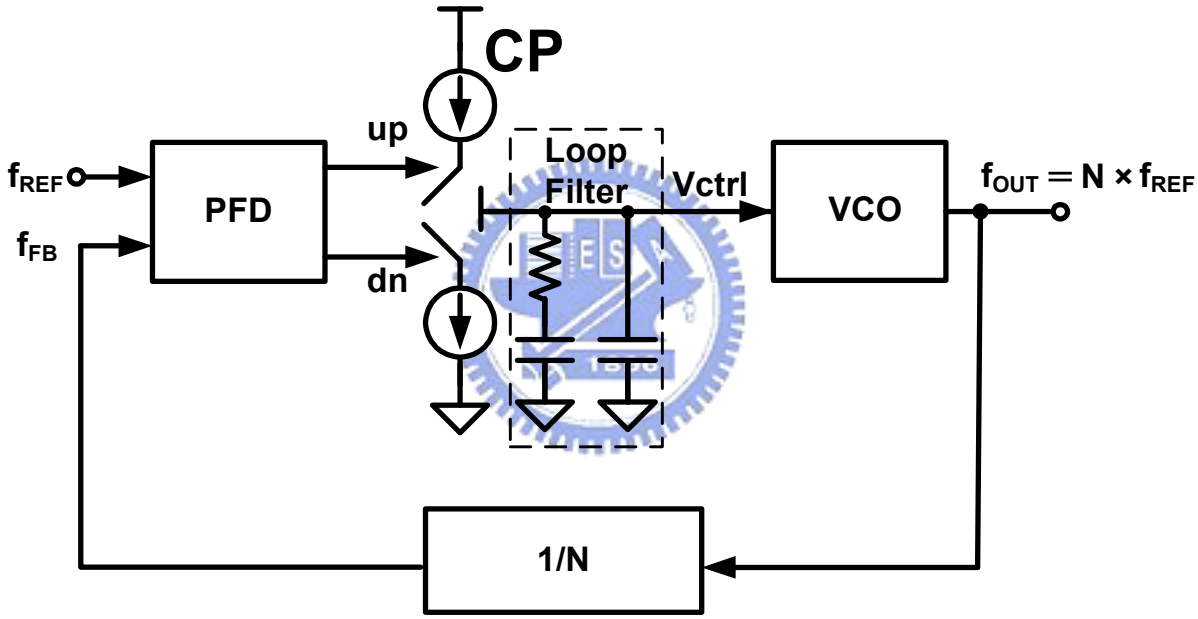


Fig. 2-1 Architecture of charge-pump PLL

In this architecture a voltage control oscillator (VCO) generates a periodic output signal having a frequency f_{OUT} determined by a control voltage Vctrl. The output signal is divided by a frequency divider. The output frequency of the frequency divider f_{FB} is $f_{FB}=f_{OUT}/N$, where N is the divide ratio and could be integer or fractional. A phase frequency detector (PFD) compares the phase or frequency of the feedback clock f_{FB} against between reference frequency f_{REF}. The information on the phase or frequency difference activates the charge-pump (CP) and the CP varies the control voltage Vctrl to adjust the output frequency

of the VCO. A loop filter is used to reduce the noise formed by the CP. This loop locks when the phase difference drops to zero.

With the explosive growth of the processes, the use of deep-submicrometer CMOS processes allows for an unprecedented degree of scaling and integration in digital circuitry, but complicates the implementation of traditional RF and analog circuits. In the advance processes, the channel length of CMOS transistors becomes shorter to reduce the chip area, and the supply voltage of the circuits becomes lower to diminish the power consumption. The gate oxide of CMOS transistors gets thinner to enhance the driving strength in the advance processes. The current leakage of the transistors gets larger because of the thinner gate oxide that causes current mismatch in the CP. The range of the control voltage of the VCO shrinks because of the lower supply voltage that makes higher gain of the VCO. The VCO would be very susceptible to the noise of the control voltage that makes the VCO difficult to control.

Recently, a digitally controlled oscillator (DCO), which deliberately avoids any analog tuning voltage controls, was first ever presented in [8] for RF wireless applications. This allows for its loop control circuitry to be implemented in a fully digital manner. Staszewski develops an architecture of all-digital PLL (ADPLL) [9][10] which could integrate with digital circuitry. Fig. 2-2 shows the structure of Staszewski's ADPLL [10].

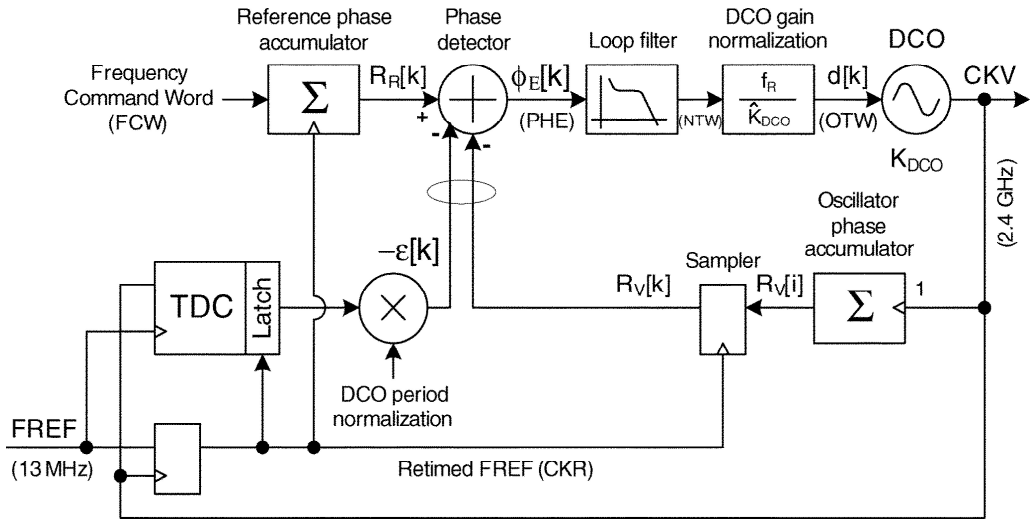


Fig. 2-2 Structure of Staszewski's ADPLL [10]

In Fig. 2-2, a digital control oscillator (DCO) generates a periodic signal CKV and feedbacks to an oscillator phase accumulator. The variable phase signal $R_V[i]$ is determined by counting the number of the rising clock transitions of the DCO oscillator clock. The reference phase signal $R_R[k]$ is obtained by accumulating by frequency command word (FCW) with every rising edge of the retimed frequency reference clock (CKR). FCW is the integer divide ratio of the target frequency to the reference frequency. A phase detector compares the difference of the sampled variable phase $R_V[k]$ and the reference phase $R_R[k]$ and gives an adjust signal which is conditioned by digital loop filter and modifies the output frequency of DCO. A time-to-digital converter (TDC) is used to increase the resolution of the phase error between reference clock and output signal. DCO gain normalization is needed to precisely establish the loop bandwidth. Because most of the circuits in this architecture are design in the digital manner, the ADPLL is easily implemented with the synthesis tool and is compatible with other digital circuits. In this way, the cost and the power consumption of the ADPLL could be shrunk with the development of CMOS process and integrated with digital circuitry.

Although many studies have been published concerning ADPLL, little attention has been paid to reduce power consumption in ADPLL. The DCO in ADPLL consumes about 25mW in a 90nm digital CMOS process [11] because of the LC oscillator. Fig. 2-3 is the architecture of the DCO which is controlled by varactor bank with digital codes. To diminish the power consumption of the DCO, the quality factor (Q) of the varactor needs to be high enough, and that is difficult to implement. If we use ring oscillator for DCO, we could lower the power consumption of the DCO, but the gain of DCO would be higher with lower supply voltage that makes DCO more sensitive to the noise.

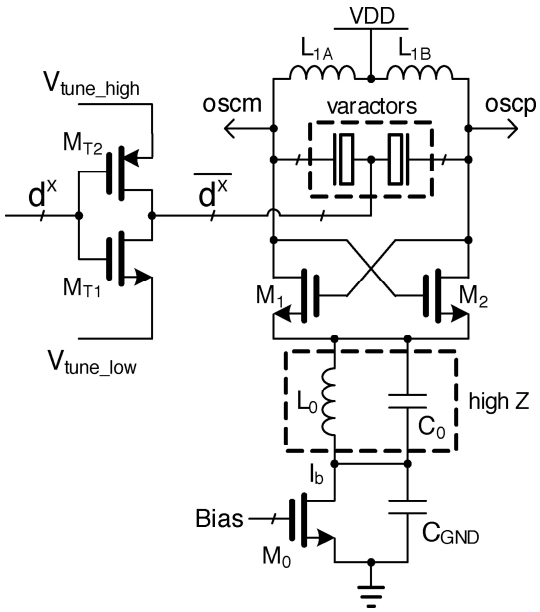


Fig. 2-3 Architecture of Staszewski's DCO [11]

In this thesis, we present a method to control a high gain DCO which could operate with low supply voltage. This study aims to present a low power ADPLL which could integrate with digital circuitry and oppose with process, voltage, and temperature (PVT) variation. The following section shows the proposed architecture of the low power ADPLL.

2.2 Proposed Architecture of the Low Power ADPLL

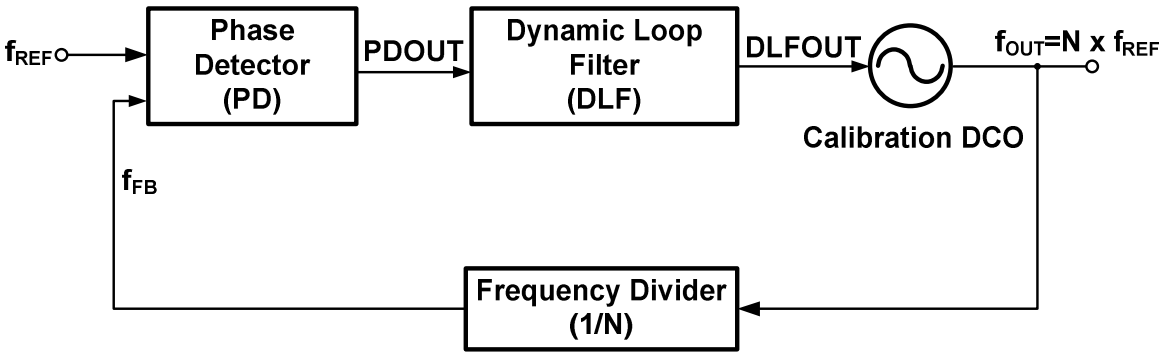


Fig. 2-4 Architecture of the proposed ADPLL

The proposed architecture of all-digital PLL (ADPLL) is shown as Fig. 2-4. This architecture includes a calibration digital controlled oscillator (Calibration DCO), a frequency divider, a phase detector (PD), and a dynamic loop filter (DLF). The basic operation of the ADPLL is as following. The Calibration DCO generates a periodic clock and is divided by the frequency divider. The output frequency of the frequency divider is f_{Out}/N. The phase detector compares the phase difference between reference frequency f_{Ref} and feedback clock f_{FB} and delivers the adjust signal PDOUT to the DLF. The DLF produces the control code of the DCO to modify the output frequency of the DCO. The loop becomes stable when the output frequency f_{OUT} is N times of reference frequency f_{REF}.

The charge pump in conventional architecture is replaced by the DLF whish is composed with digital circuits and overcomes the non-idea effect in charge pump. The DLF also adds a mechanism to adjust the loop bandwidth automatically to shorten the acquisition time. The calibration DCO is used to oppose against the PVT variation and make the implemented loop transfer

function approach our target design. The detail description of the DLF and the calibration DCO is written in Chapter 4.

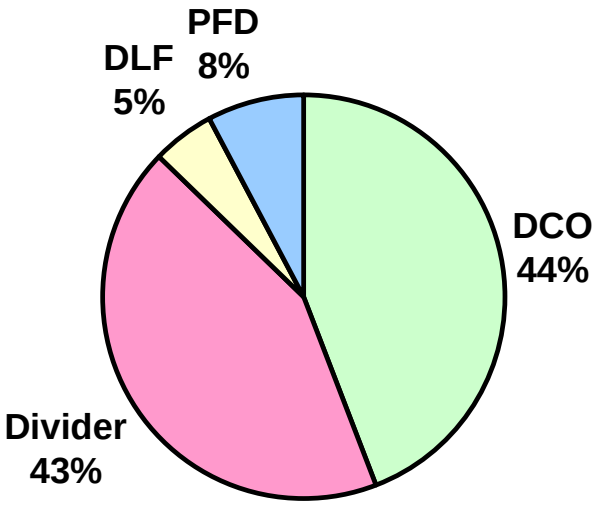


Fig. 2-5 The distribution of power consumption in each building block in a PLL

The distribution of power consumption in each building block of a PLL is illustrated in Fig. 2-5. In general speaking, the DCO uses almost half of total power consumption. If the power consumption of the DCO is reduced, the total power of the PLL would be decreased efficiently. From specification in Table 1-1 and the distribution of the total power, the power consumption of the DCO should be less than 450μW. The control current of the DCO has to be reduced to less than hundred micro watts to save more power, but the gain of the DCO might be higher that make the DCO difficult to control and sensitive to the noise on the control current or voltage.

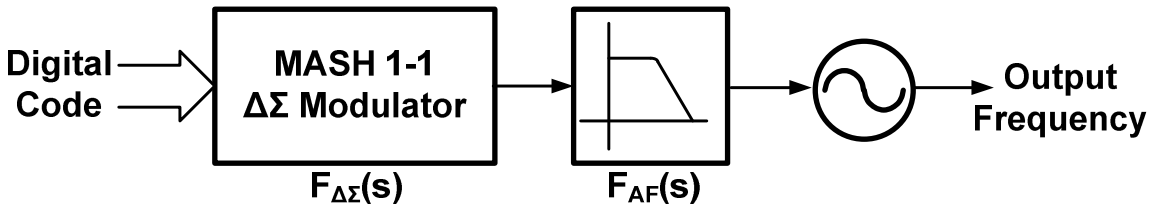


Fig. 2-6 The concept of the DCO

A ΔΣ modulator could provide high resolution, so we introduce a ΔΣ modulator to control a high gain DCO. The concept of the DCO is shown as Fig. 2-6. A filter is added at the output of the ΔΣ modulator to reduce the quantization

noise which is injected by the ΔΣ modulator. The width of the accumulator in the ΔΣ modulator decides the resolution of the DCO and the quantization noise which would affect the phase noise performance of the DCO. To solve this problem, the effects of the bit number of the ΔΣ modulator and the bandwidth of the filter to the noise performance will be investigated in the following chapter.

Chapter 3 Analysis of the ADPLL

3.1 The Dynamics of the ADPLL

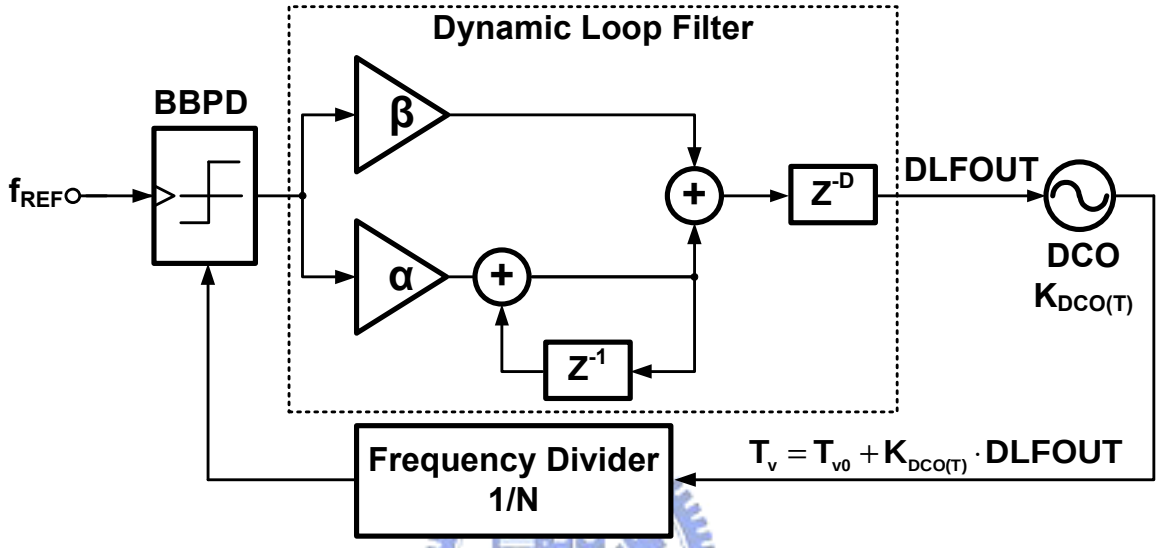


Fig. 3-1 The ADPLL time domain model

The bang-bang PD (BBPD) in the ADPLL introduces nonlinearity in the loop that invalidates the traditional Laplace domain analysis used in linear PLLs. Some researchers provide time domain analysis in the recent years [12]. The ADPLL time domain model is illustrated in Fig. 3-1, where T_v, D, and $K_{DCO(T)}$ mean the period gain of the DCO output, the total loop delay normalized to the period of reference clock f_{REF}, and the gain of DCO which is expressed in equation 3.1.

$$K_{DCO(T)} = \frac{\Delta T_v}{\Delta Code} \qquad (3.1)$$

According to his analyze, this loop would be stable when the parameters of the dynamic loop filter, β and α, fit in the following condition:

$$\frac{\alpha}{\beta} < \frac{2}{2D+1} \qquad (3.2)$$

The architecture of the BBPD provides one clock delay which is described in section 4.1. To avoid the data racing in the DLF, one register is put between the DLF and the DCO, so that induces one clock delay. We assume the loop delay D as 2. The ratio of α to β must be less than 0.4, so let α=1 and β=8.

3.2 Linear Model of the ADPLL

The block diagram of the ADPLL can be shown as Fig. 2-4. The linear model of each block would be derived in the following section, and we would give a complete linear model of the PLL in section 3.2.5.

3.2.1 Linear Model of the DCO

The output frequency of the DCO could be varied according to the input code and it could be expressed as equation 3.3

$$f_{OUT}(t) = f_1 + K_{DCO} \times DLFOUT(t) \qquad (3.3)$$

, where f_1 is the running frequency of the DCO, and K_{DCO} is the gain of the DCO of which the unit is Hert/LSB. The angular frequency of the DCO could be derived as equation 3.4 which is rewritten by equation 3.3.

$$\omega_{OUT}(t) = \omega_1 + 2\pi K_{DCO} \times DLFOUT(t) \qquad (3.4)$$

The phase of the $\omega_o(t)$ is

$$\int_0^t \omega_{OUT}(\tau)d\tau = \omega_1 t + 2\pi K_{DCO} \int_0^t DLFOUT(\tau)d\tau$$

$$\phi_{OUT} = \phi_1 + \phi_o$$

, where Φ_o is the excess phase of the output which could be written as

$$\phi_o(s) = \frac{2\pi K_{DCO}}{s} DLFOUT(s)$$

3.2.2 Linear Model of the Frequency Divider

The relationship of the input and output of the frequency divider could be expressed in equation 3.5.

$$f_{OUT}(t) = Nf_{FB}(t) \qquad (3.5)$$

From equation 3.5, the transfer function of the frequency divider could be derived as following.

$$\frac{f_{FB}(s)}{f_{OUT}(s)} = \frac{1}{N} \qquad (3.6)$$

3.2.3 Linear Model of the Bang-Bang PD

In this structure, the BBPD is the only nonlinear element and the gain K_{bpd} depends on the jitter between the reference clock and the feedback clock. To model the behavior of the BBPD, Nicola derived the expression for the linearized gain of the BBPD with Markov chain theory [13]. If the rising edges instants of the reference and the feedback clock are t_r and t_d, the linearized model of the BBPD could be illustrated in Fig. 3-2.

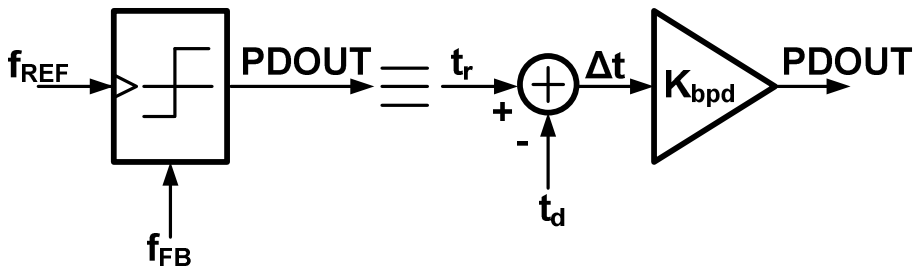


Fig. 3-2 The linearized model of the BBPD

In locked condition, the average value of the output of the BBPD must be zero.

$$E[PDOUT] = 0$$

If the reference clock leads the feedback clocks, $\Delta t>0$, there will be more iterations with PDOUT=1, so that the average value of PDOUT will be positive, vice versa. It could be defined that the gain of the BBPD around the locked condition as rate of change in E[PDOUT] with a small difference δ of the probability density function (pdf) around the locked condition.

$$K_{bpd} \equiv \frac{\partial}{\partial \delta}\left(E\left[PDOUT \mid difference = \delta\right]\right)\Big|_{\delta=0} \qquad (3.7)$$

With the definition in equation 3.7, the gain of the BBPD could be derived as the following expression [13]

$$K_{bpd} = 2 f_{\Delta t}(0) \qquad (3.8)$$

, where $f_{\Delta t}$ means the pdf of the time difference Δt.

Assume α<<β, the nonlinear map in presence of jitter t_{jr} on the reference clock is the same as equation (5) in reference [12], exclude the loop delay D.

$$\Delta t_{k+1} = \Delta t_k + t_{jr} - N\beta K_{DCO(T)} \operatorname{sgn}\left(\Delta t_{k-D}\right) \qquad (3.9)$$

If the values of Δt in case of unjittered reference is Δt^*, Δt^* can assume values on discrete states: $nN\beta KDCO(T)+\Delta t_0^*$, where state number n is integer. From a given state n, Δt^* might go either to state n+1 or state n-1, and the transition probabilities from state n to state n+1 is defined as G_{-n}. If a given cumulative distribution function (cdf) of the jitter t_{jr} is $F_{tjr}(x)=P[t_{jr}<x]$, the transition probability could be expressed as:

$$P\left[\Delta t_{k+1}^* \in n+1 \mid \Delta t_k^* \in n\right] = F_{t_{jr}}\left(-nN\beta K_{DCO(T)}\right) \equiv G_{-n} \qquad (3.10)$$

In section 3.1, the loop delay D is supposed to 2. From equation 3.9 the infinite Markov chain could be simplifies to a seven state chain which is

illustrated in Fig. 3-3, where the transition probability $G_2=G_1=G_0=G_{-1}=G_{-2}=0.5$ and $G_3=1$.

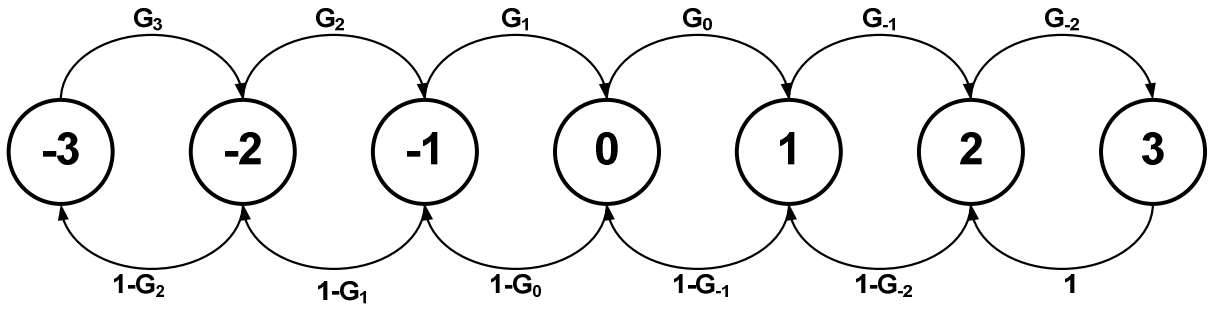


Fig. 3-3 Markov chain approximating

The stationary probability of occupancy of the state n is defined as q_n which could be expressed as:

$$q_n \equiv P\left[\Delta t^* \in n\right]$$

The stationary probability q_n could be derived by the transition probability G_n [13].

$$q_0 = \left[1 + 2\sum_{n=1}^{\infty}\prod_{m=1}^{n}\left(\frac{1-G_{m-1}}{G_m}\right)\right]^{-1} \qquad (3.11)$$

$$q_n = q_{-n} = \prod_{m=1}^{n}\left(\frac{1-G_{m-1}}{G_m}\right)q_0 \qquad (3.12)$$

From equation 3.11 and 3.12, we could find the stationary probability q_n.

$$q_0 = q_1 = q_{-1} = q_2 = q_{-2} = \frac{1}{6} \qquad (3.13)$$

$$q_3 = q_{-3} = \frac{1}{12} \qquad (3.14)$$

If t_{jr} is Gaussian with variance σ_{tjr}^2, then the equation 3.8 could be rewritten as the following:

$$K_{bpd} = 2\sum_{n=-\infty}^{n=\infty} q_n f_{t_{jr}}\left(-nN\beta K_{DCO(T)}\right) \qquad (3.15)$$

$$f_{t_{jr}}\left(-nN\beta K_{DCO(T)}\right) = \frac{1}{\sigma_{t_{jr}}\sqrt{2\pi}} e^{-\frac{1}{2}\left(\frac{nN\beta K_{DCO(T)}}{\sigma_{t_{jr}}}\right)^2} \qquad (3.16)$$

An approximate expression for K_{bpd} might be applied by equation 3.13-3.16 and could be shown as:

$$K_{bpd} = \frac{1}{\sigma_{t_{jr}}\sqrt{2\pi}}\left[\frac{1}{3} + \frac{2}{3}e^{-\frac{1}{2}\left(\frac{N\beta K_{DCO(T)}}{\sigma_{t_{jr}}}\right)^2} + \frac{2}{3}e^{-2\left(\frac{N\beta K_{DCO(T)}}{\sigma_{t_{jr}}}\right)^2} + \frac{1}{3}e^{-4.5\left(\frac{N\beta K_{DCO(T)}}{\sigma_{t_{jr}}}\right)^2}\right] \quad (3.17)$$

From the linear model of BBPD in Fig. 3-2, the unit of the gain K_{bpd} is sec^{-1}. To analyze this model in phase domain, the linear model of BBPD is redraw in Fig. 3-4.

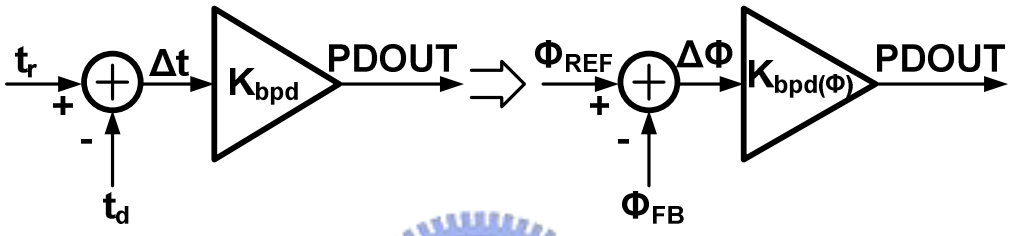


Fig. 3-4 The linear model of BBPD in phase domain

The relationship between K_{bpd} and $K_{bpd(\Phi)}$ could be derived in equation 3.18.

$$K_{bpd(\Phi)} = \frac{K_{bpd}}{2\pi f_{REF}} \quad (3.18)$$

3.2.4 Linear Model of the Loop Filter

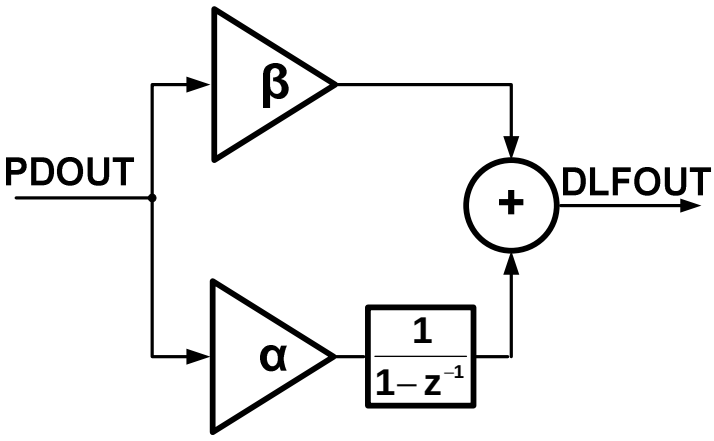


Fig. 3-5 z-domain model of the dynamic loop filter

Fig. 3-5 shows the z-domain model of the dynamic loop filter. The z operator is defined as $z = e^{s/f_R}$, where $s = j2\pi f$ and $1/f_R$ is the period of the sampling rate which is the same as the period of the reference frequency f_{REF} in this design. We can make the following approximation:

$$z^{-1} = e^{-s/f_{REF}} \approx 1 - \frac{s}{f_{REF}} \qquad (3.19)$$

Using equation 3.19, s-domain model of the dynamic loop filter could be illustrated in Fig. 3-6.

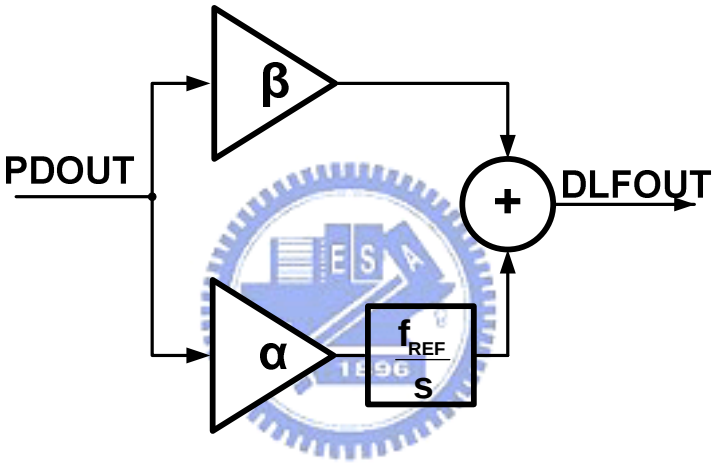


Fig. 3-6 s-domain of the dynamic loop filter

The transfer function of the dynamic loop filter could be written as:

$$F(s) = \frac{DLFOUT(s)}{PDOUT(s)} = \beta + \alpha \frac{f_{REF}}{s} \qquad (3.20)$$

In the concept of the DCO in Fig. 2-6, the DCO includes a ΔΣ modulator and an analog filter. If the transfer function the analog filter is $F_{AF}(s)$, which is a low pass filter, those transfer functions could combine to the dynamic loop filter, and the total transfer function of the loop filter could be written as:

$$F'(s) = F(s) \cdot F_{AF}(s) = \left(\beta + \alpha \frac{f_{REF}}{s} \right) \cdot F_{AF}(s) \qquad (3.21)$$

3.2.5 Linear Model of the Complete PLL Loop

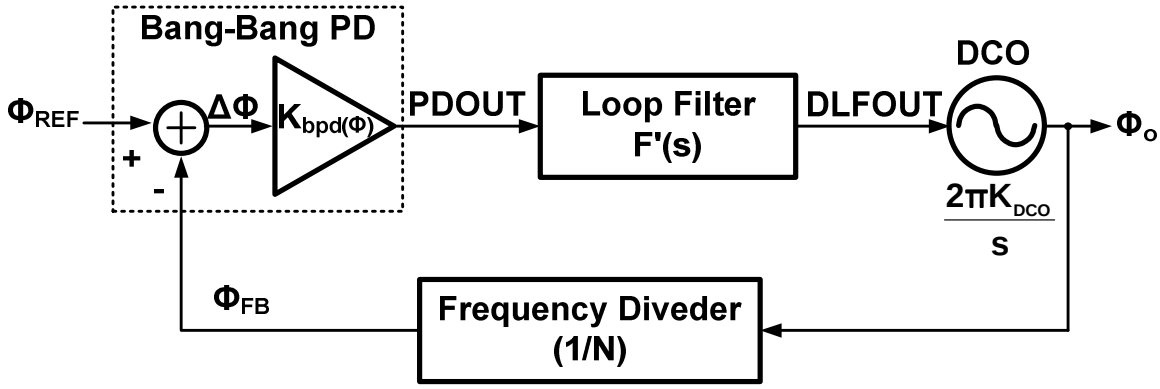


Fig. 3-7 The linear model of the PLL loop

The linear model of the PLL loop is illustrated in Fig. 3-7, where $K_{bpd(\Phi)}$ and F'(s) are applied by equation 3.18 and 3.21.

3.3 Generated Phase Noise

3.3.1 Noise Model of the DCO

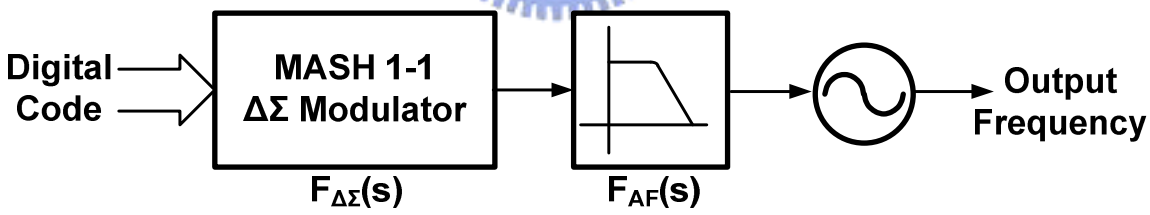


Fig. 3-8 The concept of the DCO

The concept of the DCO is shown in Fig. 3-8. A ΔΣ modulator is used to control the high gain oscillator, but the ΔΣ modulator might induce a quantization noise. An analog filter is added to cancel the noise caused by the ΔΣ modulator.

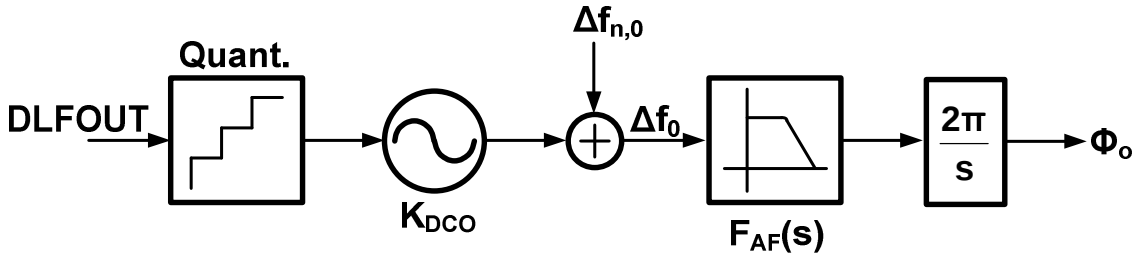


Fig. 3-9 The noise model of the DCO architecture, excluding the DCO noise

The noise model of the DCO architecture is shown in Fig. 3-9, excluding the DCO noise. Since the input code spans multiple quantization levels, the DCO frequency quantization error is modeled in Fig. 3-9 as an additive uniformly-distributed random variable $\Delta f_{n,0}$ with white noise spectral characteristics. Another noise source is the nature noise caused by the DCO. The DCO noise spectrum affected by the ΔΣ modulator could be expressed as following.

$$S_{\Phi_{n,DSM}} = \left| F_{AF}(s) \cdot \frac{2\pi}{s} \right|^2 S_{\Delta f_{n,0}} \qquad (3.22)$$

The noise spectrum of the random variable $\Delta f_{n,0}$ includes the quantization noise from finite frequency range and the dithering noise from noise-shaping by the ΔΣ modulator and could be written as:

$$S_{\Delta f_{n,0}} = S_{\Delta f_{n,quantize}} + S_{\Delta f_{n,dithering}}$$

Staszewski who proposed a digital controlled oscillator has provided the analytic method to design the DCO [11], but an analog filter is added in the architecture of the DCO in this thesis.

The variance of the adjust frequency $\Delta f_{0,quantize}$ is

$$\sigma^2_{\Delta f_{0,quantize}} = \frac{(\Delta f_{res})^2}{12} \qquad (3.23)$$

$$\Delta f_{res} = \frac{\Delta f_T}{2^m} \qquad (3.24)$$

, where Δf_{res} is the frequency resolution, m is the width of the ΔΣ modulator, and Δf_T is the frequency tuning range of the DCO. The single-sided spectral density of the quantization noise $\Delta f_{n,quantize}$ is

$$S_{\Delta f_{n,quantize}}(\Delta f) = \frac{\sigma^2_{\Delta f_{0,quantize}}}{f_{REF}} \qquad (3.25)$$

From equation 3.23~3.25, the single-sided power spectrum density (PSD) to the output could be derived as equation 3.26 which multiplied by the sinc function corresponding the operation of the register (sample and hold).

$$\begin{aligned} S_{\Delta\Phi_{o,quantize}}(\Delta f) &= \left| F_{AF}(j2\pi\Delta f) \cdot \frac{2\pi}{j2\pi\Delta f} \right|^2 \cdot S_{\Delta f_{n,quantize}} \\ &= \frac{1}{12} \cdot \left(\frac{\Delta f_{res}}{\Delta f} \right)^2 \cdot \frac{1}{f_{REF}} \cdot \left(\operatorname{sinc} \frac{\Delta f}{f_{REF}} \right)^2 \cdot \left| F_{AF}(j2\pi\Delta f) \right|^2 \end{aligned} \qquad (3.26)$$

The frequency step of the switching of the ΔΣ modulator is the frequency tuning range Δf_T, so the variance of the dithering frequency is

$$\sigma^2_{\Delta f_{0,dithering}} = \frac{(\Delta f_T)^2}{12} \qquad (3.27)$$

The spectrum of the ΔΣ-shaped frequency deviation could be written as

$$S_{\Delta f_{n,dithering}}(\Delta f) = \frac{(\Delta f_T)^2}{12} \cdot \frac{1}{f_{OS}} \cdot \left(2\sin \frac{\Delta f}{f_{OS}} \right)^{2n} \qquad (3.28)$$

, where f_{os} and n mean the oversampling rate and the number of stages of the ΔΣ modulator. The output noise PSD due to the ΔΣ modulator could be written as

$$S_{\Delta\Phi_{o,dithering}}(\Delta f)=\left|F_{AF}(j2\pi\Delta f)\cdot\frac{2\pi}{j2\pi\Delta f}\right|^2\cdot S_{\Delta f_{n,dithering}}$$
$$=\frac{1}{12}\cdot\left(\frac{\Delta f_T}{\Delta f}\right)^2\cdot\frac{1}{f_{OS}}\cdot\left(2\sin\frac{\pi\Delta f}{f_{OS}}\right)^{2n}\cdot\left|F_{AF}(j2\pi\Delta f)\right|^2 \quad (3.29)$$

In 1999, few researchers presented the phase noise of the differential MOS ring oscillator [14]. The total power of the ring oscillator could be derived in the equation 3.30, where N, I_{tail}, and VDD mean the number of stages of the oscillator, the tail current in each stage, and the supply voltage.

$$P=NI_{tail}V_{DD} \quad (3.30)$$

The frequency of the oscillation would be approximated as

$$f_o\approx\frac{I_{tail}}{2\eta N(C_{node}V_{\max})}$$

, where η is the propagation constant, C_{node} is the capacitance of the output node, and V_{max} is the maximum voltage swing of the output. The output noise of the ring oscillator could be derived in equation 3.31, where $k=1.38\times10^{-23}$ J/K is the Boltzmann constant, T is the temperature in Kelvin degree, V_{char} is the characteristic voltage of the device, and R_L is the load resistor.

$$S_{\Phi_{n,DCO}}(\Delta f)=\frac{8}{3\eta}\cdot N\cdot\frac{kT}{P}\cdot\left(\frac{VDD}{V_{char}}+\frac{VDD}{R_LI_{tail}}\right)\cdot\left(\frac{f_o}{\Delta f}\right)^2 \quad (3.31)$$

$$V_{char}=\frac{V_{GS}-V_T}{\gamma}$$

From our specification in Table 1-1, the power consumption of the whole system is less then 1mW, so that the DCO has to operate under 400mA for 1V power supply. To reduce the power consumption of the DCO, the ring oscillator would be designed in three stages. If the power consumption of the ring oscillator is

about 100μW, the tail current of each stage has to be about 30μW. The phase noise caused by the ring oscillator circuits is pictured in Fig. 3-10.

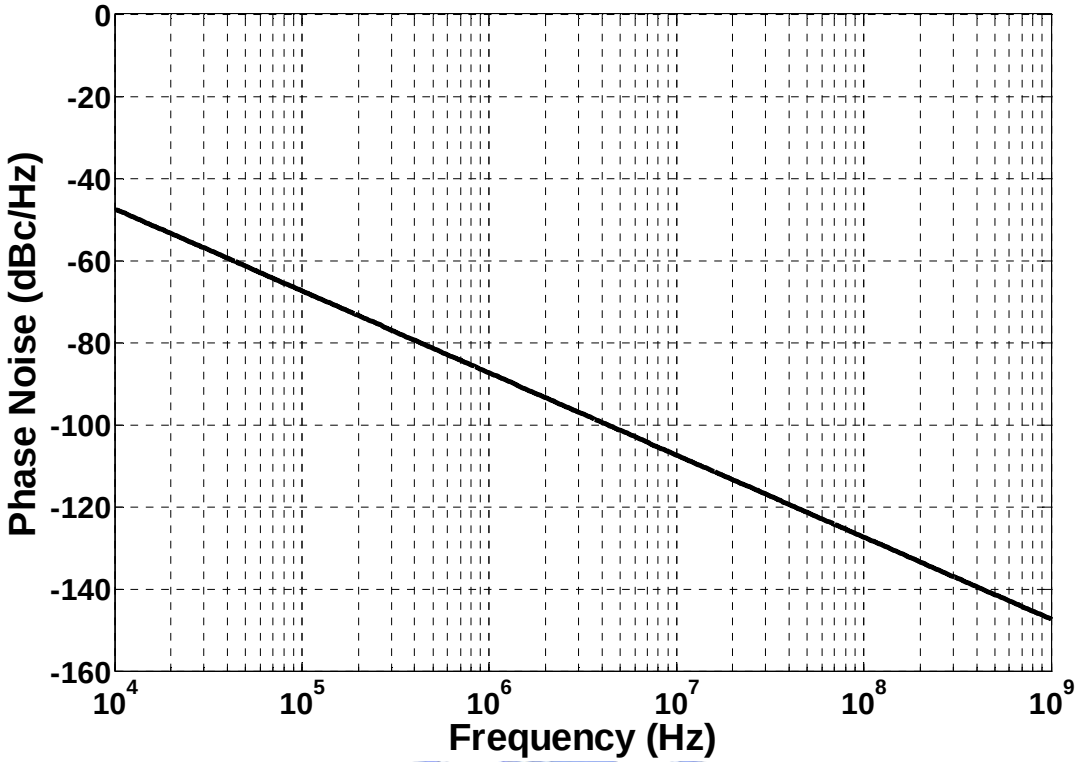


Fig. 3-10 Nature noise spectrum of the oscillator

The total DCO noise spectrum density which is formulated in equation 3.22 could be rewritten in the following equation, where $S_{\Delta\Phi nSDM}$ and $S_{\Delta\Phi o,quantize}$ are shown in equation 3.22.

$$S_{\Phi_{n,DCO\_Total}} = S_{\Phi_{n,DCO}} + S_{\Phi_{n,DSM}} \qquad (3.32)$$

To reduce the affect of the quantization and dithering noise to the output, the width of the ΔΣ modulator and the bandwidth of the analog filter should be designed by equation 3.29 and 3.26 properly, and we let the output noise caused by those two factors less than the nature noise of the oscillator and the specification. A 2nd order ΔΣ modulator is chose in this research. The signal transfer function of the MASH (Multi-stage noise shaping) 1-1 ΔΣ modulator is formulated in equation 3.33.

$$H_{\Delta\Sigma}(z)=\left(\frac{z^{-1}}{1-z^{-1}}\right)^2 \qquad (3.33)$$

Use the approximation in equation 3.19, the formula could be rewritten as

$$H_{\Delta\Sigma}(s)=\left(\frac{f_{OS}}{s}-1\right)^2 \qquad (3.34)$$

, where f_{OS} is the over sampling rate of the ΔΣ modulator.

If the tuning range of the oscillator is 30%, the frequency range of the oscillator is designed as 400MHz. From equation 3.26, the quantization noise to output could be lower with hither resolution of the ΔΣ modulator. Fig. 3-11 shows the expected phase noise spectrum caused by the quantization noise with difference width m of the ΔΣ modulator, neglected the effect of the analog filter. The width of the ΔΣ modulator has to more than 15 bits to make the phase noise less than -100dBc/Hz at 1MHz offset.

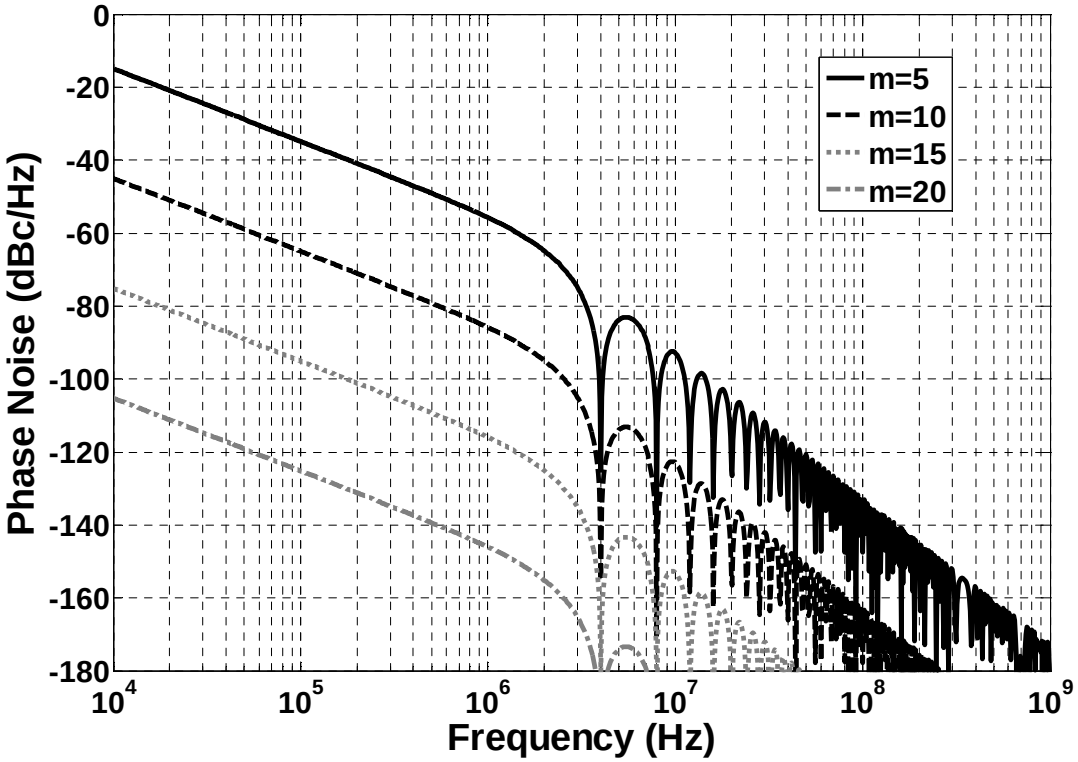


Fig. 3-11 Quantization noise with different width m of the ΔΣ modulator, excluded analog filter

In the specification in Table 1-1, the resolution has to be lower than 20ppm, so that the frequency step has to be less than 28 kHz for each modified signal provided by the BBPD.

$$(\alpha+\beta)\cdot K_{DCO}=9\cdot\frac{400MHz}{2^m}<28kHz$$

$$m>16.97$$

The width of the ΔΣ modulator has to more than 17 bits. We choose 19bits as the resolution of the ΔΣ modulator.

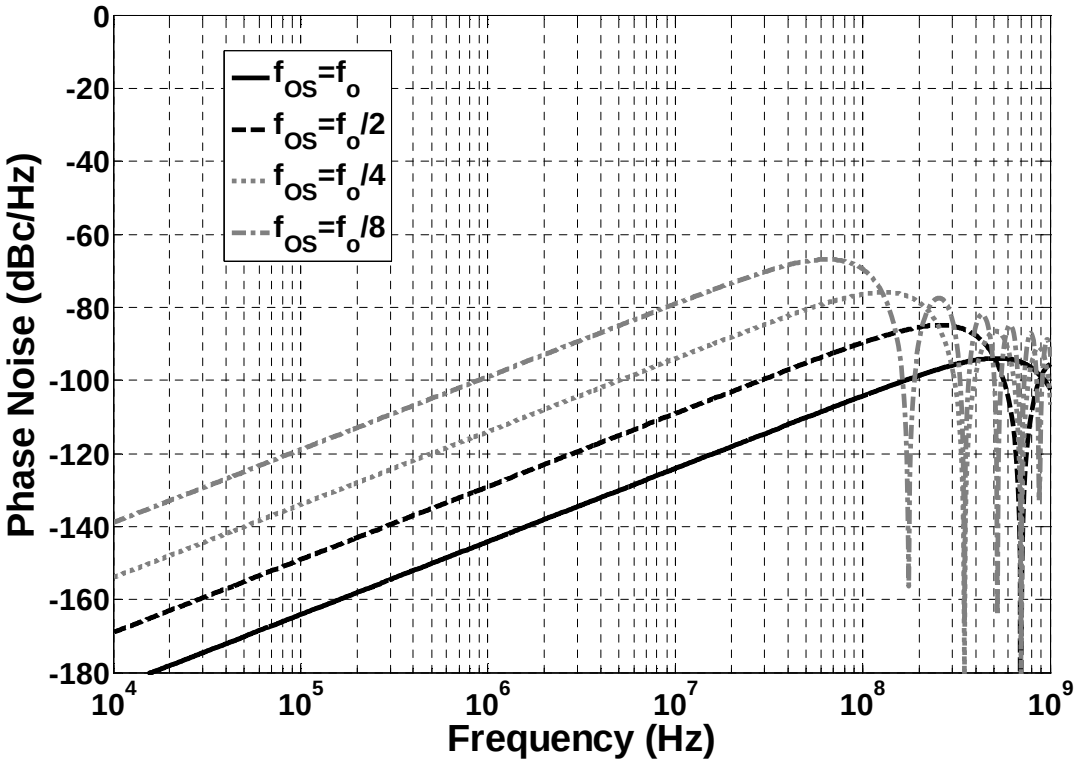


Fig. 3-12 Dithering noise with different oversampling rate f_{OS} of the ΔΣ modulator, excluded analog filter

From equation 3.29, the dithering noise to output could be less with hither oversampling rate f_{OS} of the ΔΣ modulator. The expected phase noise spectrum caused by the dithering noise with difference oversampling rate of the ΔΣ modulator neglected the effect of the analog filter is illustrated in Fig. 3-12, where f_o is the oscillation frequency. The oversampling rate of the ΔΣ modulator has to higher than eighth of the oscillation frequency to make the phase noise

less than -100dBc/Hz at 1MHz offset, so that we choose a quarter of the oscillation frequency as the oversampling rate.

If the resolution of the ΔΣ modulator is 19 bits and the oversampling rate of the ΔΣ modulator is one quarter of the oscillation frequency, and neglect the analog filter, the output phase noise due to the ΔΣ modulator is figured in Fig. 3-13.

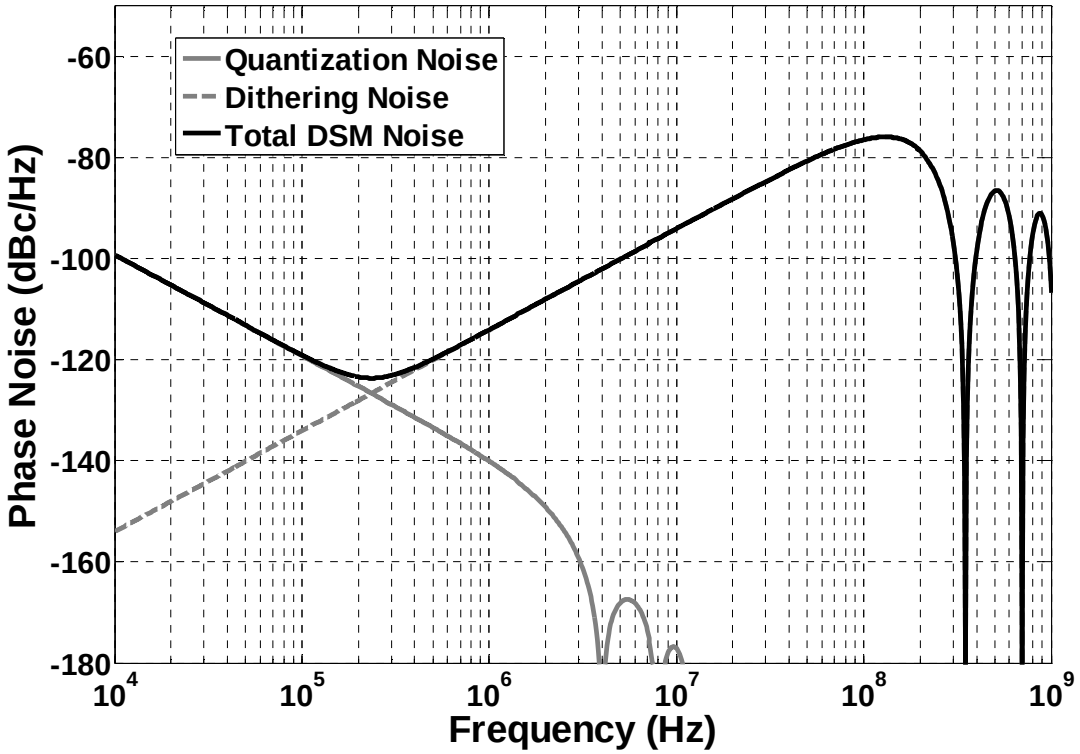


Fig. 3-13 The output phase noise due to the ΔΣ modulator

From Fig. 3-13, we could observe that the output phase noise due to the ΔΣ modulator would get higher after 300 kHz frequency offset. A 3rd order analog filter is used to reduce the noise of the 2nd order ΔΣ modulator, and the bandwidth of the analog filter has been chosen as 500 kHz. The output phase noise due to the ΔΣ modulator after the analog filter is shown in Fig. 3-14.

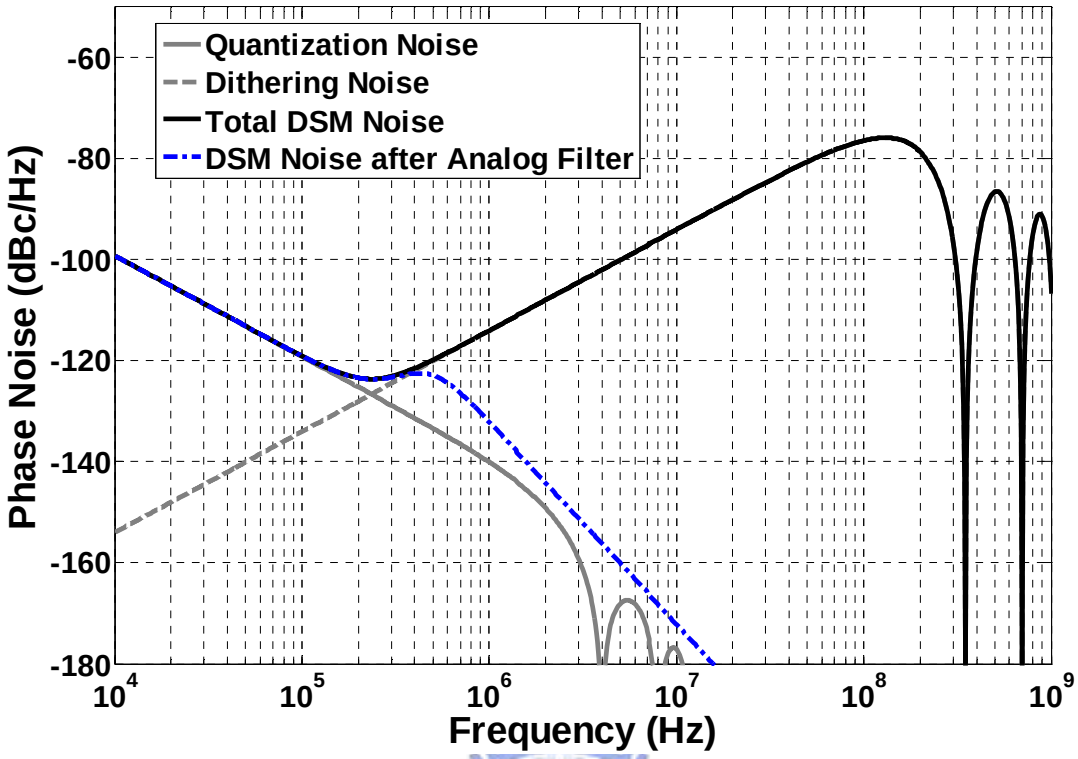


Fig. 3-14 The output phase noise due to the ΔΣ modulator after analog filter

The output phase noise spectrum of the DCO is illustrated in Fig. 3-15.

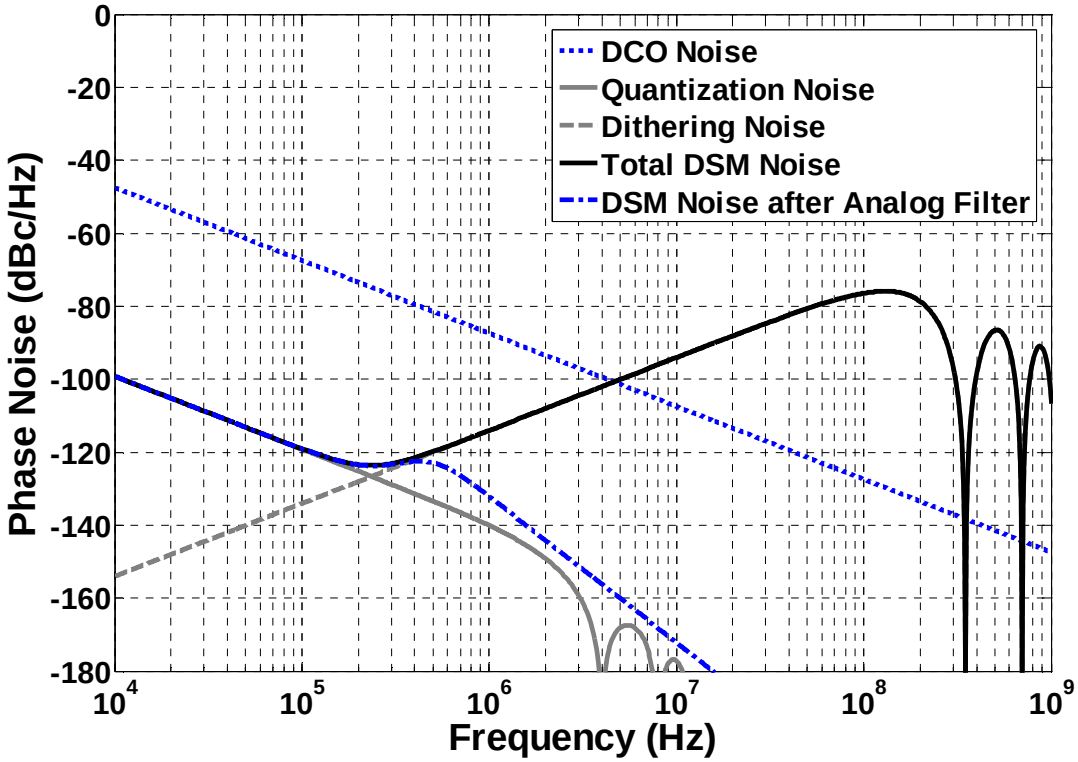


Fig. 3-15 The output phase noise spectrum of the DCO

3.3.2 Noise Model of the BBPD

The concept of the BBPD is shown in Fig. 3-2. The BBPD quantizes the phase difference of the reference frequency f_{REF} to ±1, and the average of the PDOUT is 0. The variance of the PDOUT is

$$\sigma^2_{\Delta PDOUT} = \frac{(\Delta PDOUT)^2}{12} = \frac{1}{3}$$

The single-sided spectral density of the quantization noise of the BBPD with zero-order hold could be derived as

$$S_{\Phi_{n,PD}}(\Delta f) = \frac{\sigma^2_{\Delta PDOUT}}{f_{REF}} \cdot \left(\text{sinc} \frac{\Delta f}{f_{REF}} \right)^2 = \frac{1}{3} \cdot \frac{1}{f_{REF}} \cdot \left(\text{sinc} \frac{\Delta f}{f_{REF}} \right)^2 \quad (3.35)$$

The spectrum of the BBPD quantization noise is shown in Fig. 3-16.

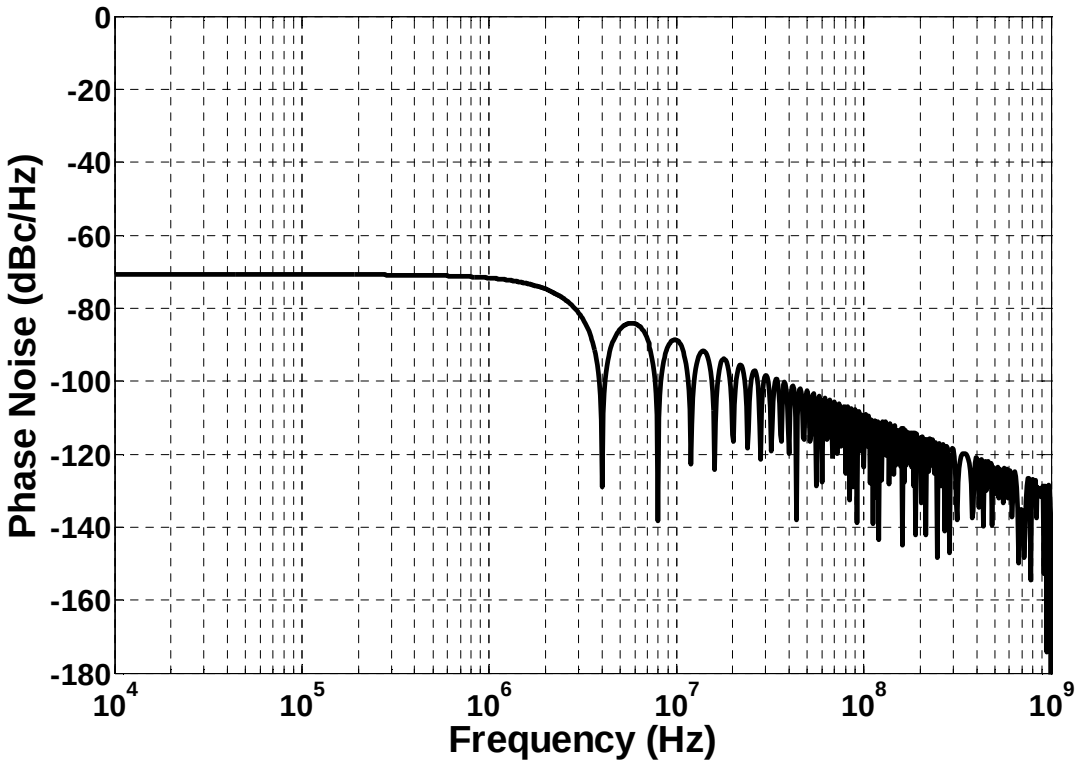


Fig. 3-16 The spectrum of the BBPD quantization noise

3.3.3 Output Phase Noise Power Spectral Density

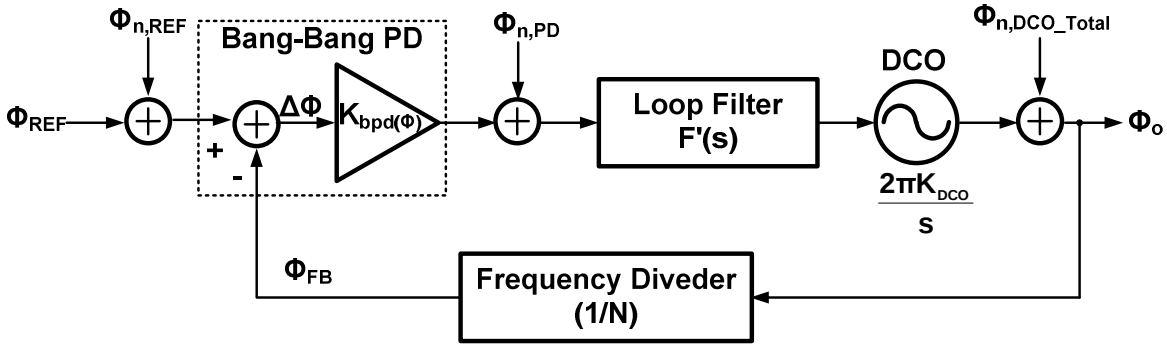


Fig. 3-17 The linear model of the ADPLL with noise sources

The linear model of the ADPLL with noise sources can be shown as Fig. 3-17, in which each major block is replaced with its linear model, where $K_{bpd(\Phi)}$ and F'(s) is given by equation 3.18 and . In this model, $\Phi_{n,REF}$ is the noise which is induced by signal generator, $\Phi_{n,PD}$ is the quantization noise which is caused by BBPD, and $\Phi_{n,DCO}$ is the noise of the DCO. The transfer function from the input of the BBPD to the output of PLL is:

$$\frac{\Phi_{n,o}}{\Phi_{n,REF}} = H(s) = \frac{K_{bpd(\Phi)}F'(s)(2\pi K_{DCO})}{s + K_{bpd(\Phi)}F'(s)(2\pi K_{DCO})/N} \qquad (3.36)$$

The transfer function from the output of the BBPD to the output of PLL is:

$$\frac{\Phi_{n,o}}{\Phi_{n,PD}} = \frac{F'(s)(2\pi K_{DCO})}{s + K_{bpd(\Phi)}F'(s)(2\pi K_{DCO})/N} = \frac{H(s)}{K_{bpd(\Phi)}} \qquad (3.37)$$

The transfer function from the output of the DCO to the output of PLL is:

$$\frac{\Phi_{n,o}}{\Phi_{n,DCO\_Total}} = \frac{s}{s + K_{bpd(\Phi)}F'(s)(2\pi K_{DCO})/N} = 1 - \frac{H(s)}{N} \qquad (3.38)$$

If the noise spectrum of the signal generator, the BBPD and the DCO are $S_{\Phi n,REF}$, $S_{\Phi n,PD}$, and $S_{\Phi n,DCO}$, the output phase noise spectrum of the system could be derived as:

$$S_{\Phi_{n,o}} = |H(s)|^2 S_{\Phi_{n,REF}} + \left|\frac{H(s)}{K_{bpd(\Phi)}}\right|^2 S_{\Phi_{n,PD}} + \left|1 - \frac{H(s)}{N}\right|^2 S_{\Phi_{n,DCO\_Total}} \quad (3.39)$$

The Bode plot of the open loop transfer function of the ADPLL is figured in Fig. 3-18. The unit-gain bandwidth of this system is about 246.26 kHz, and the phase margin of this loop is 38.22°.

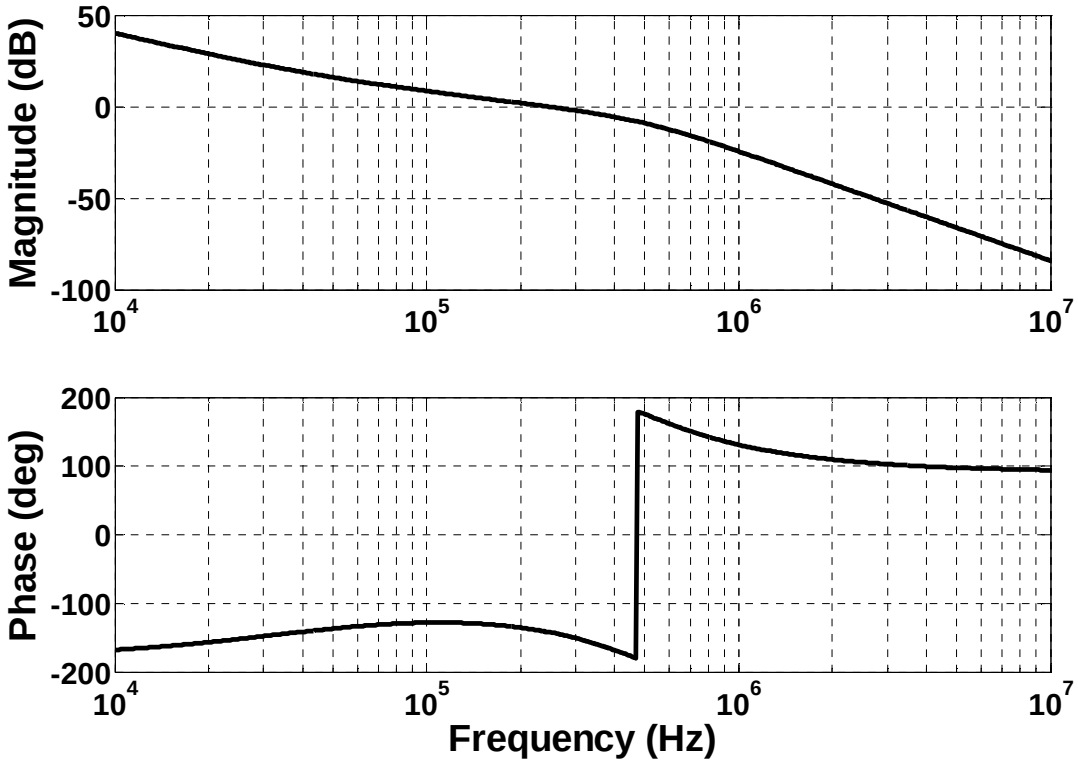


Fig. 3-18 The Bode plot of the open loop transfer function of the ADPLL

The total output phase noise spectrum is illustrated in Fig. 3-19.

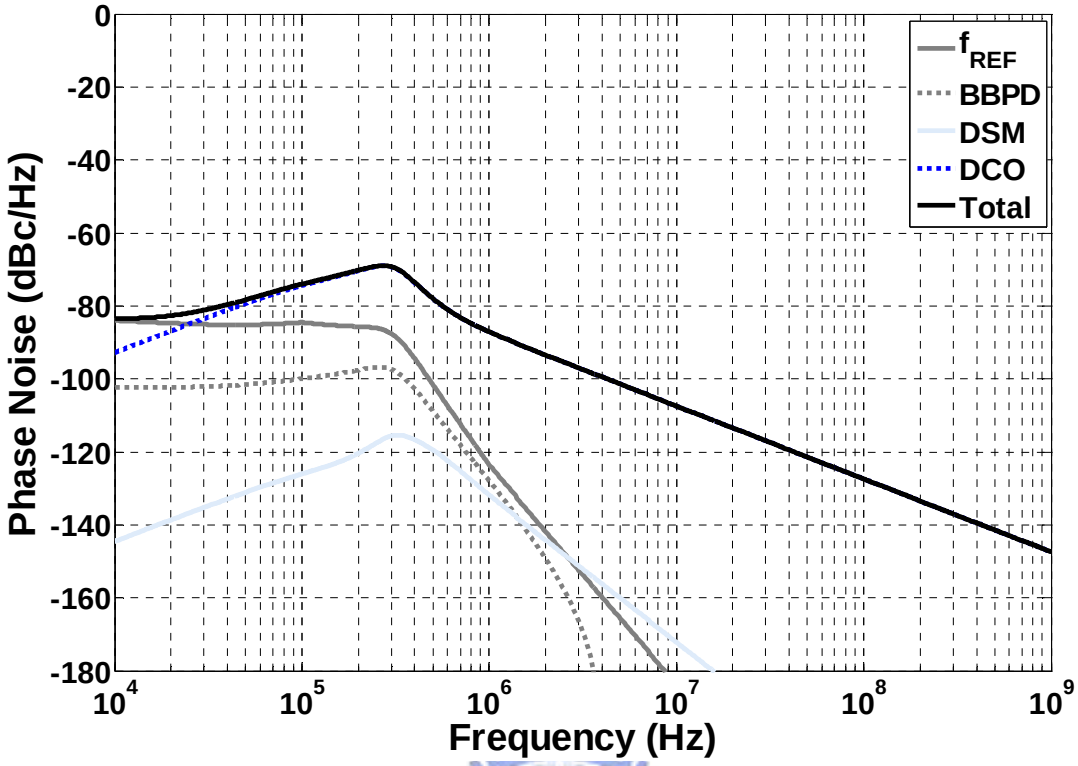


Fig. 3-19 The total output phase noise spectrum

Chapter 4 Design and Implementation

4.1 Phase Detector (PD)

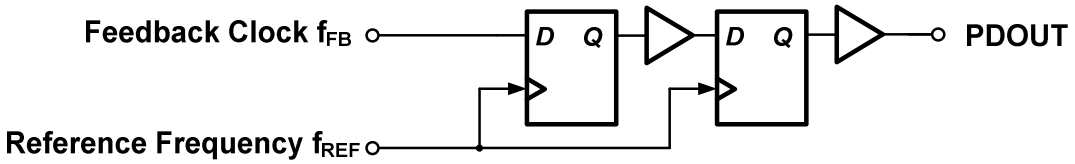


Fig. 4-1 The structure of the phase detector (PD)

The structure of the phase detector (PD) is illustrated in Fig. 4-1. Two D flip-flops string together to avoid meta-stability problem. To get higher resolution for small phase error, the first D flip-flop uses a sense amplifier cascaded a SR latch to increase the sensitivity [15]. The second D flip-flop would resample the output of the first D flip-flop. The architecture of the first D flip-flop is shown in Fig. 4-2.

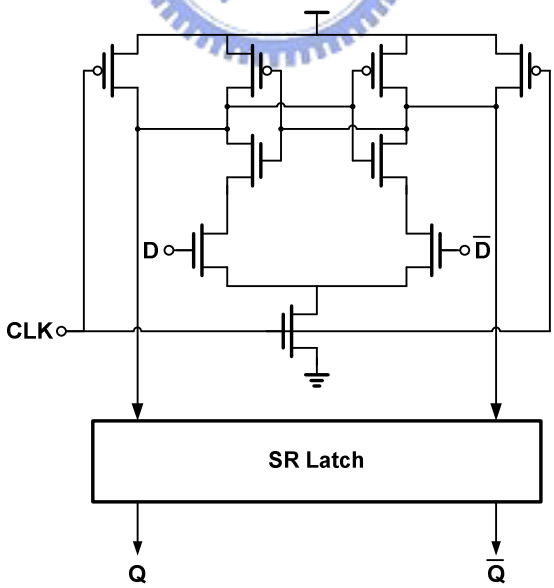


Fig. 4-2 The architecture of the first D flip-flop

The hysteresis diagram of the PD with different corner is illustrated in Fig. 4-3, where t_{REF} and t_{FB} is the rising edge of the reference and the feedback signal. The dead zone of the PD is lower than 3 ps.

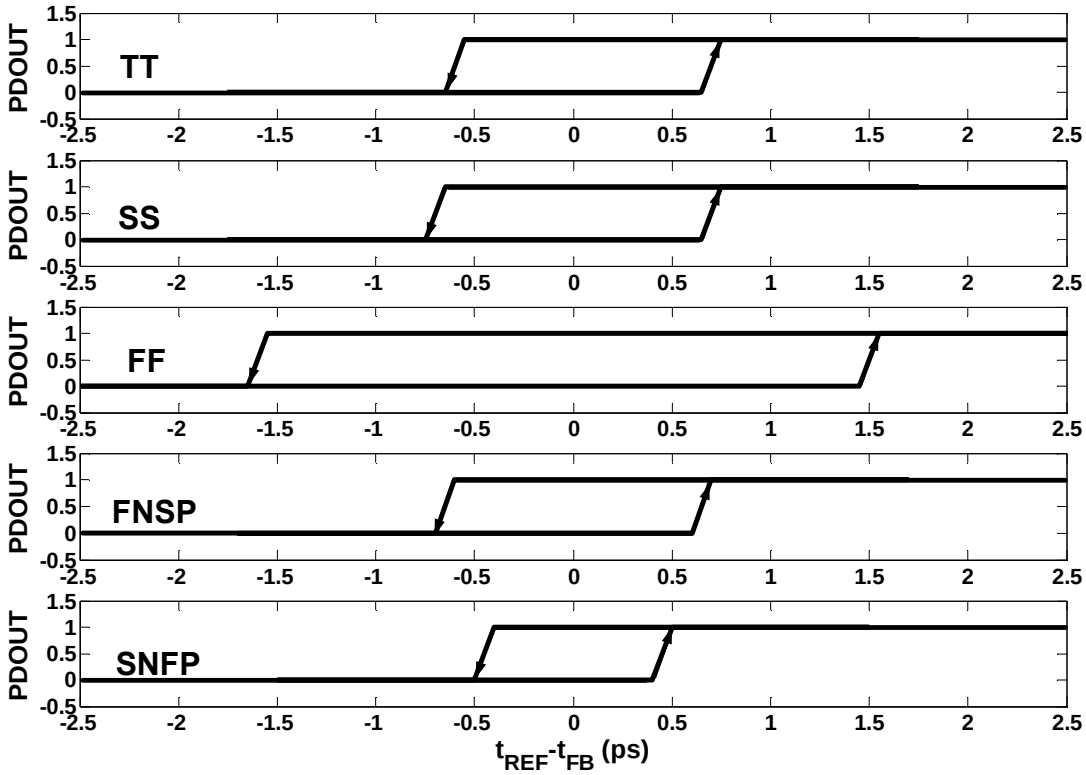


Fig. 4-3 The hysteresis diagram of the PD with different corner

4.2 Dynamic Loop Filter (DLF)

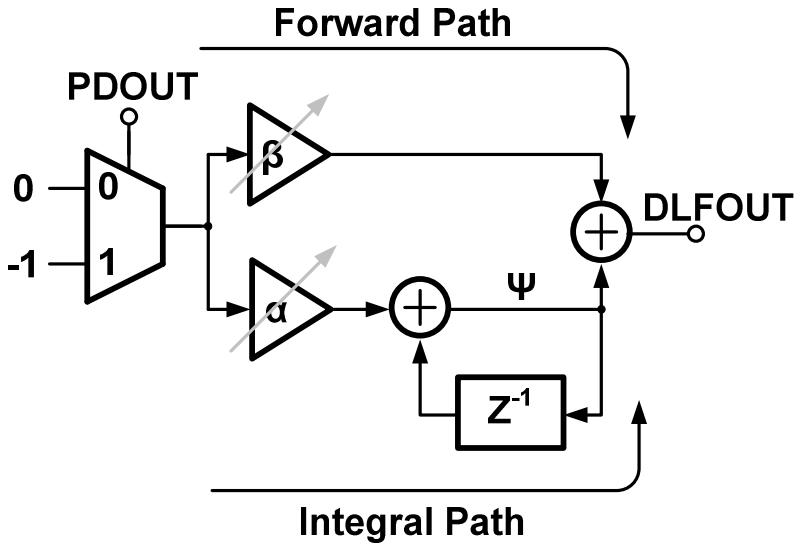


Fig. 4-4 The structure of the dynamic loop filter

The structure of the dynamic loop filter (DLF) is shown in Fig. 4-4 [12]. The DLF is composed by a forward path and an integral path, and the parameters, α and β, would affect the settling time and the frequency jitter of the ADPLL output which might influent the phase noise performance. If α and β are large, we could speed up the settling time, but the output frequency jitter would be high because the digital control code might change with large steps, vice versa. To overcome this problem, a dynamic gain control (DGC) is used to alter those parameters dynamically. The DGC would give a few sets of large parameters to speed up the settling time and after stable it would replace those parameters with smaller ones to keep better jitter and phase noise performance. The concept of the operation of the DGC would be described as following.

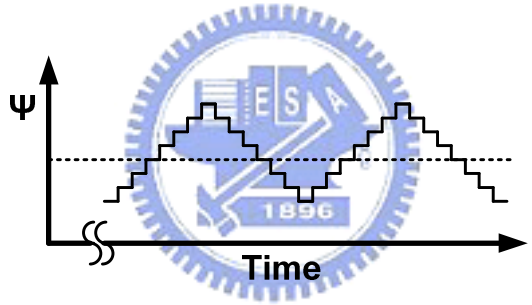


Fig. 4-5 The waveform of the output of the integral path Ψ when stable

The output of the integral path Ψ after stable would vibrate up and down with an average value because of the property of the BBPD, and the waveform of the output of the integral path Ψ is shown in Fig. 4-5. With this phenomenon, we could check if the loop is stable, and decide when we change the parameters of the DLF. The process of the DGC is figured in Fig. 4-6.

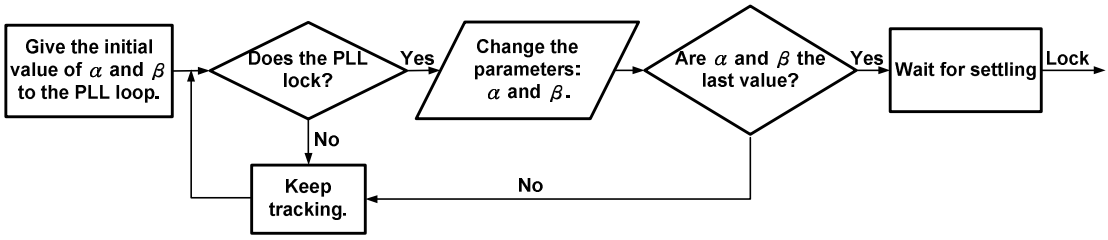


Fig. 4-6 The process of the DGC

4.3 Calibration Digital Controlled Oscillator (CDCO)

4.3.1 Digital Controlled Oscillator (DCO)

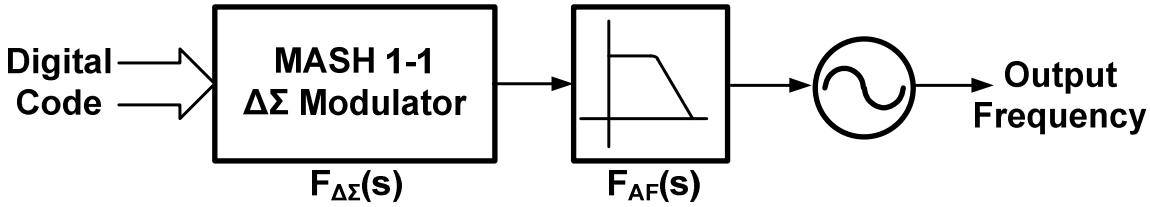


Fig. 4-7 The concept of the low power digital controlled oscillator

The concept of the low power digital controlled oscillator (DCO) is redrawn in Fig. 4-7. The width of the ΔΣ modulator is 19 bits and the bandwidth of the 3rd order analog filter is 500 kHz by the analysis in session 3.3.1. To implement such a low power DCO, we combine the ΔΣ modulator and the analog filter as a current digital to analog converter (IDAC) to provide a fine current to control a ring oscillator. The architecture of the DCO is figured in Fig. 4-8.

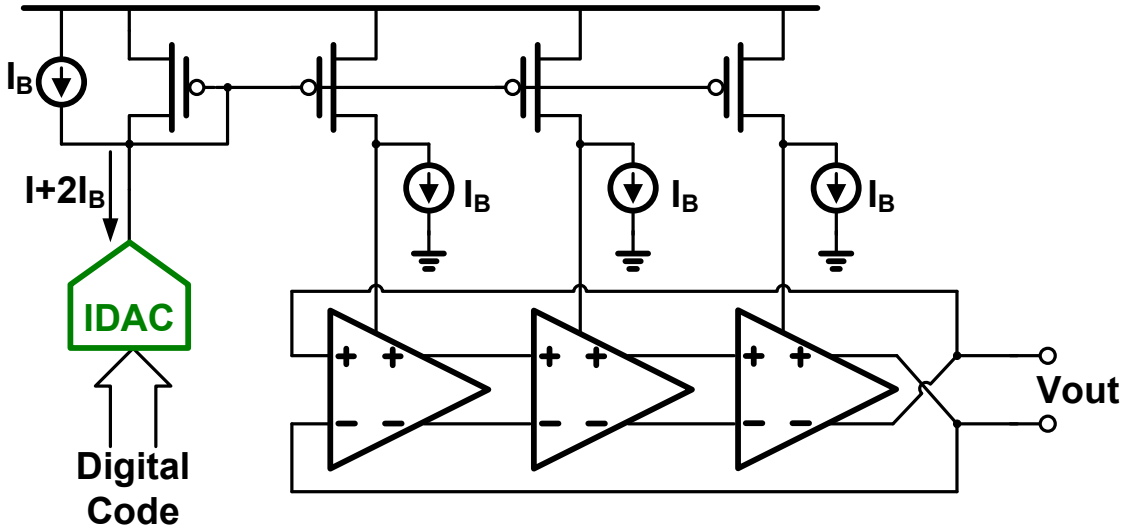


Fig. 4-8 The architecture of the DCO

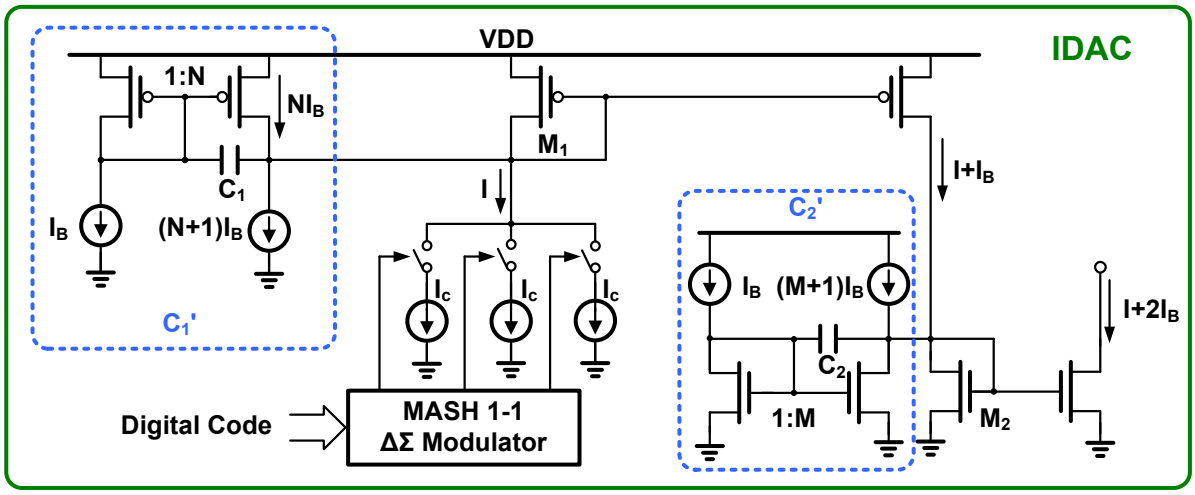


Fig. 4-9 The architecture of the IDAC

The architecture of the IDAC is shown in Fig. 4-9. In this thesis, we need a 3rd order analog filter with 500 kHz bandwidth by the previous analysis in session 3.3.1. However, the parasitic capacitor which is provided by the current mirror near the ring oscillator gives a high frequency pole. We implement a 2nd order analog filter with 500 kHz, and the transfer function of the filter is expressed as equation 4.1, where ω_{p1} andω_{p2} are two poles of this filter.

$$H_{AF}(s)=\frac{\omega_{p1}\omega_{p2}}{s^2+(\omega_{p1}+\omega_{p2})s+\omega_{p1}\omega_{p2}} \qquad (4.1)$$

If we let ω_{p1} and ω_{p2} the same as ω_p, the equation could be rewritten as following.

$$H_{AF}(s)=\frac{\omega_p^2}{s^2+\omega_p s+\omega_p^2}$$

The -3dB bandwidth of the analog filter could be expressed as equation 4.2.

$$\omega_{-3dB}^2=(\sqrt{2}-1)\omega_p^2 \qquad (4.2)$$

Those two poles of the analog filter ω_p are 800 kHz. The parameters of the analog filter are shown in Table 4-1.

Table 4-1 The parameters of the analog filter

Parameter	**g_{M1}**	**g_{M2}**
Value	120.63 μA/V	195.28 μA/V
Parameter	**C_1'**	**C_2'**
Value	24pF	38.85pF
Parameter	**Δg_{M1}**	**Δg_{M2}**
Value	12.5%	6.65%

In this analog filter, two capacitors are used to provide two poles for -3dB bandwidth with 500 kHz. To minimize the area of the capacitor, an impedance scalar is used in this structure [16]. The concept of the impedance scalar is shown in Fig. 4-10. The equivalent input current from node X is N+1 times of the current bias I_{in}, so the equivalent capacitor is N+1 times of the capacitor C_1.

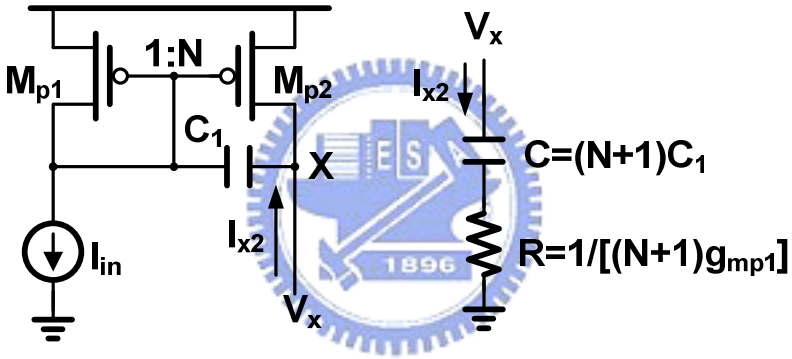


Fig. 4-10 The concept of the impedance scalar

The ΔΣ modulator is built as a second-order MASH 1-1 structure and the architecture is shown in Fig. 4-11 [11], where DSM_CLK is the oversampling frequency clock of the ΔΣ modulator, which is a quarter of the output clock frequency, and K is the calibration signal which would be expressed in session 4.3.2. The output of the ΔΣ modulator is used to control three switches in Fig. 4-9 to get the finest current tuning.

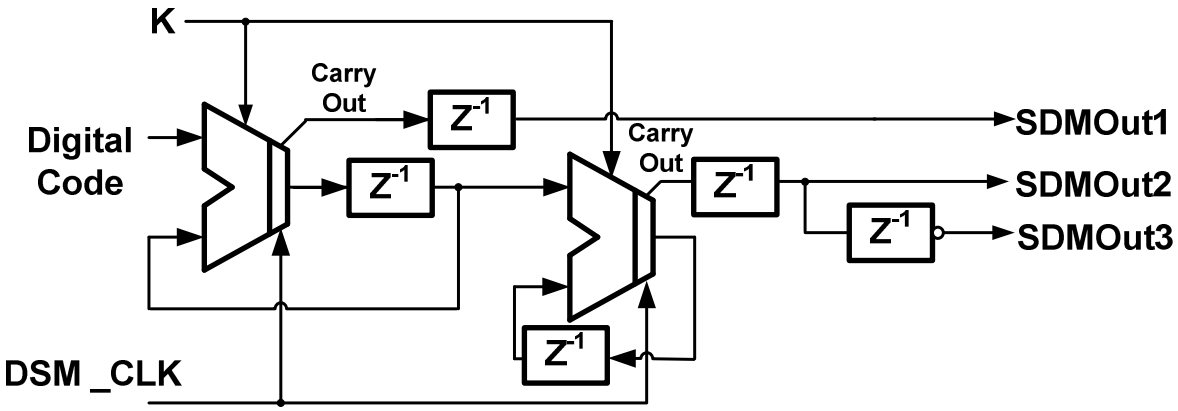


Fig. 4-11 The architecture of the ΔΣ modulator

Fig. 4-12 and Fig. 4-13 are the post simulation of the tuning curve of the DCO and the transient response of the DCO with 1.4GHz RF output. The output frequency is monotonically increasing with digital codes. The power consumption of the DCO with 1.4GHz RF output is about 250μW, and the output swing is about 400mV$_{pp}$.

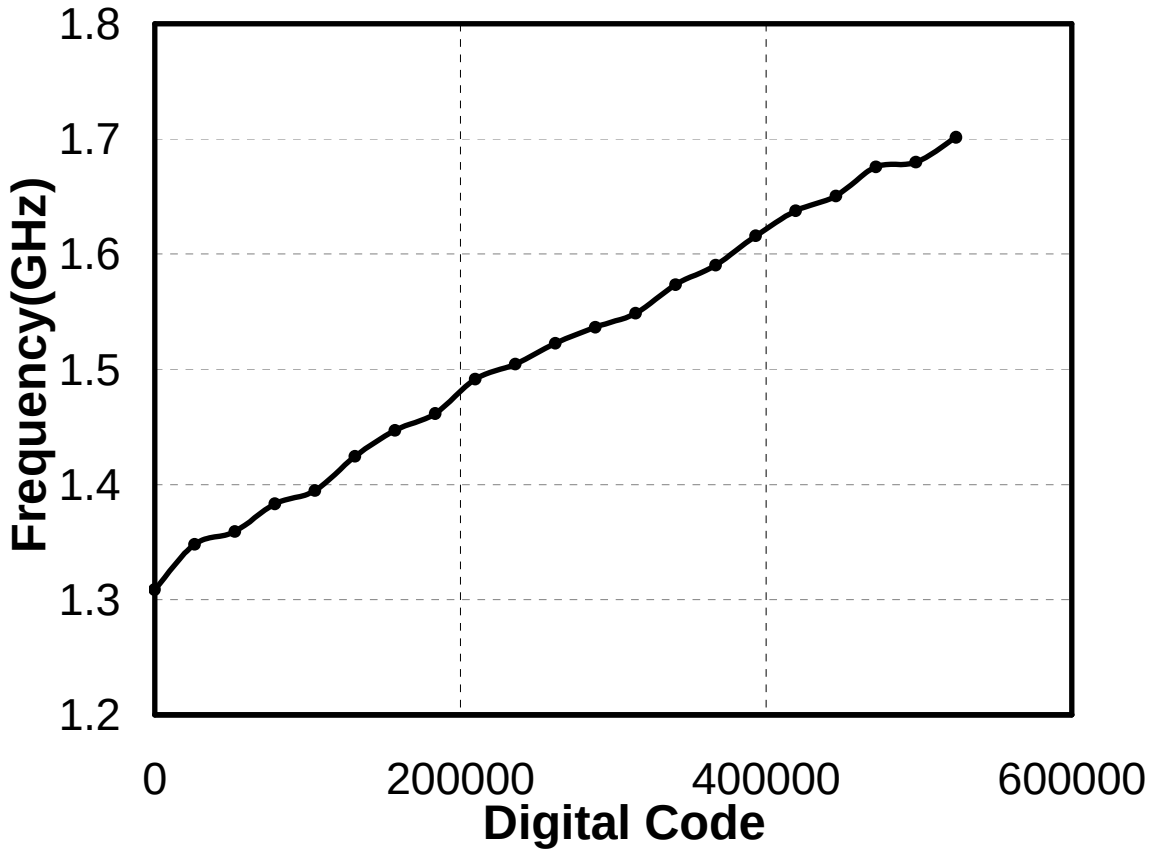


Fig. 4-12 The tuning curve of the DCO

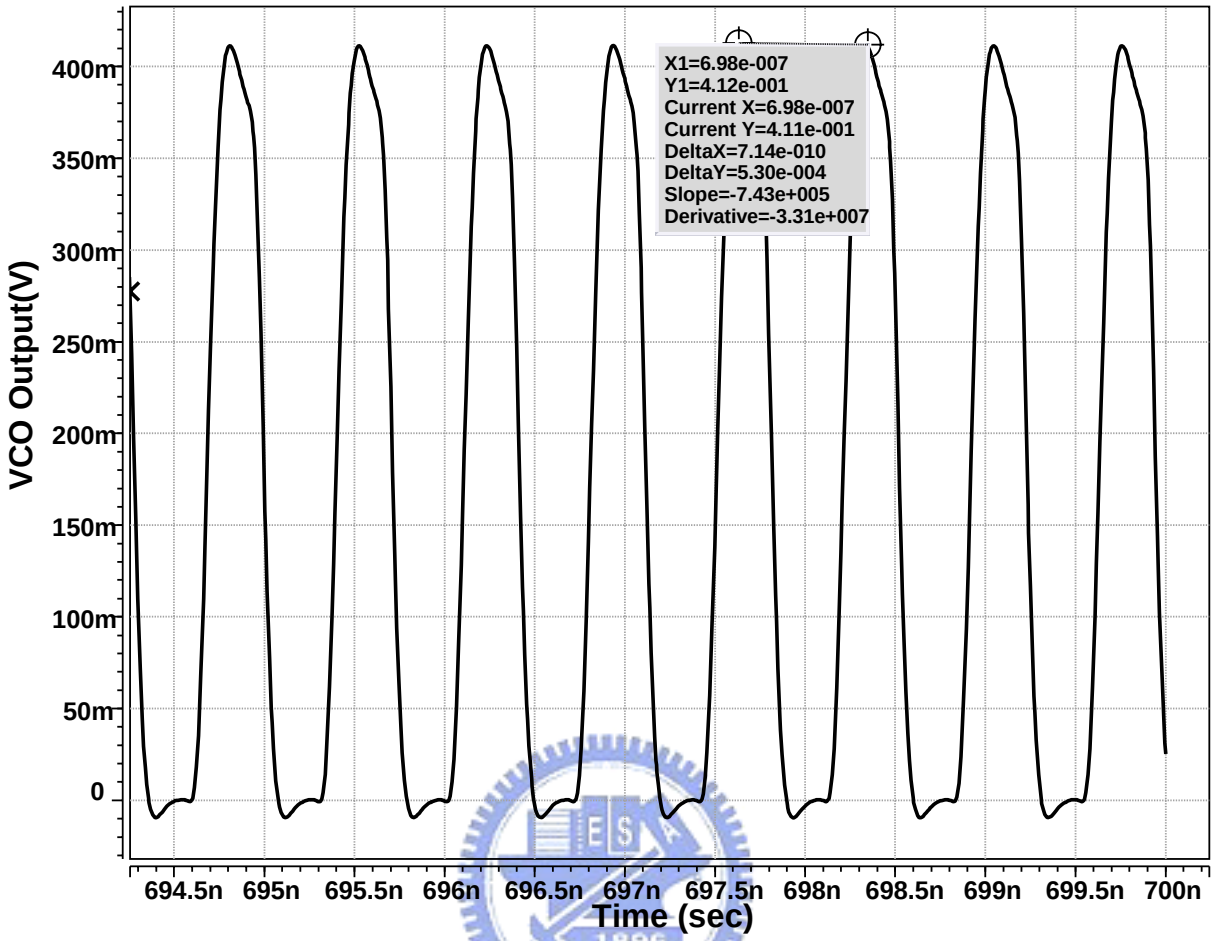


Fig. 4-13 The transient response of the DCO with 1.4GHz RF output

The frequency range of the DCO with different corner is shown in Table 4-2, and the output frequency of the DCO could cover 1.4GHz in each corner.

Table 4-2 The frequency range of the DCO with different corner

Corner	Frequency Range (GHz)
TT	1.2965~1.6903
SS	1.2555~1.6624
FF	1.2542~1.6432
SNFP	1.2835~1.7086
FNSP	1.2828~1.6453

4.3.2 DCO Calibration Circuit (DCC)

The DCO is the most sensitive element in the PLL. The properties of the DCO would drift because of the effect of the PVT variation, and that would affect the

stability and phase noise performance of the whole loop. To overcome this problem, a DCO calibration circuit (DCC) is used to modify the properties of the DCO to the original designed ones.

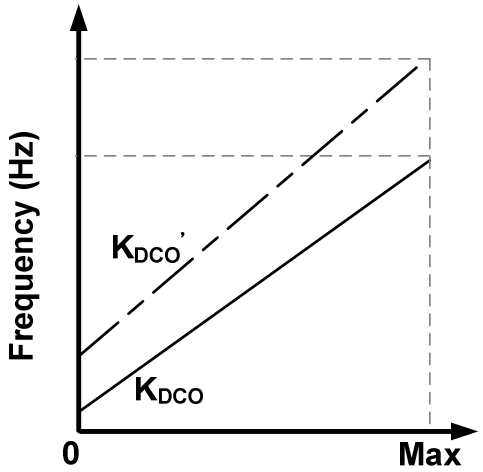


Fig. 4-14 The relationship of the frequency to the different digital codes

Fig. 4-14 shows the relationship of the frequency to the different digital codes of the DCO, where K_{DCO} is the target gain of the DCO and K_{DCO}' is the implemented gain of the DCO. If the implemented gain of the DCO is measured, the gain of the DCO could be normalized to the target gain. The concept of the DCO gain normalization is figured in Fig. 4-15.

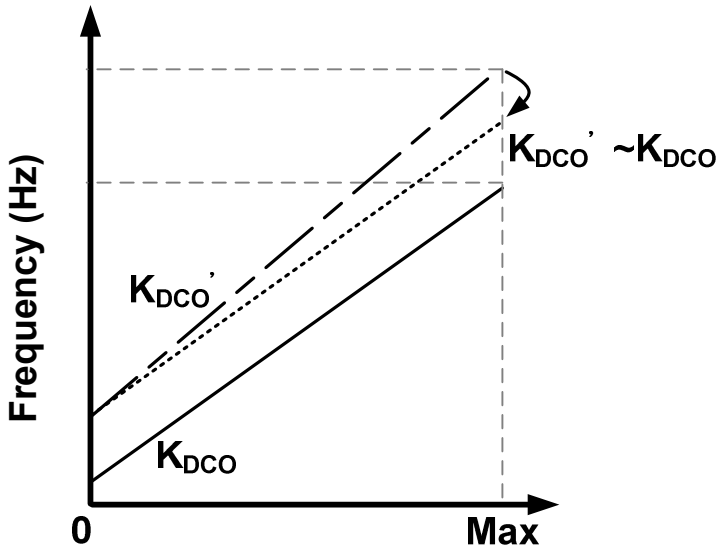


Fig. 4-15 The concept of the DCO gain normalization

To normalize the gain of the DCO, we might need a divider which is difficult to implement and cost great power consumption and area. As one knows, the ΔΣ modulator could not only provide high resolution but a divider with $1/2^N$, where N is the length of the accumulator in the ΔΣ modulator. If the length of the accumulator in the ΔΣ modulator could be changed, the normalization mathematics could be combined into the ΔΣ modulator.

In this design, the digital code for the required frequency 1.4GHz could be the initial value to speed up the locking process, but the value would be different with the drift of the characteristic of the DCO. If we find out the difference of the initial value L, we might calibrate the offset of the digital code. The concept of the DCO frequency offset calibration is shown in Fig. 4-16.

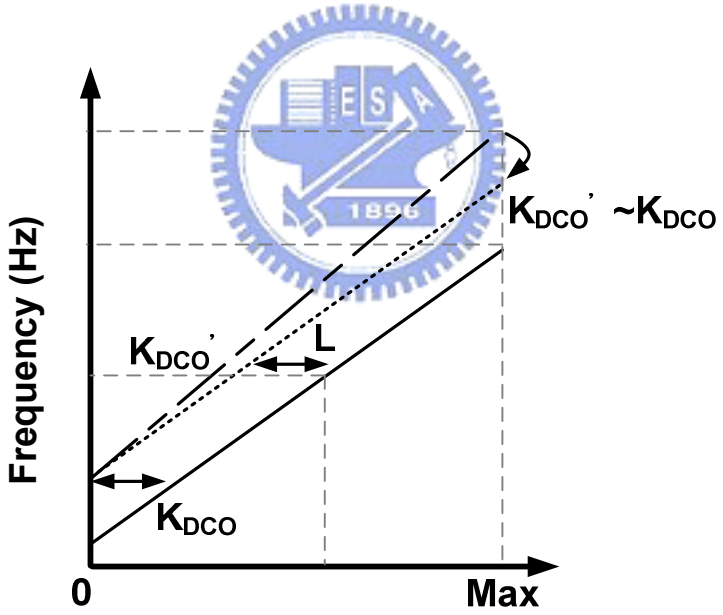


Fig. 4-16 The concept of the DCO frequency offset calibration

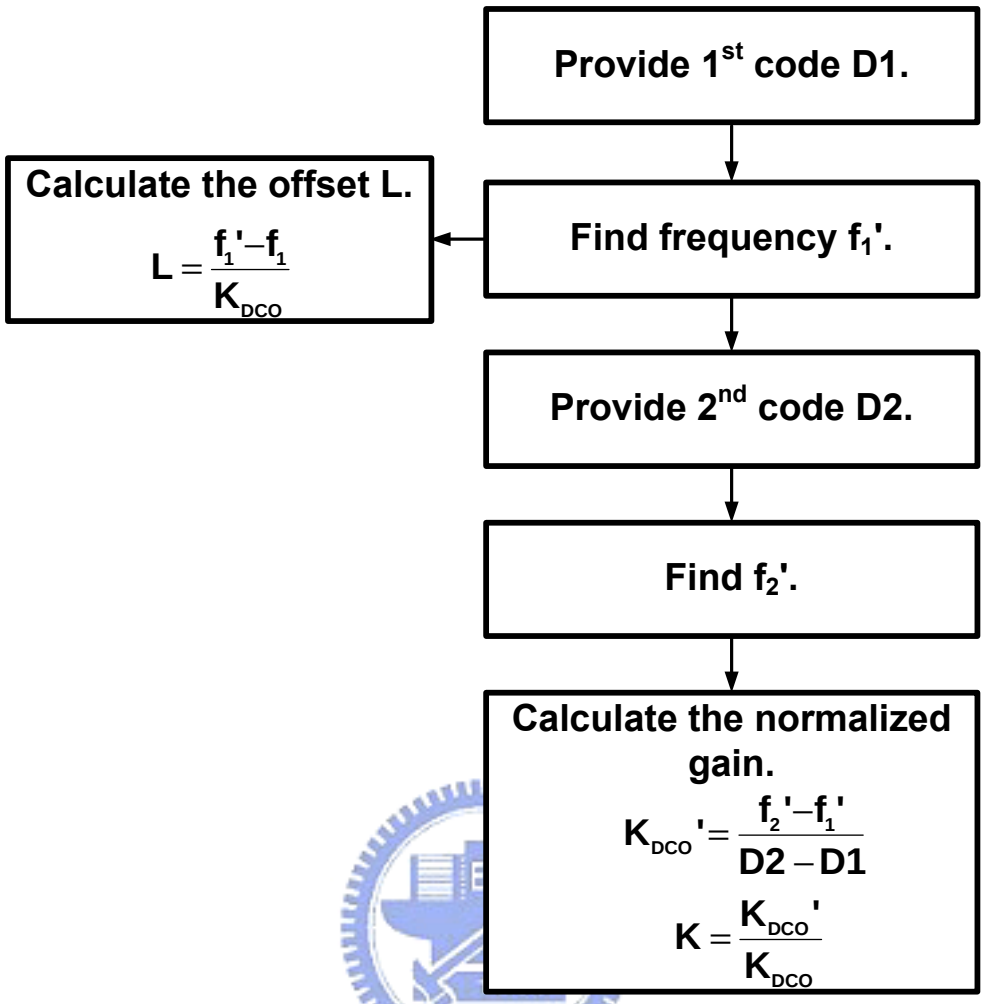


Fig. 4-17 The process of the DCC

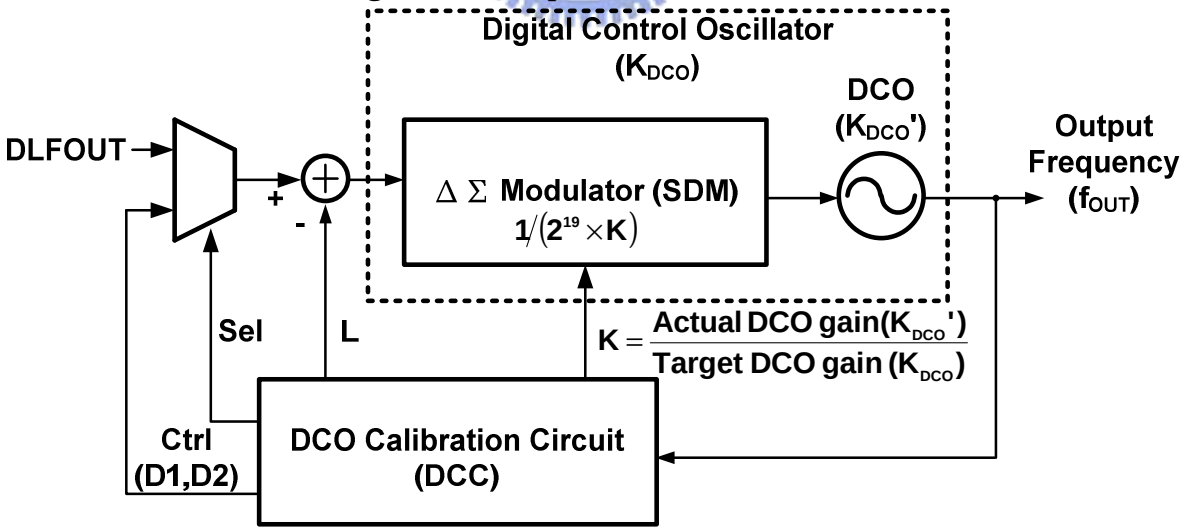


Fig. 4-18 Control method of the DCC

The process of the DCC and the control method is figured in Fig. 4-17 and Fig. 4-18. At the beginning of the DCC, it would provide the first control code

D1 and find out the output frequency f_1'. The target frequency f_1 is known from our design, so the offset of the digital code L could be express as equation 4.3.

$$L = \frac{f_1' - f_1}{K_{DCO}} \qquad (4.3)$$

The second control code D2 is sent to get the output frequency f_2'. The actual gain of the DCO could be measured by the difference of the output frequency f_1' and f_2', and the normalized gain K would be calculated. When the locking process starts, the control signals, K and L, would be sent into the DCO to calibrate the characteristic of the DCO.

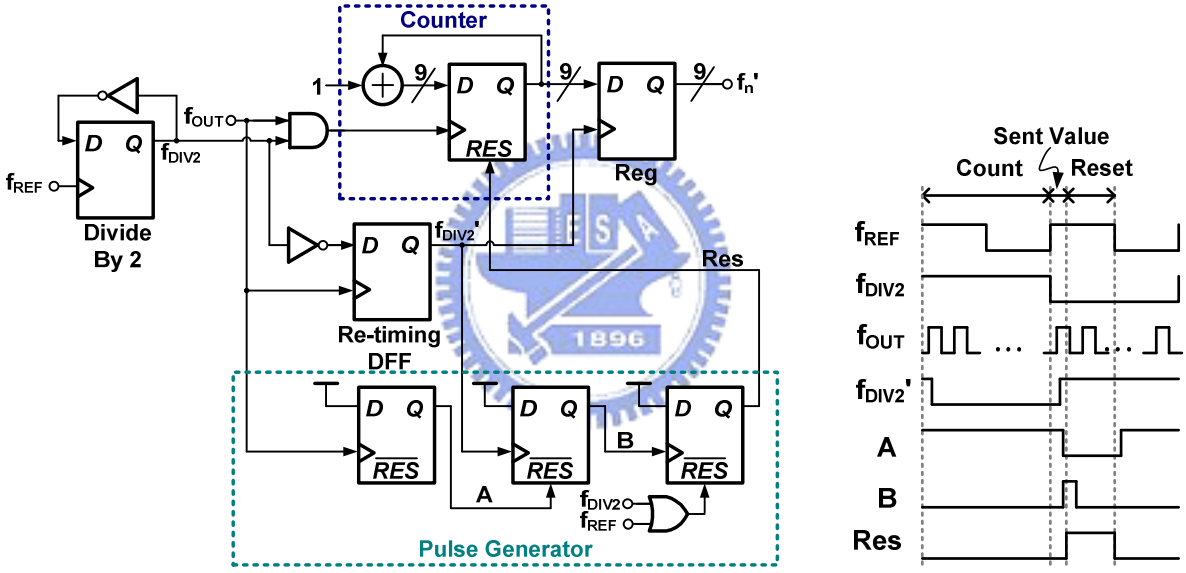
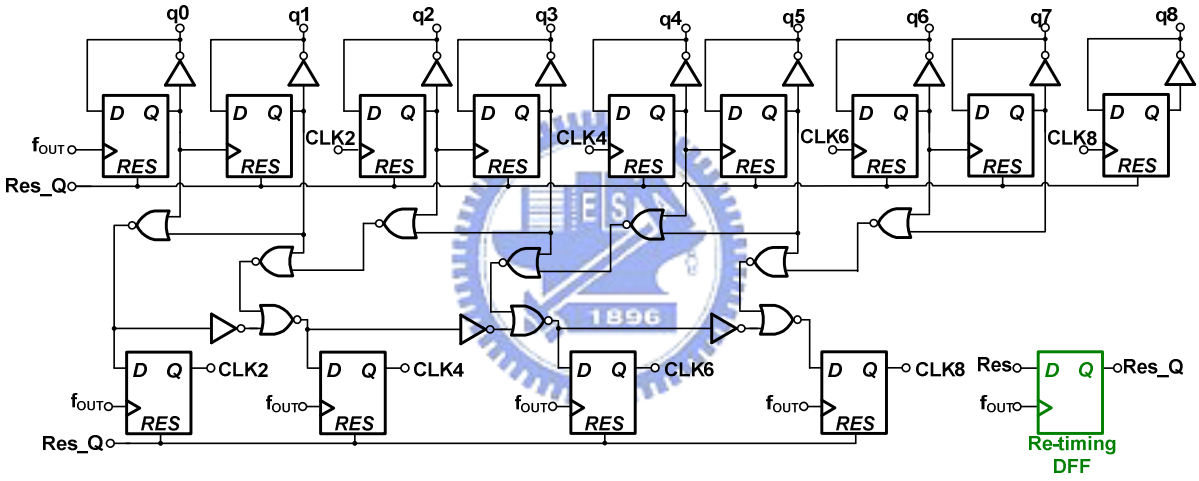


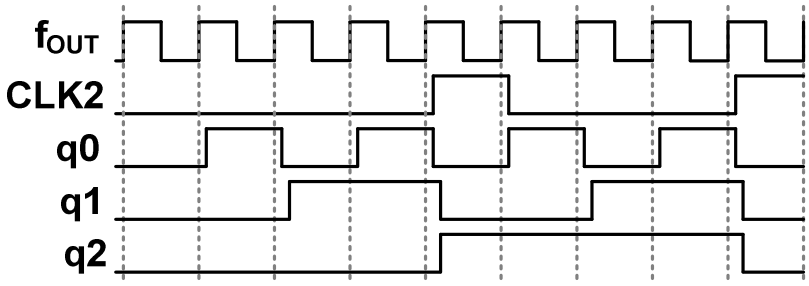
Fig. 4-19 The architecture of the frequency detector

To get the output frequency information, a frequency detector is used in DCC. The architecture of the frequency detector is shown in Fig. 4-19. A synchronous counter is used to count out the pulse number of the output clock in one period of the reference frequency, and the pulse number would be sent to digital circuits to do the calculation. The counter would be reset after the value catches by the registers. The frequency range of this frequency detector is about 2GHz.

The architecture of the synchronous counter and the time diagram of the first three bits are shown in Fig. 4-20. In generally speaking, an asynchronous counter consumes lower power than a synchronous counter, but the asynchronous counter is difficult to operate in high speed because of the propagation delay in the logic gates and the registers. To combine the advantages of these two types of the counters, each two bit are cascaded as an asynchronous counter stage, and each stage would be re-synchronous by the generated signal, CLK2, CLK4, CLK6, and CLK8. The reset signal of the counter has been oversampled to prevent data racing.



(a)



(b)

Fig. 4-20 (a) The architecture of the synchronous counter (b) The time diagram of the first three bits

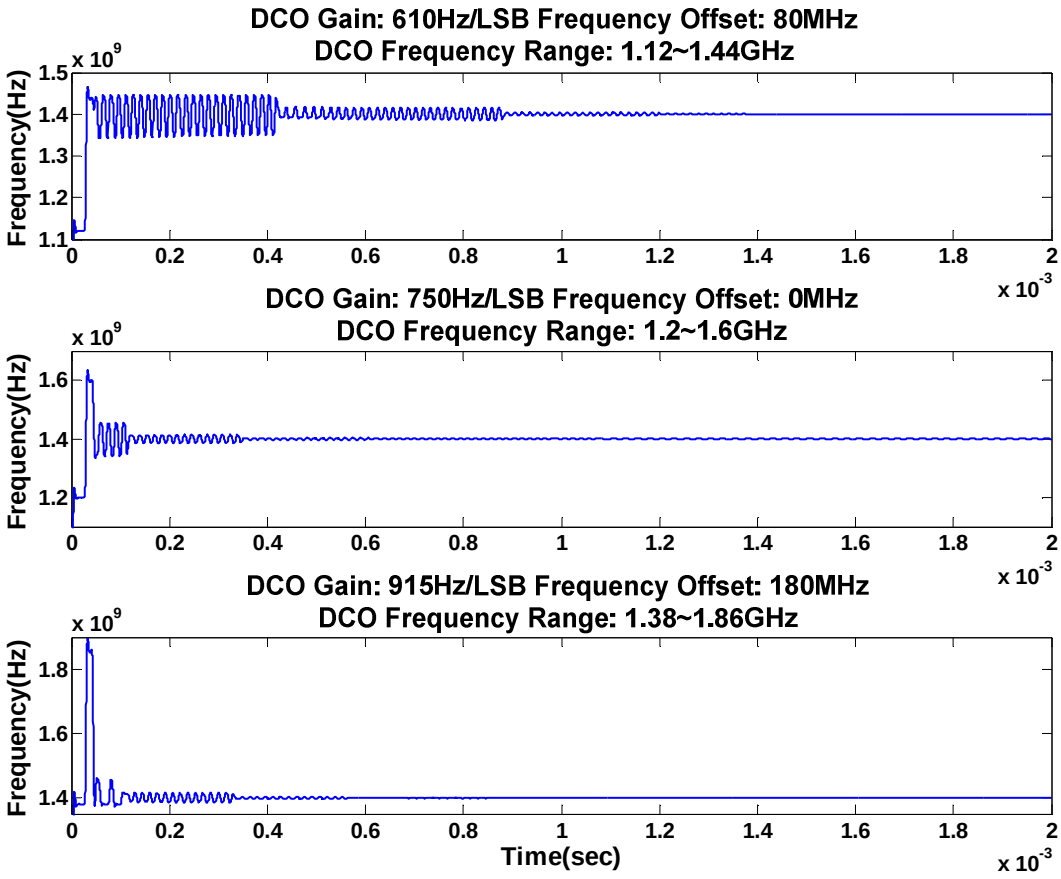


Fig. 4-21 The simulation results of the behavior model

The simulation results of the behavior model of the DCC are shown in Fig. 4-21. The DCO gain estimation error is defined as equation 4.4, where $\hat{K}_{DCO}'$ is the gain of the DCO after calibration.

$$\varepsilon = \frac{\hat{K}_{DCO}' - K_{DCO}}{K_{DCO}} \qquad (4.4)$$

The gain estimation error with different condition in Fig. 4-21 is list in Table 4-3.

Table 4-3 The gain estimation error with different condition in Fig. 4-21

DCO Gain (Hz/LSB)	DCO Gain Estimation Error (%)
610	0.93
750	0.5
915	0.21

4.4 Frequency Divider

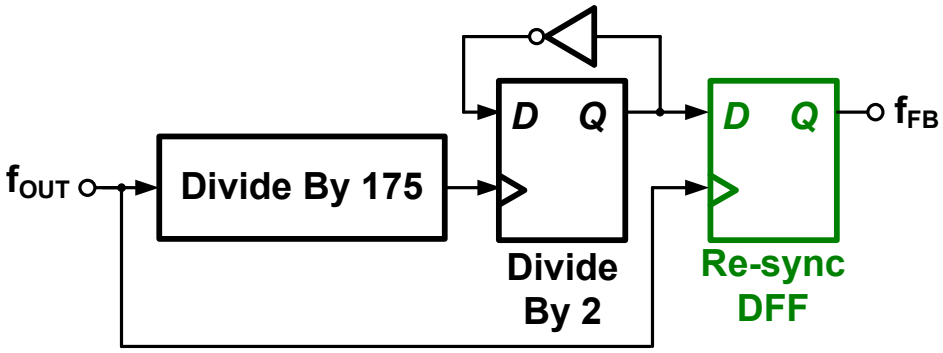


Fig. 4-22 The architecture of the frequency divider

The architecture of the frequency divider is shown in Fig. 4-22. In this design, the divider ratio has to be 350 for 4MHz reference clock. A divide by 175 and a divide by 2 are cascaded to implement this frequency divider, and a re-sync DFF is used to eliminate the accumulation error in the frequency divider.

In the last session, we use a synchronous counter as a frequency detector. To reduce the power consumption and the chip area, we use this counter cascaded with some logic gates as a divide by 175 in the tracking progress. The structure and the time diagram of the divide by 175 are figured in Fig. 4-23. Due to the reset signal of the counter would be retiming by a D flip-flop as Res_Q which is shown in Fig. 4-20, the reset signal of the counter has to be settle when the output of the counter is 173.

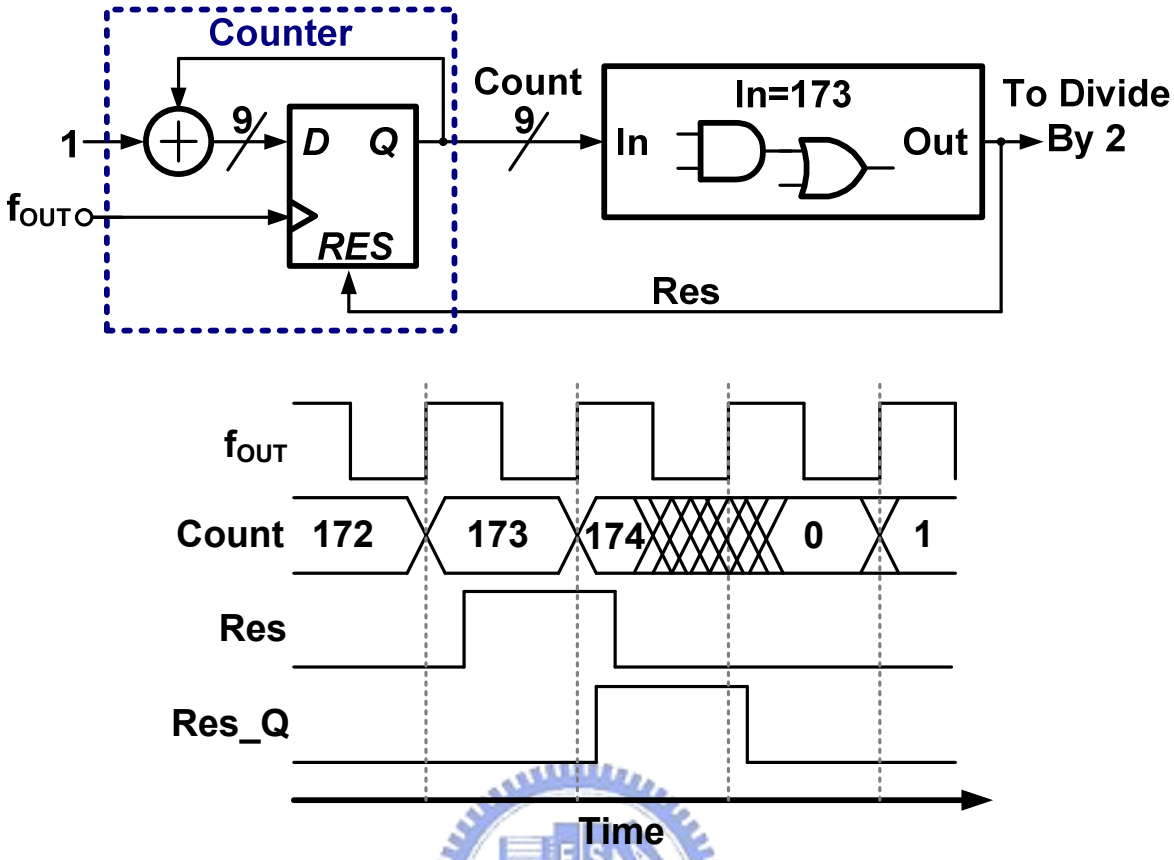


Fig. 4-23 The structure and the time diagram of the divide by 175

The post simulation results of the frequency divider with different corner are shown in Fig. 4-24.

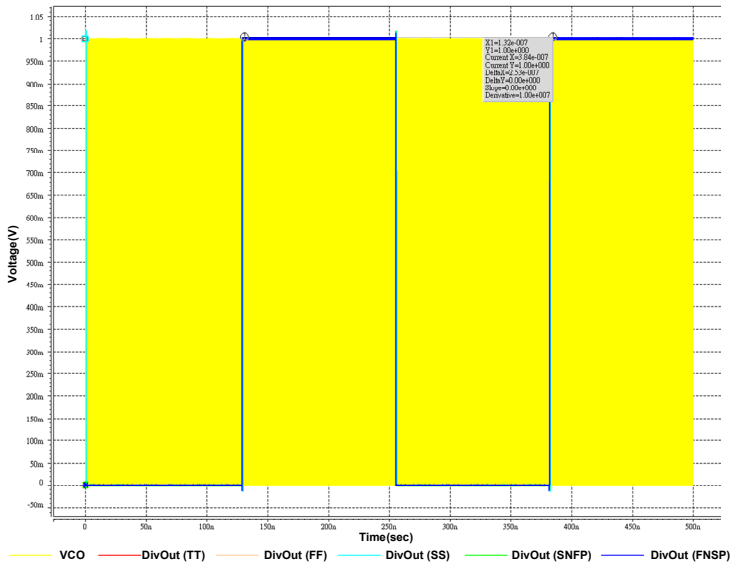


Fig. 4-24 The post simulation results of the frequency divider with different corner

Chapter 5 Experimental Results

5.1 Layout and Chip Photo

In Fig. 5-1 the layout of the ADPLL is shown, and the test chip is implemented in UMC 90nm 1P9M CMOS process. The layout of the ADPLL is composed by digital circuits which is used cell-based design flow and analog circuits designed by full-custom design flow. The digital circuits include the ΔΣ modulator and the digital controllers such as DLF and DCC; the analog circuits include the analog filter, the oscillator, frequency divider, the PD, and the output buffer.

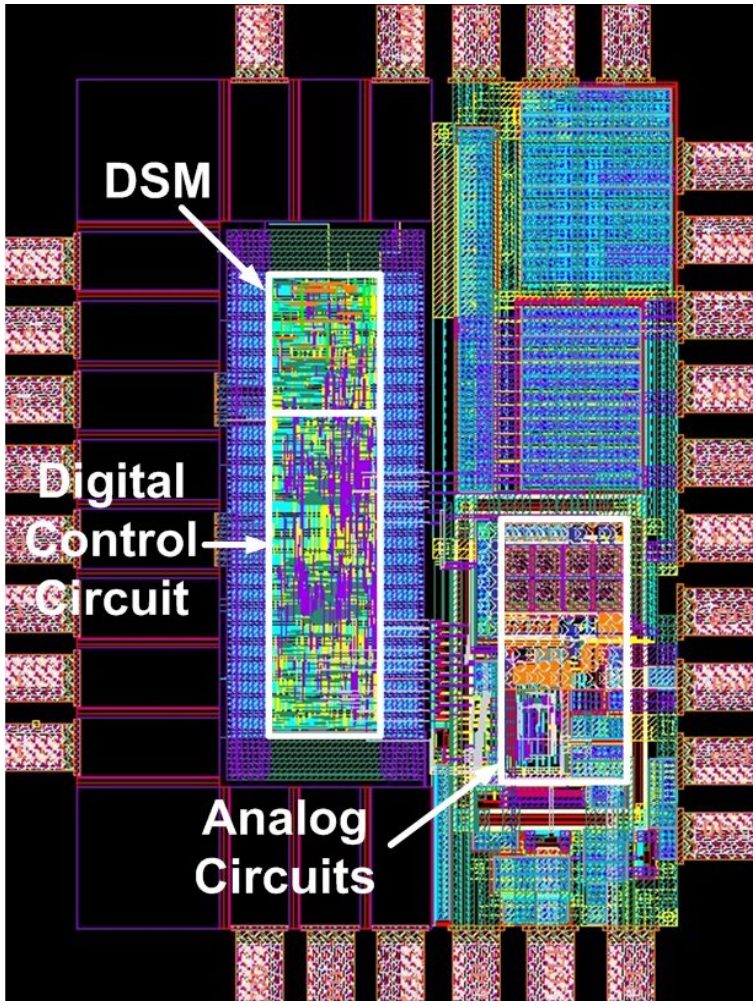


Fig. 5-1 The layout of the ADPLL

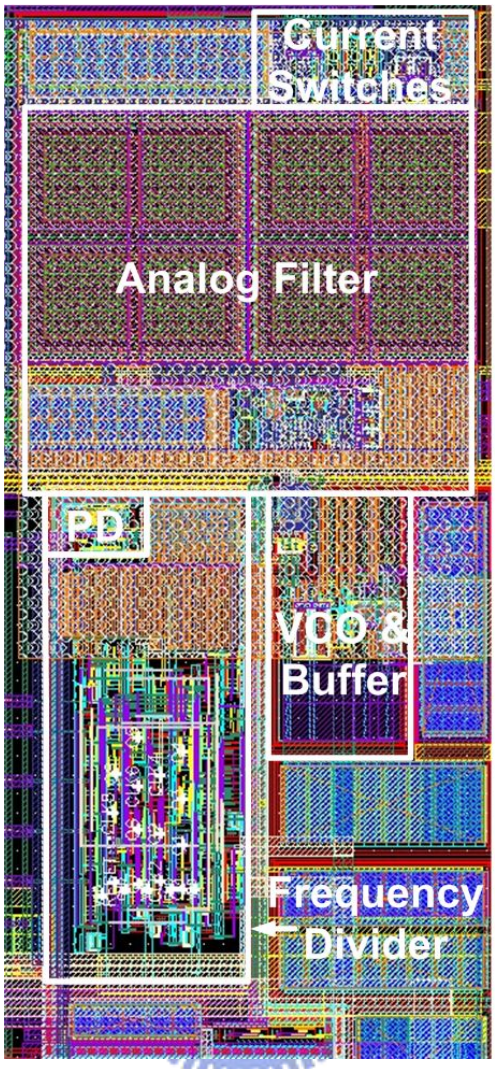


Fig. 5-2 The floor plane of the analog circuits

The area of the analog circuits is about 185.5 × 333.3 μm^2, and the floor plane of the analog circuits is figured in Fig. 5-2.The output of the ΔΣ modulator is near the current switches, and the analog filter is close to the current switches and the oscillator to minimize the loss on the signal path. The output buffer is beside the oscillator and the output pad to reduce the loading on the signal path. The frequency divider is put between the oscillator and the PD, and the signal path is as short as possible to eliminate the loop delay. To satisfy the requirements of the minimum metal and diffusion density defined in the design rule, MOS capacitors are put around the analog circuits as the bypass capacitors.

The photograph of the whole chip is shown in Fig. 5-3. Due to the metal filling procedure which is now standard in advanced sub-micron process, there is not much to be seen. Only the MIM capacitors have been excluded from the filling pattern.

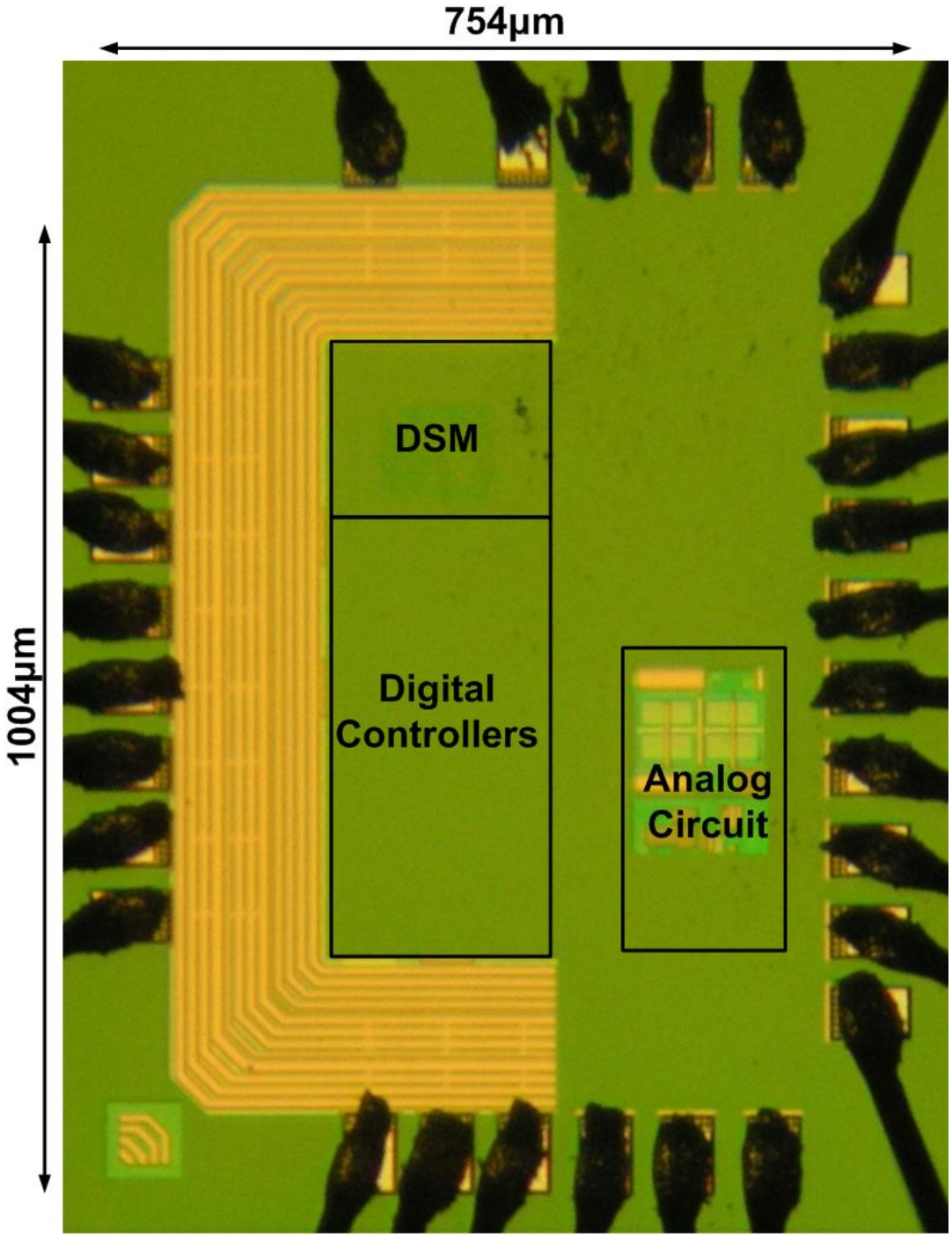


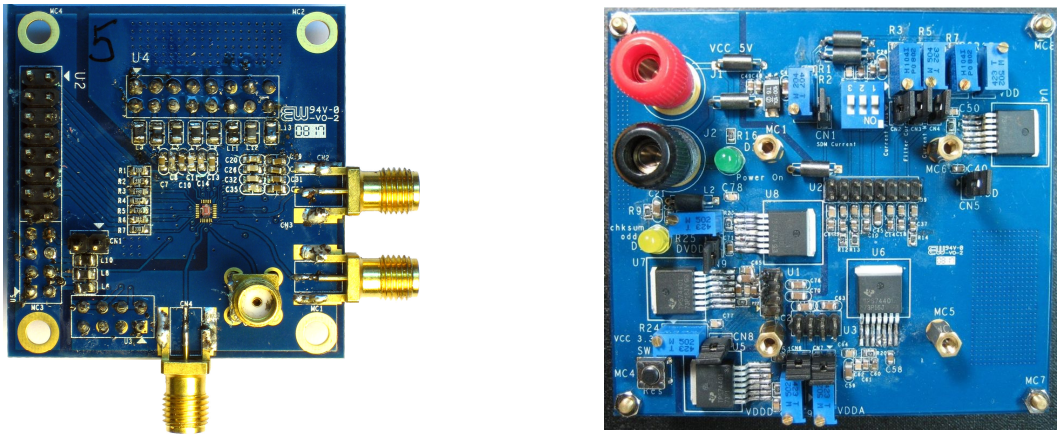
Fig. 5-3 The photograph of the whole chip

5.2 Experimental Setup

The photograph of the evaluation board is shown in Fig. 5-4. To shorten the RF signal as short as possible, the bias circuits and the control signals are put on the DC board, and the test chip is bonded at the center of the AC board with bond wires.

Fig. 5-4 (a) is the AC board. The 1.4GHz RF output, the output of the frequency divider, and the 4MHz reference clock are connected with semi-precision subminiature A (SMA) connectors, which provide 0 to 10 GHz broadband performance with low reflections and constant 50Ω impedance. The connectors on the left hand side of the AC board attach the evaluation board to a PC interface, which is used to control the test chip by means of a graphical user interface (GUI) computer program.

Fig. 5-4 (b) is the DC board. The DIP switch is used to control the bias condition of the DCO. To reduce the noise of each supply voltage and the bias current, low dropout linear (LDO) regulators, TPS74401, and bypass capacitors are added to provide low noise supply voltages and increase the performance of the ADPLL.



(a) (b)

Fig. 5-4 The evaluation board (a) AC board (b) DC board

The experimental setup is shown in Fig. 5-5. The reference input is provided using an Agilent E8257D signal generator which has a phase noise of about -130dBc/Hz at a 20 kHz offset. The RF output port is connected to an Agilent E4448A spectrum analyzer, and the output of the divider is observed by Agilent 86100C oscilloscope. The digital control signal input is provided by a PC with the GUI (Graphic User Interface).

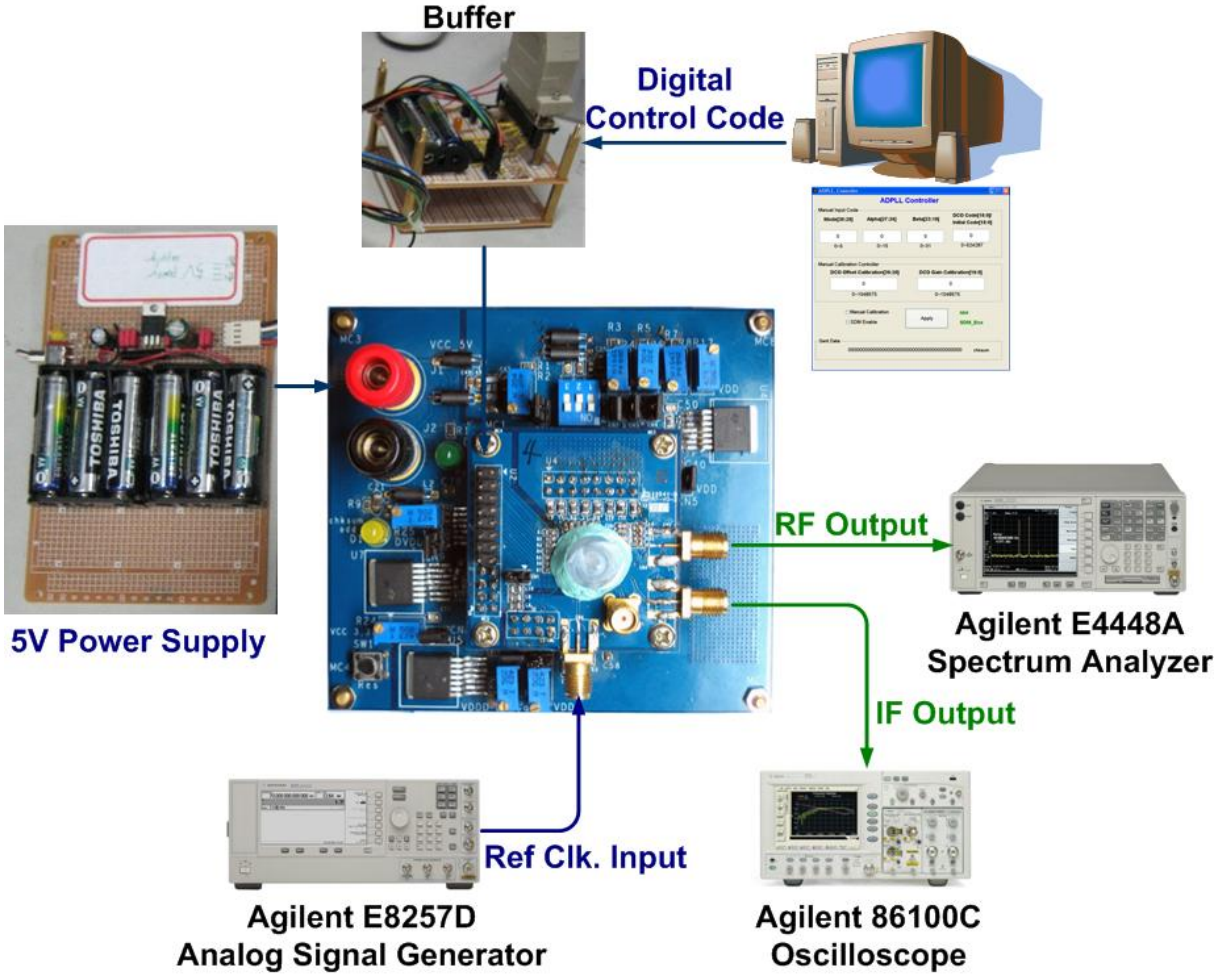


Fig. 5-5 The experimental setup

5.3 Experimental Results

5.3.1 Open-Loop of the ADPLL

The current bias of the DCO is the same of the post simulation of the DCO. The frequency range of the DCO is 1.338~1.715GHz. The tuning curve of the DCO is shown in Fig. 5-6.

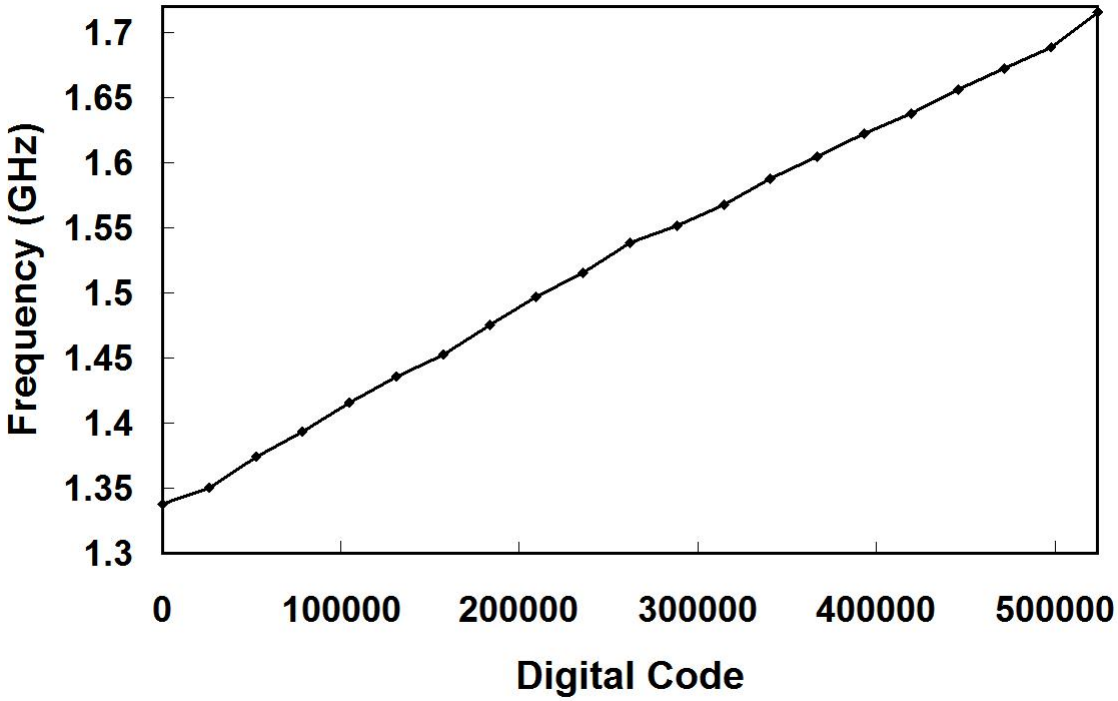
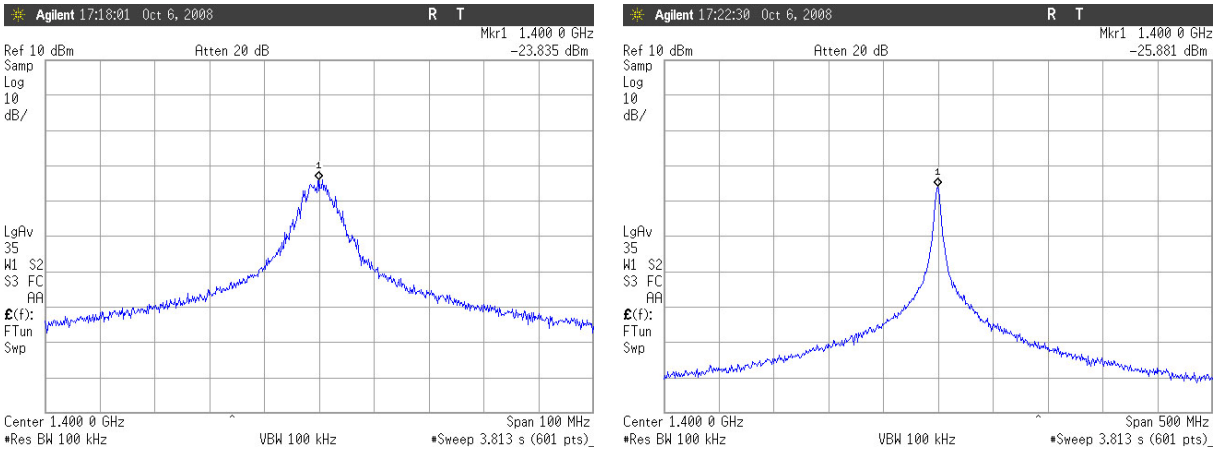
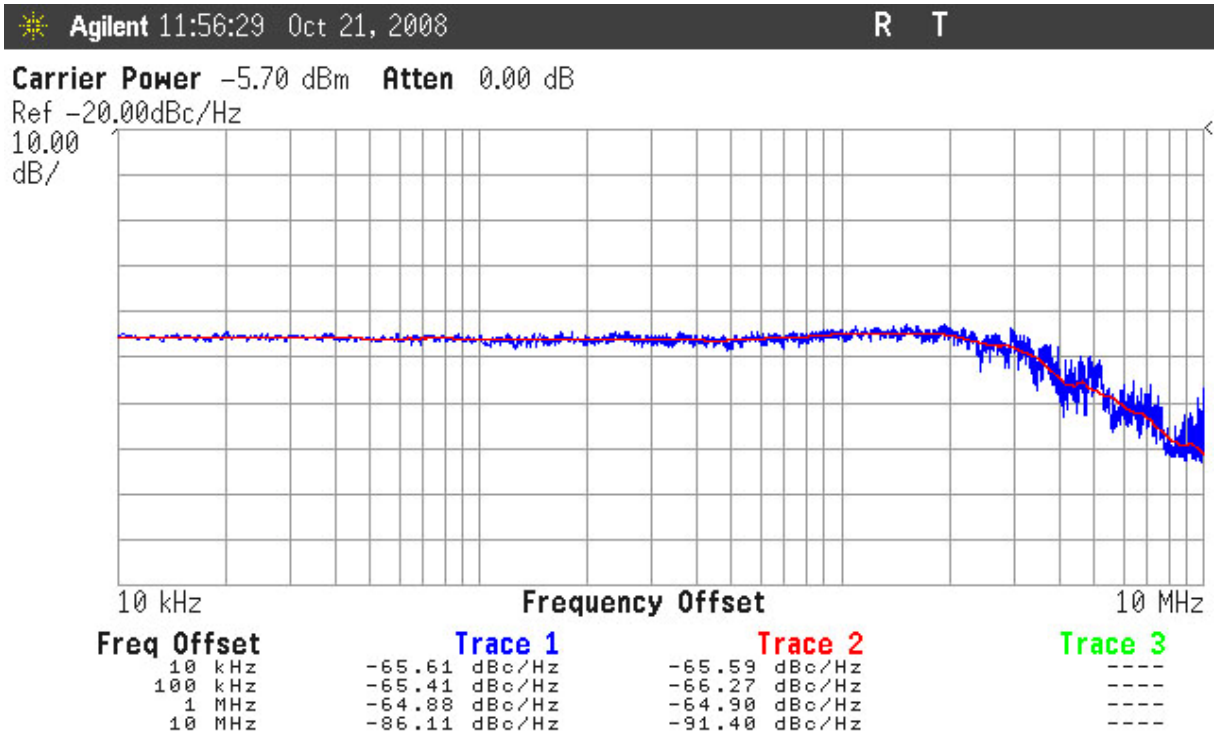


Fig. 5-6 The tuning curve of the DCO

The spectrum and the phase noise of the RF output without the DSM is shown in Fig. 5-7, and the phase noise at 1MHz offset is about -64.88dBc/Hz.



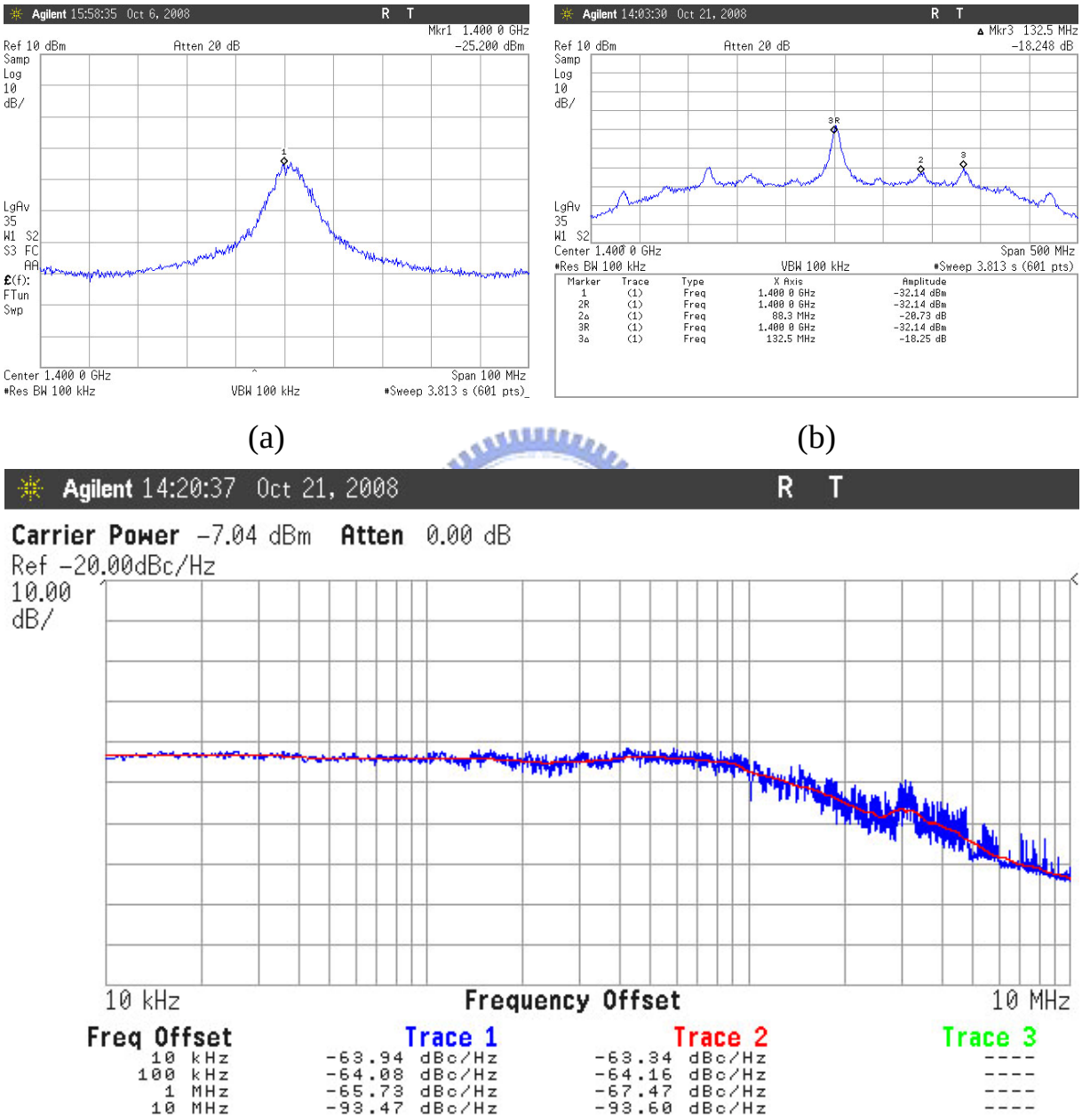
(a) (b)



(c)

Fig. 5-7 (a) The spectrum of the RF output without the DSM with 100MHz frequency span (b) The spectrum of the RF output without the DSM with 500MHz frequency span (c) The phase noise of the RF output without the DSM

The spectrum and the phase noise of the RF output with the DSM is shown in Fig. 5-8, and the phase noise at 1MHz offset is about -65.73dBc/Hz. The spur caused by the DSM appears on the spectrum when the frequency span is 500MHz.



(a) (b)

(c)

Fig. 5-8 (a) The spectrum of the RF output with the DSM with 100MHz frequency span (b) The spectrum of the RF output with the DSM with 500MHz frequency span (c) The phase noise of the RF output with the DSM

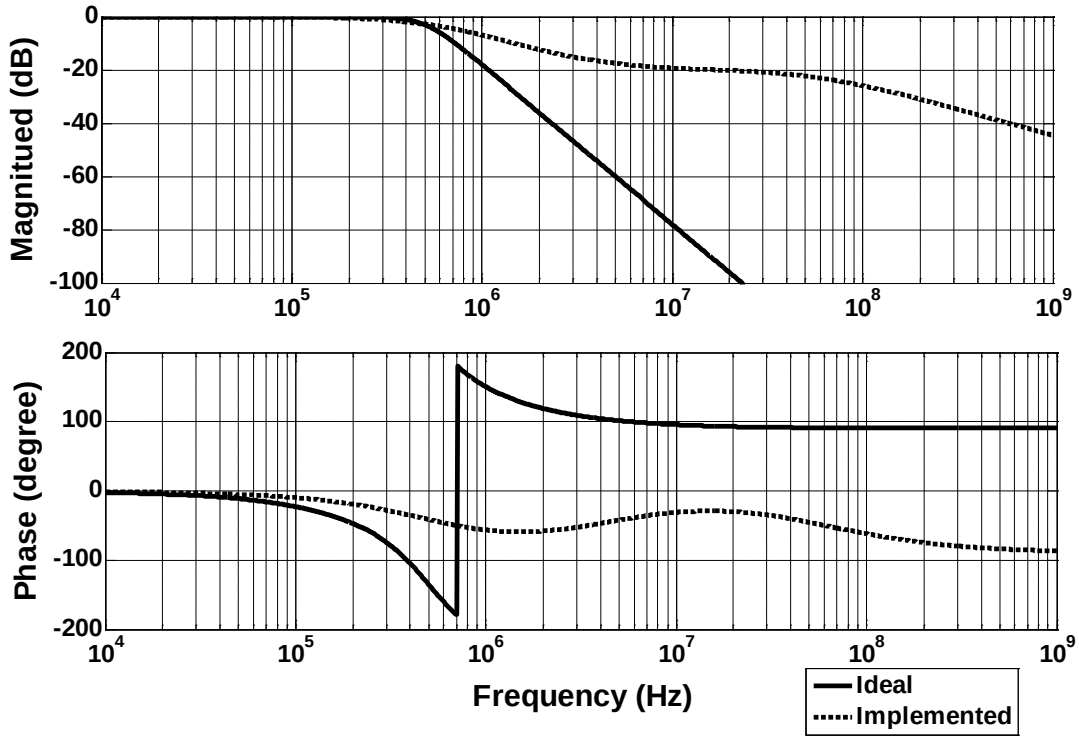


Fig. 5-9 The frequency response of the ideal and the implemented analog filter

Table 5-1 The distribution of the poles and the zeros

	Implemented Filter
Pole 1	-610.24kHz
Pole 2	-882.63kHz
Pole 3	-57.97MHz
Zero 1	-1.28MHz
Zero 2	-4.16MHz

From Fig. 5-7 and Fig. 5-8, we could observe that the characteristics of the analog filter might be different from the original design, and that causes the quantization noise of the DSM couldn't be reduce properly. Fig. 5-9 compares the frequency response of the ideal analog filter and the implemented analog filter. The distribution of the poles and the zeros is shown in Table 5-1. The third pole is much far from the second pole, and two zeros induced into the implemented filter by the impedance scalar. The magnitude of the implemented analog filter couldn't decade rapidly because the zeros are near from the second

pole. Fig. 5-10 is the phase noise of the DCO with the ideal filter and the implemented analog filter, excluding the nature noise of the DCO.

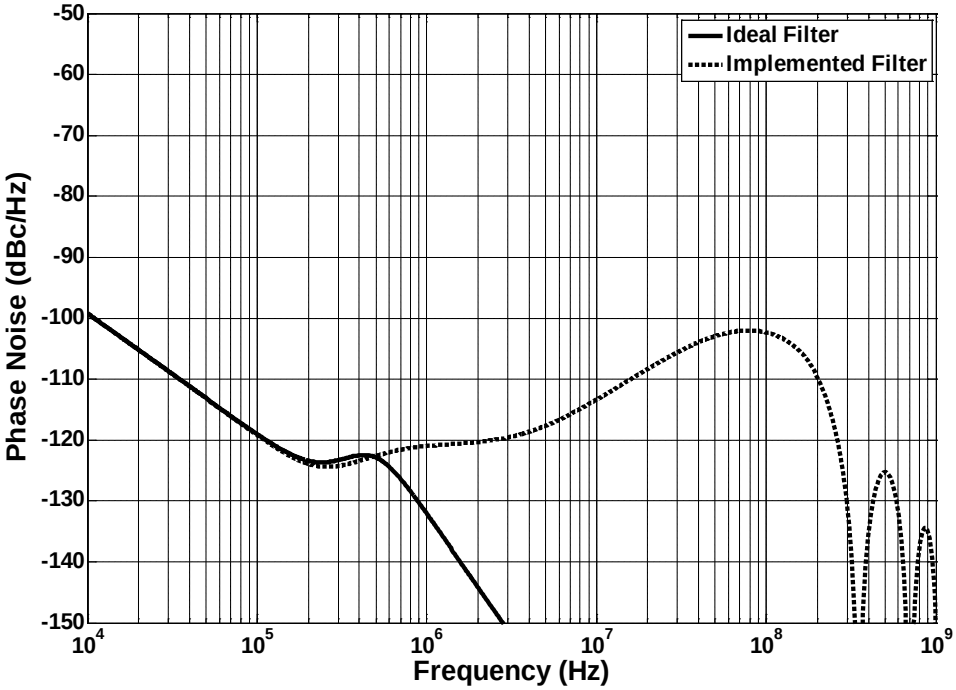


Fig. 5-10 The phase noise of the DCO with different analog filter, excluding DCO nature noise

Fig. 5-11 shows the output of the frequency divider at 1.3 GHz and 1.7 GHz RF output frequency, and the frequency divider could work at the highest and the lowest RF output frequency.

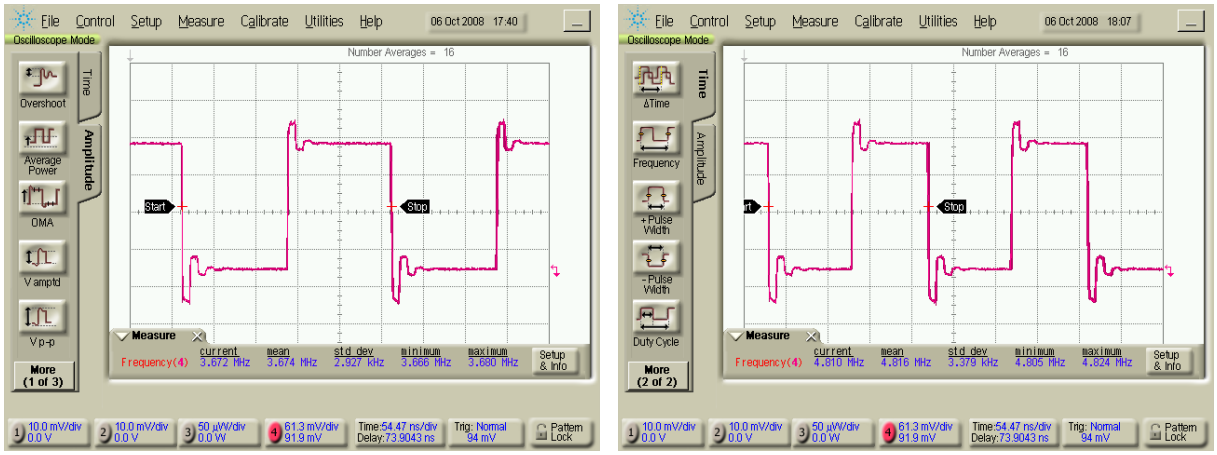
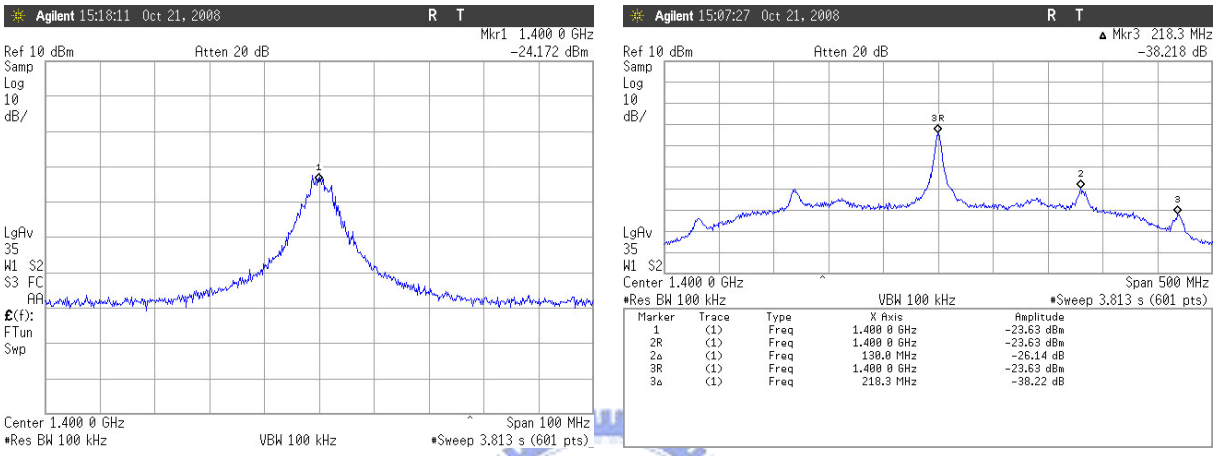


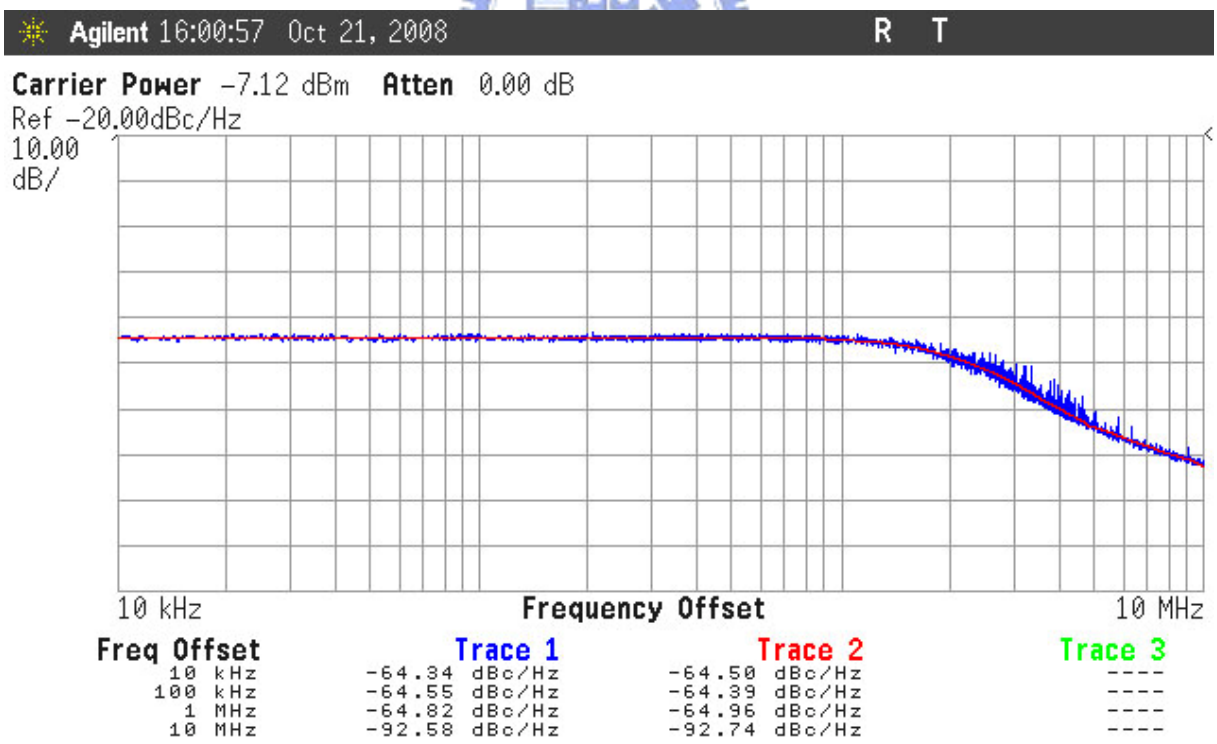
Fig. 5-11 The output of the frequency divider with 1.3 GHz and 1.7 GHz RF output frequency

5.3.2 Closed-Loop of the ADPLL

The spectrum and the phase noise of the RF output are shown in Fig. 5-12. The center frequency is 1.4 GHz, and the phase noise at 1MHz offset is -64.82dBc/Hz.



(a) (b)

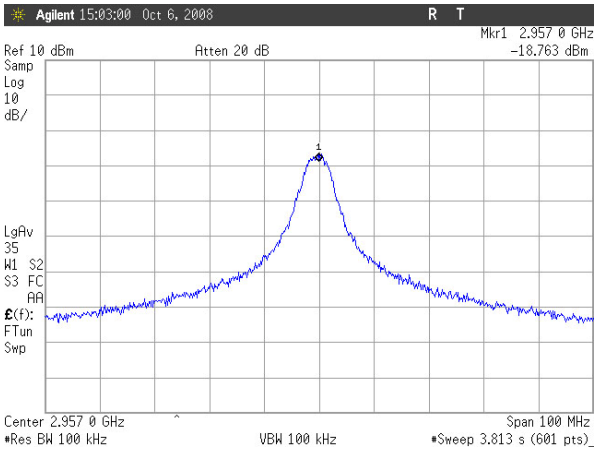


(c)

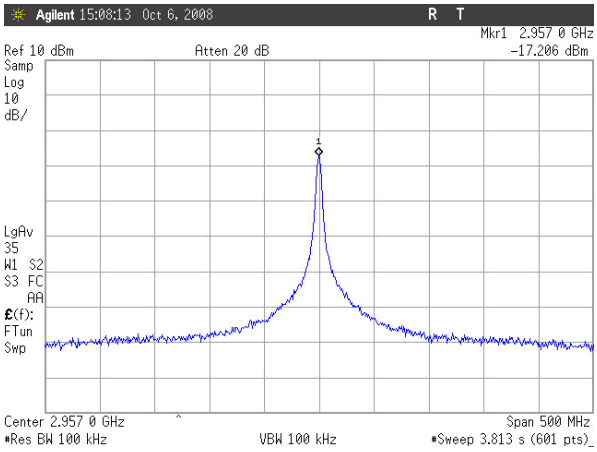
Fig. 5-12 (a) The spectrum of the RF output with 100MHz frequency span (b) The spectrum of the RF output with 500MHz frequency span (c) The phase noise of the RF output

The analog filter doesn’t work very well, and that causes the spur of the DSM on the frequency domain. We let the PLL work on higher frequency and figure the spectrum and the phase noise of the RF output shown in Fig. 5-13. The center frequency is 2.957 GHz, and the phase noise at 1MHz offset is -57.28dBc/Hz.The spur of the DSM is moved to higher frequency because of the higher over sampling rate. Due to the larger transconductance of the transistors caused by the increasing bias current from 10 μA to 50 μA, the bandwidth of the analog filter would be higher, and the phase noise of the PLL doesn’t improve enough.

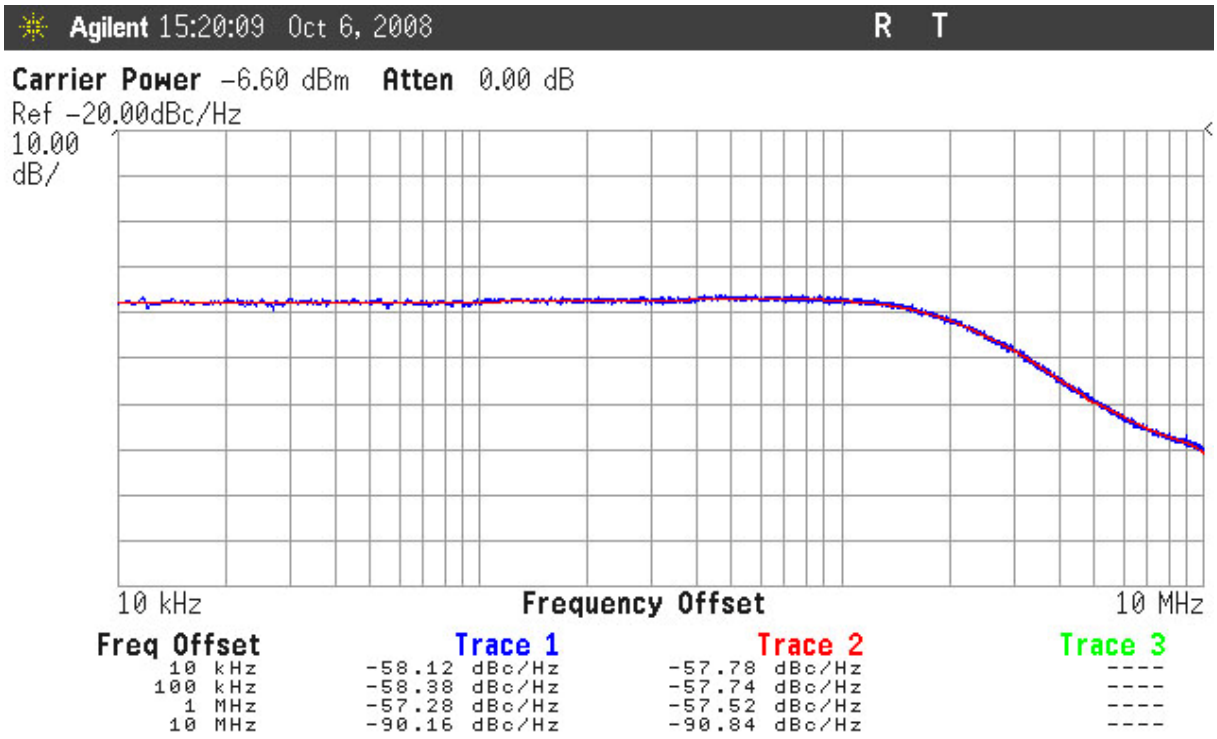
When the DCC is enabled, the spectrum and the phase noise of the RF output are shown in Fig. 5-14. The phase noise at 1MHz offset is -64.79dBc/Hz.



(a)

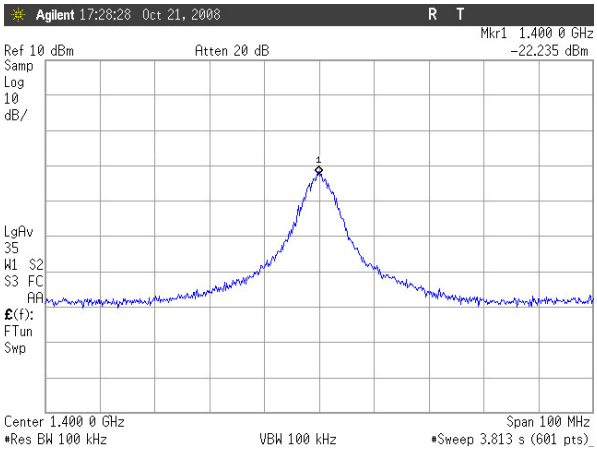


(b)

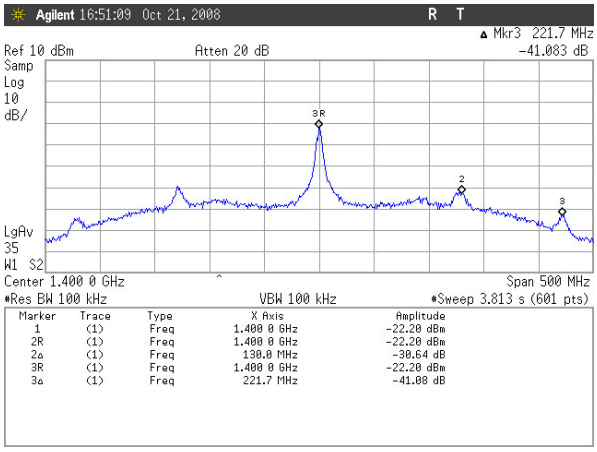


(c)

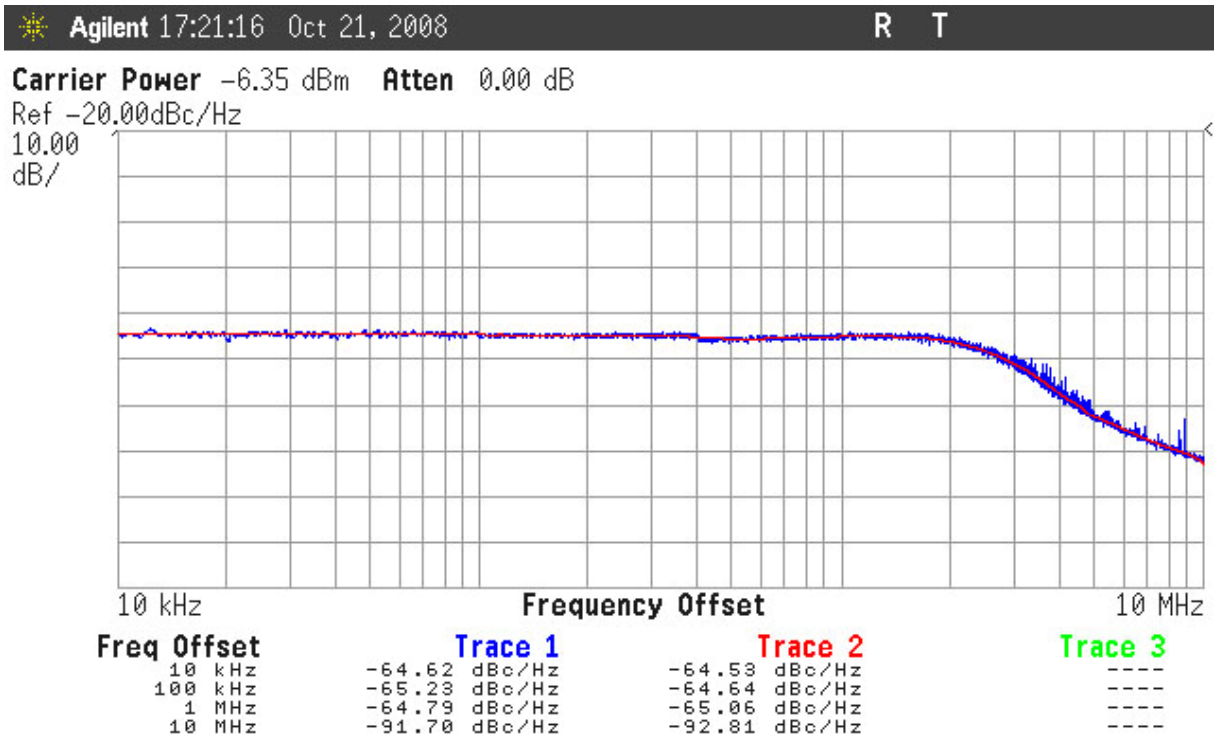
Fig. 5-13 (a) The spectrum of the RF output with 100MHz frequency span (b) The spectrum of the RF output with 500MHz frequency span (c) The phase noise of the RF output with higher bias current of the analog filter



(a)



(b)



(c)

Fig. 5-14 After the DCC enabled, (a) The spectrum of the RF output with 100MHz frequency span (b) The spectrum of the RF output with 500MHz frequency span (c) The phase noise of the RF output with higher bias current of the analog filter

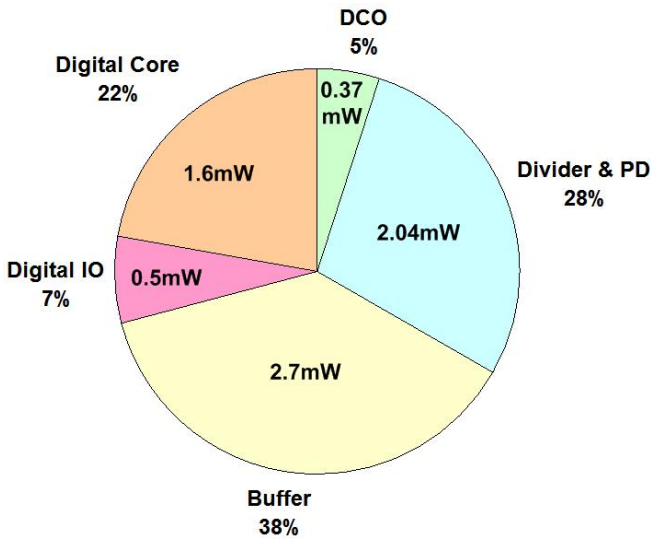


Fig. 5-15 The power distribution of the ADPLL

The power distribution of the ADPLL is figured in Fig. 5-15. The total power, excluding the digital IO and the buffer, is 4.01mW.

5.4 Performance Summary

The performance summary of this thesis is shown in Table 5-2.

Table 5-2 Performance Summary

Process		UMC 90nm
Supply Voltage		1V
Reference Frequency		4MHz
Output Frequency		1.4GHz
Phase Noise		-64.82dBc/Hz @ 1MHz
Power Consumption	DCO	0.37mW
	Divider & PD	2.04mW
	Digital Core	1.6mW
	Total	4.01mW
Chip Area		0.757mm^2

Chapter 6 Conclusion

A low power digital phase locked loop with self-calibration is implemented.

- This system is implemented with digital feature which would be more robust against the PVT variation and easier to operate under low supply voltage.
- A ΔΣ modulator is used in DCO to provide a high resolution and current fine tuning which is less than 10μA. The noise contributed by the ΔΣ modulator is analyzed, and a 500 kHz analog filter is added to reduce the effect of the ΔΣ modulator to the whole system.
- A DCO calibration circuit is proposed to adjust the characteristic of the DCO and precisely match between the dynamic loop filter and the desire transfer function across the PVT variation.

Reference

[1] IEEE 802.15.4 WPAN-LR Task Group “http://www.ieee802.org/15/pub/TG4.html”

[2] IEEE 802.15.1, “http://www.ieee802.org/15/pub/TG1.html”

[3] Wireless Medical Telemetry, “http://www.fda.gov/cdrh/emc/wmt/index.html”

[4] S. Beyer, "A 2.4GHz direct modulated 0.18um CMOS IEEE 802.15.4 compliant Transmitter for ZigBee," *IEEE Custom Integrated Circuits Conference*, pp. 121-124, 2006.

[5] W. Rahajandraibe, "Frequency Synthesizer and FSK Modulator for IEEE 802.15.4 Based Applications," *RFIC Symposium, 2007 IEEE*, pp. 229-232, 2007.

[6] Ching-Lung Ti, "A 2.4-GHz 18-mW Two-Point Delta-Sigma Modulation Transmitter for IEEE 802.15.4," *VLSI Design, Automation and Test, 2007. VLSI-DAT 2007. International Symposium on*, pp. 1-4, 2007.

[7] B. Razavi, *Design of Integrated Circuits for Optical Communications.* Boston: McGraw-Hill, 2003.

[8] R. B. Staszewski, Chih-Ming Hung, D. Leipold and P. T. Balsara, "A first multigigahertz digitally controlled oscillator for wireless applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 51, pp. 2154-2164, 2003.

[9] R. B. Staszewski, J. Wallberg, S. Rezeq, Chih-Ming Hung, O. Eliezer, S. Vemulapalli, C. Fernando, K. Maggio, R. Staszewski, N. Barton, Meng-Chang Lee, P. Cruise, M. Entezari, K. Muhammad and D. Leipold, "All-digital PLL and GSM/EDGE transmitter in 90nm CMOS," *ISSCC*, Vol. 1, pp. 316-600, 2005.

[10] R. B. Staszewski and P. T. Balsara, "Phase-domain all-digital phase-locked loop," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 52, pp. 159-163, 2005.

[11] R. B. Staszewski, "A digitally controlled oscillator in a 90 nm digital CMOS process for mobile phones," *IEEE Journal of Solid-State Circuits*, vol. 40, pp. 2203-2211, 2005.

[12] N. Da Dalt, "A design-oriented study of the nonlinear dynamics of digital bang-bang PLLs," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 52, pp. 21-31, 2005.

[13]N. D. Dalt, "Markov Chains-Based Derivation of the Phase Detector Gain in Bang-Bang PLLs," *IEEE Transactions on Circuits and System s II: Express Briefs*, vol. 53, pp. 1195-1199, 2006.

[14]A. Hajimiri, S. Limotyrakis and T. H. Lee, "Jitter and phase noise in ring oscillators," *IEEE Journal of Solid-State Circuits*, vol. 34, pp. 7 90-804, 1999.

[15]N. Da Dalt, E. Thaller, P. Gregorius and L. Gazsi, "A compact triple-band low-jitter digital LC PLL with programmable coil in 130-nm C MOS," *IEEE Journal of Solid-State Circuits*, vol. 40, pp. 1482-1490, 2005.

[16]S. Solis-Bustos, J. Silva-Martinez, F. Maloberti and E. Sanchez-Sinenci o, "A 60-dB dynamic-range CMOS sixth-order 2.4-Hz low-pass filter f or medical applications," *IEEE Transactions on Circuits and Systems I I: Analog and Digital Signal Processing*, vol. 47, pp. 1391-1398, 200 0.

簡歷

基本資料				
中文姓名	張巧伶	英文姓名	Chiao-Ling, Chang	
聯絡電話	0937004143	電子信箱	7350324@gmail.com	
通訊地址	新竹市大學路 81 巷 27 號			
戶籍地址	台北縣板橋市幸福路 60 巷 45 號 4F			
宗教	基督教			
教育背景				
學歷	學校	系所	組別	時間
碩士	國立交通大學	電子所	系統組	94.9~97.11
大學	國立中興大學	電機工程學系		90.9~94.6 畢
高中	台北市立第一女子高級中學			87.9~90.6 畢
專長				
修習科目	類比積體電路(一)(二) 數位積體電路 有線傳輸通信積體電路設計 行動通訊 適應性訊號處理 數位通訊 鎖相迴路設計與應用			
專業能力	類比電路設計 鎖相迴路設計	Full-Custom Design Flow Cell-Based Design Flow		
熟悉軟體	MATLAB/Simulink HSPICE Spectre RF Virtuoso Calibre	Verilog Design Vision SOC Encounter Office: Word, Excel, Power Point		
特殊表現	CIC 下線審查評鑑:B 斐陶斐榮譽會員 中興大學菁莪獎 大三書券獎兩學期 大二書券獎兩學期 大一書券獎兩學期			