國 立 交 通 大 學

電子工程學系 電子研究所

博 士 論 文

新式奈米碳管電晶體製造與特性研究

A Study on the Fabrication and Characteristics of Novel Carbon Nanotube Field-Effect Transistors

研 究 生: 陳 百 宏

指導教授: 黃 調 元 博士

趙 天 生 博士

中 華 民 國 九 十 五 年 七 月

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研 究 生：陳 百 宏　　Student: Bae-Horng Chen

指導教授：黃 調 元 博士　　Advisor: Dr. Tiao-Yuan Huang

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博 士 論 文

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推薦函

事由：推薦電子研究所博士班研究生 陳百宏 先生提出論文以參加國立交通大學博士論文口試。

說明：本校電子研究所博士班研究生陳百宏，業已完成電子所之規定學分，通過博士資格考中之學科考試，並完成博士論文初稿之撰寫，論文名稱為：**新式奈米碳管電晶體製造與特性研究 (A Study on the Fabrication and Characteristics of Novel Carbon Nanotube Field-Effect Transistors)**。博士論文內容中並有數篇論文發表或送審於國際學術期刊，茲列舉如下：

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3. “Localized lateral growth of single-walled carbon nanotubes for field-effect transistors by a cobalt-mix-TEOS method,” ***Electrochemical and Solid-State Letters***, Vol. **8**, pp.G290-G293, August, 2005.
4. “Complementary carbon nanotube-gated carbon nanotube thin-film transistor,” ***Appl. Phys. Lett.***, Vol. **88**, p.093502, February, 2006.
5. “Localized laterial growth of single-walled carbon nanotube by novel cobalt mix TEOS method,” in ***Twelfth Canadian Semiconductor Technology Conference***, p.105, Ottawa, Canada, 2005
6. “A novel method to convert metallic-type CNTs to semiconducting-type CNT-FETs,” ***Solid State Devices and Materials Symp.,*** pp.776-777, Kobe, Japan, 2005.
7. “Gate-position effects on tunable conduction-type carbon nanotube field effect transistors,” in ***NT06 : Seventh International Conference on the Science and Application of Nanotubes,*** Nagano, Japan, 2006.
8. **“**Prospect of cobalt-mix-TEOS method on localized lateral growth of carbon nanotubes for both p- and n-Type field effect transistors,**” *Journal of Vacuum Science & Technology B***, accepted for publication, July, 2006.

綜上所陳，陳君已具備國立交通大學電子研究所應有之教育及訓練水準，謹此推薦並請准予參加博士論文畢業口試。

國立交通大學電子所教授　　黃調元博士

國立交通大學電子物理所教授　　趙天生博士

新式奈米碳管電晶體製造與特性研究

研究生: 陳百宏　　指導教授: 黃調元博士

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摘要

在本論文中，我們詳細描述了奈米碳管電晶體(CNT-FET)與生化感測器(bio-sensor)的光罩設計與其製程步驟。其中包括光罩中各個不同的功能區塊的描述以及主要元件的設計尺寸大小。同時我們也設計兩種不同的觸媒島(catalyst island)供在觸媒化學氣相沉積法(catalytic chemical vapor deposition)中，成長單壁奈米碳管(single-walled carbon nanotube) ，以提供奈米碳管電晶體中的半導體層，也就是通道(channel)使用。

首先，為了改善每一批次製造出來的 CNT-FET，其電特性相差甚多(主要為 P 型與雙極性(ambipolar 型)。我們提出一個有上下閘極(gate electrode)的雙閘極奈米碳管電晶體(DG CNT-FET)架構，且上下閘極的電壓可以獨立控制，藉以調變 CNT-FET 能帶(energy band) ，來獲得所需要的具特定電特性的 CNT-FET。對一個 Double-gated CNTFET 來說，利用上閘極(top gate)之正負偏壓控制，可以調整 CNT-FET 中央能帶彎曲之方向，亦即在 CNT 中間製造了一個能障(energy barrier)，而依據上閘極偏壓方向的不同，所製造出的能障方向也不同。所以原本因為製程中不可控制因素而造成的雙向導通型的 CNT-FET，可藉由上閘極之正

負偏壓控制，即可調變使雙向導通型(ambipolar type)的奈米碳管電晶體轉換成 p-type 或 n-type 導通之 CNT-FET。

其次，奈米碳管的導電性與其螺旋性(chirality)向量有關。而現存的 CNT 成長過程中，沒有方法可以控制其 chirality，導致世界上所有的研究團隊所成長出來的 CNT，其金屬性(metallic-type)/半導體性(semiconducting-type)的 CNT 往往都是混雜在一起，不僅比率很難控制，成長 CNT 之後也很難將半導體性的 CNT 分離出來。這是要將 CNT 有效運用在 FET 與 sensor 的研究上，一個很難突破的瓶頸，因為金屬性 CNT 的存在會破壞 FET 的運作，使得 FET 不具備良好的電晶體功能。而吾人提出以氬氣電漿(argon plasma)對成長完後的 CNT 做離子轟擊(ion bombardment)，可以使 metallic-type CNT 因為以電漿處理時產生的 eddy current 而將其燒毀，或造成 metallic-type CNT 的 point defect，使其等效/有效的對稱結構改變，因而顯示出 semiconductin-type 的特性。我們的實驗也顯示，原本 p-type 的 CNT-FET 在接受電漿處理後仍然為 p-type。

為了使奈米碳管可以應用於微電子元件中，我們也發展一種定位成長 SWNT 的觸媒化學氣相沉積法。在此論文中，我們以奈米級鈷(Co)觸媒顆粒與四氧乙基矽(tetraethoxysilane, TEOS)的混合溶液來形成觸媒層，隨後會用黃光與蝕刻製程在特定的位置形成觸媒島(catalyst islands)，其結構可用於 CVD 方式成長 SWNT。這個製程是與目前的積體電路製程相容，可以同時製造許多 CNT-FET。藉由控制**成長時間**、**還原時間**與**溫度**，我們可以達到預期的成長效果。同時，經由覆蓋氮化矽的製程與否，我們可以得到 N 或是 P 型的 CNT-FET，日後可以構成似互補式金氧半場效電晶體(CMOS)的架構。

最後，我們展示了一個新的 CNT-FET 元件架構。經由兩個互相垂直且覆蓋

不同的介電層(inter layer dielectric, ILD)的奈米碳管，吾人可以得到一個 channel length(即是 bundle SWNT 的直徑)小於 50 奈米的 CNT-FET 元件。同時這兩根奈米碳管可以分別扮演 gate 與 channel 的角色，搭配不同的 passivation layer 製程(ILD)，我們可以得到 N 或是 P 型的 CNT-FET。這種特性可以增加日後 CNT-FET 電路的設計彈性，同時可以製造互補式的奈米碳管電晶體。

A Study on the Fabrication and Characteristics of Novel Carbon Nanotube Field-Effect Transistors

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Abstract

In this dissertation, we report the layout designs and the process recipe for fabricating carbon nanotube field effect transistors (CNT-FETs) and bio-sensors, including the definitions of cell blocks, characters of device structures in detail. For the purpose of aligned growth of carbon nanotubes, two kinds of layouts for catalyst islands are also designed for catalytic chemical vapor deposition (CCVD) method.

To start with, we propose a conduction-type-tunable CNT-FETs with double-gated structure (DG CNT-FET). A specially designed narrow top-gate is created to modulate the energy band in the middle region of a single CNT. In the proposed DG device structure, the top-gate and bottom-gate biases exhibit independent modulation behaviors. Energy band diagram conducive to the physical mechanisms of the proposed DG CNT-FET device structure is proposed. Based on the proposed hypothesis, ambipolar CNT-FETs can indeed be converted to n- or p-type-like behaviors.

Next, we also demonstrate a novel plasma treatment method that allows us to convert metallic-type carbon nanotubes to semiconducting-type CNT-FETs. This is important as the production of single-walled carbon nanotubes (SWNTs), irrespective of synthesis methods, still yields a mixture of both types thus far, with the metallic type being prevalent. However, semiconducting-type SWNTs are needed for CNT-FETs as well as many sensors. Judging from our experimental results, we believe that the ion bombardment during plasma treatment attacks both metallic- and semiconducting-type nanotubes; however, the metallic-type carbon nanotubes are more vulnerable to the attack than the semiconducting-type, and are subsequently transformed into the latter type.

In order to apply CNTs to nanoelectronics, in this thesis we also demonstrate a precise growth of SWNTs on pre-assigned locations with only cobalt (Co) as catalyst. This is in contrast to the laborious and time-consuming physical manipulation of numerous nanotubes one at a time used in the conventional approach. Laterally-grown carbon nanotubes are accomplished in pre-assigned areas using an integrated-circuit (IC)-compatible process in this thesis. In order to synthesize SWNT to serve as the channel of a FET, the cobalt-mix-tetraethoxysilane (CMT) solution and catalytic chemical vapor deposition are used. Our results show that laterally-grown bundled-CNTs could be formed in CCVD with ethanol, by properly controlling the

temperature of process, the process time, and the hydrogen reduction time. The use of pre-patterned catalyst islands, CCVD method and flexibility of silmutaneously manufacturing both n- and p-type CNT-FETs may open a new era for applications of CNT-based nanoelectronics.

Finally, we introduce a complementary carbon-nanotube(CNT)-gated CNT thin-film field effect transistor. By using two perpendicularly-crossed SWNT bundles as the gate and the channel interchangeably, a sub-50 nm complementary CNT-FET is demonstrated. It is found that the new CNT-FET shows acceptable FET characteristics by interchanging the roles of the gate and the channel. The unique dual-functionality of the device will open up a new possibility and flexibility in the design of future complementary CNT electronic circuits.

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六年前，自己處於工研院低溫複晶矽 TFT-LCD 計劃如火如荼執行多年，且國防役身份也屆滿兩年的情況下，面臨是否要到業界發展的抉擇。在 吳恩柏副所長的鼓勵下，個人毅然選擇申請並通過工業技術研究院的在職進修甄選，也承蒙 徐爵民副院長、 邱華樑副所長與 胡其俊廠長，以及國立成功大學 鄭國順教授、 許渭州教授、 方炎坤教授與本校電子所 黃遠東教授等師長的全力奧援下，使我得以排除萬難，順利考取國立交通大學電子工程所博士班並且就讀迄今。

求學期間，我要特別感謝我的指導教授 黃調元博士。黃老師在半導體業界的資深經驗以及擁有 IEEE FELLOW 的桂冠，佐以上課時的旁徵博引與穿插歷史典故，真像是醍醐灌頂、使我茅塞頓開。同時黃老師也在我茫然失措時多所指點，令我點滴在心頭。尤其是黃老師身體雖微恙，但修改論文的速度與鞭辟入裏的剖析，真真使我拳拳服膺，佩服之至!

另一方面我也要感謝共同指導教授 趙天生博士。若不是趙老師在實驗資源上鼎力相助與對各篇論文的提綱挈領、耳提面命，只怕我現在還是惶惶不可終日。此外，趙老師提供了我許多半導體知識的正確觀念與想法，亦在我迷惘灰心時給我鼓勵與幫助，令我銘感五內。

謝謝兩位恩師多年來的耳提面命，諄諄善誘。若有機會，個人定當銜環結草，並且將這份精神用以提攜後進。

在工作與實驗上，我特別要向魏拯華博士致謝。這許多年來他給了我很多實驗上的建議，同時他對奈米碳管與半導體的瞭解，真的是我學習的榜樣。此外，更要謝謝蔡銘進組長與高明哲組長對於我工作與實驗資源上的協助。謝謝駱伯遠同仁這一段時間來的砥礪。當然，也謝謝王宏祥與賴明駿的協助與鼓勵。更謝謝實驗室中設備與生產線同仁---彭雲錦、呂俊霖、溫永宏、萬坤鴻、劉九如、李國瑞、黃惠瓊、彭惠甘、王美玲、胡素琴、陳惠珍、邱芹英等人的協助。同時感謝工研院化工所與趙老師提供我 CVD 機台來成長奈米碳管。我想，我一輩子都不會忘記那一段幾乎每天晚上熬夜做實驗，一直要到天亮才回到宿舍，小憩一下就必須去上班的日子。

歲月不饒人，自己的記憶力與理解力都大不如前。要不是有呂嘉裕、李明賢、林宏年、盧景森、蘇俊榮、賴大偉、李維、林柏青、林盈彰等實驗室成員，以及

葉冠麟、李耀仁、盧文泰等學長的相濡以沫，只怕個人無法順利通過博士班層層疊疊的大小考試、作業繳交與各種半導體實驗的淬鍊。謝謝大家，好哥兒們!

在知識的饗宴外，我也要謝謝陪我登山、玩飛行傘的朋友。否則，有時候我真的壓力會大到不知道生活的目的是什麼。也謝謝竹東家扶中心與交大愛盲有聲書的夥伴們，讓我知道什麼是『施比受更有福』。謝謝陳氏太極拳 董冠言老師的言教身教，也謝謝普親精舍的見桅師父與見曇師父，是您們的引領，讓我的心靈可以通過這一路來的驚濤駭浪，勉力不激起絲絲漣漪。

此外，我也要祝福與感謝清華大學的魏鴻文。祝福你儘速順利取得博士學位。

同時，我要特別感謝工研院影像顯示科技中心的 林治民組長在我最關鍵的撰寫論文階段大力相助，讓我牛步化的論文撰寫速度轉為無後顧之憂的積極快速。

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千言萬語，不足以表達我的謝意。僅以此論文，獻給我摯愛的家人。

若是人生可以重來，我仍然會做一樣的選擇。只因這一路上有您們。

再一次，將此論文獻給一路上幫助我、關心我的人。

謝謝交通大學，謝謝工研院，謝謝幫助我的親朋好友、師長、長官與同學們。

陳百宏

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Content

Chapter 3

A Carbon Nanotube Field Effect Transistor with Tunable Conduction-Type by Electrostatic Effects

Chapter 4

A Novel Method of Converting Metallic-Type Carbon Nanotubes to Semiconducting-Type Carbon Nanotube Field-Effect Transistors

Chapter 5

Prospects of Cobalt-Mix-TEOS Method on Localized Lateral Growth of Carbon Nanotubes for Both P- and N-Type Field Effect Transistors

Chapter 6

Complementary Carbon Nanotube-Gated Carbon Nanotube Thin-Film Transistor

Chapter 7

Conclusions and Suggestions for Future Work

Table Captions

Chapter 1

Chapter 2

Chapter 3

Chapter 4

Chapter 5

Chapter 6

Figure Captions

Chapter 1

Chapter 2

Chapter 3

Fig. 3.1 Conduction-Type-Tunable CNT-FETs. Figs. 1(a)- 1(d) depict key process steps for Type-I structure, while Fig. 3.1e shows the cross-sectional view for Type-II structure. (a) 100nm oxide or nitride was grown as the back-gate dielectric on p-type silicon wafer (0.02 Ω-cm), followed by Ti deposition/pattern/etch to serve as the source/drain metal. (b) SWNT was spun-on the wafer in proper solution concentration. (c) Top-gate dielectric layer was deposited by low temperature PE-CVD (PE-oxide or PE-nitride). (d) Second Ti layer was sputtered, patterned, and etched to serve as the top-gate. (e) Cross-sectional view of the new Type-II double-gated (DG) CNT-FET structure. The major differences between Type-I (Fig. 3.1d) and Type-II (Fig. 3.1e) lie in the separate bottom-gate design in Type-II structure and the different dielectric layers between the two types. (f) SEM picture with SWNT/DMF solution spun on a wafer.

Fig. 3.2 Transfer characteristics (drain current versus bottom-gate voltage) highlighting that generic ambipolar-type CNT-FET can be gradually converted to p-type CNT-FET by simply varying the top-gate bias at Vds = 1V.

Fig. 3.3 (a) Transfer characteristics (i.e., drain current versus bottom-gate voltage) with floating top-gate showing ambipolar behaviors. (b)Band diagram with floating top-gate and bottom-gate, only a few holes can drift through the interface Schottky barrier, corresponding to the region Ⅰ of (a). (c) Band diagram with floating top-gate and negative bottom-gate, the hole will flow easily through the interface Schottky barrier, corresponding to the region II of (a). (d) Band diagram with floating top-gate and positive bottom-gate,

the electron will tunnel easily through the interface Schottky barrier, corresponding to the region III of (a).

Fig. 3.4 By varying the top-gate voltage from positive to negative in the presence of positive bottom-gate voltage, the energy band within the CNT will be shifted as follows: (a) With positive top-gate, the electron flow will act as if no top-gate bias is applied. (Even if a large positive bias is applied to the top-gate, the down-bending potential profile will only slightly accelerate the electron flow in the CNT due to the barrier lowering effect, and the drain current will increase only slightly.) (b) With negative top-gate, the electron flow will be suppressed (red solid circle line in Fig. 3.4(c)), and the current level will drop effectively. (c) Transfer characteristics corresponding to Fig. 3.4(b).

Fig. 3.5 By varying the top-gate bias from negative to positive in the presence of negative bottom-gate voltage, the energy band within the CNT will be shifted as follows: (a) With negative top-gate bias, the hole current will act as if no top-gate bias is applied. (When the top-gate voltage is at a much more negative bias, the barrier lowering effect occurs at the drain side, and results in a significant increase of hole-tunneling) (b) With positive top-gate bias, the hole flow will be suppressed (red solid circle line in Fig. 3.5(c)), and the current level will drop effectively. (c) Transfer characteristics corresponding to Fig. 3.5(b).

Fig. 3.6 (a) According to the hypothesis proposed in Fig. 3.4, n-type behavior in Type-II CNT-FET can be fully suppressed by applying negative bias to the top-gate. In other word, the on/off ratio can be controlled at will. (b) A bloated view of Fig. 3.6a with bottom-gate varying between 0~5V. With

positive top-gate bias, the down-bending potential profile shown in Fig. 3.4a will slightly accelerate the electron flow due to the barrier lowering effect, and the drain current will increase slightly.

Fig. 3.7 According to the hypothesis proposed in Fig. 3.5, p-type behavior in Type-II CNT-FET can be fully suppressed by applying positive bias to the top-gate. This figure shows gradual conversion by simply varying the top-gate bias at Vds = 1V.

Fig. 3.8 The top-gate can be used to shift the Fermi-level of the entire CNT. This feature can be utilized to adjust Vth of DG CNT-FETs precisely.

Chapter 4

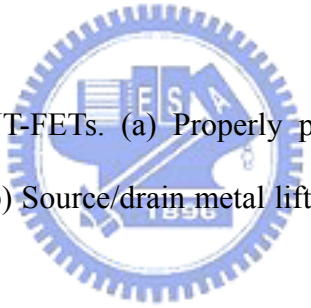


Fig. 4.1 Process flow of CNT-FETs. (a) Properly prepared SWNT/DMF solution spun on the wafer, (b) Source/drain metal lift-off process, and (c) Ar plasma treatment.

Fig. 4.2 Ids-Vds characteristics of (a) an as-grown metallic-CNTs, (b) after first Ar plasma treatment under 20 W/20 W/1 s conditions, (c) after second Ar plasma treatment under 20 W/20 W/1 s conditions, and (d) after third Ar plasma treatment. Insets show the corresponding transfer characteristics.

Fig. 4.3 Ids-Vds characteristics of (a) as-grown p-type semiconducting CNT-FETs, (b) after first Ar plasma treatment under 20 W/20 W/1 s conditions, (c) after second Ar plasma treatment under 20 W/20 W/1 s conditions, and (d) after third Ar plasma treatment. Insets show the corresponding transfer characteristics. Note that the as-grown p-type characteristics are preserved after plasma treatments.

Chapter 5

and (c) are pre-defined n^+-poly bottom gate electrodes.

Fig. 5.2 Process flow for the growth of bundled-CNTs. (a) Catalyst mixed TEOS (CMT) and pure TEOS layers were spun on oxidized substrate with patterned bottom gates, followed by photolithography and RIE processes to form CMT catalyst islands. (b) Growth of suspending SWNTs connecting two neighboring catalyst islands. (c) Ti metal lift-off process to form source/drain electrodes. The inset of Fig. 5.2(c) shows two kinds of catalyst islands and S/D metal pads in our layout design. Note that the individual bottom n^+-poly gate and the gate oxide or nitride layer were both formed before the CMT was spun.

Fig. 5.3 TEM pictures for CMT layer and bridged-CNT. (a) Cobalt nanoparticle uniformly embedded in oxide layer. (b) Bundled-SWNT synthesized from CMT powders with 10 nm in diameter. (c) Many bridged SWNTs are formed between the CMT catalyst islands.

Fig. 5.4 The adhesion of CMT layer on different layers. The vernier structure (i.e., the scale bars) indicates the resolution of photolithography and the finest pattern after dry etching. (a) CMT spun well on thermal oxide layer. (b) Poor adhesion of CMT layer on nitride. (c) By adding a hexamethyldisilazane (HMDS) layer before CMT spinning, good CMT catalyst islands are obtained on nitride layer suitable for bio-sensor purposes.

Fig. 5.5 SEM pictures of lateral-grown CNTs (a) Formed by dry etching. (b) Formed by wet etching. The bundled CNTs bridge the CMT layer from the catalyst. (c)-(d) The leakage current range without any post treatment by using dry etcher to form the catalyst islands. Note the leakage current is in the μA range because of the residues of Co particle/CMT layer, which can leave a

Chapter 6

Fig. 6.3 I_{ds}-V_{ds} curves of CG CNT-FET in the upright mode, showing typical *n*-type FET characteristics (i.e., the bottom CNT1 as the channel, and the top CNT2 as the gate).

Fig. 6.4 I_{ds}-V_{ds} curves of CG CNT-FET after interchanging the roles of the channel and the gate (i.e., the bottom CNT1 as the gate, and the top CNT2 as the channel). The upsidedown FET shows typical *p*-type FET characteristics.

Fig. 6.5 (a) The energy barrier around both source and drain electrodes is small. So even the top-gate (CNT1) is floating, the holes can tunnel through the small barrier after applying voltage between S/D electrodes. This is a "normally on" device. (b) With negative top-gate bias, the up-bending potential profile will slightly accelerate the hole flow due to the barrier lowering effect, and the drain current will increase slightly, as shown in Fig. 6.4. (c) With positive top-gate bias, the band diagram will block the hole flow, and the drain current will be suppressed (as shown in Fig. 6.4).

Chapter 1

Introduction

1.1 General Background

The carbon nanotube (CNT) is a hollow tube composed of carbon atoms with its diameter ranging from a few nanometers to tens of nanometers. CNTs have been extensively studied and analyzed since their discovery [1] in 1991 by Dr. Sumio Iijima of the NEC Fundamental Research Laboratory, as their excellent electrical and mechanical properties appear to be promising for many micro- and nanoelectronic applications, such as field-emission displays [2], sensors [3,4] and field-effect transistors (FET) [5]. The reason why the CNTs possess particular mechanical and thermal properties is strongly related to their structure. Colbert et al. indicates that these properties are closely related to the hexagonal array of graphene, which is the densest possible packing of atoms in two dimensions, together with the extraordinary strength of C-C sp^2 bonds [6]. The CNT is about 100 times stronger than steel, yet one-sixth the weight because of its hollow center and chicken-wire-like structure. As for thermal conduction, the CNT surpasses even that of diamond. All of the mechanical, thermal and electrical characteristics make the CNTs (both single- and multi-walled) become an attracting candidate for the future micro- and nano-electronics.

CNTs fall under the category of fullerenes, which in turn falls under the category of all carbonic substances. There are three major forms of carbon, i.e., graphite, diamond and fullerene.

First of all, graphite is composed of stacked sheets (i.e., graphene sheets) of carbon. Each graphene sheet is composed of hexagonally arranged carbon atoms and

the structure is analogous to honeycomb. Figure 1.1(a) shows three graphene sheets stacked together. It is worth noting that a piece of graphite can consist of millions of layers of stacked graphene sheets. Each dot in Figure 1.1 represents a carbon atom, and each line between two dots represents the covalent bond between two carbon atoms.

Second, Figure 1.1(b) shows the atomic structure of diamond. Diamond is a kind of ores that is hard and highly thermally conductive and the carbon atoms are arranged tetrahedrally.

Fullerene, the third form of carbon, exhibits hollow and cage-like structures. The Bucky ball is one of the well-known structures (Figure 1.1(c)). The soccer-ball-like sphere is constructed hexagonally or pentagonally by carbon atoms, and can range in diameter.

The CNT is basically a fullerene and is an extended Bucky ball (Figure 1.2). It can be viewed as a graphene sheet rolled up to form a seamless cylinder of variable length. In Figure 1.2 we can see that the CNT is capped by half of a Bucky ball at both ends. CNTs include both single-and multi-walled structures. Single-walled carbon nanotubes (SWNTs) comprise just only one cylindrical graphite sheet. Their diameters are typically ~1nm. The multi-walled nanotubes (MWNTs) comprise several to tens of concentric cylinders, and the space between two successive graphitic shells is $3.4\,\mathring{A}$. Typically, the MWNTs tend to have diameters in the range 2-100nm.

Figure 1.3 shows the size distribution of the major carbonic substances. Theoretically, the smallest SWNT diameter is 0.4nm [7], and was demonstrated by Wang et al. in 2000 [8]. It is also noted that the length to width ratio (i.e., aspect ratio) of a CNT can be up to one thousand or even higher. This characteristic also prolongs

the application field of the CNTs.

There are three major methods to manufacture CNTs. They are laser ablation, arc-discharge and catalytic chemical vapor deposition (CCVD).

In laser ablation process, a graphite target loaded with a catalyst is positioned in a tube furnace and irradiated by a laser. This method can manufacture both SWNTs and MWNTs with high yield. The nanostructures are deposited at the cooler zone near the end of the furnace tube in the direction of the gas flow. The method has several advantages, such as high-quality SWNT production, diameter control and the investigation of growth dynamics.

In arc-discharge method, an arc discharge between two graphite rods is ignited and results in the consumption of one electrode, forming different carbon nanostructures that can be collected at different positions in the reactor chamber. SWNTs, MWNTs and fullerenes can be grown with different yields. Usually, a considerable amount of soot and carbon nanoparticles are also formed concurrently which must be removed by complex after-treatments. Large-scale synthesis of MWNTs by arc discharge has been achieved by using He-gas, and their thermal purification has also been successful. When a graphite rod with metal catalyst (Fe, Co, Ni, etc.) is used as the anode with a pure graphite cathode, SWNTs are generated in the form of soot. The crystallinity and perfection of arc-produced CNTs are generally high.

All kinds of carbon nanostructures (i.e., filaments) can be synthesized by applying catalytic chemical vapor deposition (CCVD) method. In this process, a furnace is loaded with a metal catalyst and fed with a carbon-containing gas (carbon source). Then the CNTs are synthesized on the catalyst surfaces at moderate temperatures in the range of 600 to 1000°C (and different pressures).

In order to make good use of the promising material, CNTs have been intensively studied by many research groups in many different fields in the paste decade. Among them, we pay our attention to the electrical properties mainly in this dissertation.

Again, CNTs have several impressive properties, including ultrahigh mobility, high current density capacity, and a suitable on/off ratio for FET purposes [9]. Generally, CNTs depict two different types of electrical characteristics (i.e., metallic- or semiconducting-type), depending mainly on the CNTs' chirality. The word "chirality" refers to the angle in which the hexagonal network of the nanotube is formed with respect to the tube axis. Therefore, not only the length and diameter of the CNT can be varied, but also helicity of the hexagonal network.

For clarity, the CNTs discussed in the following sections are single-walled carbon nanotubes (SWNTs). SWNTs are made from a single graphene sheet (Figure 1.2). The SWNT consists of a single CNT, typically on the order of 1.4nm in diameter. Figure 1.4 shows a TEM picture of a SWNT. The two dark lines in the TEM picture correspond to two sides of the SWNT's wall.

Figure 1.5 illustrates the concept of chirality. The STM picture (Figure 1.5(a)) shows five CNTs with different chiralities for demonstration [10]. The dotted line (vector **T)** is drawn along each CNT axis. Then a vector, **H**, is drawn from the same starting point with **T**. It is worth noting that vector **H** is parallel to the rows of consecutive hexagons in the carbon atom network and the vector is chosen to be parallel to what are called nearest-neighbor (with respect to the tube axis) hexagon rows. The angle between vectors **T** and **H** is defined as **Φ**. The chiral angle (i.e., chirality), **θ**, is defined as:

$$\boldsymbol{\theta} = 30^\circ - \boldsymbol{\Phi}$$

Depending on **θ** value**, t**here are three types of chiralities. A CNT with 30˚chiral angle is categorized as armchair CNT. The CNT is called zigzag CNT (No.7 CNT in Figure 1.5(a)) if the chiral angle is zero (**Φ** = 30˚), while those with the chiral angles ranging from 0˚ to 30˚ are categorized as chiral CNTs. For examples, Number 10, 11 and 1 in Figure 1.5(a) are chiral CNTs with chiral angles of 23˚ (**Φ** = 7˚), 16˚ (**Φ** = 14˚) and 5˚ (**Φ** = 25˚) respectively. The electrical property of CNTs with different chiralities will be briefly described later.

After giving the definition of chiral angle, we must also define another parameter, the chiral vector, which can indicate the CNT structure. In other words, the chiral vector can represent the chiral angle and diameter of the CNT simultaneously. Basically, the chiral vector is a line that traces the CNT along its circumference from one carbon atom (i.e., the reference atom) back to itself. Imaginably, if a CNT is cut open along the tube axis and through the reference atom, the CNT can be spread out and become a graphene sheet (Figure 1.5(b)). The dotted lines at both left and right sides of the figure represent the cut made along the CNT. Although the chiral vector begins and ends on the same reference atom, the end is represented by position (11,7) in the graphene sheet. It is worth noting that the locations (0,0) and (11,7) coincide on the same reference atom when the graphene sheet is wrapped to form a cylinder.

Again, vector **H** is drawn parallel to the nearest neighboring row. Whereas the chiral vector is perpendicular to the tube axis, the armchair (dotted line) is perpendicular to the **H** vector (The row of large dots in Figure 1.5(b) indicates the nearest neighboring row of hexagons). The resulting rolled-up carbon nanotube would be an armchair CNT, if the chiral vector lines up with the armchair line. In other words, the armchair line bisects every hexagon it passes through.

The unit vectors, **a1** and **a2**, the unit vectors, both begin at one corner of a single

hexagon and end two corners away in the same hexagon. Since **a1** and **a2** each traverse one whole hexagon, the coordinates (*n*, *m*) represent atoms that are *n* and *m* hexagons away from the reference atom in the **a1** and **a2** directions respectively. The chiral vector is therefore represented as following:

$$\mathbf{C} = n\mathbf{a1} + m\mathbf{a2}$$

A CNT can be characterized by the notation (*n*,*m*) which refers to the chiral vector, where *n* and *m* are positive integers.

According to the chiral angle equation mentioned earlier, the angles **θ** and **Φ** always combine to form 30°. A (*n*,*n*) configuration will result in an armchair CNT, while (*n*,0) and (*0*,*m*) configurations will result in zigzag CNTs. Finally, the (*n*,*m*) indicates the chiral CNT when both n and m are non-zero integers and $\mathbf{n \neq m}$ [10].

After introducing the fundamental concepts of the CNTs, we will discuss the metallic and semiconducting conduction of CNTs with different chiralities.

It has been proved that metallic tubes have conductivities higher than copper and can carry a current density that meets or exceeds the best metals (Table 1.1). The excellent metallic behavior makes CNTs a potential candidates for nanoscale wires [11]. It is also worth noting that semiconducting tubes have mobilities and transconductances that meet or exceed the best semiconductors [12]. The following sections will discuss how to distinguish metallic CNTts from semiconducting CNTs by using the chiral vector mentioned earlier.

Table 1.1 and Table 1.2 show the armchair, zigzag, and chiral tubes and their corresponding electrical properties. The chirality and diameter of a CNT is extremely important because they determine the properties of the CNTs, especially the electrical characteristics [10]. In short, both the diameter and chirality determine whether the CNT will be metallic or semiconducting.

Armchair CNTs (i.e., chiral angle is 30°) have been demonstrated theoretically and experimentally to be metallic in conduction (Table 1.2). Similarly, zigzag and chiral tubes have been shown to be metallic- or semiconducting-type given the appropriate diameter. Jeroen W. G. Wildooer et al. indicates that the energy gap (E_g) is dependend on the diameter [10], that is, E_g is proportional to 1/diameter (i.e., $E_g = 1/diameter$).

For a given (n, m) nanotube, if $2n + m = 3q$ (where q is an integer), then the nanotube is metallic, otherwise the nanotube is semiconducting. Thus all armchair nanotubes ($n = m$) are metallic.

However, CNTs can consist of multiple layers of grapheme sheets concentrically, resulting in the well-known multi-walled carbon nanotubes (MWNTs). The diameter of the outermost tube in a MWNT ranges from 10-20nm typically. Figure 1.6 shows TEM pictures of three MWNTs with different quantities of tubes concentrically. The conductivity of each tube in a MWNT is different, just like the SWNT. In short, there is high possibility that both metallic and semiconducting-type nanotubes (layers) exist in the same MWNT.

Currently, both metallic- and semiconducting-type CNTs are produced simultaneously in the three CNT synthesis methods mentioned earlier. For further applications of CNTs in micro- or nano-electronics, it is crucial to be able to distinguish metallic-type CNTs from semiconducting-type CNTs. Some research groups has developed a technique successfully for sorting SWNTs by their electronic properties and diameters. They found out that a certain sequence of single-stranded DNA could be formed as a helical structure around individual SWNTs. The most important discovery was that the electrical characteristics of the DNA-CNT hybrid strongly depend on the diameter and chirality of SWNT strongly. Later, a technique

called anion exchange [13] was used to filter out the hybrids and the mixture of metallic and semiconducting type CNTs could be sorted out.

Collins et al. demonstrated a method [14] for selectively removing single carbon shells from multi-walled CNTs (MWNTs) stepwise and individually characterizing the different shells using the partial electrical breakdown of a MWNT at constant voltage stress. By choosing among the shells, Collins et al could convert a MWNT into either metallic or semiconducting conductor. This approach takes advantage of current-induced electrical breakdown to eliminate individual shells one at a time, and the outer shells are more likely to breakdown. However, the applied current needs to be controlled precisely, otherwise, both metallic and semiconducting CNTs would fail. Moreover, this method is time-consuming.

Balasubramanian et al. have disclosed a selective electrochemical approach to fabricate CNT-FETs [15]. They used electrochemistry for selective covalent modification of metallic CNTs, resulting in exclusive electrical transport through the unmodified semiconducting CNTs. The semiconducting CNTs were rendered nonconductive by application of an appropriate gate voltage prior to the electrochemical modification. The FETs fabricated in this manner display good hole mobilities and a ratio approaching 106 between the current in the ON and OFF state. However, this approach is problematic. For example, when there are much more metallic nano-tubes than semiconducting nano-tubes in the deposited CNT-based material, this electrochemical approach can only improve the electrical characteristics of the few semiconducting CNT-FETs and still fails to increase the percentage of semiconducting CNT-FETs. On the other hand, this approach requires the chip to be immersed in a chemical solution, which reduces the yield and throughput. Moreover, the phenyl group in the solution may react with semiconducting CNTs to form

covalent bonds and adversely affects the electrical characteristics of the chip, which makes it unsuitable for use in sensors.

Since CNTs exhibit two different types of electrical properties, they can be employed as FETs as well as interconnects/vias/contact holes. However, there are challenges that need to be tackled before their adoption to many practical applications, especially the process compatibility with the existing silicon-based semiconductor technologies, controlling the placement and manipulation of massive numbers of CNTs at precise locations, the chirality of the CNTs, and the manufacturing of both n- and p-type CNTs simultaneously on the same substrate. Among these challenges, an effective method must be developed for efficiently controlling the placement of massive numbers of CNTs because conventional silicon-based micro- or nanoelectronics often consist of millions or billions of devices.

Although IBM's research group has demonstrated the repositioning of a single CNT on particular surface successfully, it is obvious that this technique is limited to manipulate one CNT at a time. If an IC chip uses nanotubes as channel/active layer of FETs (semiconducting-type CNTs) or interconnect (metallic-type CNTs), millions or billions of nanotubes would require accurate placement over the chip. The physical manipulation of nanotubes one at a time is absolutely inefficient for current IC technology.

Efforts have been made by many research groups to overcome the manipulation issue. There are two major approachs to manufacture CNT-FETs in the past few years. One approach is to first create the source and drain electrodes throughout the wafer, and then disperse CNTs on the wafer. Undoubtedly, there exists a small probability for CNTs to bridge some of the electrodes to form functional CNT-FETs. The drawback is the yield is quite low and impractical [16].

Another popular technique is to spread large quantities of CNTs on a wafer. Then EM and STM are applied to find the location of CNTs with desired chirality and dimensions. Electrodes can then be deposited on top of the CNT with the desired properties by e-beam lithography and lift-off method. It goes without saying that the yield of this technique is also very low [17].

It is obvious that the physical manipulation of numerous CNTs or spreading CNTs randomly one at a time is laborious and impractical for mass production, thus the ability to form massive numbers of CNTs in precise locations remains a key issue for CNTs in nanotechnology applications.

In order to overcome the manipulation problem, a number of techniques have been proposed to achieve a regular CNT network by controlling the gas flow direction [18], using porous templates [19], using electric-field-assisted assembly [20,21], utilizing chemically functionalized template [22], adopting fluidic alignment [23,24], or using electric-field-directed-growth of CNTs [25]. Although these methods all achieve acceptable results in both the growth direction and the length of CNTs, they require additional equipments [26]. It is obvious that the aligned-CNT-growth methods [27] are more promising than post-growth-assembly-of-CNT methods for CNT-FETs mentioned above. One of the aligned-CNT-growth methods, which has emerged as the most popular method, involves the catalytic disproportionation of carbon source (carbon monoxide usually) on bimetallic catalysts containing molybdenum/cobalt in chemical vapor deposition (CVD) system [28].

Although catalytic mixtures of cobalt (Co) and molybdenum (Mo) have been considered essential for the growth of single-walled carbon nanotubes (SWNTs) from carbon monoxide (CO) or hydrocarbons by the CVD method, we demonstrate the growth of bundled-CNTs with only Co particles as catalyst [29,30] and ethanol as

carbon source in this dissertation. Some previous reports also indicated that CNTs manufactured by CVD methods with Co catalyst usually resulted in predominantly multi-walled tubes [31,32]. In this thesis, our reiterative and systematic experiments show that the selective growth of bundled-CNTs produces mostly SWNTs.

For CNT-FETs and biosensors, it is necessary to employ single-walled carbon nanotubes (SWNTs) instead of multi-walled carbon nanotubes (MWNTs) because of the unique semiconducting property of the SWNTs. In order to obtain SWNTs, the catalyst size should be reduced to as small as possible [29]. In this dissertation, a method is proposed to synthesize SWNTs and form bridged-CNTs between two catalyst islands. The dominant parameters in the aligned growth of SWNTs are found to be the size and the location of catalyst nanoparticles. The characteristics of embedded Co nanoparticles in patterned cobalt-mix-tetraethoxysilane (CMT) islands for SWNT growth are discussed under different hydrogen reduction conditions, catalyst concentrations, and carbon ratios during CNT growth.

Since for the mainstream complementary metal oxide semiconductor (CMOS) circuit applications, both p- and n-type metal-oxide-semiconductor field effect transistors (MOSFET) are called for simultaneously on the same chip. It is thus necessary to fabricate n-type, in addition to p-type CNT-FETs, on the same chip for the complementary circuits. In general, the CNT-FET acts like a p-type conduction device when the CNT is exposed to air [33-37]. However, it is quite difficult to manufacture n-type CNT-FETs. Several approaches have been previously reported to form n-type CNT-FETs by employing complex doping processes (i.e., adopting alkali metals) [38-41] or thermal/electrical annealing processes [41]. These approaches, however, require extra processing and masking steps to convert generic p-type CNT-FETs in vacuum or in the inert gas. In contrast, no extra annealing steps are

needed to form air-stable n-type CNT-FETs [42-44] using the passivation method proposed in this dissertation

In conclusion, we will demonstrate that CNT is an appropriate material for FET applications. We will show the result of manufacturing both air-stable p- and n-type CNTFETs for CMOS without any complex ion doping process. Research for enhancing the CNTFET electrical properties and practicality is still on-going, and has made some progress.

1.2 Organization of the Dissertation

This dissertation is divided into seven chapters

In Chapter 2, we report the layout designs for carbon nanotube field effect transistors (CNT-FETs) and bio-sensors, including the definitions of cell blocks, feature size of device structures in detail. For the purpose of aligned growth of carbon nanotubes, we also design two kinds of layouts to form catalyst islands for CCVD method described in section 1.1.

In Chapter 3, we report a conduction-type-tunable CNT-FETs with double-gated structure (DG CNT-FET). In this chapter, a specially designed narrow top-gate is created to modulate the energy band in the middle region of a single CNT. In the proposed DG device structure, the top-gate and bottom-gate biases exhibit independent modulation behaviors. Depending on whether a positive or negative bias is applied to the top-gate, the CNT-FET can be operated in either n- or p-type conduction. Energy band diagram conducive to the physical mechanisms of the proposed DG CNT-FET device structure is proposed. Based on the proposed

hypothesis, ambipolar CNT-FETs can indeed be converted to n- or p-type-like behaviors.

In Chapter 4, we demonstrate for the first time a novel plasma treatment method that allows us to convert metallic-type carbon nanotubes to semiconducting-type CNT-FETs. This is important as the conventional production of SWNTs, irrespective of synthesis methods, still yields a mixture of both types, with the metallic type being prevalent. However, semiconducting-type SWNTs are needed for carbon nanotube field-effect transistors (CNT-FETs) as well as many sensors. This is because only the semiconducting-type SWNTs can be effectively modulated by the gate voltage. In contrast, the lack of field effect in metallic-type SWNTs adversely impacts their applications in high-performance electronic devices. Judging from our experimental results, we believe that the ion bombardment during Ar plasma treatment attacks both metallic- and semiconducting-type nanotubes; however, the metallic-type carbon nanotubes are more vulnerable to the attack than those of the semiconducting type, and are subsequently transformed into the latter type.

In Chapter 5, we demonstrate a precise growth of single-walled carbon nanotubes (SWNT) on pre-assigned locations with only cobalt (Co) as catalyst in order to apply CNTs to nanoelectronics. This is in contrast to the laborious and time-consuming physical manipulation of numerous nanotubes one at a time used in the conventional approach. Laterally-grown carbon nanotubes (CNTs) were accomplished in pre-assigned areas using an integrated circuit (IC) compatible process in this chapter. In order to synthesize SWNT as the channel of a field effect transistor (FET), the cobalt-mix-tetraethoxysilane (CMT) solution and catalytic chemical vapor deposition (CCVD) were used. Our results show that laterally-grown bundled-CNTs could be formed in atmospheric chemical vapor deposition (APCVD)

with ethanol, by properly controlling the temperature of process, the process time, and the hydrogen reduction time. The use of pre-patterned catalyst islands, CVD method and flexibility of simultaneously manufacturing both n- and p-type CNT-FETs may open a new era for applications of CNT-based nanoelectronics.

In Chapter 6, we introduce a complementary carbon nanotube (CNT)-gated CNT thin-film field effect transistor (FET). By using two perpendicularly-crossed single-wall CNT (SWNT) bundles as the gate and the channel interchangeably, a sub-50 nm complementary CNT-FET is demonstrated. It is found that the new CNT-FET shows acceptable FET characteristics by interchanging the roles of the gate and the channel. The unique dual-functionality of the device will open up a new possibility and flexibility in the design of future complementary CNT electronic circuits.

Finally, a summary of the results in this dissertation and suggestions for future work are given in Chapter 7.

References

[1] S. Iijima, ”Helical microtubules of graphitic carbon,” *Nature*, Vol. **354**, pp.56-58, Nov. 1991.

[2] W. B. Choi, D. S. Chung, J. H. Kang, H. Y. Kim, Y. W. Jin, I. T. Han, Y. H. Lee, J. E. Jung, N. S. Lee, G. S. Park, and J. M. Kim, “Fully sealed, high-brightness carbon-nanotube field-emission display,” *Appl. Phys. Lett*,,. Vol. **75**, Issue: 20, pp.3129-3131, November , 1999.

[3] K. A. Williams, P. T. M. Veenhuizen, B. G. de la Torre, R. Eritja, C. Dekker, “Nanotechnology: Carbon nanotubes with DNA recognition,” *Nature*, Vol. **420,** Issue: 6917, p.761, Dec. 2002.

[4] A. J. Storm, J. van Noort, S. de Vries, and C. Dekker, ”Insulating behavior for DNA molecules between nanoelectrodes at the 100 nm length scale,” *Appl. Phys. Lett.*, Volume **79**, Issue: 23, pp.3881-3883, December, 2001.

[5] R. Martel, T. Schmidt, H. R. Shea, T. Hertel, and Ph. Avouris, “Single- and multi-wall carbon nanotube field-effect transistors,” *Appl. Phys. Lett.*, Vol. **73**, Issue: 17, pp.2447-2449, October, 1998.

[6] D. T. Colbert and R. Smalley, “Past, present and future of fullerene nanotubes: Buckytubes,” In: *Perspectives of Fullerene Nanotechnology*, edited by Eiji Osawa, Kluwer Academic Publishers, 2002.

[7] L. C. Qin, X. Zhao, K. Hirahara, Y. Miyamoto, Y. Ando, S. Iijima, “The smallest carbon nanotube,” *Nature*, Vol. **408**, Issue: 6808, p.50, November, 2000.

[8] N. Wang, Z. K. Tang, G. D. Li, J. S. Chen, “ Single-walled 4 $\mathring{A}$ carbon nanotube arrays,” *Nature*, Vol. **408**, Issue: 6808, pp.50-51, November, 2000.

[9] B. Q. Wei, R. Vajtai, and P. M. Ajayan, “Reliability and current carrying capacity of carbon nanotubes,” *Appl. Phys. Lett.*, Vol. **79**, Issue: 8, pp.1172-1174, August, 2001.

[10] J. W. G. Wildooer, L. C. Venema, A. G. Rinzler, R. E. Smalley and C. Dekker, “Electronic structure of atomically resolved carbon nanotubes,**”** *Nature*, Vol. **391**, Issue: 6662, pp.59-62, January, 1998.

[11] J. Appenzeller, R. Martel, V. Derycke, M. Radosavljevic, S. Wind, D. Neumayer, Ph. Avouris, “Carbon nanotubes as potential building blocks for future nanoelectronics,” *Microelectronic Engineering*, Vol. **64**, Issue: 1-4, pp.391-397, October, 2002.

[12] P. L. McEuen, M. S. Fuhrer, and H. Park, “Single-walled carbon nanotube Electronics,” *IEEE Transactions on Nanotechnology*, Vol. **1**, No. 1, pp.78-85, March, 2002.

[13] M. Zheng, A. Jagota, M. S. Strano, A. P. Santos, P. Barone, S. G. Chou, B. A.

Diner, M. S. Dresselhaus, R. S. Mclean, C. B. Onoa, C. C. Samsonidze,.E. D. Semke, M. Usrey, D. J. Walls, “Structure-based carbon nanotube sorting by sequence-dependent DNA assembly,” *Science*, Vol. **302**, Issue: 5650, pp.1545-1548, November, 2003..

[14] P. G. Collins, M. S. Arnold, P. Avouris, “Engineering carbon nanotubes and nanotube circuits using electrical breakdown,” *Science*, Vol. **292**, Issue: 5517, p.706, April, 2001.

[15] K. Balasubramanian, R. Sordan, M. Burghard, and K. Kern, “A selective electrochemical approach to carbon nanotube field-effect transistors,” *Nano Letters*, Vol. **4**, No. 5, pp.827-830, April, 2004.

[16] W. Hoenlein, F. Kreupl, G. S. Duesberg, A. P. Graham, M. Liebau, R. Seidel, E. Unger, “Integration of carbon nanotubes devices into microelectronics,” *Mat. Res. Soc. Symp. Proc.*, Vol. **772**, pp. M4.5.1-4.5.13, 2003.

[17] Ph. Avouris, T. Hertel, R. Martel, T. Schmidt, H. R. Shea, and R. E. Walkup, “Carbon nanotubes: nanomechanics, manipulation and electronic devices,” *Applied Surface Science*, Vol. **141**, No.3-4, pp.201-209, July, 1999.

[18] S. Huang, X. Cai, C. Du, and J. Liu, “Oriented long single walled carbon nanotubes on substrates from floating catalysts,” *J. Phys. Chem. B*, Vol. **107**, No. 48, pp.13251-4, December, 2003.

[19] S. Fan, M. G. Chapline, N. R. Franklin, T. W. Tombler, A. M. Cassell, and H. Dai, "Self-oriented regular arrays of carbon nanotubes and their field emission properties," *Science,* Vol. **283**, Issue: 5401, p.512, January, 1999.

[20] P. A. Smith, C. D. Nordquist, T. N. Jackson, T. S. Mayer, B. R. Martin, J. Mbindyo, and T. E. Mallouk, "Electric-field assisted assembly and alignment of metallic nanowires," *Appl. Phys. Lett.,* Vol. **77**, Issue: 9, pp.1399-1401, August, 2000.

[21] K. Yamamoto, S. Akita, and Y. Nakayama, "Orientation and purification of carbon nanotubes using ac electrophoresis," *J. Phys. D: Appl. Phys.,* Vol. **31,** No. 8, pp. L34-L36, April 1998.

[22] J. Liu, M. J. Casavant, M. Cox, D. A. Walters, P. Boul, W. Lu, A. J. Rimberg, K. A. Smith, D. T. Colbert, and R. E. Smalley, "Controlled deposition of individual single-walled carbon nanotubes on chemically functionalized templates," *Chemical Physics Letters*, Vol. **303**, Issue: 1-2, pp.125-129, April, 1999.

[23] Y. Huang, X. Duan, Q. Wei, Lieber, M. Charles, "Directed assembly of one-dimensional nanostructures into functional networks," *Science,* Vol. **291**, Issue: 5504, p.630, January, 2001.

[24] Y. Huang, X. Duan, Y. Cui, L. J. Lauhon, K.-H. Kim, Lieber, M. Charles, "Logic gates and computation from assembled nanowire building blocks," *Science,* Vol.

294, Issue: 5545, p.1313, November, 2001.

[25] Y. Zhang, A. Chang, J. Cao, Q. Wang, W. Kim, Y. Li, N. Morris, E. Yenilmez, J. Kong, and H. Dai, "Electric-field-directed growth of aligned single-walled carbon nanotubes," *Appl. Phys. Lett.*, Vol. **79**, Issue: 19, pp.3155-3157, November, 2001.

[26] K. H. Lee, J. M. Cho, and W. Sigmund, "Control of growth orientation for carbon nanotubes," *Appl. Phys. Lett.*, Vol. **82**, Issue: 3, pp.448-450, January, 2003.

[27] B.-H. Chen, P.-Y. Lo, J.-H. Wei, M.-J. Tsai, C.-L. Hwang, T.-S. Chao, H.-C. Lin, and T.-Y. Huang, "Localized lateral growth of single-walled carbon nanotubes for field-effect transistors by a Cobalt-Mix-TEOS method," *Electrochem. Solid-State Lett.*, Vol. **8**, Issue: 10, pp.G290-293, August, 2005.

[28] W. E. Alvarez, B. Kitiyanan, A. Borgna, and D. E. Resasco, "Synergism of Co and Mo in the catalytic production of single-wall carbon nanotubes by decomposition of CO," *Carbon*, Vol. **39**, Issue: 4, pp.547-558, June, 2001.

[29] A. Lan, Y. Zhang, X. Zhang, Z. Iqbal, H. Grebel, "Is molybdenum necessary for the growth of single-wall carbon nanotubes from CO? " *Chemical Physics Letters*, Vol. **379**, Issue: 5-6, pp.395-400, October, 2003.

[30] B. C. Satishkumar, A. Govindaraj, R. Sen, C.N.R. Rao, "Single-walled nanotubes by the pyrolysis of acetylene-organometallic mixtures," *Chemical Physics*

Letters, Vol. **293**, Issue: 1-2, pp.47-52, August, 1998.

[31] B. Kitiyanan, W. E. Alvarez, J.H. Harwell, and D. E. Resasco, "Controlled production of single-wall carbon nanotubes by catalytic decomposition of CO on bimetallic Co–Mo catalysts," *Chemical Physics Letters*, Vol. **317**, Issue: 3-5, pp.497-503, February , 2000.

[32] X. Z. Liao, A. Serquis, Q. X. Jia, D. E. Peterson, Y. T. Zhu , and H. F. Xu, "Effect of catalyst composition on carbon nanotube growth," *Appl. Phys. Lett.*, Vol. **82**, Issue: 16, pp.2694-2696, April, 2003.

[33] M. S. Dresselhaus, G. Dresselhaus, Ph. Avouris, *Carbon nanotubes: synthesis, structure, properties, and applications:* Springer-Verlag, Berlin, 2001.

[34] A. Bachtold, P. Hadley, T. Nakanishi C. Dekker**,** "Logic circuits with carbon nanotube transistors," *Science*, Vol. **294**, Issue: 5545, p.1317, November, 2001.

[35] S. J. Wind, J. Appenzeller, R. Martel, V. Derycke, Ph. Avouris, "Vertical scaling of carbon nanotube field-effect transistors using top gate electrodes," *Appl. Phys. Lett.*, Vol. **80**, Issue: 20, pp.3817-3819, May, 2002.

[36] J. Appenzeller, J. Knoch, V. Derycke, R. Martel, S. Wind, and Ph. Avouris, "Field-modulated carrier transport in carbon nanotube transistors," *Phys. Rev. Lett.*, Vol. **89**, Issue: 12-16, p.126801, September, 2002.

[37] A. Javey, Q. Wang, W. Kim, and H. Dai, "Advancements in complementary

carbon nanotube field-effect transistors," *IEDM Technol. Dig.,* pp.741-744, 2003.

[38] M. Bockrath, J. Hone, A. Zettl, P. L. McEuen, A. G. Rinzler and R. E. Smalley, "Chemical doping of individual semiconducting carbon-nanotube ropes," *Phys. Rev. B.*, Vol. **61,** Issue: 16, pp.R10606-8, April, 2000.

[39] C. Zhou, J. Kong, E. Yenilmez, H. Dai, "Modulated chemical doping of individual carbon nanotubes,**"** *Science,* Vol. **290**, No. 5496, pp.1552–1555, November, 2000.

[40] N. Bendiab, A. Righi, E. Anglaret, J. L. Sauvajol, L. Duclaux, F. Béguin, "Low-frequency Raman modes in Cs- and Rb-doped single wall carbon nanotubes," *Chemical Physics Letters*, Vol. **339**, Issue: 5-6, pp.305-310, May, 2001.

[41] V. Derycke, R. Martel, J. Appenzeller, Ph. Avouris, "Controlling doping and carrier injection in carbon nanotube transistors," *Appl. Phys.Lett.*, Vol. **80**, Issue: 15, pp.2773-2775, April, 2002.

[42] J.-H. Wei, H.-H. Wang, M.-J. Kao, "Method for fabricating n-type carbon nanotube device", U.S patent, Patent number: US6723624, Date of patent: 2004-04-20.

[43] D. Kaminishi, H. Ozaki, Y. Ohno, K. Maehashi, K. Inoue, K. Matsumoto, Y. Seri,

A. Masuda, and H. Matsumura, “Air-stable *n*-type carbon nanotube field-effect transistors with Si_3N_4 passivation films fabricated by catalytic chemical vapor deposition,**”** *Appl. Phys.Lett.*, Vol. **86,** p.113115, March, 2005.

[44] J.-H Wei, H.-H Wang, H.-H Chen, M.-J Lai, M.-J Kao, and M.-J Tsai, “A novel short-gate carbon nanotube thin film transistors,” *Proceedings of the IEEE-TSA*, pp.42-45, 2003.

[45] Peter J. F. Harris, *Carbon nanotubes and related structures: new materials for the twenty-first century*. Cambridge University Press, 1999.

[46] S. Frank, P. Poncharal, Z. L. Wang, and W. A. de. Heer, “Carbon nanotube quantum resistors,” *Science*, Vol. **280**, Issue: 5370, pp.1744-1746, June, 1998.

[47] Ph. Avouris, R. Martel, H. Ikeda1, M. Hersam, H. R. Shea, and A. Rochefort, “Electrical properties of carbon nanotubes: spectroscopy, localization and electrical breakdown,”

Source: http://nanostructures.phys.polymtl.ca/publications/book_2000.pdf

[48] C. Dekker, ”Carbon nanotubes as molecular quantum wires,” *Physics Today*, Vol. **52**, Issue: 5, pp.22-28, May, 1999.

Table 1.1 The major electrical properties of different chiralities' carbon nanotubes.

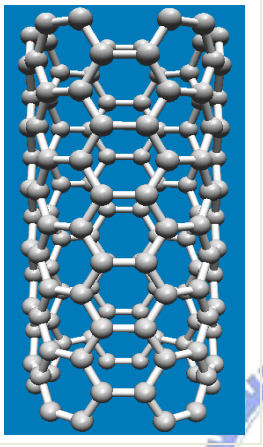
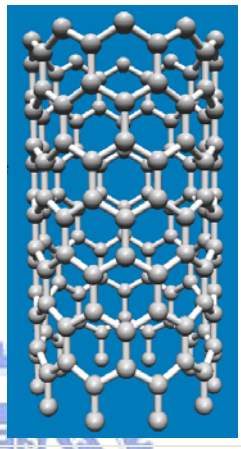
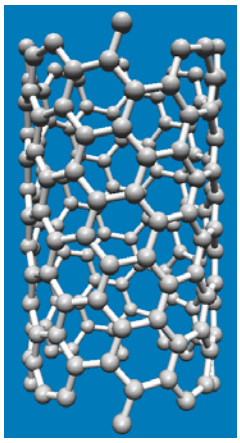
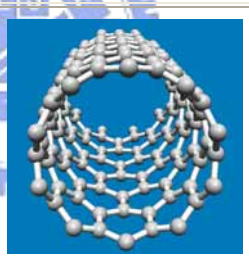
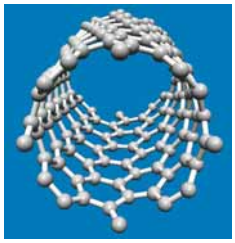
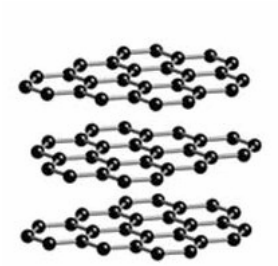
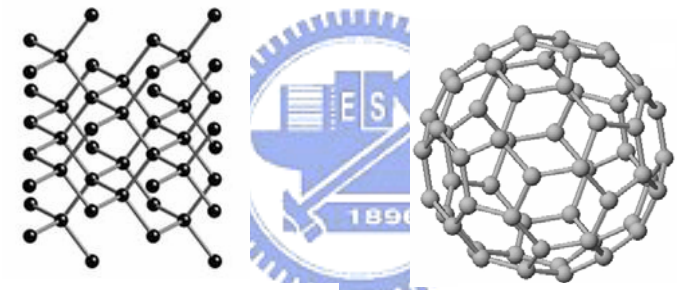
TYPE	**Armchair**	**Zig-zag**	**Chiral**
Chiral vector, (n,m)	(5, 5)	(10, 0)	(8, 4)
Side view			
View down tube			
Symmetry/asymmetry	Symmetry		Asymmetry
Electronic characteristic [45]	metallic	1/3 ： metallic (when n can be divided by 3) 2/3 ： semiconducting	1/3 ： metallic (when $2n + m = 3q$, q: integer); 2/3 ： semiconducting

Table 1.2 Comparsion between carbon nanotubes and other materials.

Physical properties	Nanotubes	Comparison
Dimension (diameter)	SWNT：0.4nm – few nanometers MWNT：less than 50 nm	Approximately 50,000 times smaller than the diameter of a human hair
Current density	10^7 A/cm^2 [46]~ 10^{13} A/cm^2 [47]	More than 1,000 times larger than metals such as silver and copper
Electrical characteristic	(*n*,*m*) nanotube, if $2n + m = 3q$ (*q:* integer), then the CNT is metallic, energy gap is 0 eV [48]. Otherwise the CNT is a semiconductor and the energy gap is less than 2 eV [10,32,48]. Note that all $n = m$ (armchair) are metallic (Table 1.1).	Ge : 0.67eV, Si：1.11 eV, GaAs：1.43 eV
Heat transmission characteristic	Predicted to be as high as 6,000 W/m·K (@ room temperature)	Nearly pure diamond transmits heat at 3,320 W/m·K
Field emission characteristic	CNT arrays can activate phosphors in less than 5 volts (if electrodes are spaced 1 um apart)	Conventionally, molybdenum tip requires electrical fields of 50 – 100 V/μm and have very limited lifetimes



(a) Graphite



(b) Diamond (c) Fullerene

Figure 1.1 Three major forms of carbon (a) graphite, (b) diamond, and (c) fullerene.

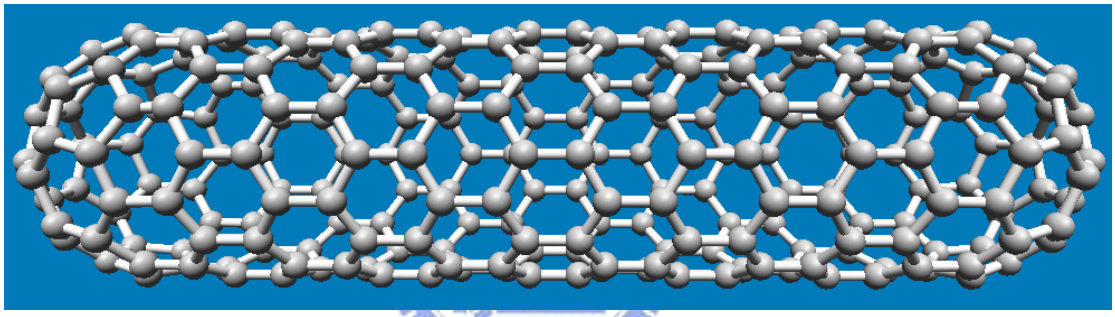


Figure 1.2 A (6,6) armchair single-walled carbon nanotube.

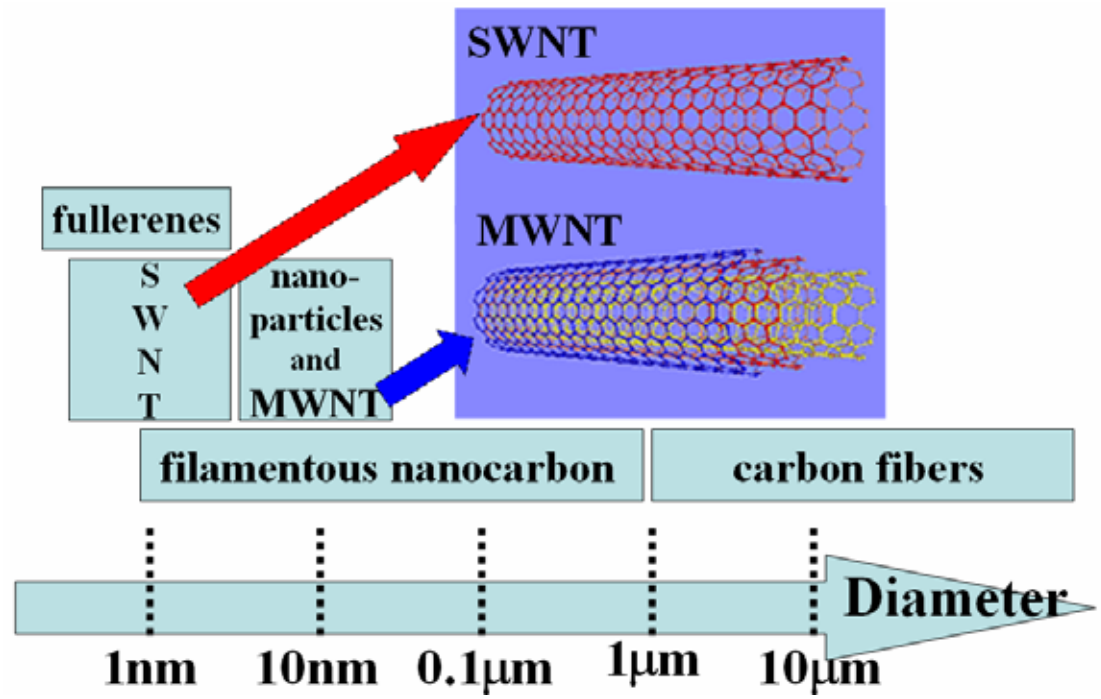


Figure 1.3 The size distribution of the major carbonic substances.

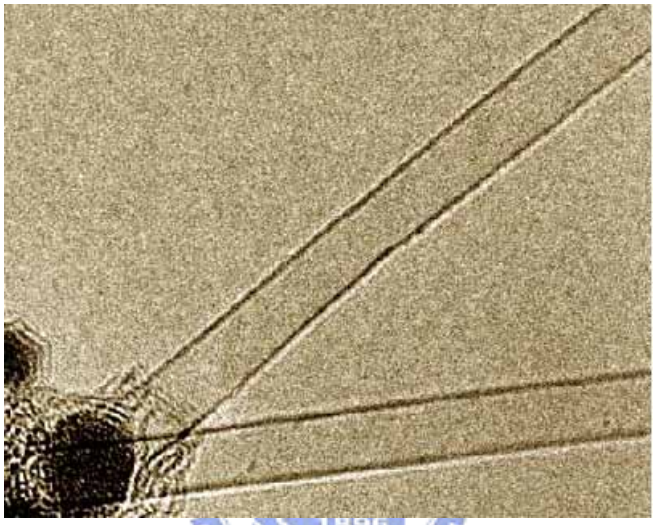
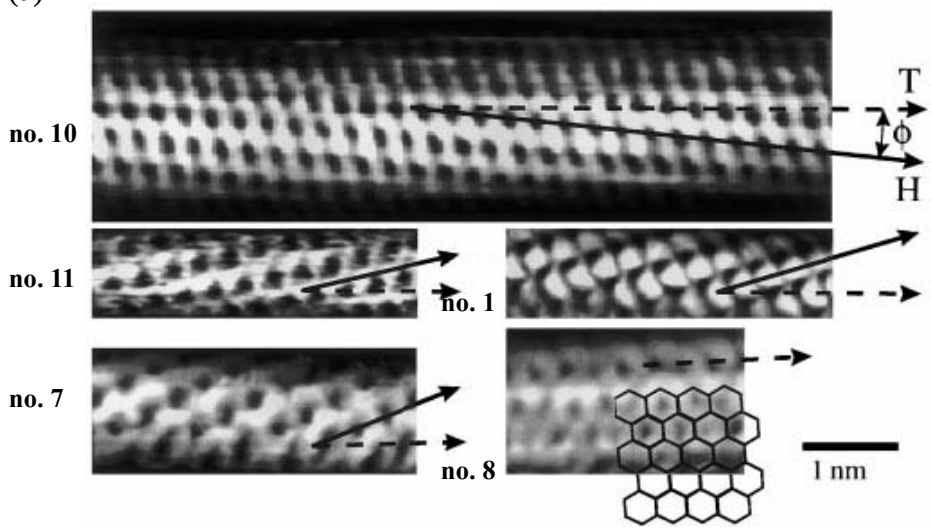


Figure 1.4　TEM picture of SWNTs.
(Source : http://members.cox.net/hongweizhu/bridge/p1.htm)

(a)



(b)

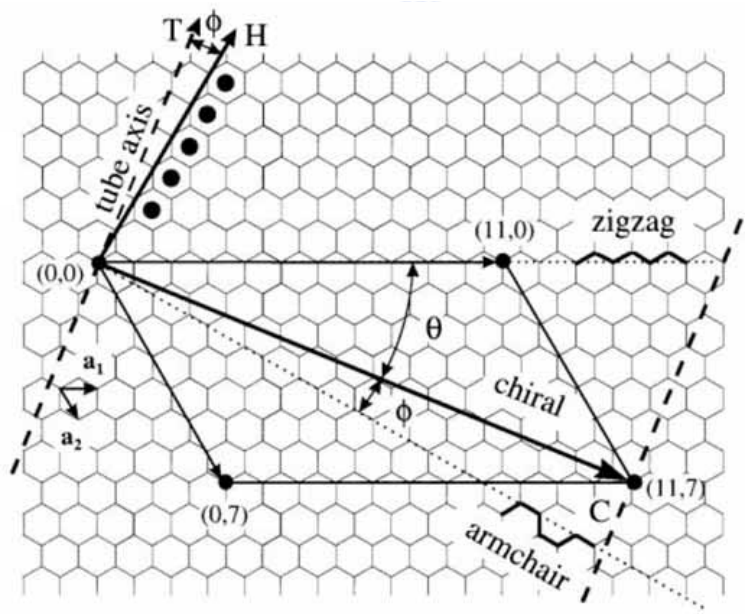


Figure 1.5 (a) Chiral angles. (b) Chiral vector for CNT characterization.

(from [10] J. W. G. Wildooer et. al., Nature, **391**, 1998)

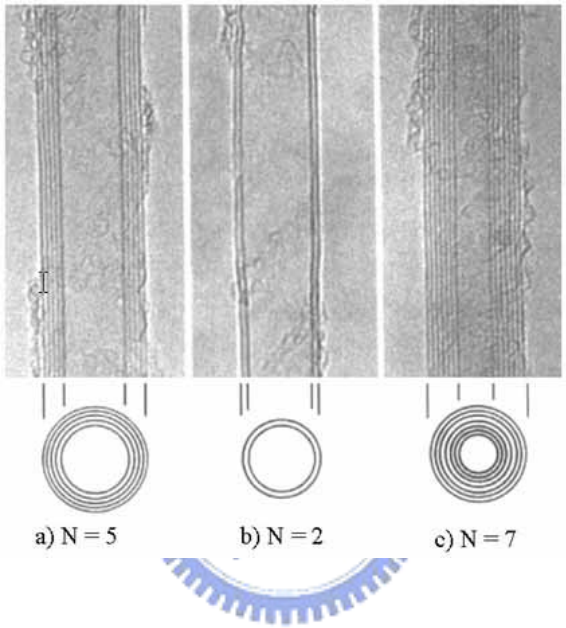


Figure 1.6 TEM pictures of MWNTs (“N” indicates the number of tubes) (from [33]; Dresselhaus, 2001)

Chapter 2

Overview of Photomask Design for Carbon Nanotube Field-Effect Transistors

2.1 Backgrounds and Motivation

In Chapter 1, we have stated that there are two major approaches to manufacture CNT-FETs. One approach is to first create the source and drain electrodes throughout the wafer, and then disperse CNTs on the wafer in hopes that there is a finite probability for CNTs to bridge some of the electrodes, thus forming the channel. The entire silicon substrate serves as the back-gate electrode in this approach. However, generally only a few p-type CNT-FETs are randomly formed on the wafer. It is obvious that the yield is impractically low. Besides, the CNT-FETs cannot operate independently because of the "universal back-gate" limitation.

The second approach is to first spread large quantities of CNTs on a wafer. TEM and STM can then be used to find the location of CNTs with desired chirality and dimensions. Electrodes can then be deposited on top of the CNT with the desired properties. The yield for this approach, however, is low as well and the same "universal back-gate" limitation is also applied in this approach.

To eliminate the above-shortcomings, a new set of photomasks (Figure 2.1) with the following features are designed and used in this thesis:

1. Bottom-gate mask: each CNT-FET has its own individually-controlled bottom-gate
2. Channel mask: CNT-FETs with different channel lengths/widths could be designed (Figure 2.2)
3. Top-gate mask (Figure 2.3): each CNT-FET has its own top-gate

4. Mask for consideration of bio-sensor implementation (Figure 2.5)
5. Mask to designate channel-type: Both p- and n-type CNT-FETs can be formed on the same chip
6. Catalyst island mask: for catalytic chemical vapor deposition (CCVD)

The new mask design features allows the fabrication of CNT-FETs which are free from the above-shortcomings, and suitable for practical applications.

2.2 Device Fabrication

The new mask set features a separate bottom-gate and allows the formation of CNT-FETs with different channel lengths/widths. Besides, both p- and n-type CNT-FETs for CMOS circuits can be manufactured simultaneously without resorting to any complex doping process. This is accomplished by designing a mask to selectively expose the CNT to the air or not. This is the key to manufacture the air-stable n-type CNT-FETs. N-type CNT-FETs can be obtained if the adsorption of oxygen in CNTs is blocked. This is because the major role of oxygen in the conductance of CNT-FET is to change the barrier level between the metal and CNT. Since oxygen is electron rich, it can depress electron transport and increase hole transport. So the CNT-FETs will become p-type if the channel is exposed to air [1-3]. The fabrication of n-type CNT-FETs and the electrical characteristics will be discussed in detail in Chapters 3, 4 and 6.

The purpose of the top-gate (Figure 2.3) is to modulate the conductance of CNTs by utilizing the electrostatic effects, as illustrated by the energy band diagram, which will be explained explicitly in Chapter 3.

Since it is obvious that the physical manipulation of numerous CNTs or the spreading of CNTs randomly one at a time is laborious and impractical for mass

production, the ability to form massive numbers of CNTs in precise locations remains a key challenge for CNTs in nanotechnology applications.

Efforts have been made by many research groups to overcome the manipulation issue. A case in point is that our group proposed the “spreading CNTs method” to manufacture CNT-FETs five years ago. Undoubtedly, there exists a small probability for CNTs to bridge some of the electrodes (i.e., source and drain) to form functional CNT-FETs. The drawback is the quite low yield.

In this dissertation, we propose a new method to synthesize SWNTs and form bridged-CNTs between two catalyst islands for CNT-FETs. Figure 2.4 shows the design of photomask. The patterned cobalt-mix-tetraethoxysilane (CMT) islands for SWNT growth will be discussed in Chapter 4 under different hydrogen reduction conditions, catalyst concentrations, and carbon ratios during CNT growth.

The development of bio-sensor devices is proposed for future work. In fact, the design for bio-sensor has been included in our photomasks, as shown in Figure 2.5. In addition, Figure 2.1 includes three blocks associated with bio sensor devices: device_BIO1, device_BIO2 and device_BIO3. All these cells are designed to perform bio-electronic or chemical-electronic testing by CNT-FET devices. Some preliminary results will be shown in Chapter 7.

Finally, we also design process monitor test keys (i.e., for process monitor purpose), as shown in Figure 2.6. The process monitor test keys will help confirm the etching conditions of contacts and pads, and avoid over-etching. It is also worth noting that there are several sets of CD bar and vernier for checking the resolution and shift of lithography (Figure 2.7).

2.3 Experimental Results and Summary

Table I illustrates the detail process of our CNT-FETs. We will discuss the electrical performance of several kinds of devices in the following chapters.

Figure 2.8 shows a CNT-FET by using the lift-off process. The electrical characteristics will be discussed in detail in Chapter 3 and Chapter 5.

References

[1] P. G. Collins, K. Bradley, M. Ishigami, and A. Zettl, "Extreme oxygen sensitivity of electronic properties of carbon nanotubes," *Science*, Vol. **287**, No. 5459, pp.1801-1804, March, 2000.

[2] V. Derycke, R. Martel, J. Appenzeller, Ph. Avouris, "Controlling doping and carrier injection in carbon nanotube transistors," *Appl. Phys.Lett.*, Vol. **80**, Issue 15, pp.2773-2775, April, 2002.

[3] D. Kaminishi, H. Ozaki, Y. Ohno, K. Maehashi, K. Inoue, K. Matsumoto, Y. Seri, A. Masuda, and H. Matsumura, "Air-stable *n*-type carbon nanotube field-effect transistors with Si_3N_4 passivation films fabricated by catalytic chemical vapor deposition,**"** *Appl. Phys.Lett.*, Vol. **86,** p.113115, March, 2005.

Table 1. Process flow of CNT-FET.

No	Stage Title	Step	Equipment	Recipe			Spec.
				Temp.	Condition	Time (min)	
	WF_START_0						
1	STARTING MATERIAL	* WAFER START					**CZ, P-type, <100>, 4" 15~25 ohm-cm**
2	WAFER MARK	* LASER MARK	Laser marker				
	ZR_PH_0		**Zero-layer etching**				
3	ZERO MASK	* SPIN	SVG coater		38A9 **photoresist**	4.6Krpm	
		* EXPOSE	I-Line Stepper		MASK #0 E=130 F=F*+0.7		8700 ±100A
		* DEVELOP	SOLITEC developer			28 sec	
	ZR_ETCH_0		**Zero-layer etching**				
4	ZERO ETCH	* ZERO ETCH	PR5000E-C	Dry etcher			
		Main etch			HBr 30sccm Cl_2 40 sccm 215W/ 60mT/ 75Gauss	[2]=22 +5 sec	1200 ±200A
5	PR Strip	* PLASMA	Mega 6 Dry etcher		O_2/CF_4	30:03	
		* RES. STRIP	Chemical station	110℃~ 130℃	H_2SO_4+ H_2O_2	30	
	FL_OX_0		**Field oxide deposition**				
6	FIELD OX.	* OXIDATION	F6-3 Furnace		G503	06:14:00	6000 ± 300A
	MT1_SPUT_0		**Metal 1 (for bottom gate) layer**				
7	METAL SPUT.	* PRE. METAL ETCH	DC3-6R chemical station	24~26℃	20:1BOE + DI water	3	
		*METAL 1 SPUT.	3190 metal sputter	275℃	Ti		3KA
8	Metal Gate MASK	* HMDS	VPU oven	250℃ /35℃			
		* SPIN	SVG coater		47B8 **photoresist**	4.6Krpm	17200 ±100A
		* EXPOSE	I-Line Stepper		**MASK**		

					CNT-130C E=160 F=F*+0.5		
		* DEVELOP	SOLITEC developer			28 sec	
9	Metal gate etch	* BAKE	oven	125℃		30	
		* METAL ETCH	TCP9600 Metal etcher		#6012		3KA
		Main Etch			Cl_2/Ar, **180W/220W** 10mT	[4]=70 sec By time	
		* PR Strip					
		PLASMA	Mega 6 Dry etcher		O_2	20:00	
		RES. STRIP	DC8-1 chemical station	110℃~ 130℃	H_2SO_4+ H_2O_2	30	
	LTO2_DEP_0		**Bottom gate dielectric layer (Nitride or oxide deposition)**				
10	Nitride dep. as gate dielectric	* Nitride DEP.	PR5000D PECVD	400℃	**SiH_4 120sccm/ NH_3 28 sccm/ N_2 2000 sccm**	20sec	2KA
			Bottom gate contact hole				
11	Gate pad Contact Mask	* HMDS	VPU oven	250℃ /35℃			
		* SPIN	SVG coater		38A9 **photoresist**	4.6Krpm	8700 ±100A
		* EXPOSE	I-Line Stepper		CNT-154C E=150 F=F*+0.5		
		* DEVELOP	SOLITEC developer			28 sec	
12	Gate pad Contact etch	* BAKE	oven	110℃		30	
		* PLASMA DESCUM	Mega 6 dry etcher		O_2	2	
		*Gate pad contact etch	PR5000E-B -Nitride-1	Dry etcher			2000A
	PL1_ETCH_0						
13	PR Strip	* PLASMA	Mega 6 dry etcher		O_2	30:00	
		* RES. STRIP	DC8-1 chemical station	110℃~ 130℃	H_2SO_4+ H_2O_2	30	

Step 14~22 stand for Localized Lateral Growth of SWNTs for CNT-FET method							
14	Catalyst Spray	*Spin catalyst	Spin coater			500rpm /10sec 4000rpm/30sec	
		*Soft bake	SOG hot plate	150℃		10	
		*Hot bake	Send to UCL/ITRI	550℃	CVD	60	
15	Catalyst layer Mask	* EXPOSE	I-Line Stepper		CNT-110D E=150 F=F*+0.5		
		* DEVELOP	SOLITEC developer			28 sec	
16	Catalyst Etch	Dry or wet etch	**See Chapter 4**				
17	PR Strip	* PLASMA	TCP9600 PLL chamber				
18	Tube Growth	*Send to UCL	**See Chapter 4**				
19	RemCa layer	* Nitride DEP.	PR5000D PECVD	400℃	**SiH_4 120sccm/ NH_3 28 sccm/ N_2 2000 sccm**	10sec	1KA
20	RemCa layer Mask	* HMDS	VPU oven	250℃ /35℃			
		* SPIN	SVG coater		38A9 **photoresist**	4.6Krpm	8700 ±100A
		* EXPOSE	I-Line Stepper		CNT-112D E=150 F=F*+0.5		
		* DEVELOP	SOLITEC developer			28 sec	
21	RemCa Layer Etch	* BAKE	SOG hot plate	125℃		30	
		* Dry or wet Etch	1KA nitride				
22	PR Strip	* RES. STRIP	DC8-1 chemical station	110℃~ 130℃	H_2SO_4+ H_2O_2	30	
	MT1_SPUT_0		**Source/Drain metal electrode**				
23	Metal 1 SPUT.	*METAL 1 SPUT.	3190 sputter	275℃	Ti		1KA

			3190		AlSiCu		4KA
	MT1_PH_0						
24	Metal 1 Mask	* HMDS	VPU oven	250℃ /35℃			
		* SPIN	SVG coater		47B8 **photoresist**	4.6Krpm	17200 ±100A
		* EXPOSE	I-Line Stepper		MASK CNT-160C E=160 F=F*+0.3		
		* Mark Clear					
		* DEVELOP	SOLITEC developer			32 sec	
	MT1_ETCH_0						
25	Metal 1 etch	* BAKE	oven	125℃		30	
		* METAL ETCH	TCP9600 Metal etcher		#1004		4KA AlSiCu
		Break Through			BCl_3/Ar 540W/180W 15mT	[2]=10 sec	
		Main Etch			Cl_2/BCl_3/N_2/ Ar, 500W/200W 10mT	[4]=20 sec ENDPOINT	
		Over Etch			Cl_2/Ar 180W/220W 10mT	[5]=100%	
		* METAL ETCH	TCP9600		#6012		1KA Ti
		Main Etch			Cl_2/Ar, 180W/220W 10mT	[4]=25 sec By time	
		* PR Strip					
		PLASMA	MEGA Dry etcher		O_2	20:00	
		RES. STRIP	DC8-1 chemical station	110℃~ 130℃	H_2SO_4+ H_2O_2	30	
	LTO2_DEP_0		**Top gate dielectric layer (Nitride or oxide deposition)**				
26	Nitride dep. as gate dielectric	* Nitride DEP.	PR5000D PECVD	400℃	**SiH_4 120sccm/ NH_3 28 sccm/**	20sec	2KA

					N_2 2000 sccm		
	MT2_SPUT_0		**Top gate metal**				
27	Metal 2 SPUT.	*METAL 2 SPUT.	3190 sputter	275℃	Ti		1KA
			3190		AlSiCu		4KA
	MT2_PH_0						
28	Metal 2 Mask	* HMDS	VPU oven	250℃ /35℃			
		* SPIN	SVG coater		47B8 **photoresist**	4.6Krpm	17200 ±100A
		* EXPOSE	I-Line Stepper		MASK CNT-180C E=160 F=F*+0.3		
		* DEVELOP	SOLITEC developer			32 sec	
	MT2_ETCH_0						
29	Metal 2 etch	* BAKE		125℃		30	
		* METAL ETCH	TCP9600 metal etcher		#1004		4KA AlSiCu
		Break Through			BCl_3/Ar 540W/180W 15mT	[2]=10 sec	
		Main Etch			Cl_2/BCl_3/N_2/ Ar, 500W/200W 10mT	[4]=20 sec ENDPOINT	
		Over Etch			Cl_2/Ar 180W/220W 10mT	[5]=100%	
		* METAL ETCH	TCP9600		#6012		1KA Ti
		Main Etch			Cl_2/Ar 180W/220W 10mT	[4]=25 sec By time	
30	PR Strip	* PLASMA	MEGA dry etcher		O2	20:00	
		* RES. STRIP	DC8-1 chemical station	110℃~ 130℃	H_2SO_4+ H_2O_2	30	

	PV_PH_0		**Source/drain contact holes**				
31	S/D pad Contact Mask	* HMDS	VPU oven	250℃~ 35℃			
		* SPIN	SVG coater		47B8	4.6Krpm	17200 ±100A
		* EXPOSE	I-Line Stepper		CNT-107D E=150 F=F*+0.1		
		* DEVELOP	SOLITEC developer			28 sec	
32	S/D pad Contact etch	* BAKE		125℃		30	
		* Gate pad contact etch	PR5000E-B -Nitride-1	Dry etcher			
		Main etch			CHF_3 60sccm+ O_2 35 sccm 550W	[2]=25 +5 sec	2000A
	PV_ETCH_0						
33	PR Strip	* PLASMA	MEGA dry etcher		O_2	20:00	
		* RES. STRIP	DC8-1 chemical station	110℃~ 130℃	H_2SO_4+ H_2O_2	30	
33	**WAFOUT**						
34	**Measurement**						

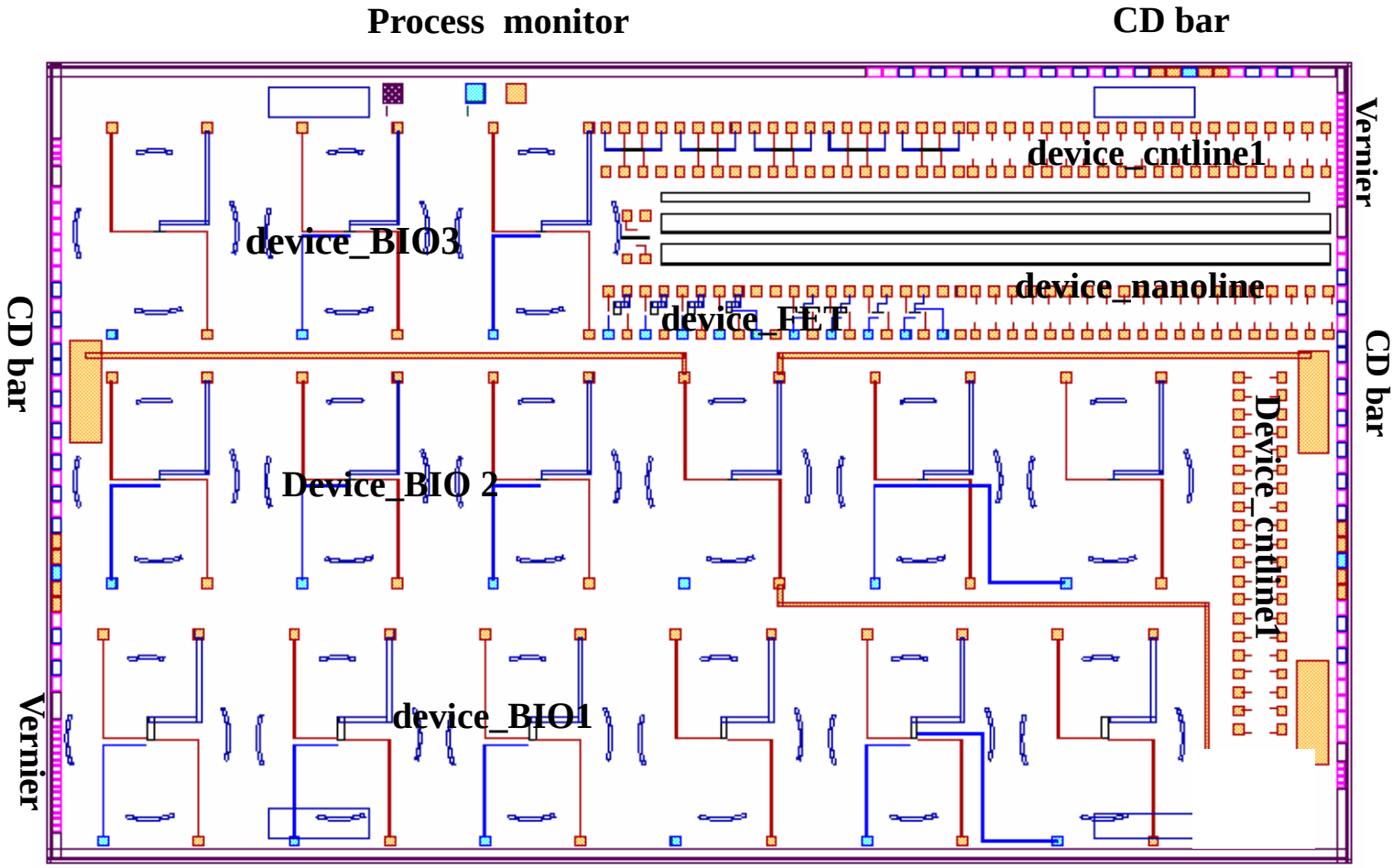


Figure 2.1 The overall layout of our photomask

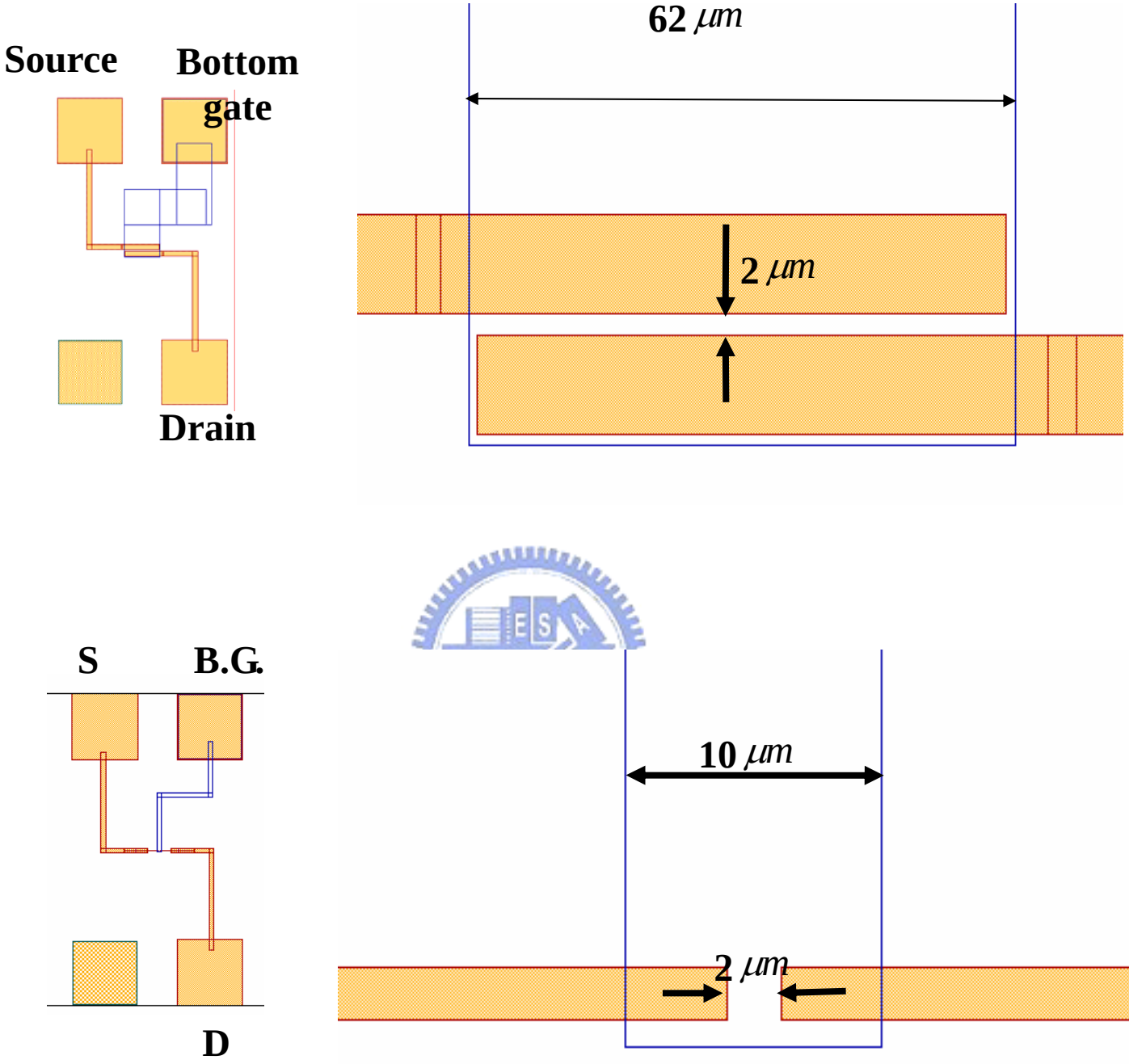


Figure 2.2 Two different Lengths/Widths layout of CNT-FETs

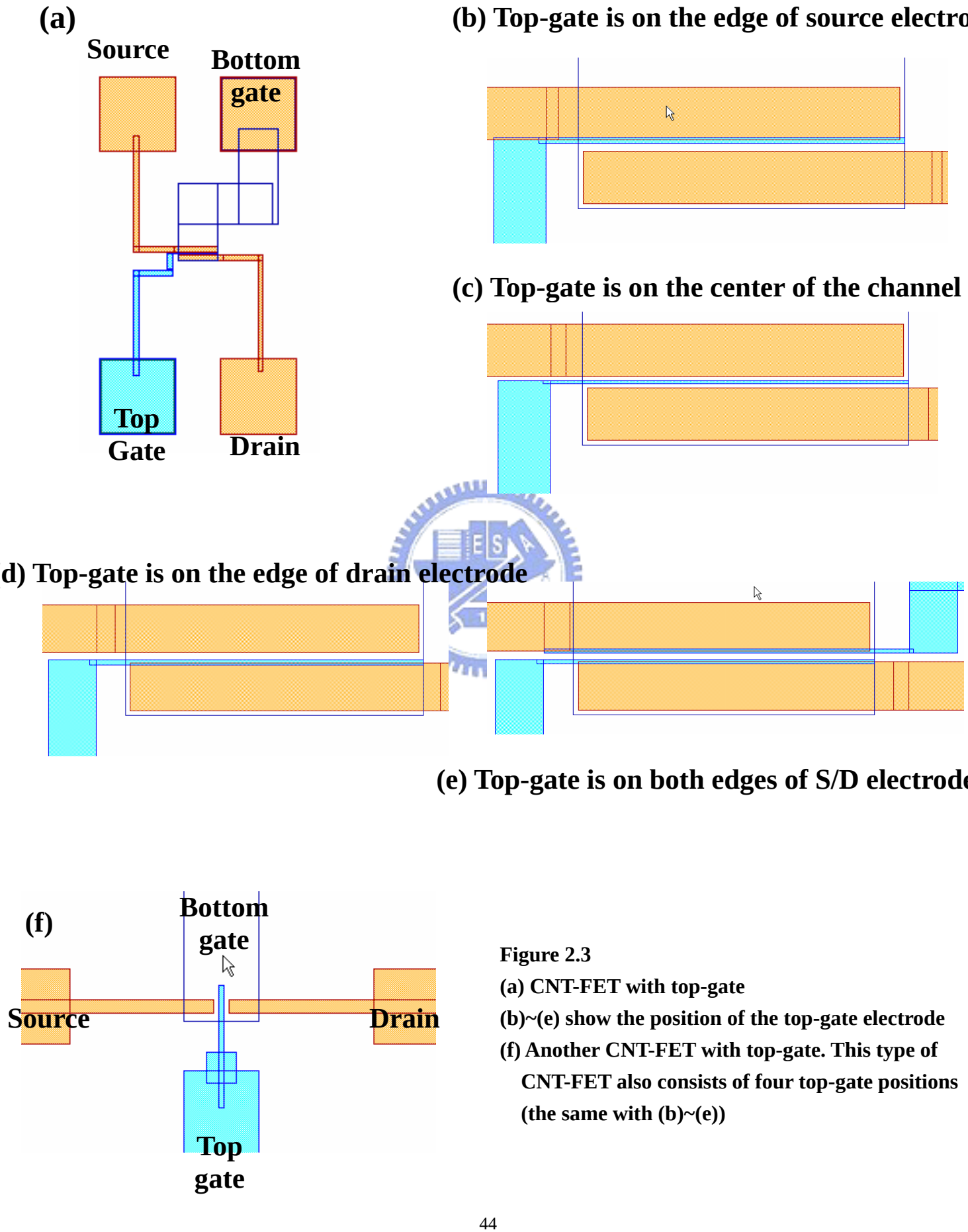


Figure 2.3
(a) CNT-FET with top-gate
(b)~(e) show the position of the top-gate electrode
(f) Another CNT-FET with top-gate. This type of CNT-FET also consists of four top-gate positions (the same with (b)~(e))

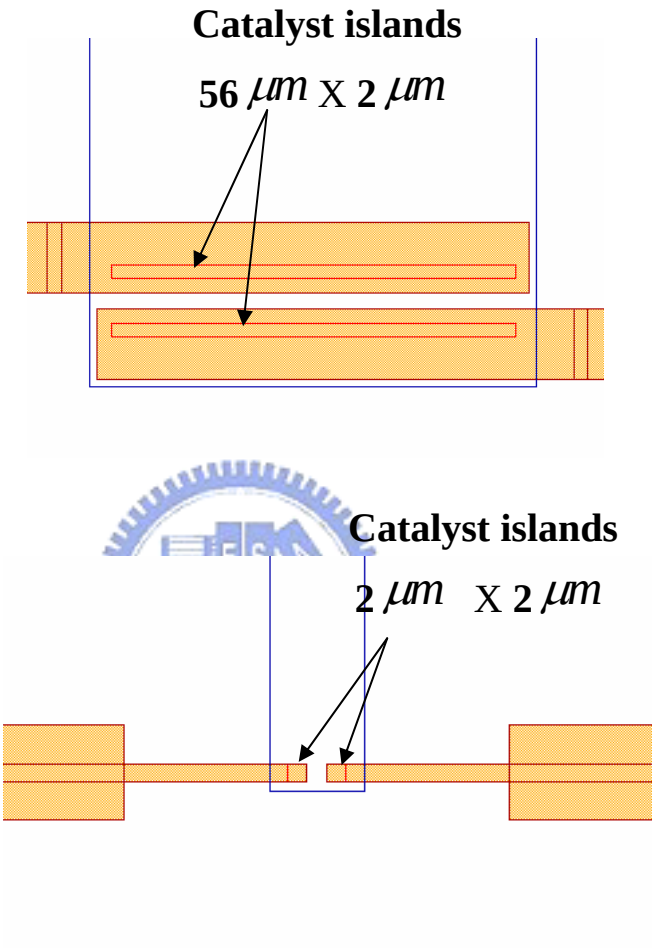


Figure 2.4 Two different catalyst islands design.

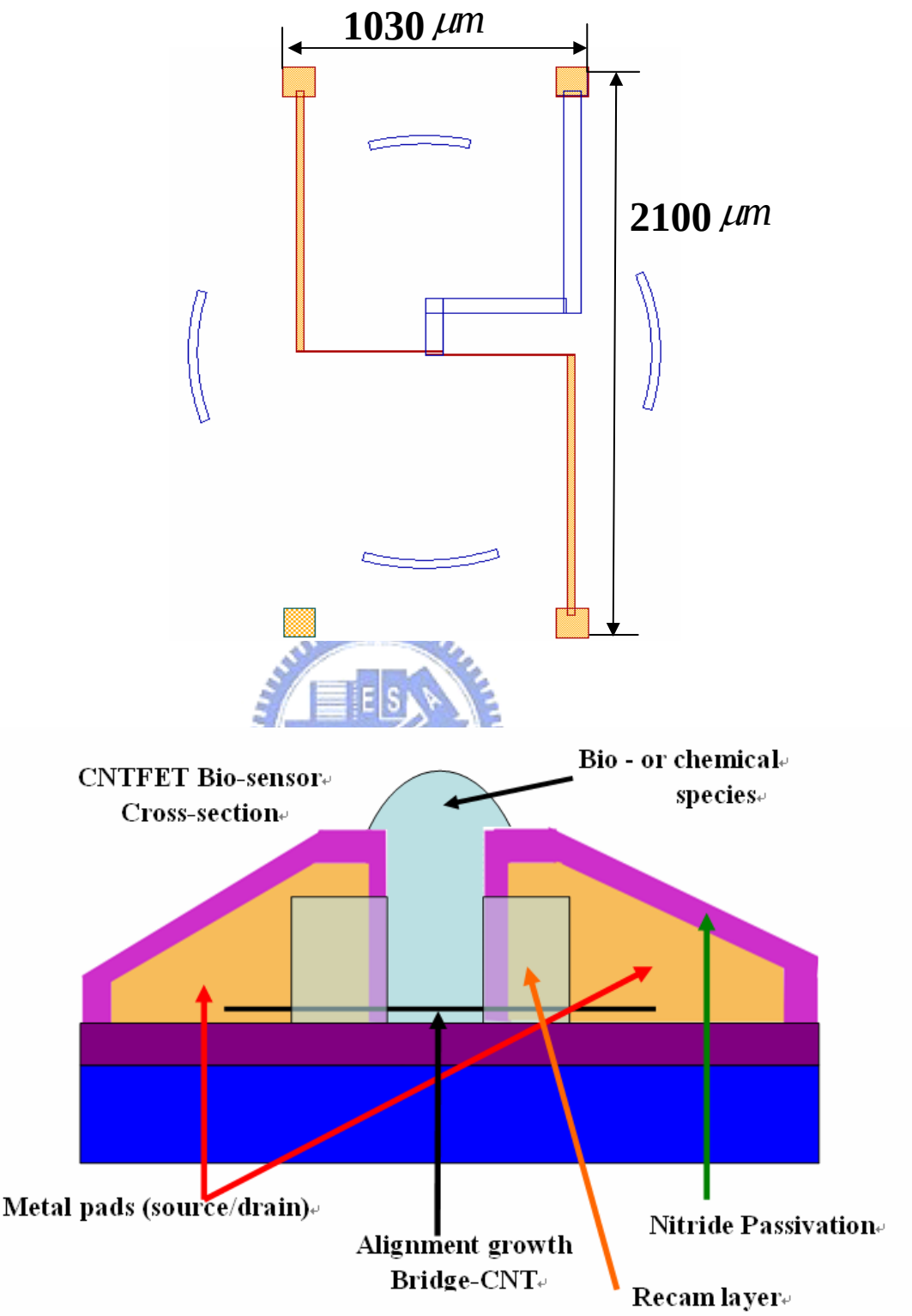


Figure 2.5 Layout and cross-section diagram of bio-sensor.

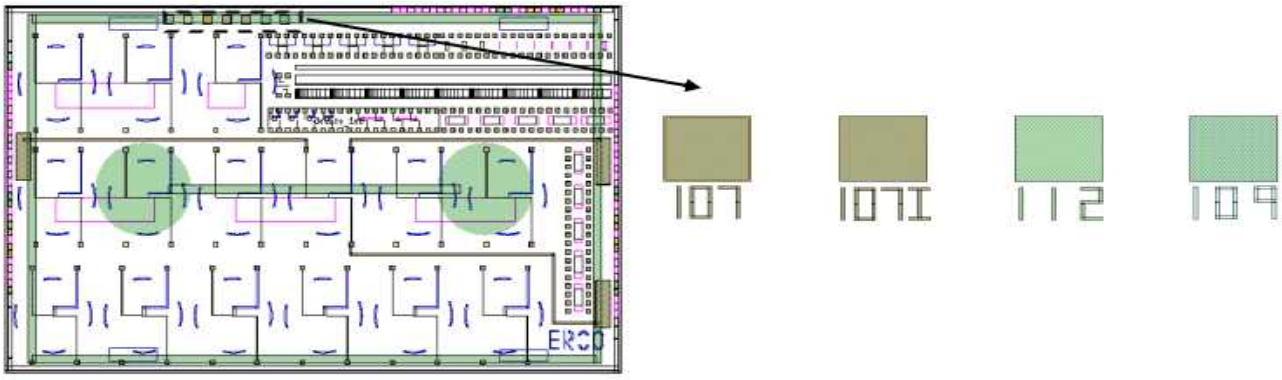
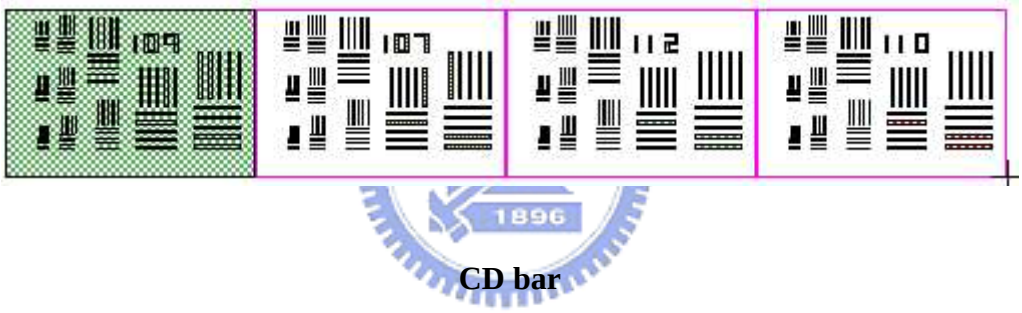
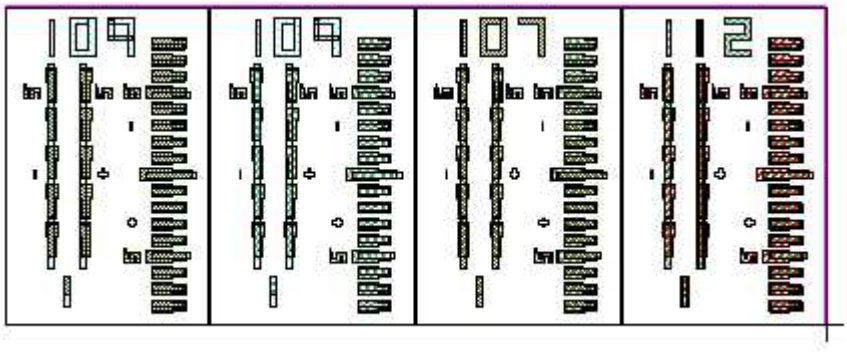


Figure 2.6

Process monitor test key is designed to confirm the etching conditions of contacts and pads and avoid over-etching.



CD bar



Vernier

Figure 2.7

CD bar and vernier are included to check the resolution and shift of lithography.

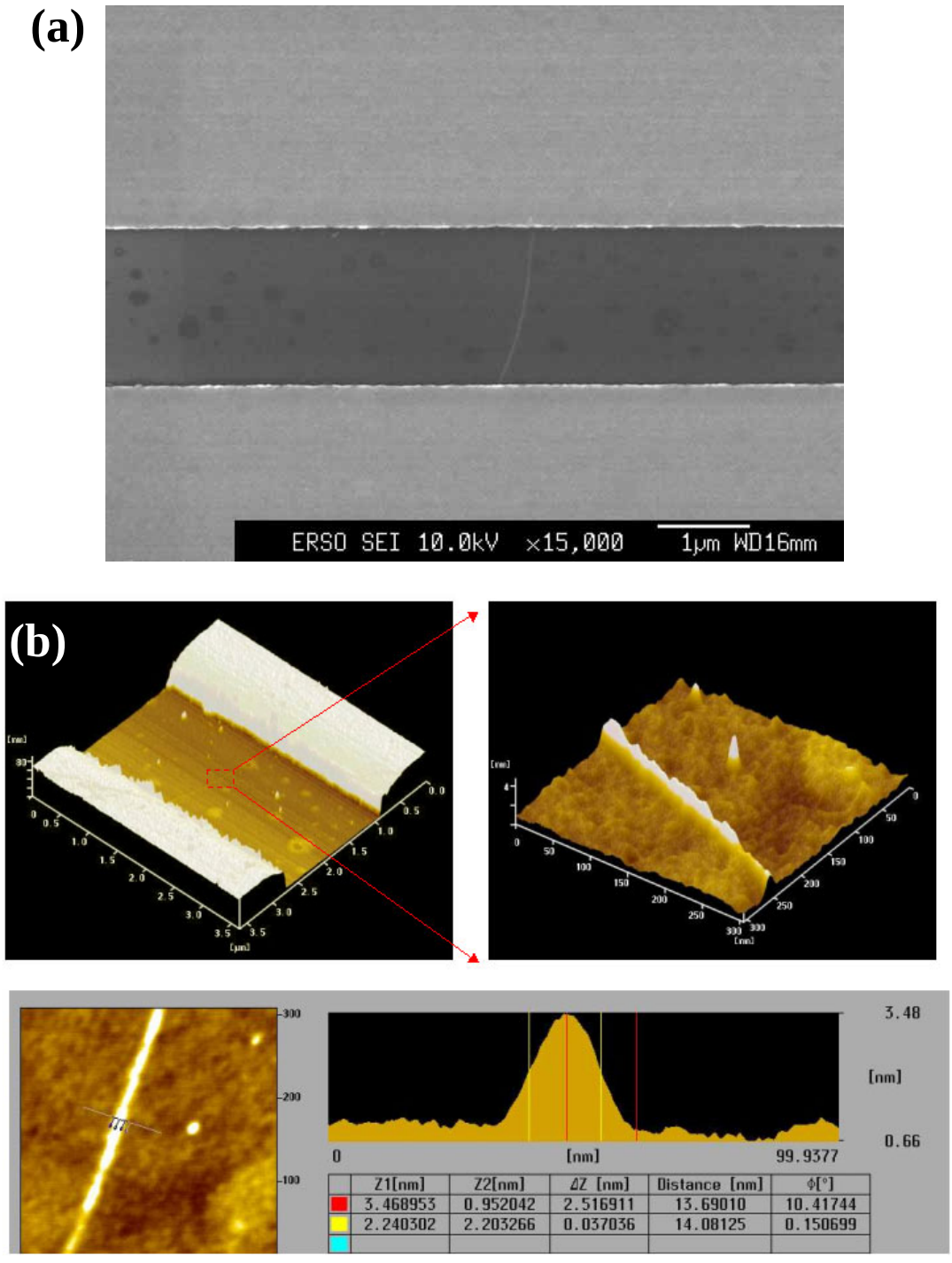


Figure 2.8

(a) A CNT-FET with a bundle of SWNTs (diameter = 14nm)

(b) AFM image of (a)

Chapter 3

A Carbon Nanotube Field Effect Transistor with Tunable Conduction-Type by Electrostatic Effects

3.1 Backgrounds and Motivation

For active device applications similar to the conventional FETs, the semiconducting-type single-walled nanotube (SWNT) is more suitable than the metallic-type SWNT because in the former, the channel conductance can be controlled/modulated by the gate bias. It is also noted that if the CNTs are multi-walled (MWNT) in nature, they will depict metallic-type electrical behaviors and will not be suitable for many nanoelectronics applications. In general, the CNT-FET acts like a p-type conduction device when it is exposed to air [1-5]. This phenomenon is ascribed to the absorbed oxygen at the interface of metal/SWNT, causing the pinning of Fermi level near the valance band [6-10]. Once the p-type CNT-FET is annealed in vacuum, the absorbed oxygen in the interface will be removed, and the CNT-FET is transformed from the pure p-type conduction to ambipolar or n-type conduction, depending on the annealing condition and/or the amount of remaining oxygen [10,13,15-17]. It is worth noting that if a device is ambipolar, it conducts either electrons or holes depending on the gate bias (In this chapter, the gate bias corresponds to bottom-gate bias. For the conventional structure with a traditional single gate, the ambipolar phenomenon would be disastrous as the ambipolar phenomenon cannot be easily suppressed). However, the electrical characteristics of the converted CNT-FETs vary widely and uncontrollably in this process, and the across-the-chip variations of FETs often widen and become intolerable after annealing.

Based on a former study of our group, we can manufacture air-stable n-type [12-13] or p-type CNT-FETs without any additional or complex annealing process (Table 3.1). However, we found that some ambipolar-type devices are always present in the Type-I devices due to process nonuniformity. And the Type-II devices always depict either n- or p-type characteristics rather than ambipolar type, depending on the passivation layer deposited on the SWNTs. For practical applications, we must eliminate the ambipolar devices by converting them to n- or p-type devices as needed.

Nonetheless, it is difficult to alter the conduction-type of individual CNT-FET located on the same chip. In contrast, the novel double-gated CNT-FET (DG CNT-FET) structure proposed in this chapter can provide a practical and reproducible method to form both n- and p-type-like CNT-FET devices as well as unipolar-type CNT-FET devices on the same chip [12,14]. The bias applied to the narrow top-gate plays the pivotal role of modulating the energy level within the CNT energy band. With the new approach, we can control the electrical characteristics of the CNT-FETs reliably without depending on complicated and often uncontrollable processes [15-16].

3.2 Device Fabrication

Two double-gated (DG) device structures, i.e., Type-I and Type-II, were fabricated in this work. While Type-I DG device utilizes the substrate wafer as a universal bottom-gate, Type-II DG device employs a separate patterned Ti layer as its individual bottom-gate. More importantly, different dielectric layers (both oxide and nitride) were employed in both types of devices (Table 3.1), which allows us to study the effects of oxygen absorption behaviors on the devices. The key process flows for fabricating the two device types are described below:

3.2.1. DG CNT-FETs with substrate wafer as the universal bottom-gate (Type-I)

The key process flow of the tunable Type-I DG CNT-FET structure with a universal substrate bottom-gate is shown in Figs. 3.1(a) – 3.1(d). Briefly, a 100nm silicon oxide was thermally grown on a 4-inch p-type silicon wafer. The silicon substrate wafer with a low resistivity of $0.02\,\Omega\text{-cm}$ also serves as the universal bottom-gate (i.e., Si substrate acts as the back-gate). Then, a 150-nm Ti layer was deposited by RF sputter, patterned, and etched to serve as the source/drain metal, as shown in Fig. 3.1(a). The spacing between the source and the drain electrodes is designed to be $2\,\mu m$. After the source/drain electrodes were patterned and etched, a prepared SWNT/Dimethylformamide (DMF) solution with the CNT density of $10{,}000/mm^2$ (counted by SEM pictures manually, as shown in Fig. 3.1(f)) was spun on the wafer, as shown in Fig. 3.1(b). Subsequently, a 200-nm low-temperature PE-CVD oxide was deposited at around 400 ^oC, as shown in Fig. 3.1(c). Next, contact holes of the source/drain regions were etched in the MERIE (magnetic enhanced RIE) dry etcher using CHF_3 gas. Finally, a second 150-nm Ti layer was deposited by RF-sputter, patterned, and etched to serve as the top-gate, as shown in Fig. 3.1(d). The top-gate length is designed to be either $0.6\,\mu m$ or $0.8\,\mu m$, and is placed in the middle between the S/D regions. The patterned second Ti layer also serves simultaneously as the pads for the source/drain contacts. In this way, a narrow top-gate was thus created on a bottom-gated SWNT FET, and the conduction type of the FET could be modulated by the bias applied to the narrow top-gate.

3.2.2 DG CNT-FETs with patterned Ti-layer as the individual bottom-gate (Type-II)

In order to strengthen the modulation of CNT-FET channel conduction, we

modify the Type-I design (shown in Fig. 3.1(d) as described above) to that shown in Fig. 3.1(e). It should be noted that a separate patterned bottom-gate is adopted while Type-I employs a universal bottom-gate. More importantly, while PECVD oxide was adopted as the top-gate dielectric in Type-I devices, both PECVD oxide and nitride were tried as the top-gate dielectric layer in Type-II devices, which allowed us to study the effects of oxygen desorption on the CNT-FET behaviors. Briefly, to fabricate Type-II devices, a 600-nm SiO_2 field oxide layer was first grown by wet oxidation at 985 ^{o}C on the 4-inch p-type silicon wafer. Then, a 150-nm Ti layer was deposited by RF sputtering, which was subsequently patterned and etched to serve as the bottom-gate metal. Afterwards, the wafer received a 200-nm low temperature PE-CVD oxide or nitride deposition process. A second 150-nm Ti layer was then deposited by RF sputtering, patterned, and etched to serve as the source/drain electrodes. Next, the SWNT/DMF solution was spun on the wafer, followed by another 200-nm PE-CVD dielectric deposition at around 390 ^{o}C (Table 3.1). Then, the contact holes of the source/drain regions were etched in the same MERIE dry etcher. Finally, a third 150-nm Ti layer was deposited by RF-sputtering, patterned, and etched as the top-gate. This patterned 3rd Ti layer also serves simultaneously as the pads for the source/drain contacts, while the position and dimension of the top-gate are nominally identical to those in Type-I structure. Afterwards, the wafers were annealed at 250°C in the air to improve the metal/CNT contact. The final Type-II DG CNT-FET device structure is as shown in Fig. 3.1(e). A commercial HP-4155A was applied to measure the I_d/V_g transfer curves of the CNT-FETs. The result will be discussed in the following sections.

3.3 Experimental Results and Discussion

Since we have fabricated two types of DG CNT-FET device structures, the device characteristics of both structures will be discussed. For the first device structure (Type-I, as shown in Fig. 3.1(d)), the entire substrate wafer, which serves as the bottom-gate, was biased from -5V to +5V at V_{ds} = 1V; while the top-gate was biased from 0V to -12V, at a step of -2V. The resultant transfer curves (i.e., drain current versus bottom-gate voltage) of a Type-I CNT-FET are shown in Fig. 3.2. It can be seen that, for this particular Type-I CNT-FET, when the top-gate voltage is biased at 0V, the CNT-FET exhibits ambipolar-type FET behavior. However, when the top-gate is biased toward more negative value (e.g., from 0V to -12V), the transfer characteristics change significantly. Specifically, for a given positive bottom-gate voltage, the drain current I_{DS} decreases as the top-gate voltage V_{tg} decreases from 0V to -12V, while I_{DS} for a given negative bottom-gate voltage increases instead. It can be seen that when the top-gate is decreased to -12V, the conducting channel under positive bottom-gate voltage is effectively pinched off, while the channel under the negative bottom-gate voltage is enhanced, as shown in Fig. 3.2. In a word, ambipolar-type CNT-FET is gradually converted to p-type CNT-FET by simply changing the top-gate voltage. In Fig. 3.5(c), it can be seen that a Type-I ambipolar device could be converted to n-type CNT-FET by applying a positive top-gate voltage.

A hypothesis based on the CNT-FET band gap structure is proposed to gain insights into the physical mechanisms of the conduction-type-tunable Type-I DG CNT-FET structure shown in Fig. 3.1(d). It is worth noting that many generic (i.e., without top-gate bias) Type-I CNT-FET devices in our study exhibit ambipolar behaviors, rather than the n-type-only behaviors. This trend in Type-I devices is

believed to be the result of using PECVD oxide as the top-gate dielectric. This is because at the process temperature of around 400 °C, even though high enough to desorb oxygen from CNT, a few oxygen atoms could be driven back to CNT during the PE-CVD TEOS oxide deposition process [10,13-14]. We therefore choose a generic ambipolar, rather than the n-type-only, CNT-FET to illustrate the proposed hypothesis. Its transfer characteristics (drain current versus bottom-gate voltage) are as shown in Fig. 3.3(a).

There has been increasing evidence to support that the interface behaves as a Schottky contact at the source and drain regions [10-11,13,15-17]. As shown in Fig. 3.3(b), when the bottom-gate voltage is floating, a few holes can be conducting. However, as shown in Fig. 3.3(d), when a positive bottom-gate voltage (with the top-gate floating) is applied to the CNT-FET, the energy band corresponding to the middle CNT channel region will be pulled down, decreasing the effective electron tunneling barrier. As a result, more electrons can tunnel through the interface barrier, and the electron current increases. On the other hand, as shown in Fig. 3.3(c), when a negative bottom-gate bias is applied (with the top-gate still floating), the energy band corresponding to the middle CNT channel region will be raised, so the holes can drift through the interface barrier easily. Consequently, the DG CNT-FET with the top-gate floating exhibits ambipolar characteristics.

Fig. 3.4 shows the band diagram when the effect of the top-gate bias is superimposed to our DG CNT-FET. As mentioned above, for a given positive bottom-gate, the energy band will be pulled down, and allows the electrons to tunnel through easily. By simultaneously applying a top-gate voltage to the DG CNT-FET, the energy band of CNT region directly under the top-gate electrode is altered. Specifically, when a positive bias is applied to the top-gate, the energy band of CNT

region directly under the top-gate electrode is pulled further down, while the barrier at the metal-CNT interface remains unchanged, as shown in Fig. 3.4(a). The current, resulting from electron flow, therefore remains essentially unchanged. If a large positive top-gate voltage is applied, the down-bending potential profile will slightly accelerate the electron flow in the CNT due to the barrier lowering effect, and the drain current will increase slightly. However, when a negative bias is applied to the top-gate, the energy band of CNT region directly under the top-gate electrode is pulled up instead, as shown in Fig. 3.4(b). Since the extra electron barrier at the conduction band is created within the CNT region itself, the electron flux inside the CNT is effectively blocked. Therefore, even though the initial CNT-FET shows ambipolar behaviors, the electron flow channel is effectively blocked off by the negative top-gate bias. At the same time, the hole current at the negative bottom-gate region remains essentially unchanged because the extra barrier exists at the conduction band only (Fig. 3.5(a)). The CNT-FET now behaves like a p-type conduction, as shown in Fig. 3.4(c) (V_{ds}=1V). The more negative the top-gate bias is, the lower the conducting current can be obtained at a given positive bottom-gate bias. This is consistent with the trend shown previously in Fig. 3.2. This explains why the Type-I DG CNT-FET will behave like p-type FET under the negative top-gate bias, even the generic Type-I CNT-FET (i.e., the device without the top-gate modulation) depicts ambiploar behaviors.

Fig. 3.5 shows the case for the negative bottom-gate bias. When a negative bias is applied to the top-gate simultaneously, the barrier lowering effect occurs at the drain side that results in a significant increase of hole tunneling, as shown in Fig. 3.5(a) [18]. However, when a positive bias is applied to the top-gate, as shown in Fig. 3.5(b), the hole flux is blocked. This will suppress the conductance of holes, and the

generic ambipolar CNT-FET now depicts n-type FET characteristics, as shown in Fig. 3.5(c) (V_{ds} = 1V).

Since for the mainstream CMOS circuit applications, both p- and n-type MOSFETs are called for on the same chip. It is necessary to form n-type, in addition to p-type CNT-FETs, on the same chip for the complementary circuits. Several approaches have been previously reported to form n-type CNT-FETs by employing complex doping processes (e.g., adopting alkali metals) [19-21] or thermal/electrical annealing processes [10]. These approaches, however, require extra processing and masking steps to convert generic p-type CNT-FETs in vacuum or in the inert gas. In contrast, no extra annealing steps are needed to form air stable n-type CNT-FETs [12-13] selectively using the DG CNT-FET structure proposed in this chapter. As mentioned previously, for the Type-II structure both PE-oxide and PE-Nitride were tried as the top-gate dielectric. By using PE-Nitride as the top-gate dielectric, the process temperature of the deposition would be high enough to simultaneously remove the oxygen atoms from the CNT or CNT/metal interface in the PE-CVD deposition chamber. So we can fabricate n-type CNT-FETs by selectively converting generic Type-II structures without extra processing steps. This is because when the oxygen atoms are removed during the PE-CVD process, the Fermi-level in Type-II structure moves away from the valence band and becomes closer to the middle of the bandgap, compared with that of Type-I structure shown already in Fig. 3.3(b). So by applying a negative bias to the bottom-gate of Type-II CNT-FETs selectively, the hole cannot tunnel through the energy barrier efficiently, and we could selectively create n-type CNT-FETs on the chip.

Although we can create n-type CNT-FETs selectively, how to control the uniformity of electrical characteristics of these devices remains an open question.

Since the generic Type-I devices tend to depict ambipolar behaviors, the electrical characteristics of the Type-I devices, however, can be tuned to either n- or p-type behaviors precisely, according to the hypothesis described above.

As shown in Fig. 3.6(a), the initial transfer characteristics of the Type-II CNT-FET depict pure n-type behavior with I_{max} = 63.2 nA at V_{bg} = 10V and V_{ds} = 1V, representing on/off ratio of greater than $\mathbf{10^5}$. Depending on whether a positive or negative bias is applied to the top-gate, the Type-II CNT-FET will behave differently. When the top-gate is negatively biased, the drain current of Type-II CNT-FET decreases, and reaches complete pinch-off when the top-gate becomes more negative than Vtg = -10V. On the other hand, the drain current increases slowly as the top-gate increases toward more positive value. These trends could again be explained by the proposed hypotheses shown previously in Fig. 3.4 and Fig. 3.5. At Vtg = -10V, the down-bending energy band in the Type-II CNT FET, similar to that shown in Fig. 3.4(b) for the Type-I structure, is pulled up instead in the region directly under the top-gate, which effectively blocks the electron flow. On the contrary, when a positive top-gate is applied, the down-bending potential profile, similar to that shown previously in Fig. 3.4(a) for Type-I structure, will slightly accelerate the electron flow due to the barrier lowering effect, and the drain current increases slightly, as shown in Fig. 3.6(b). It is noticed that the current in Fig. 3.6(a) decreases in the negative bottom-gate region when the top-gate voltage increases. This is because according to Fig. 3.5(b), when the top-gate voltage becomes more positive, the energy band directly under the top-gate will be bent down further, and this down-bending potential will block the hole tunneling.

This hypothesis could also be applied to explain the suppression of the p-type behavior in Type II devices (Fig. 3.7). Fig. 3.6 shows a generic n-type Type-II device

with its n-type characteristics being gradually suppressed under negative top-gate biases, while Fig. 3.7 depicts a generic p-type Type-II device with its p-type characteristics being gradually suppressed under positive top-gate biases. These trends are consistent with our proposed hypothesis.

By resorting to DG CNT-FET structure, V_{th} of the device can be modulated by varying the biases of the top-gate and the bottom-gate. When the roles of the top-gate and the bottom-gate are reversed, the transfer curves (drain current versus top-gate voltage) of DG CNT-FET are plotted in Fig. 3.8. It can be seen that when the bottom-gate is floating and the top-gate voltage is swept from –8V to +8V and back to –8V, a pronounced hysteresis loop is observed [22-25]. In our work, four kinds of bottom-gate and top-gate dielectric layers (i.e., PE-oxide, PE-nitride, thermal-oxide, and thermal-nitride) were studied, and the hysteresis phenomenon persists. Here in Fig. 3.8 we only depict the data with PE-nitride as both the bottom- and top-gate dielectric layers. When $V_{bg} > 0V$, by sweeping from $-V_{tg}$ to $+V_{tg}$, the corresponding energy band switches from that shown in Fig. 3.4(b) to Fig. 3.4(a); and by sweeping from $+V_{tg}$ back to $-V_{tg}$, the corresponding energy band switches from that shown in Fig. 3.4(a) back to Fig. 3.4(b). The energy band shift that occurs during Vtg sweeping accounts for the observed hysteresis loop observed in Fig. 3.8. Similarly, When $V_{bg} < 0V$, by sweeping from $-V_{tg}$ to $+V_{tg}$, the corresponding energy band switches from that shown in Fig. 3.5(a) to Fig. 3.5(b), and vice versa. The corresponding shift in energy band between the two cases (i.e., from Fig. 3.4(b) to Fig. 3.4(a), compared to that from Fig. 3.5(a) to Fig. 3.5(b); and vice versa) is essentially identical. This explains why the hysteresis loops between the curves with either positive or negative bottom-gate biases are essentially identical, as shown in Fig. 3.8.

3.4 Summary

In this chapter, a novel double gate structure is proposed to control the conducting type of the CNT-FET in order to achieve unipolar-type devices without resorting to complex processes. Our results show that ambipolar-type CNT-FET can be converted to n- and p-type CNT-FETs by controlling the biases applied to the top- and bottom-gate electrodes. Our approach opens the possibility of creating specific type of CNT-FETs with well-controlled characteristics. This is crucial for CMOS circuits as well as certain circuit applications, such the detector applications where p-type CNT-FET sensor with high on/off current ratio is required for negative charge enzyme system [26]. In the proposed DG CNT-FET structure, the I-V characteristics of each random device can be well-turned to the same level, and the ambipolar character of CNT-FETs can be annihilated. Furthermore, the threshold voltage of CNT-FETs can be possibly adjusted by using different bottom-gate and top-gate biases. These features make the new structure especially promising for applications in future ultrahigh sensitive sensors.

References

[1] M. S. Dresselhaus, G. Dresselhaus, Ph. Avouris, *Carbon nanotubes: synthesis, structure, properties, and applications*: Springer-Verlag, Berlin, 2001.

[2] A. Bachtold, P. Hadley, T. Nakanishi C. Dekker**,** "Logic circuits with carbon nanotube transistors," *Science*, Vol. **294**, Issue: 5545, p.1317, November, 2001.

[3] S. J. Wind, J. Appenzeller, R. Martel, V. Derycke, Ph. Avouris, "Vertical scaling of carbon nanotube field-effect transistors using top gate electrodes," *Appl. Phys. Lett.,* Vol. **80**, Issue: 20, pp.3817-3819, May, 2002.

[4] J. Appenzeller, J. Knoch, V. Derycke, R. Martel, S. Wind, and Ph. Avouris, "Field-modulated carrier transport in carbon nanotube transistors," *Phys. Rev. Lett.,* Vol. **89**, Issue: 12-16, p.126801, September, 2002.

[5] A. Javey, Q. Wang, W. Kim, and H. Dai, "Advancements in complementary carbon nanotube field-effect transistors," *IEDM Technol. Dig.,* pp.741-744, 2003.

[6] P. G. Collins, K. Bradley, M. Ishigami, A. Zettl, "Extreme oxygen sensitivity of electronic properties of carbon nanotubes," *Science*, Vol. **287**, pp.1801-4, March, 2000.

[7] G. U. Sumanasekera, C. K. W. Adu, S. Fang, and P. C. Eklund, "Effects of gas adsorption and collisions on electrical transport in single-walled carbon nanotubes," *Phys. Rev. Lett.,* Vol. **85**, Issue: 5, pp.1096-9, July, 2000.

[8] K. Bradley, S.-H. Jhi, P. G. Collins, J. Hone, M. L. Cohen, S. G. Louie, and A. Zettl, "Is the intrinsic thermoelectric power of carbon nanotubes positive?" *Phys. Rev. Lett.,* Vol. **85**, Issue: 20, pp.4361-4, November, 2000.

[9] S.-H. Jhi, S. G. Louie, and M. L. Cohen, "Electronic properties of oxidized carbon nanotubes," *Phys. Rev. Lett.,* Vol. **85**, Issue: 8, pp.1710-3, August, 2000.

[10] V. Derycke, R. Martel, J. Appenzeller, Ph. Avouris, "Controlling doping and

carrier injection in carbon nanotube transistors," *Appl. Phys. Lett.,* Volume **80**, Issue: 15, pp.2773-2775, April, 2002.

[11] S. Heinze, J. Tersoff, R. Martel, V. Derycke, J. Appenzeller, and Ph. Avouris, "Carbon nanotubes as schottky barrier transistors," *Phys. Rev. Lett.,* Vol. **89**, Issue: 10, pp.106801-4, September, 2002.

[12] J.-H. Wei, H.-H. Wang, M.-J. Kao, "Method for fabricating n-type carbon nanotube device," US patent, Patent number: US6723624, Date of patent: 2004-04-20.

[13] D. Kaminishi, H. Ozaki, Y. Ohno, K. Maehashi, K. Inoue, K. Matsumoto, Y. Seri, A. Masuda, and H. Matsumura, "Air-stable *n*-type carbon nanotube field-effect transistors with Si_3N_4 passivation films fabricated by catalytic chemical vapor deposition,**"** *Appl. Phys.Lett.,* Vol. **86, p.**113115, March, 2005.

[14] J.-H Wei, H.-H Wang, H.-H Chen, M.-J Lai, M.-J Kao, and M.-J Tsai, "A novel short-gate carbon nanotube thin film transistors," *Proceedings of the IEEE-TSA,* pp.42-45, 2003.

[15] Y.-M. Lin, J. Appenzeller, and Ph. Avouris, "Ambipolar-to-unipolar conversion of carbon nanotube transistors by gate structure engineering," *Nano Lett.,* Vol. **4**, No. 5, pp.947-950, March, 2004.

[16] A. Javey, J. Guo, D. B. Farmer, Q. Wang, D. Wang, R. G. Gordon, M. Lundstorm, and H. Dai, "Carbon nanotube field-effect transistors with integrated ohmic contacts and high-κ gate dielectric**s,"** *Nano Lett.,* Vol. **4**, No. 3, pp. 447-450, February, 2004.

[17] M. Radosavljeviá, J. Appenzeller, Ph. Avouris, and J. Knoch, "High performance of potassium n-doped carbon nanotube field-effect transistors," *Appl. Phys. Lett.,* Vol. **84**, No. 18, pp.3693-3695, May, 2004.

[18] S. M. Sze, *Physics of Semiconductor Devices*: Wiley, 1981.

[19] M. Bockrath, J. Hone, A. Zettl, P. L. McEuen, A. G. Rinzler and R. E. Smalley, "Chemical doping of individual semiconducting carbon-nanotube ropes," *Phys. Rev. B.,* Vol. **61,** Issue: 16, pp.R10606-8, April, 2000.

[20] C. Zhou, J. Kong, E. Yenilmez, and H. Dai, "Modulated chemical doping of individual carbon nanotubes,**"** *Science,* Vol. **290**, No. 5496, pp.1552–1555, November, 2000.

[21] N. Bendiab, A. Righi, E. Anglaret, J. L. Sauvajol, L. Duclaux, F. Béguin, "Low-frequency Raman modes in Cs- and Rb-doped single wall carbon nanotubes," *Chemical Physics Letters*, Vol. **339**, Issue: 5-6, pp.305-310, May, 2001.

[22] W. Kim, A. Javey, O. Vermesh, Q.Wang, Y. Li, and H. Dai, "Hysteresis caused by water molecules in carbon nanotube field-effect transistors," *Nano Lett.,* Vol. **3**, No. 2, pp.193-198, January, 2003.

[23] J. B. Cui, R. Sordan, M. Burghard, and K. Kern, "Carbon nanotube memory devices of high charge storage stability," *Appl. Phys. Lett.,* Vol. **81**, No. 17, pp. 3260-3262, October, 2002.

[24] M. S. Fuhrer, B. M. Kim, T. Durkop, and T. Brintlinger, "High-mobility nanotube transistor memory," *Nano Lett.,* Vol. **2**, No. 7, pp.755-759, May, 2002.

[25] M. Radosavljevic´, M. Freitag, K. V. Thadani, and A. T. Johnson, "Nonvolatile molecular memory elements based on ambipolar nanotube field effect transistors," *Nano Lett.,* Vol. **2**, No. 7, pp.761-764, June, 2002.

[26] K. Besteman, J.-O. Lee, F. G. M. Wiertz, H. A. Heering, and C. Dekker, "Enzyme-coated carbon nanotubes as single-molecule biosensors," *Nano Lett.,* Vol. **3**, No. 6, pp.727-730, May, 2003.

Table 3.1 The electrical characteristics of device Type I and Type II

	The gate dielectric layer of bottom gate /Deposition temperature /Film thickness	The gate dielectric layer of top gate /Deposition temperature /Film thickness	Majority type of The Devices On a wafer
*	PE-oxide/400 °C/200nm	PE-oxide/400 °C/200nm	P-type[a]
Type II[d]	PE-oxide/400 °C/200nm	PE-nitride/390 °C/200nm	N-type[b]
*	PE-nitride/390 °C/200nm	PE-oxide/400 °C/200nm	P-type[a]
Type II[d]	PE-nitride/390 °C/200nm	PE-nitride/390 °C/200nm	N-type[b]
Type I[c]	Thermal-oxide/400 °C/100nm	PE-oxide/400 °C/200nm	P-type[a]
*	Thermal-oxide/400 °C/100nm	PE-nitride/390 °C/200nm	N-type[b]

*** Data not shown**

[a,b]Some of these devices contains Ambipolar-type characteristics

[c,d]The major differences between Type-I (Fig. 3.1d) and Type-II (Fig. 3.1e) lie in the separate bottom-gate design in Type-II structure and the different dielectric layers between the two types

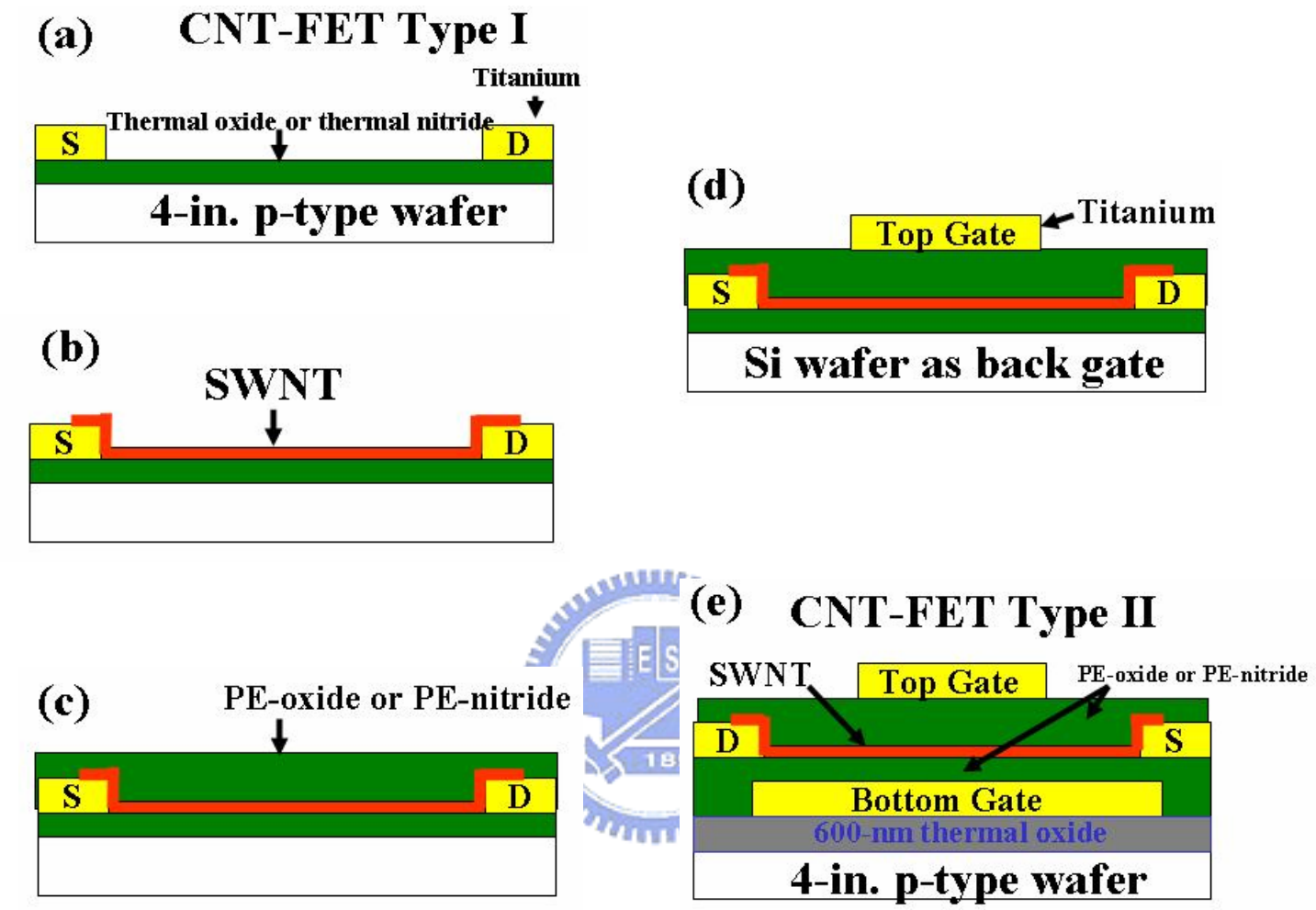


Fig. 3.1 Conduction-Type-Tunable CNT-FETs. Figs. 1(a)- 1(d) depict key process steps for Type-I structure, while Fig. 3.1e shows the cross-sectional view for Type-II structure. (a) 100nm oxide or nitride was grown as the back-gate dielectric on p-type silicon wafer (0.02Ω-cm), followed by Ti deposition/pattern/etch to serve as the source/drain metal. (b) SWNT was spun-on the wafer in proper solution concentration. (c) Top-gate dielectric layer was deposited by low temperature PE-CVD (PE-oxide or PE-nitride). (d) Second Ti layer was sputtered, patterned, and etched to serve as the top-gate. (e) Cross-sectional view of the new Type-II double-gated (DG) CNT-FET structure. The major differences between Type-I (Fig. 3.1d) and Type-II (Fig. 3.1e) lie in the separate bottom-gate design in Type-II structure and the different dielectric layers between the two types.

(f)

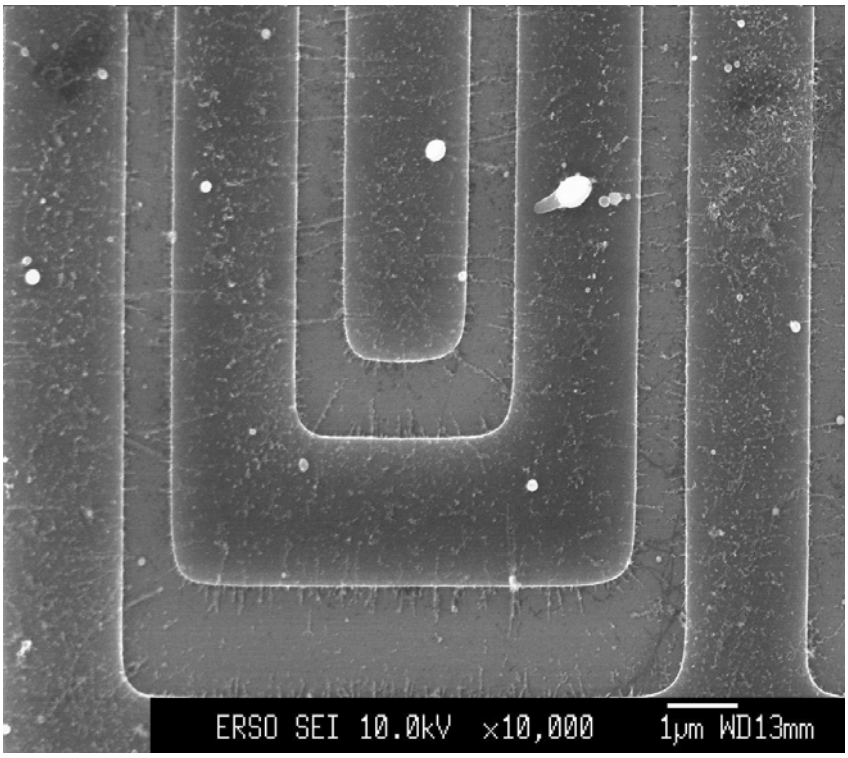


Fig. 3.1 (f) SEM picture with SWNT/DMF solution spun on a wafer.

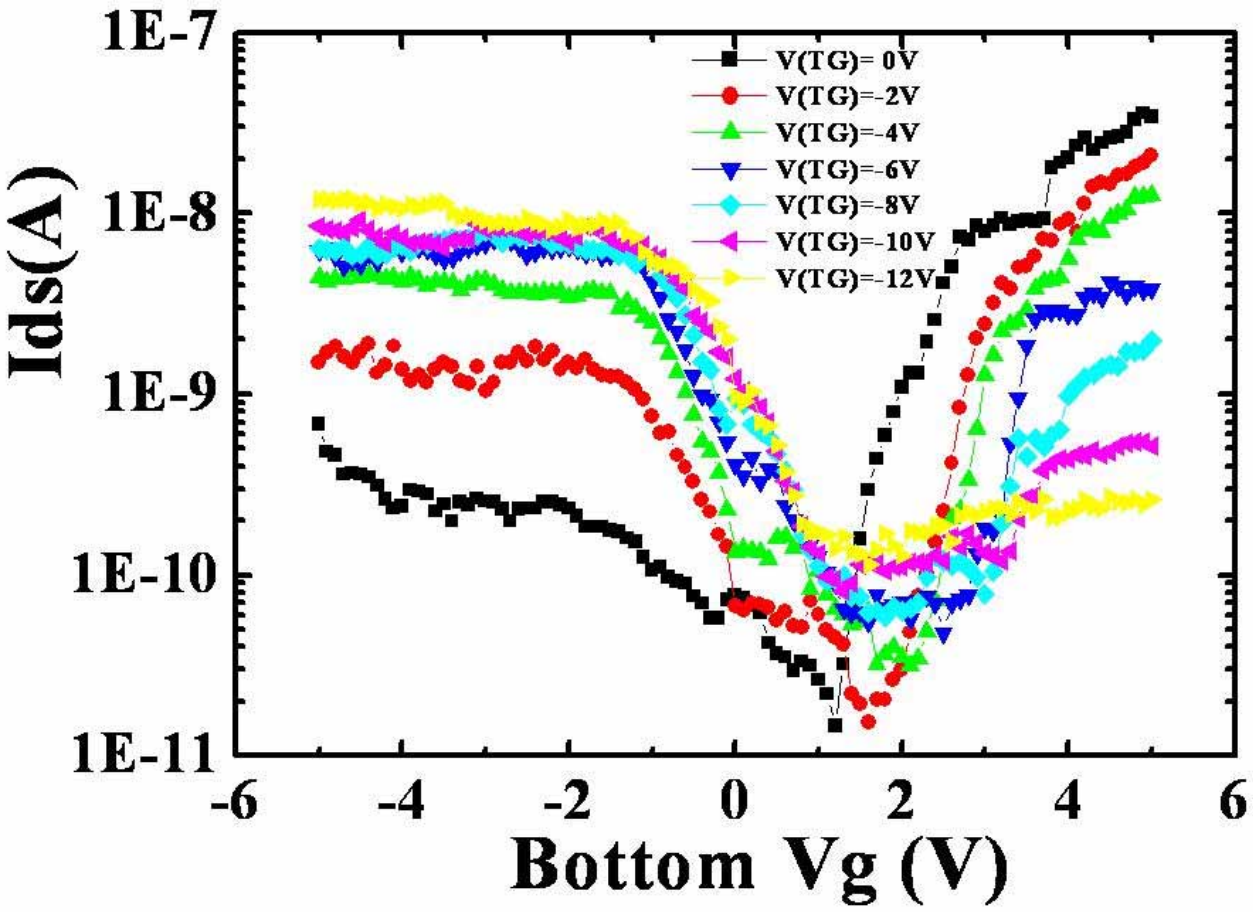
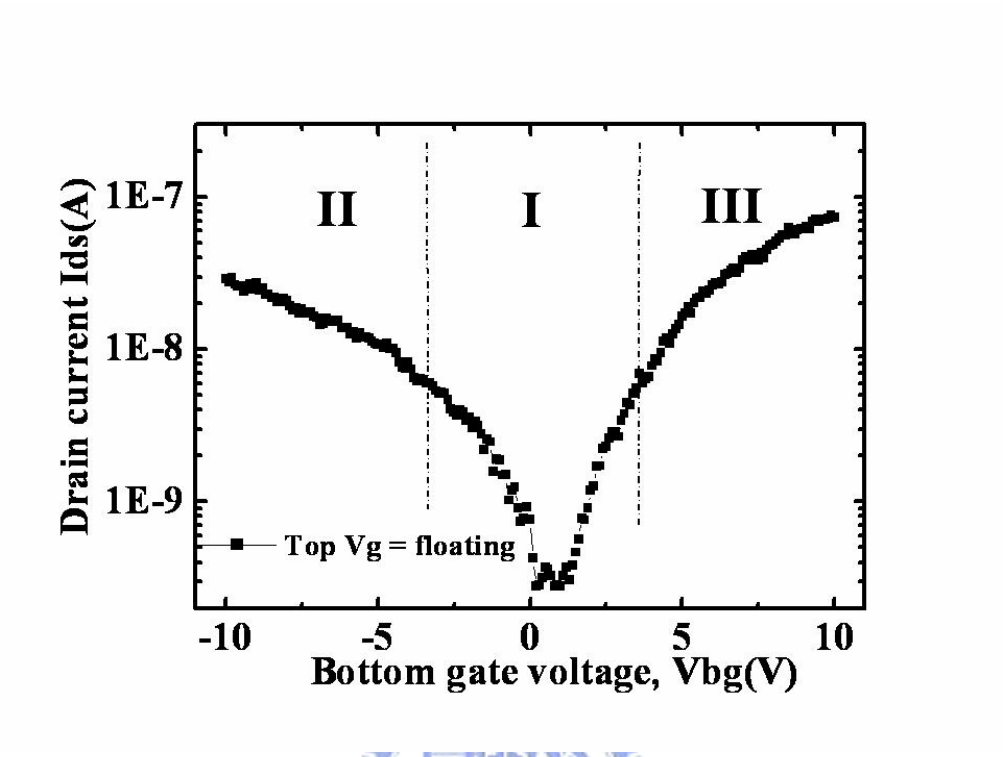


Fig. 3.2 Transfer characteristics (drain current versus bottom-gate voltage) highlighting that generic ambipolar-type CNT-FET can be gradually converted to p-type CNT-FET by simply varying the top-gate bias at Vds = 1V.



(a) Transfer characteristics

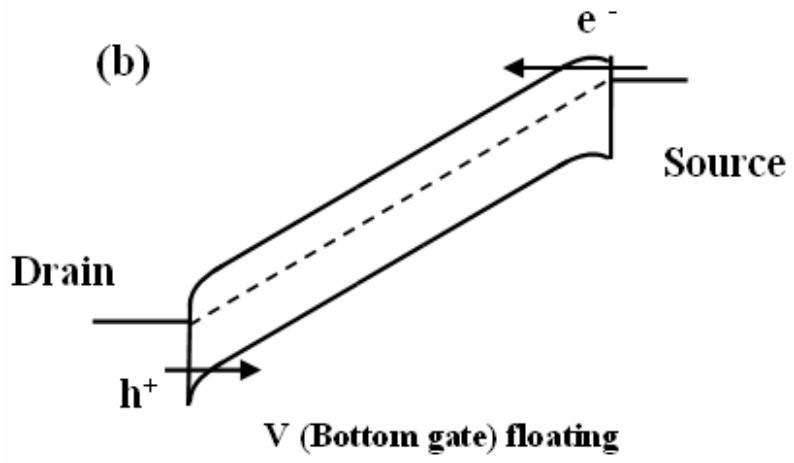


Fig. 3.3 (a) Transfer characteristics (i.e., drain current versus bottom-gate voltage) with floating top-gate showing ambipolar behaviors. (b)Band diagram with floating top-gate and bottom-gate, only a few holes can drift through the interface Schottky barrier, corresponding to the region Ⅰ of (a).

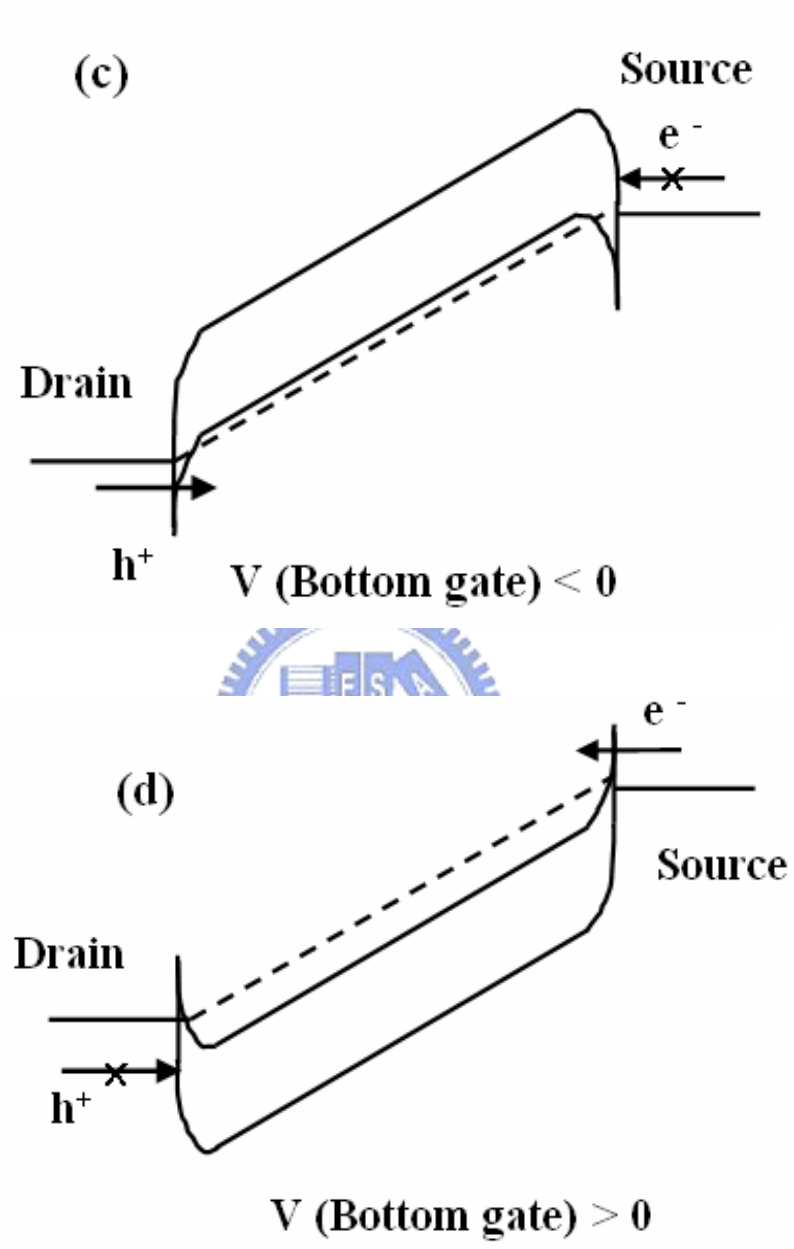


Fig. 3.3 (c) Band diagram with floating top-gate and negative bottom-gate, the hole will flow easily through the interface Schottky barrier, corresponding to the region II of (a). (d) Band diagram with floating top-gate and positive bottom-gate, the electron will tunnel easily through the interface Schottky barrier, corresponding to the region III of (a).

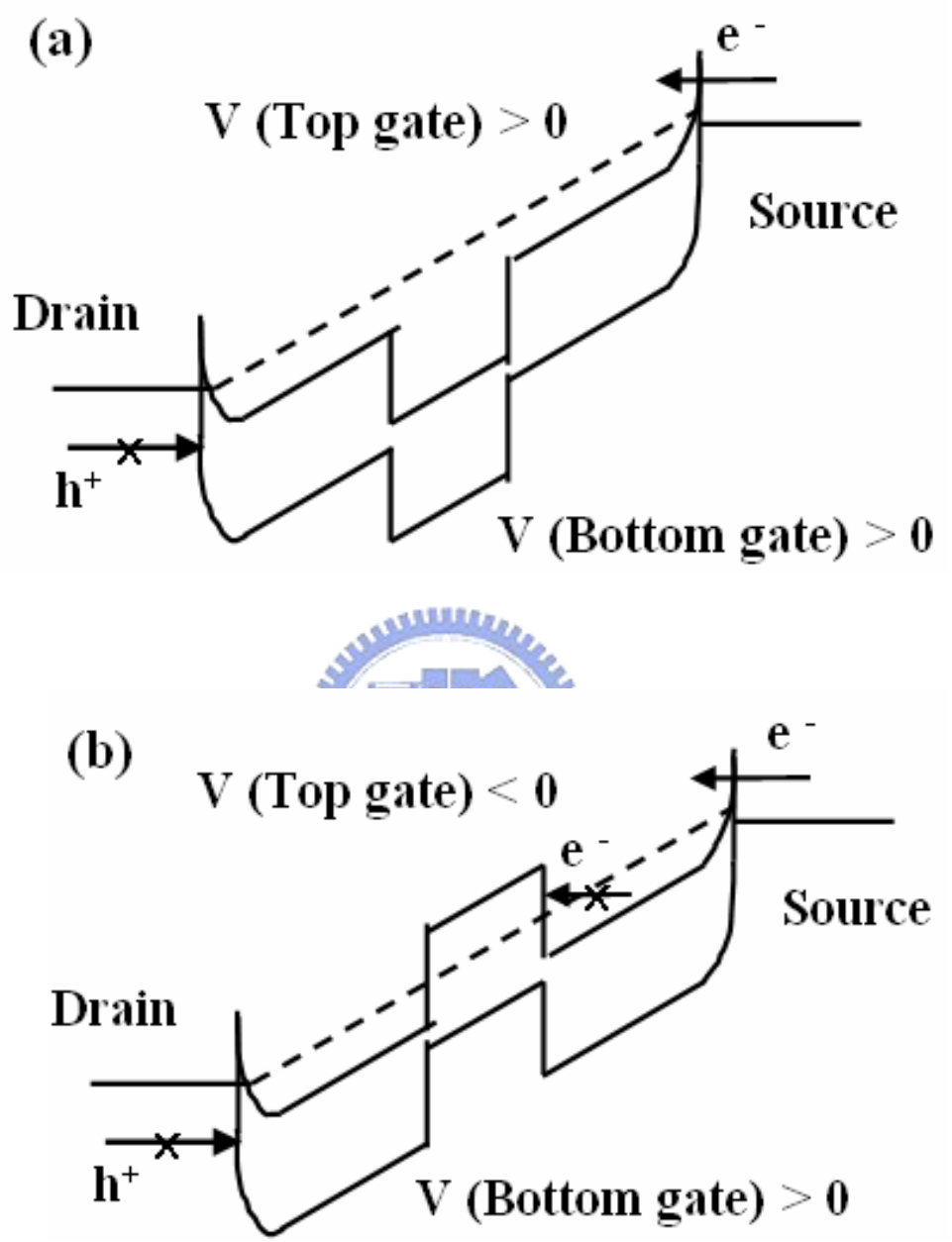


Fig. 3.4 By varying the top-gate voltage from positive to negative in the presence of positive bottom-gate voltage, the energy band within the CNT will be shifted as follows: (a) With positive top-gate, the electron flow will act as if no top-gate bias is applied. (Even if a large positive bias is applied to the top-gate, the down-bending potential profile will only slightly accelerate the electron flow in the CNT due to the barrier lowering effect, and the drain current will increase only slightly.) (b) With negative top-gate, the electron flow will be suppressed (red solid circle line in Fig. 3.4(c)), and the current level will drop effectively.

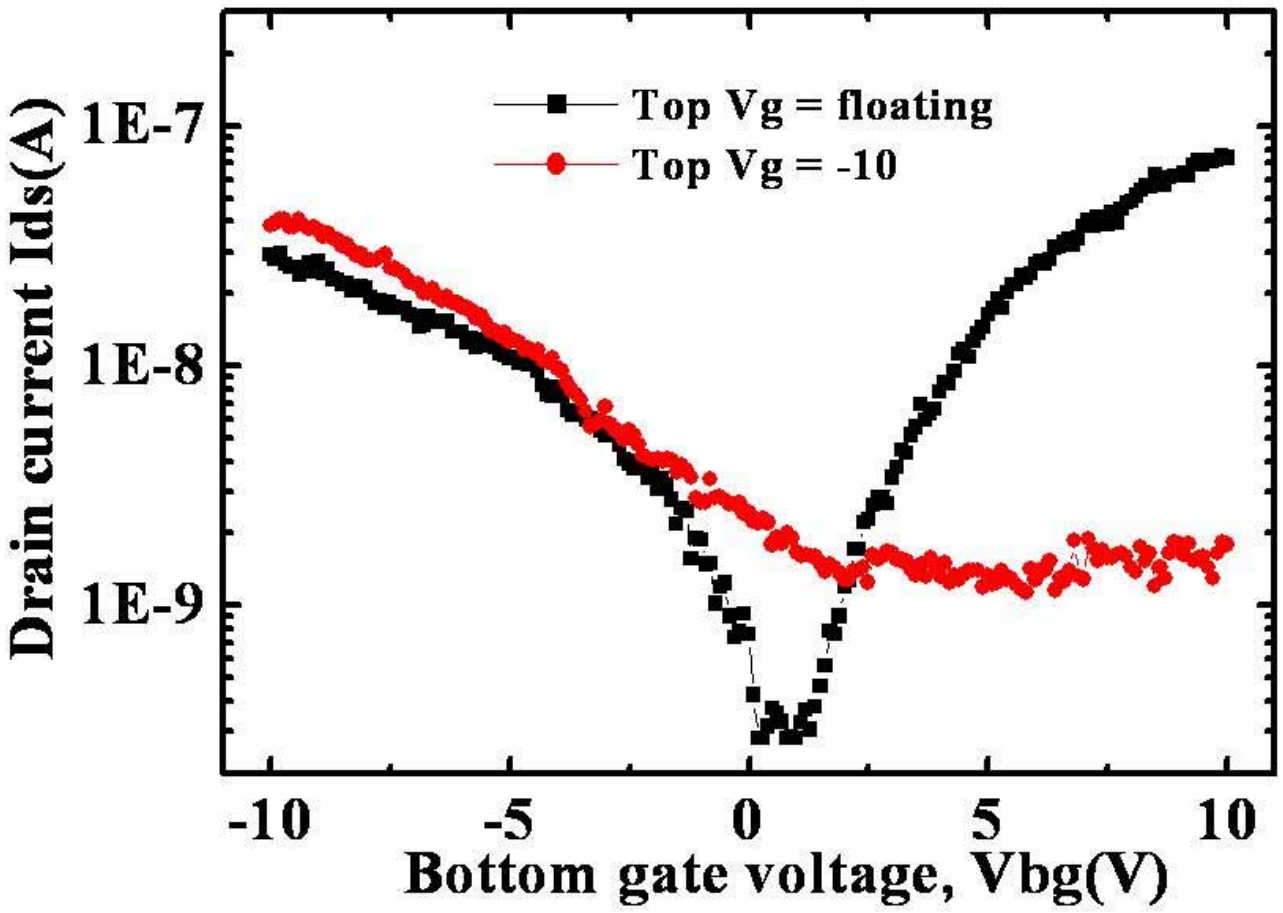


Fig. 3.4 (c) Transfer characteristics corresponding to Fig. 3.4(b).

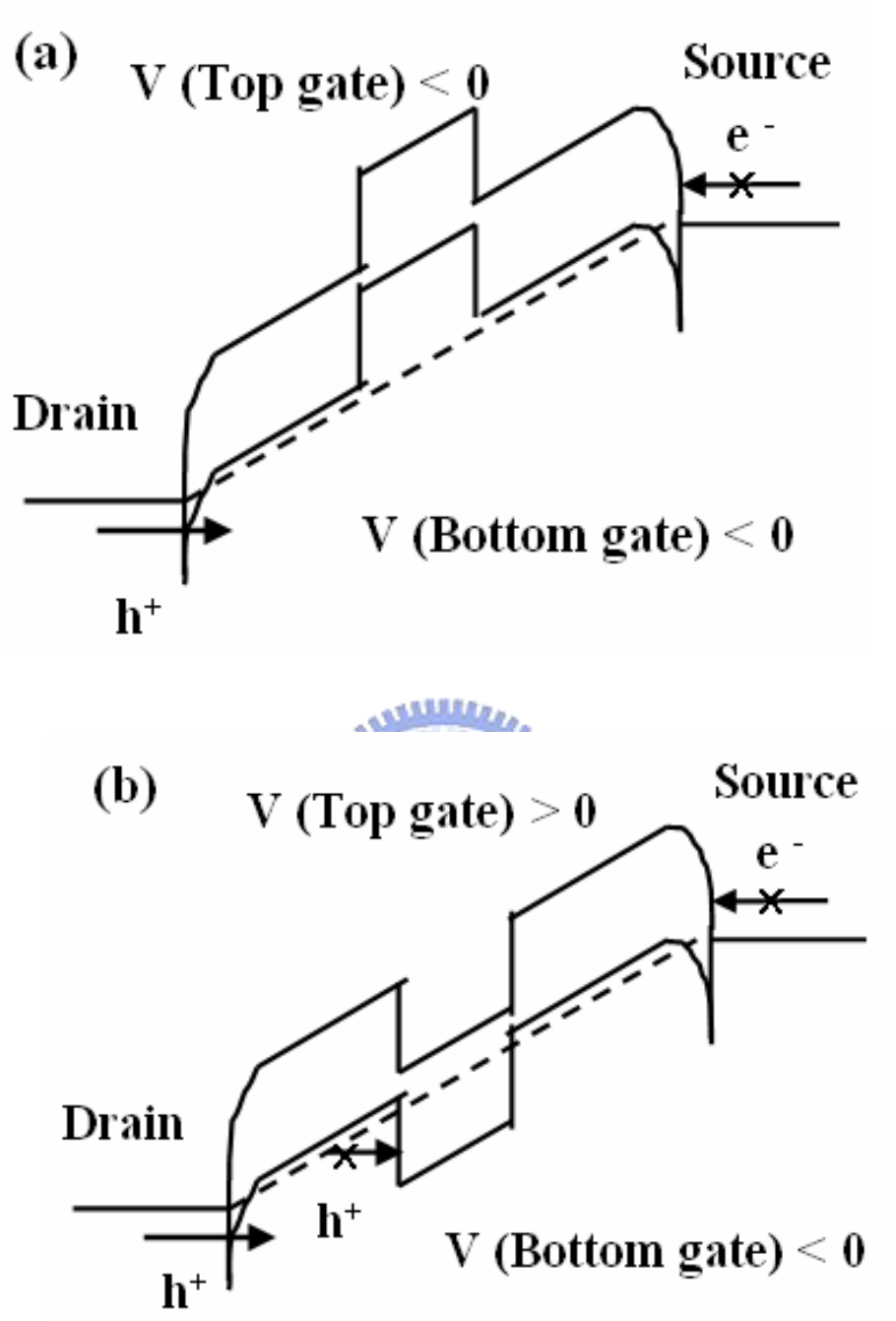


Fig. 3.5 By varying the top-gate bias from negative to positive in the presence of negative bottom-gate voltage, the energy band within the CNT will be shifted as follows: (a) With negative top-gate bias, the hole current will act as if no top-gate bias is applied. (When the top-gate voltage is at a much more negative bias, the barrier lowering effect occurs at the drain side, and results in a significant increase of hole-tunneling) (b) With positive top-gate bias, the hole flow will be suppressed (red solid circle line in Fig. 3.5(c)), and the current level will drop effectively.

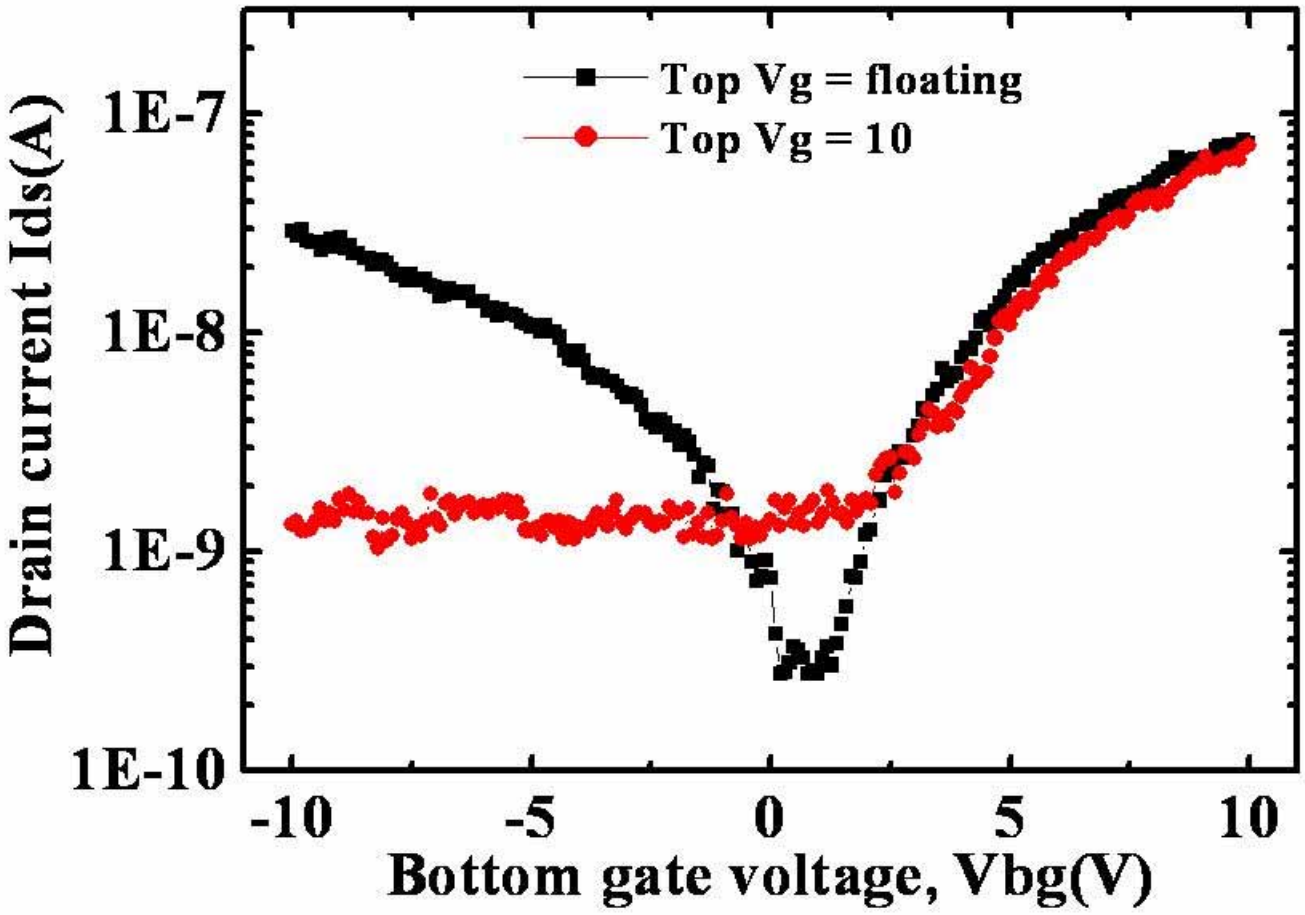


Fig. 3.5 (c) Transfer characteristics corresponding to Fig. 3.5(b).

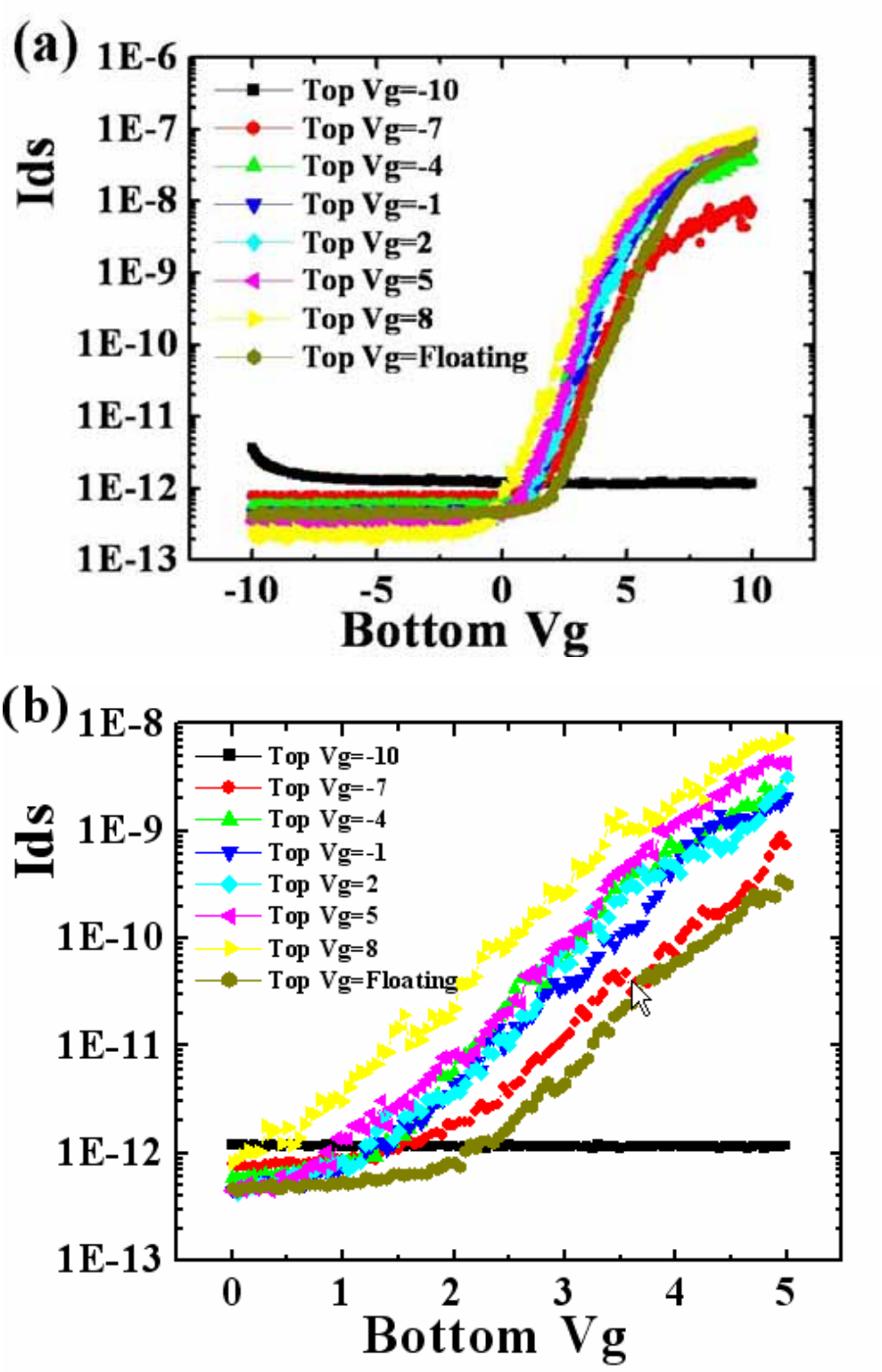


Fig. 3.6 (a) According to the hypothesis proposed in Fig. 3.4, n-type behavior in Type-II CNT-FET can be fully suppressed by applying negative bias to the top-gate. In other word, the on/off ratio can be controlled at will. (b) A bloated view of Fig. 3.6a with bottom-gate varying between 0~5V. With positive top-gate bias, the down-bending potential profile shown in Fig. 3.4a will slightly accelerate the electron flow due to the barrier lowering effect, and the drain current will increase slightly.

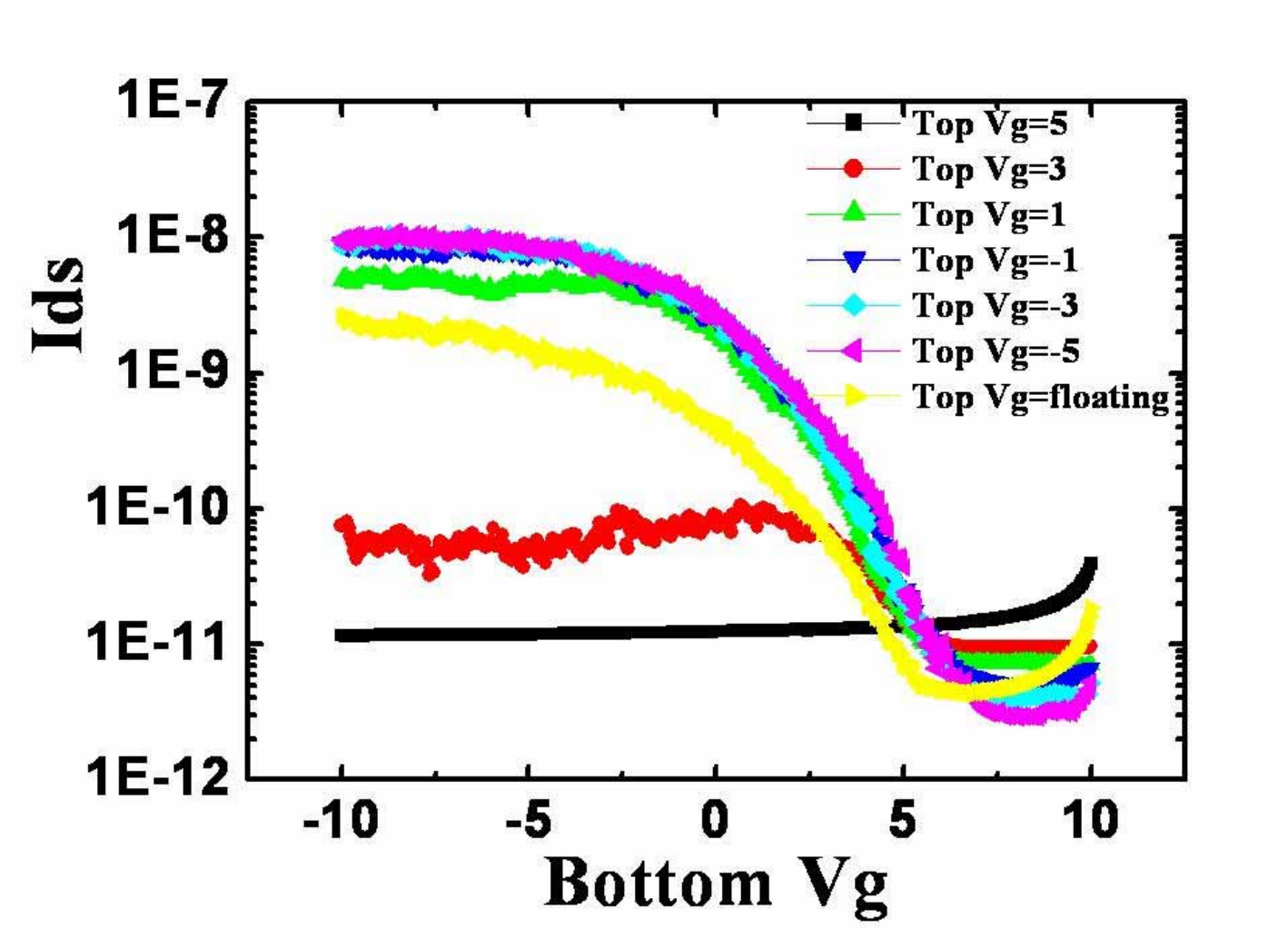


Fig. 3.7 According to the hypothesis proposed in Fig. 3.5, p-type behavior in Type-II CNT-FET can be fully suppressed by applying positive bias to the top-gate. This figure shows gradual conversion by simply varying the top-gate bias at Vds = 1V.

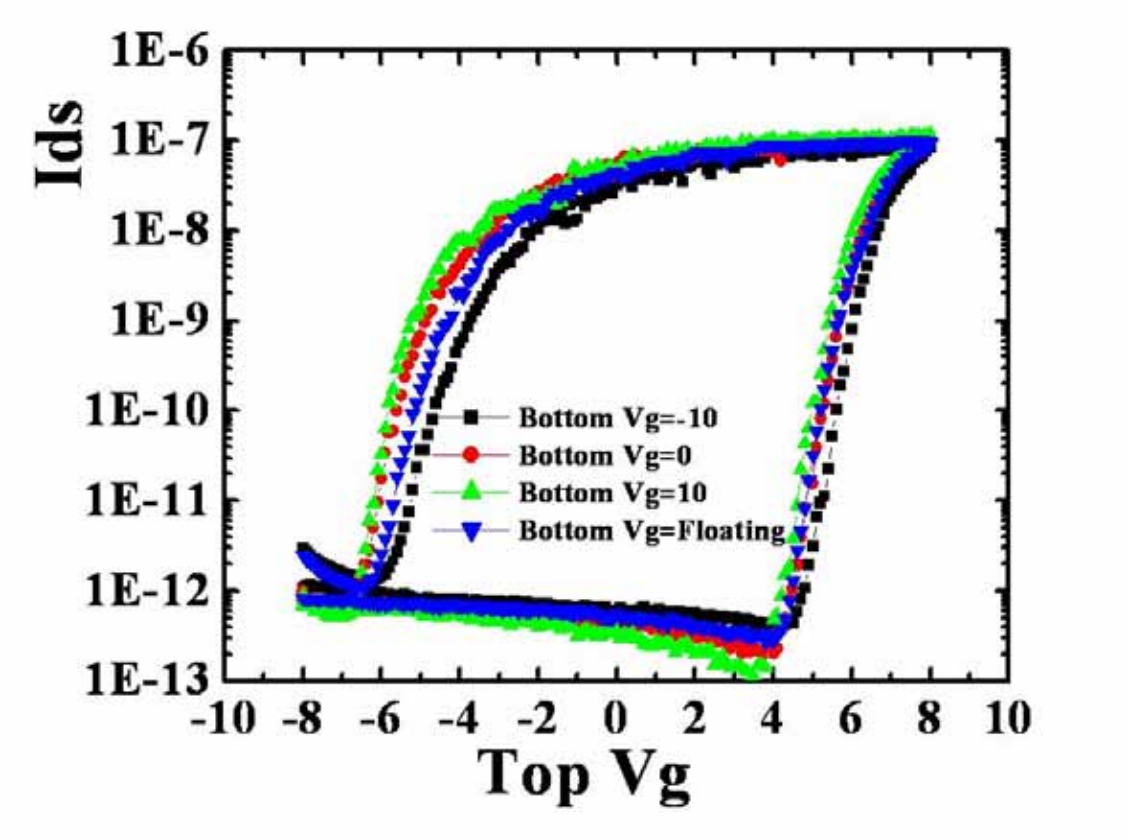


Fig. 3.8 The top-gate can be used to shift the Fermi-level of the entire CNT. This feature can be utilized to adjust Vth of DG CNT-FETs precisely.

Chapter 4

A Novel Method of Converting Metallic-Type Carbon Nanotubes to Semiconducting-Type Carbon Nanotube Field-Effect Transistors

4.1 Backgrounds and Motivation

Many kinds of CNTs have been proposed over the past decade. Among them, the single-walled carbon nanotube field-effect transistor (CNT-FET) possesses attractive properties indispensable for future nanoelectronics. For active device applications similar to the conventional FETs, the semiconducting-type, rather than the metallic-type, single-walled nanotube (SWNT) is mandatory, as only the channel conductance of the former can be modulated by the gate [1-3].

Although many studies about CNTs have been performed over the past few years, the production of SWNTs by various synthesis methods so far still yields a mixture of both types of SWNTs [4-6]. In fact, SWNTs available commercially contain about 33~60% metallic CNTs [7].

The coexistence of both types of SWNTs represents a major hurdle to many applications. It is known that the electrical characteristics of the SWNTs are strongly related to the chirality of their own structure [8-14]. If the structure of a SWNT is symmetric, it will depict metallic-type electrical behaviors.

Many techniques for screening the two kinds of SWNTs have been demonstrated [5,6,15,16]. However, most of the available screening methods are not easily compatible with integrated-circuit processes and their effectiveness is still uncertain.

Several experimental and theoretical studies show that the irradiation of CNTs with energetic particles can generate defects [17,18] and can be cleverly employed to modify the structure, shape, and chemistry of CNTs controllably. In this letter, a novel approach for bypassing the screening problem is proposed. We demonstrate the use of 20 ~180 W of Ar plasma RF power applied to the as-grown CNT-FETs and study the electrical properties of the devices. By using Ar plasma to ”burn off” the metallic-type SWNTs, only pure semiconducting-type SWNTs are retained, thus saving the trouble of resorting to complex screening methods mentioned above, and we can achieve mass-production goals easily.

4.2 Device Fabrication

The SWNT devices we fabricated in this chapter employ a separately patterned Ti layer to serve as the bottom gate of individual devices, as shown in Fig. 4.1. Briefly, a 600 nm SiO_2 field oxide layer was first grown as an insulating layer by wet oxidation at 985 ^{o}C on a 4-in. p-type silicon wafer. Then, a 150 nm Ti layer was deposited by RF sputtering, which was subsequently patterned and etched to serve as the bottom-gate metal. Subsequently, a 200 nm low-temperature plasma enhanced chemical vapor deposition (PECVD) oxide was deposited at 400^{o}C as a gate dielectric layer. Then, a properly prepared SWNT/Dimethylformamide (DMF) solution with the right density ($10{,}000/\mathrm{mm}^2$) was spun on the wafer prior to the source/drain metal lift-off process. The SWNTs for this work were purchased from Tube@Rice (by Smalley group). After blanket-coating a photoresist layer, and using a photolithographic step with a negative source/drain pattern mask to etch away the photoresist from the source/drain area, a second 150 nm Ti layer was deposited by RF sputtering at room temperature. Next, an ultrasonic machine with acetone was used

for the Ti lift-off process, leaving the second Ti film only on the Source/Drain (S/D) regions. The spacing between the source and drain electrodes was designed to be 2μm. Afterwards, a 13.56MHz transformer coupled plasma/inductively coupled plasma (TCP/ICP) metal etcher (Lam research TCP9600) was chosen as the Ar plasma source to treat the SWNTs. A commercial HP-4155A was applied to measure the I_d/V_g transfer curves of the SWNTs before and after each Ar plasma treatment.

4.3 Experimental Results and Discussion

Table 4.1 summarizes the experimental conditions and the resultant percentage of metallic CNTs and semiconducting CNT-FETs. Before Ar plasma treatment, we can see that the percentage of metallic-type SWNTs ranges from 56.5 to 73% (see Table 4.1), with only a few semiconducting-type CNT-FETs present. It is worth noting that our experience also suggests that the percentage of as-grown metallic SWNTs is strongly dependent on the characteristics of the SWNTs purchased and the concentration of the SWNT/DMF solution spun on the wafer.

Initially, the baseline recipe of etching Ti or AlSiCu in the TCP/ICP metal etcher was adopted in this work, with the RF power of 180 /160 W (top/bottom, experiments I and II in Table 4.1). However, no working devices were found. By lowering the RF power to one third (60 /55 W) of the original recipe, some functional devices were found (Experiment III in Table 4.1). Finally, by keeping the RF top/bottom power at 60W/55W, and by reducing the process time from 30 to 1 s (experiment IV in Table 4.1), 18.2% of the devices were shown to behave like p-type semiconducting CNT-FETs, albeit with a small ON/OFF ratio (< two orders of magnitude). In addition, the percentage of metallic CNTs was significantly reduced from 73 to 3%, although most of the metallic-type CNTs as well as all the devices with a high ON/OFF ratio

(≥ two orders of magnitude) were electrically open (up to 78.8%) after being subjected to such process condition.

On the basis of these data, we can conclude that both the RF power and the process time strongly affect the yield of working CNT-FETs. Eventually, we settled for an even lower RF power of 20 /20 W, and the process time was kept at 1 s (experiment V in Table 4.1). The DC bias was set at –37 V, smaller than the baseline recipe. We repeated this process three times on the same 4-in. wafer, and measured drain current-drain bias (I_d-V_d) and drain current-gate bias (I_d-V_g) each time to study the effects on the devices' ON/OFF ratio.

The results are shown in Fig. 4.2 for the (a) as-grown device, and after the (b) first, (c) second, and (d) third Ar plasma treatments. We found that for devices that show p-type semiconducting characteristics the current level is from a few nA to hundreds of nA (I_{ds} at V_g = -10 V and V_{ds} = -1 V), whereas for devices that show metallic-type characteristics the current level is on the order of 10 μA . After the first Ar plasma treatment (20 /20 W) for 1 s, the current level is reduced by 20~30 times and 2~8 times for p-type CNT-FETs and metallic-type devices, respectively. More importantly, some metallic-type devices begin to behave like p-type FET devices, albeit with a small ON/OFF ratio. From Figs. 2(a)-2(d), we can observe the transition from metallic to semiconducting CNT-FETs induced by the Ar plasma treatment. The effect of plasma treatment is evident since the corresponding transfer curve (the inset of Fig. 4.2(b)) reveals an almost two orders of magnitude ON/OFF ratio after the first Ar plasma treatment. After the second plasma treatment, it can be seen that the ON/OFF ratio increases further to three orders (Fig. 4.2(c)). The result of the third plasma treatment is shown in Fig. 4.2(d).

The as-grown p-type CNT-FETs retain their p-type FET characteristics after

repetitive plasma treatments. Fig. 4.3 shows the evolution of the electrical properties of an as-grown semiconducting-type CNT-FET (Fig. 4.3(a)) after repetitive Ar plasma treatments (Fig. 4.3(b)-(d)). After the first plasma treatment, the ON/OFF ratio drops from more than six to four orders of magnitude, as shown in Fig. 4.3(b). Both ON/OFF ratio and I_{ds} continue to drop after repetitive Ar plasma treatments, as shown in Fig. 4.3(c) after the second Ar plasma treatment, and Fig. 4.3(d) after the third Ar plasma treatment. Notwithstanding, the semiconducting-type CNT-FETs maintain their original semiconducting characteristics.

In general, the metallic-type devices with a current level greater than 50 μA are hard to convert to p-type by Ar plasma treatment. More particularly, those with mA current levels are almost impossible to convert to p-type, whereas those with a current level at a few μA are apt to become p-type after being subjected to 1~3 Ar plasma treatments. It should also be noted that the p-type devices with several tens of nA are apt to "burn out" after being subjected to 2~3 Ar ion bombardment treatments.

Although some of the metallic-type devices remain metallic, their current drops noticeably, indicating that the structure of these SWNTs has also been altered after the plasma treatments. Some of the p-type devices with an ON/OFF ratio of 2~4 orders of magnitude increases their ON/OFF ratio after the first Ar plasma treatment, but they easily become electrically open when subjected to two or more Ar ion bombardment treatments. Fig. 4.4 shows the results for 408 devices we measured each time after the 20 W/20 W/1 s Ar plasma process repetitively. We can see that the number of metallic-type devices drops significantly from 160 to 35, whereas the number of devices with ON/OFF ratios of less than 10 increases from 63 to 125, and the number of devices with 1~2 order of magnitude ON/OFF ratios increases markedly from 15 to 76. In general, when the on/off ratio of bundled CNTs is about 10~100, then less than

10 metallic SWNTs are included in the channel (i.e., the space between source and drain electrodes). Only when all SWNTs in the device channel are semiconducting can a high performance in the CNT-FETs be expected.

In short, the number of CNT-FETs with 1~3 orders of magnitude ON/OFF ratios is about 84% (compared with the original data of 33%) after the first Ar plasma treatment. These devices are suitable for use as sensors. Moreover, irradiation-induced defects could increase the chemical reactivity of CNTs [19].

In this chapter, the Ar-plasma-treated CNT-FETs exhibit different hysteresis in the electrical characteristics. Fig. 4.5 shows the shift in the transfer curves of a p-type CNT-FET after successive plasma treatments. Before Ar plasma treatment, the device shows a 6~7 orders of magnitude ON/OFF ratio. As the gate voltage is swept between –10 V and +10 V back and forth, a large hysteresis loop is generated. The threshold voltage (i.e., gate voltage Vg) of the device is shifted by more than 8 V. The shift in threshold voltage indicates that the redistribution of the charges is near the SWNTs in the underlying layer. There are four kinds of charges in the gate dielectric layer: mobile charges, trapped charges, interface trapped charges, and fixed charges. It is obvious that the first three kinds of charges will redistribute when we apply the gate voltage to the CNT-FET. However, we must also consider the injection or removal of electrons from the dielectric layer through the SWNTs or the Ti S/D electrodes [20,21]. The positive gate voltage increases the threshold voltage, which suggests that electrons are injected from the SWNTs because of the high electrical field at the nanotubes (due to the geometry of the device structure) [20].

After the first Ar plasma treatment, we observe a considerable decrease (to only 1/7 in the original hysteresis curve, and the measured data from other first-plasma-treatment devices ranges between 1/10 ~ 2/5) in the hysteresis curve (Fig.

4.5). It is worth noting that the direction of the hysteresis loop is also reversed (see the arrow in Fig. 4.5). Moreover, the hysteresis curve also changes its direction after the third Ar plasma treatment. This is because of the implantation of Ar^+ ions in the dielectric layer. All of the CNT-FETs in this work exhibit similar hysteresis curves after plasma treatment. For simplicity, we measured our samples under atmospheric pressure.

Fig. 4.6 shows the shift in the hysteresis curves of metallic CNT-FETs after successive plasma treatments. We can also observe the reversal in direction of the hysteresis loop after plasma treatment. In Fig. 4.7, we demonstrate a device that depicts minimum hysteresis (i.e., some of the hysteresis curves almost overlap each other).

To the best of our knowledge, this is the first demonstration of the conversion of metallic-type CNTs to semiconducting-type CNT-FETs by Ar plasma. According to SEM pictures of the third-plasma-treatment samples (data not shown here), if the electrical measurement data indicate that the devices are electrically open, we cannot find any CNTs linking the source and drain metal electrodes. Instead, CNT segments are found randomly everywhere. Note that all these “electrically open” devices depicted a normal field effect due to gate voltage before Ar plasma treatment as well as after the first and second Ar plasma treatments. In contrast, we can find CNTs linking between the source and drain metal electrodes in those devices that still depict a field effect after the third plasma irradiation. These observations are consistent with a literature report [22] that if the CNTs were irradiated with energetic ions, the smaller (i.e., diameter) CNTs can be thinned and sliced, whereas the larger ones reveal no observable changes (i.e., I_d remains unchanged after Ar plasma treatment).

On the basis of the Scanning Electron Microscope (SEM) observation and the

electrical measurement data, we deduce that metallic-type CNTs are more easily burned out than semiconducting-type CNTs and begin to show semiconductor behavior.

We have also proposed a plasma-induced-structure-modification model to explain the observed conversion. Previously, Osváth et al. reported that Ar^+ ion irradiation caused defects on CNTs [23]. The irradiation-induced defects appeared as hillock-like protrusions on the nanotube walls. It is therefore a mind-boggling question whether these defects will change the effective chirality of the nanotubes or not. On the basis of the SWNT band structure, the SWNT will depict metallic-type behaviors when its symmetric structure is preserved during roll-up [1,9]. When the SWNT symmetry is broken, the nanotube will instead depict semiconducting behaviors with a small band gap. This suggests that if we can alter the SWNT's symmetric structure during or after growth, high yields of semiconducting SWNTs are expected. In the literature, SWNTs grown by PECVD indeed yield a higher percentage of semiconducting-type SWNTs [24] than those grown by other CNT synthesis methods such as laser ablation, arc discharge, and low pressure chemical vapor deposition (LPCVD). This trend is consistent with our finding, as PECVD tends to induce more plasma damage on the SWNTs' structure, and therefore results in a higher percentage of semiconducting CNTs with a field effect. PECVD, however, is difficult to control. In our proposed Ar plasma treatment, the Ar plasma induces local damage and modifies the surface structure of metallic-type SWNTs. It breaks the symmetry of the SWNTs, thus converting the metallic-type SWNTs to semiconducting FETs. At the same time, the surface of as-deposited semiconducting-type SWNTs is also affected by Ar plasma, although the as-deposited semiconducting CNT-FETs still retain their p-type semiconducting behaviors. This is

because the original structure of semiconducting-type SWNTs is asymmetric, extra modification by Ar plasma treatment does not convert it to a symmetric structure, so the conduction type does not change to the metallic type, and CNT-FETs tend to retain their p-type semiconducting behaviors. Nonetheless, the SWNTs' surface is modified by Ar plasma bombardment, the extra defects will reduce the SWNTs' conductance, and the CNT-FETs' conduction current decreases after plasma treatment, as shown in Fig. 4.3. When the plasma bombardment level, including treatment time and power, reaches a critical level, the SWNTs' conduction channels are destroyed and the CNT-FETs show open-circuited I-V characteristics. On the basis of the above model, we can improve the electrical performance of CNT-FETs and other CNT devices further by optimizing the plasma treatment process.

Recently, Vijayaraghavan et al. have reported the metal-semiconductor transition in SWNTs by electron irradiation [25], and they attributed the mechanism to inhomogeneous electric fields [26] arising from charging during electron irradiation. Our results are consistent with their research because it is plausible that Ar^+ ions and some charges in our oxide layer might generate inhomogeneous electric fields that serve to break the mirror symmetry of our nanotubes and open a gap in the density of states near the Fermi level.

4.4 Summary

In this chapter, semiconducting-type CNT-FETs are realized for the first time using a simple and potentially inexpensive process. On the basis of our experimental results, we believe that the ion bombardment during Ar plasma treatment attacks both metallic- and semiconducting-type nanotubes. As long as the metallic-type CNTs that dominate the transport are broken by plasma, the resultant CNT-FETs will

unambiguously show semiconductor features. In addition, we also propose the possibility of altering the symmetry of SWNT-FETs by damaging the surface structure. In other words, the effective chirality of the SWNTs can be altered by Ar plasma treatment.

Our research efforts are now focused on further improving of the parameters of the plasma treatment process by controlling the physical conditions of our process chamber. It appears to be feasible to use plasma to treat the whole wafer directly. In doing so, the metallic-type CNTs can be converted to semiconducting FETs without adversely impacting the as-grown semiconducting FETs with a high ON/OFF ratio, as our data show that these as-grown p-type FETs can withstand the ion bombardment and retain their semiconducting characteristics.

Although the electrical performance of our non-optimum process has yet to be improved, the results are promising and suggest a viable method of producing semiconducting-type CNT-FETs. With the plasma treatment process described in this chapter, we believe it is possible (after optimization) to produce semiconducting-type CNT-FETs suitable for many applications, especially sensors. As mentioned above, the SWNTs we purchased contain a high percentage of metallic-type SWNTs, resulting in about 50~70% metallic-type CNTs in our as-grown devices. We do believe, however, that other research groups suffer from the same problem as all start with commercially-available SWNTs that are expected to be similar. Our new method allows us to treat the metallic-type CNTs with plasma after initial device measurement. Our proposed method can be implemented in two ways. First, we can identify the position of the metallic-type devices and selectively expose these devices using a standard photolithography process, and then use plasma to selectively convert them. Alternately, we can gather all the metallic-type devices after scribing the wafer into

dice, and send these metallic-behaving dice to receive plasma treatment.

References

[1] M. S. Dresselhaus, G. Dresselhaus, Ph. Avouris, *Carbon nanotubes: synthesis, structure, properties, and applications*: Springer-Verlag, 2001.

[2] A. Bachtold, P. Hadley, T. Nakanishi C. Dekker**,** "Logic circuits with carbon nanotube transistors," *Science*, Vol. **294**, Issue: 5545, p.1317, November, 2001.

[3] S. J. Wind, J. Appenzeller, R. Martel, V. Derycke, Ph. Avouris, "Vertical scaling of carbon nanotube field-effect transistors using top gate electrodes," *Appl. Phys. Lett.*, Vol. **80**, Issue: 20, pp.3817-3819, May, 2002.

[4] M. Zheng, A. Jagota, E. D. Semke, B. A. Diner, R. S. Mclean, S. R. Lustig, R. E. Richardson and N. G. Tassi, "DNA-assisted dispersion and separation of carbon nanotubes," *Nat. Mater.*, Vol. **2**, pp.338-342, May, 2003.

[5] R. Krupke, F. Hennrich, H. V. Lohneysen and M. M. Kappes, "Separation of metallic from semiconducting single-walled carbon nanotubes," *Science*, Vol. **301**, No: 5631, pp.344-347, July, 2003.

[6] Z. Chen, X. Du, M.-H. Du, C. D. Rancken, H.-P. Cheng and A. G. Rinzler, "Bulk separative enrichment in metallic or semiconducting single-walled carbon nanotubes," *Nano Lett.*, Vol. **3**, No. 9, pp.1245-1249, August, 2003.

[7] Data supplied by SWNT vendors such as Carbon Solutions, Inc., and Helix Material Solutions. Data sheets are available from their official websites.

[8] D. H. Robertson, D. W. Brenner and J. W. Mintmire, “Energetics of nanoscale graphitic tubules,” *Phys. Rev. B*, Vol. **45**, No. 21, pp.12592-12595, June, 1992.

[9] M. S. Dresselhaus, G. Dresselhaus, and R. Saito, “Carbon fibers based on C_{60} and their symmetry,” *Phys. Rev. B*, Vol. **45**, No. 21, pp.6234-6242, March, 1992.

[10] N. Hamada, S. Sawada, and A. Oshiyama, “New one-dimensional conductors: Graphitic microtubules,” *Phys. Rev. Lett.*, Vol. **68**, No. 10, pp.1579-1581, March, 1992.

[11] J. W. Mintmire, B. I. Dunlap and C. T. White, “Are fullerene tubules metallic?” *Phys. Rev. Lett.*, Vol. **68**, No. 5, pp.631-634, February, 1992.

[12] M. S. Dresselhaus, G. Dresselhaus and P. C. Eklund, *Science of Fullerenes and Carbon Nanotubes*：Academic Press, 1996.

[13] S. Berber, Y.-K. Kwon, and D. Tománek, “Unusually high thermal conductivity of carbon nanotubes,” *Phys. Rev. Lett.*, Vol. **84**, pp.4613-1616, May, 2000.

[14] A. Kleiner and S. Eggert, “Band gaps of primary metallic carbon nanotubes,” *Phys. Rev. B*, Vol. **63**, Issue: 7, p.073408, February, 2001.

[15] P. G. Collins, M. S. Arnold, P. Avouris, “Engineering carbon nanotubes and nanotube circuits using electrical breakdown,” *Science*, Vol. **292**, Issue: 5517, p.706, April, 2001.

[16] K. Kamaras, M. E. Itkis, H. Hu, B. Zhao, and R. C. Haddon, “Covalent bond

formation to a carbon nanotube metal," *Science*, Vol. **301**, Issue: 5639, p.1501, September, 2003.

[17] A. V. Krasheninnikov, K. Nordlund, M. Sirvio, E. Salonen and J. Keinonen, "Formation of ion-irradiation-induced atomic-scale defects on walls of carbon nanotubes," *Phys. Rev. B,* Vol. **63**, Issue: 24, p.245405, June, 2001.

[18] K. Kanzaki, S. Suzuki, Y. Kobayashi, Y. Ono, and H. Inokawa, "Control of electrical properties of single-walled carbon nanotubes by low-energy electron irradiation," *Solid State Devices and Materials Symp.*, pp. 772-773, Kobe, Japan, 2005.

[19] A. V. Krasheninnikov and K. Nordlund, "Irradiation effects in carbon nanotubes," *Nucl. Instrum. Methods Phys. Res. Sect. B,* Vol. **216**, pp.355-366, February, 2004.

[20] M. S. Fuhrer, B. M. Kim, T. Durkop, and T. Brintlinger, "High-mobility nanotube transistor memory," *Nano Lett.*, Vol. **2**, No. 7, pp.755-759, May, 2002.

[21] M. Radosavljevic, M. Freitag, K. V. Thadani, and A. T. Johnson, "Nonvolatile molecular memory elements based on ambipolar nanotube field effect transistors," *Nano Lett.*, Vol. **2**, No. 7, pp.761-764, June, 2002.

[22] M. S. Raghuveer, P. G. Ganesan, J. D'Arcy-Gall, G. Ramanath, M. Marshall, and I. Petrov, "Nanomachining carbon nanotubes with ion beams," *Appl. Phys. Lett.*,

Vol. **84**, No. 22, pp.4484-4486, May, 2004.

[23] Z. Osváth, G. Vértesy, L. Tapasztó, F. Wéber, Z. E. Horváth, J. Gyulai, and L. P. Biró, "Atomically resolved STM images of carbon nanotube defects produced by Ar^+ irradiation," *Phys. Rev. B*, Vol. **72**, p.045429, July, 2005.

[24] Y. Li, D. Mann, M. Rolandi, W. Kim, A. Ural, S. Hung, A. Javey, J. Cao, D. Wang, E. Yenilmez, Q. Wang, J. F. Gibbons, Y. Nishi and H. Dai, "Preferential growth of semiconducting single-walled carbon nanotubes by a plasma enhanced CVD method," *Nano Lett.*, Vol. **4**, No. 2, pp.317-321, January, 2004.

[25] A. Vijayaraghavan, K. Kanzaki, S. Suzuki, Y. Kobayashi, H. Inokawa, Y. Ono, S. Kar and P. M. Ajayan, "Metal-semiconductor transition in single-walled carbon nanotubes induced by low-energy electron irradiation," *Nano Lett.*, Vol. **5**, No. 8, pp.1575-1579, July, 2005.

[26] S. V. Rotkin and K. Hess, "Possibility of a metallic field-effect transistor," *Appl. Phys. Lett.*, Vol. **84**, No. 16, pp.3139-3141, April, 2004.

Table 4.1 Summary of experimental conditions and percentage of metallic-CNTs and semiconducting-CNT-FETs.

	RF power: top/bottom/ DC bias (W/W/V)	Substrate / chamber wall temp. (^{o}C)	Process gas (sccm)	Process time (s)	Before plasma treatment (%)		After plasma treatment (%)		Electrical open after plasma (%)
					M-type[a)]	S-type[b)]	M-type	S-type	
Experiment I	180/160 /no record	60 /60	Ar (80)/ Cl_2/BCl_3	45	65	35	0	0	100
Experiment II	180/160 /no record	60 /60	Ar (80)	45	60.6	39.4	0	0	100
Experiment III	60/55/-107	60 /60	Ar (80)	30	56.5	43.5	first : 1.6 second: 0.4	first: 0.4 second: 0	first: 98 second: 99.6
Experiment IV	60/55/-107	60 /60	Ar (80)	1	73	27	first: 3	first:18.2	first: 78.8
Experiment V	20/20/-37	60 /60	Ar (80)	1	60.8	39.2	first: 13 second: 8 third: 8	first: 83 second: 75 third: 68	first: 4 second: 17 third: 24

[a)]M-type stands for metallic-type CNT. [b)]S-type stands for semiconducting-type CNT-FET.

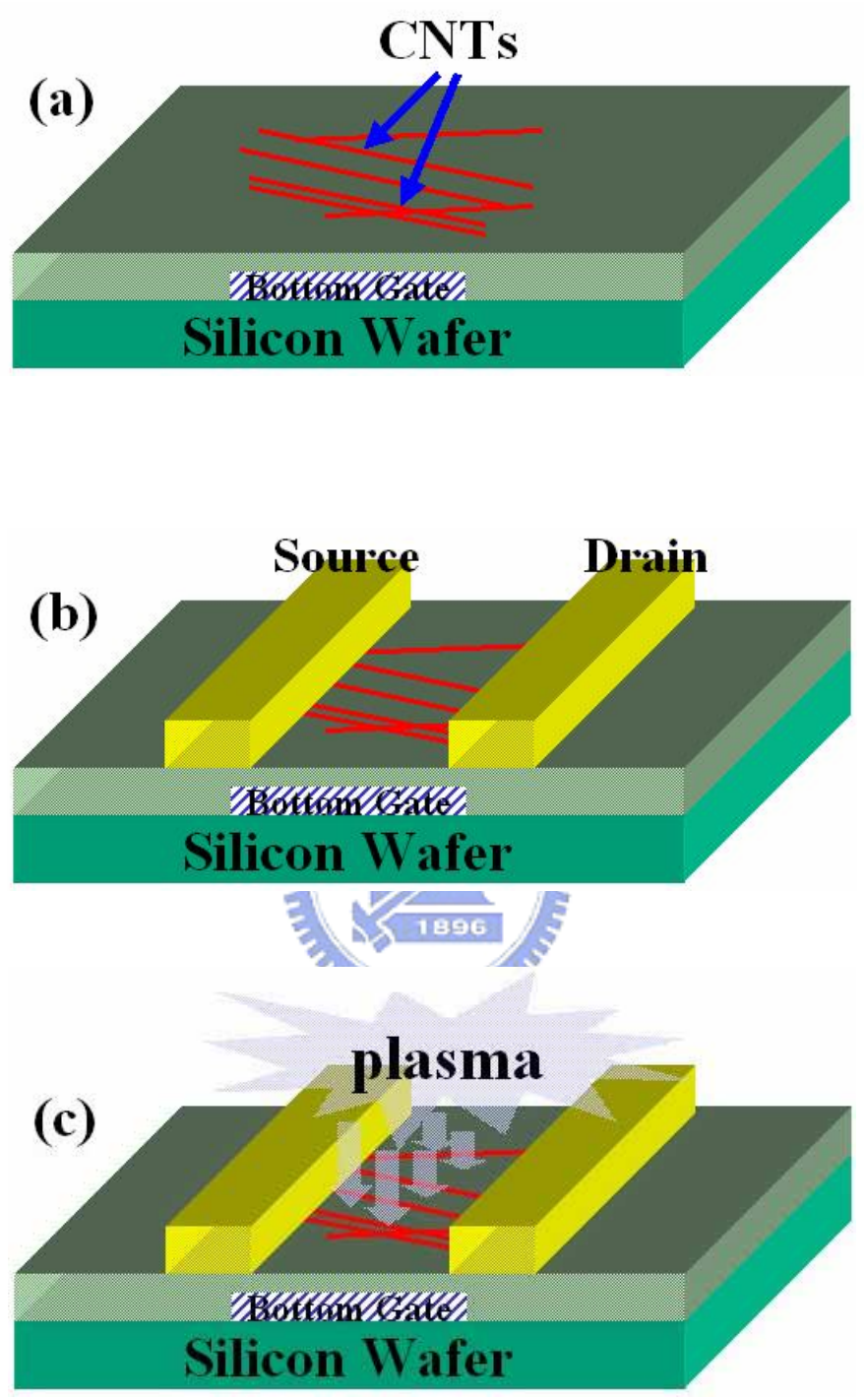


Fig. 4.1 Process flow of CNT-FETs. (a) Properly prepared SWNT/DMF solution spun on the wafer, (b) Source/drain metal lift-off process, and (c) Ar plasma treatment.

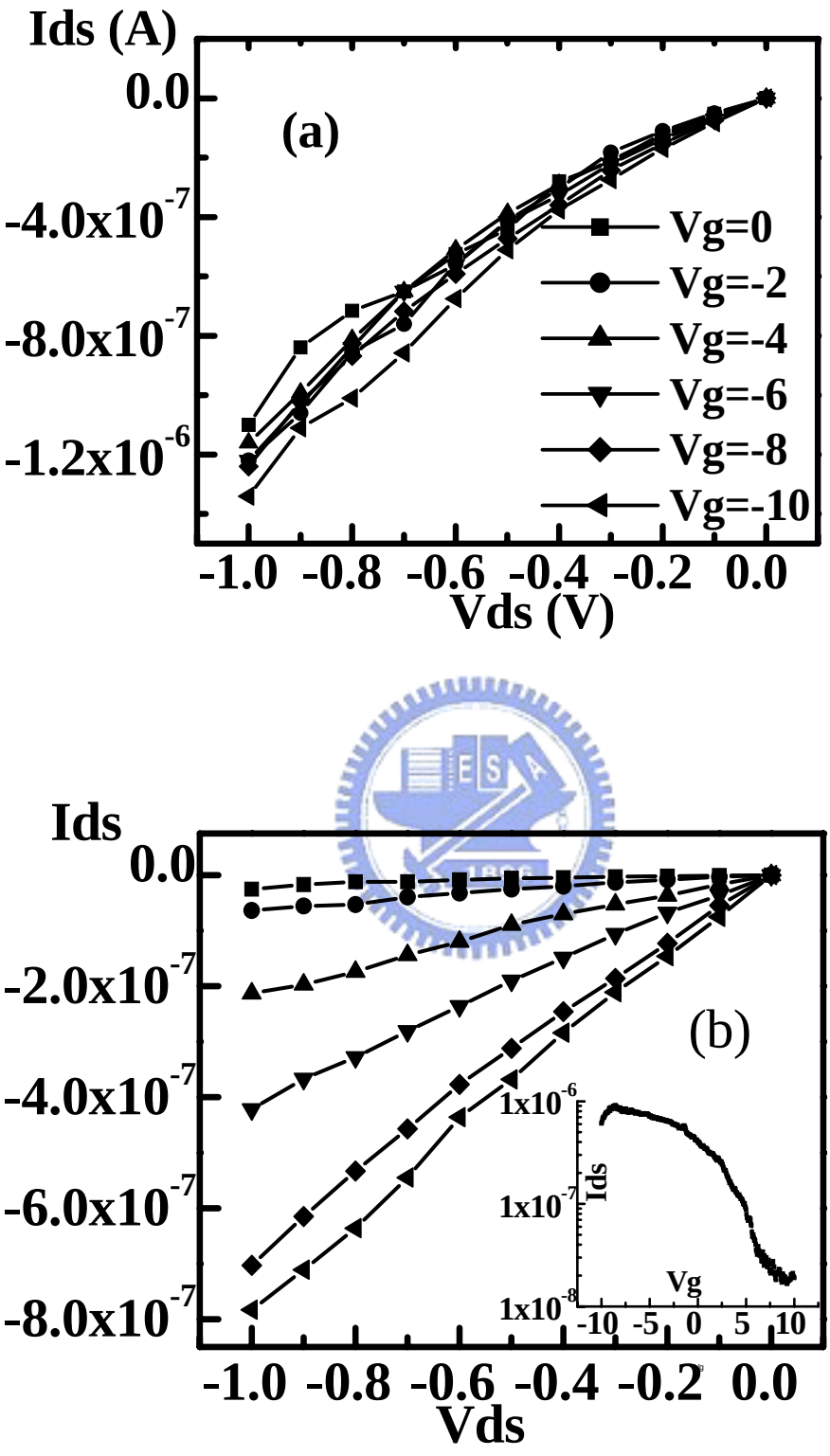


Fig. 4.2 Ids-Vds characteristics of (a) an as-grown metallic-CNTs, (b) after first Ar plasma treatment under 20 W/20 W/1 s conditions. Insets show the corresponding transfer characteristics.

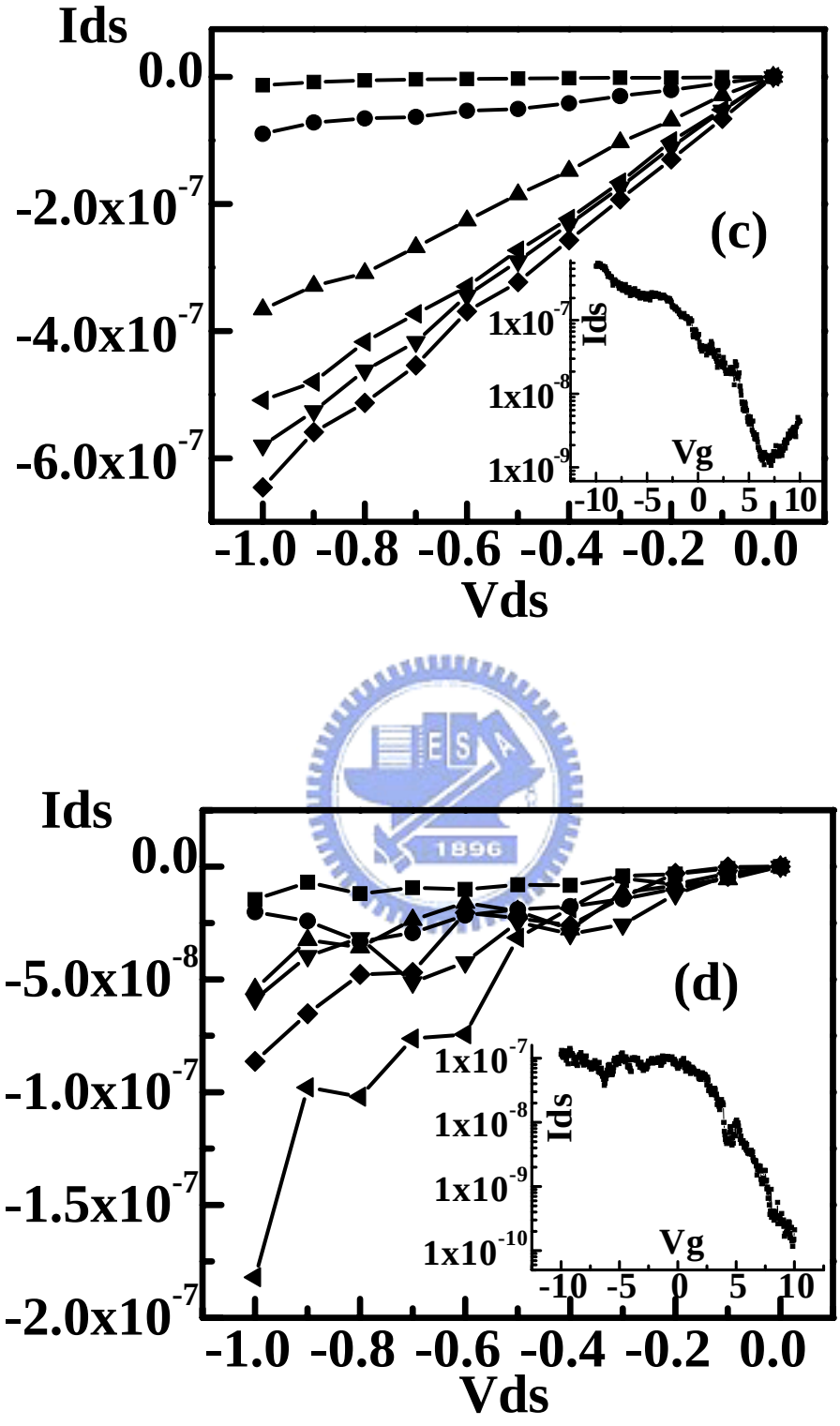


Fig. 4.2 Ids-Vds characteristics of (c) after second Ar plasma treatment under 20 W/20 W/1 s conditions, and (d) after third Ar plasma treatment. Insets show the corresponding transfer characteristics.

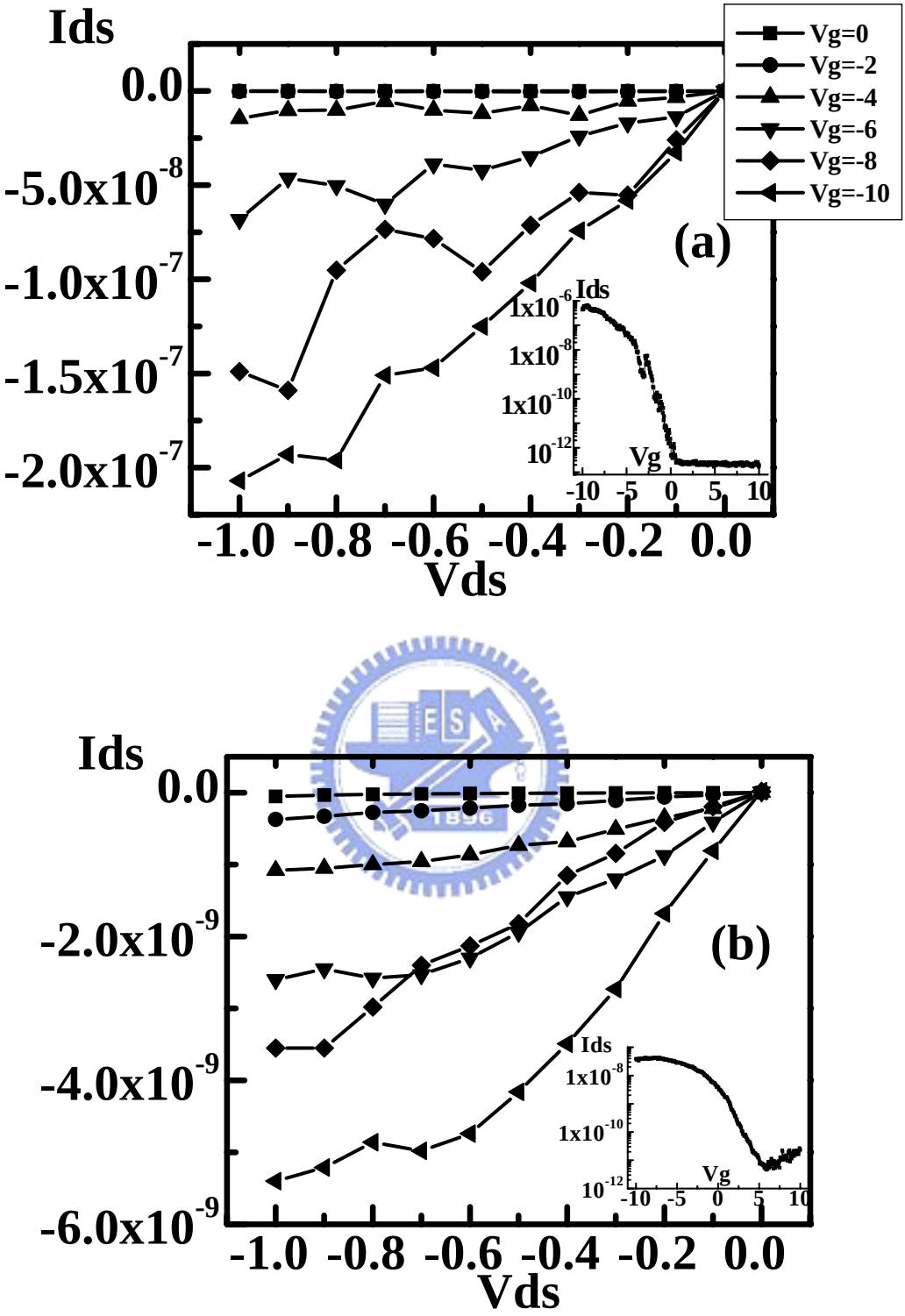


Fig. 4.3 Ids-Vds characteristics of (a) as-grown p-type semiconducting CNT-FETs, (b) after first Ar plasma treatment under 20 W/20 W/1 s conditions. Insets show the corresponding transfer characteristics. Note that the as-grown p-type characteristics are preserved after plasma treatments.

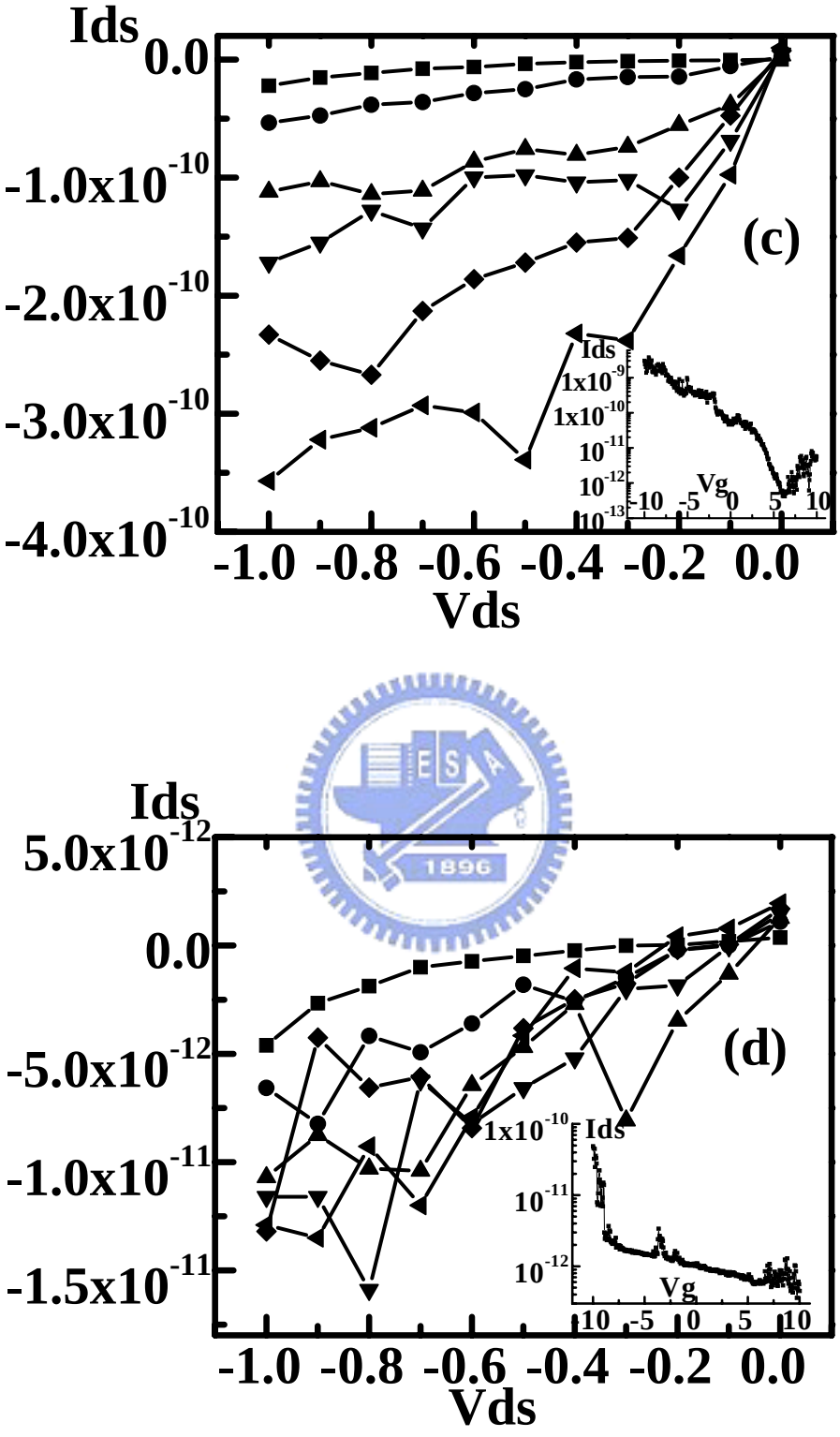


Fig. 4.3 Ids-Vds characteristics of (c) after second Ar plasma treatment under 20 W/20 W/1 s conditions, and (d) after third Ar plasma treatment. Insets show the corresponding transfer characteristics. Note that the as-grown p-type characteristics are preserved after plasma treatments.

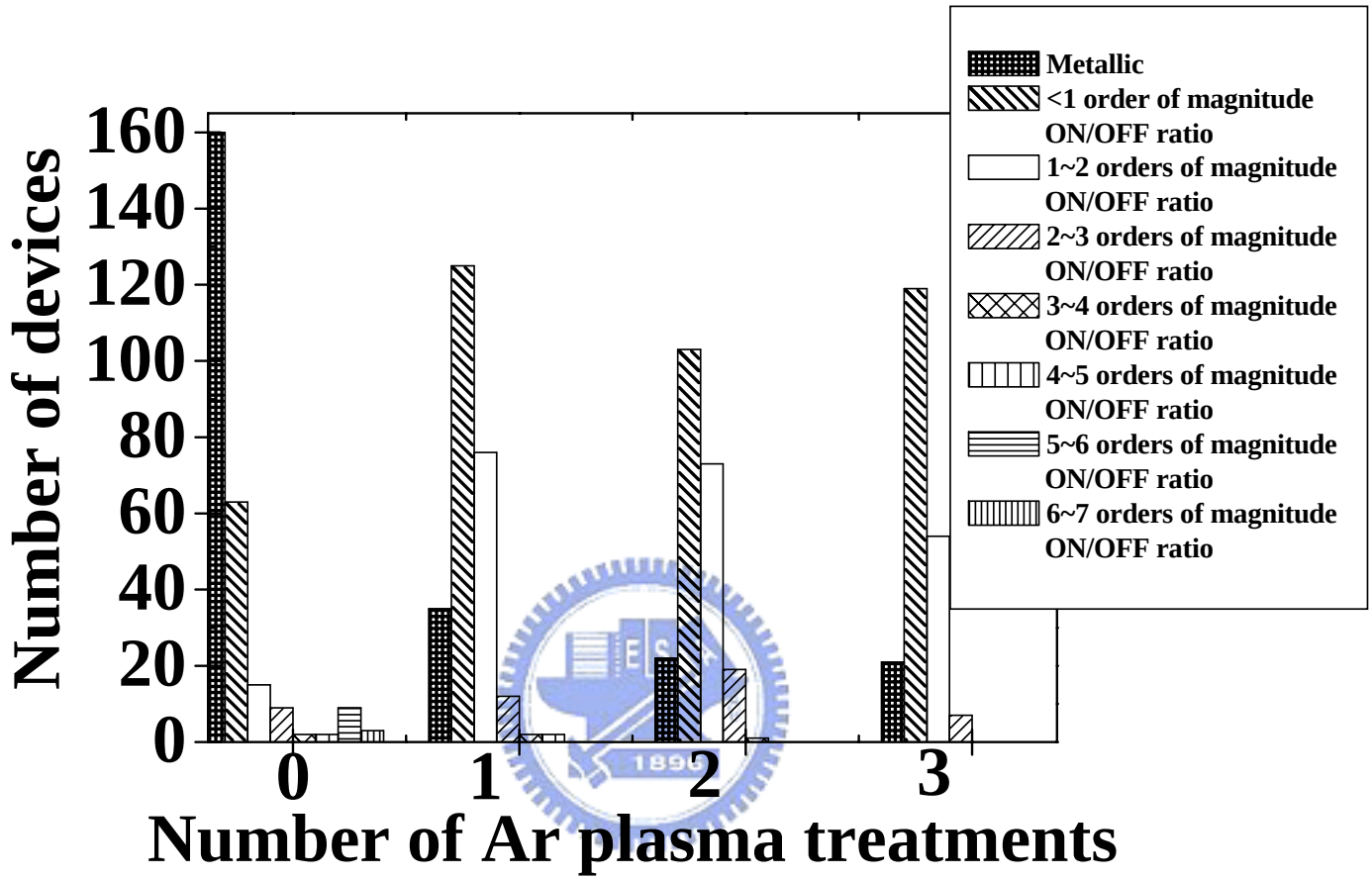


Fig. 4.4 Measured results for 408 devices after repetitive 20 W/20 W/1 s Ar plasma treatments. The number of metallic-type CNTs drops abruptly after plasma treatment, whereas devices with ON/OFF ratios less than 10 increase considerably, and devices with 1~2 order of magnitude ON/OFF ratios also increase markedly from 15 to 76 devices. In short, devices with 1~3 order of magnitude ON/OFF ratios are about 84% (compared with the original data of 33%) after the first Ar treatment.

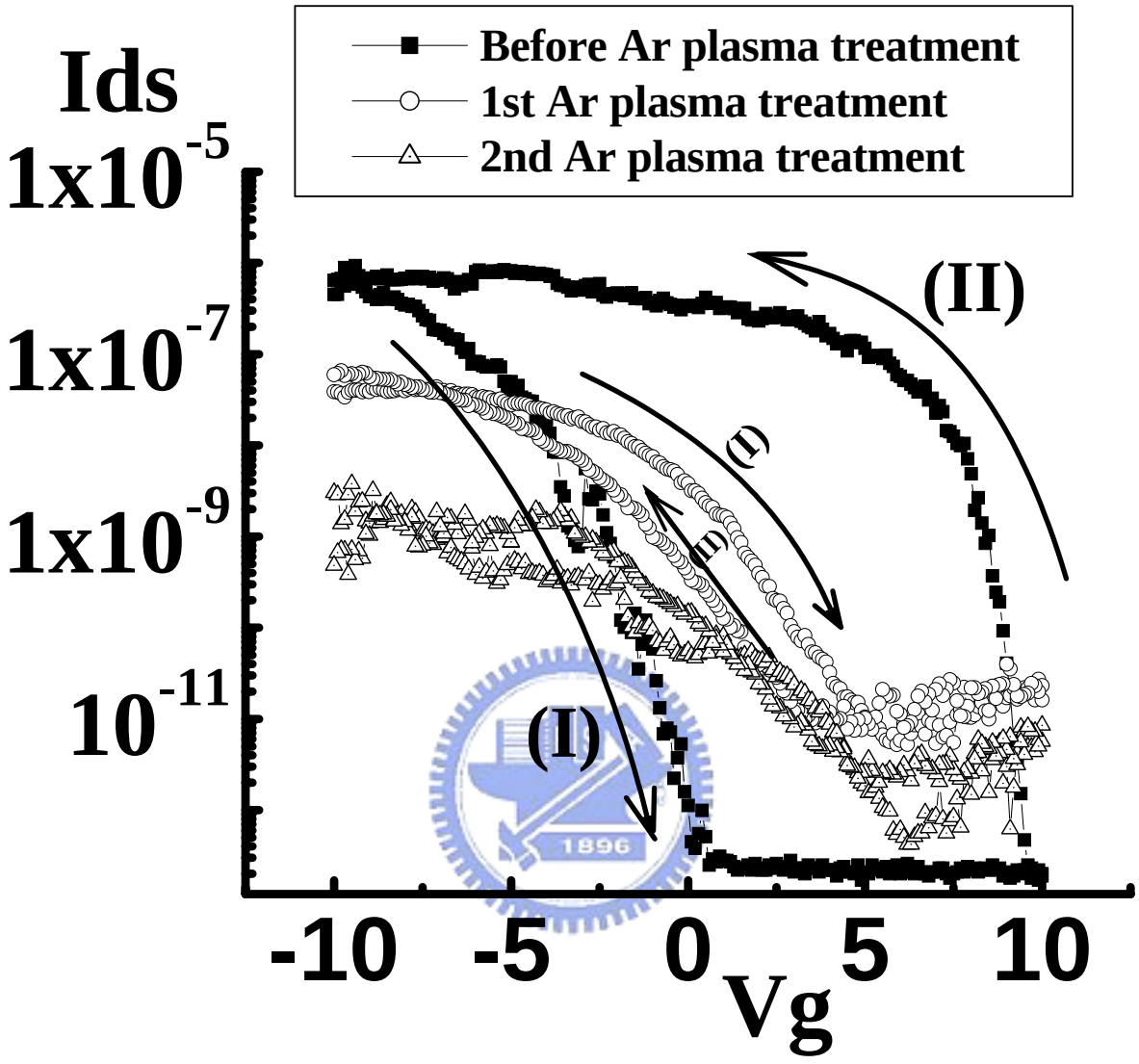


Fig. 4.5 Shift in transfer curve of CNT-FET after successive plasma treatments. The gate voltage is swept (I) from –10 to +10 V, and (II) from +10 to –10 V. After the first Ar plasma treatment, we can observe a considerable decrease (only 1/7 of the original hysteresis curve) in the hysteresis curve. Note that the direction of the hysteresis loop is also reversed. In addition, the hysteresis loop changes its direction after the 3rd Ar plasma treatment.

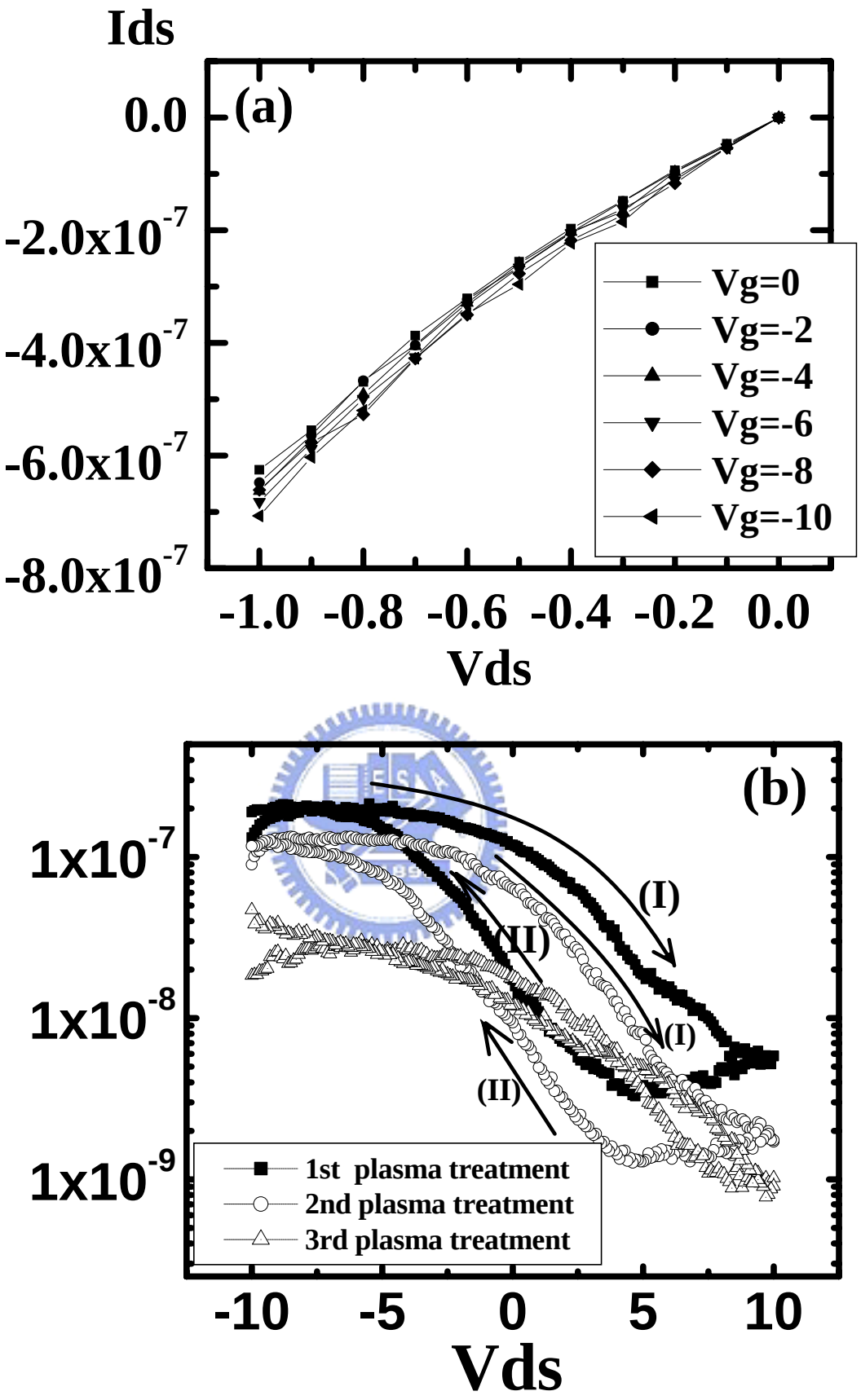


Fig. 4.6 Shift in hysteresis curves of metallic CNT-FET after successive plasma treatments. We can also observe the reversal in the direction of the hysteresis curve after plasma treatment.

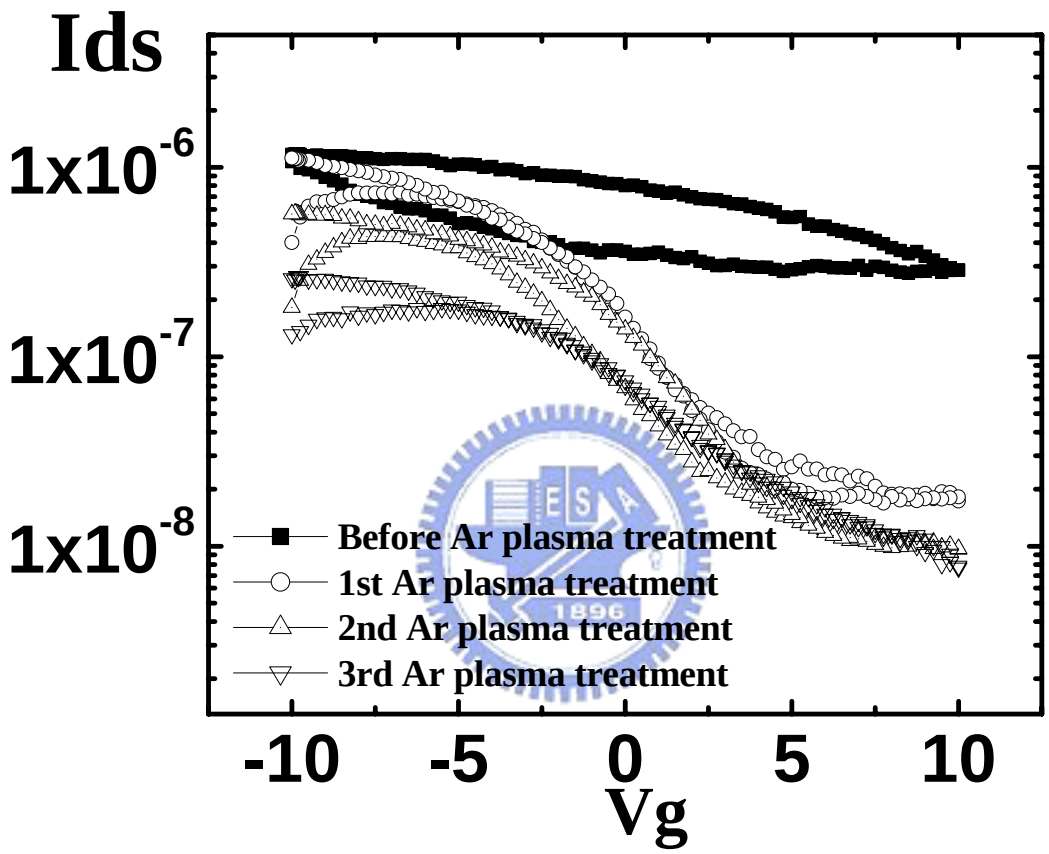


Fig. 4.7 Demonstration of a device without large hysteresis curve. Note that some of the hysteresis curves almost overlap each other.

Chapter 5

Prospects of Cobalt-Mix-TEOS Method on Localized Lateral Growth of Carbon Nanotubes for Both P- and N-Type Field Effect Transistors

5.1 Backgrounds and Motivation

Although carbon nanotube has several impressive electrical properties [1], there are challenges before their adoption to many practical applications. Especially the process compatibility with the existing silicon-based semiconductor technologies, controlling the placement and manipulation of massive numbers of CNTs at precise locations, the chirality of the CNTs, and the manufacturing of both n- and p-type CNTs simultaneously on the same substrate. To use CNTs as a replacement building block for silicon-based devices, millions or billions of nanotubes must be placed accurately over the chip. It is obvious that the tedious physical manipulation of numerous nanotubes one at a time is impractical for mass production. A number of techniques have been proposed to achieve a regular CNT network by controlling the gas flow direction [2], using porous templates [3], using electric-field-assisted assembly [4,5], utilizing chemically functionalized template [6], adopting fluidic alignment [7,8], or using electric-field-directed-growth of CNTs [9]. Although these methods all achieve acceptable results in both the growth direction and the length of CNTs, they require additional equipments [10]. It is obvious that the aligned-CNT-growth methods [11,12] are more promising than post-growth-assembly-of-CNT methods for CNT-FETs.

In this chapter, we demonstrate the growth of bundled-CNTs for CNT-FETs

with only Co particles as catalyst [13,14] and ethanol as carbon source. Some previous reports also indicated that CNTs manufactured by CVD methods with Co catalyst usually resulted in predominantly multi-walled tubes [15,16]. In this chapter, our reiterative and systematic experiments show that the selective growth of bundled-CNTs produces mostly SWNTs.

In order to obtain semiconducting-type SWNTs, the catalyst size should be reduced to as small as possible [13]. In this work, a method is proposed to synthesize SWNTs and form bridged-CNTs between two catalyst islands. The characteristics of embedded Co nanoparticles in patterned cobalt-mix-tetraethoxysilane (CMT) islands for SWNT growth are discussed under different hydrogen reduction conditions, catalyst concentrations, and carbon ratios during CNT growth in this chapter.

It is also necessary to fabricate n-type, in addition to p-type CNT-FETs, on the same chip for the complementary circuits. In general, the CNT-FET acts like a p-type conduction device when the CNT is exposed to air [17-21]. Several approaches have been previously reported to form n-type CNT-FETs by employing complex doping processes [22-24] or thermal/electrical annealing processes [25]. These approaches, however, require extra processing and masking steps to convert generic p-type CNT-FETs in vacuum or in the inert gas. In contrast, no extra annealing steps are needed to form air-stable n-type CNT-FETs [26-28] using the passivation method proposed in this chapter.

5.2 Device Fabrication

5.2.1 Preparation of cobalt-mix- tetraethoxysilane solution and formation of catalyst islands

First, 25ml tetraethoxysilane (TEOS, reagent grade) was added into 25ml

absolute alcohol (ethanol) and slowly stirred for 20 ~ 30 minutes, then 1.5M Co^{2+} ($Co(NO_3)_2 \cdot 6H_2O$ + ethanol) solution was added slowly over 90 minutes by using clean burette (~ 10ml/90 min @ $23 \pm 2\,^{o}C$ and relative humidity: $43 \pm 5\%$ in class 10 clean room). After adding Co^{2+}, cares were taken to protect the solution from moisture, and the solution was stirred slowly for over 24 hours. It should be noted that if the solution was exposed to moisture or stirred unevenly, the CMT film would crack easily after the 1st 133°C soft bake as shown in Fig. 5.1(a). Fig. 5.1(b) shows that lots of Co particles are aggregated together if the stir time is shortened to about 12 hours. Fig. 5.1(c) shows that the Co particles will disperse well if the CMT solution is stirred long enough under well-controlled environment.

Fig. 5.2 illustrates a bridged-CNT FET process flow of the proposed CMT method. In order to fabricate CNT-FETs, the gate dielectric layer under the CNT channel must first be considered. Different gate dielectric layers would exhibit different surface characteristics and the choice of this layer would be critical for the dispersion of the CMT solution. In the proposed process, a 600 nm field oxide (SiO_2) layer was first grown as an insulating layer by wet oxidation at $985\,^{o}C$ on the 4-inch p-type silicon wafers. Then, a 300-350 nm n^+-poly silicon layer was deposited by LPCVD, and subsequently patterned and etched to serve as the bottom-gate electrodes. Afterwards, another oxide or nitride layer was grown on the wafers to serve as the gate insulator (Fig. 5.2(a)). Then the CMT solution was spun onto the gate dielectric layer as the catalyst layer. The oxidation and activation of the CMT layer were carried out by a pre-bake at 133°C in the atmosphere, followed by a hot-bake at 550°C in argon (Ar) environment. After the annealing process, the catalyst islands were patterned on the CMT layer by using standard lithography and dry/wet etching processes (Fig. 5.2(a)).

5.2.2 Growth of carbon nanotubes

The growth of CNTs was conducted in a customized quartz tube reactor placed in a horizontal tubular furnace. After the formation of catalyst islands described in Section 2.1, wafers were heated in pure H_2 for 5 ~ 15 minutes at 550°C to convert Co^{2+} to metal particles. Then the process temperature was raised to 850°C in Ar at a flow rate of 5000 sccm, and subsequently ethanol was introduced into APCVD furnace as the carbon source with Ar as the carrier gas at a flow rate of 3500 ~ 5000 sccm for 40 minutes in ambient atmosphere. After completion of the reaction, the power was turned off and the reactor was cooled down under flowing Ar. Finally, the suspended CNTs were grown between two neighboring catalyst islands by APCVD with ethanol/Ar (Fig. 5.2(b)).

After blanket-coating a photoresist layer, and using a photolithographic step with a negative source/drain (S/D) pattern mask to etch away the photoresist from the S/D area, a titanium (Ti) layer was deposited by radio frequency (RF) sputtering at room temperature. Next, an ultrasonic instrument and acetone were used for the Ti lift off process, leaving the Ti film only on the S/D regions (Fig. 5.2(c)). The spacing between the source and the drain electrodes was designed to be 2μm (i.e., the channel length of the devices).

A commercial HP-4155A was applied for measuring the I_d-V_g transfer curves and I_d-V_d of the CNT-FETs. The raw nanotubes were examined by high-resolution transmission electron microscopy (TEM, JEOL JEM 2000EX).

5.3 Experimental Results and Discussion

5.3.1 Transition metal contamination

Since an IC-compatible process is highly desirable, we adopt a standard IC

process to manufacture our catalyst islands and grow the CNTs. However, the catalyst metals, which belong to the transition metals, can potentially contaminate the expensive semiconductor equipments. As such the foundry is usually reluctant to allow such materials to enter their production lines. When the dimensions of integrated circuits become smaller, the thickness of the gate oxide is being reduced to virtually atomic levels. With oxide thicknesses being less than a few tens of angstroms, the metal impurities can have serious effects on the oxide properties. Generally, transition metals, such as Fe, Co, Ni are commonly used as catalysts for carbon nanotube growth. Unfortunately, these transition metals can be unintentionally left on the surface of the chamber at a number of processing steps including wet chemical etching, dry etching, photolithography and chemical vapor deposition. Therefore, trace transition metals analysis has become essential for the development of CNT processes that are compatible with silicon circuit technologies.

In order to clarify the contamination issue, monitors were set up to measure the cobalt ion concentration in the process chambers (including loadlock chambers and robot arms). The key machines monitored included dry etchers and the CVD machine (Table 5.1). In addition, particle levels were also monitored in our I-line stepper, chemical stations, and spin dryers. The monitor results showed that the monitored particle levels were quite normal (within specification). In our study, VG-PQ3, an inductively-coupled plasma-mass spectrometer (ICP-MS), was used to analyze the monitor wafers which were processed by the semiconductor equipments in question. From Table 5.1, we can conclude that no noticeable increase in cobalt ion concentration is observed.

5.3.2 The diameter of cobalt catalyst

Fig. 5.3(a) shows the TEM picture of Co catalyst distribution in CMT powder. The diameters of the embedded Co catalysts range from 10 to 20 nm, which is a parameter crucial to confining the width of the CNTs. Fig. 5.3(b) demonstrates the bundled-SWNTs that were synthesized from CMT powders with a diameter of 10 nm. After the SWNTs were grown, some bridged SWNTs were found between the CMT powders, as shown in Fig. 5.3(c). These results suggest that the CNT bundle can indeed be naturally bridged between two CMT catalyst islands. It is worth noting that the diameters of Co catalysts are strongly related to the formation procedure of CMT described in Section 2.1 such as the stir time and process environment.

5.3.3 The adhesion of CMT layer on different bottom-gate dielectric layers

In this chapter, we investigate the dispersion/adhesion of our CMT on different bottom-gate dielectric layers (i.e., either thermal oxide or nitride). Fig. 5.4 shows that the CMT can disperse/adhere well and can be patterned well (by dry etching), as evidenced by the vernier structure (i.e., the Arabic numerals in the SEM pictures is an indicator for the resolution of photolithography and the finest pattern after dry etching) on thermal oxide layer. Unfortunately, the oxide bottom-gate dielectric layer with its hydroxyl (-OH) bonds is undesirable for many biosensor applications. To avoid the complication of hydroxyl bonds, nitride in lieu of oxide can be adopted as the bottom-gate dielectric layer. However, our data show that the adhesion of CMT layer on nitride is quite poor (Fig. 5.4(b)), so the direct spinning of the CMT solution on nitride film is not practical. In this work, we found that by adding a hexamethyldisilazane (HMDS) layer on the nitride film before spinning the CMT, good CMT catalyst islands can be formed on the nitride layer for biosensor purposes

(Fig. 5.4(c)).

5.3.4 Effects on CMT patterns by using dry or wet etching process

Fig. 5.5 illustrates the effects on the CMT patterns when growing CNTs using either dry or wet etching process. Fig. 5.5(a) shows the cross-sectional SEM picture of a pattern by dry etching. It can be seen that a suspending CNT is formed between the CMT patterns. In addition, sidewall polymers, which are frequently produced in the dry etching process, can be found all over the trench. These sidewall polymers will inhibit the formation of the CNTs. In contrast, no obvious polymer is found in the wet etching process by BOE (5:1) (buffered oxide etch solution, six parts 40% NH_4F and one part 49% HF), as shown in Fig. 5.5(b). Nevertheless it is known that the control of the pattern profile and gap is quite poor in the wet etching process because of the isotropic etching nature. Since the CMT layer is vulnerable to severe over-etching because of its porosity, we eventually adopt a standard reactive ion etching (RIE) dry etching process for the formation of the catalyst islands.

In this work, post-etch cleaning was employed to remove the sidewall polymer (i.e., residue) and some cobalt/CMT debris spreads everywhere. In order to quantify the amount of the residue, we applied a voltage to two random positions on the blanket portion of the wafer and measured the current. In general, the current was expected to be very small (i.e., less than pico-ampere) on the blank region theoretically. Fig. 5.5(c) shows the distribution of leakage current level on the blanket portion of the wafer without receiving any post treatment after using dry etcher to form the catalyst islands. Fig. 5.5(d) indicates that the leakage current is in tens of μA range around the wafer center. Moreover, the dice with the leakage current in the μA range account for about 33.3% of the total dice (17 out of a total of 51dice). We

believe the high leakage current is caused by the conducting residues or the incomplete etching of the conducting CMT layer at the center of the wafer because the CMT is much denser there, so the wafer surface becomes conductive and the leakage current reaches the μA range (compared with the insulator whose current level should fall in the pico-ampere range). The high leakage on the wafer surface could result in the malfunction of the transistors. In order to minimize the leakage current, post treatment (i.e., descum process) after our dry etching process is necessary to remove these residues. To effectively remove the residue, the thickness of bottom-gate dielectric layer was increased and the over-etching time of our dry etching was prolonged.

5.3.5 Other factors that affect the length of CNTs

For CNT-FET applications, vertical distribution and lateral growth of CNTs by the proposed CMT method are critical and must therefore be studied thoroughly. It should be noted, however, that the length of the CNT is also important for some device applications. These include bio-sensors and dual/multiple-gated devices where longer CNT bundles are necessary.

In our reiterative experiments, the major parameter that affects the CNT length and the CNT tip-growth rate is found to be the concentration of carbon atoms. This parameter can be controlled by adjusting the reactive gas ratio (ethanol to Ar) [16]. Fig. 5.6(a) shows the results of the CNT length versus the composition of the reaction gas. For a given Ar flow rate of 5000 sccm, the length of CNT increases as the ethanol to Ar ratio increases from 0.25 to 0.5. This is ascribed to more carbon atoms being carried to the surface of the cobalt catalyst. A higher carbon concentration within the cobalt-carbon mixed catalyst will probably increase both the growth rate and the

length of the CNTs. However, when the ethanol/Ar ratio approaches unity, it is found that the CNT length does not increase any further, perhaps due to the accumulation of excess carbon atoms on the catalyst nanoparticles that eventually poison the catalysts. When the total gas flow rate reduces from 5000 to 3500 sccm, the length of CNT increases to greater than 4.5 μm. Since our APCVD chamber pressure remains unchanged, when the gas flow rate is decreased, the exhaust speed is also reduced simultaneously. Consequently, the carbon atoms can stay much longer around the Co catalyst. Therefore, the solubility of carbon atoms into the Co increases, resulting in the increase of the growth rate and the length of the CNTs. Under this process condition, a CNT is found to bridge the 6μm-gap, as shown in Fig. 5.8(b).

Besides controlling ethanol/Ar ratio of the reactive gas, the density of CNTs can be tuned by the concentration of Co^{2+} ion in the CMT solution. Figs. 6(b) and 6(c) show SEM images of the CNTs grown by different Co^{2+} concentrations of 1.5 M and 0.5 M, respectively. When the Co^{2+} concentration is 1.5 M, the CMT solution is more viscous, and the final thickness of catalyst islands is about 150 nm. The resultant density of the CNTs is higher as shown in Fig. 5.6(b), in which CNTs grow on the catalyst islands' sidewalls. However, when the Co^{2+} concentration is reduced to 0.5 M, the viscosity of the CMT solution is reduced and the thickness of the catalyst layer reduces to 20 nm. Obviously the density of the CNTs grown by the 0.5 M CMT solution is lower, and all the CNTs are located just in one single layer, as shown in Fig. 5.6(c).

In our experiments, for longer hydrogen (H_2) reduction time, the growth mechanism favors the base-growth-type CNT. While for shorter hydrogen reduction time, the growth mechanism favors the tip-growth mechanism (Fig. 5.7), resulting in longer CNTs. So it appears that H_2 reduction time also plays a role on activating the

Co particle as catalyst in our CMT method. This result is not consistent with other group who used Co and carbon monoxide to synthesize CNTs.

The effects of the process gas flow direction in the APCVD quartz tube were also investigated in this chapter, no obvious difference was found when the gas flow is in either X- or Y-direction (Fig. 5.4(a)).

5.3.6 Performance of CNT-FET devices

Out of a total 1173 devices produced on one test wafer, 493 metallic bundled-CNTs (42.03%), 204 semiconducting-type CNT-FETs (17.39%) with an on/off ratio of less than or equal to two orders, and 17 semiconducting-type CNT-FETs (1.45%) with an on/off ratio ranging from two to six orders, were obtained in this study. It is worth noting that in a batch of as-grown CNTs, both metallic and semiconducting type CNTs were present [17]. When at least one metallic CNT is included in the bundle, the bundled-CNTs would show a gradual transition to metallic character. It is plausible that if the number of metallic CNTs is small, the bundled-CNTs will still exhibit weak semiconducting characteristics. On the contrary, if the number of metallic CNTs is large, the bundled-CNTs will show metallic characteristics. In general, when the on/off ratio of our CNT-FETs is about 10 ~ 100, less than 5 ~ 10 metallic CNTs are included in the channel (i.e., the space between two catalyst islands). Only when all CNTs in the bundle are semiconducting can a high performance in the CNT-FETs be expected.

Since our bundled-CNTs were exposed to the air (Fig. 5.2(c)), all the as-grown CNT-FETs manufactured in this study were p-type semiconducting in nature [29,30]. Fig. 5.8(c) shows the electrical properties (i.e., I_d-V_d and I_d-V_g) of an as-grown p-type CNT-FET with five orders of on/off ratio. The bottom-gate voltage applied in Fig.

5.8(c) varies from 0V to -10V (at a step of -2V) at Vds = -1V. It should also be noted that the CNT-FETs with one to two orders of on/off ratio are rendered acceptable to serve the role of sensors. However, in order to manufacture complementary CNT-FET structure (similar to conventional silicon-based CMOS devices) for broader applications, n-type CNT-FETs are indispensable. Previously, our group has successfully manufactured air-stable n-type CNT-FETs [26-28] without resorting to any additional and complex annealing process. After measuring the electrical properties of some wafers that depict generic p-type CNT-FETs in this work, a 300 ~ 400nm-thick silicon nitride film was deposited on the wafer as passivation layer by PECVD at 390^{o}C. Afterwards, the contact holes of the source/drain and bottom-gate regions were etched in the same MERIE dry etcher. Our experimental data confirmed that the generic p-type CNT-FETs are converted to air-stable n-type CNT-FETs, as shown in Fig. 5.8(d). The converted n-type CNT-FETs depict one to four orders of on/off ratio when the bottom-gate is biased from 0V to 10V (at a step of 2V) at Vds = 1V. This is ascribed to the use of PE-nitride film as the passivation layer whose deposition temperature is high enough to simultaneously remove the oxygen atoms from the CNTs or CNT/metal interface in the PE-CVD deposition chamber. The approach offers a feasible method to fabricate air-stable n-type CNT-FETs by converting the generic p-type CNT-FETs.

It is worth noting that theoretically both n- and p-type CNT-FETs can be fabricated on the same chip by selectively converting some of the generic p-type CNT-FETs on the chip, while leaving other p-type CNT-FETs on the same chip untouched. The design of a new photo mask set is currently under way which will allow us to test the feasibility of the idea.

Although the device performance of our proposed process has yet to be

optimized, our initial results are encouraging and suggest a viable method of fabricating functional CNT-FETs. Using the CNT growth method proposed in this chapter, we believe it is possible, with further process refinement, to manufacture semiconducting-type CNT-FETs suitable for many applications, especially sensors. As mentioned above, the CNTs synthesized in this study contain a high percentage of metallic-type CNTs, representing about 42.03% of metallic bundled-CNTs out of the total as-grown devices. We do believe however that after optimizing the growth conditions and applying plasma treatment on the as-grown CNT-FETs, a much higher percentage and a higher on/off ratio of semiconducting-type CNT-FETs are achievable [31].

5.4 Summary

To the best of our knowledge, only SWNTs can show the semiconducting-type behaviors. And judging from our electrical measurement results and TEM pictures (Fig. 5.3(b)), we deduce that the CNTs we synthesized are mostly bundled-SWNTs. This result is also consistent with earlier study [32].

In order to synthesize long CNTs, it is critical to balance the rate of ethanol decomposition and the rate of carbon atom diffusion. In other words, the carbon supply route needs to remain open during processing. The rate of carbon diffusion will be dominated mostly by the temperature, and the ethanol decomposition rate will be affected by both the synthesis temperature and the flow rate of the carrier gas (Ar).

In short, we have developed an integrated circuit (IC) compatible process for fabricating CNT-FETs successfully with a shorter hydrogen reduction time in this study. Longer CNT length can be obtained by optimizing carbon ratio during synthesis, and the accumulation of carbon on the catalyst tip can be controlled by

mixing inert gas with the carbon source. This IC compatible process seems to be promising for fabricating a pre-aligned single-walled carbon nanotube matrix for both n- and p-type CNT-FETs.

References

[1] B. Q. Wei, R. Vajtai, and P. M. Ajayan, “Reliability and current carrying capacity of carbon nanotubes,” *Appl. Phys. Lett.*, Vol. **79**, Issue: 8, pp.1172-1174, August, 2001.

[2] S. Huang, X. Cai, C. Du, and J. Liu, “Oriented long single walled carbon nanotubes on substrates from floating catalysts,” *J. Phys. Chem. B*, Vol. **107**, No. 48, pp.13251-4, December, 2003.

[3] S. Fan, M. G. Chapline, N. R. Franklin, T. W. Tombler, A. M. Cassell, and H. Dai, “Self-oriented regular arrays of carbon nanotubes and their field emission properties,” *Science*, Vol. **283**, Issue: 5401, p.512, January, 1999.

[4] P. A. Smith, C. D. Nordquist, T. N. Jackson, T. S. Mayer, B. R. Martin, J. Mbindyo, and T. E. Mallouk, “Electric-field assisted assembly and alignment of metallic nanowires,” *Appl. Phys. Lett.*, Vol. **77**, Issue: 9, pp.1399-1401, August, 2000.

[5] K. Yamamoto, S. Akita, and Y. Nakayama, “Orientation and purification of carbon nanotubes using ac electrophoresis,” *J. Phys. D: Appl. Phys.*, Vol. **31,** No. 8, pp.L34-L36, April 1998.

[6] J. Liu, M. J. Casavant, M. Cox, D. A. Walters, P. Boul, W. Lu, A. J. Rimberg, K. A. Smith, D. T. Colbert, and R. E. Smalley, “Controlled deposition of individual single-walled carbon nanotubes on chemically functionalized templates,” *Chemical Physics Letters*, Vol. **303**, Issue: 1-2, pp.125-129, April, 1999.

[7] Y. Huang, X. Duan, Q. Wei, Lieber, M. Charles, “Directed assembly of one-dimensional nanostructures into functional networks,” *Science*, Vol. **291**, Issue: 5504, p.630, January, 2001.

[8] Y. Huang, X. Duan, Y. Cui, L. J. Lauhon, K.-H. Kim, Lieber, M. Charles, “Logic gates and computation from assembled nanowire building blocks,” *Science*, Vol.

294, Issue: 5545, p.1313, November, 2001.

[9] Y. Zhang, A. Chang, J. Cao, Q. Wang, W. Kim, Y. Li, N. Morris, E. Yenilmez, J. Kong, and H. Dai, “Electric-field-directed growth of aligned single-walled carbon nanotubes,” *Appl. Phys. Lett.*, Vol. **79**, Issue: 19, pp.3155-3157, November, 2001.

[10] K. H. Lee, J. M. Cho, and W. Sigmund, “Control of growth orientation for carbon nanotubes,” *Appl. Phys. Lett.*, Vol. **82**, Issue: 3, pp.448-450, January, 2003.

[11] B.-H. Chen, P.-Y. Lo, J.-H. Wei, M.-J. Tsai, C.-L. Hwang, T.-S. Chao, H.-C. Lin, and T.-Y. Huang, “Localized lateral growth of single-walled carbon nanotubes for field-effect transistors by a Cobalt-Mix-TEOS method,” *Electrochem. Solid-State Lett.*, Vol. **8**, Issue: 10, pp.G290-293, August, 2005.

[12] W. E. Alvarez, B. Kitiyanan, A. Borgna, and D. E. Resasco, “Synergism of Co and Mo in the catalytic production of single-wall carbon nanotubes by decomposition of CO,” *Carbon*, Vol. **39**, Issue: 4, pp.547-558, June, 2001.

[13] A. Lan, Y. Zhang, X. Zhang, Z. Iqbal, H. Grebel, “Is molybdenum necessary for the growth of single-wall carbon nanotubes from CO? ” *Chemical Physics Letters*, Vol. **379**, Issue: 5-6, pp.395-400, October, 2003.

[14] B. C. Satishkumar, A. Govindaraj, R. Sen, C.N.R. Rao, “Single-walled nanotubes by the pyrolysis of acetylene-organometallic mixtures,” *Chemical Physics Letters*, Vol. **293**, Issue: 1-2, pp.47-52, August, 1998.

[15] B. Kitiyanan, W. E. Alvarez, J.H. Harwell, and D. E. Resasco, “Controlled production of single-wall carbon nanotubes by catalytic decomposition of CO on bimetallic Co–Mo catalysts,” *Chemical Physics Letters*, Vol. **317**, Issue: 3-5, pp.497-503, February , 2000.

[16] X. Z. Liao, A. Serquis, Q. X. Jia, D. E. Peterson, Y. T. Zhu , and H. F. Xu, “Effect of catalyst composition on carbon nanotube growth,” *Appl. Phys. Lett.*, Vol. **82**,

Issue: 16, pp.2694-2696, April, 2003.

[17] M. S. Dresselhaus, G. Dresselhaus, Ph. Avouris, *Carbon nanotubes: synthesis, structure, properties, and applications*: Springer-Verlag, Berlin, 2001.

[18] A. Bachtold, P. Hadley, T. Nakanishi C. Dekker**,** "Logic circuits with carbon nanotube transistors," *Science*, Vol. **294**, Issue: 5545, p.1317, November, 2001.

[19] S. J. Wind, J. Appenzeller, R. Martel, V. Derycke, Ph. Avouris, "Vertical scaling of carbon nanotube field-effect transistors using top gate electrodes," *Appl. Phys. Lett.*, Vol. **80**, Issue: 20, pp.3817-3819, May, 2002.

[20] J. Appenzeller, J. Knoch, V. Derycke, R. Martel, S. Wind, and Ph. Avouris, "Field-modulated carrier transport in carbon nanotube transistors," *Phys. Rev. Lett.*, Vol. **89**, Issue: 12-16, p.126801, September, 2002.

[21] A. Javey, Q. Wang, W. Kim, and H. Dai, "Advancements in complementary carbon nanotube field-effect transistors," *IEDM Technol. Dig.*, pp.741-744, 2003.

[22] M. Bockrath, J. Hone, A. Zettl, P. L. McEuen, A. G. Rinzler and R. E. Smalley, "Chemical doping of individual semiconducting carbon-nanotube ropes," *Phys. Rev. B.*, Vol. **61,** Issue: 16, pp.R10606-8, April, 2000.

[23] C. Zhou, J. Kong, E. Yenilmez, H. Dai, "Modulated chemical doping of individual carbon nanotubes**,"** *Science*, Vol. **290**, No. 5496, pp.1552–1555, November, 2000.

[24] N. Bendiab, A. Righi, E. Anglaret, J. L. Sauvajol, L. Duclaux, F. Béguin, "Low-frequency Raman modes in Cs- and Rb-doped single wall carbon nanotubes," *Chemical Physics Letters*, Vol. **339**, Issue: 5-6, pp.305-310, May, 2001.

[25] V. Derycke, R. Martel, J. Appenzeller, Ph. Avouris, "Controlling doping and

carrier injection in carbon nanotube transistors," *Appl. Phys.Lett.*, Vol. **80**, Issue: 15, pp.2773-2775, April, 2002.

[26] J.-H. Wei, H.-H. Wang, M.-J. Kao, "Method for fabricating n-type carbon nanotube device", U.S patent, Patent number: US6723624, Date of patent: 2004-04-20.

[27] D. Kaminishi, H. Ozaki, Y. Ohno, K. Maehashi, K. Inoue, K. Matsumoto, Y. Seri, A. Masuda, and H. Matsumura, "Air-stable *n*-type carbon nanotube field-effect transistors with Si_3N_4 passivation films fabricated by catalytic chemical vapor deposition,**"** *Appl. Phys.Lett.*, Vol. **86,** p.113115, March, 2005.

[28] J.-H Wei, H.-H Wang, H.-H Chen, M.-J Lai, M.-J Kao, and M.-J Tsai, "A novel short-gate carbon nanotube thin film transistors," *Proceedings of the IEEE-TSA*, pp.42-45, 2003.

[29] P. G. Collins, K. Bradley, M. Ishigami, and A. Zettl, "Extreme oxygen sensitivity of electronic properties of carbon nanotubes," *Science*, Vol. **287**, pp.1801-4, March, 2000.

[30] K. Bradley, S.-H. Jhi, P. G. Collins, J. Hone, M. L. Cohen, S. G. Louie, and A. Zettl, "Is the intrinsic thermoelectric power of carbon nanotubes positive?" *Phys. Rev. Lett.*, Vol. **85**, Issue: 20, pp.4361-4, November, 2000.

[31] B.-H. Chen, J.-H. Wei, P.-Y. Lo, Z.-W. Pei, T.-S. Chao, H.-C. Lin and T.-Y Huang, "Novel method of converting metallic-type carbon nanotubes to semiconducting-type carbon nanotube field-effect transistors," Japanese Journal of Applied Physics, Vol. **45**. No. 4B, pp.3680-3685, April, 2006.

[32] H. Kanzow and A. Ding, "Formation mechanism of single-wall carbon nanotubes on liquid-metal particles" *Phys. Rev. B,* Vol. **60**, No. 15, pp.11180-86, October, 1999.

Table 5.1 Co^{2+} residues in major process equipments.

	Metal etcher	Chemical Vapor Deposition Chamber	Dry etcher
Background wafer (before cobalt processings)	**3546 ppt**	**1015 ppt**	**3858 ppt**
Monitor wafers (after cobalt catalyst processings)	**wafer #11：2736 ppt wafer #04：1890 ppt**	**wafer #20：966 ppt wafer #14：2102 ppt**	**wafer #09：4297 ppt wafer #10：2445 ppt**
Monitor wafers (dry/wet cleaned after Co catalyst processings)	**wafer #18：2059 ppt (wet-cleaned)**	**wafer #08：3204 ppt (dry-cleaned)**	**wafer #17：3509 ppt (dry-cleaned)**

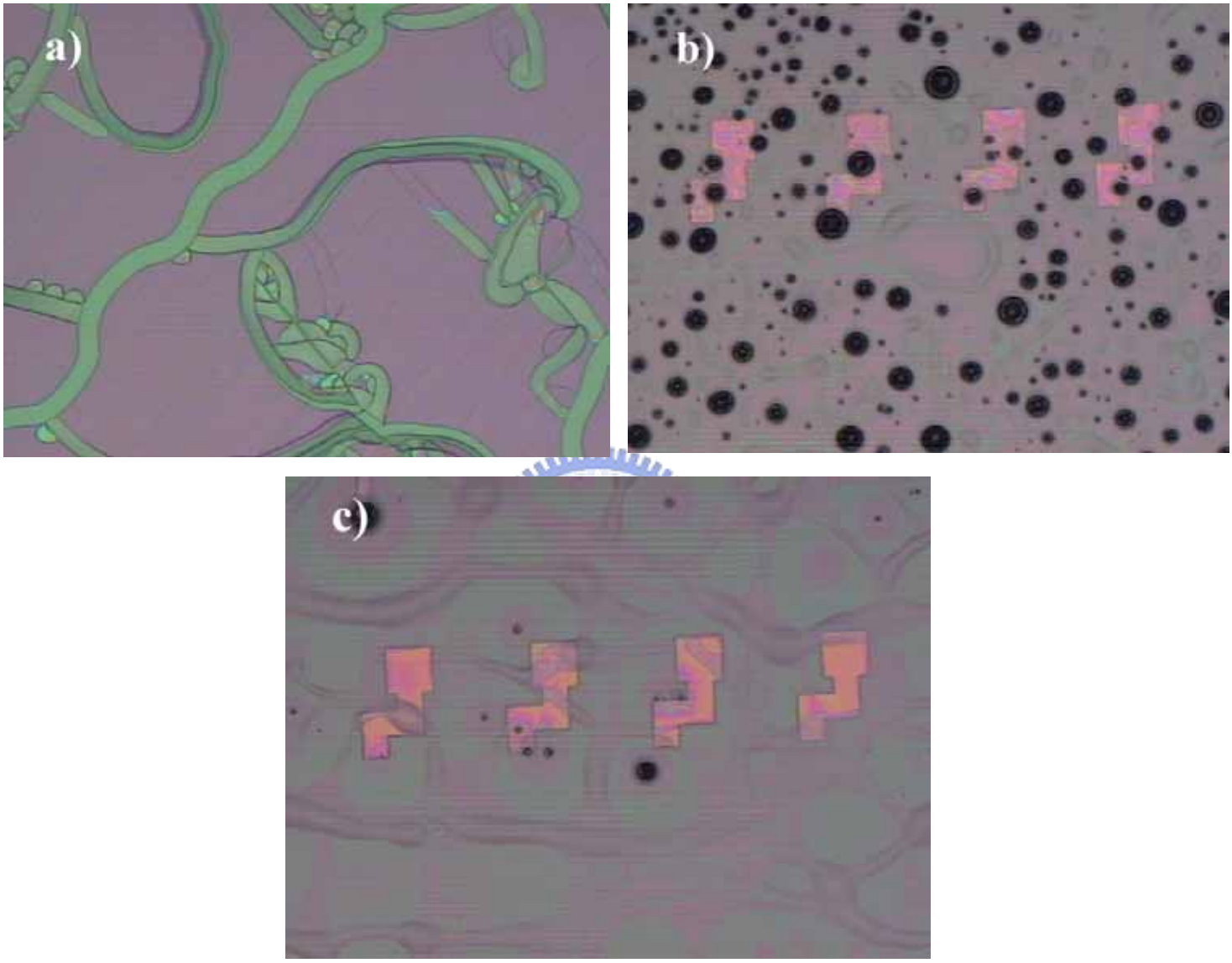


Figure 5.1 The influence of moisture and stirring time on the preparation of CMT solution. (a) CMT film cracks after first soft bake (CMT was exposed to moisture when stirred). (b) Co particles aggregate together after first soft bake without proper stirring. (c) Co particles disperse well after first soft bake with proper stirring of the CMT solution. Note that the patterns in (b) and (c) are pre-defined n^+-poly bottom gate electrodes.

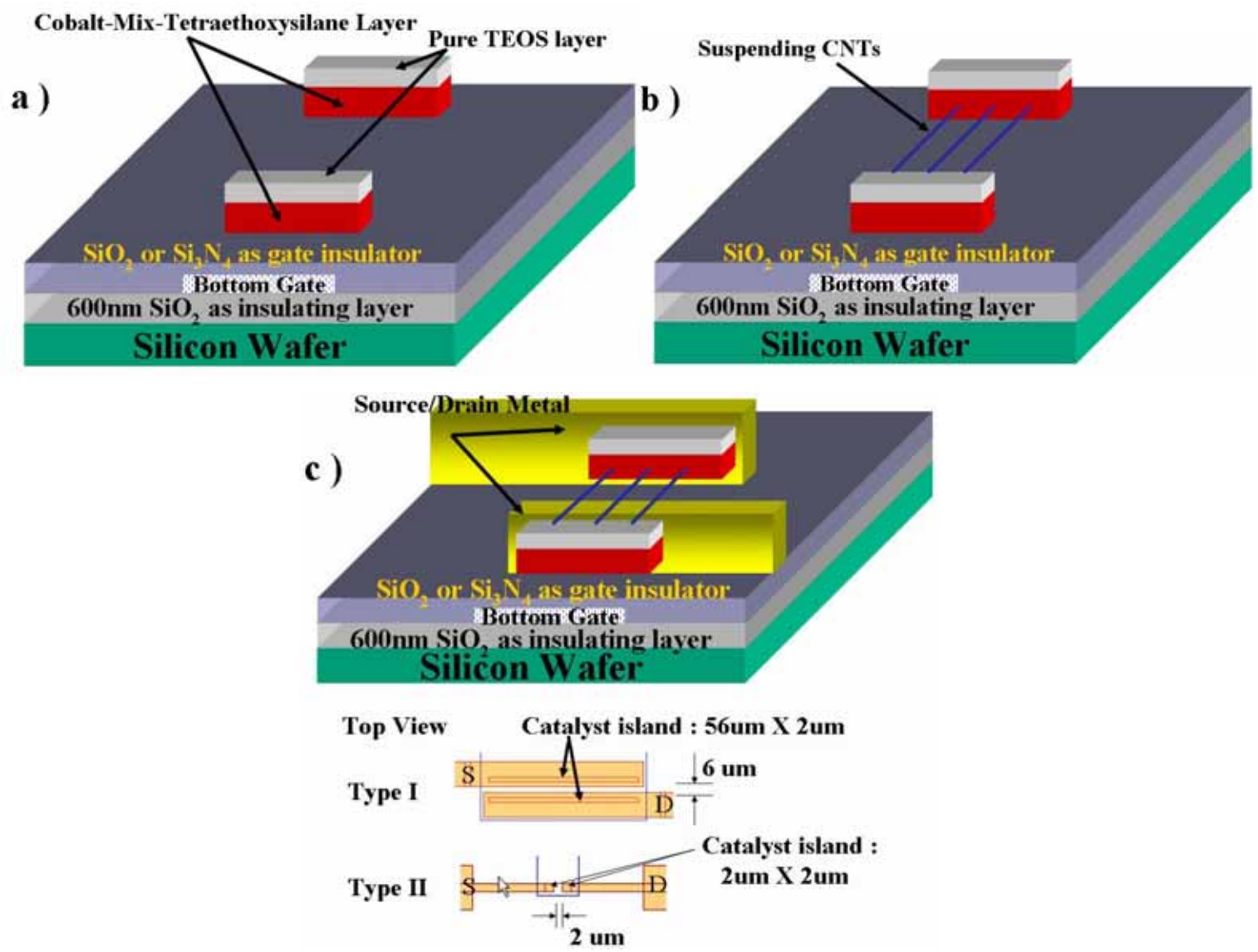


Figure 5.2 Process flow for the growth of bundled-CNTs. (a) Catalyst mixed TEOS (CMT) and pure TEOS layers were spun on oxidized substrate with patterned bottom gates, followed by photolithography and RIE processes to form CMT catalyst islands. (b) Growth of suspending SWNTs connecting two neighboring catalyst islands. (c) Ti metal lift-off process to form source/drain electrodes. The inset of Fig. 5.2(c) shows two kinds of catalyst islands and S/D metal pads in our layout design. Note that the individual bottom n^+-poly gate and the gate oxide or nitride layer were both formed before the CMT was spun.

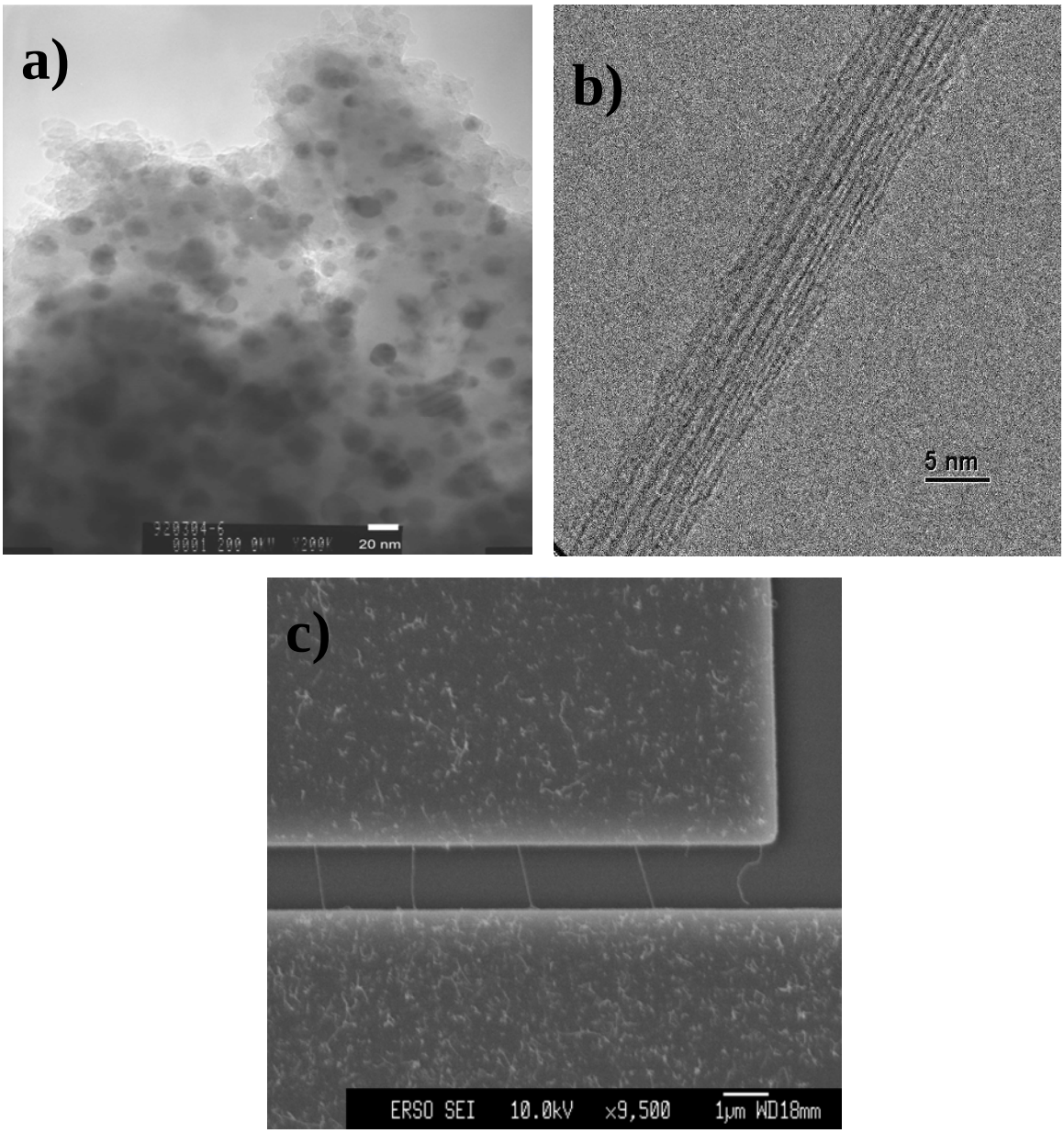


Figure 5.3 TEM pictures for CMT layer and bridged-CNT. (a) Cobalt nanoparticle uniformly embedded in oxide layer. (b) Bundled-SWNT synthesized from CMT powders with 10 nm in diameter. (c) Many bridged SWNTs are formed between the CMT catalyst islands.

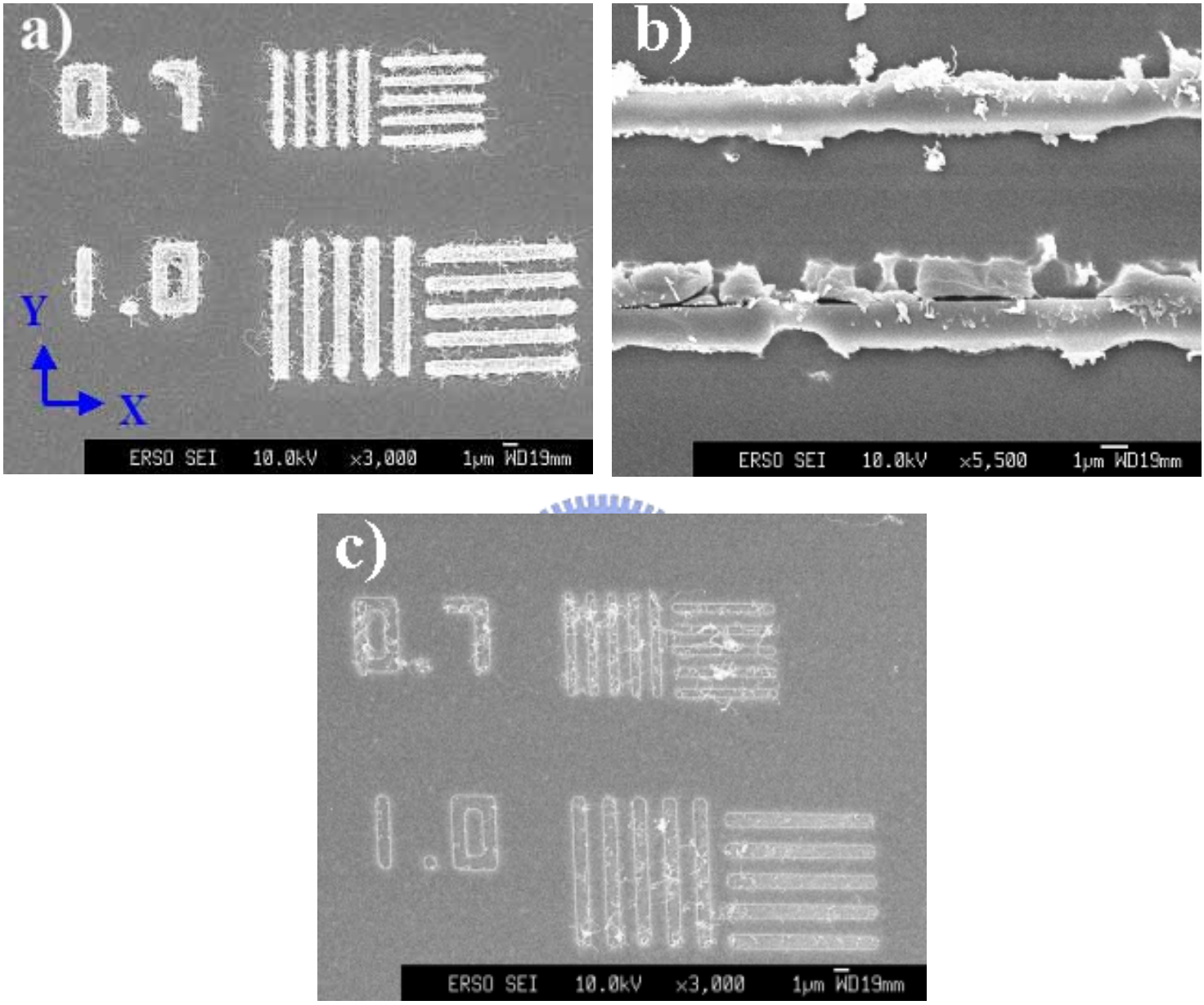


Figure 5.4 The adhesion of CMT layer on different layers. The vernier structure (i.e., the scale bars) indicates the resolution of photolithography and the finest pattern after dry etching. (a) CMT spun well on thermal oxide layer. (b) Poor adhesion of CMT layer on nitride. (c) By adding a hexamethyldisilazane (HMDS) layer before CMT spinning, good CMT catalyst islands are obtained on nitride layer suitable for bio-sensor purposes.

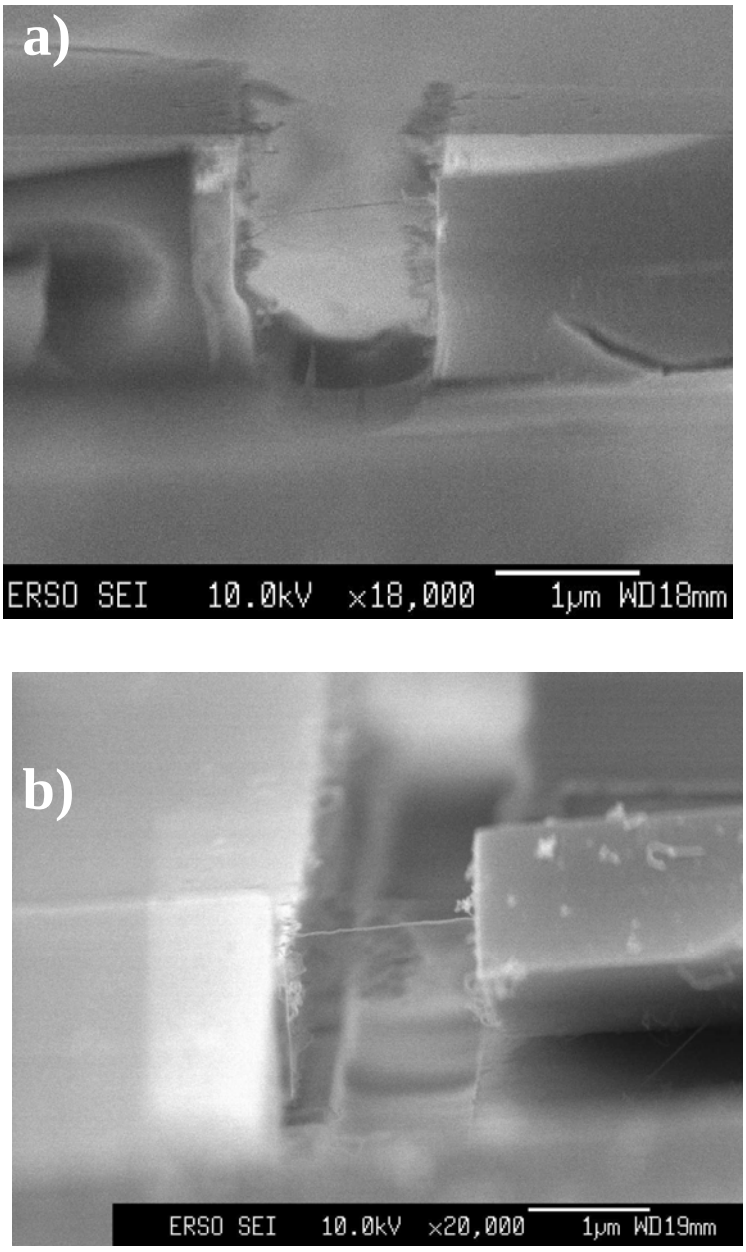
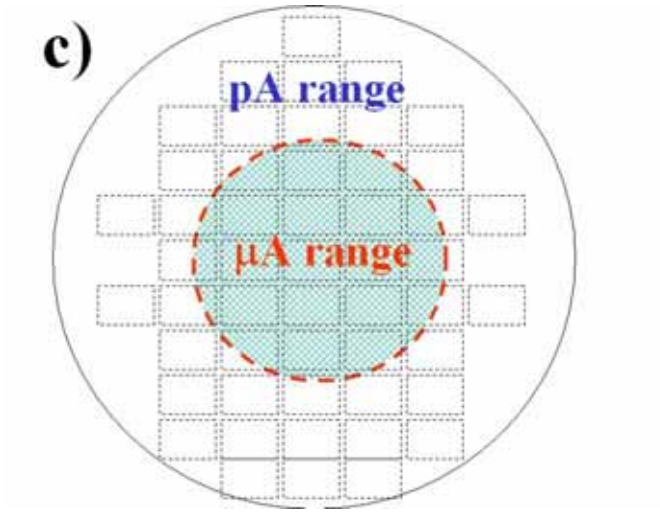


Figure 5.5 SEM pictures of lateral-grown CNTs (a) Formed by dry etching. (b) Formed by wet etching. The bundled CNTs bridge the CMT layer from the catalyst.



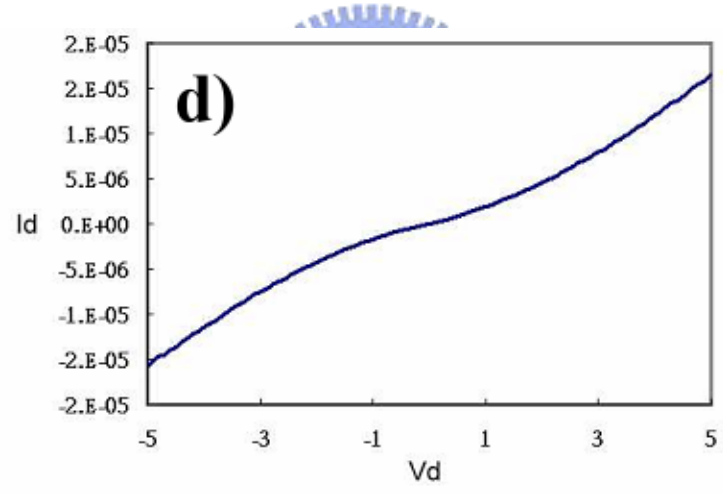


Figure 5.5 (c)-(d) The leakage current range without any post treatment by using dry etcher to form the catalyst islands. Note the leakage current is in the μA range because of the residues of Co particle/CMT layer, which can leave a conductive layer on the wafer surface and short the CNT-FETs.

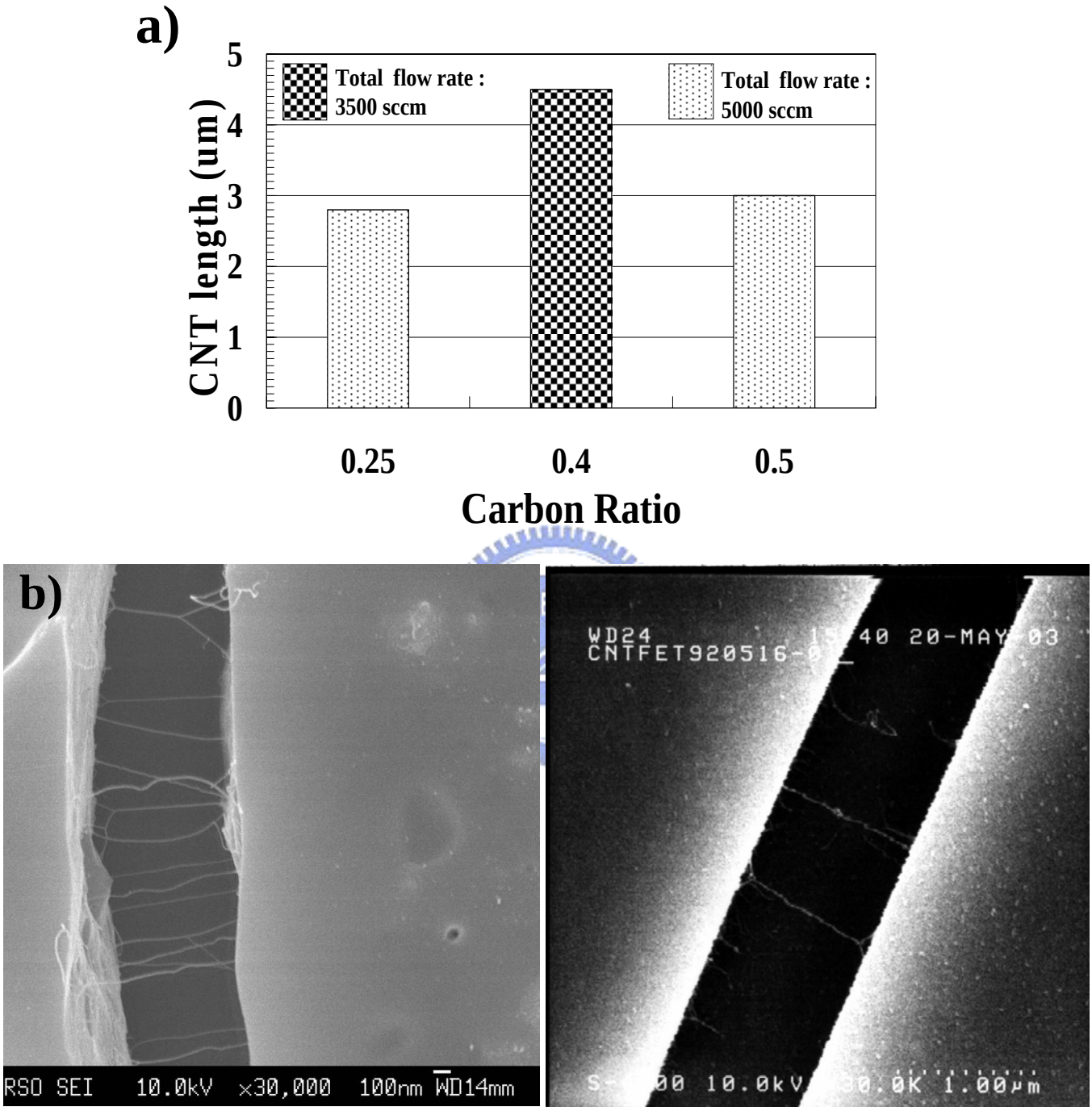


Figure 5.6 (a) Lateral length of CNT versus gas composition. (b) SEM picture of CNTs when Co^{2+} concentration is 1.5M. and (c) SEM picture of CNTs when Co^{2+} concentration is 0.5M.

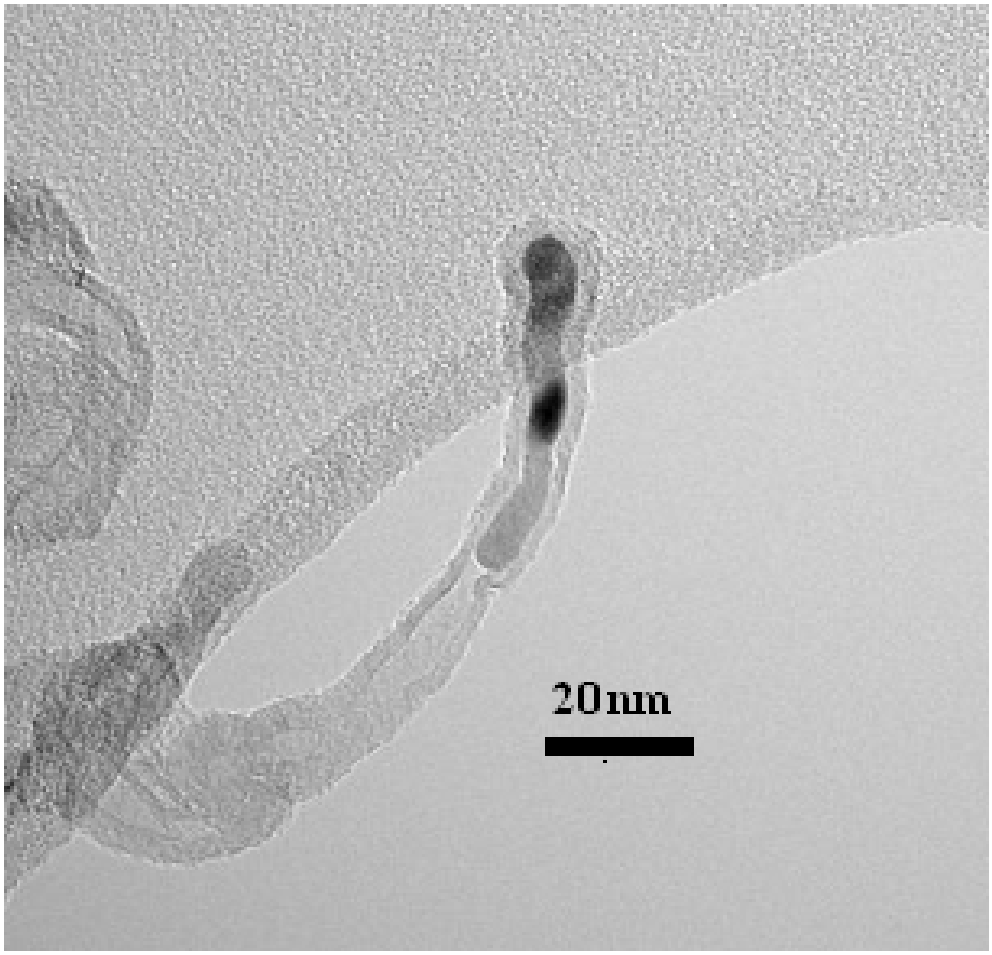


Figure 5.7 SEM picture of tip-growth.

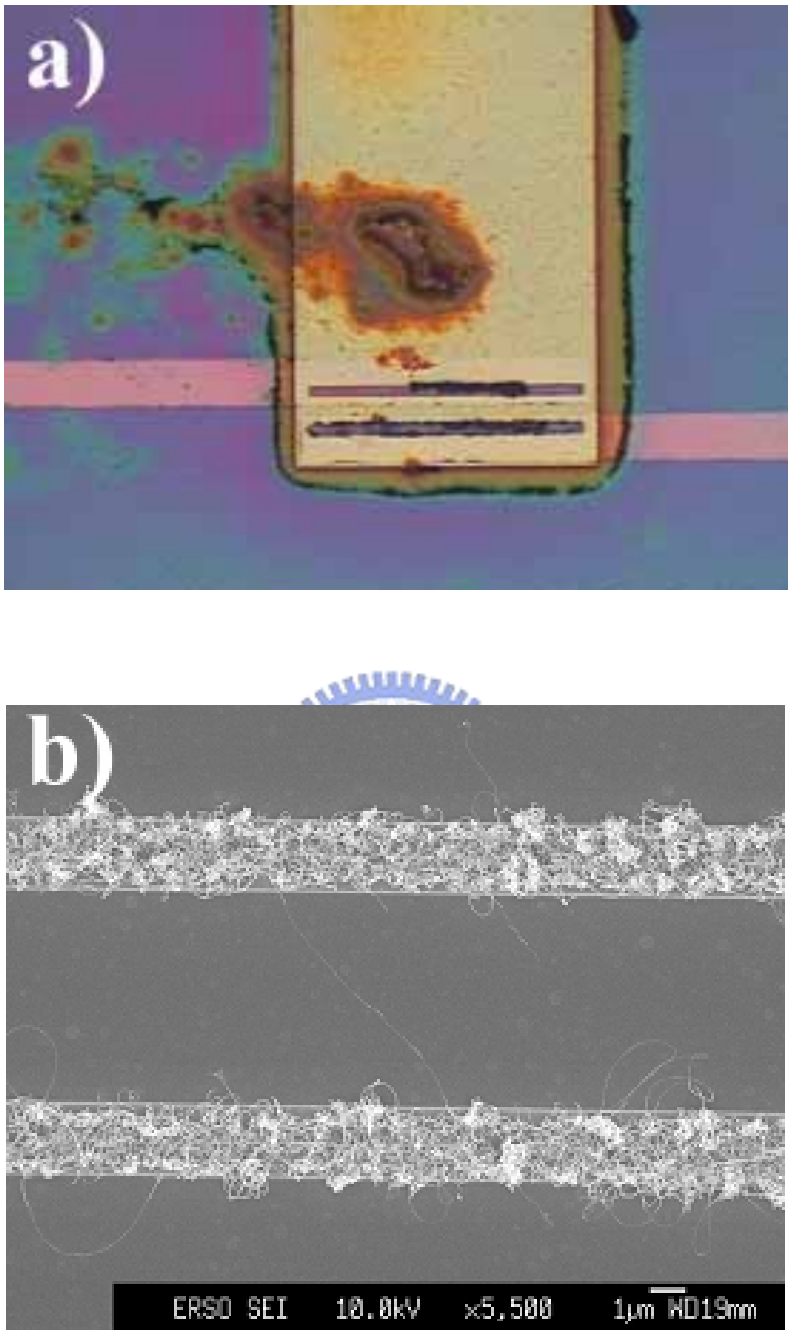


Figure 5.8 The picture of an as-grown semiconducting-type CNT-FET and its I_{ds}-V_{ds} curve. Insets show the corresponding transfer curves (I_{ds}-V_g). (a) The optical microscope image of the Type-I device in Fig. 4.2(c). Note the black clusters are CNTs (without TEOS layer covering CMT catalyst islands). (b) SEM morphology of 6 μm-long CNT grown between two catalyst islands.

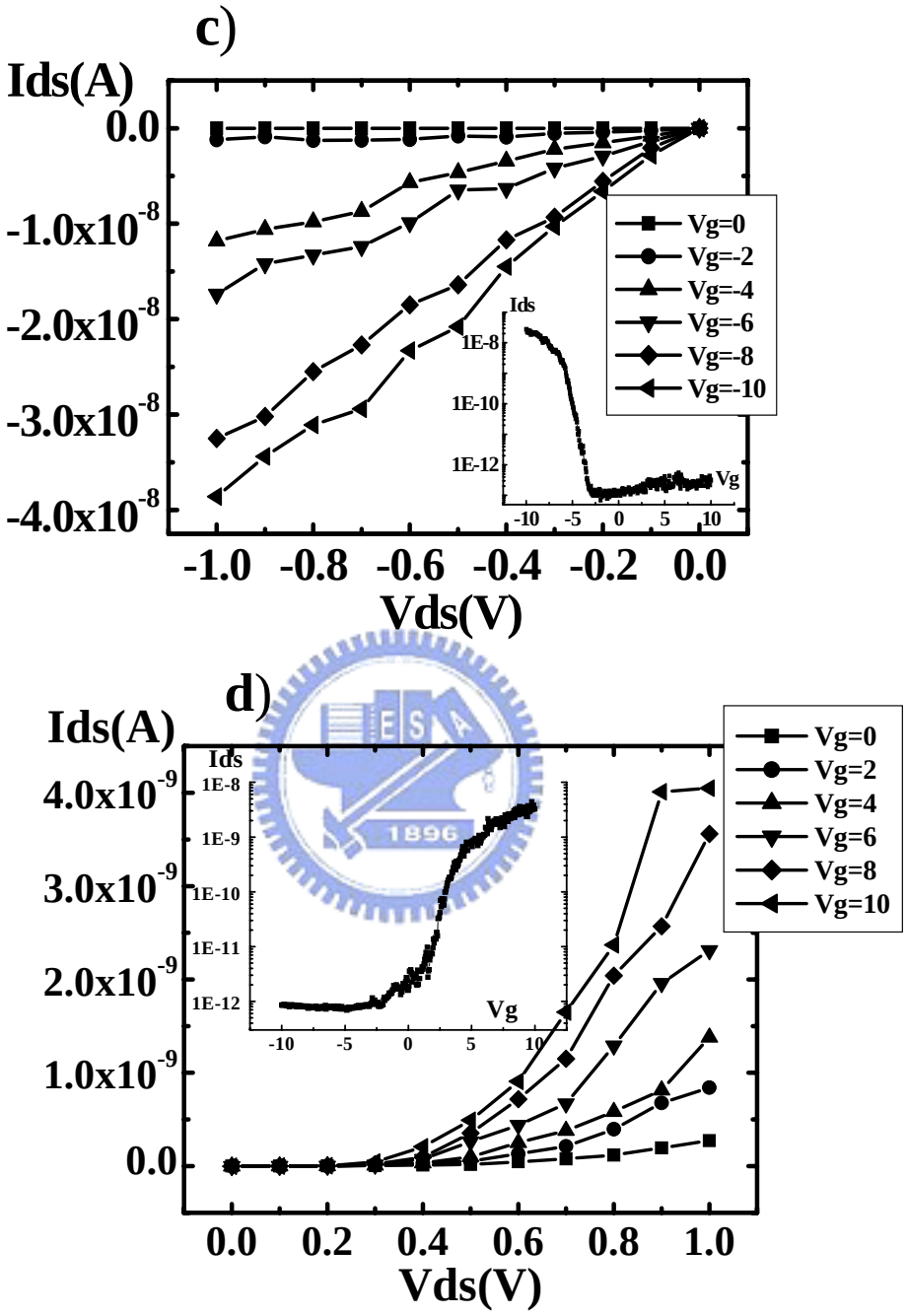


Figure 5.8 (c) An as-grown p-type CNT-FET with five orders of on/off ratio. (d) Converted n-type CNT-FET after depositing a 300 nm Si_3N_4 film on the p-type CNT-FET shown in (c).

Chapter 6

Complementary Carbon Nanotube-Gated Carbon Nanotube Thin-Film Transistor

6.1 Backgrounds and Motivation

Single-wall carbon nanotube (SWNT) is an ideal candidate for future nanoelectronics because of its small diameter, high current-carrying capability, and high conductance in a one-dimensional nanoscale channel. The carbon nanotube (CNT) field effect transistor (FET) and several related logic gates have been fabricated by using semiconducting-type CNTs [1–3] as the building block, and the CNT-FET shows superior electrical properties over the conventional silicon metal-oxide-semiconductor field effect transistor (MOSFET). Although these CNT-FETs feature a small channel width, the gate length is usually larger than 100 nm which is limited by the lithography process [3].

Previously, our group have manufactured *n*-type [4–6] and *p*-type CNT-FETs without resorting to any additional and complex annealing process (Table 6.1). In this study, a complementary CNT-gated CNT-FET (CG-CNT-FET) structure is proposed and demonstrated. Without relying on electron-beam lithography, the gate length and the gate width of CNT-FET are easily shrunk to 20– 50 nm or less. This is achieved by using two perpendicularly-crossed SWNT bundles as the interchangeable channel and gate. The new CG-CNT-FET shows either *n*-or *p*-type FET characteristics, depending on whether the bottom CNT bundle (CNT1) or the top CNT bundle (CNT2) is used as the channel, with the other CNT bundle acting as the gate. After interchanging the roles of the gate and the channel, the upsidedown device still shows good FET characteristics. Detailed operation principles will be explained next.

6.2 Device Fabrication

The key fabrication process of the dual-functionality CG-CNT-FET is as follows: Briefly, a 600 nm SiO_2 field oxide layer was first grown by wet oxidation at 985 ° C on 4 in. *p*-type silicon wafer. Then, a 100 nm Ti layer was deposited by radio-frequency (rf) sputtering, and subsequently patterned and etched to serve as the source/drain metal pads in the upright mode (and as the gate metal pads in the upsidedown mode). The width of the source/drain metal pads is $1\mu m$, and the spacing between source and drain pads is $2\mu m$, as shown in Fig. 6.1(a). Afterwards, the bottom SWNT bundle (CNT1) was coated to serve as the channel in the upright mode (and as the gate in the upsidedown mode). Then, a 100 nm Si_3N_4 was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 390°C to serve as the gate insulator. Next, a second 100 nm Ti layer was deposited by rf sputtering, and subsequently patterned by lithography and dry etching to serve as the gate metal pads in the upright mode (and as the source/drain metal pads in the upsidedown mode). Afterwards, the top SWNT bundle (CNT2) was coated. It is worth noting that CNT2 was laid perpendicularly crossing the first CNT1 bundle to serve as the gate in the upright mode (and as the channel in the upsidedown mode). This is followed by a 100 nm SiO_2 deposition by PECVD at 400°C to serve as the passivation layer. Contact holes to the gate and source/drain metal pads were subsequently etched in a MERIE dry etcher. Wafers could then follow a standard back-end processing to completion. A commercial HP-4155A was applied to measure I_{ds}-V_{ds} and I_{ds}-V_g transfer curves of the CNT-FETs.

6.3 Experimental Results and Discussion

The top view and cross section of the completed device are shown in Figs. 6.1(a) and 6.1(b), respectively. By controlling the process, the bottom CNT1 bundle behaves as an *n*-type semiconductor, while the top CNT2 bundle behaves as *p*-type semiconductor [4-6].

Scanning electron microscopy (SEM) image of the CNT-gated CNT-FET is shown in Fig. 6.2. It can be seen that the two CNT bundles, which serve as the gate and the channel interchangeably, are placed on each side of the gate insulator. Note that the two CNT bundles are perpendicularly crossed so as to form a FET structure at the intersection. The diameter of each CNT bundle is around 20 to 50 nm. A bias voltage, which is applied to the top CNT2 bundle, modulates the bottom CNT1 bundle at the intersection. The effective gate length is only 20– 50 nm. I_{ds}-V_{ds} characteristics of the CNT-gated CNT-FET are shown in Fig. 6.3. The drain current of the CNT-FET with silicon nitride as the gate insulator increases with the gate voltage, and shows typical *n*-channel FET characteristics. The on/off current ratio is ~ 1000. By interchanging the roles of the channel and the gate, i.e., the conducting channel now becomes the gate (i.e., the bottom CNT1 bundle becomes the gate), while the gate becomes the new channel (i.e., the top CNT2 now becomes the channel), the upsidedown device also shows FET characteristics, as shown in Fig. 6.4, albeit with the complementary conduction type (i.e., *p* type). This is because of the close proximity between CNT2 bundle and the oxide passivation layer (Table 6.1).

From the above results, we found that both the bottom and top CNT bundles in the structure can act as the channel and the gate interchangeably. This behavior is unique and differs from traditional Si-based devices. It opens up a new possibility and flexibility in circuit design. For example, the signal is usually routed from one

MOSFETs' drain electrode (i.e., output) to the next stages' gate electrode (i.e., input) in Si-based MOSFET circuits. It would require a via and a metal line to connect the two MOSFETs. In contrast, in the new dual-functionality CG CNT-FET structure, one CNT can act as the conduction channel of the first FET and the gate electrode of the next one simultaneously. No interconnection metal is thus needed. In addition to the small gate length and the dual-functionality CNT, the new CNT-FET also offers both *n*-and *p*-type characteristics, lending itself readily to complementary-type circuit implementation, i.e., the CNT conducting channel is changed from *n* type (i.e., CNT1, as described previously) to the *p* type (i.e., CNT2). It is worth noting that the conduction-type of CNT can be tailored by the passivation layer in close contact with the CNT (Table 6.1), as the passivation layer greatly affects the oxygen desorption/reabsorption of the nearby SWNTs, which in turn set the conduction type.

By using plasma-enhanced (PE) nitride as the gate dielectric layer on top of CNT1, the process temperature of the deposition would be high enough (390°C) to simultaneously remove the oxygen atoms from the CNT1 and CNT1/metal interface in the PECVD deposition chamber. Therefore, we can achieve *n*-type CNT1 channel without extra processing steps [4-6]. For CNT2 as the channel, we adopted PECVD oxide as the passivation layer in this work. The process temperature was around 400°C. Even though this temperature was high enough to desorb oxygen from CNT2, a few oxygen atoms could be driven back to CNT2 during PECVD TEOS oxide process [7,8]. So CNT2 depicts *p*-type semiconducting characteristics. This is because when the oxygen atoms are reabsorbed during the PECVD oxide process, the Fermi level in CNT2 moves away from the conduction band, and becomes closer to the valence band. So, by applying a negative bias to CNT1 as the gate electrode, the hole can tunnel through the energy barrier efficiently in CNT2 channel. Similarly, we

could selectively create *p*-type CNT-FETs (actually, depletion-mode *p*-type CNT-FET, as shown in Fig. 6.4), by using CNT2 as the channel and CNT1 as the gate. In Fig. 6.4, the upsidedown FET shows “normally on” p-type FET characteristics. The reason why this p-type device is normally on is as following. In Fig. 6.5(a), we can see the energy barrier around both source and drain electrodes are quite small. So even the top-gate (CNT1) is floating, the holes can tunnel through the small barrier height after applying voltage between S/D electrodes. This is the reason why we can measure drain current (I_d) when Vg = 0 and this is a “normally on” device.

With negative top-gate bias, the up-bending potential profile shown in Fig. 6.5(b) will slightly accelerate the hole flow due to the barrier lowering effect, and the drain current will increase slightly, as shown in Fig. 6.4.

With positive top-gate bias, the band diagram shown in Fig. 6.5(c) will block the hole flow, and the drain current will be suppressed (as shown in Fig. 6.4).

Both *n*-and *p*-type devices are crucial for complementary metal-oxide-semiconductor (CMOS) circuits as well as certain circuit applications, such as detectors, i.e., a *p*-channel CNT-FET sensor is required for negative charge enzyme system [9]. In the proposed CG-CNT-FET structure, the current-voltage (*I*-*V*) characteristics of each device can be turned by the nearby passivation layer. With the small gate length of CG-CNT-FET, it appears to be promising for future ultrahigh sensitive sensors. In conventional ultra large-scale integrated technology, all devices in a chip, or more precisely the whole wafer, are all predetermined early in the process flow. In contrast, for the proposed CG CNT-FET, the type of conduction of each individual CNT-FET in a wafer can be individually controlled much later in the process flow by metal routing. This is because CNT1 and CNT2 can be tuned to different conduction-type by the different passivation layers (Table 6.1). It thus opens

up the possibility and flexibility in future CMOS circuit design and fabrication.

6.4 Summary

In summary, a dual-functionality complementary CG CNT-FET is proposed in this study. This CNT-FET has sub-50 nm or smaller feature size without using electron-beam lithography and sub-100 nm etching technology. Two separate CNT bundles are deposited to serve the dual roles of gate and channel of the FET simultaneously. The conduction type of each device is individually determined by selecting CNT1 or CNT2 as the channel, with the other CNT serving as the gate. While the conduction type of CNT1 and CNT2 can be set to be of the complementary type by choosing different passivation layers in close proximity with each CNT bundle. The diameter of CNT bundle could shrink further by improving the CNT purification process, a FET of the SWNT with 1– 2 nm gate length can be expected. This unique dual functionality offers the flexibility in the design of future complementary CNT logic circuits.

References

[1] R. Martel, T. Schmidt, H. R. Shea, T. Hertel, and Ph. Avouris, “Single- and multi-wall carbon nanotube field-effect transistors,” *Appl. Phys. Lett.,* Vol. **73**, Issue: 17, pp.2447-2449, October, 1998.

[2] V. Derycke, R. Martel, J. Appenzeller and Ph. Avouris, “Carbon nanotube inter- and intramolecular logic gates,” *Nano Lett.,* Vol. **1**, No. 9, pp.453-456, September, 2001.

[3] S. J. Wind, J. Appenzeller, R. Martel, V. Derycke, and Ph. Avouris, “Vertical scaling of carbon nanotube field-effect transistors using top gate electrodes,” *Appl. Phys. Lett.,* Vol. **80**, Issue: 20, pp.3817-3819, May, 2002.

[4] J.-H. Wei, H.-H. Wang, and M.-J. Kao, “Method for fabricating n-type carbon nanotube device”, US patent, Patent number: US6723624, Date of patent: 2004-04-20.

[5] J.-H Wei, H.-H Wang, H.-H Chen, M.-J Lai, M.-J Kao, and M.-J Tsai, “A novel short-gate carbon nanotube thin film transistors,” *Proceedings of the IEEE-TSA,* pp.42-45, 2003.

[6] D. Kaminishi, H. Ozaki, Y. Ohno, K. Maehashi, K. Inoue, K. Matsumoto, Y. Seri, A. Masuda, and H. Matsumura, “Air-stable *n*-type carbon nanotube field-effect transistors with Si_3N_4 passivation films fabricated by catalytic chemical vapor deposition,**”** *Appl. Phys.Lett.,* Vol. **86,** p.113115, March, 2005.

[7] V. Derycke, R. Martel, J. Appenzeller, Ph. Avouris, “Controlling doping and carrier injection in carbon nanotube transistors,” *Appl. Phys.Lett.,* Vol. **80**, Issue: 15, pp.2773-2775, April, 2002.

[8] S. Heinze, J. Tersoff, R. Martel, V. Derycke, J. Appenzeller, and Ph. Avouris, “Carbon nanotubes as schottky barrier transistors,” *Phys. Rev. Lett.,* Vol. **89**, Issue:

10, pp. 106801-4, September, 2002.

[9] K. Besteman, J.-O. Lee, F. G. M. Wiertz, H. A. Heering, and C. Dekker, "Enzyme-coated carbon nanotubes as single-molecule biosensors," *Nano Lett.*, Vol. **3**, No. 6, pp.727-730, May, 2003.

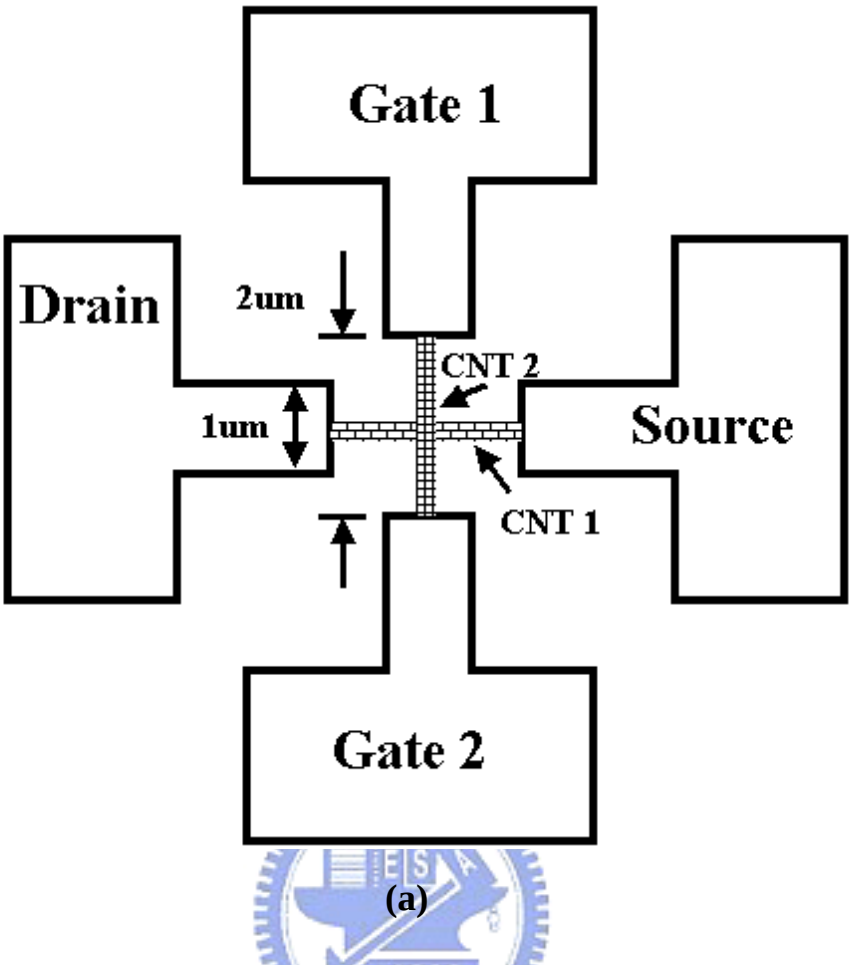
Table 6.1 The influence of electrical characteristics by depositing different dielectric layers

	Dielectric layer deposited on bottom CNT (i.e., CNT 1) /deposition temperature /film thickness	Dielectric layer deposited on top CNT (i.e., CNT 2) /deposition temperature /film thickness	Majority type of Devices on a wafer (using CNT 2 as gate electrode and CNT 1 as channel)	Majority type of Devices on a wafer (using CNT 1 as gate electrode and CNT 2 as channel)
This study[a]	PE-oxide/400 °C/200nm	PE-oxide/400 °C/200nm	*p*-type[b]	*p*-type[b]
This study[a]	PE-oxide/400 °C/200nm	PE-nitride/390 °C/200nm	*p*-type[b]	*n*-type[b]
This study[a]	PE-nitride/390 °C/200nm	PE-oxide/400 °C/200nm	*n*-type[b]	*p*-type[b,c]
This study[a]	PE-nitride/390 °C/200nm	PE-nitride/390 °C/200nm	*n*-type[b]	*n*-type[b]

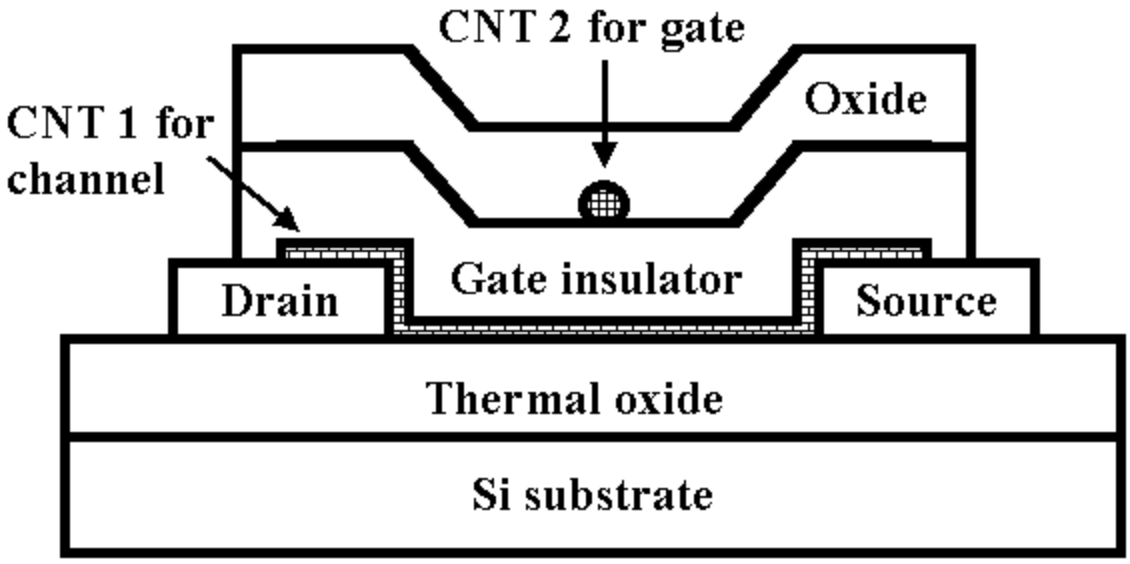
[a] Data not shown here

[b] Some of these devices depict ambipolar characteristics

[c] P-type depletion mode device is obtained in this work



(a)



(b)

Fig. 6.1 Top-view (a), and cross-sectional (b) images of the dual-functionality CG CNT-FET.

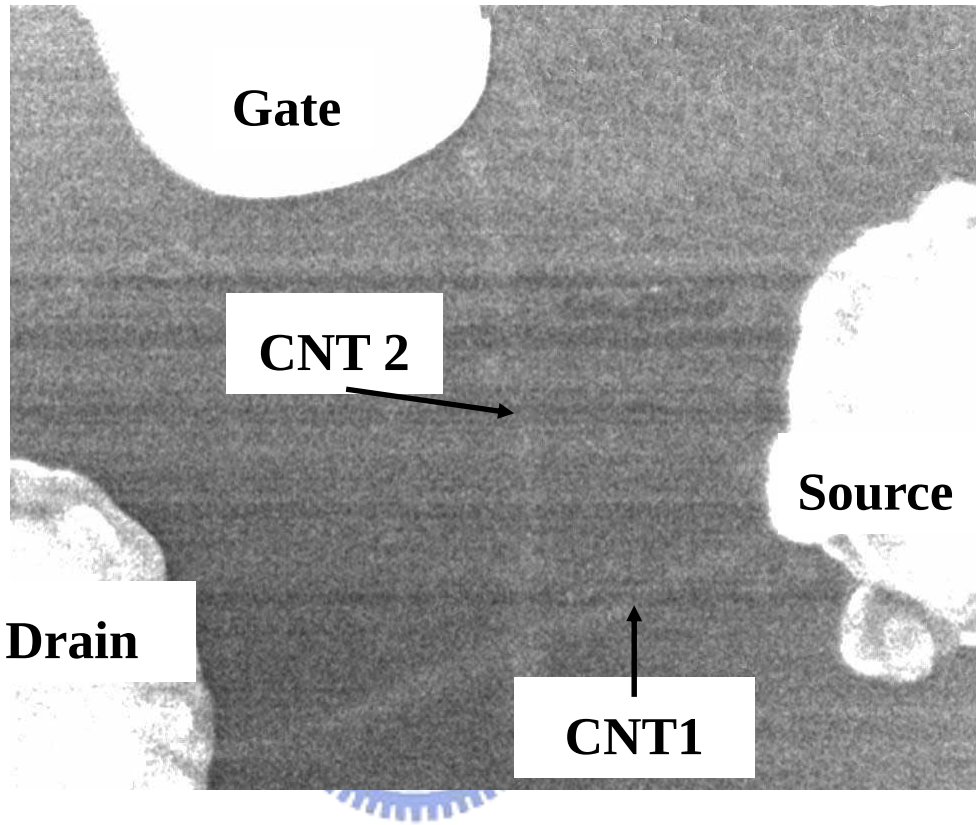


Fig. 6.2 SEM image of the perpendicularly-crossed CNT-FET. Two CNT bundles connected to metal pads are shown forming a cross in this image.

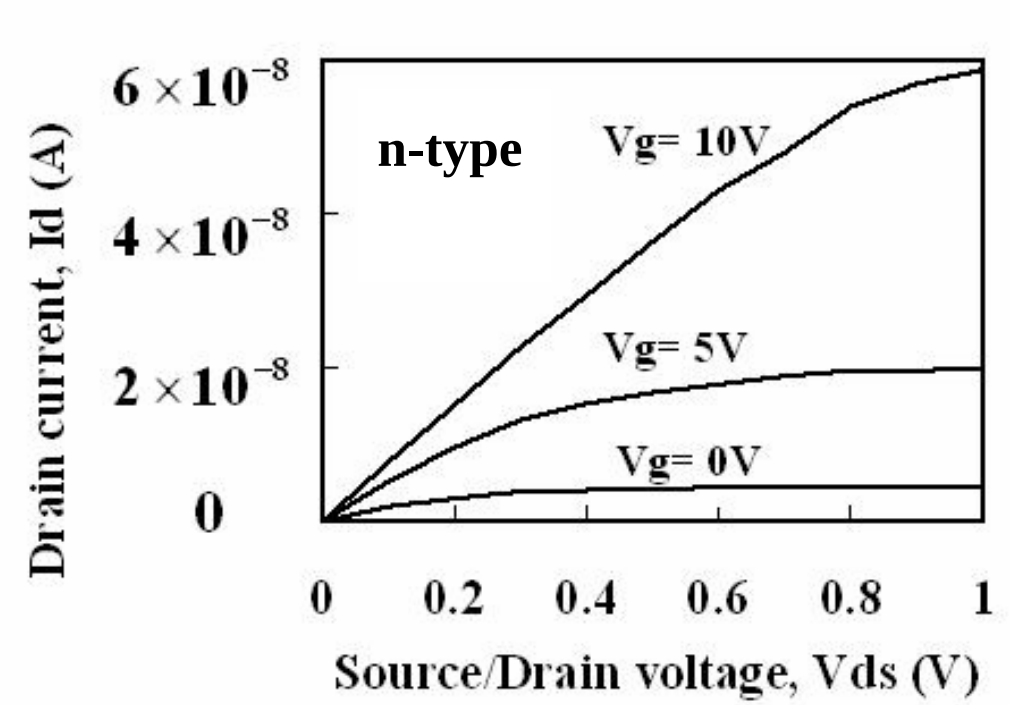


FIG. 6.3 I_{ds}-V_{ds} curves of CG CNT-FET in the upright mode, showing typical *n*-type FET characteristics (i.e., the bottom CNT1 as the channel, and the top CNT2 as the gate).

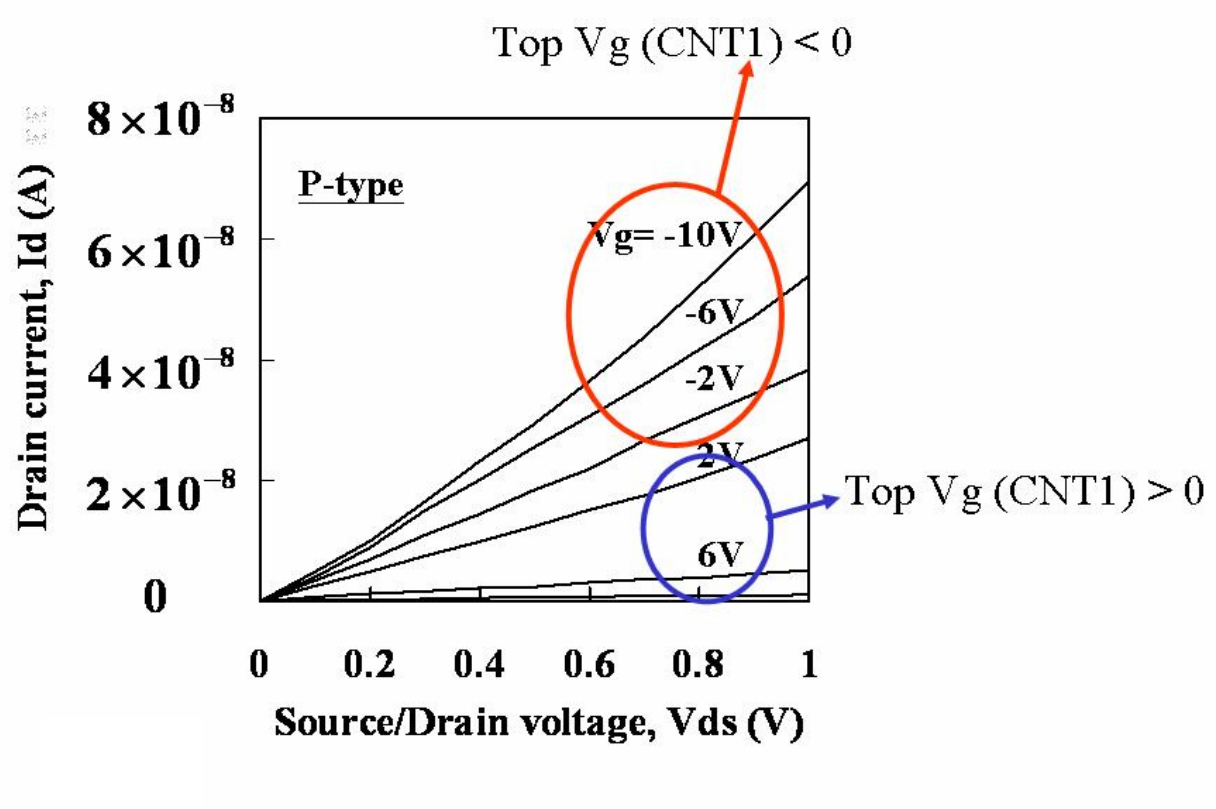
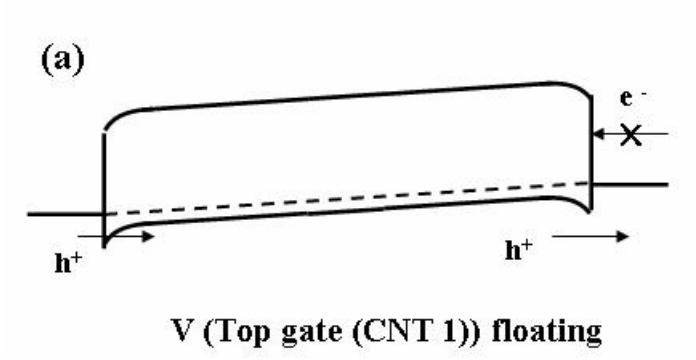
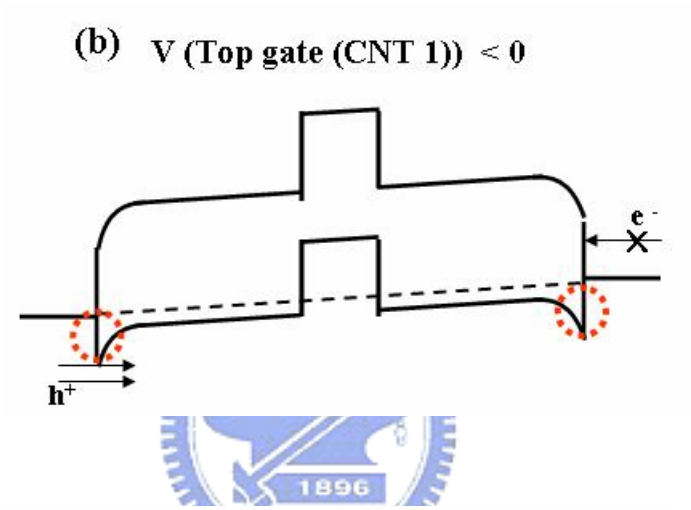


FIG. 6.4 I_{ds}-V_{ds} curves of CG CNT-FET after interchanging the roles of the channel and the gate (i.e., the bottom CNT1 as the gate, and the top CNT2 as the channel). The upsidedown FET shows typical *p*-type FET characteristics.





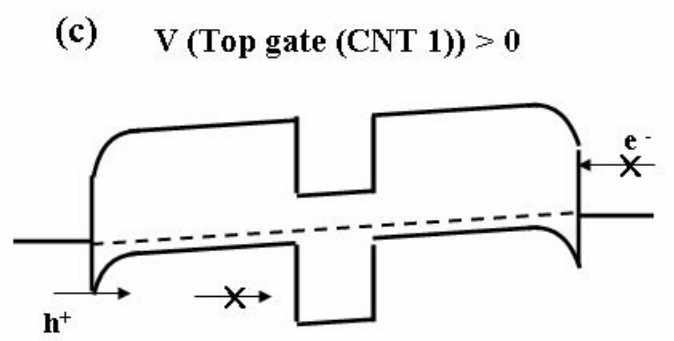


Fig. 6.5 (a) The energy barrier around both source and drain electrodes is small. So even the top-gate (CNT1) is floating, the holes can tunnel through the small barrier after applying voltage between S/D electrodes. This is a "normally on" device.

(b) With negative top-gate bias, the up-bending potential profile will slightly accelerate the hole flow due to the barrier lowering effect, and the drain current will increase slightly, as shown in Fig. 6.4.

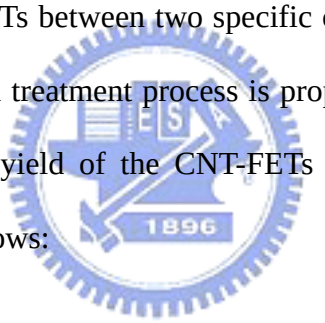
(c) With positive top-gate bias, the band diagram will block the hole flow, and the drain current will be suppressed (as shown in Fig. 6.4).

Chapter 7

Conclusions and Suggestions for Future Work

7.1 Conclusion

Major challenges still lie ahead for the CNT before it can become a replacement material for nanoelectronic applications. In this dissertation, the characteristics of CNT-FETs by using different manufacturing methods were discussed. For CNTs to be used in nanoelectronics, innovations are called for to efficiently control the placement of massive amounts of CNTs. In line of this, a CVD method is proposed to synthesize SWNTs and form bridged-CNTs between two specific catalyst islands for CNT-FETs successfully. Finally, a plasma treatment process is proposed to burn out the metallic type CNTs and increase the yield of the CNT-FETs efficiently. Several important results are summarized as follows:



1. In Chapter 2, we design a new set of photomasks for CNT-FETs which contain separate bottom gate and different channel length/width. We can also use this set of photomasks to manufacture both p- and n-type CNT-FETs for CMOS circuits without any complex doping process. When the CNT is used as the channel (active layer) of the CNT-FET, our method allows us to selectively exposing the individual CNT to the air or not. This is the key process which allows us to manufacture the air-stable n-type CNT-FETs. Specifically, we can manufacture p-type CNT-FETs if the channels (CNTs) of those devices are exposed to air. While n-type CNT-FETs can be obtained if the adsorption of oxygen in CNTs is deliberately blocked. The major role of oxygen in the conductance of CNT-FET is to change the barrier level between the metal and CNT.

The oxygen is electron rich, and can reduce the chance of electron-transport and increase the mechanism of hole transport. Therefore, the CNT-FETs will become p-type if their channels are exposed to air.

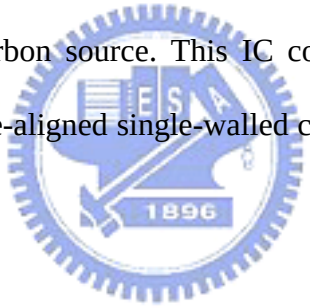
Finally, we also design process monitor testkey (for process monitoring purpose). The process monitor testkey will help us monitor the etching conditions of contacts or pads and avoid the over-etching. It is worth noting that there are several sets of CD bars and vernier for checking the resolution and shift of lithography.

2. In Chapter 3, a novel doublegated structure is proposed to control the conducting type of the CNT-FET in order to achieve unipolar-type devices without resorting to complex processes. Our results show that ambipolar-type CNT-FET can be converted to n- and p-type CNT-FETs by controlling the biases applied to the top- and bottom-gate electrodes. Our approach opens the possibility of creating specific type of CNT-FETs with well-controlled characteristics. This is crucial for CMOS circuits as well as certain circuit applications, such the detector applications where p-type CNT-FET sensor with high on/off current ratio is required for negative charge enzyme system. In the proposed DG CNT-FET structure, the I-V characteristics of each random device can be well-turned to the same level, and the ambipolar character of CNT-FETs can be annihilated. Furthermore, the threshold voltage of CNT-FETs can be possibly adjusted by using different bottom-gate and top-gate biases. These features make the new structure especially promising for applications in future ultrahigh sensitive sensors.

3. In Chapter 4, semiconducting-type CNT-FETs are realized by Ar plasma treatment. We believe that the ion bombardment during Ar plasma treatment attacks both

metallic- and semiconducting-type nanotubes. As long as the metallic-type CNTs that dominate the transport are broken by plasma, the resultant CNT-FETs will unambiguously show semiconductor features. In addition, we also propose the possibility of altering the symmetry of SWNT-FETs by damaging the surface structure. In other words, the effective chirality of the SWNTs can be altered by Ar plasma treatment.

4. In Chapter 5, we have developed an integrated circuit (IC) compatible process for fabricating CNT-FETs successfully with a shorter hydrogen reduction time in CCVD process. Longer CNT length can be obtained by optimizing carbon ratio during synthesis, and the accumulation of carbon on the catalyst tip can be controlled by mixing inert gas with the carbon source. This IC compatible process seems to be promising for fabricating a pre-aligned single-walled carbon nanotube matrix for both n- and p-type CNT-FETs.



5. In Chapter 6, a novel dual-functionality complementary CG CNT-FET is proposed in this study. This CNT-FET has sub50-nm or smaller feature size without using electron-beam lithography and sub-100 nm etching technology. Two separate CNT bundles are deposited to serve the dual roles of gate and channel of the FET simultaneously. The conduction type of each device is individually determined by selecting CNT1 or CNT2 as the channel, with the other CNT serving as the gate. While the conduction type of CNT1 and CNT2 can be set to be of the complementary type by choosing different passivation layers in close proximity with each CNT bundle. This unique dual functionality offers the flexibility in the design of future complementary CNT logic circuits.

7.2 Suggestions for Future Work

There are some works that deserve further efforts:

1. In Chapter 3, the purpose of top-gate is to modulate the conductance of CNTs by utilizing the electrostatic effects on the energy band diagram. We have design a new set of photomasks which contain different top-gate positions. These top-gate positions are as following: “on the edge of source electrode”, “on the center of the channel”, “on the edge of drain electrode” and “on both edges of S/D electrodes” (as shown in Fig. 2.3). We believe these testkeys will allow us to study the effect of the electrostatic effects on the energy band diagram in more detail. In short, the electrical properties of different top-gate positions will help us understand the metal-CNT interface characteristics further.

2. In Chapter 4, we also propose the possibility of altering the symmetry of SWNT-FETs by damaging the surface structure. In other words, the effective chirality of the SWNTs can be altered by Ar plasma treatment. More studies should be done to strengthen our hypothesis. Future research efforts should also be focused on further improving the parameters of the plasma treatment process by controlling the physical conditions of the process chamber.

3. In Chapter 5, we are still unable to grow CNTs with single chirality. In fact, the control over the chirality of the CNTs grown is the greatest challenge for all the researchers. Although we are now able to control the length of the CNTs growth by adjusting the growth temperature, hydrogen reduction time and the size of catalyst, yet in a batch of grown nanotubes we would still have both metallic and

semiconducting CNTs. Although our group can apply plasma treatment to increase the yield of the as-grown CNT-FETs, it is still an important topic to control the chirality of the CNTs and deserve further research efforts.

Publication List

International Journal

1. **Bae-Horng Chen,** Jeng-Hua Wei, Po-Yuan Lo, Zing-Way Pei, Horng-Chih Lin, Tien-Sheng Chao, and Tiao-Yuan Huang, "Novel Method of Converting Metallic-Type Carbon Nanotubes to Semiconducting-Type Carbon Nanotube Field-Effect Transistors," ***Japanese Journal of Applied Physics***, Vol. **45**, pp.3680-3685, April, 2006.
2. **Bae-Horng Chen,** Jeng-Hua Wei, Po-Yuan Lo, Hung-Hsiang Wang, Ming-Jinn Lai, Ming-Jinn Tsai, Tien Sheng Chao, Horng-Chih Lin, and Tiao-Yuan Huang, **"**A Carbon Nanotube Field Effect Transistor with Tunable Conduction-Type by Electrostatic Effects**"** ***Solid State Electronics***, accepted for publication, May, 2006.
3. **Bae-Horng Chen,** Jeng-Hua Wei, Po-Yuan Lo, Chien-Liang Hwang, Ming-Jinn Tsai, Horng-Chih Lin, Tien Sheng Chao, and Tiao-Yuan Huang, **"**Prospect of Cobalt-Mix-TEOS Method on Localized Lateral Growth of Carbon Nanotubes for Both P- and N-Type Field Effect Transistors**"**, ***Journal of Vacuum Science & Technology B***, accepted for publication, July, 2006.

International Letter

4. **Bae-Horng Chen**, Po-Yuan Lo, Jeng-Hua Wei, Ming-Jinn Tsai, Chien-Liang Hwang, Horng-Chih Lin, Tien-Sheng Chao, and Tiao-Yuan Huang, "Localized Lateral Growth of Single-Walled Carbon Nanotubes for Field-Effect Transistors by a Cobalt-Mix-TEOS Method," ***Electrochemical and Solid-State Letters***, Vol. **8**, pp.G290-G293, August, 2005.
5. **Bae-Horng Chen**, Jeng-Hua Wei, Hung-Hsiang Wang, Ming-Jinn Tsai, Horng-Chih Lin, Tien Sheng Chao, and Tiao-Yuan Huang, "Complementary Carbon Nanotube-Gated Carbon Nanotube Thin-Film Transistor," ***Appl. Phys. Lett.***, Vol. **88,** Issue: 9**,** p.93502, February, 2006.

International Conference Paper

6. **Bae-Horng Chen**, Po-Yuan Lo, Jeng-Hua Wei, Tien-Sheng Chao, and Tiao-Yuan Huang, "Localized Laterial Growth of Single-Walled Carbon Nanotube by Novel Cobalt Mix TEOS Method," in ***Twelfth Canadian Semiconductor Technology Conference***, p.105, Ottawa, Canada, 2005.
7. **Bae-Horng Chen,** Jeng-Hua Wei, Po-Yuan Lo, Ming-Jinn Tsai, Horng-Chih Lin, Tien-Sheng Chao, and Tiao-Yuan Huang, "A Novel Method to Convert Metallic-Type CNTs to Semiconducting-Type CNT-FETs," ***Solid State Devices and Materials Symp.***, pp.776-777, Kobe, Japan, 2005.
8. Jeng-Hua Wei, Ying-Ren Chen, Horng-Jiunn Lin, and **Bae-Horng Chen**, "Gate-Position Effects on Tunable Conduction-Type Carbon Nanotube Field Effect Transistors," in ***NT06 : Seventh International Conference on the Science and Application of Nanotubes***, Nagano, Japan, 2006.

Patent:

1. 駱伯遠、魏拯華、**陳百宏**、江日舜、黃建良、高明哲“形成奈米碳管與金屬複合材料的電鍍互連導線的方法”，中華民國專利、中國大陸專利與美國專利審查中，September 12, 2005。
2. **陳百宏**、魏拯華、駱伯遠、裴靜偉“製造奈米碳管場效電晶體之方法”，中華民國專利、中國大陸專利與美國專利審查中，December 29, 2005。

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2006 年 1 月~

博士論文題目:

新式奈米碳管電晶體製造與特性研究
A Study on the Fabrication and Characteristics of Novel Carbon Nanotube Field-Effect Transistors