國 立 交 通 大 學

電子工程學系電子研究所

碩 士 論 文

應用於 Serial ATA 6Gb/s
之展頻時脈產生器

A Spread Spectrum
Clock Generator for Serial ATA 6Gb/s
Application

研 究 生：黃 彥 穎

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A Spread Spectrum Clock Generator for 6 Gb/s Serial ATA Applications

研 究 生：黃彥穎　　Student：Yen-Ying Huang

指導教授：周世傑　　Advisor：Prof. Shyh-Jye Jou

國　立　交　通　大　學

電子工程學系 電子研究所碩士班

碩　士　論　文

A Thesis

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in Partial Fulfillment of the Requirements

for the Degree of

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In

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中華民國　九十六　年　十二　月


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應用於 Serial ATA 6Gb/s 之展頻時脈產生器

研究生：黃彥穎　　指導教授：周世傑 博士

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摘要

展頻技術主要是對時脈信號的頻率做調變，使得信號能量平均分散到較為寬大的頻譜內。降低其在頻譜上相對應的能量峰值。本論文先簡單的介紹鎖相迴路的設計觀念，並提出了展頻的穩態以及暫態現象的分析與鎖相迴路系統參數的關係，使得我們可以得到一個較佳的設計概念。並解決了在多工器操作之下，所造成不當的信號突波。為了保證電路操作的穩定性，我們同時採取了數位控制的解決方法，來保證相位變化是單調且一致的。在鎖相迴路中，為了減小時脈抖動，我們採取錯誤放大器的方式來解決電路操作中電流不匹配的問題，同時採用三階迴路濾波器濾除鎖相迴路中週期性的突波現象。我們在振盪器中加入被動電阻，以降低對震盪器輸入端的敏感度並提高線性度；又加入交互偶合電晶體來加速震盪器震盪轉態的操作。

我們所提出的展頻時脈產生器主要應用於 Serial ATA 6Gbps 中，向下展頻 5000ppm 同時採用三角波調變且調變頻率為 30KHz。此展頻時脈產生器使用和差調變器及相位旋轉方式完成之。此電路是在 90 奈米互補式金氧半的製程下所製

造。展頻時脈最大週期對週期時脈抖動為 1.13ps 並操作在 1.4GHz 時消耗 7.57 毫瓦。能量峰值所能降低的最大數量為 20.6dB。晶片面積分為: 鎖相迴路主要電路$170\times80um^2$，迴路濾波器$235\times325um^2$，相位旋轉單位$170\times20um^2$。

A Spread Spectrum Clock Generator for 6Gb/s Serial ATA Application

Student：Yen-Ying Huang Advisor：Prof. Shyh-Jye Jou

Department of Electronics Engineering

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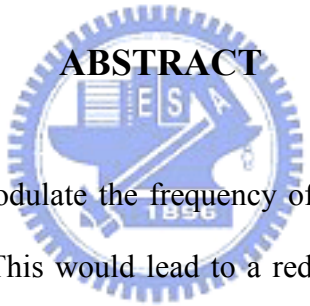
National Chiao Tung University



ABSTRACT

Spread spectrum is to modulate the frequency of clock and to spread the clock energy in a wider spectrum. This would lead to a reduction of the peak level of the clock energy. In this thesis, we will describe the phase-locked loop (PLL) design considerations first. Then, we will introduce the steady-state and transient analysis of spread spectrum behavior. These can help us to express the SSCG design consideration with PLL parameters. We also use the interpolation technique to avoid the glitch problem due to the operation of multiplexer and provide a thermal code control to guarantee the monotonic behavior in the process of phase rotation.

In the PLL design, we achieve low jitter issue by using error amplifier to resolve the current mismatch in charge pump and a third order loop filter is adopted to reduce the reference spur. A passive resistor is presented in the VCO delay cell to reduce the K_{vco} gain and an additional cross-couple CMOS is also included to the delay cell to

boost the operation of delay cell. Our spread spectrum clock generator (SSCG) for Serial ATA Specification is down spread 5000ppm with a triangular modulation profile and the modulation frequency is 30 kHz. A spread spectrum technique using PLL with a sigma delta modulator and phase rotation algorithm is proposed. This proposed architecture has been designed in a 90-nm CMOS process. The spread clocking has a peak-to-peak cycle-to-cycle jitter of 1.13ps and consumes 7.57mW at 1.4GHz. The EMI reduction in this circuit is about 20.6dB. The core area includes PLL Main Circuit ($170 \times 80 um^2$), Loop Filter ($235 \times 325 um^2$) and Phase Rotation Block ($170 \times 20 um^2$).

誌 謝

碩士生涯兩年半即將到一段落，兩年半的時間中受到許多人的幫助才使得我能夠順利的在今天拿到學位。特別要感謝我的指導教授周世傑老師在這段時間對我的指導，不只在研究方面給予我指引，同時鞭策我使我能有更為嚴謹的研究態度，也感謝老師對於散漫的我的諄諄教誨。另外還要感謝一直以來帶著我做研究的 totoro 學長，能夠不厭其煩的引領我進入這個領域，還有志龍學長，在 modeling 以及 layout 量測部分給予我很大的幫助；另外就是我的研究夥伴 apu，這段時間的互相討論跟合作，一起熬夜趕 tape-out，我想以後這會是一段想起來有點痛苦不過又值得回味的回憶。

我也要感謝 316 實驗室的同學們，碩一的時候常常一起熬夜寫作業、吃火鍋、打電動、打紙棒球的俊男、國光、俊誼、建君、apu、晉欽讓我的碩士生涯豐富不少，我想我很難忘記那段瘋狂 AOC 的時候，我也是唯一被老闆抓到兩次的傢伙。另外就是學妹 van、學長庭禎、小胖組成了八卦閒聊組合，雖然很多東西都是唬爛的，不過卻也充滿歡笑。還有誠文、momo 在研究上及找國防役的時候給我的建議；蔡 group 的宜興、珣益、茂成在研究上的協助；還有我一大堆的球友:企鵝、昭安、孟祺、阿國..，讓我在研究所生涯中保持強健的體魄。

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Chapter 1
Introduction

1.1 Introduction to High-Speed Serial Link

The multi-gigabit transmission through wire has been applied extensively. There are two approaches for such high speed applications: parallel buses and serial link buses. The conventional parallel buses would contribute the complexity of routing and additional power consumption. For this reason, the high speed serial link buses become more attractive one for high speed application. Another property of high speed serial link is easy to do port expansion. A new function or capability is added to the PC, a new defined interface addresses the demand.

However, it is unfortunate that off-chip (I/O) bandwidth has not grown up with the increasing operating frequency. Due to the limited bandwidth of transmission line (I/O), there are new challenges in the design of high speed system. Channel, transmitter and receiver should be worked together to achieve low cost and high performance design.

There are high speed serial link standards are defined over short distance in copper cable or longer distance in fiber, such as Serial ATA, IEEE1394b and so on. Table.1.1 makes a list of some industrial standards [1].

Table.1.1 Industrial standard for high speed serial link

Standard	USB2.0[1]	IEEE1394b[2]	Serial ATA[3]	Parallel ATA
Speed	480Mbps	1.6-3.2Gbps	1.5/3/6Gbps	1.33Gbps max
Max. Cable length	5m	4.5m	1m(3Gbps)	0.46m
Hot Swappable	Yes	Yes	Yes	No

1.2 Timing Specifications and Application Issues

Serial Advanced Technology Attachment (SATA) [3] is a computer bus for connecting the storage devices and a computer. SATA uses only four signal lines, allowing the more compact cables than PATA. It also offers the new features, including hot swapping as shown in Table.1.1.

The serial ATA 1.0a targeted at the interface between desktop PC motherboard, devices, CD ROMs, and DVD ROMs. Serial SATA Ⅱ[3]expands the application of serial ATA 1.0a. We will show some potential applications which take advantage of new features in Serial SATA Ⅱ. The SATA Ⅱ supports several kinds of connections, including:

A. Internal 1 meter cabled host to device

B. Short backplane to device

C. Long backplane to device

D. Internal 4-lane cabled serial ATA disk arrays

E. System to system interconnect-data center application

F. System to system interconnects-external desktop applications

G. Proprietary serial ATA disk arrays

Serial ATA also offers the use of spread spectrum clocking (SSC). The goal of this modulation is to decrease the peak spectral energy of the clocking to mitigate the interference to peripheral device. The related spread spectrum parameters are shown in Table.1.2. Modulation frequency must locate in the range of 30 to 33 KHz. The modulation frequency deviation is requested to down spread within -5000ppm to 0ppm. The instantaneous frequency of clock should fall into the T_{UI} range. The f_{tol} specifies the permissive frequency variation from nominal except the frequency variation because of jitter, spread spectrum clocking, or phase noise of clock source.

Table.1.2 General Specifications of SATA Gen2 [3]

Parameter	Units	Limit	SATA Usage Model
T_{UI}, unit interval	*ps*	Min	333.2167
		Nom	333.3333
		Max	333.1167
f_{tol}, Frequency Long term Stability	*ppm*	Min	-350
		Max	+350
Spread-Spectrum Modulation Frequency	kHz	Min	30
		Max	33
Spread-Spectrum Modulation Deviation	*ppm*	Min	-5000
		Max	0

Both Serial Attached SCSI-2(SAS-2) and PCI express also adopt the SSC application. Accordingly, the related spread spectrum parameters in different standard

are shown in Table.1.3.

Table.1.3 General Specifications and Comparison of SSC in different standards

Standard	SATA		SAS-2		PCI express	
Spread Spectrum Modulation Frequency	30~33kHz		30~33kHz		30~33kHz	
SSC modulation type	Down spreading	0/-5000 ppm	Center spreading	+2300/-2300 ppm	Down spreading	0/-5000 ppm
			Down spreading	0/-2300 ppm		
Frequency Long term Stability	+-350ppm		+-100ppm		+-300ppm	

We give an example of modulation profile for down spreading illustrated in Fig.1.1 [3]. Where f_{nom} is the nominal frequency of clock source in non-SSC mode, f_m is the modulation frequency, δ is the modulation frequency deviation and t is the time. The EMI reduction of SSC is defined as Δ as shown in Fig.1.2.

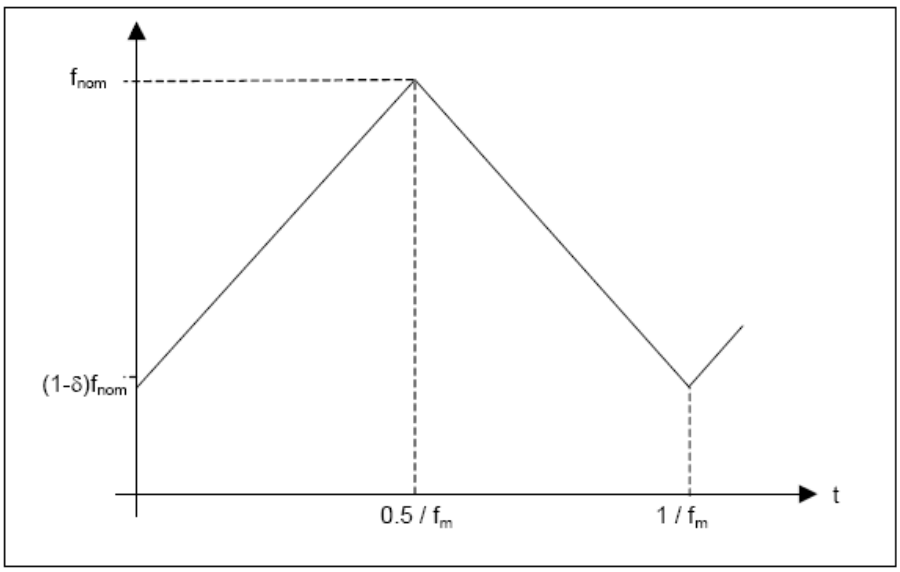


Fig.1.1 Triangular modulation profile of SSC

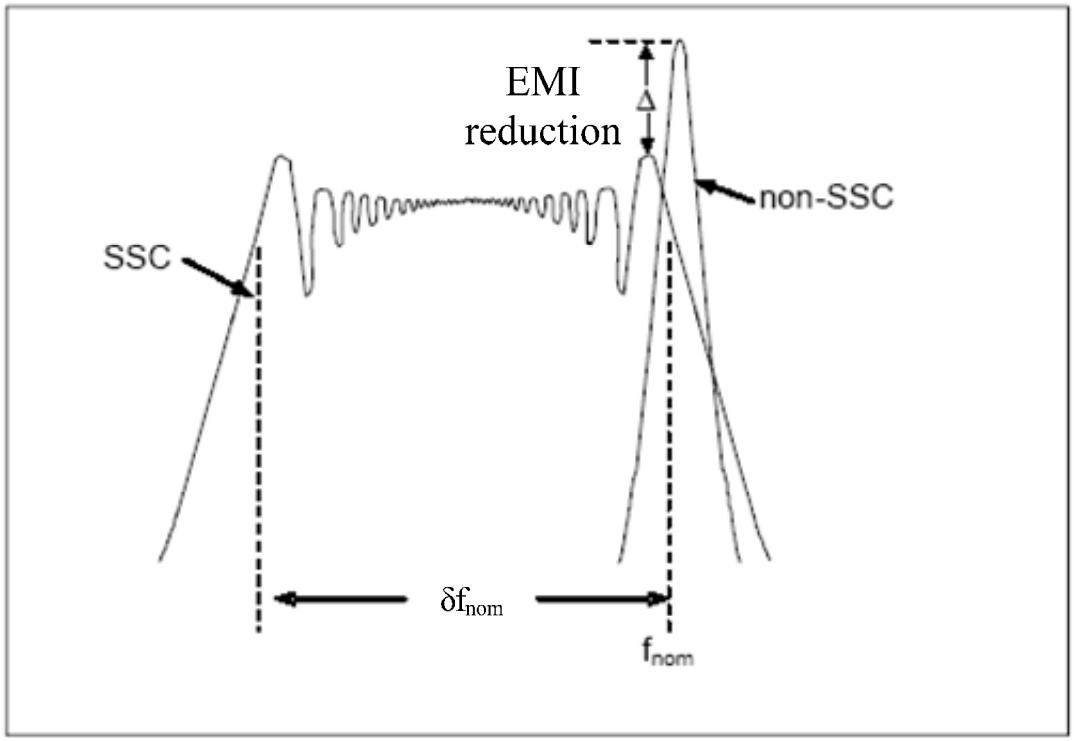


Fig.1.2 Spread spectrum clocking and non-spread mode comparison[3]

1.3 Motivation

As the higher operation speed is required, the signals pose more stringent timing requirement. Hence, a pure and stable clock source is needed to achieve the skew reduction and improve the overall system timing. With the shrinking tolerance of jitter, the low jitter design of PLL has become a challenge. Besides, the application of PLL has appeared in many domains. For examples, frequency synthesizer, clock and data recovery, frequency multiplication, and clock de-skew are different applications of PLL systems.

Spread spectrum techniques are methods by spreading the signal energy in the frequency domain. These techniques are used for EMI reduction. In real world, the synchronous systems radiate electromagnetic energy in the clock frequency and its

harmonics. This electromagnetic interference might cause damage to the peripheral storages and other signal processing unit. To not exceed the regulative limit of electromagnetic interference, the Serial ATA defines the EMI reduction using spread spectrum clocking.

Spread spectrum clocking techniques have been frequently needed in portable device due to faster clock frequency and the highly integrated LCD displays in a small device. On the other hand, heavy metal shielding is not the low-cost option in the lightweight portable device. For active EMI reduction methods such as SSC, some challenges are existed for circuit designer because the modified clock doses not align any more in the synchronous system. The transmitter and receiver run into new difficulties in this SSC system due to the occurrence of the deterministic timing jitter.

1.4 Thesis Organization

This thesis is divided into six chapters. Experimental verifications is presented in fifth chapter as the circuit implementation, rather than being isolated in a separate chapter.

Chapter 1 introduces the high speed serial link and some of the industrial standards. The applications concerned with SATA are also mentioned. SATA specifications about spread spectrum clocking are introduced. The motivation and goals are described for this thesis. Finally, the structure of this thesis is presented.

Chapter 2 covers the mathematical development of a linear PLL for conventional continuous-time s-domain analysis. The conventional analysis method is divided into closed-loop and open-loop analysis.

Chapter 3 reviews the common modulation mechanisms nowadays. This review

also shows and compares the corresponding noise trnasfer function among them. A discrete-time open loop approach for analyzing the spread spctrum transient behavior is addressed. The transient response of spread spectrum clocking behavior is then carried out. Finally, the overall process of spread spectrum will be carried out and then the analysis of the quantization noise due to sigma delta modulation is included. The timing impact involves the cycle-to-cylce jitter is developed in the end of this chapter.

Chapter 4 describes the concept of the proposed SSC and a steady state formula is reviewed first. Then, phase rotation mechnism and design details are covered. The last section introduces the phase rotation with sigma delta modulation method.

Chapter 5 shows the impelemenation of each circuit block, including PLL subblocks and spread spectrum blocks. The behavior simulation is included to obtain the design parameters in PLL at the same time. The measurement setup and experimental results are presented in the final section.

Chapter 6 gives a conclusions and future works are recommended at the end of this thesis.

Chapter 2
Principles of Phase-Locked Loop

2.1 Introduction to PLL

Phase-locked loop is an electrical control system that generates a signal with a fixed relation to the phase of reference input. A phase-locked loop regulates the phase and frequency of an oscillator until it matches to the reference input in phase and frequency. Additionally, a phase-locked loop is an example of the control system with negative feedback.

Phase-locked loop is used widely in synchronous system, the main applications comprises clock and data recovery, de-skewing, clock generation, spread spectrum, clock distribution and so on.

Clock and data recovery [4]**:** A serial data is sent without clock signal across the channel to the receiver. A clock is recovered from the incoming data at the receiver end by the way of a clock and data recovery circuit.

De-skewing [5]**:** A clock signal is amplified or buffered before it can drive the electrical component, such as CPU, MEM and I/O. As a result, the received clock experiences the timing skew among these electrical blocks. To eliminate the delay, a de-skew PLL is included at the receiver side.

Clock generation [16]**:** In most electrical system, the operating frequency of each processor is quite different from each other for different purpose. The clock sources from PLL supplies these processors, which multiply the low frequency of crystal oscillator by a multiplication ratio.

Spread spectrum [9]**:** All electrical system radiate electromagnetic interference. Many regulatory agencies put the limit on the emitted energy. A circuit designer can adopt a spread spectrum PLL to reduce this interference.

Clock distribution [5]**:** A PLL drives the clock distribution that is usually balanced and arrive the endpoints simultaneously. A PLL compares one of the endpoints with the reference clock and then changes its phase and frequency to align the incoming reference clock.

Classification of phase-locked loop consists of linear PLL, digital PLL and all digital PLL [6]. A linear PLL is composed of analog input and analog circuit. A digital PLL is formed by a digital input, partial digital circuit and partial analog circuit. An all digital PLL consists of all digital circuits. Our design is based on the digital PLL.

2.2 Analysis of PLL Linear Model

A digital PLL is usually built of phase frequency detector, charge pump, loop filter and voltage control oscillator (VCO) with dividing by N negative feedback. This kind of system is shown conceptually in Fig.2.1. The phase frequency detector compares the phase difference between the reference input and the feedback signal from the VCO dividing by N. The purpose of the charge pump is to convert the logic states of the PFD into analog signals suitable for VCO. Therefore, the phase difference message is sent to the loop filter to establish a control signal on VCO. The

VCO is an oscillator that generates a periodic output signal depending on the input control voltage from the loop filter. The frequency feedback ratio $N = \frac{f_{out}}{f_{ref}}$ is provided by a divider so that PLL's output signal frequency is an integer multiple of the reference.

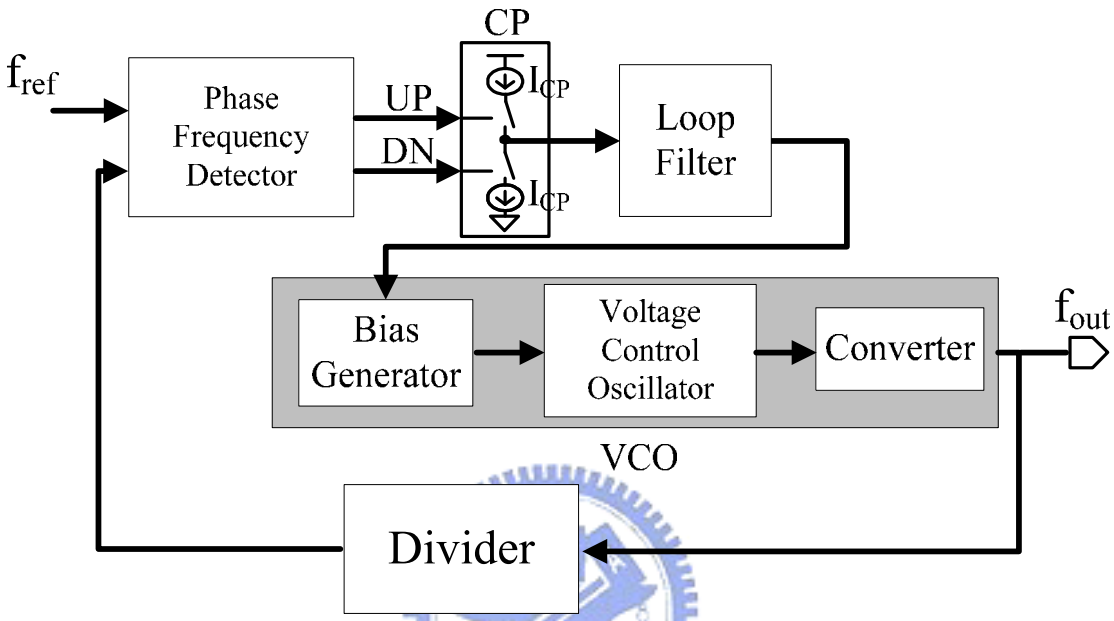


Fig.2.1 A General PLL block diagram

The only digital block is the phase detector and the remaining blocks are similar to the linear PLL. A linear model can also be used for analyzing digital PLL by making some assumption. The first assumption describes that the loop bandwidth of the PLL system, which presents the response rate of the PLL, should be about 1/20 of the reference frequency. The continuous-time approximation holds true in such a case. We also assume that the discrete-time operation of the charge pump can be approximated to its average behavior. The average error current i_e over one cycle is $i_e = I_p \times \frac{t_p}{T_{ref}} = \frac{I_p}{2\pi} \times \theta_e$ where t_p is the turn-on time of either UP or DN equaling

to $|\theta_e| / \omega_{ref}$, T_{ref} is the input reference clock cycle, I_p means the charge pump current, and θ_e presents the phase error between the input reference clock f_{ref} and feedback clock signal f_{out}/N. A linear model of a digital PLL is shown in Fig.2.2.

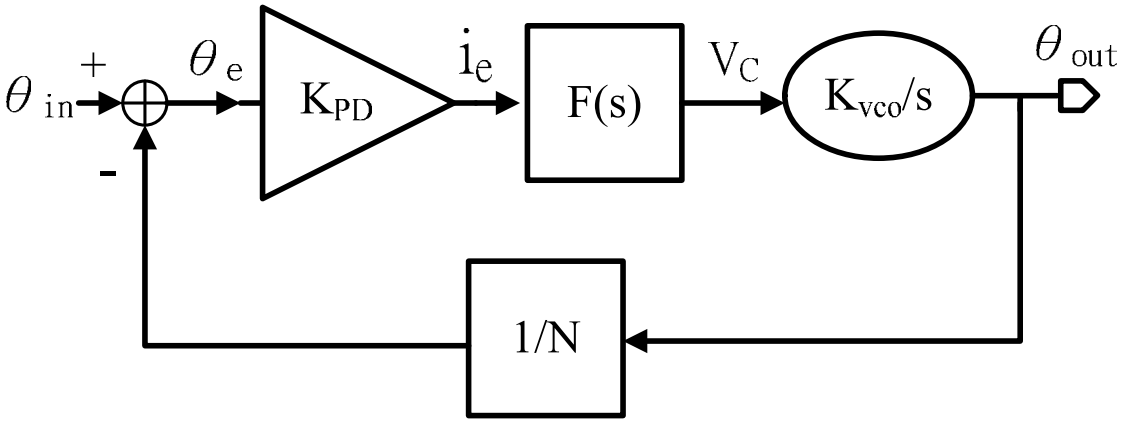


Fig.2.2 A equivalent linear model of a digital PLL

2.2.1 Analysis of Closed Loop Transfer Function

We will develop a closed loop transfer function based on [7]. If the average error current i_e is shown as above, the VCO control voltage can be expressed as

$$V_C(s) = i_e(s)F(s)$$
$$= \frac{I_P}{2\pi}\theta_e(s)F(s) \qquad (2.1)$$

where $i_e(s)$ is the Laplace transformation of i_e and F(s) describes the loop filter transfer function. The VCO output phase is given by

$$\theta_{out}(s) = V_C(s)\frac{K_{VCO}}{s} \qquad (2.2)$$

These formulas would lead to a loop transfer functions, H(s) as

$$H(s) = \frac{\theta_{out}(s)}{\theta_{in}(s)} = \frac{K_{VCO} I_P F(s)}{2\pi s + K_{VCO} I_P F(s)} \tag{2.3}$$

$$1 - H(s) = \frac{\theta_e(s)}{\theta_{in}(s)} = \frac{2\pi s}{2\pi s + K_{VCO} I_P F(s)} \tag{2.4}$$

Equation (2.3) indicates low-pass filtering characteristic from the PLL input to its output with dc gain equaling to unit. It indicates that the change in the output will be identical to input variation as long as tracking time is long enough and F(0)=∞.

A steady state phase error θ_s will arises when PLL experiences a frequency step $\Delta\omega$. Apply the final value theorem, the steady state phase error can be found to be

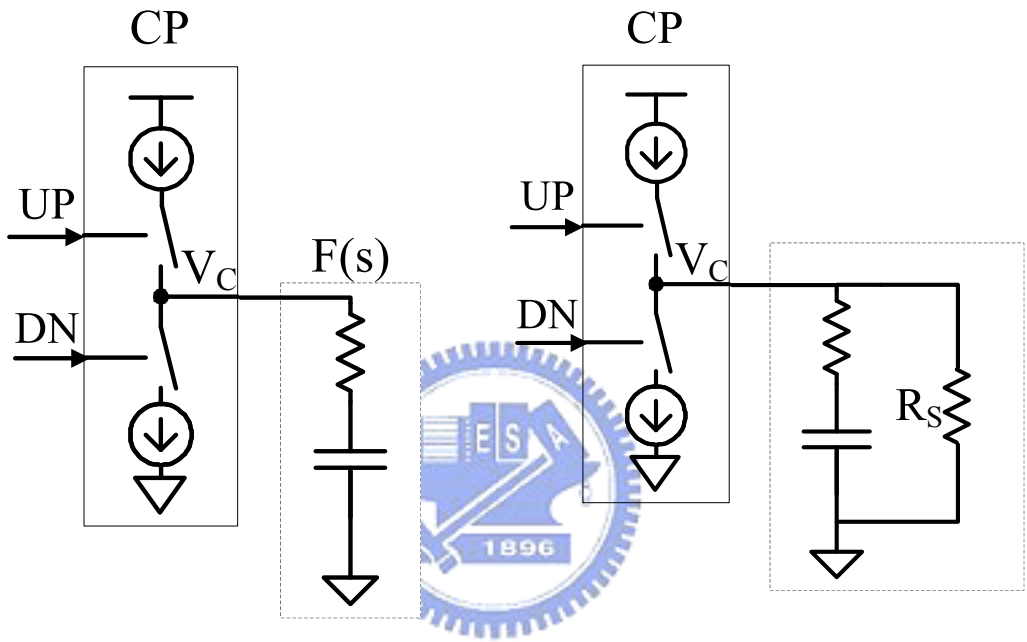
$$\theta_s = \left. \frac{2\pi\Delta\omega}{K_{VCO} I_P F(s)} \right|_{S=0} rad \tag{2.5}$$

Note that the result from (2.5) can be derived regardless of the type of the loop filter. It is necessary to turn the dc gain of the loop filter into an infinite value for the zero steady state phase error when a frequency offset is existed between the input reference clock and free-running frequency of the VCO. This important property implies that a dc pole is required in the loop filter.

A traditional second order loop PLL which is produced by a series connection of a resistor and a capacitor is shown in Fig.2.3 (a). Fig.2.3 (b) shows the practical circuit with a shunting resistance denoted as R_S. The shunt loading is most likely to come from the input resistance of the VCO. The actual steady state phase error shown in (2.5) will be changed to

$$\theta_s = \frac{2\pi\Delta\omega}{K_{VCO} I_P R_S} rad \tag{2.6}$$

Note that in equation (2.6), the steady state phase error is inverse proportional to the shunting resistance, R_S. Thus, a large shunting resistive loading or a capacitive loading seen from the VCO input terminal is preferred to guarantee zero steady state phase error. Hence, a bias generator not only provides a bias voltage to VCO but also prevent the shunting resistance seen at the VCO input from connecting with loop filter.



(a) (b)

Fig.2.3 (a) Traditional 2nd order PLL loop filter and (b) A shunt loading is included in the practical circuit

2.2.2 Analysis of Open Loop Transfer Function

The closed loop analysis usually involves the second order PLL whose loop filter composes of a series resistance and a capacitance. The critical drawback of this second order PLL is that each time a charge pump current is injected into the loop filter, the control voltage experience a large voltage jump. The resulting ripple

severely disturbs the VCO, corrupting the output phase. Therefore, additional pole is required to alleviate the voltage ripple. Another reason for higher order design of a PLL is to eliminate the reference spur due to the periodic operation of PFD, charge pumping circuit and frequency divider. Especially for low cycle-to-cycle jitter design of a SSCG, the reference spur becomes more serious owing to the phase rotation per reference clock cycle. Consequently, for a high order PLL, the natural frequency and damping factor of a second order PLL are no longer suitable for the analysis of the system stability. An open loop analysis is generally used to meet the stability issue of higher order PLL. Here we show the third order PLL analysis in analytic form and express the forth order PLL with rough approximation.

The concept of the phase margin is commonly adopted in the analysis of the open loop control system. Usually, 60 degree of phase margin is adopted and Fig.2.4 represents the loop filter of a third order PLL.

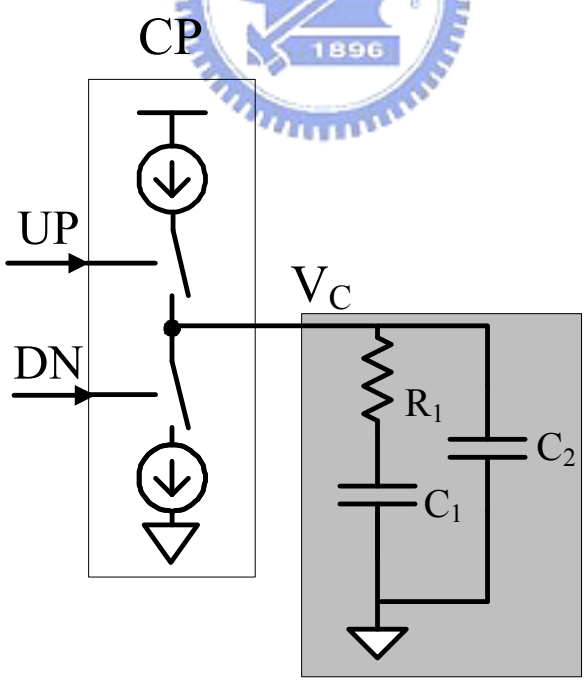


Fig.2.4 Third order charge pump PLL with additional C_2

We rewrite the loop filter transfer function

$$\frac{V_C(s)}{\theta_e(s)} = K_{PD}F(s) = \frac{I_P}{2\pi}[(R_1 + \frac{1}{sC_1}) \| \frac{1}{sC_2}]$$

$$= \frac{I_P}{2\pi s(C_1 + C_2)} \times \frac{sR_1C_1 + 1}{sR_1(C_1 \| C_2) + 1}$$

$$\omega_z = \frac{1}{R_1C_1}; \omega_P = \frac{1}{R_1(C_1 \| C_2)} \tag{2.7}$$

A general derivation of PLL open loop transfer function can be developed as follows

$$\frac{V_C(s)}{\theta_e(s)} = \frac{I_P}{2\pi s(C1+C2)} \times \frac{1 + s/\omega_z}{1 + s/\omega_p}$$

$$L(s) = \frac{V_C(s)}{\theta_e(s)} \times \frac{K_{VCO}}{s} \times \frac{1}{N}$$

$$= \frac{K_{VCO}I_P}{2\pi s^2 N(C1+C2)} \times \frac{1 + s/\omega_z}{1 + s/\omega_p} \tag{2.8}$$

where L(s) is the open loop gain transfer function, substitute $s = j\omega$ into (2.8) to obtain the amplitude response and phase response of the open loop transfer function

$$L(s)|_{s=j\omega} = -\frac{K_{VCO}I_P}{2\pi\omega^2 N(C1+C2)} \times \frac{1 + j\omega/\omega_z}{1 + j\omega/\omega_p} \tag{2.9}$$

$$\angle L(j\omega) = \tan^{-1}(\omega/\omega_z) - \tan^{-1}(\omega/\omega_P) - \pi \tag{2.10}$$

$$\frac{d\angle L(j\omega)}{d\omega}|_{\omega_C} = \frac{1/\omega_x}{1 + (\omega/\omega_z)^2} - \frac{1/\omega_p}{1 + (\omega/\omega_p)^2} = 0$$

$$\Rightarrow \omega = \omega_c = \sqrt{\omega_z\omega_p}$$

$$= \frac{1}{R1C1}\sqrt{1 + \frac{C1}{C2}} \tag{2.11}$$

We will find a maximum phase margin as $\omega = \omega_t$ where ω_t is the unit gain frequency of the open loop transfer function. That is, if we choose $\omega_t = \omega_c$, the third

order PLL has the maximum phase margin. The corresponding phase margin is

$$\phi_p = \tan^{-1}\left(\frac{\sqrt{\omega_z \omega_p}\left(\frac{1}{\omega_z} - \frac{1}{\omega_p}\right)}{2}\right) \tag{2.12}$$

$$= \tan^{-1}\left(\frac{\sqrt{\frac{C_1 + C_2}{C_2}} - \sqrt{\frac{C_2}{C_1 + C_2}}}{2}\right) \tag{2.13}$$

Given the unit gain frequency ω_t and the phase margin ϕ_p, we obtain the relative design parameters shown as below

$$C_2 = \frac{\omega_z}{\omega_p} \frac{K_{PD} K_{VCO}}{\omega_t^2 N} \sqrt{\frac{1 + (\omega_t / \omega_z)^2}{1 + (\omega_t / \omega_p)^2}} \tag{2.14}$$

$$C_1 = C_2\left(\frac{\omega_p}{\omega_z} - 1\right) \tag{2.15}$$

$$R_1 = \frac{1}{\omega_z C_1} \tag{2.16}$$

$\frac{\omega_p}{\omega_t} = \frac{\omega_t}{\omega_z} = \frac{1}{4}$ gives a phase margin $\approx 60^\circ$

As mentioned above, the forth order PLL with third order loop filter can be illustrated in Fig.2.5. The design consideration is more complicate and a simple analytic equation cannot be derived in the forth order PLL. The lower of the frequency of the third pole in the loop filter would attenuate frequency spur more but reduce the stability margin. For a third order loop filter, the added attenuation from the R_2 and C_3 can be approximated as a low-pass filter

$$Attenuation = 20\log[(\omega_{ref} R_2 C_3)^2 + 1] \tag{2.17}$$

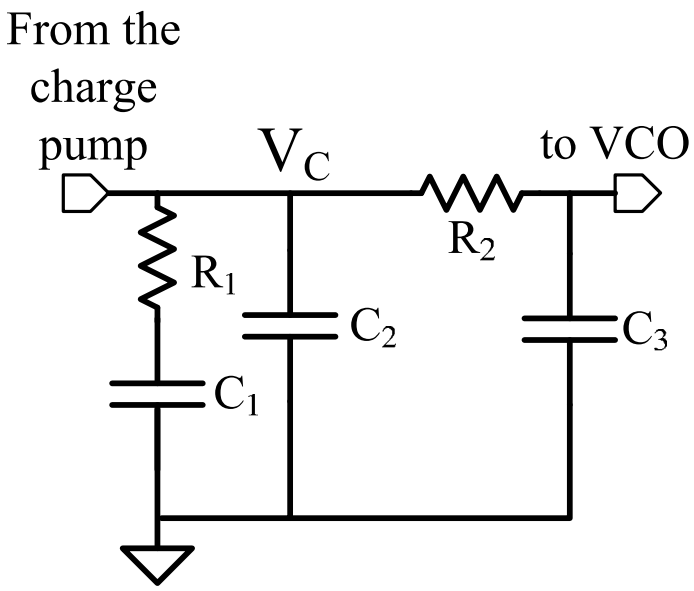


Fig.2.5 Third order loop with additional R_2 and C_3

Chapter3

Analysis of Spread Spectrum Clock Generator

3.1 Spread spectrum Mechanism

With the development of high performance computer and peripheral systems, the operation speed is in GHz range. The high-speed signal interface between transmitter and receiver contributes most of noise in the system. These signals often generate Electric-Magnetic Interference (EMI) that affects the operation of other equipments. When the operation speed is higher, the EMI problem is more severe. Thus, the popular promising technology like Serial-ATA defines the EMI reduction using spread-spectrum clocking has been explored [8] [9] [10] [11].

This section includes two subsections. The first subsection shows the different modulation mechanism. In the second subsection, we address the issue related to noise transfer function in the SSC. We also refer the effective phase jump of all methods to the input of PLL to do the transient analysis for all different modulation mechanism.

3.1.1 Introduction to Modulation Mechanism

In general, there are four types of modulation mechanism in SSCG, that is,

modulation on VCO, modulation on input reference clock, modulation on divider and modulation with phase selection method. Fig.3.1 shows that modulating the output clock of a PLL by giving periodic drift on VCO control voltage with another charge pump used is in [8]. This is an analog technique that suffers new jitter source from the analog modulator and the process variation will affect the performance of SSCG.

The SSCG technique with modulation on input reference clock is presented in [9] and is shown in Fig.3.2. Because of the phase selection using multiplexer, glitch problem is very series. Moreover, the glitch will cause an injected noise and the noise transfer function in that port has very large DC gain. This poor noise transfer function will be shown in the next subsection.

Another SSCG type is to utilize modulation on divider [10] as shown in Fig.3.3. It has the same noise transfer function as the second method. Moreover, this technique could not achieve high modulation profile precision. Thus, the low jitter requirement cannot be satisfied.

Finally, the phase selection from the coherent multi-phase output of PLL is reported [11] and shown in Fig.3.4. Unfortunately, techniques in [10] and [11] both suffers serious glitch problem because of the operation of multiplexer.

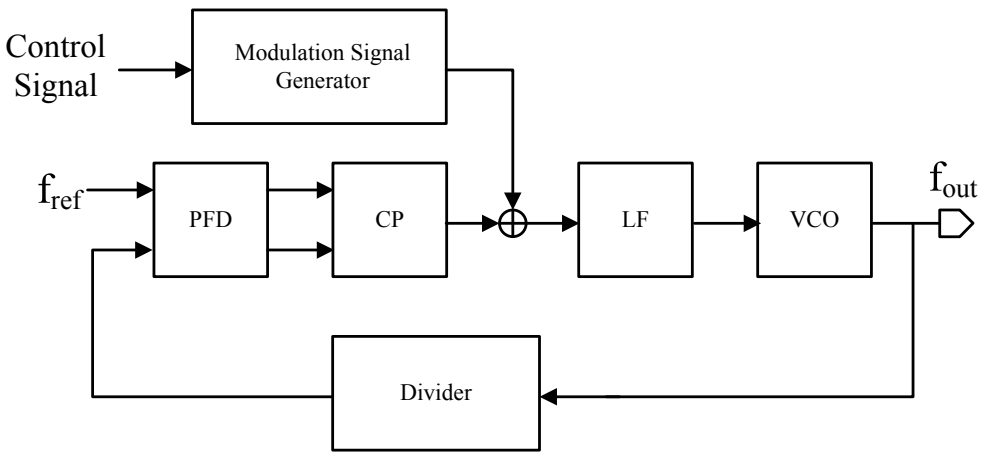


Fig.3.1 Block diagram of a SSCG with modulation on VCO

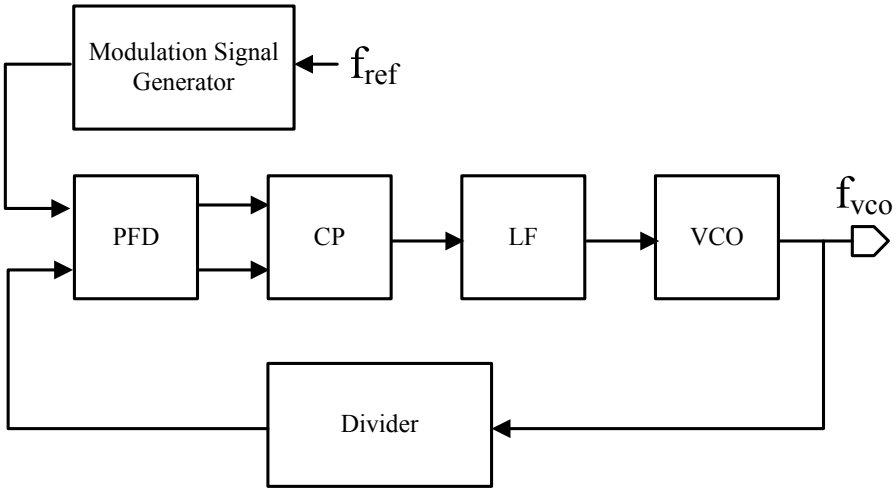


Fig.3.2 Block diagram of a SSCG with modulation on input reference clock

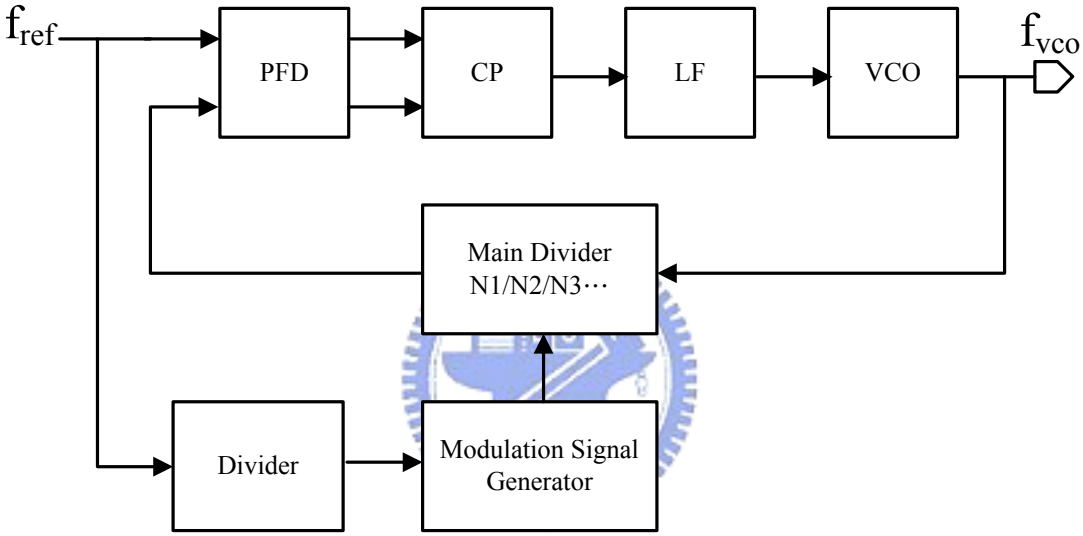


Fig.3.3 Block diagram of a SSCG with modulation on divider

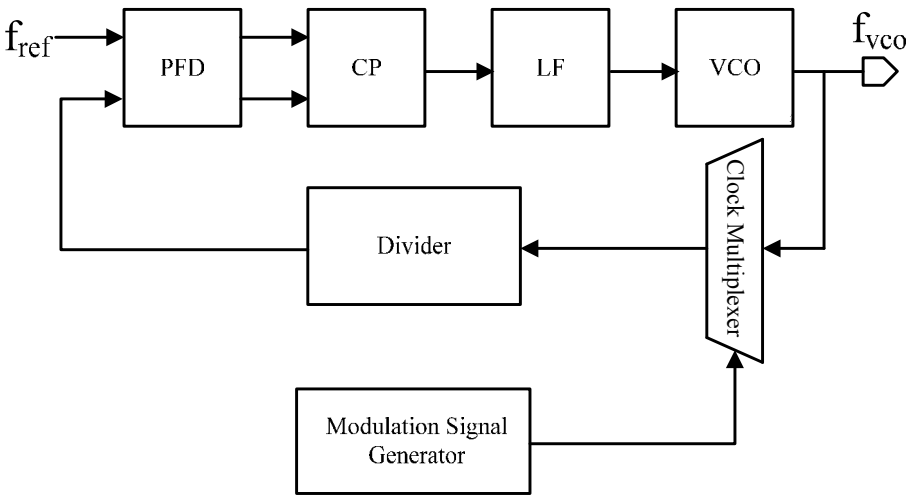


Fig.3.4 Block diagram of a SSCG with phase selection method

3.1.2 Noise Transfer Function

We derive the noise transfer function of each modulation mechanism to understand the noise performance of each of them. To do this, we can choose one of them as our basic modulation method to minimize quantization noise due to digital signal processing.

Fig.3.5 illustrates the equivalent linear model of each modulation mechanism. K_{PD} is the gain of phase detector, F(s) means the transfer function of the loop filter, K_{VCO} is the sensitivity of voltage control oscillator, and 1/N represents the divider ratio. The quantization noise of each method is listed below:

- ϕ_{out} presents the output noise due to the quantization noise
- ϕ_{in} models the quantization noise of a SSCG with modulation on input reference clock
- ϕ_c models the quantization noise of a SSCG with modulation on VCO
- ϕ_r models the quantization noise of a SSCG with phase selection method
- ϕ_d models the quantization noise of a SSCG with modulation on divider

The quantization noise and effective phase variation of each modulation method is shown below. The noise transfer function of each modulation method is given by

$$\frac{\phi_{out}}{\phi_{in}} = \frac{K_{PD}F(s)K_{VCO}}{s + \frac{1}{N}K_{PD}F(s)K_{VCO}} \tag{3.1}$$

$$\frac{\phi_{out}}{\phi_{C}} = \frac{F(s)K_{VCO}}{s + \frac{1}{N}K_{PD}F(s)K_{VCO}} \tag{3.2}$$

$$\frac{\phi_{out}}{\phi_r} = \frac{\frac{-1}{N}K_{PD}F(s)K_{VCO}}{s+\frac{1}{N}K_{PD}F(s)K_{VCO}} \tag{3.3}$$

$$\frac{\phi_{out}}{\phi_d} = \frac{-K_{PD}F(s)K_{VCO}}{s+\frac{1}{N}K_{PD}F(s)K_{VCO}} \tag{3.4}$$

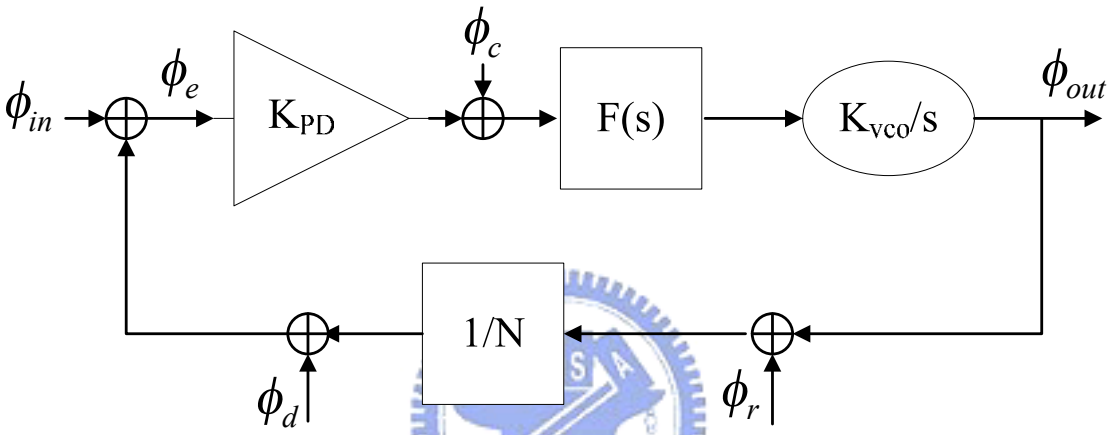


Fig.3.5 Noise transfer function of each modulation mechanism

As shown in the Eqn.(3.1) to (3.4) , all of them reveal the low frequency passing characteristic. Therefore, the sigma-delta modulation is usually adopted to implement the modulation signal generator and the analysis of the quantization noise is almost the same. Although all the noise transfer function presents the same low-pass character, they have different DC gain. This feature makes the quantization noise effect quite different. Inserting s=0 in Eqn.(3.1) to (3.4) , we find the respective DC gain:

$$\left.\frac{\phi_{out}}{\phi_{in}}\right|_{S=0} = N \tag{3.5}$$

$$\left.\frac{\phi_{out}}{\phi_C}\right|_{S=0} = \frac{N}{K_{PD}} \tag{3.6}$$

$$\left.\frac{\phi_{out}}{\phi_r}\right|_{S=0} = -1 \tag{3.7}$$

$$\left.\frac{\phi_{out}}{\phi_d}\right|_{S=0} = -N \tag{3.8}$$

Note that the DC gains are greater than one except the phase selection method. The quantization noise will be amplified through the PLL loop due to the closed loop gain. To achieve the same noise level at the output of PLL, a higher order of the sigma-delta modulation is required when the DC gain is higher. Thus, our design is based on the phase selection method published in [11].

Due to the same filter attribute, the transient response of spread spectrum behavior of a SSCG will be realized with modulation on input. All the other modulation mechanism can be accomplished with the corresponding input referred signal at the phase detector input. Using the concept, we can begin our transient response analysis with corresponding input referred signal at the phase detector input.

3.2 Discrete-Time Open-Loop Criteria of PLL

At first, we introduce the traditional continuous-time model of a second-order linear PLL based on [12] as shown in Fig.3.6 and then a discrete-time open loop analysis depending on [12]. Here the two tracking path are modeled as the gain of proportional path K_P and the gain of integral path K_I. The integral path helps to

suppress the static phase error because it provides infinite gain in the open loop of PLL. However, the integral path might make the loop of PLL unstable as a result of two poles at DC. Hence, a compensating zero or a proportional path is needed to stabilize the loop. As shown in Fig.3.6, the integral path sets one of the VCO frequency term to a time-integral of the past phase error with a gain K_I. The proportional path sets the other frequency term of the VCO proportion to the current phase error.

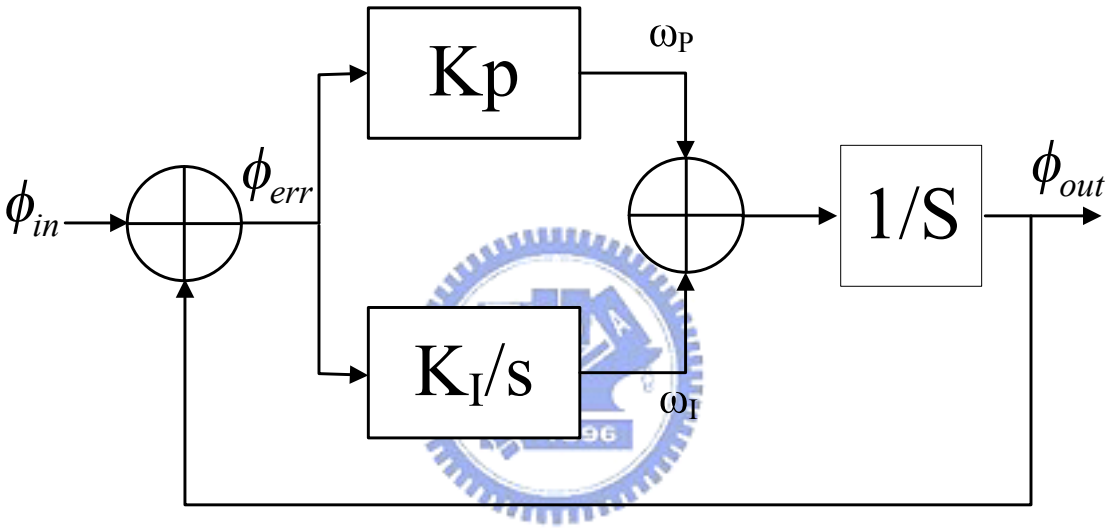


Fig.3.6 Continuous-time model of a second-order linear PLL

Note that we will make a link between open loop transfer function and closed loop transfer function to find the relationship of proportional gain K_P and integral gain K_I to natural frequency ω_n and damping factor ξ. To do this, the open-loop transfer function of the PLL, $L_{PLL}(s)$, defined as $\phi_{out}(s) / \phi_{err}(s)$, is

$$L_{PLL}(s) = \frac{\phi_{out}(s)}{\phi_{err}(s)}$$

$$= \frac{sK_P + K_I}{s^2} \qquad (3.9)$$

then, the closed loop transfer function $H_{PLL}(s) = \phi_{out}(s) / \phi_{in}(s)$ is

$$H_{PLL}(s) = \frac{L_{PLL}(s)}{1 + L_{PLL}(s)}$$

$$= \frac{sK_P + K_I}{s^2 + sK_P + K_I}$$

$$= \frac{2\xi\omega_n s + \omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \tag{3.10}$$

From the derivation above, we can express ω_n and ξ in terms of K_P and K_I

$$\omega_n = \sqrt{K_I} \tag{3.11}$$

$$\xi = \frac{K_P}{2\omega_n} = \frac{K_P}{2\sqrt{K_I}} \tag{3.12}$$

We can express the proportional gain K_P and integral gain K_I with circuit design parameters such as charge pump current I_P, sensitivity of VCO K_O, C_1 in loop filter and R_1 in loop filter. From (3.11) and (3.12), K_I and K_P can be expressed as

$$K_I = K_O \times \frac{I_P}{C_1} \tag{3.13}$$

$$K_P = I_P \times R_1 \times K_O \tag{3.14}$$

Equation (3.13) implies that integral gain is proportional to the voltage slew rate of C_1 in the loop filter with a proportional constant K_O. The proportional gain is directly proportional to the voltage drop $I_P R_1$. From this point of view, we can explain

the PLL loop characteristic in discrete time.

The above system behavior involves continuous-time quantity. But ϕ_{err} is actually a sampled value when phase detector detects the phase error. The phase comparison can occur only once per cycle. Therefore, a PLL shall be described with discrete-time open loop characteristics. Fig.3.7 shows the discrete-time model of a PLL.

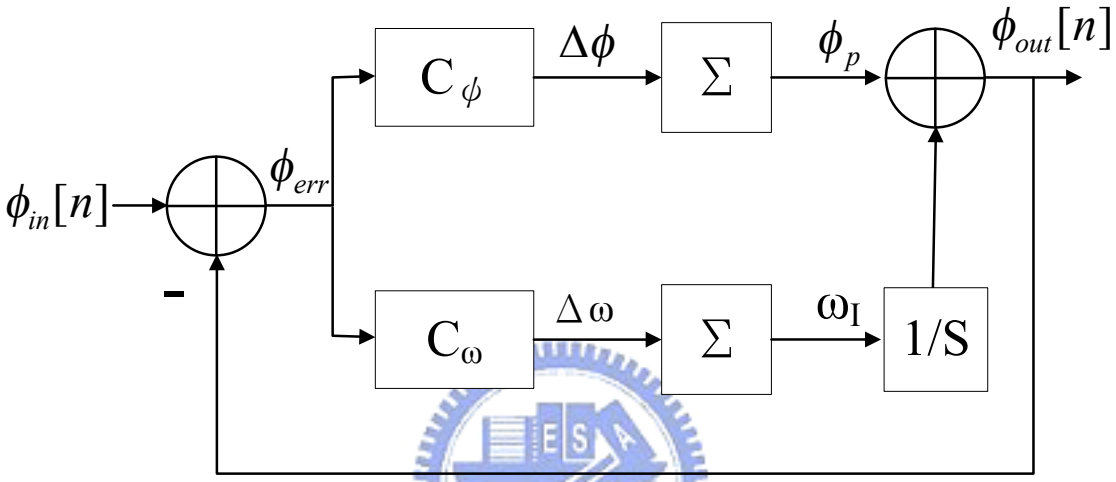


Fig.3.7 A discrete-time PLL models the changes in phase $\Delta\Phi$ and in frequency $\Delta\omega$ of each cycle due to the sampled phase error $\phi_{err.}$

As shown in Fig.3.6, the integral frequency term $\omega_I = K_I \phi_{err}(s)/s$ can be regarded as a discrete-time summation

$$\omega_I[n] = \omega_I(nT_{ref}) = \sum_{i=-\infty}^{n-1} K_I T_{ref} \phi_{err}(iTref) \tag{3.15}$$

T_{ref} is the input reference clock period. A similar derivation can be carried out about the proportional frequency term $\omega_P(s) = K_P \phi_{err}(s)$. If the resulting phase $\phi_P = \omega_P(s)/s$ is considered as the output, the corresponding discrete-time description can be expressed as

$$\phi_P[n] = \phi_P(nT_{ref}) = \sum_{i=-\infty}^{n-1} K_P T_{ref} \phi_{err}(iTref) \tag{3.16}$$

Following from equation (3.15) and (3.16), the frequency ω_I and the phase ϕ_P shown in Fig.3.7 were updated the in each cycle. The modified quantities in each input reference clock cycle will be proportional to the current sampled phase error $\phi_{err.}$

$$\Delta\omega = \omega_I[n] - \omega_I[n-1]$$

$$= K_I T_{ref} \phi_{err} = \frac{2\pi K_I}{\omega_{ref}} \phi_{err} \tag{3.17}$$

$$\Delta\phi = \phi_P[n] - \phi_P[n-1]$$

$$= K_P T_{ref} \phi_{err} = \frac{2\pi K_P}{\omega_{ref}} \phi_{err} \tag{3.18}$$

Equation (3.17) and (3.18) describes the open-loop dynamic equation that models the change in phase and frequency due to each sampled phase error. Since $K_I = \omega_n^2$ and $K_P = 2\xi\omega_n$, (3.17) and (3.18) become

$$\begin{aligned} \Delta\omega &= 2\pi\omega_{ref}\left(\frac{\omega_n}{\omega_{ref}}\right)^2 \phi_{err} \\ \Delta\phi &= 4\pi\xi\frac{\omega_n}{\omega_{ref}}\phi_{err} \end{aligned} \tag{3.19}$$

We have derived the discrete-time open-loop criteria of a PLL. The dynamic equation describes change of frequency and phase in each cycle. This property can

help us to do transient response of spread spectrum behavior with PLL system parameters such as ω_n and ξ.

3.3 Transient response of Spread Spectrum

With the derivation of the discrete-time open-loop criteria of a PLL, we can analyze spread spectrum behavior using digital signal processing. As shown in Fig.3.1, Fig.3.2, Fig.3.3 and Fig.3.4, Modulation Signal Generator is usually a digital processing block clocked by input reference clock of PLL by a specified ratio. Hence, we can develop the difference equation of spread spectrum behavior according to the concept of discrete-time open-loop criteria of a PLL.

The understanding of transient response of spread spectrum behavior can help to express the SSCG design requirement with PLL system parameters. As will be shown later, we will discover that the design consideration of SSCG would be different with different PLL system parameters.

In section 3.3.1, we discuss the behavior of SSC and model it as a equivalent difference equation expressed with PLL system parameters such as ω_n and ξ. Thus, in section 3.3.2, we will display the transient response with different PLL system parameters and discuss about the design consideration. Finally, we show the effective frequency of spread spectrum clocking.

3.3.1 Equivalent Difference Equation of SSC

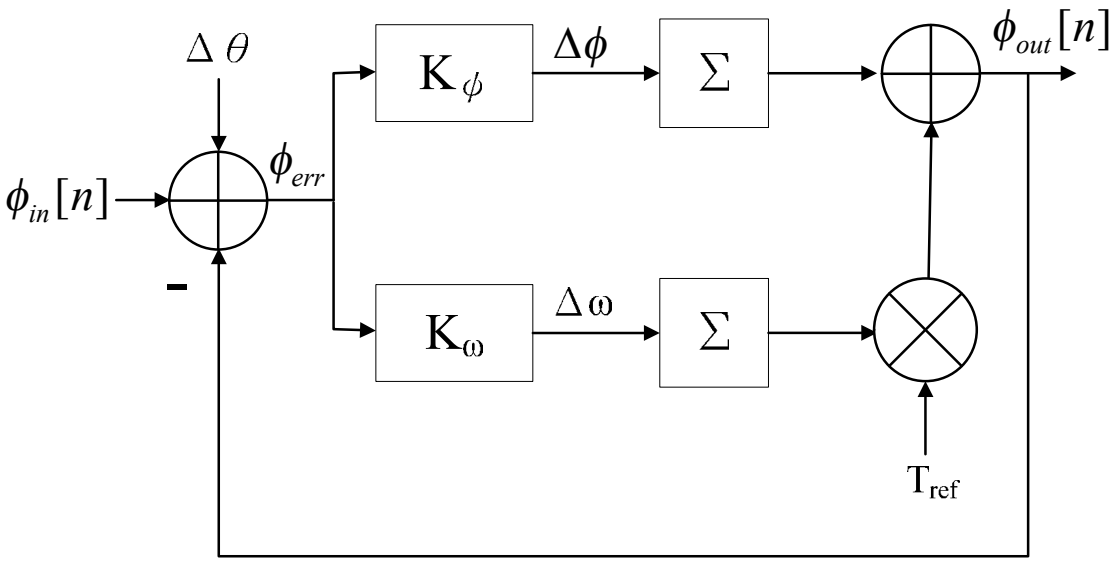


Fig.3.8 A modified discrete-time PLL model

To derive the difference equation of spread spectrum behavior from equation (3.19), we redraw the discrete-time PLL model as shown in Fig.3.8. Where K_ω and K_ϕ are the open-loop integral gain and open-loop proportional gain, respectively and are as defined as in Eqn.(3.19). T_{ref} is the input reference clock period to present the integration operation. Note that the spread spectrum behavior is performed when the PLL is in lock. Consequently, to produce spread spectrum equivalent frequency in each modulation mechanism, the effective phase jump at different location in the PLL loop can be transferred to input to simplify our analysis. And then the spread spectrum equivalent frequency can be modeled as a phase jump $\Delta\theta$ per reference clock cycle time. We neglect the input reference clock induced phase noise. So $\phi_{in}[n]$ equals to zero for simplifying analysis. Hence, we formulate the block diagram and display the phase error at each sampling time

$$\phi_{err}[1] = \Delta\theta$$

$$\phi_{err}[2] = \phi_{err}[1] - (\Delta\omega[1] \times T_{ref} + \Delta\phi[1]) + \Delta\theta$$

$$\phi_{err}[3] = \phi_{err}[2] - (\Delta\omega[2] \times T_{ref} + \Delta\phi[2]) + \Delta\theta - \Delta\omega[1] \times T_{ref}$$

$$\phi_{err}[4] = \phi_{err}[3] - (\Delta\omega[3] \times T_{ref} + \Delta\phi[3]) + \Delta\theta - T_{ref} \times (\Delta\omega[1] + \Delta\omega[2])$$

.....

$$\phi_{err}[n] = \phi_{err}[n-1] - (\Delta\omega[n-1] \times T_{ref} + \Delta\phi[n-1]) + \Delta\theta - T_{ref} \times (\Delta\omega[1] + ... + \Delta\omega[n-2])$$

We rearrange the equation mentioned above into the following

$$\phi_{err}[n] = \phi_{err}[n-1] + \Delta\theta - \Delta\phi[n-1] - T_{ref} \times (\Delta\omega[n-1] + .. + \Delta\omega[1]) \qquad (3.20)$$

Again, we can express the difference equation of $\phi_{err}[n]$ in terms of open-loop gain K_{ω}, and K_{ϕ}, effective phase jump $\Delta\theta$, and T_{ref} that represents the integration operation. The new equation of $\phi_{err}[n]$ is

$$\varphi_{err}[n] = (1 - K_{\varphi})\varphi_{err}[n-1] - T_{ref} \times K_{\omega} \sum_{i=1}^{n-1} \varphi_{err}[i] + \Delta\theta \qquad (3.21)$$

We can analyze system response in discrete-time method based on (3.21) with K_{ω} and K_{ϕ} describing the characteristic of the PLL system. We can also demonstrate the same system response in both open loop and closed loop description.

3.3.2 Transient Response of SSC with different PLL system parameters

In section 3.3.1, we discuss and derive the equivalent difference equation of

spread spectrum behavior. In this section, we will display and discuss the system response with different system parameters. Table.3.1 shows some general settings of PLL system parameters. These include ω_n and ξ and substitute ω_n and ξ into the open-loop parameters, K_ω and K_ϕ to get the relative value.

Table.3.1 The relative open-loop parameters according to different closed-loop parameters

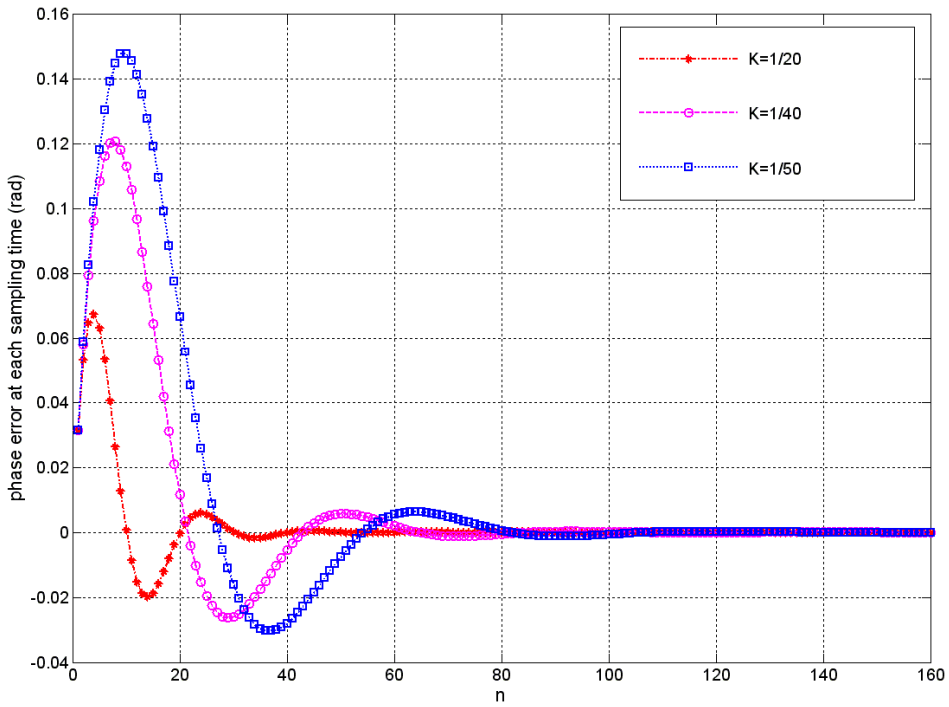
$\xi = \frac{1}{\sqrt{2}}$	$\frac{\omega_n}{\omega_{ref}} = \frac{1}{20}$	$\frac{\omega_n}{\omega_{ref}} = \frac{1}{40}$	$\frac{\omega_n}{\omega_{ref}} = \frac{1}{50}$
$T_{ref} \times K_\omega$	$\frac{1}{100}\pi^2$	$\frac{1}{400}\pi^2$	$\frac{1}{625}\pi^2$
K_φ	$\frac{\sqrt{2}}{10}\pi$	$\frac{\sqrt{2}}{20}\pi$	$\frac{\sqrt{2}}{25}\pi$

$\xi = 1$	$\frac{\omega_n}{\omega_{ref}} = \frac{1}{20}$	$\frac{\omega_n}{\omega_{ref}} = \frac{1}{40}$	$\frac{\omega_n}{\omega_{ref}} = \frac{1}{50}$
$T_{ref} \times K_\omega$	$\frac{1}{100}\pi^2$	$\frac{1}{400}\pi^2$	$\frac{1}{625}\pi^2$
K_φ	$\frac{1}{5}\pi$	$\frac{1}{10}\pi$	$\frac{2}{25}\pi$

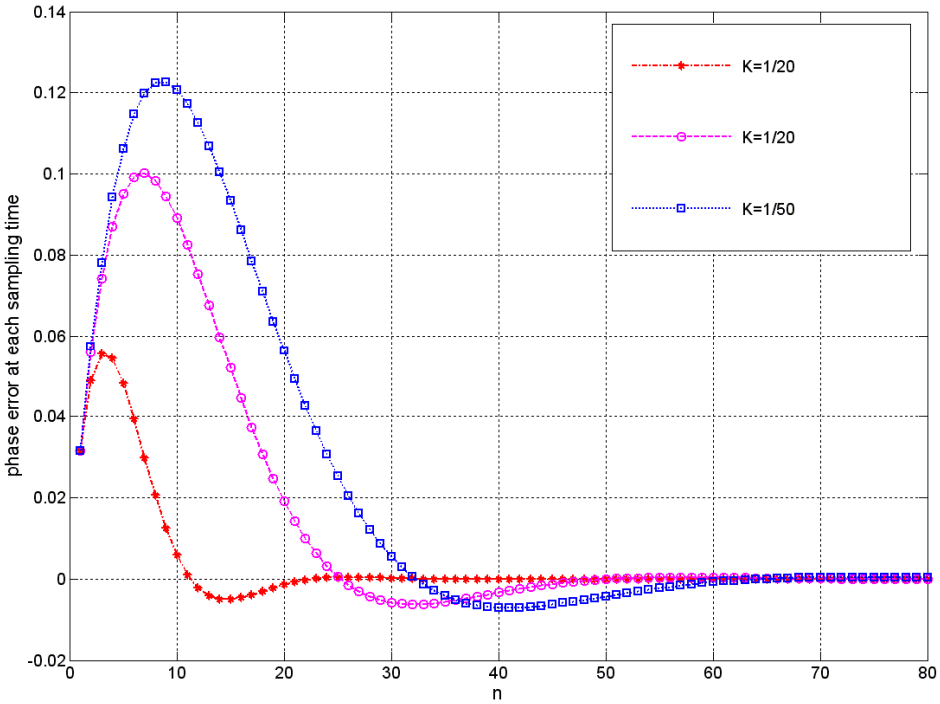
$\xi = 3$	$\frac{\omega_n}{\omega_{ref}} = \frac{1}{20}$	$\frac{\omega_n}{\omega_{ref}} = \frac{1}{40}$	$\frac{\omega_n}{\omega_{ref}} = \frac{1}{50}$
$T_{ref} \times K_\omega$	$\frac{1}{100}\pi^2$	$\frac{1}{400}\pi^2$	$\frac{1}{625}\pi^2$
K_φ	$\frac{3}{5}\pi$	$\frac{3}{10}\pi$	$\frac{6}{25}\pi$

$\xi = 0.5$	$\frac{\omega_n}{\omega_{ref}} = \frac{1}{20}$	$\frac{\omega_n}{\omega_{ref}} = \frac{1}{40}$	$\frac{\omega_n}{\omega_{ref}} = \frac{1}{50}$
$T_{ref} \times K_{\omega}$	$\frac{1}{100}\pi^2$	$\frac{1}{400}\pi^2$	$\frac{1}{625}\pi^2$
K_{φ}	$\frac{1}{10}\pi$	$\frac{1}{20}\pi$	$\frac{1}{25}\pi$

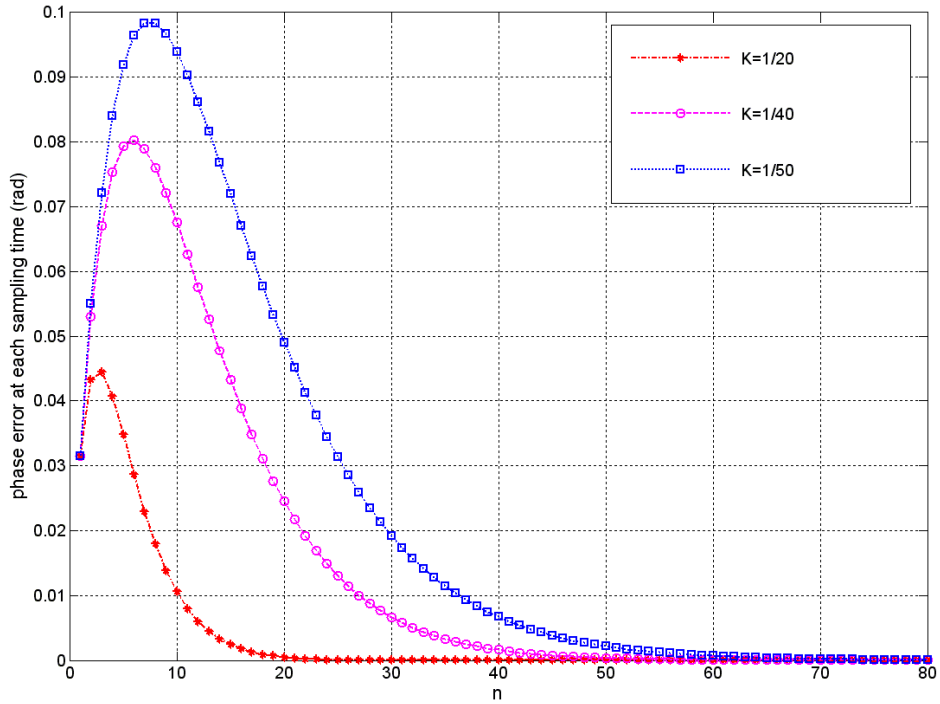
We simulate the difference equation (3.21) in Matlab with corresponding coefficient settings in Table.3.1. The test pattern is 5000ppm frequency deviation with effective input referred phase jump= $\frac{1}{100}\pi$ at the phase detector input and the sampling frequency equals the input reference clock frequency. We define the ratio $\frac{\omega_n}{\omega_{ref}}$ = K.



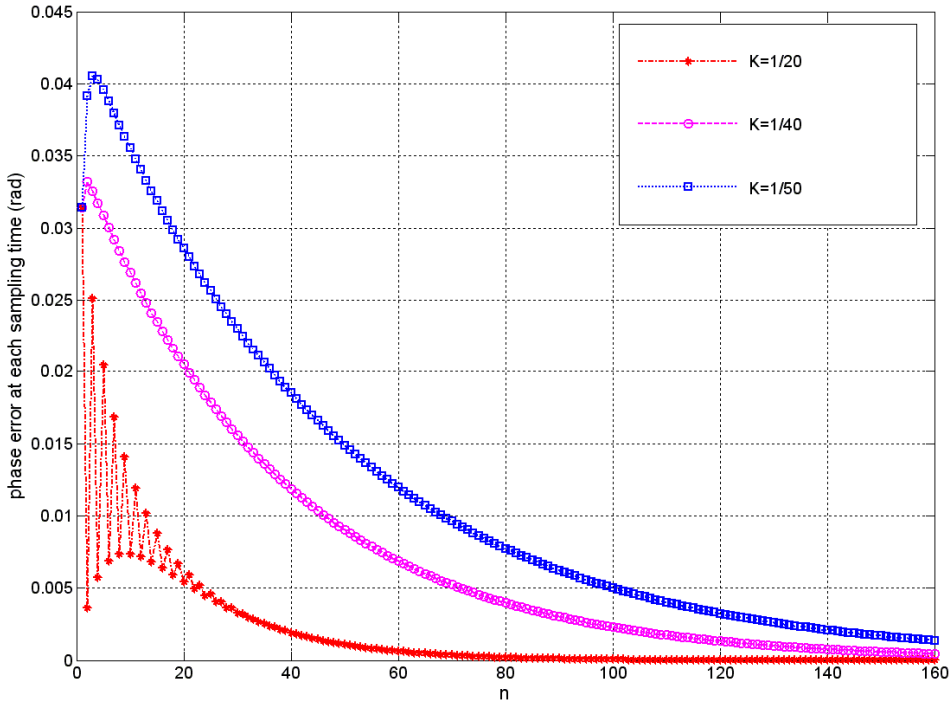
(a)


K=1/20
K=1/20
K=1/50
phase error at each sampling time
n

(b)


K=1/20
K=1/40
K=1/50
phase error at each sampling time (rad)
n

(c)



(d)

Fig.3.9 Transient response of phase error $\varphi_{err}[n]$ with damping factor (a) 0.5, (b) 0.707, (c) 1 and (d) 3

Notice that we make some observations could be made on the results of Fig.3.9 and Table.3.1.

(1) We note that the damping factor ξ does not affect the open-loop integral gain.

(2) Open-loop phase tracking gain K_ϕ is directly proportional to damping factor ξ.

(3) When the natural frequency to input clock frequency ratio $\frac{\omega_n}{\omega_{ref}}$ is determined, the corresponding frequency tracking gain is also decided.

From the observations above, the four cases all shows that the larger the $\frac{\omega_n}{\omega_{ref}}$, the faster the system response. It means that the frequency tracking gain increases as $\frac{\omega_n}{\omega_{ref}}$ is increased with phase tracking gain unchanged. Hence, the tracking process is performed more quickly. We also note that for under damping ones, Fig.3.9 (a) and (b),

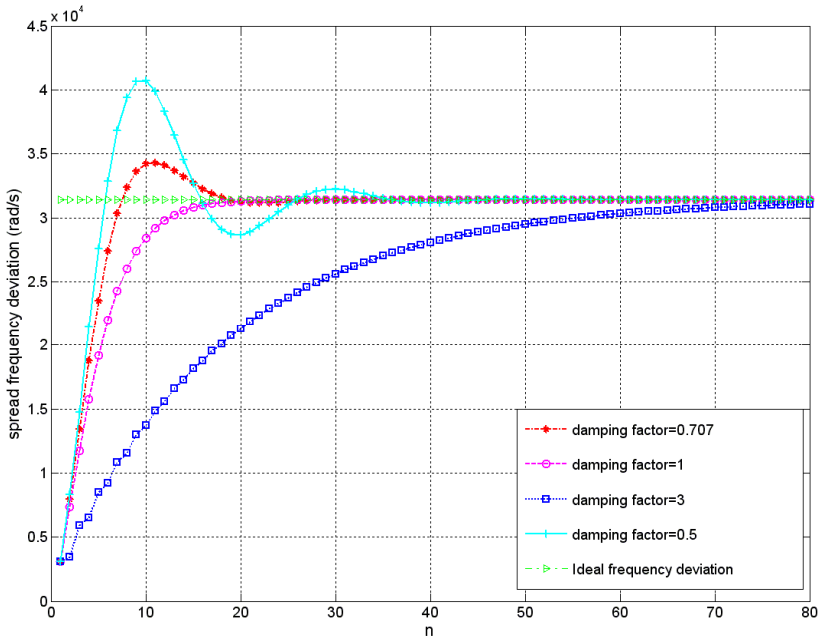
there are oscillations before the settling point is approaching. This shows the same transient behavior as the conventional continuous-time one. With the discrete-time analysis, we have the other exposition about the oscillations before settling. The frequency tracking gain is too large relative to phase tracking gain. Therefore, the frequency tracking would exceed the desired frequency jump and then the phase error will ring because of the wrong frequency tracking direction. Similarly, as shown in Fig.3.9 (d), over damping case will slow down the system response as the conventional one. The phase error tracking would oscillate at the beginning due to the large phase tracking gain. The large phase tracking gain slows down the frequency tracking action because the phase error φ_{err} could not stay high radians for enough time to complete frequency tracking.

3.3.3 Effective Spread Frequency with Different Phase Jump

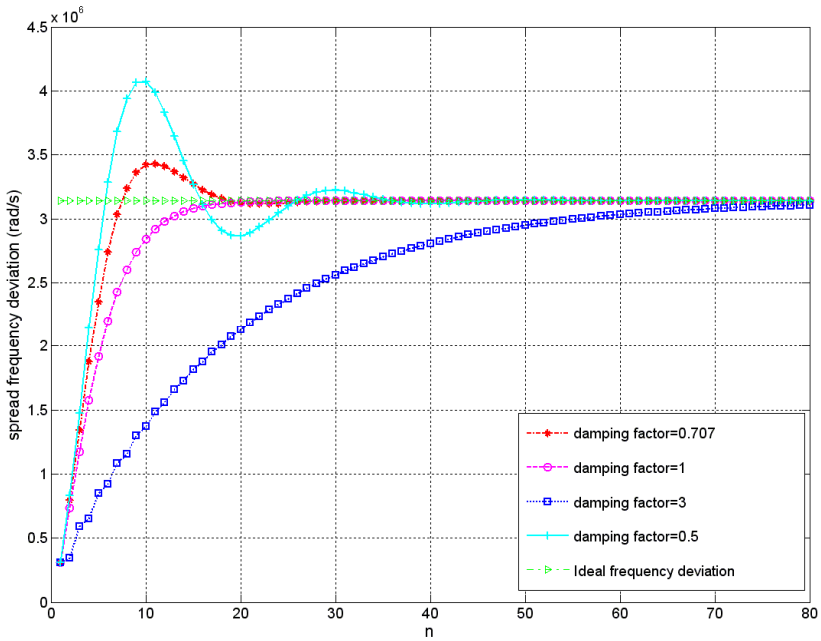
In fact, the effective spread spectrum frequency tracking is more interested in system behavior. In this section, we will show the frequency tracking behavior to prove that the discussion in section 3.3.2 and examine the effect on the amount of phase jump $\Delta\theta$.

The popular promising technology like Serial-ATA defines the EMI reduction using spread-spectrum clocking with 5000ppm frequency deviation. When the spread spectrum is performed with digital signal processing, the desired triangular modulation profile will like a triangular modulation profile with stairs. The number of stairs and step size of the stair might affect the outcome of spread spectrum behavior. As can be shown from Fig.3.10, the transient response is just like the traditional step response of a PLL system because the phase jumps at each phase detection works

equivalent to a frequency step applied to a PLL system.



(a)



(b)

Fig.3.10 Transient response of spread frequency deviation with (a) 50ppm (b) 5000ppm

As can be seen in Fig.3.10 (a) and (b), the response behaviors are almost the same except the scale of the vertical axis. The response time of a system is regardless of the spread frequency deviation. This is because in the linear-time invariant system, the output response is scaled by the same factor when the input is scaled by a factor. Therefore, the change of the amount of phase jump will not influence system response.

To reach the specification of spread frequency deviation, we would like to have fewer stairs in our triangular modulation profile when the response time of the system is long.

3.4 Overall Spread Spectrum Behavior

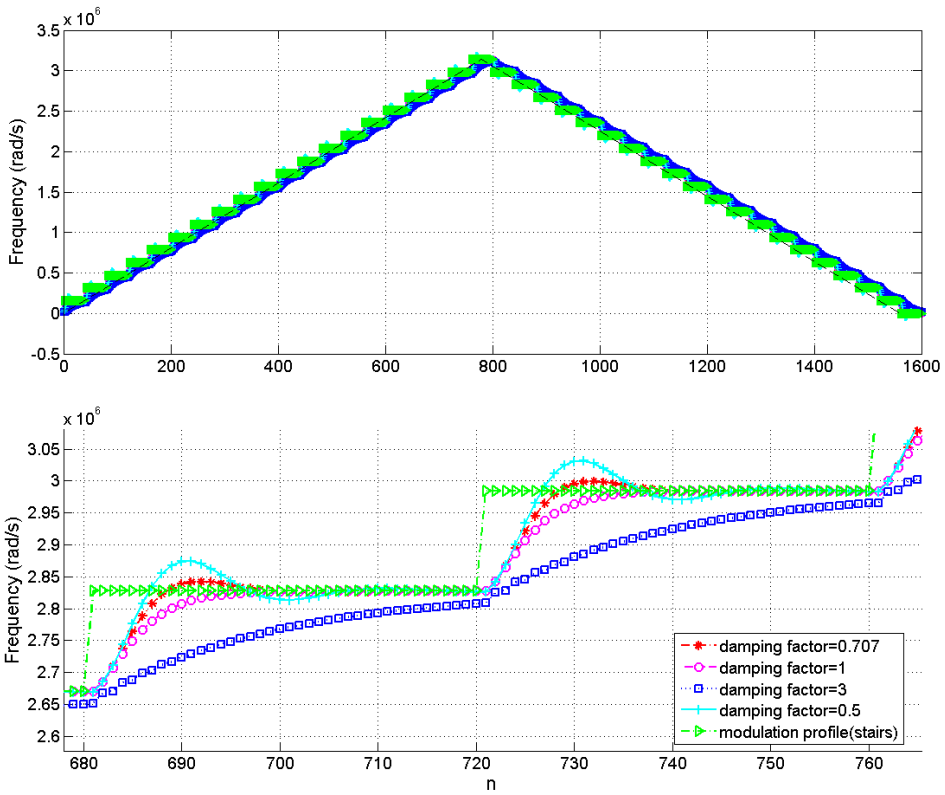
In this section, the overall spread spectrum behavior will be shown with different system parameters. Design consideration to achieve the maximum reduction of clock power and minimum cycle-to-cycle jitter of SSCG will be discussed.

It should be note that quantization noise is induced when the digital signal processing schemes are used. We first describe the overall spread spectrum behavior without quantization noise to survey the response behavior when different design parameters are used. Secondly, suppose we are designing the block of the spread spectrum circuit using digital method. We can anticipate that quantization error is produced through the digital operation. Sigma-delta modulation skill is usually used to push the quantization noise to high frequency band. Consequently, the analysis of the sigma delta modulation is included. First order and second order delta sigma modulation will be introduced.

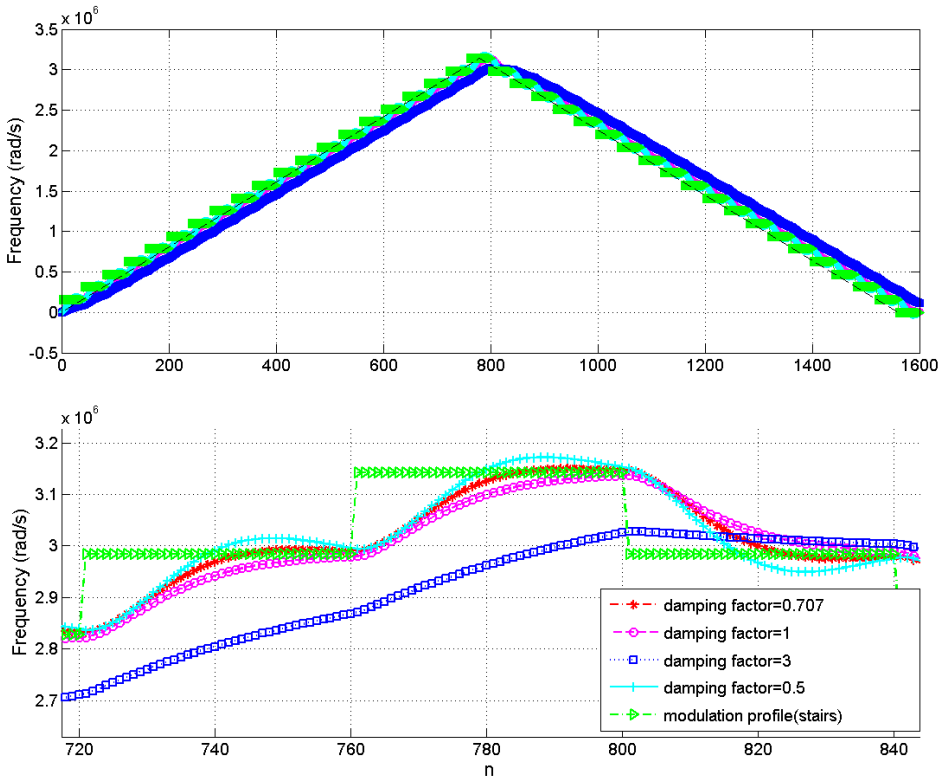
Finally, the jitter concern is critical when the spread spectrum clock is in use in the receiver for data rate of 6Gbps. This means that the jitter performance always shall be carried out, especially the cycle-to-cycle jitter.

3.4.1 Spread Spectrum behavior without Quantization Noise

The overall spread spectrum behaviors are shown in Fig.3.11 (a) and (b) with $\frac{\omega_n}{\omega_{ref}}$ equals $\frac{1}{20}$ and $\frac{1}{50}$.



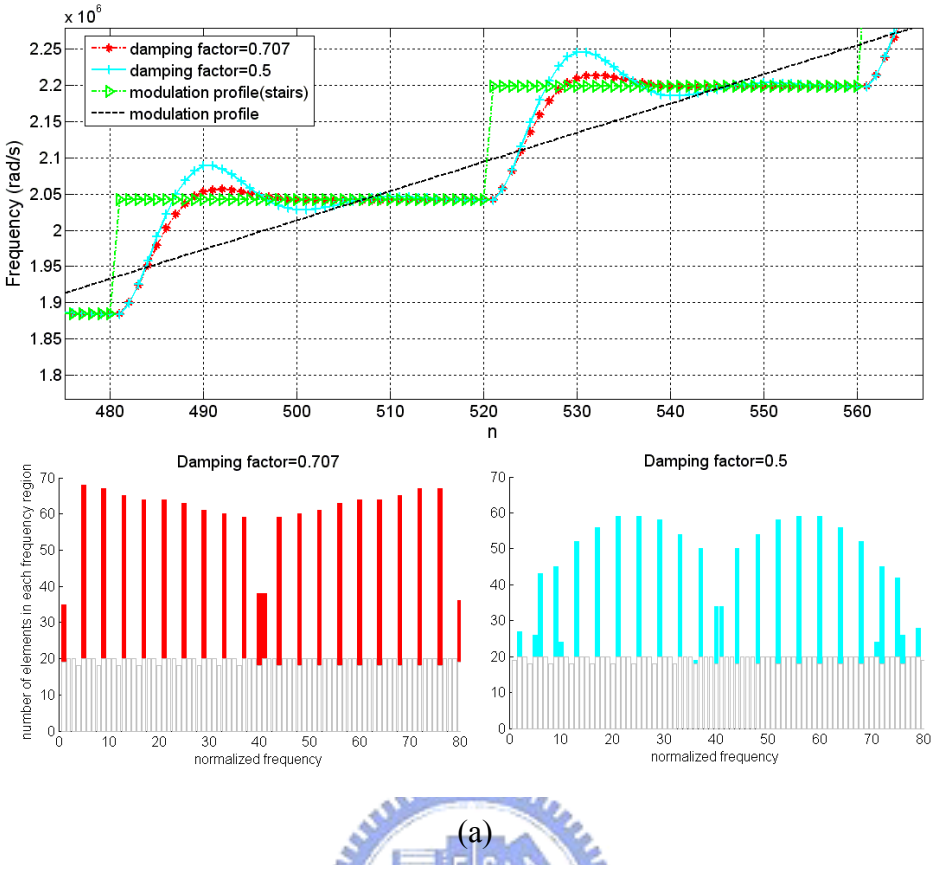
(a)



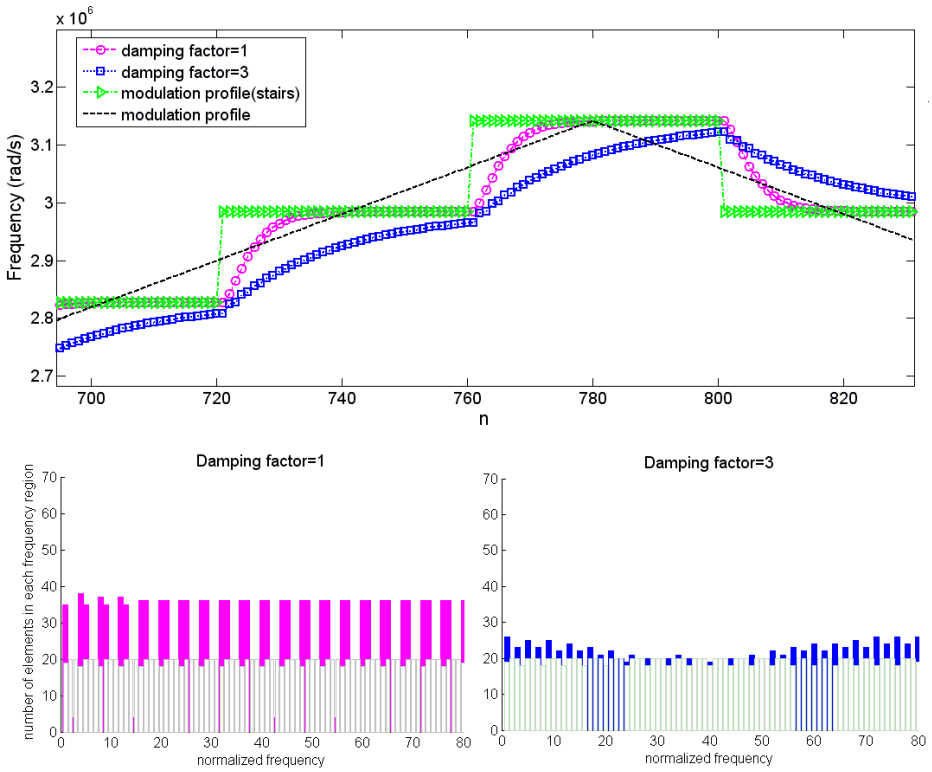
(b)

Fig.3.11 Overall spread spectrum behavior with (a) $\frac{\omega_n}{\omega_{ref}} = \frac{1}{20}$ (b) $\frac{\omega_n}{\omega_{ref}} = \frac{1}{50}$

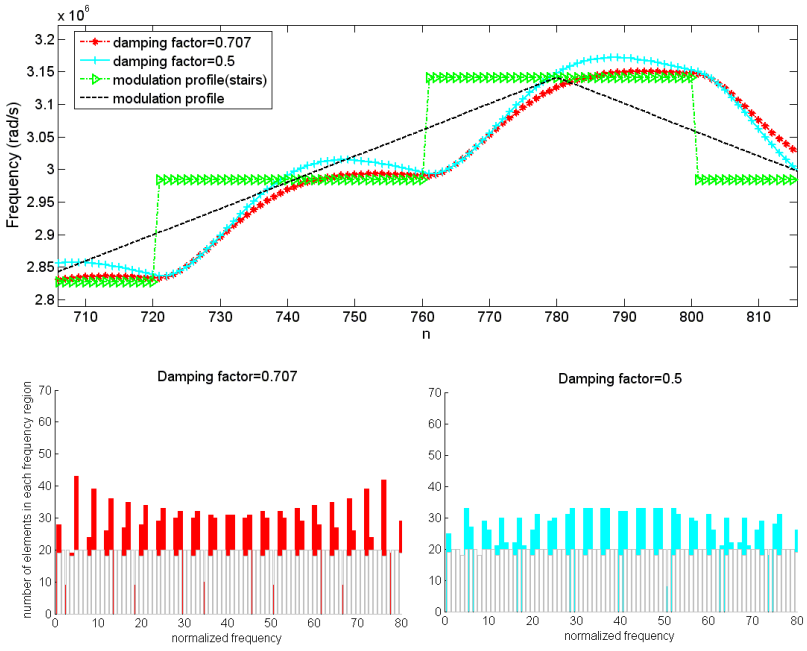
Fig.3.11 is ideal processing without digital signal processing. The quantization error is neglected to see the relationship between transient behavior and system parameters, such as ω_n and ξ. Fig.3.12 shows the histogram distribution of spread frequency deviation. Note again that the histogram does not show the absolute distribution of spread frequency deviation but a relative distribution. Each histogram shows the difference between ideal frequency distribution with perfect triangular modulation profile and spread frequency distribution with different $\frac{\omega_n}{\omega_{ref}}$ and damping factor. Consequently, we determine the PLL system parameters with more uniformly distributed one.


x 10^6
damping factor=0.707
damping factor=0.5
modulation profile(stairs)
modulation profile
Frequency (rad/s)
n
Damping factor=0.707
Damping factor=0.5
number of elements in each frequency region
normalized frequency

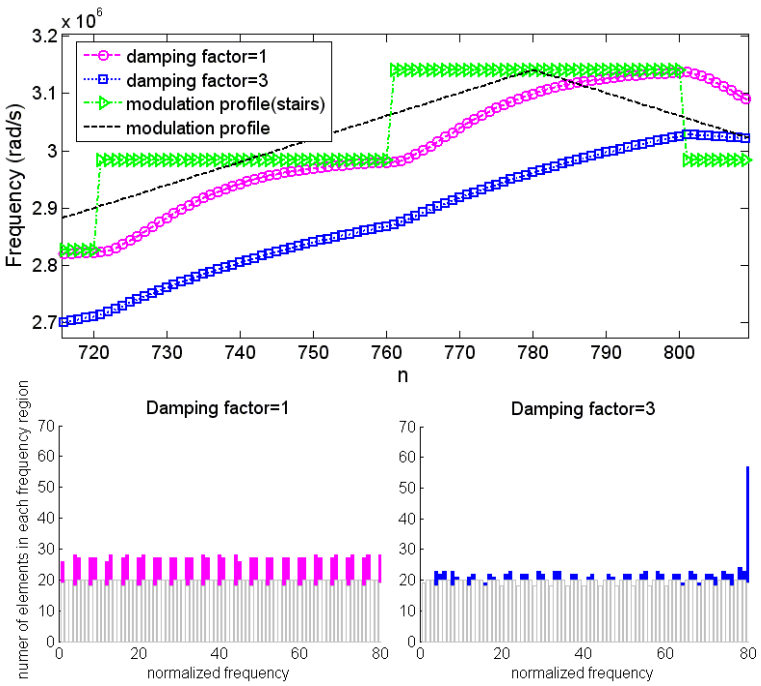
(a)


x 10^6
damping factor=1
damping factor=3
modulation profile(stairs)
modulation profile
Frequency (rad/s)
n
Damping factor=1
Damping factor=3
number of elements in each frequency region
normalized frequency

(b)



(c)



(d)

Fig.3.12 Histogram for $\frac{\omega_n}{\omega_{ref}} = \frac{1}{20}$ (a) under damping case (b) over damping case and $\frac{\omega_n}{\omega_{ref}} = \frac{1}{50}$ (c) under damping case (d) over damping case

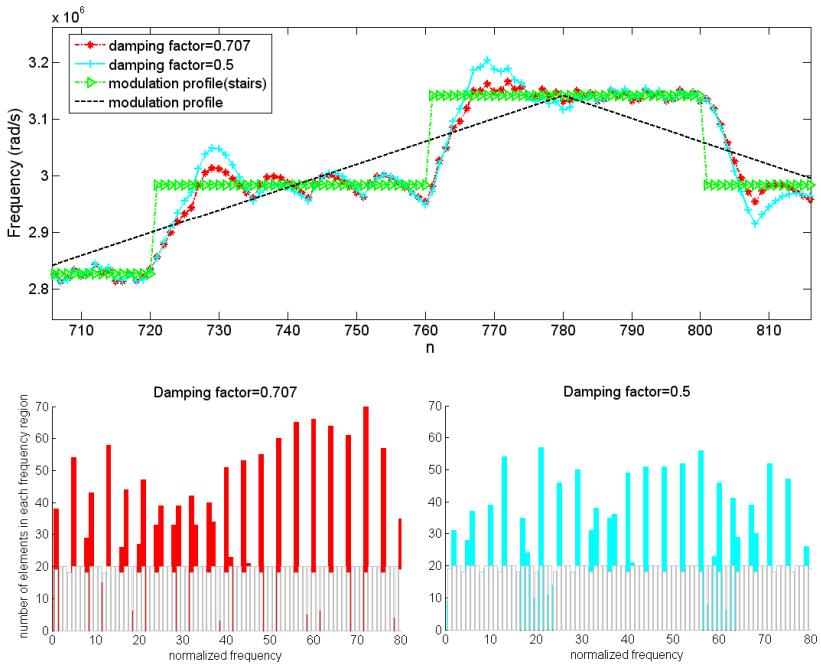
Fig.3.12 provides several insights to the design and consideration of a SSCG:

A. If the transient response of the spread spectrum behavior is more similar to an ideal triangular modulation profile, the uniform distribution is achieved.
B. The faster the transient response is, the more specific frequency terms are accumulated.
C. The slowest response shown in Fig.3.12 (d) indicates that the desired maximum frequency deviation cannot be reached.
D. More stairs will make the transient response more like an ideal triangular modulation profile in a fast response system.

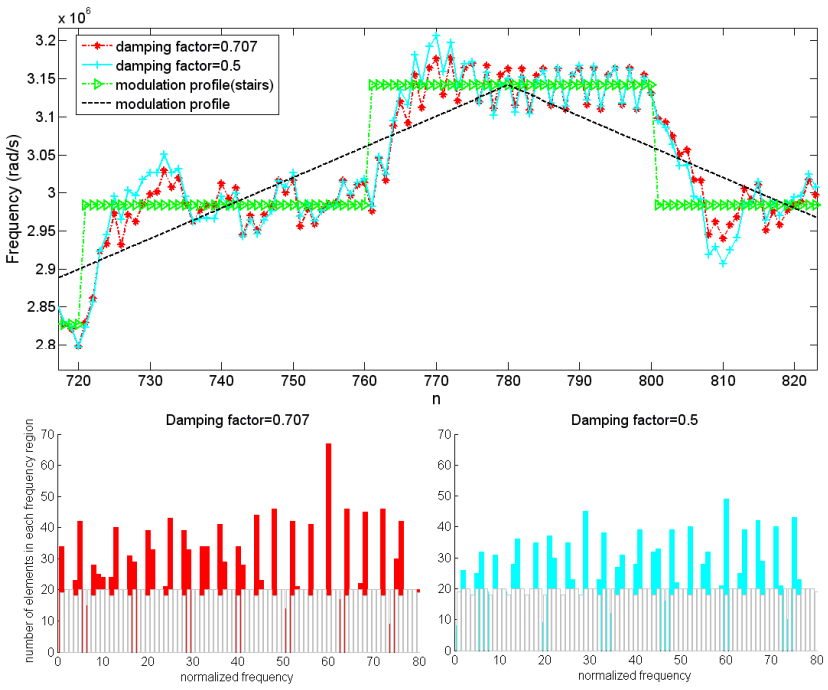
3.4.2 Sigma-Delta Modulation with Different Orders

Here we highlight the sigma-delta modulation method and the comparison between the 1st order sigma-delta modulation and 2nd order sigma delta modulation will be performed.

From Fig.3.13 to Fig.3.16 we see that the responses of different systems with different order of sigma delta modulation are illustrated. Again, the histograms display the relative distribution of spread frequency deviation and an ideal histogram is shown as reference level. There is one important thing to note is that the loop is a 2nd order system. Supposing that additional pole or zero is inserted into the loop filter, the system analysis will be different. A 3rd or 4th order system analysis and modeling should be carried out and the transient response is quite different to the second order analysis.

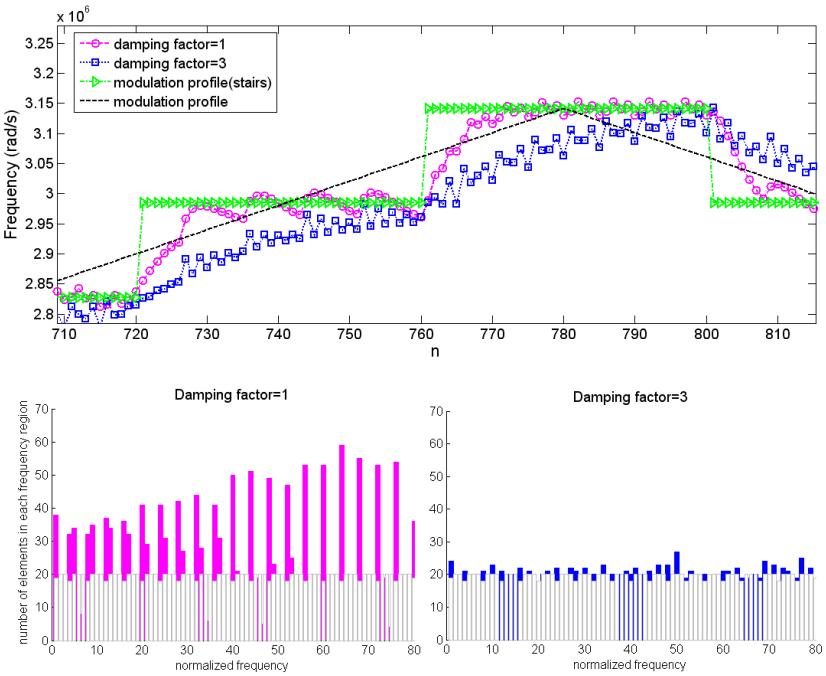


(a)

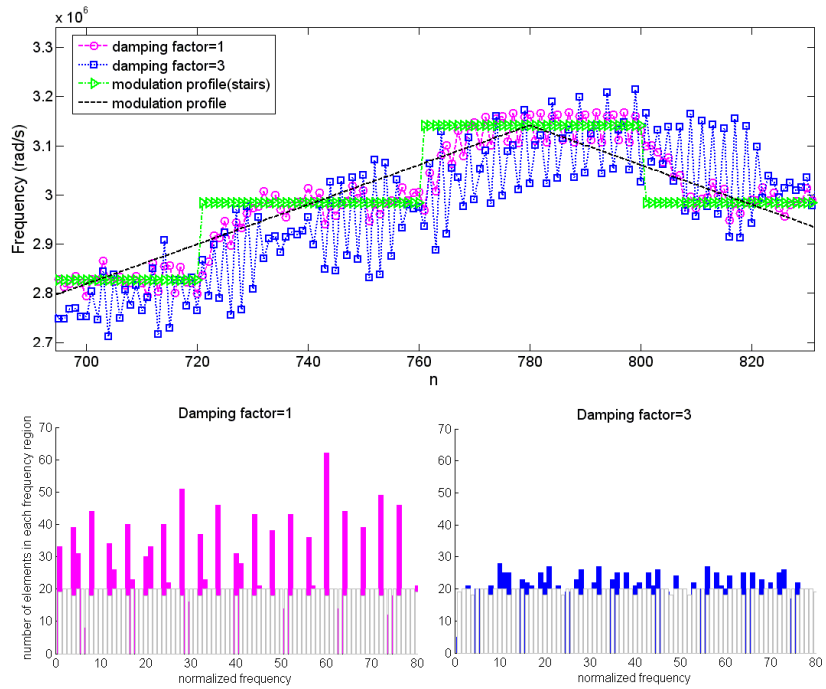


(b)

Fig.3.13 $\frac{\omega_n}{\omega_{ref}} = \frac{1}{20}$ and under damping operation with (a)1st order modulation (b) 2nd order modulation

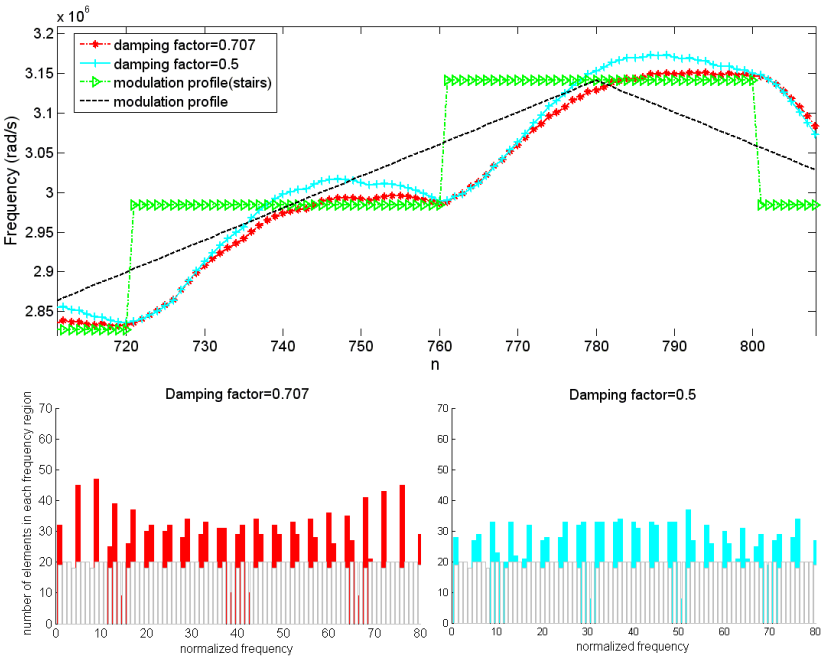


(a)

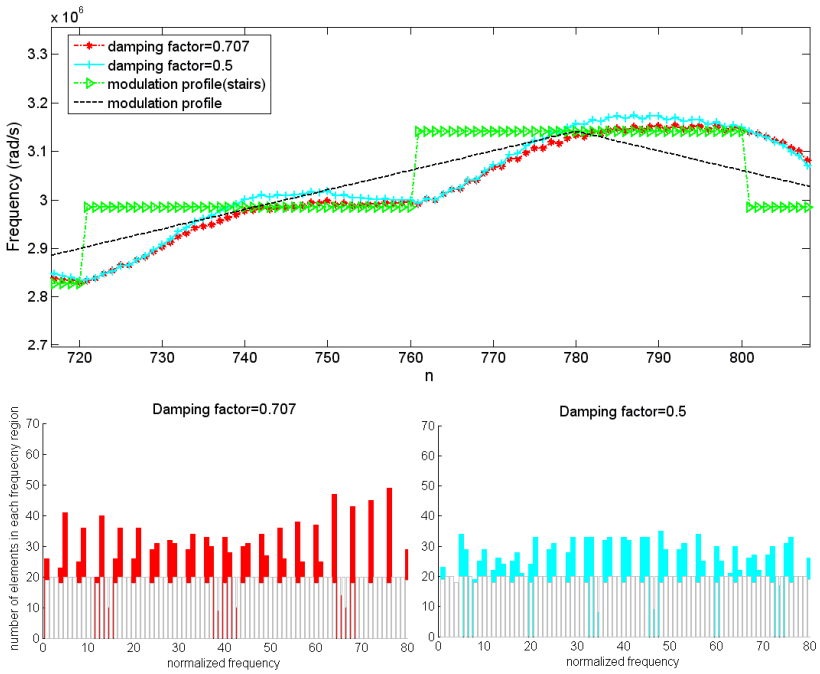


(b)

Fig.3.14 $\frac{\omega_n}{\omega_{ref}} = \frac{1}{20}$ and over damping operation with (a)1st order modulation (b) 2nd order modulation

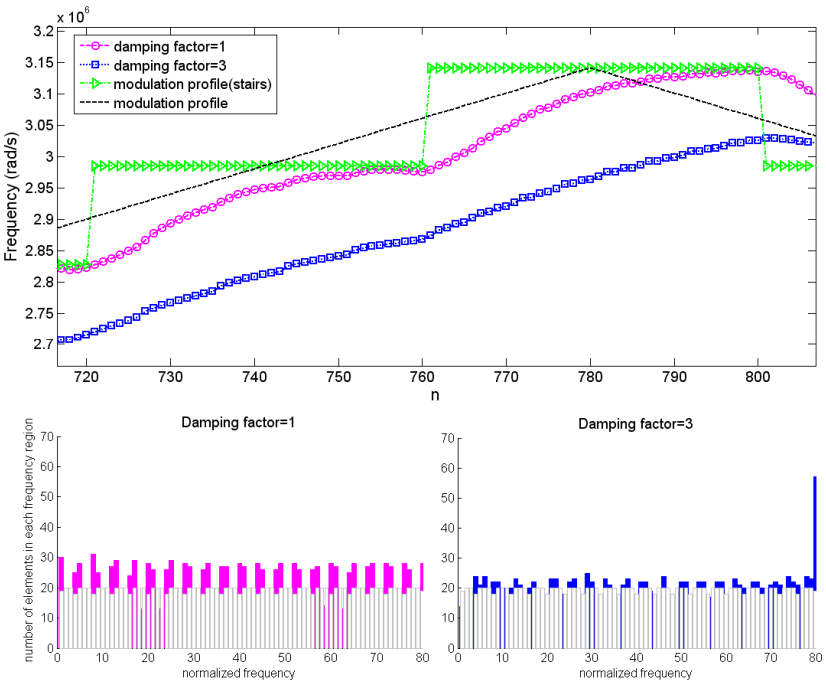


(a)

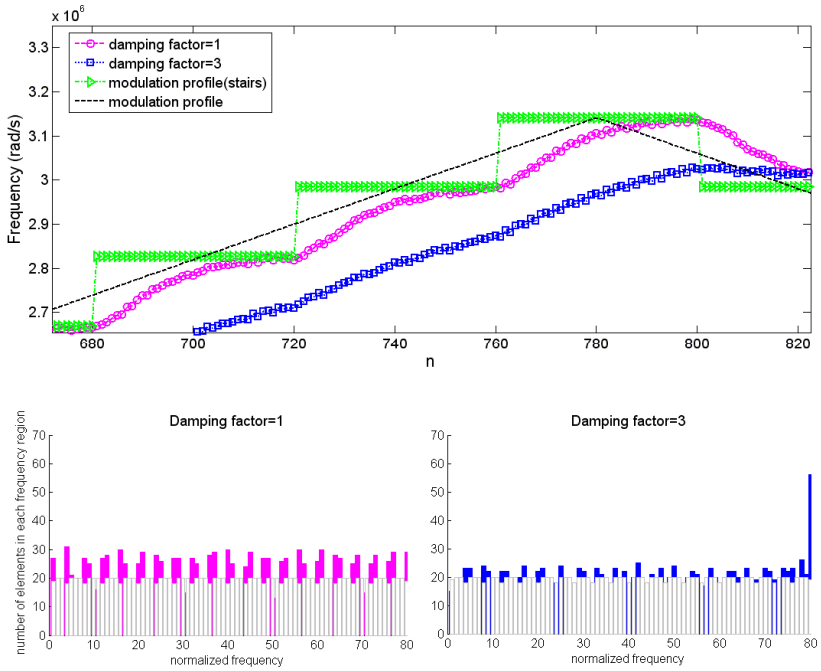


(b)

Fig.3.15 $\frac{\omega_n}{\omega_{ref}} = \frac{1}{50}$ and under damping operation with (a)1st order modulation (b) 2nd order modulation



(a)



(b)

Fig.3.16 $\frac{\omega_n}{\omega_{ref}} = \frac{1}{50}$ and over damping operation with (a)1st order modulation (b) 2nd order modulation

Some observations and design consideration are summarized below:

A. Compare with that without quantization, the quantization noise is apparent in the waveform of overall spread spectrum behavior, especially in higher open-loop integral gain and higher order sigma-delta modulation.

B. Comparing $\frac{\omega_n}{\omega_{ref}} = \frac{1}{50}$ cases with $\frac{\omega_n}{\omega_{ref}} = \frac{1}{20}$ ones, less quantization noise appears in the $\frac{\omega_n}{\omega_{ref}} = \frac{1}{50}$ cases due to the high frequency quantization noise would be filtered by the narrow system bandwidth.

C. The 2nd order modulation method would contribute more quantization noise without additional pole in the loop filter and hence the poor cycle-to-cycle jitter performance.

D. If the additional pole to filter the high frequency term, the better suggestion is to choose the first order modulation to alleviate the quantization error.

3.4.3 Timing Impacts

This section will show intuitive understanding of the low cycle-to-cycle jitter design [13]. Equation (3.22) defines the cycle-to-cycle jitter ΔT_{CC} in conventional way

$$\Delta T_{CC} = \lim_{N\to\infty} \sqrt{\frac{1}{N}\sum_{n=1}^{N}(T_{n+1} - T_n)^2} \tag{3.22}$$

The nth clock period is defined as T_n. A more general quantification of the jitter is possible by means of autocorrelation function defined as

$$C_{\Delta T}(m) = \lim_{N\to\infty} \frac{1}{N}\sum_{n=1}^{N}(T_{n+m}T_n) \tag{3.23}$$

In order to express the cycle-to-cycle jitter by (3.23), we rewrite (3.22) as

$$\Delta T_{CC}{}^2 = \lim_{N\to\infty} \frac{1}{N}\sum_{n=1}^{N}(T_{n+1} - T_n)^2$$

$$= 2C_{\Delta T}(0) - 2C_{\Delta T}(1) \tag{3.24}$$

To express the cycle-to-cycle jitter in SSC, we can model the VCO output frequency of SSCG as a sinusoidal wave first for convenience.

$$\Delta f_m(t) = K_m \cos \omega_m t \tag{3.25}$$

where K_m represents the coefficients of Fourier series composed of a frequency term with frequency of ω_m. The deviation of the period is

$$\begin{aligned} \Delta T(t) &= \frac{1}{f_o + \Delta f_m(t)} - \frac{1}{f_o} \\ &\approx \frac{K_m}{f_o^2} \cos \omega_m t \end{aligned} \tag{3.26}$$

We can obtain the continuous-time autocorrelation function shown below

$$\overline{\Delta T(t+\tau)\Delta T(t)} = \frac{K_m^2}{2 f_o^4} \cos \omega_m \tau \tag{3.27}$$

If the continuous-time autocorrelation function does not change significantly during one period, the discrete-time autocorrelation function can be approximated by continuous-time autocorrelation function. For $\Delta\tau = 0$ and $\Delta\tau = \overline{T} = 1/f_o$, we can obtain the cycle-to-cycle jitter from (3.24) to (3.27).

$$\Delta T_{CC} = \frac{K_m}{f_o^2} \sqrt{1 - \cos(\omega_m / f_o)} \tag{3.28}$$

For $f_m << f_o$ we find from (3.28)

$$\Delta T_{CC} \approx \frac{K_m \omega_m}{\sqrt{2} f_o^3} \tag{3.29}$$

Notice that from (3.28) and (3.29), the design considerations are

A. A real modulation profile can do the Fourier series expansion and the corresponding coefficients can replace coefficients into (3.28) and (3.29) to get the cycle-to-cycle jitter.

B. Once the high frequency term is included in the Fourier series expansion, the cycle-to-cycle jitter will be worse.

Chapter 4

Algorithm of the Proposed Spread Spectrum Clock Generator

4.1 Concept of SSCG Using Phase Rotation

The desired modulation profile has been shown in Fig.1.1 of chapter one. An ideal spread spectrum behavior is to modulate VCO output frequency periodically with a continuous-time triangular modulation profile. Fig.4.1 illustrates the triangular modulation profile and the corresponding specifications.

Unfortunately, analog approach to accomplish the desired modulation profile would experience the unwanted process variation and an accurate modulation profile is hard to achieve. A digital method is more popular in SSCG applications. A digital approach digitizes the triangular waveform so we can see that a straight line in triangular waveform is transformed into a stairs like waveform like Fig.4.2. We should note again that the waveform shown in Fig.4.2 represents the modulation profile without considering the transient response in the phase rotation process and the main idea of our design is based on [11].

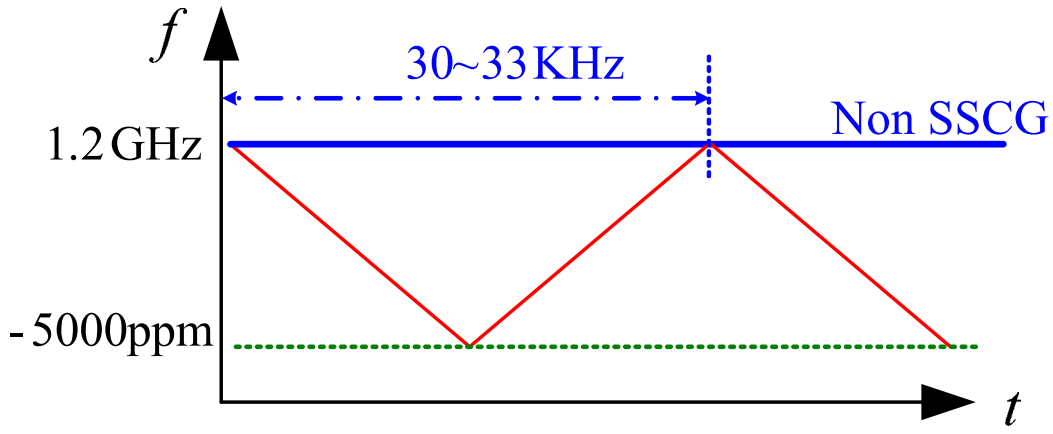


Fig.4.1 The ideal triangular modulation profile

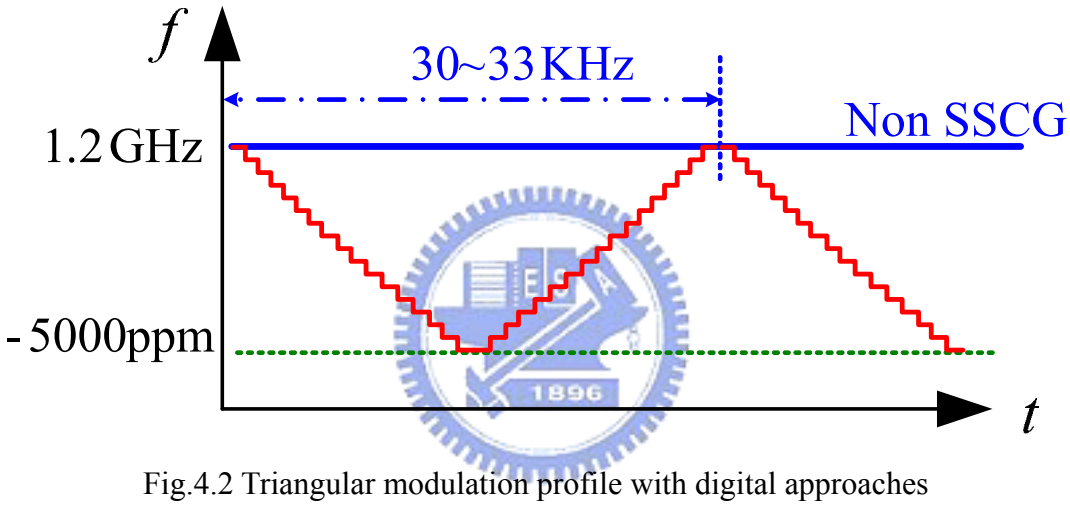


Fig.4.2 Triangular modulation profile with digital approaches

Fig.4.3 shows the block diagram of SSCG using phase rotation scheme. The key idea in digital approach is to change the rising or falling edge position of the VCO output waveform at each reference clock rising or falling edge. This timing adjustment contributes an average shift from the nominal analog value over N numbers of VCO clock cycle. Therefore, we can adjust the timing variation adequately to a desired frequency deviation of spread spectrum. We explain the overall spread spectrum behavior using uniformly distributed discrete frequency deviation, like the stairs in Fig.4.2. From now on, we introduce the timing adjustment in Fig.4.4 and derive the formula of the steady state frequency deviation to design our

circuit.

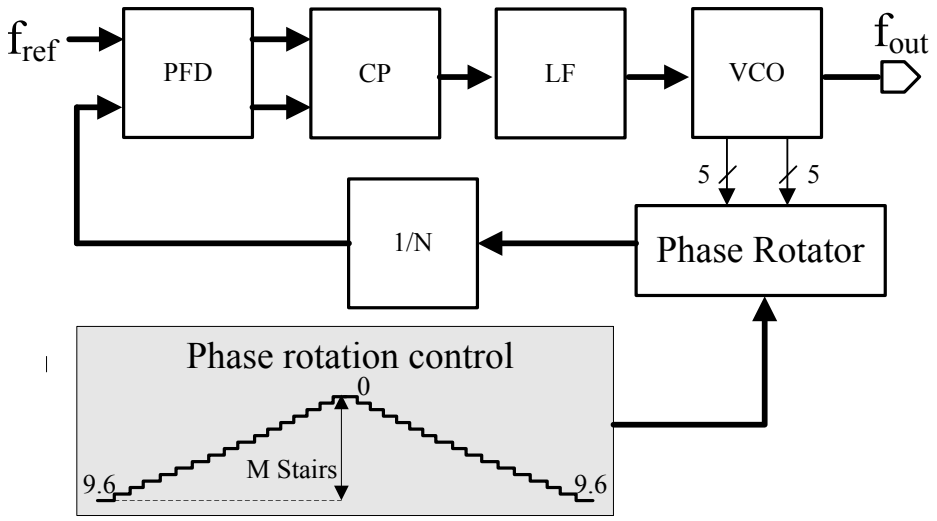


Fig.4.3 block diagram of SSCG using phase rotation scheme

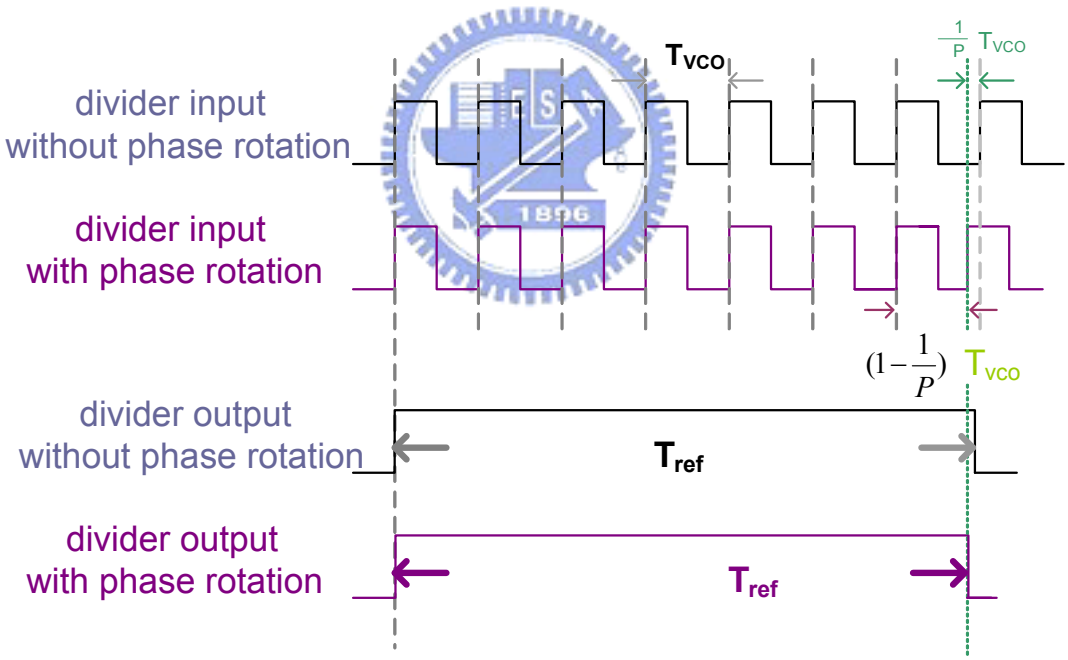


Fig.4.4 Timing diagram of the phase rotation

In Fig.4.4, T_{VCO} is the VCO oscillation period, T_{ref} is the reference clock period, T_{VCO}/p denotes the resolution of the phase rotation and p is the number of phase

provided by a phase interpolation. The VCO output waveform is adjusted by phase rotator with an amount of T_{VCO}/p at the reference clock falling edge. This timing adjustment leads to a phase error at the phase detector input. The transient phenomenon has already discussed in chapter 3 and hence we consider the steady state only. As a steady state is achieved, the phase error at the phase detector input is zero. This gives

$$NT_{VCO} - \frac{T_{VCO}}{p} = T_{ref} \tag{4.1}$$

The effective frequency deviation in steady state condition is given by

$$(N - \frac{1}{p})T_{VCO} = T_{ref} \tag{4.2}$$

$$\Rightarrow \frac{1}{(N - \frac{1}{p})T_{VCO}} = \frac{1}{T_{ref}} \tag{4.3}$$

$$f_{VCO} = f_{ispread} = f_{ref}(N - \frac{1}{p}) \tag{4.4}$$

$$= f_{nonspread}(1 - \frac{1}{N \times p}) \tag{4.5}$$

With arbitrary phase rotation, $\frac{\alpha}{p}T_{VCO}$ a general formula is given by

$$f_{ispread} = f_{nonspread}(1 - \frac{\alpha}{N \times p}) \tag{4.6}$$

An effective spread frequency is to generate the desired discrete frequency offset with $\frac{\alpha}{p}T_{VCO}$ amount of phase rotation.

4.2 Analysis of Quantization Noise

As shown in Fig.4.2, the quantization noise must be included in the ideal

frequency deviation ($f_{ispread}$) due to the digital signal processing. We introduce the steady state analysis of quantization noise in frequency domain and decide the PLL unit gain frequency f_t and orders of PLL based on the analysis. If the ideal amount of phase rotation is a fractional number (α), the practical amount of phase rotation can be presented as an ideal term ($\alpha = N^{'}$) and a quantization error term (Q_e) as shown in (4.7) and (4.8). To express the power spectrum density (PSD) of phase error, we derive the normalized frequency error first. The phase error formula in time domain is transformed into the PSD of phase error with Laplace transform as shown in (4.10) and (4.11). Eqn. (4.11) shows that as the resolution of phase rotation becomes high, a better PSD of phase error is achieved at the output of PLL.

Ideal Frequency Deviation	$f_{ispread} = f_{nonspread}(1-\frac{\alpha}{N \times p})$	(4.7)
Practical Frequency Deviation	$f_{spread} = f_{nonspread}(1-\frac{N^{'}+Q_e}{Np})$	(4.8)
Normalized Frequency Error	$\frac{Ideal-practical}{Ideal} = \frac{\frac{1}{Np}Q_e}{1-\frac{N^{'}}{Np}} = \frac{Q_e}{Np-N^{'}} \approx \frac{Q_e}{Np}$	(4.9)
Phase Error	$\theta_e(t) = 2\pi f_{ispread}\int \frac{Q_e(t)}{Np}dt = 2\pi \frac{f_{ispread}}{Np}\int Q_e(t)dt$	(4.10)
Power Spectrum Density of Phase Error	$S_{\theta e}(f) = (\frac{f_{ispread}}{fNp})^2 S_{Qe}(f) \approx (\frac{f_{ref}}{fp})^2 S_{Qe}(f)$	(4.11)

Before the steady state analysis continues, we must make some assumptions in our analysis and some design guidelines will also be shown. That is:

A. The sampling rate shall be high enough as compared to the modulation frequency so the quantization noise can be modeled as uniformly distributed function and white.

B. Higher sampling rate also pushes the spectrum of quantization noise in the higher frequency band.

C. PLL closed loop transfer function can be approximated as a open loop transfer function when frequency is high enough.

D. The high frequency poles of closed transfer function and the high frequency poles of open transfer function are almost the same.

We get the PSD of quantization noise with assumptions as shown in (4.12). The noise shaping of the quantization noise with 1st, 2nd, and 3rd order sigma delta modulator are shown in (4.13) ~ (4.15).

Power Spectrum Density of Quantization Noise	$S_{Qe}(f) = \frac{1}{12}\Delta^2 \frac{1}{f_s} = \frac{1}{12 f_s}$	(4.12)
Power Spectrum Density of Quantization Noise through 1st Sigma Delta Modulator	$S_{Qe1}(f) = \frac{1}{3 f_{ref}} \sin^2(\frac{\pi f}{f_{ref}}), f \le \frac{1}{2} f_{ref}$	(4.13)
Power Spectrum Density of Quantization Noise through 2nd Sigma Delta Modulator	$S_{Qe2}(f) = \frac{4}{3 f_{ref}} \sin^4(\frac{\pi f}{f_{ref}}), f \le \frac{1}{2} f_{ref}$	(4.14)
Power Spectrum Density of Quantization Noise through 3rd Sigma Delta Modulator	$S_{Qe3}(f) = \frac{16}{3 f_{ref}} \sin^6(\frac{\pi f}{f_{ref}}), f \le \frac{1}{2} f_{ref}$	(4.15)

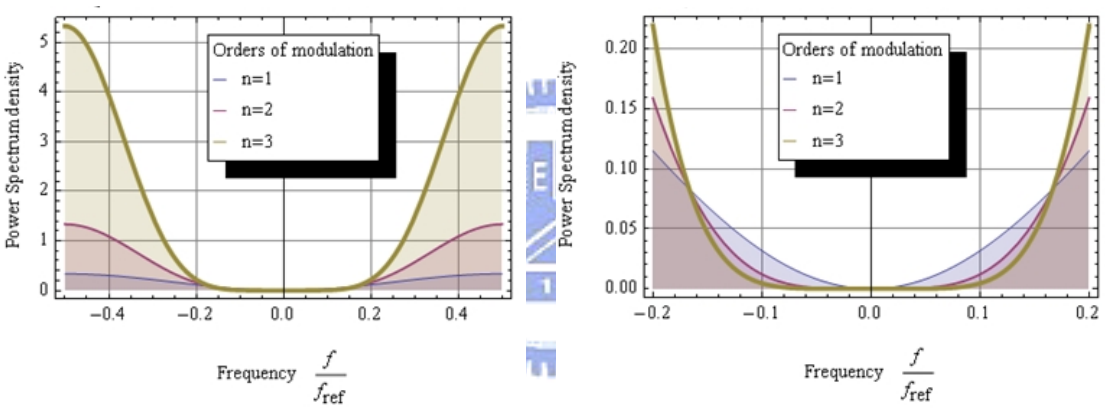
Some observations from Eqn. (4.12) ~ (4.15) can be made below:

A. The higher order modulator is, the more total noise is contributed.

B. PLL system must filter the high frequency noise when the higher order modulator is adopted to gain the benefit of lower noise in low frequency band.

C. The same noise level is achieved when $f = \frac{1}{6} f_{ref}$ among these different order modulators.

Fig.4.5 (a) shows the graphic representation of quantization noise with noise shaping applied and compares among them with different order modulator. Fig.4.5 (b) presents the enlarge diagram of Fig.4.5 (a) in the low frequency band. The quantization noise is lowered in lower frequency band and enlarged in higher frequency band with the higher order modulator. Thus, the PLL system must filter the high frequency quantization noise to get the advantage of noise shaping if the higher order modulator is adopted.



(a) (b)

Fig.4.5 PSD of Quantization Noise with different modulation order (a) Normal graph (b) Enlarge diagram of (a) in lower frequency band

The shaped quantization noise is then filtered by the PLL system and the corresponding filtered quantization noise at PLL output is shown in Fig.4.6. The unit gain frequency of PLL is set to $\frac{1}{20} f_{ref}$ and $\frac{1}{50} f_{ref}$ in the left side and right side of Fig.4.6, respectively. The quantization noise is passed through the 2nd, 3rd and 4th order PLL, as shown in Fig.4.6 (a_1,b_1), (a_2,b_2), (a_3,b_3), respectively.

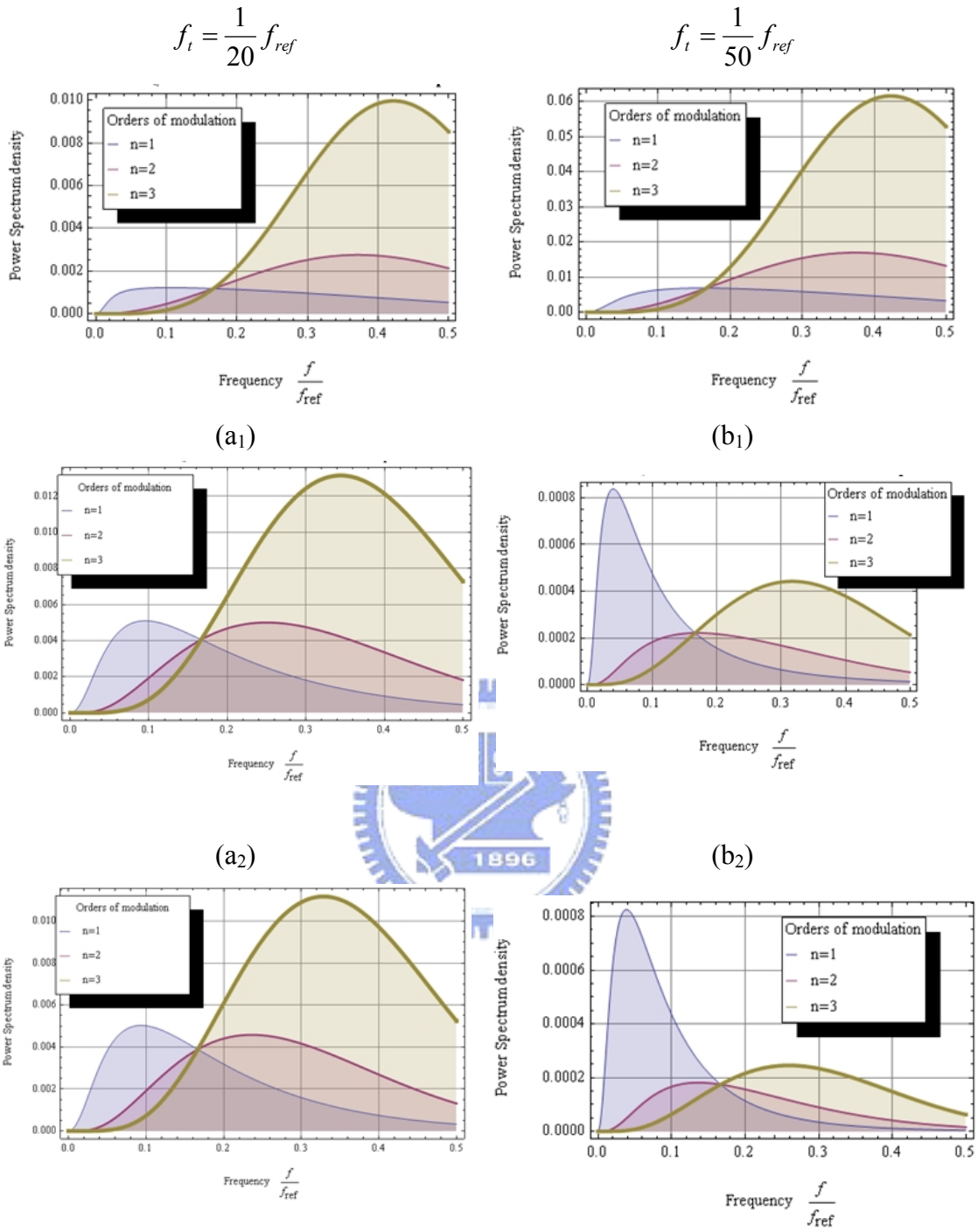
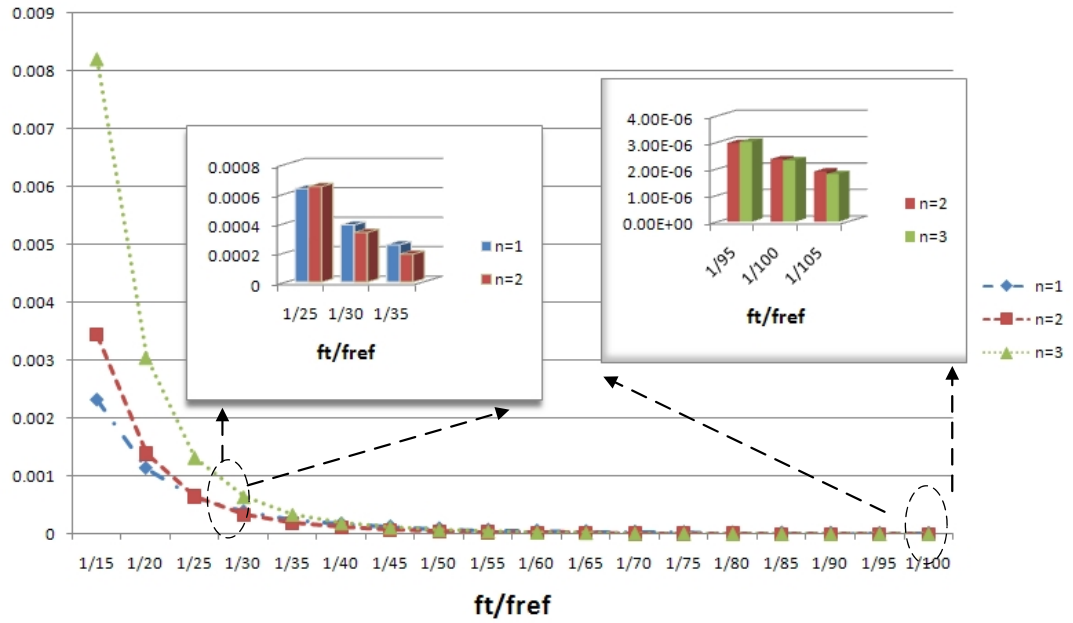
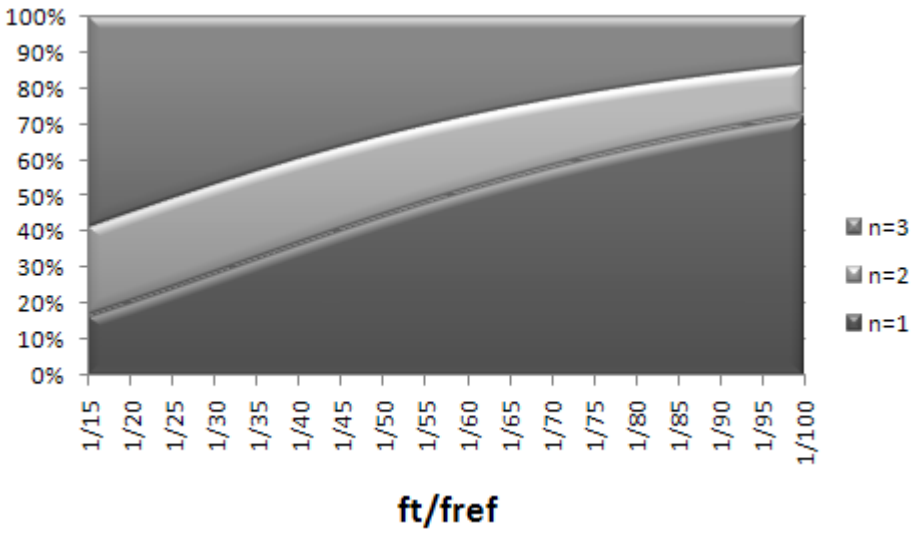


Fig.4.6 PSD of Quantization Noise at different orders PLL output with separate unit gain frequency $(a_{1\sim3})$ $f_t = \frac{1}{20} f_{ref}$ $(b_{1\sim3})$ $f_t = \frac{1}{50} f_{ref}$; (a_1,b_1) 2nd order PLL (a_2,b_2) 3rd order PLL (a_3,b_3) 4th order PLL

The orders of PLL must be higher than the orders of modulator to guarantee that the high frequency noise can be filtered out. The smaller unit gain frequency f_t of PLL is, the more high frequency noise is filtered. For the higher order modulator applications, the quantization noise in high frequency band should be low enough comparable to the one in the low frequency band to take the advantage of the higher order modulator. To do this, we integrate the PSD of filtered quantization noise to get the total noise at the PLL output with unit gain frequency of PLL as x-parameter as shown in Fig.4.7 (a). The different orders of modulator are also presented in the figure to find out the crossing point of the total power level between different orders of modulator. As shown in Fig.4.7 (a), the 2nd order modulator will be better than first order one when the unit gain frequency of PLL is about 1/30. The 3rd order one is better than 2nd order one when the unit gain frequency of PLL is about 1/100. Fig.4.7 (b) shows the relative total power level among the different order modulators as the unit gain frequency of PLL is decreasing gradually. The same feature can be observed as Fig.4.7 (a).



(a)



(b)

Fig.4.7 Total quantization noise at 4th order PLL output with different orders of modulator as the normalized unit gain frequency as x axis (a) total power vs. ft/fref (b) Relative total noise power level among different order modulators

Again, we must address that the analysis above is for the steady state analysis. If the PLL system cannot response the spread spectrum behavior quickly, the transient response would dominate the performance of SSCG. Another issue should be noted is that a low jitter PLL is achieved with higher unit gain frequency of PLL because the ring oscillator is adopted as our design. This would conflict with the quantization noise analysis. Hence, a 1st order modulator is adopted in our design.

4.3 Phase Rotation Mechanism

First, we discover that the more stairs in the modulation profile (Fig.4.2) would produce less high frequency term in modulation profile. Secondly, for a linear time invariant system, a large phase rotation also contributes large phase error at the output of the system. Consequently, high resolution of phase rotation is required and this means a large p is required. In this design, we adopt five stages VCO so a coherent

multi-phase PLL has ten uniformly distributed phases. The interpolation resolution is 1/16 in our design so the resolution of the phase rotation is $\frac{1}{160}T_{VCO}$. From (4.6) and specification described in chapter one, the desired maximum spread frequency deviation is $f_{nonspread}(1-5000\,ppm)$. The maximum amount of the phase rotation is $9.6\times\frac{1}{160}T_{VCO}$ to give a $5000\,ppm$ down-spread frequency deviation. To produce the periodic modulation profile requires the control signal to move from 0 to 9.6 and then returns to 0 in a circle as shown in Fig.4.3.

Another design consideration is the number of the stairs in modulation profile shown in Fig.4.3, denoted by M. It depends on the consideration of the hardware implementation and PLL system parameters described in the Chapter 3. The hardware design consideration would be covered in the next section. If the number of stairs is less, the system response converges more quickly to a steady state. The frequency distribution of the SSCG output would concentrate on certain frequency so the reduction of EMI will be worse. The other drawback is that lager input step in such fewer stairs contributes a bigger amplitude response. This would account for more high frequency term in the modulation profile and the cycle-to-cycle jitter performance would be bad. On the other hand, a more than enough number of stairs in the modulation profile does not increase the resolution any more due to the deterministic phase rotation resolution. A more severe problem is that the PLL system does not have enough time to response to a new phase rotation because of more stairs. The required maximum frequency deviation might not be achieved.

Before we focus on the glitch problem induced by the phase rotation progress, we introduce the block diagram of phase rotation and phase rotation control unit first.

Fig.4.8 shows the block diagram of phase rotator that consists of two multiplexer, an interpolator, a phase-rotation counter and a decoder which chooses exactly the adjacent two phases and converts the interpolation ratio signal to a thermal code.

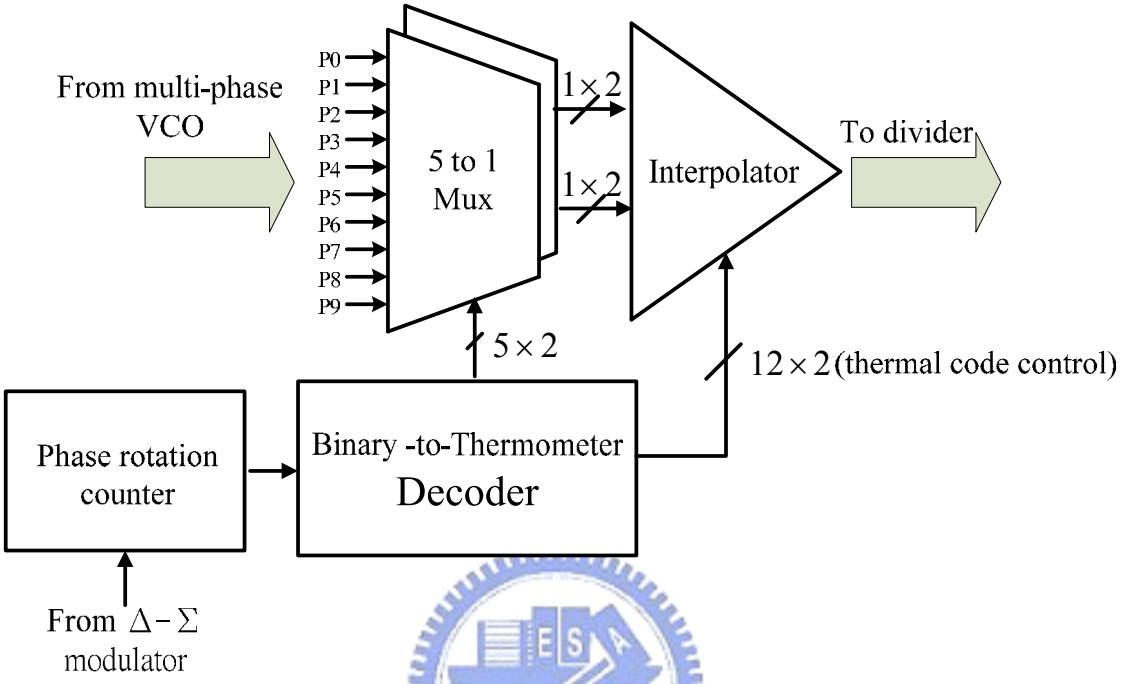


Fig.4.8 Block diagram of phase rotation unit and phase rotation control

We use the interpolation technique to avoid the glitch problem in [11]. The glitches are caused by the unequal delay in switching control signal of the phase rotation block. The phase interpolation technique is applied to avoid the glitch from the transition of control signal because the interpolation ratio is very low at the transitionary phase. For example, Fig.4 illustrates the detail opration of the mechanism of phase rotation. The dot line shown in Fig.4.9 is the progress of phase rotation. The interpolation ratio between p4 and p5 is 30%-70% at *a*, 90%-10% at *b* respectively. The phase rotation is in progress and begins at a. After rotating to *b* location, the multiplexer changes the selected phase, from (P4, P5) to (P3, P4) and the new interpolation ratio is 10%-90% at *c*. From the discussion above, we can conclude that

the transition of the selected adjacent phase will not generate glitch when the selected phase is changed because the transitionary phase have low interpolation ratio at the transition time. Hence, a no glitch method is introduced in our proposed techniques.

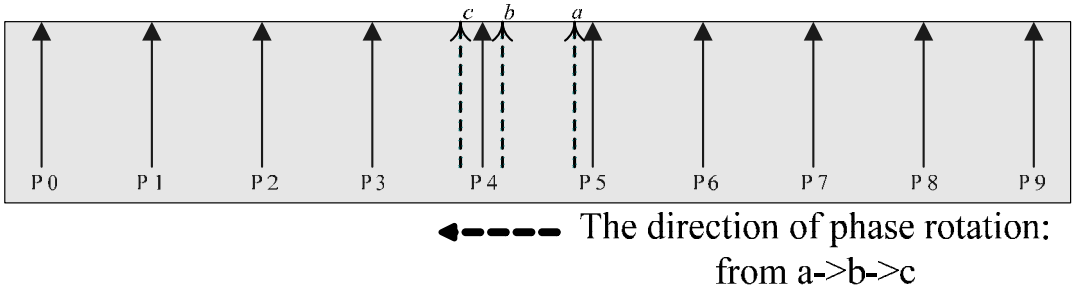


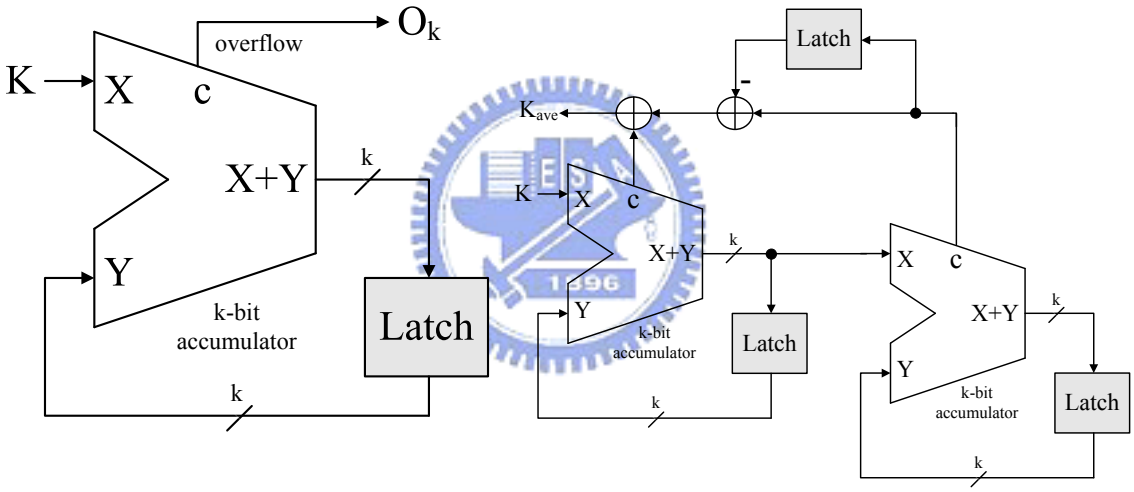
Fig.4.9 The phase rotation in progress

A thermal code is designed to control the interpolator in order to ensure the monotonic behavior in the process of phase rotation. The monotonic behavior guarantees the accumulated phase is monotonically increased or decreased during the spread spectrum process. It means that the frequency adjustment of spread spectrum output would increase or decrease toward the end of modulation profile without any spike in it. If the monotonic characteristic cannot be guaranteed, there are spikes in the modulation profile. In this case, the high frequency terms in modulation profile are amplified so that the cycle-to-cycle jitter becomes worse. The amount of EMI reduction relies on the distribution of the frequency deviation. A spike in the modulation profile will destroy a uniform distribution. The EMI reduction will be small due to the unbalanced distribution of the frequency deviation.

4.4 ΣΔ Modulator

As described in section 4.2, values from 0 to 9.6 are required in the phase rotation of the spread spectrum operation. A sigma-delta modulation technique is

adopted in such applications to carry out the fractional number, such as from 0 to 9.6. An average concept presents the desired value again on the basis of digital signal processing. A sigma delta module is accomplished with a digital accumulator as shown in Fig.4.10. The first order and second order digital implementation are illustrated below. The number K is an integer number to set the desired fractional value K_{ave} which equals to $\frac{K}{2^k}$ and is in long term average of the overflow O_k. The second order modulator is used to shape the quantization noise. The first accumulator with input K calculates the average fractional number while the second one performs the phase error spectral shaping.



(a) (b)

Fig.4.10 Equivalent digital implementation of a sigma delta modulator with (a) first order and (b) second order module

The modulation mechanism based on modulation on VCO [8], modulation on input [9], and modulation on divider [10] reveals that DC gain is larger than one and hence the quantization noise is amplified. A higher order sigma delta modulation is accomplished to shape the amplified quantization noise in these modulation

mechanisms. The technique [11] presents that the noise transfer function developed in Chapter 3 is equivalent to unity at DC so extra orders of modulation to shape the quantization noise are not necessary. The higher order modulator in our design would contribute more spikes in the modulation profile because a large input step make the system response with large output step. These high frequency spikes will enlarge the cycle-to-cycle jitter. Accordingly, we adopt the first order sigma delta modulation implementation for our proposed SSCG.

The accumulator should be implemented in a digital approach and we must decide the size of the accumulator. The size of the accumulator gives another design parameter mentioned in section 4.2. It is the number of the stairs in the modulation profile. For our example, a 4-bit accumulator is used so that the desired K in the sigma delta module equals to $2^4 \times 9.6 = 153.6$ and should be truncated to 153 to promise the maximum frequency deviation not larger than 5000ppm. Therefore, the desired amount of phase rotation, from 0 to 9.6 is accomplished by the accumulator with integer value from 1 to 153 as the input of accumulator.

If the size of accumulator is too large or too small, the EMI reduction and cycle-to-cycle jitter performance become worse. Because a larger size of accumulator means more number of stairs in the modulation profile and vice versa. The impact of number of stairs in the modulation profile impacting on the behavior of SSCG has been discussed in section 4.2.

Chapter 5
Circuit design of Spread Spectrum Clock Generator

5.1 Introduction

A proposed spread-spectrum clock generator for Serial ATA with phase rotation is presented. To achieve low jitter issue in our design, PLL uses error amplifier to resolve the current mismatch in charge pump and a third order loop filter is adopted to reduce the reference spur. A passive resistor is presented in the VCO delay cell to reduce the K_{vco} gain and an additional cross-couple CMOS is also included to the delay cell to boost the operation of delay cell. Our spread spectrum clock generator (SSCG) for Serial ATA Specification is down spread 5000ppm with a triangular modulation profile and the modulation frequency is 30 kHz. A spread spectrum technique using PLL with a sigma delta modulator and phase rotation algorithm is proposed. This proposed architecture has been designed in a 90-nm CMOS process. The non-spread clocking has a peak-to-peak jitter of 3.88ps and consumes 5.87mW at 1.4GHz. The EMI reduction in this circuit is about 18.22dB.

5.2 System architecture

The building block of the proposed SSCG architecture is shown in Fig.5.1. In our design, a SSCG, controlled by sigma delta modulator and phase rotator with interpolator can enhance the performance of SSCG. The proposed phase rotation mechanism can avoid output glitch of SSCG when the phase select is changed.

The modulation profile unit generates a periodic triangular waveform to feed into the sigma delta modulator. Sigma delta modulator converts the input signal to the desired fractional number which transmits through the phase rotator block to control the amount of phase rotation. Through a proper choice of the amount of the phase rotation by digital control scheme allows exact amount of frequency deviation.

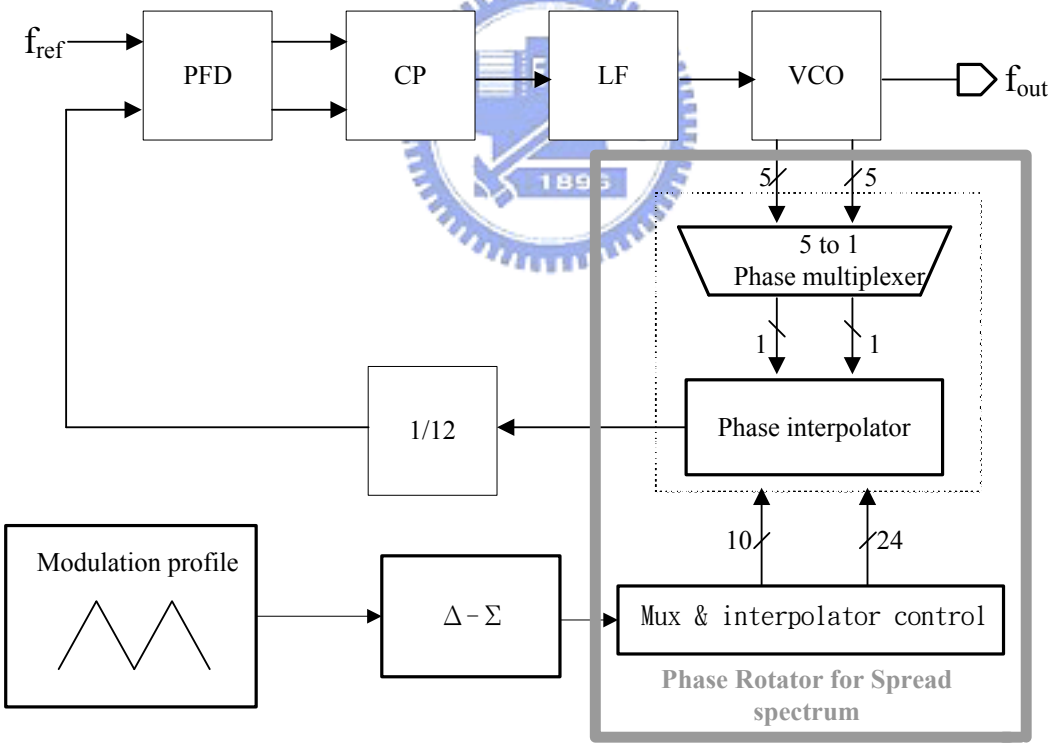


Fig.5.1 The architecture of SSCG with phase rotation technique

In order to confirm the SATA specifications, an 4-bits accumulator is adopted and the accumulator input, K runs periodically through 0, 1, 2,…, 152, 153, 152, 151,…, 0. The maximum frequency deviation is 4980ppm with 30 us modulation period.

5.3 Behavior Simulation

The forth order PLL design consideration is covered in Chapter 2 and (2.12) describes the stability of the PLL system. Eqn. (2.12) also shows adequate phase margin and the value of corresponding system components. First, we design our PLL circuit with third order closed form so that we can determine the circuit parameters. Thus, we put additional third high frequency pole into the loop filter. The location of the third pole should be high enough comparable to the second pole in the loop filter to guarantee the accuracy of the third order PLL analysis. To our experience, it shall at least four times larger than the second pole in the loop filter.

To start with the 60 degree of phase margin, we also set the open loop unit gain frequency equal to one fiftieth input reference frequency ($\omega_t = \frac{1}{50}\omega_{ref}$). In order to ease the effect of leakage current, we choose the charge pump current to be 50 uA. The sensitivity of VCO output frequency to its input control voltage is defined as K_{VCO} which is obtained from the simulation. Also note that the additional third pole in the loop filter is used to suppress the reference spur due to the periodic operation of PFD and phase rotation mechanism. This is designed based on (2.17) and should be put into higher frequency band mentioned above.

According to the discussion above, we get the design parameters as shown in Table.5.1.

Table.5.1 Corresponding system components

K_{VCO}	700MHz/V
I_p	50 uA
C_1	70pf
C_2	4.6pf
R_1	4.5kΩ
N(divider ratio)	12
R_2	1.8 kΩ
C_3	1.8pf

The open loop unit gain frequency is 100MHz divided by 50. Hence, $\omega_t = 2MHz$. Besides, a 60 degree of phase margin requires the frequency of the second pole ω_{p2} in the loop filter is four times of ω_t and we have $\omega_{p2} = 8MHz$. The third pole should be at least 32MHz to promise the stability of this feedback system. We rewrite (2.17) as shown below

$$Attenuation = 20\log[(\omega_{ref} R2C3)^2 + 1] \qquad (5.\ 1)$$

From the formula and discussion above, we substitute $\frac{1}{2\pi R2C3} = 32MHz$ into (5. 1) to get the maximum attenuation 20.6dB in this assumption. We design the additional pole conservatively and then choose $R_2 = 1.8k\Omega$ and $C_3 = 1.8pf$ to get the corresponding attenuation 14dB. We would verify the discussion in Matlab simulation to support our analysis. The Matlab verification is shown in Fig.5.2. It indicates that the frequency response of the forth order PLL almost overlaps the third order one for frequency below the open loop unit gain frequency. The extra pole

works as the frequency exceeds the third pole frequency and the attenuation is about 10dB which conforms (5. 1).

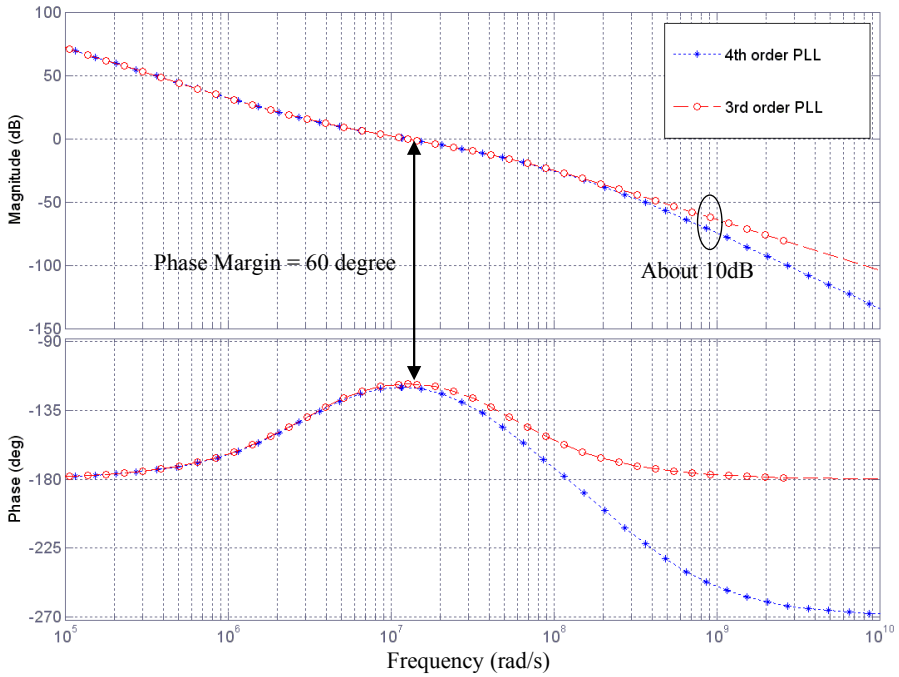


Fig.5.2 Frequency response of 3rd order and 4th order PLL

5.4 Circuit Implementation

In the following, the circuit implementation will be presented, including the major blocks of PLL, and a phase rotation control that enabling the spread spectrum. The PLL is consist of phase frequency detector (PFD), charge pump (CP), loop filter (LF), voltage-controlled oscillator (VCO), and divider. The circuit implementation and characteristics are illustrated. The simulation results with HSPICE (analog) NERO-SIM (mixed signal) simulation will be shown in the end.

5.4.1 Phase / Frequency Detector

The sequential phase frequency detector (PFD) is illustrated in Fig.5.3 [14]. One of the characteristics of this PFD is the small intrinsic parasitic so that the speed limitation would be overcome. Another attribute is the dead zone reduction. Fig.5.3 (b) shows the timing diagram of PFD. In the case of in-phase, the UP and DOWN create the same width of pulse which is designed for matching the turn-on time of charge pump. The PFD creates the lead and lag information with the width of UP and DOWN pulse, respectively. Fig.5.3 (c) presents the single to differential circuit to produce the differential signal for using in the charge pump.

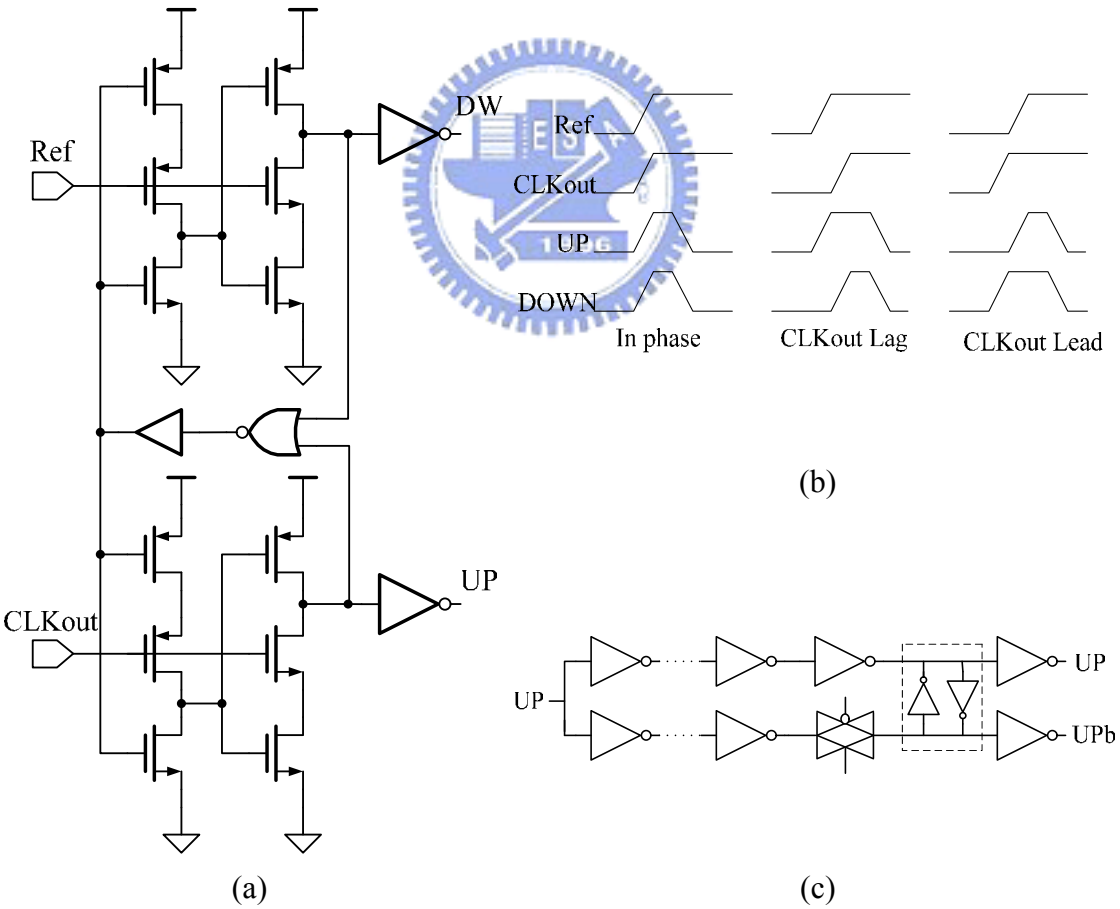


Fig.5.3 Phase frequency detector (a) schematic (b) timing diagram (c) Single to Differential circuit

5.4.2 Current Matching Charge Pump

The charge pump circuit with error amplifier applied to resolve current mismatch is presented in [15]. Fig.5.4 illustrates this design of charge pump circuit. The conventional CMOS charge pump circuits have some current mismatch due to the channel length modulation effect, especially in deep sub-micron process. Both current mismatch and leakage current generate phase offset in PLL and the corresponding spur is produced. Hence, an additional jitter is displayed at the PLL output clocking. When the current mismatch or leakage current occur, the amount of the average phase offsets is given by [7]

$$\theta_b = 2\pi \frac{I_b}{I_{cp}} \qquad (5.2)$$

where θ_b is the average phase offset, I_b is the average leakage current or the average mismatch current per cycle, and I_{cp} is the charge pump current in design. Eqn. (5. 2) can be further formulated as [15]

$$\theta_b = 2\pi \frac{I_b}{I_{cp}} = 2\pi \frac{\Delta_i}{I_{cp}} \frac{\Delta_{ton}}{T_{ref}} \qquad (5.3)$$

where Δ_i is the amount of current mismatch, Δ_{ton} is the turn-on time of CP switch and T_{ref} is the input reference frequency. Notice that we should reduce the phase offset θ_b by aggrandizing the charge pump current, decreasing the ratio of turn-on time of switch to the input reference clock cycle and diminishing the mismatch amount of charge pump current.

In Fig.5.4, $M_{7\sim10}$ is the replica of the charge-pump path made of $M_{1\sim4}$. An operational amplifier OP_2 is added to let the ref voltage follow the C_{pout} voltage by a negative feedback loop. Charge current and discharge current can be matched by the

feedback loop due to the same drain voltage in the charge and discharge current source. As long as gain of OP_2 is high, voltage at ref and C_{pout} are almost the same and in the locking state, they are almost constant. Thus, I_2 is also equals to I_3 and the feedback loop equalize the ref and C_{pout} voltage so that the bias condition of M7~10 is the perfect replica of $M_{1\sim4}$. As a result, $I_{cp2}=I_3$ and $I_{cp1}=I_2$, and this will force $I_{cp1}=I_{cp2}$. A current matching is achieved. The proposed charge pump changes the location of the switch, $M_{2\sim3}$ with the location of current source, M_1 and M_4, to reduce the turn-on time [15] of the current source. In this way, we can avoid the additional jitter induced by the long turn-on time of the current source. Fig.5.5 shows the current variations against output voltage (cpout) variations of the charge pump circuit.

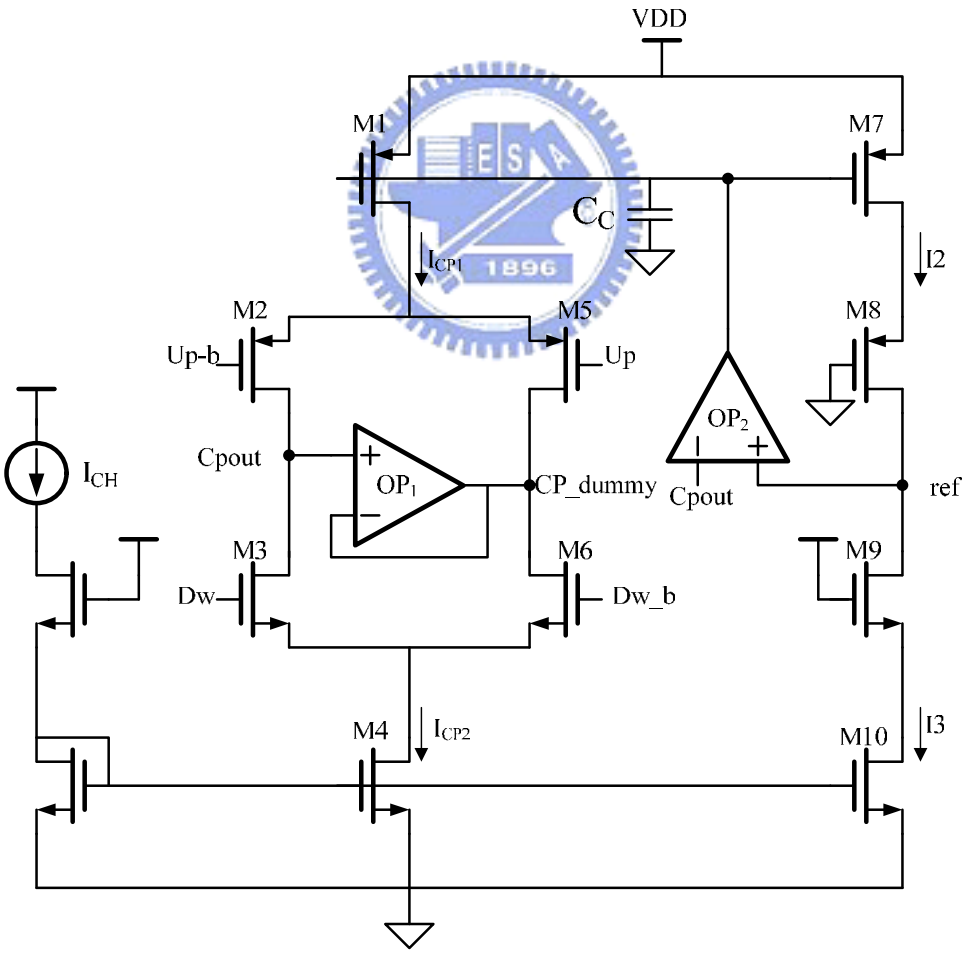
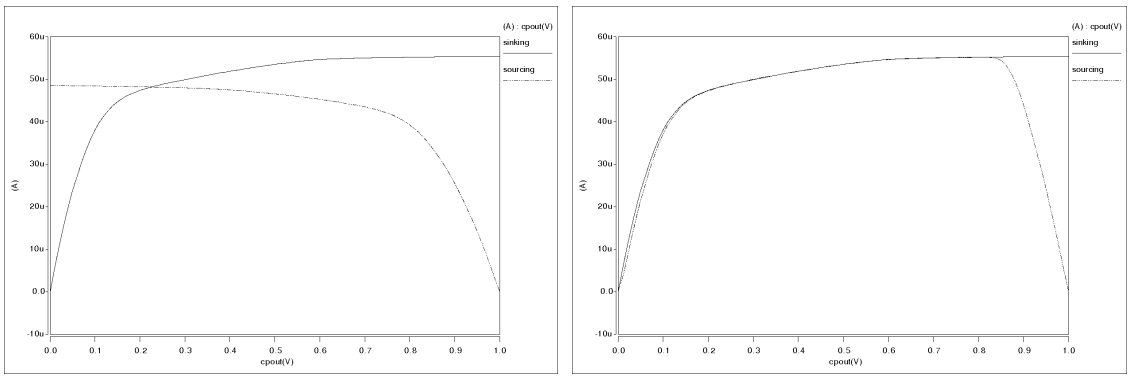


Fig.5.4 Charge pump circuit



(a) (b)

Fig.5.5 Charge Pump current matching characteristic (a)Conventional charge pump (b) proposed charge pump.

5.4.3 3th Order Loop Filter

In order to suppress the additional spur due to the phase rotation mechanism, the usage of the third order loop filter is adopted and shown in Fig.5.6. We implement the resistor with a standard cell P+ Poly resistor without salicide (RNPPO) provided by UMC and choose Mixed Mode MIM capacitor (MM MIMCAPs) as our capacitor design.

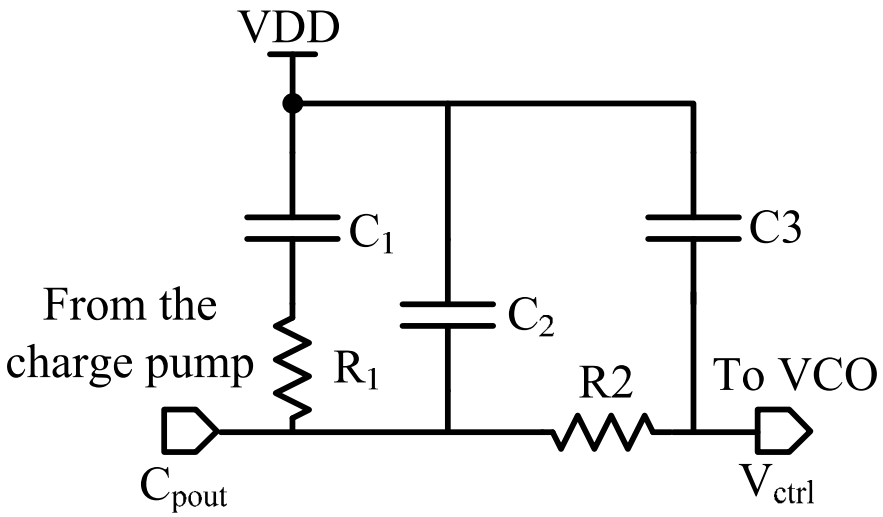


Fig.5.6 Third order loop filter

5.4.4 Voltage-Controlled Oscillator

Our VCO is based on the design published in [16]. The self-biased technique is adopted to track the supply and substrate induced noise. The operational amplifier used in bias replica is also self-biased and tracks the VCO oscillating frequency so that the suppression of the supply and substrate induced jitter remains nearly constant during the full tuning range of PLL.

As shown in Fig.5.7, the delay cell presneted in this design resembles the one in [16]. We make a little modifications about inserting a passive resistor in parallel with the symmetric load composited of $M_{1\sim2}$ and $M_{7\sim8}$. Another modification is that the CMOS cross-coupled pair is adopted, which is denoted as M_3, M_6, M_5, and M_9. The primary function of the inserted passive resistor is to lower the K_{VCO} and to promote the linearity of the symmetric load for low jitter design concern. The lower K_{VCO} would mitigate the sensitivity of VCO due to the noise contributions in the loop filter. The linearity of the loading in the delay cell can alleviate the supply and substrate induced noise and the harmonic terms perturbations. The additional cross-coupled pair boosts the transition of the delay cell output waveform. Hence, it helps to keep the high level or low level of the swing of waveform to the saturation level when the oscillating frequency is minimum or maximum of the allowed VCO frequency. Fig.5.8 shows the operating frequency with different VCO input control voltages. The resulting sensitivity of VCO is about 670MHz/V.

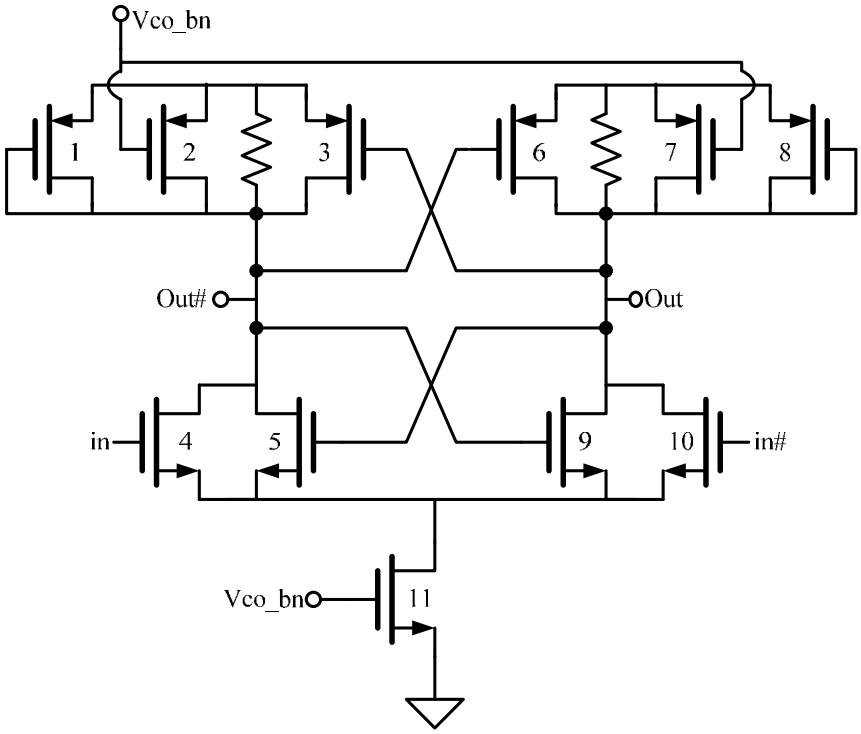


Fig.5.7 VCO delay cell

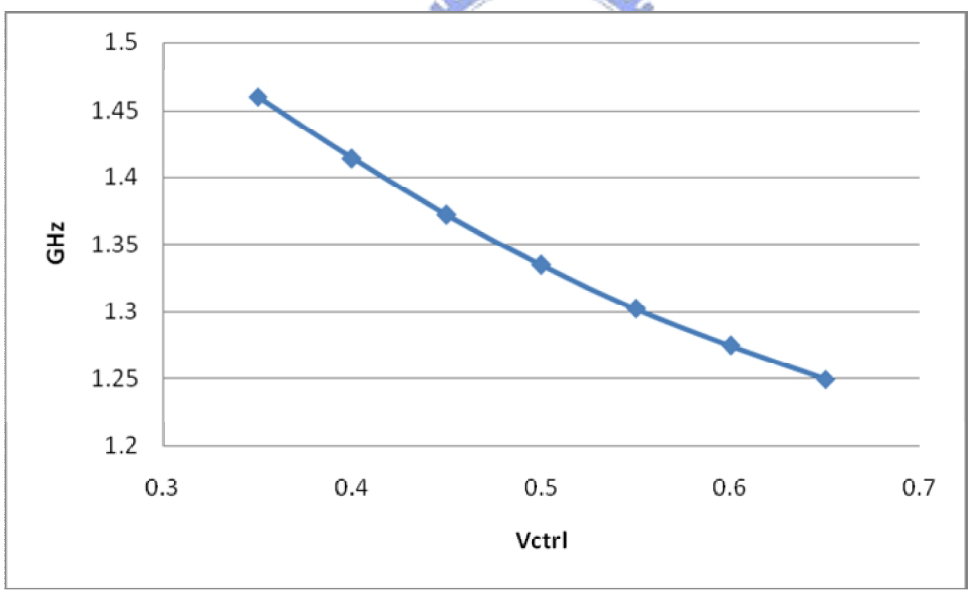


Fig.5.8 Operating Frequency with different Vctrl voltage(post-layout)

5.4.5 Multiplexer and Interpolator

Fig.5.9 and Fig.5.10 illustrate the multiplexer and interpolator, respectively. Both

of them are used in the phase rotator. The multiplexer and interpolator design are also based on the delay cell design [16], which consists of the symmetric load and the differential pair. Additional bias circuit for the multiplexer and interpolator is required to limit the output swing for low jitter purpose. The multiplexer selects the adjacent phase from VCO and send it to the phase interpolator. The proposed interpolator generates the corresponding phase rotation with a specific interpolation ratio. It would produce the correlated frequency deviation in the process of the phase rotation. The interpolator changes its interpolation ratio with a thermal code control for the reason of the monotony of phase rotation.

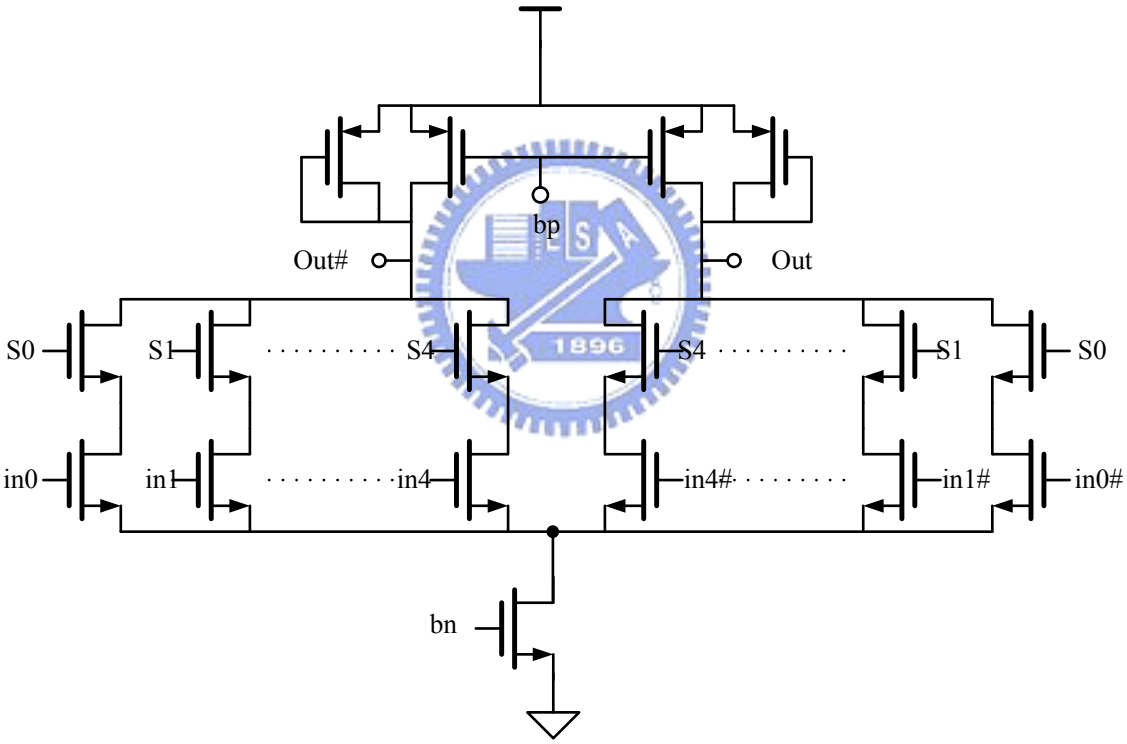


Fig.5.9 Multiplexer

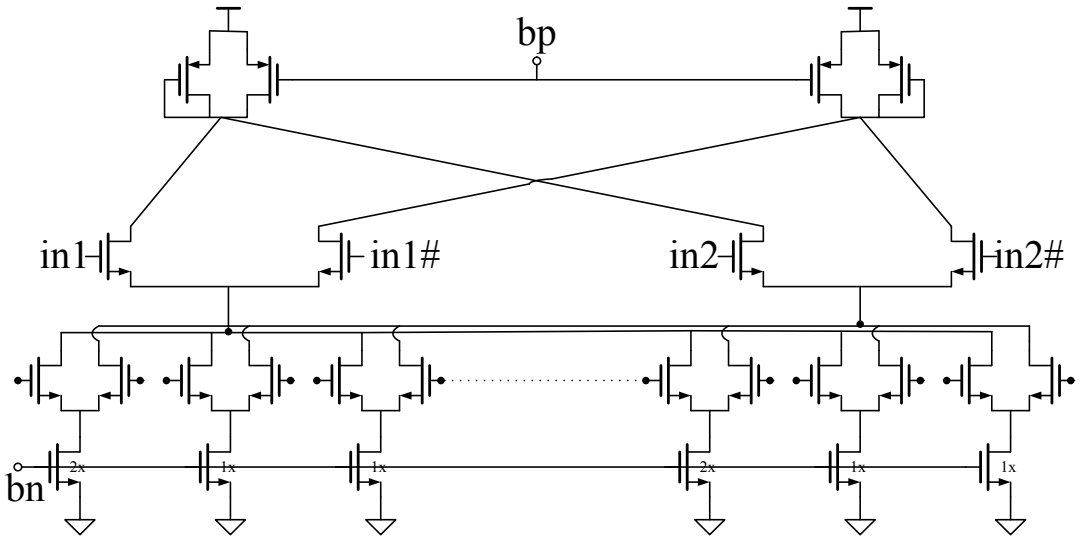


Fig.5.10 Thermal code controlled interpolator

5.4.6 Divider

The frequency divider in the feedback path of PLL is to divide by 12 as shown in Fig.5.11. We use the asynchronous circuit blocks in order to overcome the speed limit of divider and to lower the power saving consumption at the same time. The first divide-by-2 block is placed at the first stage of the divider since it experiences the fastest operating frequency from the VCO output. The other divide-by-2 block is adopted behind the divide-by-3 to adjust the duty cycle of the divid3-by-3 output to reach a 50% duty cycle. At the last stage, a D flip-flop re-samples the clock dividing by 12 to align with the input clock. On the other hand, the last stage D flip-flop suppresses the accumulated jitter due to the asynchronous operation. We use the true single phase circuit (TSPC) in the circuit implementation of divider for the purpose of the high speed requirement.

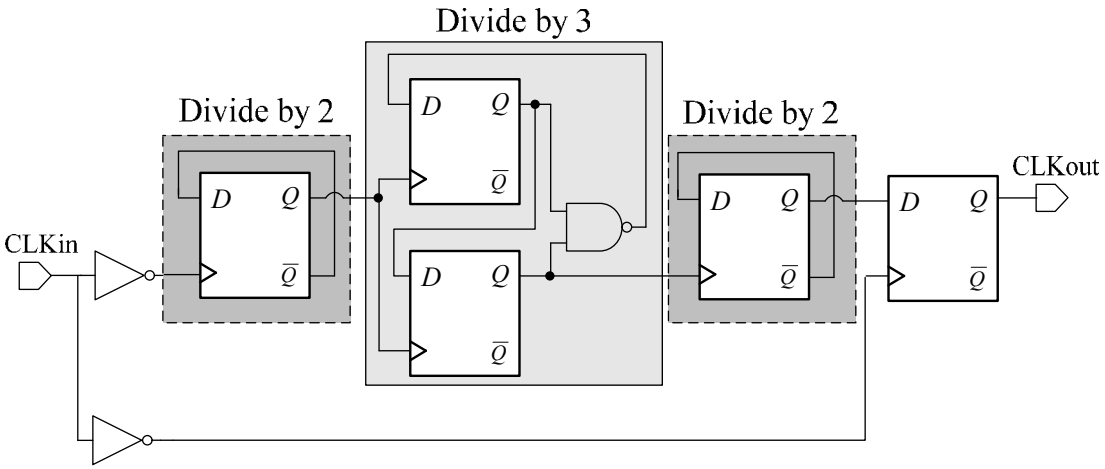


Fig.5.11 Schematic of divider

5.5 Circuit Simulation

Because the circuit implementation involves the analog and digital design, a mixed-signal simulation tool is requested to simulate the mixed-mode circuit. We simulate the analog circuit behavior with HSPICE and the mixed-signal simulation is carried out by NENO-SIM.

We simulate the modulated clock signal and non-modulated clock signal for the same time such that both have the total signal power. An FFT calculation is adopted to display the frequency domain behavior of the VCO output clock with and without modulation. Fig.5.12 (Pre-Layout) presents the spectrum of the VCO output waveform with and without spread spectrum operation. The VCO output clock is operating at 1.38GHz, the modulated clock is down-spreading 5000 ppm and the corresponding EMI reduction is 20.6dB. The time domain simulation results of the proposed SSC are shown in Fig.5.13. This diagram shows the period of VCO output vs. time. The maximum cycle-to-cycle jitter is about 1.128ps during the spread spectrum operation.

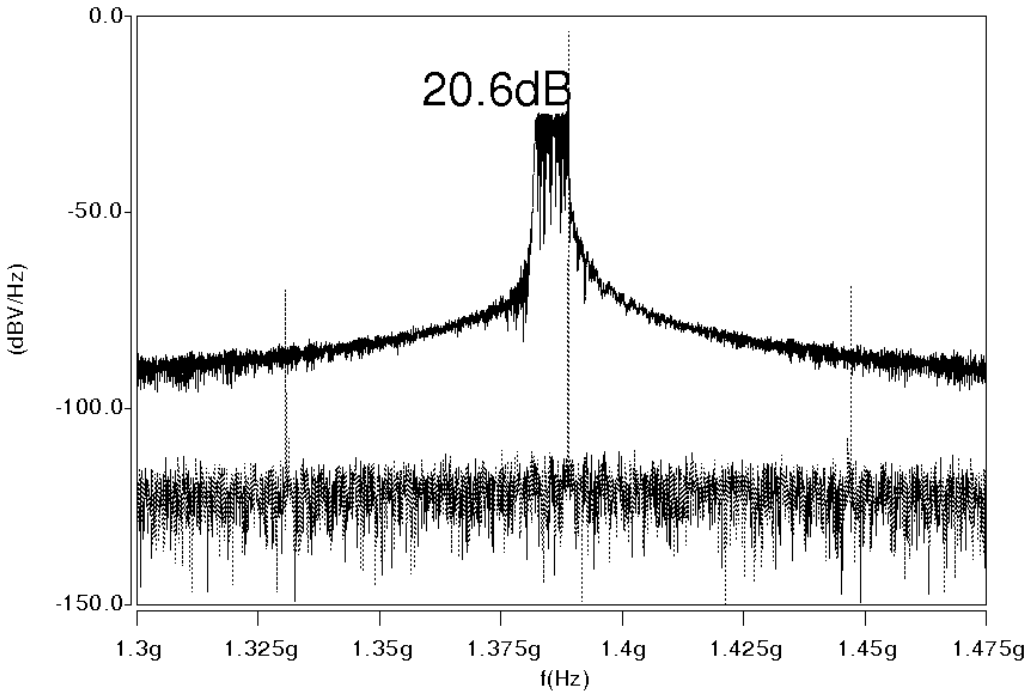


Fig.5.12 Spectrum of VCO output clock with and without spread spectrum modulation(Pre-Layout)

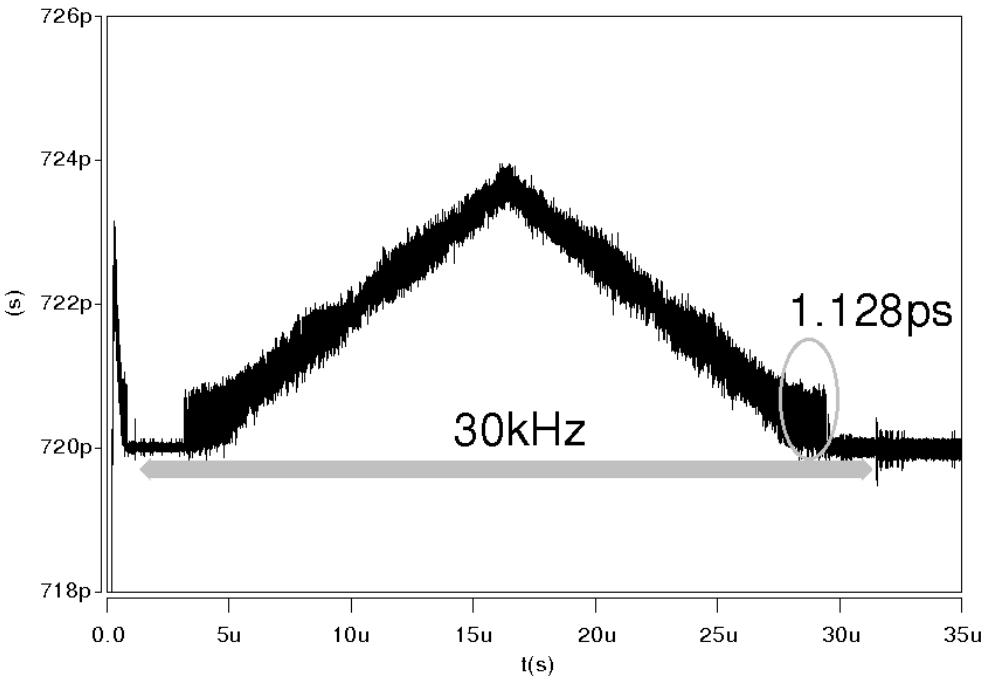
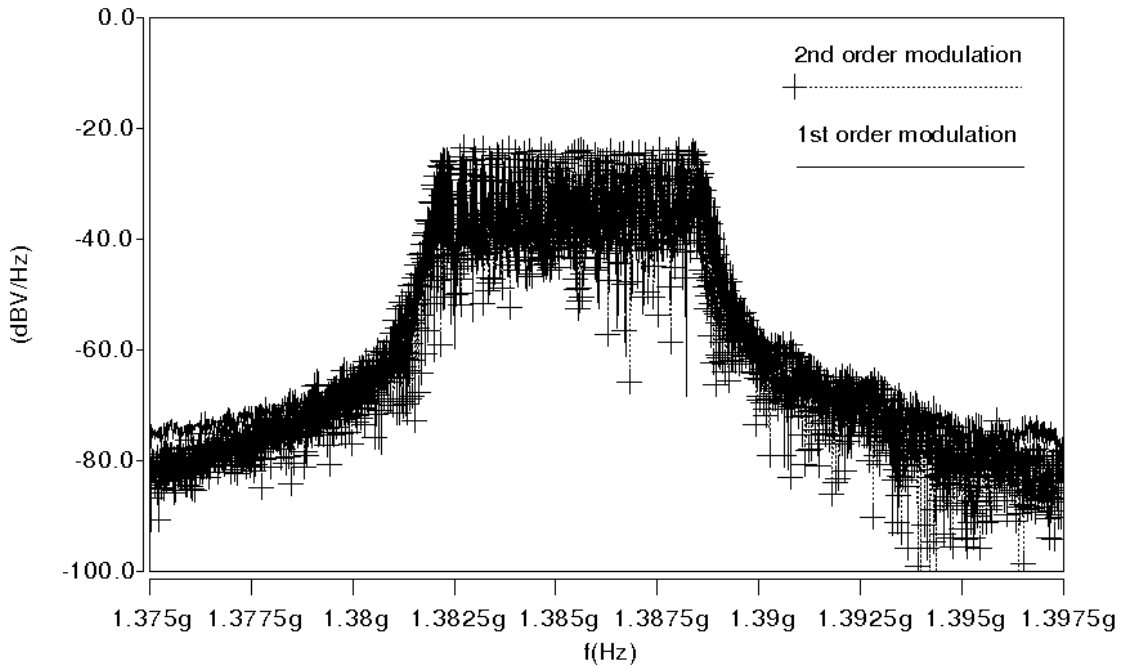
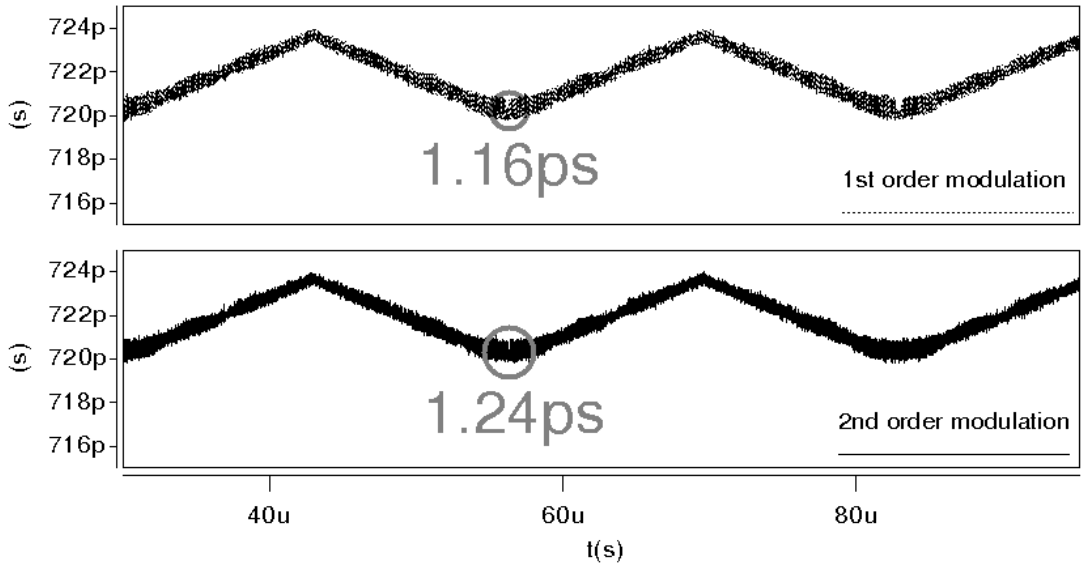


Fig.5.13 Period of VCO output waveform vs. time(Pre-Layout)

Fig.5.14 presents the spectrum and timing diagram of modulated clock signal with 1st and 2nd order modulator. The spectrum of SSCG with 1st order modulator is marked with solid line and the spectrum of SSCG with 2nd order modulator is marked by + with dashed line. Both of them almost overlap with the each other. This is consistent with the analysis as shown in Fig.3.16 (a). The period of VCO output waveform vs. time is shown in Fig.5.14. The first order one is presented with dot line and the second one is presented with solid line. The cycle-to-cycle jitter performance is better in the 1st order case due to the small input step to the PLL system. Hence, a circuit design with 1st order sigma delta modulator would be adopted.



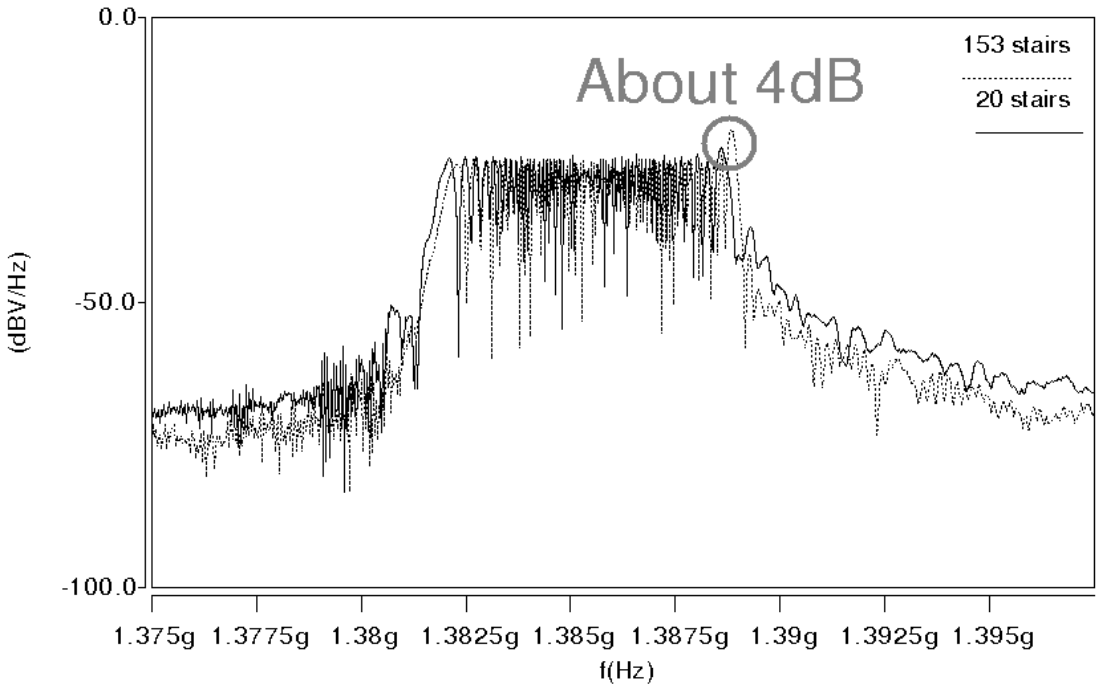
(a)



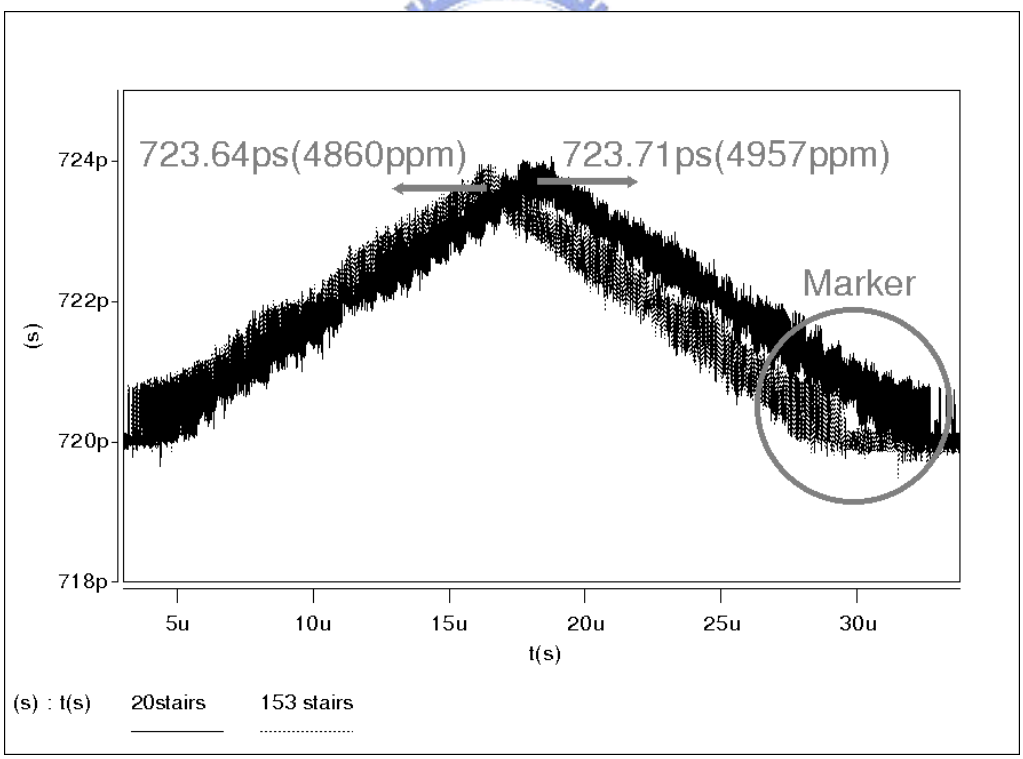
(b)

Fig.5.14 1st order and 2nd order modulation comparison (a) spectrum (b) Period of VCO output waveform vs. time(Pre-Layout)

Fig.5.15 shows the different number of stairs in the modulation profile. We adopt 153 stairs and 20 stairs to verify our analysis in Chapter 3. Fig.5.15 (a) shows a larger spike in 153 stairs case than 20stairs one about 4dB. This is because our design is based on $\frac{\omega_t}{\omega_{ref}} = \frac{1}{50}$ which represents a slow response system. The slow response system might experience an undesired frequency accumulation in high frequency band due to slow response as shown in Fig.3.16 (b). The desired maximum frequency deviation can not be reached as shown in Fig.5.15 (b). The circle marker shown in Fig.5.15 (b) presents the 153 stairs case seems to stop the spread spectrum behavior first. The resolution of phase rotation has been decided by $\frac{1}{160} T_{VCO}$. Hence, too many stairs in modulation profile would lead to a stop action of spread spectrum behavior due to the insignificant amount of phase rotation.



(a)



(b)

Fig.5.15 153 stairs and 20 stairs comparison (a) spectrum (b) Period of VCO output waveform vs. time(Pre-Layout)

A post-layout simulation result of non-spreading clock is shown as Fig.5.16. It presents the RMS jitter is 0.8ps and the peak-to-peak value is up to 3.88ps. The jitter histogram is also shown in Fig.5.16. A jitter distribution is usually Gaussian and centers at the middle the ideal clocking edge. Once mismatches of the circuit occur, this would lead to an unbalanced jitter distribution, such as current mismatch in CP, leakage current. The eye diagram of uniformly distributed multi-phase output waveform of VCO is shown in Fig.5.17. There are ten uniformly distributed phase because five stages of VCO is adopted. Fig.5.18 shows the timing diagram of VCO control voltage during the acquisition process. The VCO control voltage settles until the PLL system is in lock. The settling time is less than 3us as shown below.

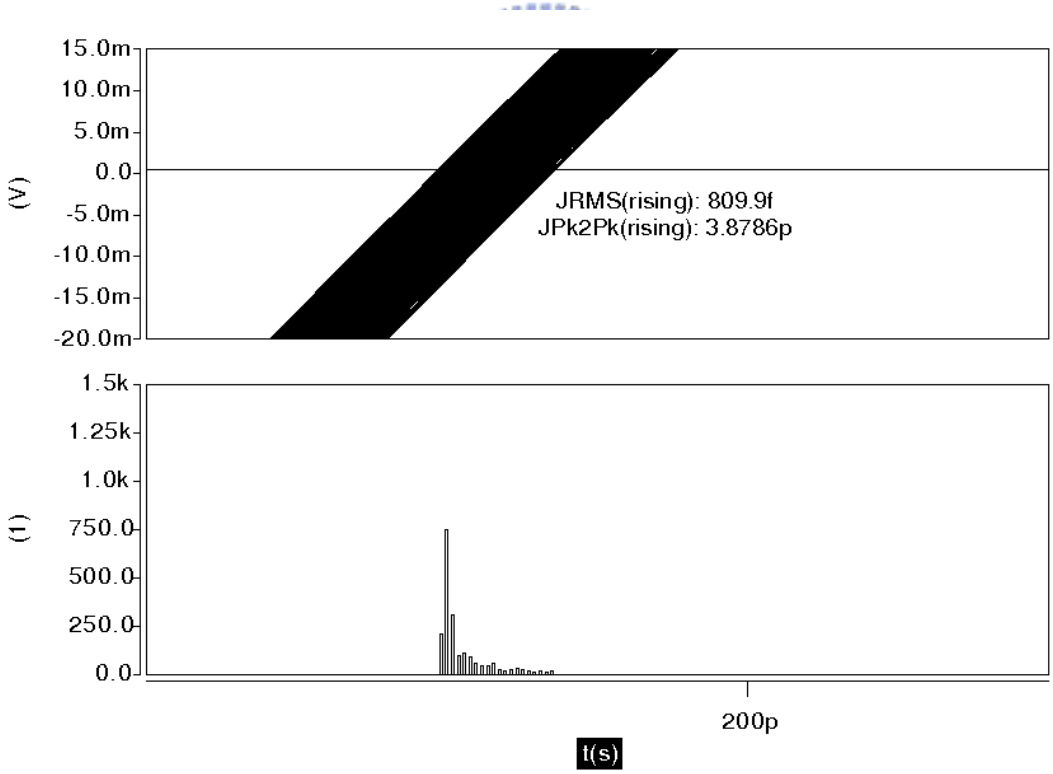


Fig.5.16 Eye diagram of VCO output and Jitter histogram without SSC(Post-Layout)

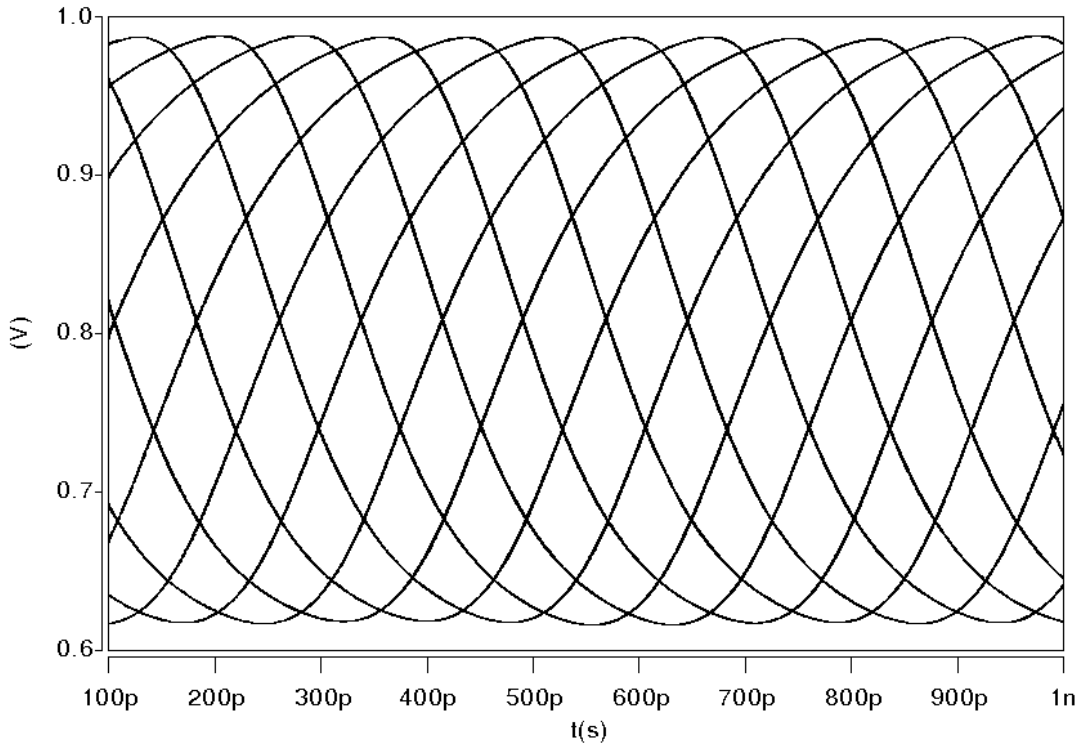


Fig.5.17 VCO output waveform(Post-Layout)

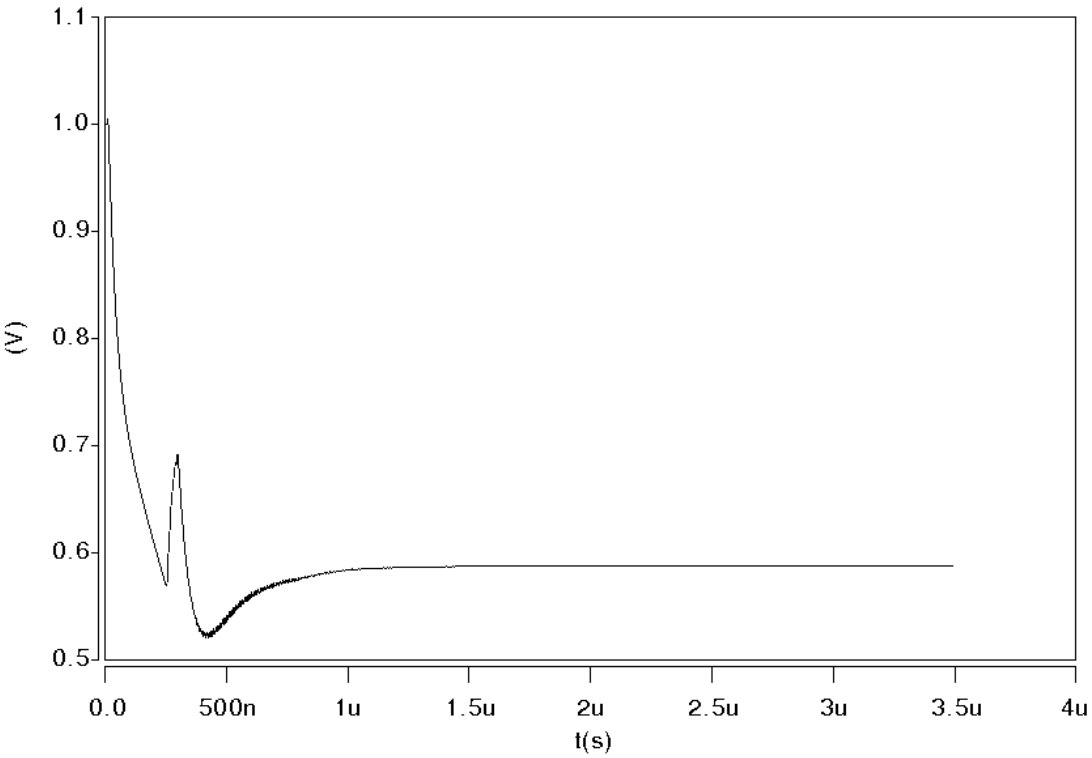


Fig.5.18 V_{ctrl} tracking behavior(Post-Layout)

The simulation results of PLL and SSCG are summarized in Table.5.2 and Table.5.3, respectively. The spread spectrum modulation block is inserted into the PLL loop to perform the spread spectrum operation and the original PLL design remains unchanged. The power consumption in SSC mode includes the original PLL power consumption and the phase rotation block, including multiplexer, interpolator and relative buffer. Table.5.4 shows the comparison with other SSCG.

Table.5.2 Design summary of the proposed PLL

Items	PLL	
Technology	UMC 90nm 1P9M	
Power Supply	1V	
Crystal Frequency	100MHz	
VCO tuning frequency	1.3~1.5GHz	
K_{VCO}	670MHz/V	
Settling time	<3us	
Jitter performance	σ_{RMS}	810fs
	σ_{p2p}	3.88ps
Power consumption	5.87mW	
Core Area	Main circuit	$170\times80um^2$
	Loop Filter	$235\times325um^2$

Table.5.3 Design summary of the proposed SSCG

Modulation Frequency	30kHz	
Max. Frequency Deviation	4983ppm	
EMI reduction	20.6dB	
Core Area	PLL Main circuit	$170\times80um^2$
	Loop Filter	$235\times325um^2$
	Phase Rotation Block	$170\times20um^2$
Jitter performance	Cycle-to-cycle (P2P)	1.13ps
Power consumption	7.57mW	

Table.5.4 Comparison of SSCG

	Proposed SSCG	ISSCC2005 [11]	ISSCC2005 [10]	ISSCC2006 [9]
Technology	90nm	0.18um	0.15um	0.15um
Modulation Mechanism	Phase Rotation	Phase Selection	Modulation on Divider	Modulation on Input
Divider Ratio	12	60	37.5/75	---
Operating Frequency	1.2GHz	1.5GHz	1.5GHz	27MHz(reference clock)
Frequency Deviation	5000ppm (6MHz)	5000ppm (7.5MHz)	5000ppm (7.5MHz)	30000ppm
EMI Reduction	20.6dB	9.8dB	20.3dB	14dB
EMI Reduction/BW	3.43dB/MHz	1.3 dB/MHz	2.7 dB/MHz	
Power Consumption	7.57mW	---	54mW	---
Power Consumption/VDD^2	7.5mW/ V^2		24 mW/ V^2	

5.6 Experimental Results

5.6.1 Layout and Pad Assignment

The proposed SSCG has been implemented with 90nm CMOS process. Fig.5.19 shows the chip layout of SSCG and the area of the PLL main circuit is $170\times80um^2$. The area of phase rotator is $170\times20um^2$ not included (the digital control block). Both are denoted as PLL as shown in Fig.5.19. The area of the loop filter is about $235\times325um^2$. The SSCG digital control block has been integrated into the total digital control (CDR & SSCG Ctrl), including clock and data recovery (CDR) algorithm block. The total circuit area is$1.25\times1.1(mm^2)$, including Equalizer (EQ), Phase-Locked Loop (PLL), Clock and Data Recovery (CDR), output driver, power

supply de-coupling capacitance, bias capacitance and pad.

Table.5.5 Pad Assignment presents the corresponding pad assignment and describes the pad configuration. The high speed inputs/outputs, including EQ input/output, SSCG output, CDR recovered clock, CDR recovered data, are routed as GSGSG mode for measurement concern. All power pads and DC bias are shown in the second kind of pad in Table.5.5 Pad Assignment and corresponding de-coupling and bias capacitor are near them. These power supply pad are placed outer circle to decrease the bonding inductance. We separate the analog and digital power supply to decrease the supply noise effect. The low speed control signal, slow output built-in testing signal and PLL input reference clock are grouped as the third kind of pad.

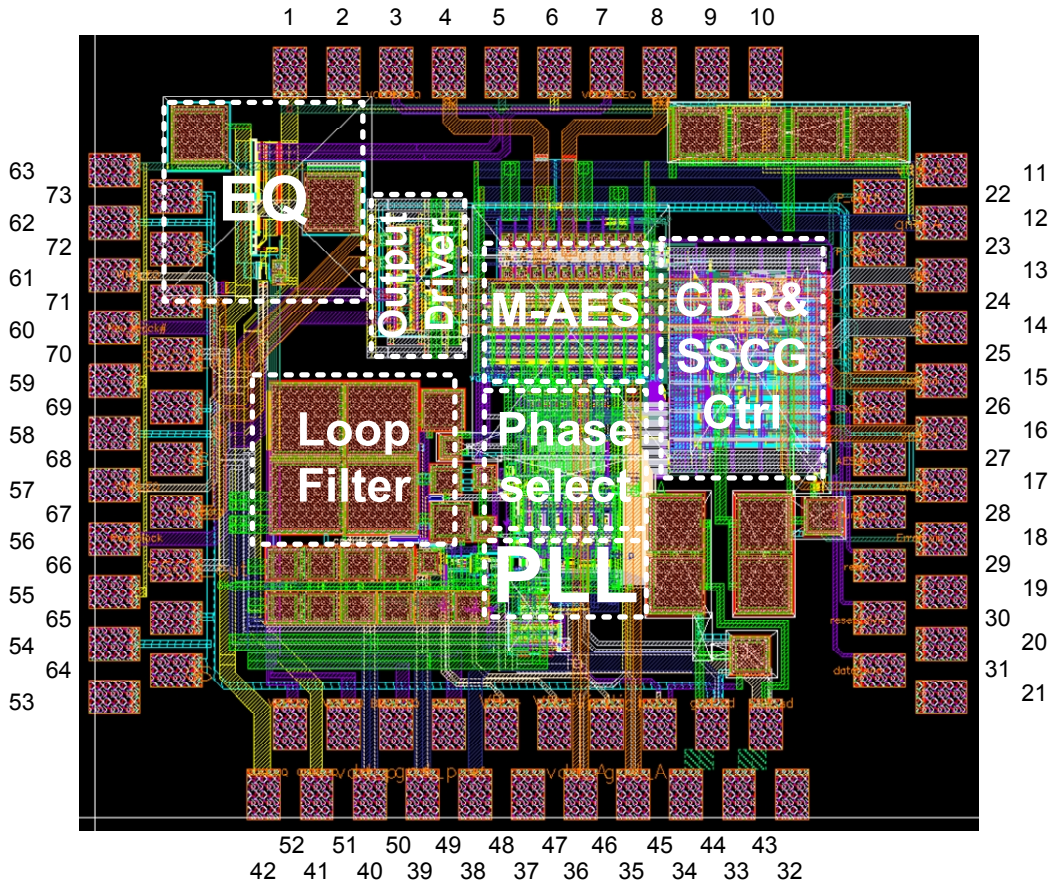


Fig.5.19 Chip Layout of SSCG

Table.5.5 Pad Assignment

	Pad	Function
High-Speed Input / Output (using GSGSG)	1,2,5,6,9,10,54,55,58,59,62,63,64, 65,68,69,72,73	Ground
	3,7	Equalizer output
	4,8	CDR input
	56,60	Recovered Clock
	57,61	Equalizer input
	66,70	SSCG output
	67,71	Recovered Data
Supply and Bias	11,12,35,36	Analog VDD/GND
	13,14	Digital VDD/GND
	15,16,33,34	Driver VDD/GND
	39,40	PLL VDD/GND
	41,42	Equalizer VDD/GND
	17,45,49	Driver Bias
	46	PLL start-up
	47,48	PLL R-variable
	50	Equalizer Bias
	51,52	Equalizer R-variable
Control signal & Low-Speed Input / Output	38	PLL Reference
	18	BER measure
	31	Data enable
	22,23	G_P ctrl
	24,25	G_I ctrl
	26	SSC enable
	27	AES enable
	28	BER measure enable
	29,30	Reset, Divider reset

5.6.2 Measurement setup

Fig.5.20 presents the measurement setup of the proposed design, including CDR and SSCG. The PLL input reference clock is produced by the Signal Generator (Agilent 81130A). The output spectrum is observed a Spectrum Analyzer (Agilent E440A) and the corresponding timing waveform is shown in Oscilloscope (Tektronics TDS6124C).

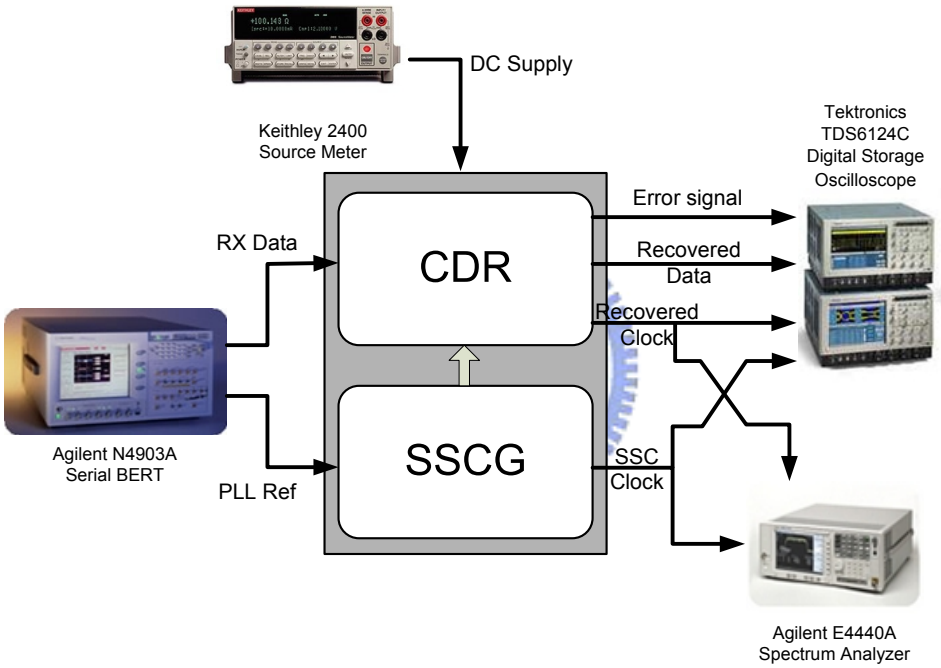


Fig.5.20 Measurement setup

Chapter 6
Conclusions

We have developed a spread spectrum clock generator for SATA specification using a 90nm CMOS process. The EMI reduction is 20.6dB while the modulation frequency is 30kHz and the required spread spectrum modulation deviation is down-spreading 5000ppm. The main contribution of this thesis is to develop a methodology to guide design for a low-jitter, high EMI reduction spread spectrum clock generator(SSCG).

We describes the four popular kinds of modulation mechnism and the corresponding noise transfer function is derived to obtain the quantization noise effect on the VCO output. A technique that has the minimum DC gain of noise transfer function is adopted in this design. The transient response analysis of spread spectrum behavior with different system parameters is performed to find out the relationship between the PLL system parameters and total EMI reduction, cycle-to-cycle jitter performance.

We introduces the concept of phase rotation used in the spread spectrum. A steady state phase rotation mechnism is developed and a thermal code control is provided to guareentee the monotony variation of phase rotation process. A phase rotator consists of multiplexer, interpolator and digital control is used to solve the

glitch problem induced by multiplexer operation. We also describes the design consideration of sigma delta modulator and the corresponding analysis of quantization noise is presented.

Finally, the circuit implementation of the proposed PLL and the corresponding simulation is provided. To achieve low jitter issue in our design, PLL uses error amplifier to resolve the current mismatch in charge pump and a third order loop filter is adopted to reduce the reference spur and quantization noise. A passive resistor is presented in the VCO delay cell to reduce the K_{vco} gain and an additional cross-couple CMOS is also included to the delay cell to boost the operation of delay cell. The non-spread clocking has a peak-to-peak jitter of 3.88ps and consumes 5.87mW at 1.4GHz. The EMI reduction in this circuit is about 20.6dB.

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