國 立 交 通 大 學

電子工程學系　電子研究所碩士班

碩　士　論　文

相容於標準金氧半技術之光接收機前端電路

Monolithically-Integrated Optical Receiver Front-End in Standard CMOS Process

研 究 生：黃世豪

指導教授：陳巍仁

中華民國九十七年九月

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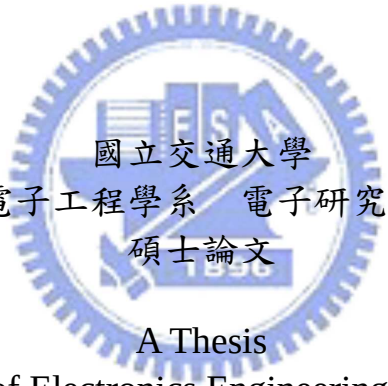

國立交通大學

電子工程學系　電子研究所

碩士論文

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摘要

本篇論文提出兩個相容於 0.18 微米標準金氧半技術之高速光接收機電路。這兩個光接收機收到光訊號以後，可以將光訊號轉換成 800 毫伏特的電壓訊號來推動 50 歐姆的輸出端負載。

在第一項電路中，它將一個空間調變光感測器(Spatially Modulated Light)、一個轉阻放大器和一個後級限伏放大器整合在單一晶片裡面。利用空間調變光感測器和適應性的類比等化器(Equalizer)使本電路可以操作到每秒 31.25 億位元的資料速度。整顆晶片耗功 175 毫瓦。晶片面積是 0.7 平方毫米。

另外一項電路，它也整合了一個光感測器、一個轉阻放大器和一個後級限伏放大器在單一晶片裡面。在不改變製程技術的情況下，我們提出一個新型的 PIN 光感測器。因為有它，所以不需要等化器就可以操作到每秒 25 億位元的資料速度。整顆晶片耗功 138 毫瓦。晶片面積是 0.53 平方毫米。

Monolithically-Integrated Optical Receiver Front-End in Standard CMOS Process

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Abstract

The thesis presents two solutions of the monolithically-integrated high-speed optical receivers in standard 0.18-μm CMOS technology. The optical receivers are capable of delivering 800 mV_{pp} to 50 Ω output load after optical to electrical conversion.

For the first one, it integrates a spatially modulated light (SML) detector, a transimpedance amplifier (TIA), and a post limiting amplifier on a single chip. A 3.125 Gbps high speed operation is achieved by utilizing SML detector and adaptive analog equalizer (EQ). The total power dissipation is 175 mW, and the chip size is 0.7 mm^2.

For the other, it also includes a photodetector, a TIA, and a post limiting amplifier on a single chip. A novel PIN detector is proposed and adopted in this design without technology modification. It can operate up to 2.5 Gbps without an equalizer. The total power dissipation is 138 mW, and the chip size is 0.53 mm^2.

Acknowledgment

經歷了 2005 年 7 月到 2008 年 9 月這交大碩士班兩年時間，我終於拿到畢業證書。這段時間真的多很多，以後不知道還不會多更多。我的意思是：在專業知識上多很多，在處理事情的成熟度上也多很多。還好啦！之前的學長也是兩年畢業。

感謝我的指導教授陳巍仁老師，在我專業知識上的指導。碩士班一起奮鬥"傻傻分不清楚"的松諭和宗裕、"張巧玲瓏"的張巧玲、黃金 307 實驗室所有學長和學弟，感謝你們給我這段時間快樂的回憶。也得感謝林森五少和新莊四少在大學和碩士期間所提供的休閒娛樂。另外，必須感謝我的家人和 CI 現役的郁玲，不斷地對我付出和關懷，讓我可以無後顧之憂完成碩士學位。最後，感謝我的觀世音菩薩，我畢業了！

黃世豪 08, Sep., 2008

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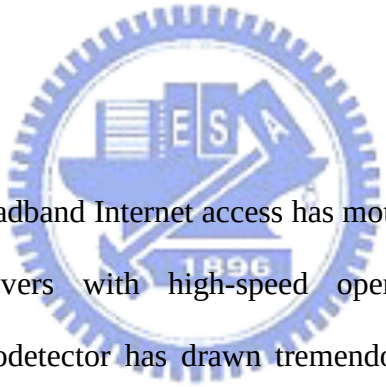
Chapter 1

Introduction



The growing demand on broadband Internet access has motivated development of low-cost, high-sensitivity optical receivers with high-speed operation. Optical receiver with monolithically-integrated photodetector has drawn tremendous research efforts recently. In contrast to conventional multi-die solutions, which composed of photodetector implemented in more expensive GaAs or InP-InGaAs technology, the fully integrated optical receiver is much more cost effective. Besides, the issues of parasitic capacitance introduced by ESD pads and leading inductance for multi-die integration can be avoided.

The fully-integrated optical receiver front-ends presented in this thesis are designed in standard 0.18 μm digital CMOS technology. The reason for choosing deep-sub-micron CMOS technology is the possibility to easily integrate a signal-processing part. The signal does not leave the chip after the optics received by photodetector in the receiver front-end. Therefore, output driver and output impedance matching are saved in system-on-a-chip (SoC).

1.1 Motivation

Over the past several decades, complementary metal oxide silicon (CMOS) technologies have the advantage that they are developed much more rapidly on the market than the other technologies, such as bipolar and BiCMOS. Thus, bipolar and BiCMOS technologies are more expensive than CMOS process of the same structure size.

Besides, the optical communication systems operate at wavelengths near 850 nm is of interest due to the wide availability of laser sources. Therefore it is obviously that CMOS is suitable for optical interconnection owing to the advantages of high-density and low-cost. They can be used in short distance and high volume communication systems, such as optical storage system, local area network and back plane interconnect.

Optical Pickup Unit

Data on an optical disc is physically contained in pits which are precisely arranged on a spiral track. Figure 1-1 illustrates the light beam generated by the laser diode, passing through a diffraction grating, directed by polarization beam splitter and mirror. Finally, the light passes through the objective lens. When a light beam strikes a land interval between two pits, the light is almost totally reflected. On the other hand, when it strikes a pit, destructive interference occurs and a lower light intensity is returned.

The reflected light passes through the objective lens, then directed by mirror and polarization beam splitter. Finally, it will project onto the photodetectors array in receiver IC. If higher light intensity is received, then photodetector generates larger photocurrent, and vice versa. Thus, data one or data zero can be interpreted.

The use of blue laser provides a dramatic increase in storage capacity. Therefore, monolithically-integrated optical receivers with high-speed operation are suitable for the next-generation optical stage systems.

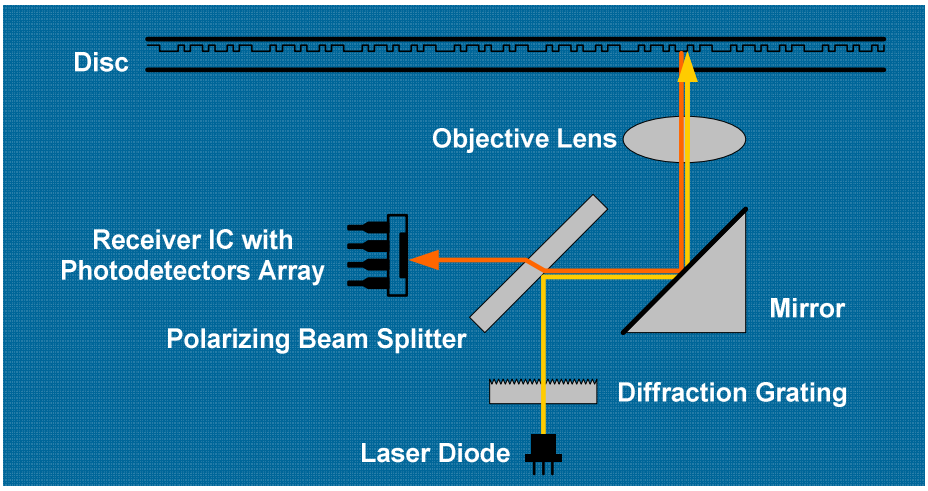


Figure 1-1 Simplified optical pickup organization.

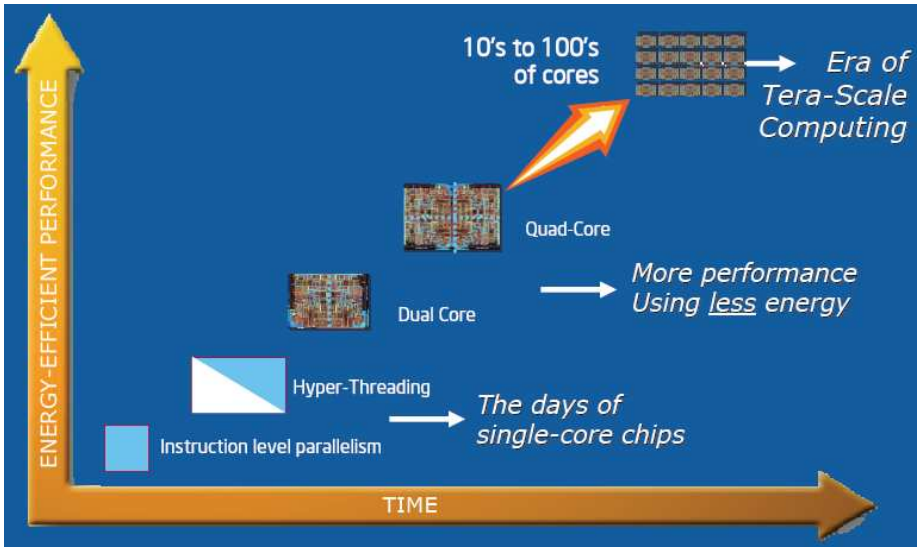


Figure 1-2 The scenario of tera-scale computing.

Tera-Scale Computing

Figure 1-2 illustrates a scenario of tera-scale computing projected by Intel. A multi-cores platform has become a main stream to realize an energy efficient computing system in the future. Meanwhile, more and more channel bandwidth are demanded to sustain the heavy data traffic between the multi-cores in the enormous computing system. In such a data intensive platform, high density electrical interconnects may suffer from severe cross talk and electro-magnetic interference. On the contrary, optical link can alleviate these difficulties in system integration while they provide more data bandwidth.

In order to achieve this data rate of tera-bit per second, it is a nice solution by using multi-channel optical communication owing to its less crosstalk and EMI effect. In addition, small form factor and low cost optical transceiver could be the enabling technologies to fulfill the bandwidth requirement and realize the tera-scale computing platform.

1.2 Thesis Organization

This thesis consists of seven chapters. The first one is the introductory chapter where motivation is given. The goal is to design a monolithically optical receiver in standard CMOS process, and bit-rates up to a fewer Gbps. This achievement can minimize the total cost of the optical system.

Chapter 2 describes the CMOS photodetectors including PN junction photodetectors, spatially modulated light detectors and a novel PIN detector. Also, the specifications and challenges of the all-silicon optical receiver are discussed in this chapter.

Chapter 3 introduces trans-impedance amplifier (TIA). First, I will point out the design issues. Then the pre-amplifiers and TIA topologies will be described and compared. Besides, the noise analysis and circuit implementation be introduced one by one. At last, simulation results will be showed.

Chapter 4 introduces limiting amplifier (LA). Architecture will be described first. Then, stage number decision is analyzed. Offset cancellation, Cherry-Hooper circuit. At last, the LA's simulated results will be showed.

Chapter 5 introduces the adaptive equalizer and output buffer.

Chapter 6 introduces the two OEICs which are realized by using the 0.18-μm standard CMOS technology. The measured results will also be showed in this chapter.

In chapter 7, final conclusion of the whole design is given.

Chapter 2

All-Silicon Optical Receiver

Typically, the speed enhancement techniques of the photodetector can be classified into two categories. One approach is to get rid of the slowly diffusive carriers to achieve a high speed operation [1]-[5], and the other approach is to compensate the frequency response of the photodetector by utilizing equalizer [6]. From technology aspect, the former approach can be achieved by using a buried oxide layer [4] or SOI [5] process, but it requires nonstandard CMOS technology and additional cost. An alternative approach is by employing spatial modulated light (SML) detector [1]-[2].

In this chapter, we will first discuss the PD's related general characteristics. Following section 2.1, the conventional PN junction photodetectors will be introduced in section 2.2. Owing to the shortcomings, such as low bandwidth and low responsivity, of PN junction photodetectors, then the high-speed spatially-modulated light (SML) detector is described in section 2.3. And section 2.4.introduces a novel lateral PIN. At last, the fully CMOS optical architecture will be introduced and system specifications will be listed.

2.1 General Characteristics

To design a CMOS photodetectors, what to do first is to understand the silicon characteristics. This section introduces the basics such as threshold wavelength, absorption coefficient, reflectivity, quantum efficiency and responsivity.

Threshold Wavelength (λ_g)

The energy of a photo is $E = h\nu$ where h is the Plank's constant, about 6.625×10^{-34} J-s or 4.135×10^{-15} eV-s, and ν is the frequency of the photo. It is given by

$$\lambda = \frac{c}{\nu} = \frac{hc}{E} = \frac{1.24}{E}(\mu m) \tag{2-1}$$

where E is the photo energy in eV and c is the speed of light, about 3×10^{8} m/s.

The creation of electron-hole pairs requires the photon energy to be at least equal to the bandgap energy E_g of the semiconductor material to excite an electron form the valance band to the conduction band. The threshold wavelength (or the upper cut-off wavelength) λ_g is therefore determined by E_g or,

$$\lambda_g = \frac{1.24}{E_g}(\mu m) \tag{2-2}$$

Table 2-1 [7] lists some typical bandgap energies and the corresponding threshold wavelengths of various photodiode semiconductor materials. It is clear that Si photodiodes cannot be used in optical communications at 1.31 μm and 1.55 μm.

Table 2-1 Bandgap energy and threshold wavelength for PD materials.

Materials	E_g (eV) @ 300K	λ_g (μm) @ 300K
GaAs	1.43	0.87
InP	1.35	0.91
Si	1.12	1.11
$In_{0.53}Ga_{0.47}As$	0.75	1.65
Ge	0.66	1.87

Absorption Coefficient (α)

Incident photos with wavelength shorter than λ_g become absorbed as they travel in the semiconductor and the light density, which is proportional to the number of photos, decays exponentially with distance into the semiconductor. The light intensity P at a distance x from the semiconductor surface is given by

$$P(x) = P_o \cdot \exp(-\alpha x) \tag{2-3}$$

where P_o is the intensity of the incident radiation and α is the absorption coefficient that depends on the photo energy or wavelength λ. Absorption coefficient α is a material property. For example, for Si, α can be approximated with the following formula [8]:

$$\log_{10}\alpha = 13.2131 - 36.7985\lambda + 48.1893\lambda^2 - 22.5562\lambda^3 \tag{2-4}$$

where λ is the wavelength of the input light signal. λ is given in μm whereas α is given in cm^{-1}. Most of the photo absorption (63%) occurs over a distance $1/\alpha$ and $1/\alpha$ is called the penetration length δ. For Si, α = 793.65 cm^{-1} and δ = 12.6 μm.

Figure 2-1 [7] shows α versus λ characteristic of various semiconductors where it is apparent that the behavior of α with the wavelength λ depends on the semiconductor material.

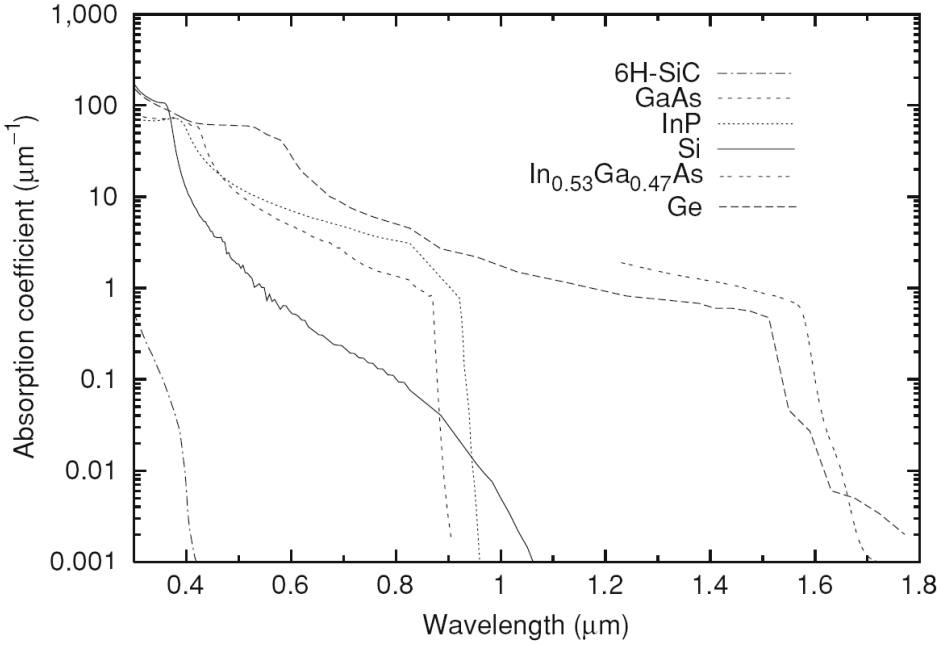


Figure 2-1 Absorption coefficient of several photodiode materials versus wavelength.

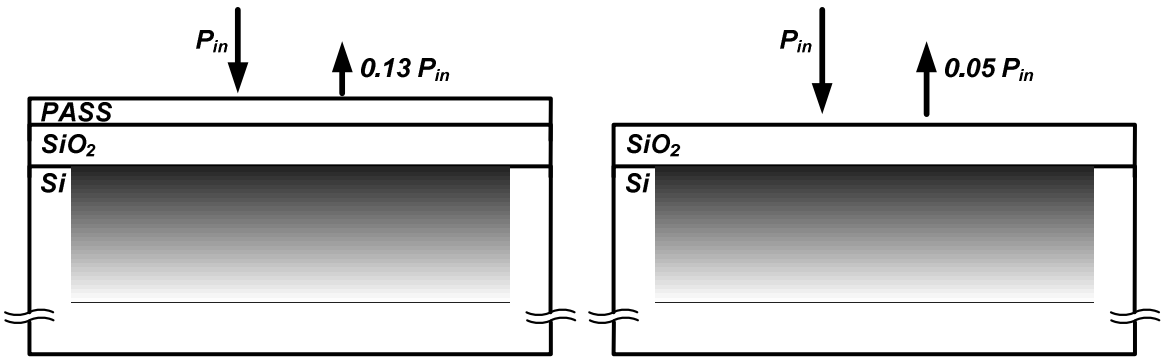
Reflectivity (*r*)

A fraction of incident optical power is reflected due to the difference in the index of refraction between the surroundings n_o (air: 1.0) and the semiconductor n_{si} (Si: 3.5). For a standard CMOS technology, the dielectric layers above the active region of photodetector comprise inter-layer dielectric, inter-metal dielectric (SiO_2: n_{so} ~ 1.45), and optional passivation layers (Si_3N_4: n_{sn} ~ 2.0), Using the impedance-transformation approach [9], the effective impedance, *Z*, and the reflectivity, *r*, of the photodiode can be expressed as:

$$Z = n_D \frac{n_{Si}\cos(kd) + i \cdot n_D \sin(kd)}{n_D \cos(kd) + i \cdot n_{Si} \sin(kd)} \tag{2-5}$$

$$r = \left| \left(\frac{Z - \eta_0}{Z + \eta_0} \right)^2 \right| \tag{2-6}$$

where $n_{D,}$ n_{si}, and n_o denotes the intrinsic impedance of the dielectric layers, silicon substrate, and air, respectively; *k* and *d* indicates the wavenumber and thickness of the dielectric layers, respectively. With 850-nm light, the simulation results reveal that the reflectivity is around 0.13 and 0.05 for the device with and without passivation layer, respectively. Therefore, the reflectivity can be improved by removing the passivation layer above the active region of the photodetectors. Figure 2-2 illustrates that the reflectivity with passivation layer is 2.6 times less than that with passivation layer in standard 0.18-μm CMOS process technology.



(a) (b)

Figure 2-2 The reflectivity with and without passivation in standard CMOS process.

Quantum Efficiency (η)

The quantum efficiency is defined as the average number of generated electron-hole pairs per incident photo. In the shallow CMOS technology, the optical light penetrates deeper into ilicon and some of the photogenerated carriers will be recombined and reduce the quantum efficiency. Typically, the value of quantum efficiency in a CMOS is about 40 % to 70 %.

Responsivity (R)

For the development of optical receiver circuits, it is interesting to know how large the photocurrent is for a specific power of the incident light with a certain wavelength. The responsivity R is a useful quantity for such a purpose:

$$R = \frac{I_{PD}}{P_{opt}} = \frac{q\lambda_o}{hc}\eta = \frac{\lambda_o \eta}{1.243} \left(A/W\right) \qquad (2\text{-}7)$$

where λ_o is in μm. The responsivity is defined as the photocurrent I_{PD} divided by the incident optical power P_{opt}. R depends on the wavelength, therefore the wavelength has to be mentioned if a responsivity value is given.

The dashed line in Figure 2-3 [7] represents the maximum responsivity of an ideal photodetector with h = 1 % or 100 %. Unfortunately, the quantum efficiency is reduced by the partial recombination of photogenerated carriers.

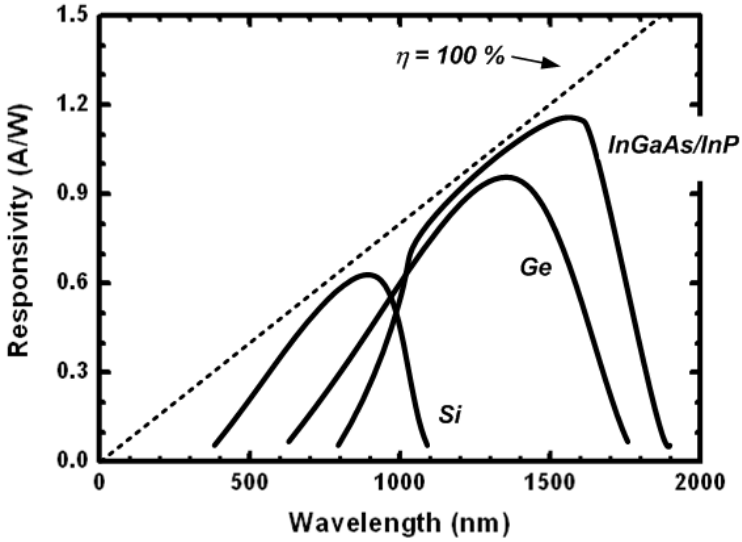


Figure 2-3 Responsivities of photodetectors as a function of wavelength.

2.2 PN Junction Photodetectors

The simplest way to build integrated photodetectors is to use the PN junctions available in standard CMOS technology. Figure 2-4 shows the typical PN diodes in the triple-well (including N-well, P-well and deep N-well (or DNW)) CMOS process technology. The PN junctions of D_1, D_2, D_3 and D_4 are N-well/P-substrate, P^+/N-well, N^+/P-well and P-well/DNW, respectively. The depletion regions of the PN photodetectors are shallow because they are less than 5 μm deep from the semiconductor surface.

When a photodetector is illuminated with an adequate light, its depletion region generates fast drift current whereas the neutral P-region and N-region generate slow diffusion current. Unfortunately, the shallow CMOS process technology cause a problem which originates from the long absorption length (about 12.6 μm) of silicon at 850-nm wavelength for high-speed applications. There is the percentage of 63% and 33% of the photon absorption occurs over a distance of 12.6 μm and 5 μm from the semiconductor surface, respectively. A large portion of carries are photogenerated within the P-substrate and move in all directions by diffusion.

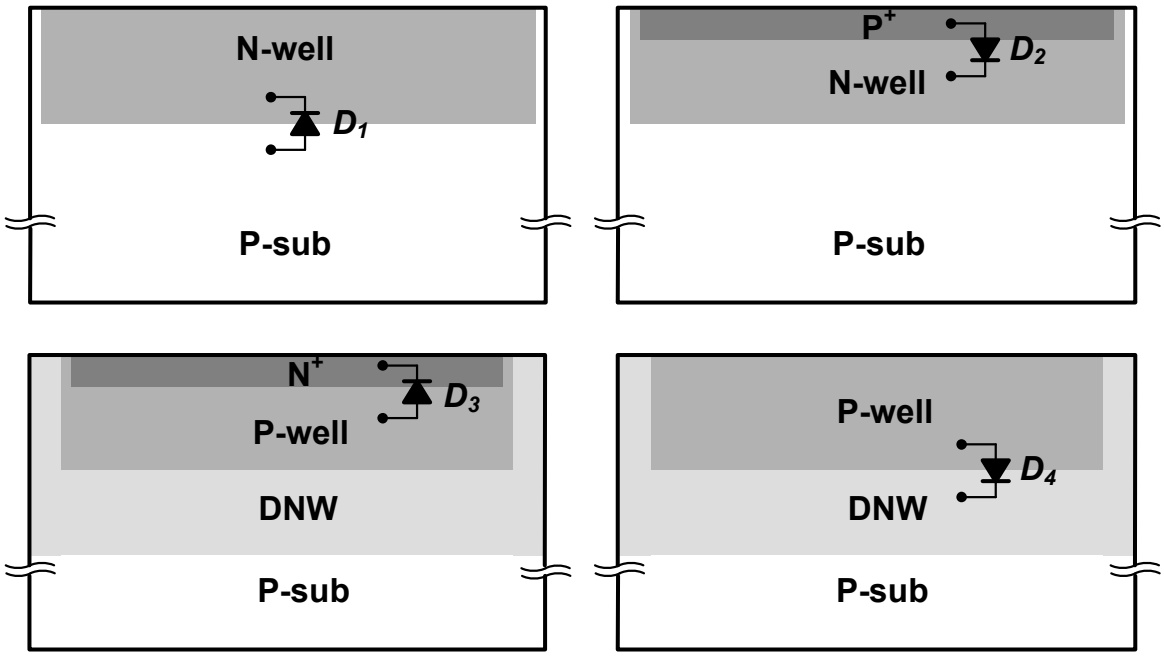


Figure 2-4 PN diodes in the generic CMOS technology.

Thus, for photodetector D_1, most of the photocurrent is the slow diffusion current which is generated by the P-substrate, thus the high -3 dB bandwidth of D_1 is quite low. Although D_2 and D_3 have higher bandwidth because of isolating the slow P-substrate diffusion current by N-wll or depp N-well, the shallow and narrow depletion region result in small responsivity. Compared to D_2, D_4 delivers larger responsivity. Unfortunately, D_2, D_3 and D_3 exhibit large parasitic capacitance owing to their high doping concentration. Thus, it is not easy to design a high-speed and high-responsivity PD under the un-modified digital CMOS technology.

2.2.1 Analysis of PN Junction Photodetectors

For the un-shaded area, the incident photon flux density is given by:

$$\Phi_o(t) = \frac{P_{opt}(t)}{A}\frac{\lambda}{hc}(1-r) \tag{2-8}$$

where $P_{opt}(s)$ is the input optical power, A is the device area, λ is the wavelength of the incident light, h is the Plank's constant, c is the speed of light, and r is the reflectivity.

Consider a single PN junction photodetector structure shown in Figure 2-5. The generation rates of carriers per unit volume is

$$g(x,t) = \alpha\Phi_o(t)e^{-\alpha x} \tag{2-9}$$

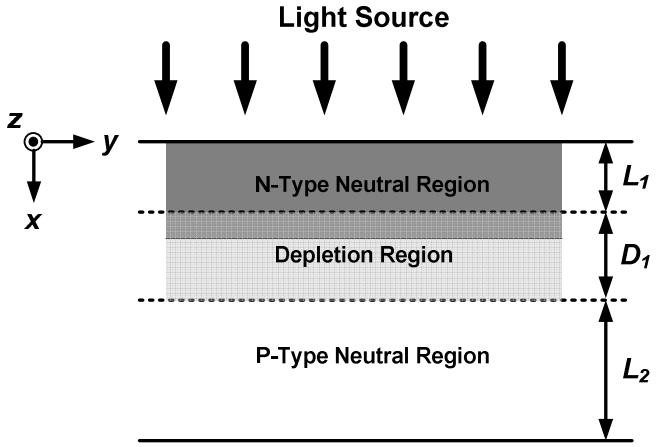


Figure 2-5 Cross section of a single PN junction PD.

N-Type Neutral Region

In the N-type neutral region, the continuity equation for holes in the time-domain is

$$\frac{\partial p_n(x,t)}{\partial t} = D_p \frac{\partial^2 p_n(x,t)}{\partial x^2} - \frac{p_n(x,t)}{\tau_p} + g(x,t) \tag{2-10}$$

where D_p is hole diffusion coefficient and τ_p is hole diffusion time in N-type neutral region. The boundary conditions are

$$\left.\frac{\partial p_n}{\partial x}\right|_{x=0} = 0 \tag{2-11}$$

$$p_n\big|_{x=L1} = 0 \tag{2-12}$$

If the concentration of hole-carriers is given, then the responsivity and frequency response of the diffusion current from N-type neutral region is got. In order to solve this problem analytically, the Laplace transform in the frequency domain is taken, and the Fourier series in the space domain is used [8]. Then the hole-carriers diffusion current can be solved as:

$$I_p(s) = \sum_{m=1}^{\infty} AqD_p\alpha \frac{(2m-1)\pi(-1)^{m+1} e^{-\alpha L_1} + 2\alpha L_1}{(\alpha L_1)^2 + \left[\frac{(2m-1)\pi}{2}\right]^2} \frac{(2m-1)\pi}{2L_1}(-1)^{m+1} \times \frac{\Phi_o(s)}{s + D_p\left[\frac{(2m-1)\pi}{2L_1}\right]^2 + \frac{1}{\tau_p}} \tag{2-13}$$

P-Type Neutral Region

In the P-type neutral region, the continuity equation for electrons in the time-domain is

$$\frac{\partial n_p(x',t)}{\partial t} = D_n \frac{\partial^2 n_p(x',t)}{\partial x'^2} - \frac{n_p(x',t)}{\tau_n} + g(x',t) \tag{2-14}$$

where D_n is electron diffusion coefficient, τ_n is electron diffusion time in P-type neutral region and $x' = x - (L_1 + D_1)$. The boundary conditions are

$$\left.\frac{\partial n_p}{\partial x'}\right|_{x'=0} = 0 \tag{2-15}$$

$$n_p\big|_{x'=L2} = 0 \tag{2-16}$$

Then the electron-carriers diffusion current in the P-type neutral region can be obtained as:

$$I_n(s)=\sum_{m=1}^{\infty} AqD_n\alpha e^{-\alpha(L_1+D_1)}\frac{2m\pi\left[1-(-1)^m e^{-\alpha L_2}\right]}{(\alpha L_2)^2+(m\pi)^2}\frac{m\pi}{2L_2}\times\frac{\Phi_o(s)}{s+D_n\left(\frac{m\pi}{2L_1}\right)^2+\frac{1}{\tau_n}} \qquad (2\text{-}17)$$

Depletion Region

In the depletion region, the fast drift current is

$$I_{dr}(s)=Aq\Phi_o(s)\left[e^{-\alpha L_1}-e^{-\alpha(L_1+D_1)}\right] \qquad (2\text{-}18)$$

Thus, the photocurrent of conventional PN junction photodetector can be expressed as

$$I_{ph}=I_p(s)+I_n(s)+I_{dr}(s) \qquad (2\text{-}19)$$

2.2.2 Simulation Results

Table 2-2 lists the simulated results of the PN junction PDs with reverse-biased voltage of 1.2 V. The conventional PN junction photodetectors have many disadvantages, such as low speed in N-well/P-substrate PD, small responsivity in P^+diff/N-well, N^+diff/P-well PD, and large parasitic capacitance in DNW/P-well, P^+diff/N-well, N^+diff/P-well PD. Thus, these CMOS photodetectors are not suitable for the general optical receiver to integrate directly without an equalizer or some good-performance front-end circuit.

Table 2-2 Comparison of the PN junction PDs with reverse-bias 1.2 V.

Diode Type	*-3dB Responsivity (mA/W)*	*-3dB Bandwidth (GHz)*	*Cap. per 65² μm² (fF)*
N-well/P-sub	379.1	0.001	473
P^+/N-well	30	1.3	3284
N^+/P-well	29.9	1.9	2983
P-well/DNW	49	1.2	2051

2.3 SML Detectors

From the perspective of a high speed light detection, the impacts coming from the slowly-diffusive current should be circumvented. In addition, to keep the wide depletion region and low parasitic capacitance, the lightly doing P-substrate and N-well will be adopted. Thus, an alternative approach is by employing spatially modulated light (SML) detector.

2.3.1 Basic Concepts

As shown in Figure 2-6, a SML detector consists of a row of photodetectors alternatively covered and uncovered with light blocking materials, such as metal layers. The covered detector is named dark detector, while the uncovered detector is named illuminated detector. As the slow carriers generated in the neutral regions of the photo detectors diffuse in all directions, they can be partially eliminated by subtracting the photo current collected by the dark detectors (mainly composed of slow carriers) from that of the illuminated detector (composed of both fast-drifting and slowly-diffusing carriers). So, the SML detector is capable of high-speed operation.

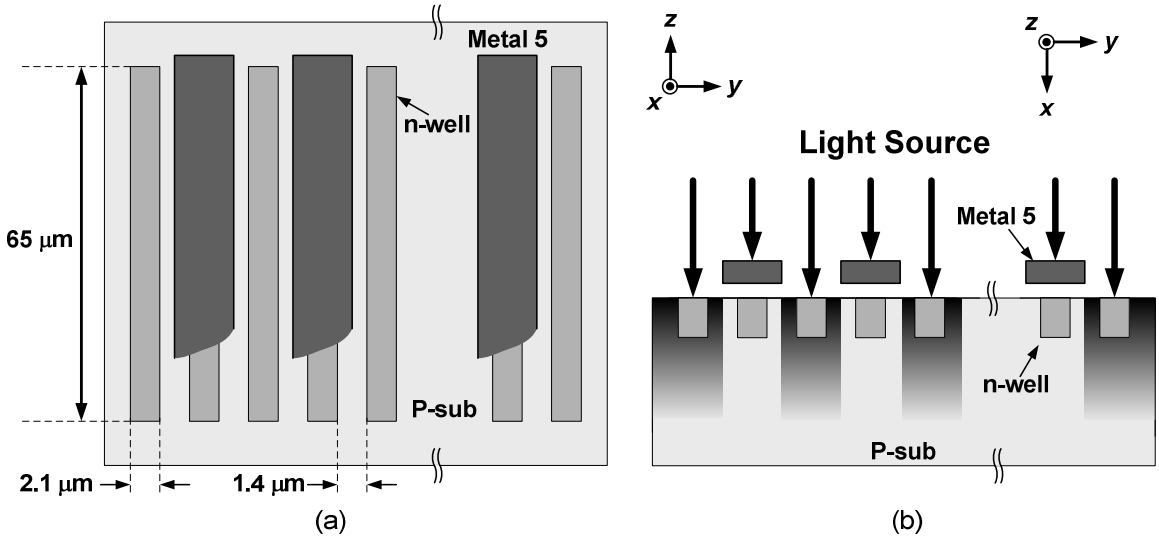


Figure 2-6 (a) top view, and (b) cross view of a SML detector.

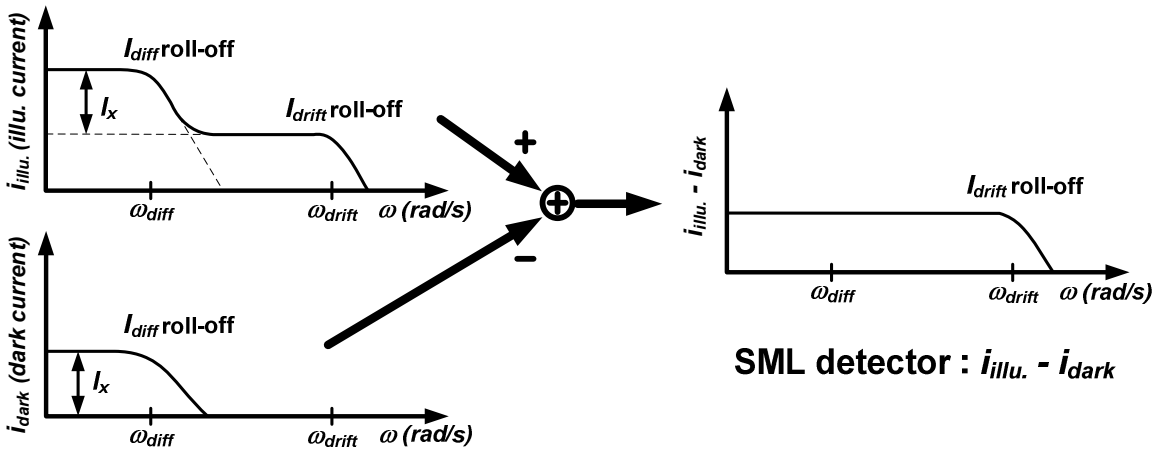


Figure 2-7 Frequency response of a SML detector's photocurrent.

The photocurrent component of a SML detector is shown in Figure 2-7. The illuminated current ($i_{illu.}$) collected by illuminated detectors consists of the fast drift current from depletion region, the slow hole-carriers diffusion current from N-well neutral region, and slow electron-carriers diffusion current from the P-substrate. On the other hand, the dark current ($i_{dark.}$) collected by illuminated detectors only consists of the slow electron-carriers diffusion current from the P-substrate. If the slow electron-carriers diffusion current generated by the P-substrate diffuse the same amount (Ix) of current to the illuminated and un-illuminated detectors at the same time, then most of the slow diffusion current can be removed ($i_{illu.}$ - i_{dark}) by utilizing a differential TIA followed by a SML detector.

2.3.2 Analysis of SML detector

The photocurrent of the proposed SML detector can be expressed as:

$$I_{ph} = I_{illu} - I_{dark} = I_p + I_{nI} - I_{nD} + I_{dr} \tag{2-20}$$

where I_p is the hole diffusion current in the N-well neutral regions, I_{nI} and I_{nD} are the electron diffusion current in the P-substrate neutral regions of the illuminated detectors and the dark detectors, respectively, and I_{dr} is the drift current in the depletion regions.

Then the hole-carrier diffusion current can be solved as:

$$I_p = \sum_{m=1}^{\infty}\sum_{n=1}^{\infty}\sum_{k=1}^{\infty} \frac{Aq\alpha\Phi_o D_p}{2L_{YP}L_{ZP}} \times \frac{(2m-1)\pi(-1)^{m+1}e^{-\alpha L_1} + 2\alpha L_1}{(\alpha L_1)^2 + \left[\frac{(2m-1)\pi}{2}\right]^2} \times \frac{4}{(2n-1)\pi} \times \frac{4}{(2k-1)\pi}$$
$$\times \frac{1}{j2\pi f + D_p\left[\frac{(2m-1)\pi}{2L_1}\right]^2 + D_p\left[\frac{(2n-1)\pi}{L_Y'}\right]^2 + D_p\left[\frac{(2k-1)\pi}{L_Z'}\right]^2 + \frac{1}{\tau_p}} \times (-1)^{m+1} \quad (2\text{-}21)$$
$$\times \left[\frac{L_Y' L_Z'}{L_1}\frac{2(2m-1)}{(2n-1)(2k-1)\pi} + \frac{L_1 L_Z'}{L_Y'}\frac{8(2n-1)}{(2m-1)(2k-1)\pi} + \frac{L_1 L_Y'}{L_Z'}\frac{8(2k-1)}{(2m-1)(2n-1)\pi}\right]$$

where α is the absorption coefficient, Φ_o is the incident photon flux density, and D_p and τ_p is diffusion constant and lifetime for holes, respectively. The frequency response is mainly determined by the term which involves *f*. It reveals that the bandwidth is proportional to the sub-term:

$$\left\{D_p\left[\frac{(2m-1)\pi}{2L_1}\right]^2 + D_p\left[\frac{(2n-1)\pi}{L_Y'}\right]^2 + D_p\left[\frac{(2k-1)\pi}{L_Z'}\right]^2 + \frac{1}{\tau_p}\right\} \quad (2\text{-}22)$$

Since D_p, L_1, and τ_p are restricted by a standard technology, the bandwidth can be improved by adopting shorter lengths (L_Y and L_Z) of the rectangular shape to get smaller L_Y' and L_Z'. In a similar way, the electron diffusion current of the P-well neutral region can be obtained.

Furthermore, the drift current, proportional to the area of the depletion region A_{dr}, is given by [7]:

$$I_{dr} = \int A_{dr} q\alpha\Phi_o e^{-\alpha x} dx \quad (2\text{-}23)$$

2.3.3 Simulation Results

Based on physical parameters of a standard 0.18-μm CMOS technology, the simulated results of photocurrent as functions of operating frequency is shown in Figure 2-8. The calculated responsivity of strip-line detector is about 62 mA/W, while its -3 dB bandwidth is about 2.1 GHz. In spite of the smaller responsivity, the responsivity bandwidth product (RBW) is much better than the conventional N-well/P-substrate junction photodetector.

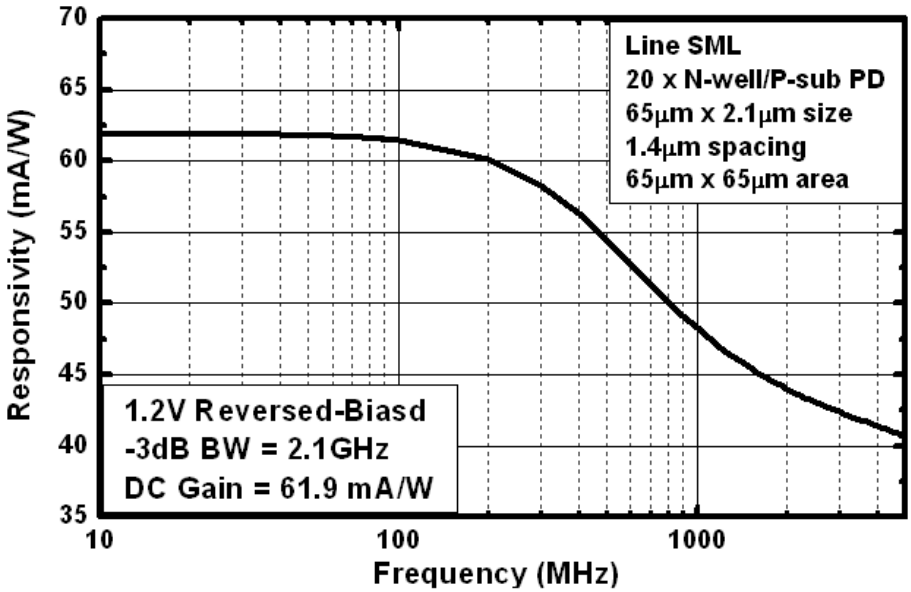


Figure 2-8 SML detector simulated results.

2.4 Lateral PIN Detectors

To circumvent the mentioned issues of conventional N-well/P-substrate SML detector without resort to a sophisticated equalizer, we proposes a novel lateral PIN detector, emulated by a P^+diffusion/P^-well/N^+diffusion interleaved architecture.

2.4.1 Basic Concepts

Figure 2-9 illustrates the top view and cross-sectional view of the detector. The detector is fabricated in the active region, surrounded by N-well and deep N-well (DNW). The top of the sensing region is striped of salicide and passivation layer to disconnect P+/P-/N+ regions and alleviate light reflection. Compared to conventional N-well/P-substrate junction, the electron-hole pairs are mainly generated in the laterally depleted regions. On the other hand, the well is tied to the highest voltage, which protects the PIN diode from substrate noise coupling.

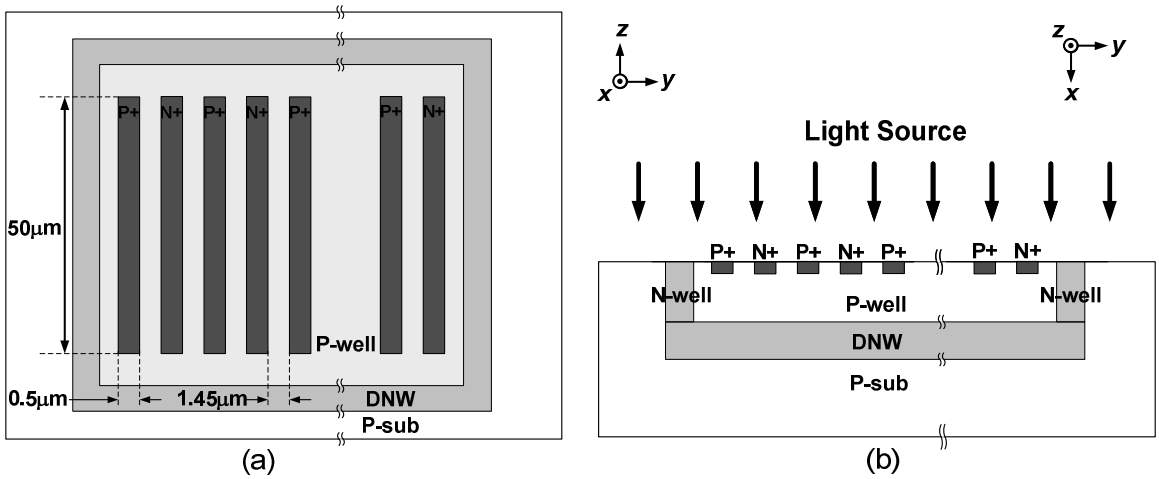


Figure 2-9 (a) top view, and (b) cross view of a PIN detector.

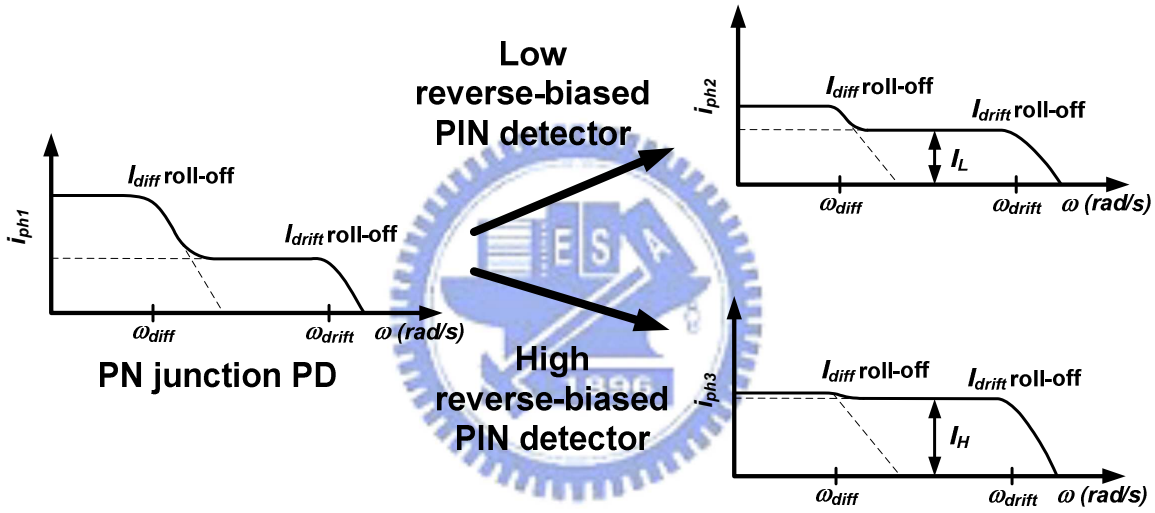


Figure 2-10 Frequency response of a PIN detector's photocurrent.

Besides, there are still wide depletion region between P-well and DNW (or N-well), since the doping of these two neutral regions is not as heavy as that of P^+diffusion or N^+diffusion. Thus, the fast drift current generated by P-well/DNW (or P-well/N-well) depletion can also be collected to increase the responsivity of this PIN detector.

The photocurrent component of a PIN detector is shown in Figure 2-10. The photocurrent (i_{ph1}) of P-substrate/N-well junction PD exhibits a large diffusion current generated by P-substrate so that its bandwidth is low. By employing the DNW and N-well, this PIN detector gets rid off the slow diffusion current. Thus, the percentage of fast drift current of the

total PIN's photocurrent (i_{ph2}) increases. In addition, if a higher reverse-biased voltage is applied, then I_{drift} becomes more and I_{diff} goes less owing to the fully-depleted P-well region. Therefore, the high-speed PD with photocurrent i_{ph3} is achieved.

2.4.2 Analysis of PIN detector

To comply with the diameter of the multi-mode fiber, the dimension of the photodetector is only 50 μm × 50 μm (*A*), consisting of 13 P-I-N fingers (see Figure 2-9). In this experimental prototype, the P+ and N+ stripes are 1.45-μm wide (*w*), separated by a 0.5-μm wide P-well region (*d*). Thus a reasonable low (~ 2 to 6 V) reverse biased voltage (V_R) is sufficient to deplete the P-well region of the photodetector for a high speed operation. The proposed architecture is expected to provide a higher responsivity by enlarging the P- region and operated in the avalanche mode. In this case, a higher reverse-biased voltage can be applied.

The photocurrent of the proposed PIN detector can be expressed as:

$$I_{ph} = I_p + I_n + I_{dr} \tag{2-24}$$

where I_p and I_n are the hole and electron diffusion current of the neutral regions, respectively, and I_{dr} is the drift current of the depletion regions.

Also, the hole-carrier diffusion current can be solved as [8]:

$$I_p = \sum_{m=1}^{\infty}\sum_{n=1}^{\infty} \frac{Aq\alpha\Phi_o D_p}{2(w+d)} \times \frac{1}{j2\pi f + D_p\left[\frac{(2m-1)\pi}{2l'}\right]^2 + D_p\left[\frac{(2n-1)\pi}{w'}\right]^2 + \frac{1}{\tau_p}} \times \frac{(2m-1)\pi(-1)^{m+1}e^{-\alpha l'} + 2\alpha l'}{(\alpha l')^2 + \left[\frac{(2m-1)\pi}{2}\right]^2} \times \frac{4}{(2n-1)\pi} \times (-1)^{m+1}\left[\frac{w'(2m-1)}{l'(2n-1)} + \frac{4l'(2n-1)}{w'(2m-1)}\right] \tag{2-25}$$

where α is the absorption coefficient, Φ_o is the incident photon flux density, and D_p and τ_p is diffusion constant and lifetime for holes, respectively. The frequency response is mainly determined by the term which involves *f*. It reveals that the bandwidth is proportional to the

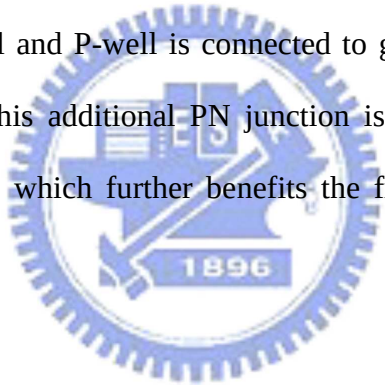
sub-term

$$\left\{ D_p \left[\frac{(2m-1)\pi}{2l'} \right]^2 + D_p \left[\frac{(2n-1)\pi}{w'} \right]^2 + \frac{1}{\tau_p} \right\} \quad (2\text{-}26)$$

Since D_p, l', and τ_p are restricted by a standard technology, the bandwidth can be improved by adopting narrower stripe width (w) to get smaller w'. In a similar way, the electron diffusion current of the P-well neutral region can be obtained. Furthermore, the drift current, proportional to the area of the depletion region A_{dr}, is given by:

$$I_{dr} = \int A_{dr} q\alpha\Phi_o e^{-\alpha x} dx \quad (2\text{-}27)$$

It is worth to mention that the total photocurrent of the device is also contributed by the P-well/DNW junction below the lateral PIN photodiodes, since DNW is connected with N+diffusion to a high potential and P-well is connected to ground, which results in another reverse-biased PN junction. This additional PN junction isolates the substrate current and increases the depletion region, which further benefits the frequency response of the entire photodetector.



2.4.3 Simulation Results

Based on physical parameters of a standard 0.18-μm CMOS technology, the calculated responsivity as functions of operating frequency is shown in Figure 2-11. For a PIN detector with DNW, the 3-dB bandwidth can be greatly promoted to 1.2 GHz and 1.9 GHz for V_R = 2 V and 6 V, respectively. The results point out that the proposed PIN detector with DNW can effectively eliminate the slow diffusion response resulting from the P-substrate current. In spite of the smaller responsivity, the responsivity bandwidth product (RBW) is much better than that of a PIN detector without DNW.

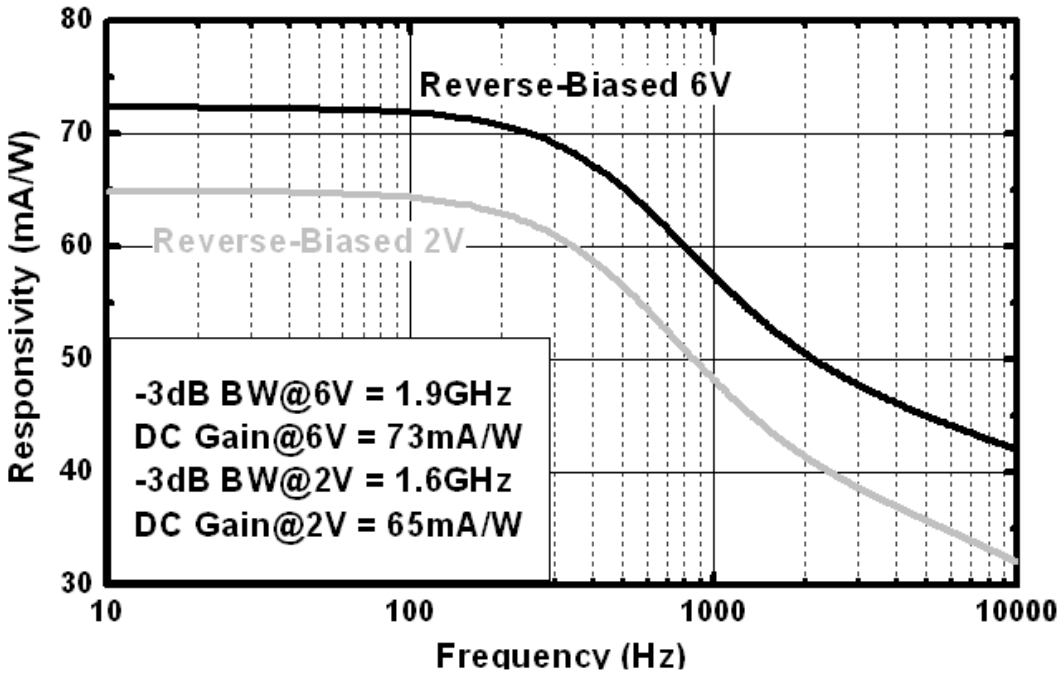


Figure 2-11 Simulated results of a PIN PD.

2.5 Fully CMOS Optical Receiver

In optical communication circuit design, the cost is always the major issue; therefore CMOS is suitable for optical interconnection owing to the advantages of high-density and cost-effective. They can be used in short distance and high volume communication systems.

2.5.1 Optical Communication Architecture

A computing system based on high density optical link is shown in Figure 2-12. In this scenario, broad band data bus are bridged through optical links, such as the host interface between the CPU and chipset, memory data bus, and I/O interface, etc.

The goal of an optical communication system is to carry large volumes of data. Figure 2-13 denotes a typical optical communication system. Digital data is amplified, and then drives the laser source at the transmitter end. In order to have a good illuminated optical light, the laser's

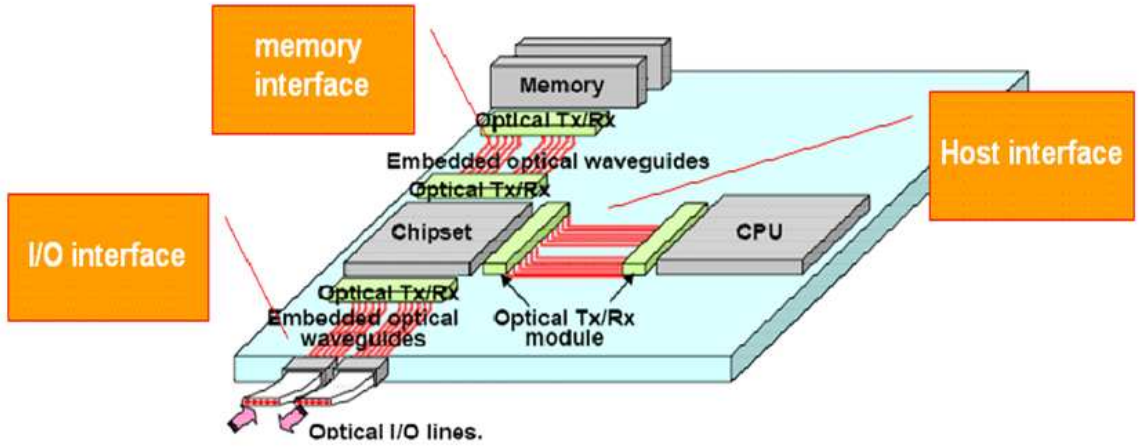


Figure 2-12 High density optical link for next generation CPU.

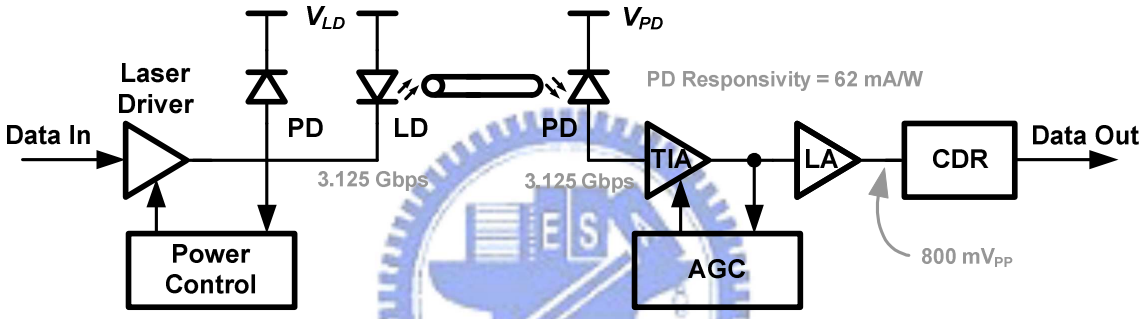


Figure 2-13 Optical transceiver architecture.

extinction-ratio (ER) will be constant, not be altered by PVT variation, the power control is needed. At the receiver end, a photodetector and a TIA translate the optical signal to a voltage data. Limiting amplifier (LA) serves as an amplitude control function to keep a constant output level, which helps the following CDR to extract the correct timing sequence.

2.5.2 Specifications of Optical Receiver

Before designing a circuit, some systematic requirements should be described. In this sub-section, some specifications of receiver front-end will be listed. Since noise, sensitivity, gain, and bandwidth of the receiver front-end dominate the performance of the overall receiver, we focus the design issues on these aspects.

Sensitivity and Noise

In the receiver, one of the most important requirements is its sensitivity. The sensitivity of the receiver is the minimal input power of light for a given bit error rate (BER), 10^{-12} for system required. The minimal accepted input power and the corresponding sensitivity can be described as:

$$P_{\min}\left(mW_{pp}\right)=\frac{SNR\cdot\sqrt{\overline{I_{n,total}^2}}}{R} \tag{2-28}$$

$$Sensitivity(dBm)=10\cdot\log\frac{P_{\min}\left(mW_{pp}\right)}{2} \tag{2-29}$$

where P_{min} is the minimum input power, R is the responsivity of a photodetector, SNR indicates a ratio of signal (peak-to-peak signal swing) to noise (root-mean-square value, which can be obtained by integrating the noise across the entire bandwidth), and $\overline{I_{n,total}^2}$ denotes the total input-referred noise current of the receiver. It can be described as:

$$\overline{I_{n,total}^2}=\overline{I_{n,PD}^2}+\overline{I_{n,TIA}^2}+\frac{\overline{V_{n,LA}^2}}{R_T^2} \tag{2-30}$$

where R_T denotes the gain of the transimpedance amplifier. (2-30) includes the noise contributed from the photodetector, TIA, and LA divided by TIA transimpedance. Usually, TIA dictates this noise performance.

The Vertical-Cavity Surface-Emitting Laser (VCSEL) is a type of semiconductor laser diode and can generate the 850-nm wavelength for CMOS photodetectors. Typically, the maximum output power of VCSEL is about **0 mW** or **0 dBm**. Assume that the insertion loss for the short-reach communication system from transmitter end to receiver end is **6dB**. The responsivity of the CMOS photodetectors (SML and PIN) is **62 mA/W**. Thus, the sensitivity of the short-reach optical receiver and transimpedance amplifier will be better than **-6 dBm** and **31 μA_{pp}**, respectively. In addition, the input-referred noise of this receiver with BER less than 10^{-12} should be smaller than **2.2 μA_{rms}**.

Besides, the sensitivity of limiting amplifier with BER less than 10^{-12} is generally about **5 mV_{pp}**. Therefore, the input-referred noise of transimpedance amplifier and limiting amplifier should be smaller than about **1.84 μA_{pp}**. and **0.36 mV_{pp}**, respectively.

Gain

Divide the receiver gain into three part, transimpedance gain, linear voltage gain and slicer voltage gain of limiting amplifier. In order to achieve the output swing of 800 mV_{pp}, the conversion gain of TIA and limiting amplifier must be mare than **25.8 kΩ** (or **88 dBΩ**). And the transimpedance gain and linear voltage gain of limiting amplifier can be allotted **60 dBΩ** and **28 dB** for noise performance and simplification consideration. However, to have a sharper switching-logic output waveform of limiting amplifier, the additional slicer gain of **16 dB** is considered.

Bandwidth

The overall receiver is designed to receive a data rate of 3.125 GHz. To avoid intersymbol interference (ISI) and must meet the sensitivity and noise requirement, the bandwidth of the overall receiver should be **2.2 GHz**. Since the bandwidth of the overall receiver is determined mostly by the transimpedance amplifier. The TIA bandwidth is typically chosen to be equal to 0.7 times the bit rate under the compromise between noise and ISI. Hence, the bandwidth of the limiting amplifier (linear part) is typically designed **3.125 GHz** to cause no ISI. Also, the bandwidth of the slicer part will be more than 3.125 GHz.

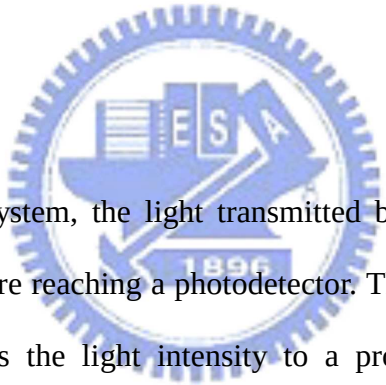
Table 2-3 lists the summary of the short-reach optical receiver specifications. Because the performances (responsivity of 73 mA/W and bandwidth of 1.9 GHz) of PIN detector is better than SML detector, the optical receiver can also be adopted while the PIN detector to receiver the 850-nm wavelength optical light.

Table 2-3 The specifications of the OEIC with SML detector.

Specifications	*SML PD*	*Receiver*	*TIA*	*LA (Linear)*	*LA (Slicer)*
Gain	62mA/W	104dB	60dB	28dB	16dB
Bandwidth(GHz)	1.6	2.2	2.2	3.2	> 3.2
Sensitivity Level	<-6dBm	$<31\mu A_{pp}$	$<26\mu A_{pp}$	$5mV_{pp}$	N.A.
Noise	N.A.	$<2.2\mu A_{rms}$	$<1.9\mu A_{rms}$	$<0.3mV_{rms}$	N.A.

Chapter 3

Transimpedance Amplifier



In optical communication system, the light transmitted by laser diode travels through a fiber and experiences loss before reaching a photodetector. The photodetector then senses the power of light and transforms the light intensity to a proportional photocurrent. At the receiver front-end, transimpedance amplifier (TIA) is an interface that converts the receiving photocurrent to electrical voltage.

In this chapter, design consideration in TIA will be introduced first. Then three typical types of preamplifier circuits are introduced and compared in section 3.2. Also, the advantages and disadvantages of two different circuit topologies (common-gate and common-source topology) will be discussed in section 3.2, too. Section 3.3 introduces the RGC-TIA chosen for meet the trade-off between large input capacitance and transimpedance gain of the TIA. And the noise analysis is also described in section3.3. Finally, the post-layout simulated results in the slow-slow (SS) corner will be shown.

3.1 Design Considerations

The transimpedance amplifier (TIA) is a critical block of a fiber-optic receiver. Its gain, input overload current, noise performance, bandwidth and group delay variation largely determine the overall sensitivity and the data rate of the optical link. Here we discuss the following design considerations.

Gain

The gain of TIA, or so-called transimpedance, is defined as the output voltage change per input current change. It must be large enough to overcome the noise of subsequent stage such as limiting amplifier or buffer. Besides, the gain will influence the sensitivity required for the following stage limiting amplifier indirectly. Typically, the transimpedance for 2.5 Gbps data rate is about 2k Ω to 4k Ω, and for 10 Gbps about 500 Ω to 2k Ω [10].

Input Overload Current

The input overload current is largest input current for TIA without distortions causing BER go above the level of 10^{-12}. It defines the upper end of the TIA's dynamic range. In SONET OC-48, the minimum required overload current is 1.6 mA_{pp}. The problem of overload characteristics enforces a gain control circuit in the TIAs [10].

Input-Referred Noise Current

The input-referred noise current of receiver front-end determines the minimum input current that yields BER be smaller than 10^{-12}. As described in section 2.3, the TIA dictates this requirement. Typically, the input-referred noise current of TIAs for 2.5 Gbps data rate is 380 nA_{rms} and for 10 Gbps is 1400 nA_{rms}.

Bandwidth

In view of noise consideration, the bandwidth of TIA must be minimized so as to reduce the total integrated input-referred noise current. On the other hand, in view of intersymbol interference (ISI) in random data, the bandwidth of TIA must be maximized. The trade-off between noise and ISI makes a compromise to a bandwidth of 0.7 times the data rate. In OC-48design and OC-192, a 1.75 GHz and 7 GHz bandwidth is required at least, respectively.

Group Delay Variation

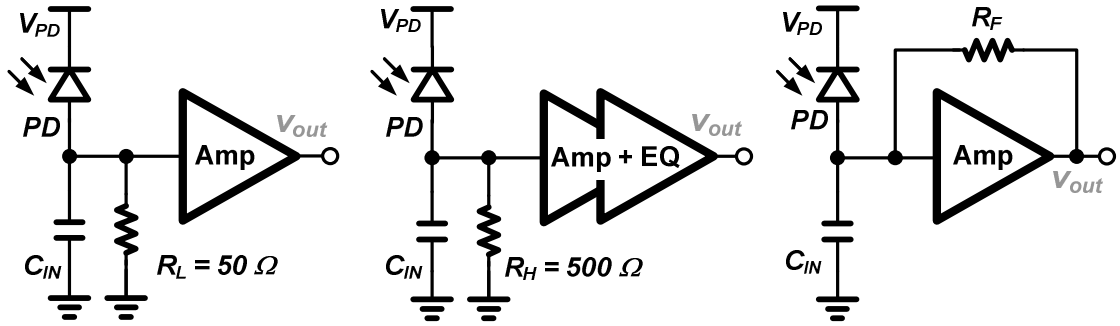
The group delay, τ, is related to the phase, Φ, as $\tau(\omega) = -d\Phi/d\omega$. The group delay variation as well as bandwidth is important parameter determining the mount of ISI and jitter introduced by the TIA. Typical values for group delay variation, $\Delta\tau$, are less than $\pm$10% of the bit time. The $\Delta\tau$ for 2.5 Gbps and 10 Gbps is about $\pm$40 ps and $\pm$10 ps, respectively.

3.2 Preamplifier Architecture

Typically, the structure of preamplifier can be classified into three categories which are low-impedance amplifier, high-impedance amplifier and transimpedance amplifier. Here we discuss those preamplifiers on structures as well as their advantages and disadvantages in the following.

3.2.1 Architecture Comparison

Figure 3-1(a) shows a typical low-impedance preamplifier. Main advantages of the structure are (i) the preamplifier is easy to be implemented since commercially available 50Ω RF amplifier can be used; (ii) the bandwidth is large due to low R_LC_T time constant, (iii) it has wide input dynamic range when the signal to the preamplifier input node is at very low level.



(a) (b) (c)

Figure 3-1 (a) low-impedance, (b) high-impedance and (c) transimpedance preamplifier architecture.

However, the input-referred noise is high due to a low resistor at the input node.

On the contrary, the structure of high-impedance preamplifier is shown in Figure 3-1(b). Compared with low-impedance preamplifier, the equivalent input-referred noise is low due to high resistance. However, the price paid for increasing input resistance is that the bandwidth is reduced. An equalizer or other circuit is commonly used to compensate the frequency response which makes the preamplifier design more complicated.

At last, the transimpedance preamplifier is shown in Figure 3-1(c). The preamplifier frequently employs the feedback technique to enhance the bandwidth and to enlarge the dynamic range. The bandwidth is enhanced by a factor of loop gain compared with that of high-impedance preamplifier with the same load resistance and input capacitance. Besides, the noise can be very low due to large feedback resistance. One problem to be care is the stability that comes with the feedback techniques.

Table 3-1 lists the comparison of the three preamplifiers. Make a comprehensive survey of the three structures, the transimpedance amplifier is suitable for fiber-optical applications.

In the transimpedance amplifier, it is desirable to achieve low noise, high transimpedance gain, and adequate bandwidth. These requirements usually conflict, requiring trade-offs to be made to suit a particular application. According to the core amplifier, transimpedance amplifier can be classified into two categories: common-source and common-gate structure.

Table 3-1 Comparison of three topologies of preamplifier.

	Bandwidth	***Dynamic Range***	***Noise***	***Design***
Low-impedance	Good	Good	High	Easy
High-impedance	Bad	Bas	Low	Difficult
Transimpedance	Good	Good	Low	Easy

3.2.2 Circuit Topology Comparison

TIA with Common-Source Amplifier

Figure 3-2 shows a typical transimpedance amplifier with common-source core amplifier. Its transimpedance gain, T_Z, and -3 dB bandwidth can be derived as:

$$T_Z = \left| \frac{v_{out}}{i_{in}} \right| \approx \frac{g_{m1} R_D R_F}{1 + g_{m1} R_{IN}} \approx R_F \tag{3-1}$$

$$\omega_{-3dB} \approx \frac{g_{m1} R_D}{2\pi R_F C_{IN}} \tag{3-2}$$

Since the gain is almost equal to the feedback resistance, a larger resistance can achieve a higher gain. However, (3-2) shows that larger feedback resistance will degrade the bandwidth. In order to enhance the bandwidth, the open loop gain should be as large as possible while ensuring the stability.

In view of noise, the input-referred noise current can be described as:

$$\overline{I_{n,in}^2} = \frac{4kT}{R_F} + \frac{1}{g_{m1}^{\ 2}} \left(\frac{4kT}{R_D} + 4kT\gamma g_{m1} \right) \left(\frac{1}{R_F^2} + \omega^2 C_{IN}^2 \right) + \frac{4kT\gamma}{g_{m1}^{\ 2} g_{m2}} \left(\frac{1}{R_D^2} + \omega^2 C_X^2 \right) \left(\omega^2 C_{IN}^2 + \frac{1}{R_F^2} \right) \tag{3-3}$$

To achieve low noise requirement, the transconductance of M_1 and the resistor R_F should be as large as possible. However, these requirements conflict with input capacitance, voltage headroom, and signal bandwidth individually. One should be care is that although the noise at

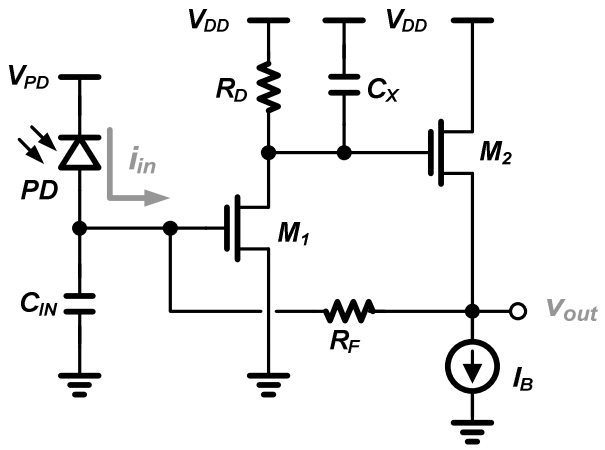


Figure 3-2 Architecture of common source feedback amplifier.

low frequency could be negligible, that at high frequency may become considerable. For CMOS TIAs, the primary factor that constrains the bandwidth and noise performance is the inherent parasitic capacitances introduced by photodetector. As a result, in conventional common-source topology, signal bandwidth has to be severely traded-off among transimpedance gain and noise performance.

TIA with Common-Gate Amplifier

The other generally used circuit structure is with the common-gate core amplifier as shown in Figure 3-3. Compared with common-source structure, the low input impedance renders the signal bandwidth almost insensitive to parasitic capacitances introduced by photodetector. The gain and bandwidth can be described as:

$$T_Z = \left| \frac{v_{out}}{i_{in}} \right| \approx \frac{g_{m2} R_{D1} R_{D2}}{1 + g_{m2} R_{D1} R_{D2} / R_F} \approx R_F \tag{3-4}$$

$$\omega_{-3dB} \approx \frac{g_{m1} g_{m2} R_{D1} R_{D2}}{2\pi C_{D1} R_F} \tag{3-5}$$

With the same gain, the common gate topology can achieve a higher bandwidth independent of feedback resistor R_F. An important drawback of common gate topologies is that they directly refer the noise current produced by the load to the input, which results in considerable

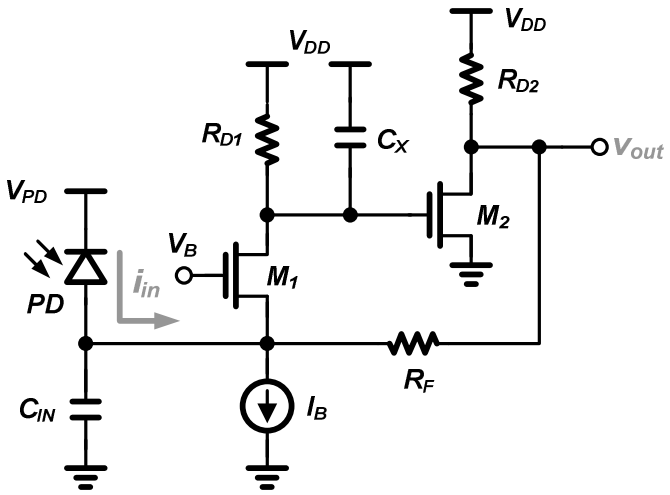


Figure 3-3 Architecture of common-gate feedback amplifier.

noise thus degrading the sensitivity. The noise current spectral density can be described as:

$$\overline{I_{n,in}^2} = \frac{4kT}{R_F} + \frac{4kT}{R_{D1}} + 4kT\gamma g_{mB} + \frac{4kT}{g_{m2}^2}\left(\frac{1}{R_F} + \frac{1}{R_{D2}} + \gamma g_{m2}\right)\left(\frac{1}{R_{D1}^2} + \omega^2 C_X^2\right) \qquad (3\text{-}6)$$

In order to reduce input-referred noise, the transconductance of M_1, the load resistor (R_{D1} and R_{D2}), feedback resistor (R_F) should be chosen large. However, the load resistors will have trade-offs with voltage headroom and signal bandwidth. Fortunately, a large feedback resistance can improve gain and noise performance at the same time while almost maintaining the signal bandwidth. On the contrary, the transconductance of current source I_B should be minimized. Under a given bias current, the gate drive voltage of I_B should be increased. In addition, the size of M_2 makes trade-off between low frequency noise and high frequency noise.

Table 3-2 Comparison of three preamplifiers.

	C_{PD} tolerance	Gain	Noise
Common-Gate TIA	Good	Good	High
Common-Source TIA	Bad	Good	Low

Table 3-2 summarizes the two topologies. Although noise produced by common-gate topology is not negligible even at low frequency, its low input impedance increase the tolerance of the large photodetector capacitance. The high gain and wide bandwidth feature makes it attractive in high speed circuit design. However, the sensitivity of fully CMOS optical receiver is very important. It uses the monolithic photodetector which has very small responsivity to sense the 850-nm optical light and generate photocurrent to the TIA. Thus, the common-source topology TIA will be chosen, and the RGC input stage is utilized to reduce the large photodetector capacitance effect.

3.3 Circuit Implementation

Figure 3-4 illustrates the circuit schematic of the TIA incorporating with SML detector. It consists of two identical TIAs (M_1, M_3, M_5 and M_2, M_4, M_6) in a fully differential configuration. To alleviate bandwidth degradation caused by the parasitic capacitance of the photodetector, a regulated cascode (RGC) input stage is adopted [11]. The current subtraction is performed in the second stage, which is a common source gain amplifier with shunt-shunt feedback. The voltage amplifier (M_3, R_3) and (M_4, R_4) provide a conversion gain of about 20 dB to enhance the bandwidth of the TIA, while the transimpedance gain is mainly provided by the resistors R_{f1} and R_{f2}. The slow photocurrent (i_{dark}) collected by the dark diode is then subtracted from that (i_{illu}) collected by the illuminated diode in the voltage domain.

Is the supply voltage of 1.8 V appropriate for this TIA? The responsivity of the SML detector (D_{illu} and D_{dark}) is higher if the reverse-bias voltage is larger. Based on the simulation, the reverse-bias voltage will be designed lager than 1.2 V so as to achieve better performance of SML detector. If V_{GS1} or V_{GS2} is about 0.7 V and the reverse-bias voltage of SML detector is1.2 V, then the gate voltage of M_1 or M_2 is lager than 1.8 V. Thus, the supply voltage (V_{DD}) of 3.3 V will be chosen for this TIA. However, to avoid the transistor breakdown, V_{GS} and V_{DS}

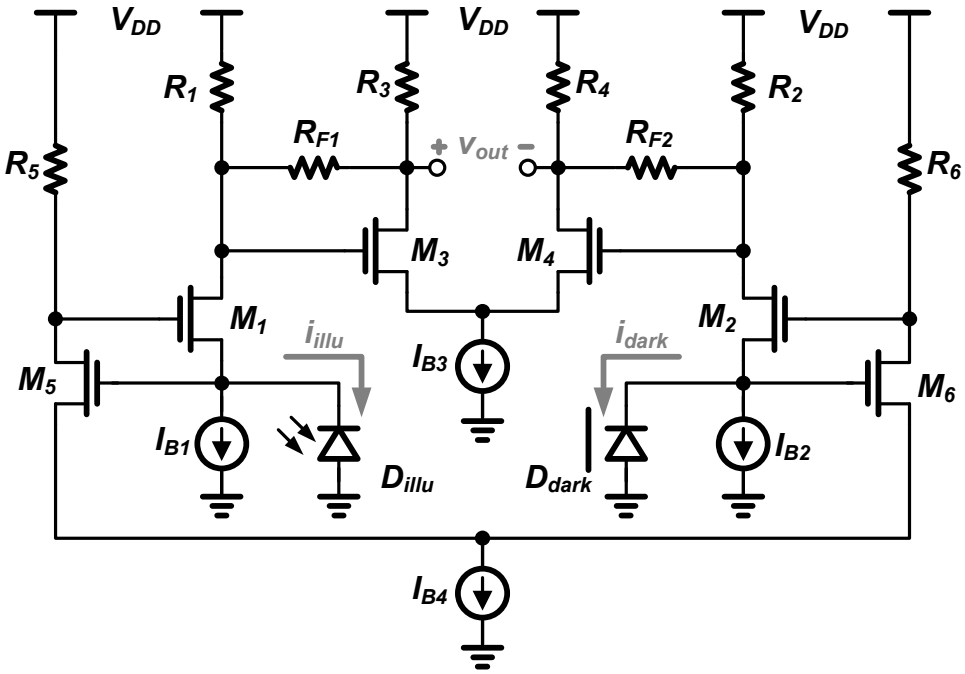


Figure 3-4 Fully transimpedance amplifier with SML detector.

of all transistors in this TIA will be designed smaller than 1.8 V.

Small-Signal Analysis

Figure 3-5 shows the equivalent half circuit of Figure 3-4, where C_X denotes the total capacitance at X to ground. The capacitance arises from C_{GD1}, C_{DB1}, C_{GS3} and the Miller effect of C_{GD3}. In addition, C_{IN} arises from C_{GDB1}, C_{DBB1}, C_{SB1}, C_{GS5}, the Miller effect of (C_{GD5} + C_{GS1}) and the photodetector capacitance. If the parasitic capacitance of the node Y is neglected for simplification, the transimpedance gain can be described as:

$$T_Z = \frac{v_{out1} - v_{out2}}{i_{illu} - i_{dark}} = \frac{v_{out}}{i_{in}} \tag{3-7}$$

$$\approx \frac{\left(R_{F1} - \frac{1}{g_{m3}}\right)}{\left[s^2 C_L C_X \frac{R_{F1}}{g_{m3}} + s\left(\frac{C_X}{g_{m3}} + \frac{C_L}{g_{m3}} + \frac{C_X}{g_{m3}}\frac{R_{F1}}{R_3} + \frac{C_L}{g_{m3}}\frac{R_{F1}}{R_1}\right) + 1\right] \times \left(s \times \frac{C_{IN}}{g_{m1} g_{m5} R_5} + 1\right)} \tag{3-8}$$

The above transfer function reveals that the transimpedance gain is about R_{F1} at relatively low frequencies if $R_{F1} >> (g_{m3})^{-1}$. Besides, the TIA circuit exhibits three poles: a pair of complex poles caused by the X node and output node, while the third pole located at the input node.

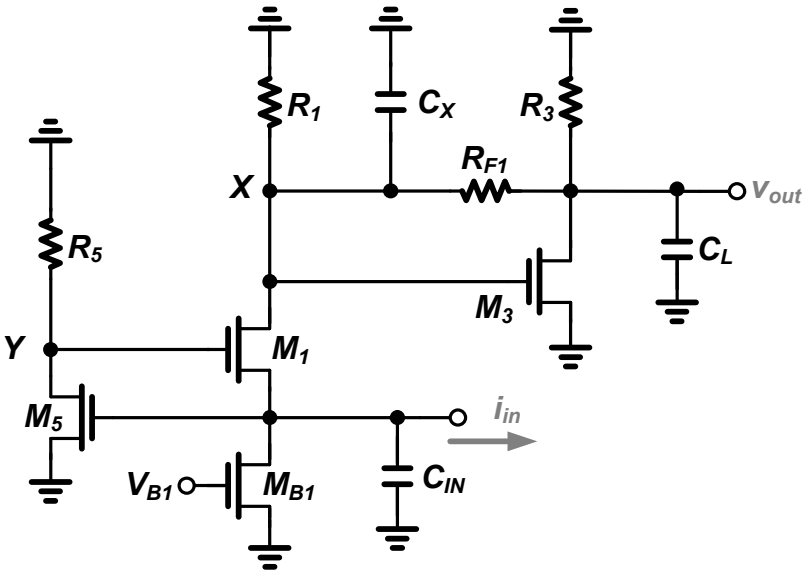
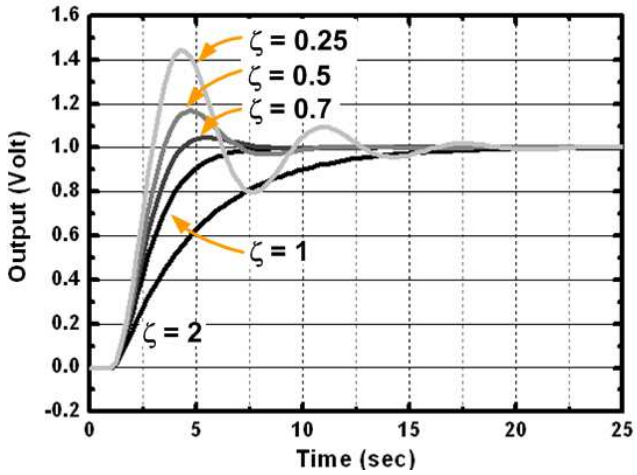
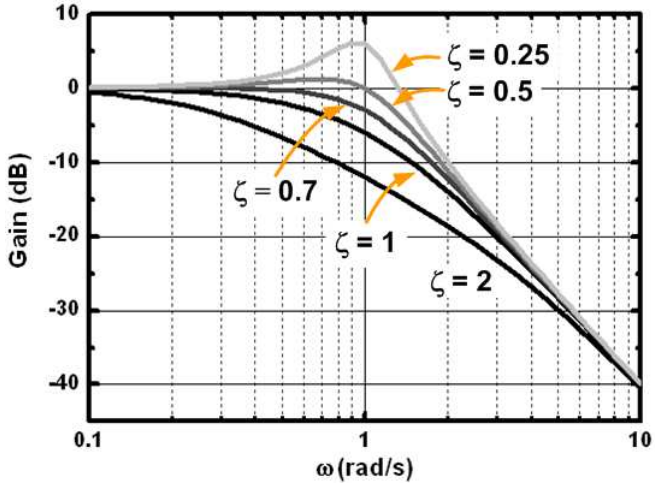


Figure 3-5 Equivalent half circuit of TIA in Figure 3-4.



(a)



(b)

Figure 3-6 (a) Step response and (b) frequency response for damping factor.

To analyze the pair of complex poles, we rewrite the function in familiar form used in control theory, $s^2 + 2\zeta\omega_n s + \omega_n^2$, where ζ is the damping ratio and ω_n is the natural frequency. That is,

$$s^2 + s\left(\frac{1}{C_L R_{F1}} + \frac{1}{C_X R_{F1}} + \frac{1}{R_3 C_L} + \frac{1}{R_1 C_X}\right) + \frac{g_{m3}}{C_L C_X R_{F1}} \tag{3-9}$$

where

$$\omega_n = \sqrt{\frac{g_{m3}}{C_L C_X R_{F1}}} \tag{3-10}$$

$$\zeta = \frac{1}{2\omega_n}\left(\frac{1}{C_L R_{F1}} + \frac{1}{C_X R_{F1}} + \frac{1}{R_3 C_L} + \frac{1}{R_1 C_X}\right) \tag{3-11}$$

The two poles are given by

$$s_{1,2} = \left(-\zeta \pm \sqrt{\zeta^2 - 1}\right)\omega_n \tag{3-12}$$

Thus, if $\zeta > 1$, both poles are real, the system is overdamped, and transient response contains two exponentials with time constants $(s_1)^{-1}$ and $(s_2)^{-1}$. On the other hand, if $0 < \zeta < 1$, the system is underdamped, the poles are complex and the response to an input current step $i_{in} = \Delta i \times u(t)$ is equal to

$$v_{out} = \left[1 - \frac{1}{\sqrt{1-\zeta^2}} e^{-\zeta\omega_n t} \sin\left(\sqrt{1-\zeta^2}\, t + \theta\right)\right]\left[\Delta i \times u(t)\right] \tag{3-13}$$

$$\theta = \sin^{-1}\sqrt{1-\zeta^2} \tag{3-14}$$

where v_{out} denotes the change in the output voltage. Illustrated in Figure 3-6, for several values of ζ and a constant ω_n, the step response exhibits severe ringing for $\zeta < 0.5$. Typically, ζ is usually chosen to be greater than $\sqrt{2}/2$ to avoid excessive ringing.

For a maximally-flat Butterworth response [12], let ζ be equal to $\sqrt{2}/2$. Then, we have

$$\left|\frac{1}{s^2 + 2\zeta\omega_n s + \omega_n^2}\right|_{s=j\omega_{3dB}} = \left|\frac{1}{-\omega_{3dB}^2 - j\sqrt{2}\omega_n\omega_{3dB} + \omega_n^2}\right| = \frac{\sqrt{2}}{2} \tag{3-15}$$

That is,

$$\left(\omega_n^2 - \omega_{3dB}^2\right)^2 + \left(\sqrt{2}\omega_n\omega_{3dB}\right)^2 = 2 \tag{3-16}$$

which yields

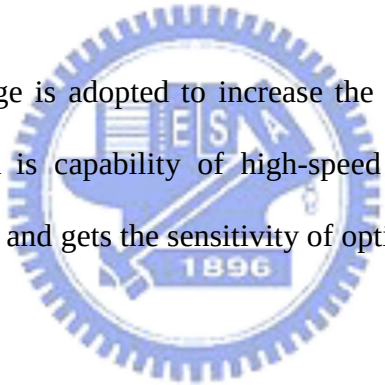
$$\omega_{-3dB} = \omega_n = \sqrt{\frac{g_{m3}}{C_L C_X R_{F1}}} \tag{3-17}$$

Compared with the third pole which is described as:

$$p_3 = \frac{g_{m1} g_{m5} R_5}{C_{IN}} \tag{3-18}$$

Generally, C_{IN} is about 1 pF or larger than C_X or C_L by 5 times. In order to eliminate the TIA's bandwidth degradation caused by the third pole, the product of g_{m5} and R_5 should be as large as possible. Thus, the transconductance of M_5 is about 8 m/V, and the resistance of R_5 is about 1k Ω and the -3 dB bandwidth of the differential amplifier (M_5, M_6, R_5, R_6 and I_{B4}) is about 2.8 GHz.

In short, the RGC input stage is adopted to increase the tolerance of large photodetector capacitance so that RGC-TIA is capability of high-speed operation. However, the RGC technique generates more noise and gets the sensitivity of optical receiver front-end worse.



Noise Analysis

The equivalent half circuit with noise source of Figure 3-5 is depicted in Figure 3-7. As introduced before, the accepted minimum input current is relative to the noise contributed by the TIA itself. The input referred noise current spectral density can be described as:

$$\begin{aligned}\overline{I_{n,in}^2} &= \overline{I_{n,R1}^2} + \overline{I_{n,MB1}^2} + \overline{I_{n,RF1}^2} + \frac{\overline{I_{n,M3}^2} + \overline{I_{n,R3}^2}}{g_{m3}^2}\left(\omega^2 C_X^2 + \frac{1}{R_{F1}^2}\right) + \frac{\overline{I_{n,M5}^2} + \overline{I_{n,R5}^2}}{g_{m5}^2}\left(\omega^2 C_{IN}^2\right) \\ &= \frac{4kT}{R_1} + 4kT\gamma g_{mB1} + \frac{4kT}{R_{F1}} + \frac{4kT(\gamma g_{m3} + \frac{1}{R_3})}{g_{m3}^2}\left(\omega^2 C_X^2 + \frac{1}{R_{F1}^2}\right) + \frac{4kT(\gamma g_{m5} + \frac{1}{R_5})}{g_{m5}^2}\left(\omega^2 C_{IN}^2\right)\end{aligned} \tag{3-19}$$

Although the proposed TIA with RGC input stage and shunt-shunt feedback to the second stage overcomes the trade-off among gain, bandwidth, and noise, the price paid is that the noise increases anyway especially at high frequency. To alleviate the first, second and last term in (3-19), g_{mB1} should be as small as possible, and g_{m5}, R_5 should be as large as possible.

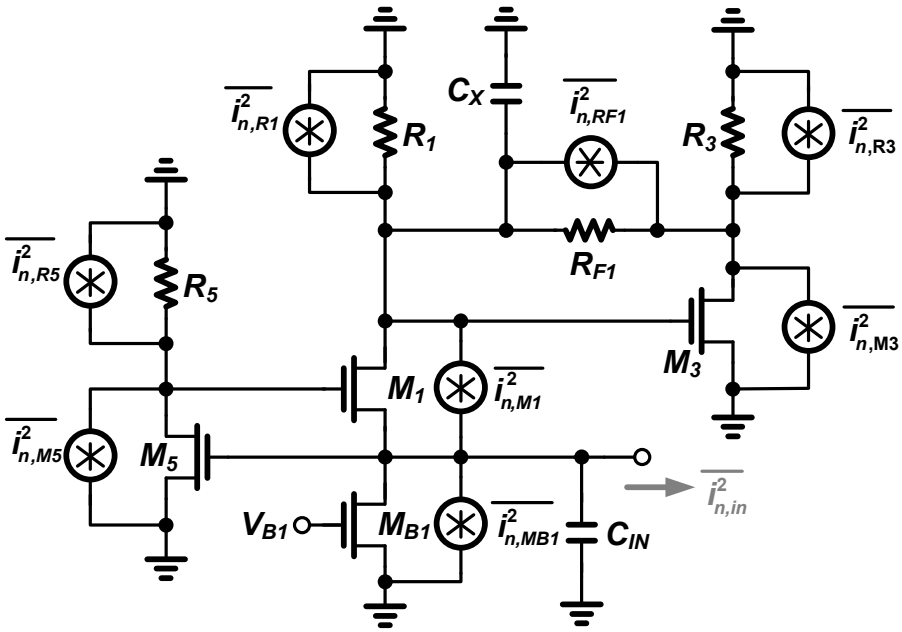


Figure 3-7 The equivalent half circuit with noise source.

Although the proposed TIA with RGC input stage and shunt-shunt feedback to the second stage overcomes the trade-off among gain, bandwidth, and noise, the price paid is that the input noise increases anyway especially at high frequency. To alleviate the first, second and last term above equation, g_{mB1} should be as small as possible, while g_{m5} and R_5 should be as large as possible.

To alleviate the noise contributes from the post gain stages, the TIA provides a conversion gain of about 60 dBΩ, and a -3dB bandwidth of about 2.9 GHz to compromise between input-referred noise and ISI. The post-layout simulation (by RCC extract) results are shown in Figure 3-8 to Figure 3-11. The parasitic capacitances of SML Detectors are both about 1.2 pF under the reverse-bias voltage 1.2V. The group delay variation is about ±15 ps from 10 MHz to 4 GHz. Besides, the input-referred noise of this TIA is about 2 μA_{rms} if the noise-bandwidth is about 3 GHz. From Figure 3-11, we can also see the TIA's gain is about 1k Ω, because it converts the current swing of 20 μA_{pp} to the voltage swing of 20 mV_{pp}.

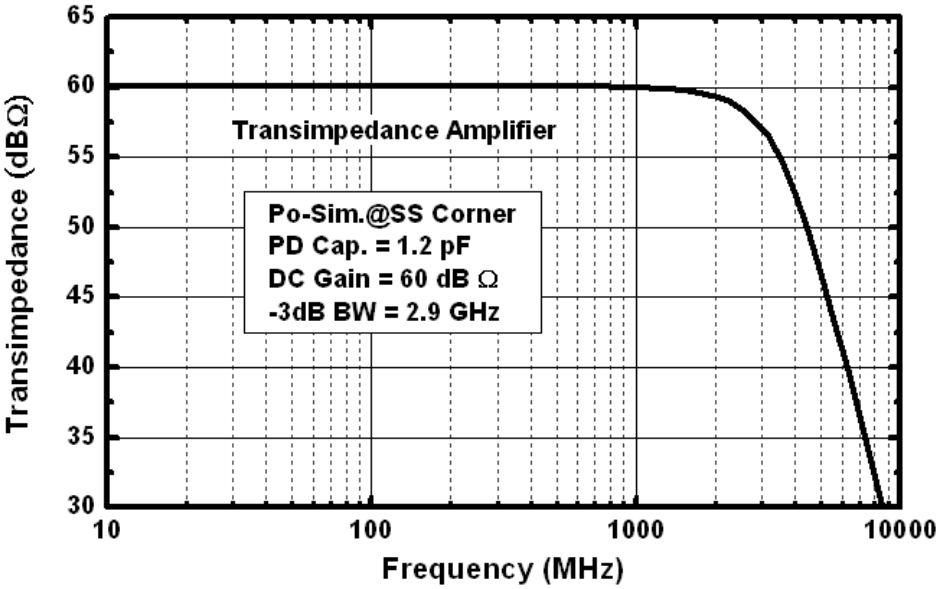


Figure 3-8 Magnitude response of TIA with SML detector.

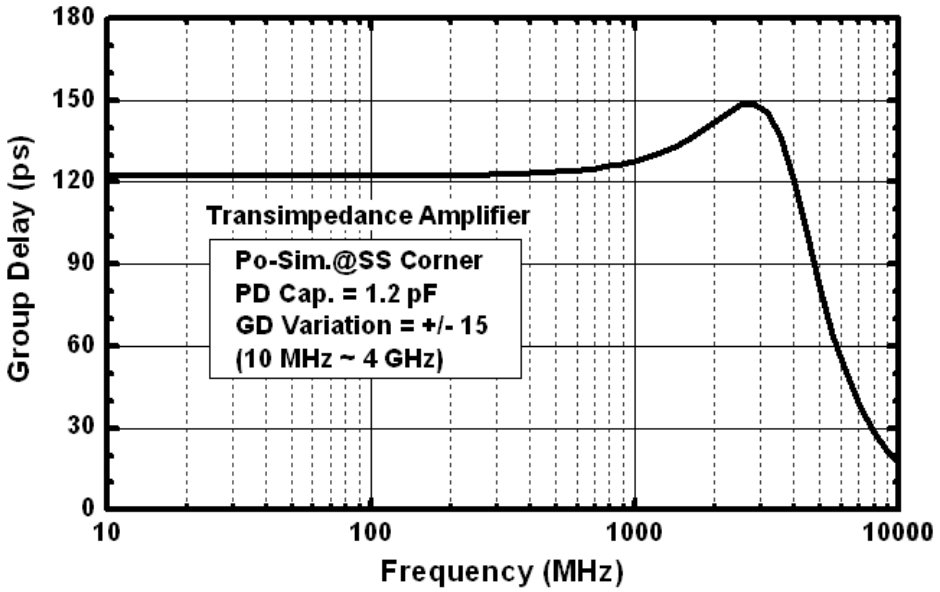


Figure 3-9 Group delay of TIA with SML detector.

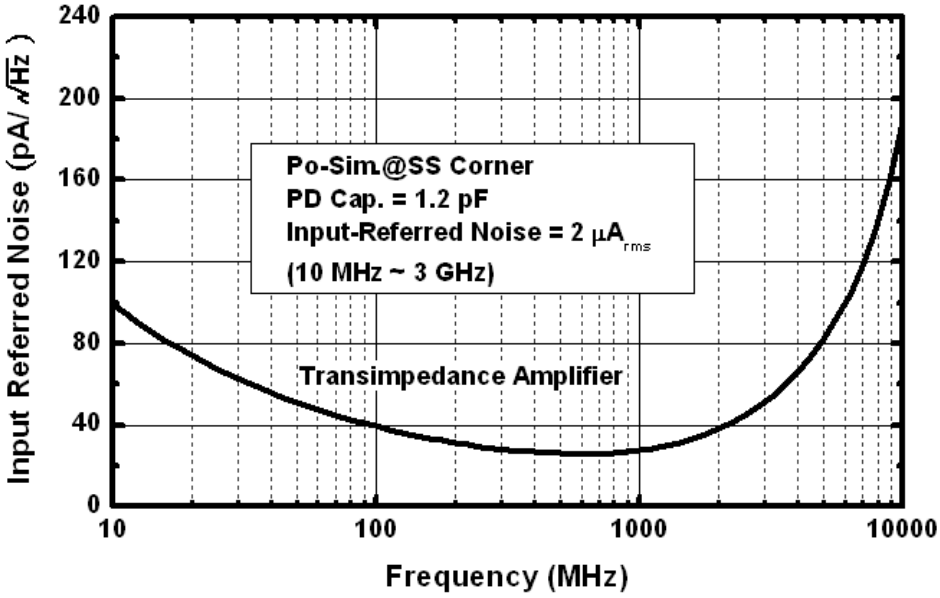


Figure 3-10 Input-referred noise of with SML detector.

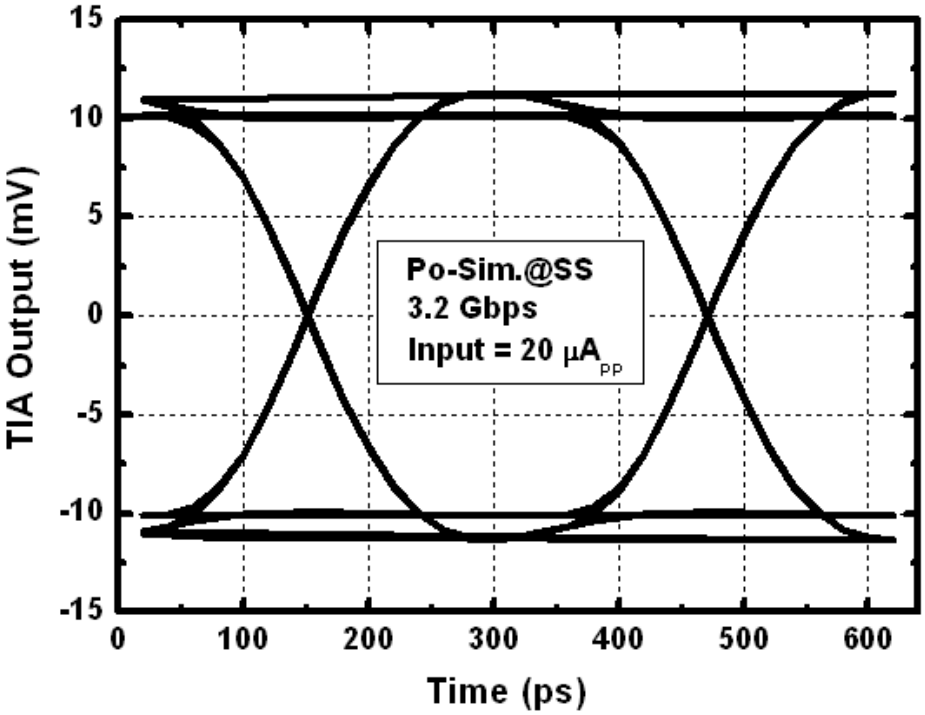


Figure 3-11 Eye diagram for 3.2 Gbps and 0.02 mA_{pp} input current.

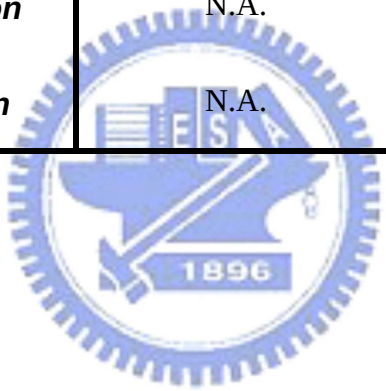
3.4 Summary

According to the post-layout simulated results, the transimpedance amplifier is able to operate for 3.2 Gbps data rate. It has a voltage gain of 60 dB Ω, -3 dBbandwidth of 2.9 GHz, group delay less than +/- 15 ps, input-referred noise about 2 μA_{rms}.

Table 3-3 lists the simulated results of the transimpedance amplifier with RGC input stage, and a resistor shunt-shunt feedback with common-source voltage amplifier.

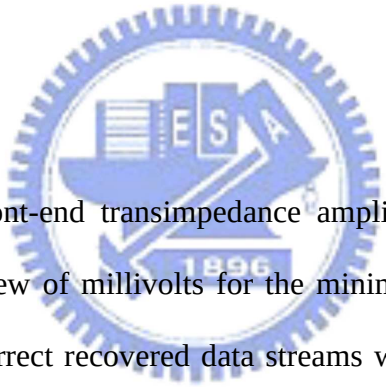
Table 3-3 Post-layout simulated results (RCC) of TIA.

	Specifications	***@ SS Corner***
Gain	60 dBΩ	60 dBΩ
- 3dB Bandwidth	2.2 GHz	2.9 GHz
Input-Referred Noise	1.84 μA_{rms}	2 μA_{rms}
Group Delay Variation	N.A.	+/- 15 ps
Power Consumption	N.A.	16 mW



Chapter 4

Limiting Amplifier



The signal produced by front-end transimpedance amplifier usually suffers from small amplitude, on the order of a few of millivolts for the minimum input current level. Such a weak signal will result in incorrect recovered data streams while it is received by clock and data recovery (CDR) circuit. Therefore, an additional gain boosting stage that boosts the signal swing to logical level is necessary. Post limiting amplifier is approach that are widely used in communication systems.

In this chapter, limiting amplifier will be discussed. That includes limiting amplifier's specifications, architectures, analysis of the stage number and circuit implementation.

4.1 Design Considerations

Gain

The gain of limiting amplifier is defined as the output voltage change per input voltage

change. A typical limiting amplifier has a gain of around for 30 dB to 50 dB. In optical communication system, limiting amplifier provides the gain to boost the TIA's output signal to logical level for CDR followed by. Thus, a TIA with high transimpedance gain helps to relax the gain requirement for the limiting amplifier.

Bandwidth

To reduce the ISI in random data, the limiting amplifier bandwidth is often made much larger than the desired receiver bandwidth. As a rule of thumb, the limiting amplifier -3dB bandwidth is chosen around 1.0 or 1.2 times the data rate, nearby twice the recommended receiver bandwidth. For example, for 2.5 Gbps and 10 Gbps data rate, a limiting amplifier -3dB bandwidth should be 2.5 GHz to 3GHz and 10 GHz to 12 GHz, respectively.

Input Offset Voltage

The limiting amplifier usually consists of several cascading gain cell stages. An offset voltage, caused by the non-ideal terms such as devices mismatch, V_t mismatch, and etc., will be amplified by the rear gain cells. It may cause incorrect data regeneration when the input signal is small. In other words, it may cause pulse-width distortion and decrease input sensitivity. Figure 4-1 shows the comparison of limiting amplifier output waveform with and without offset voltage.

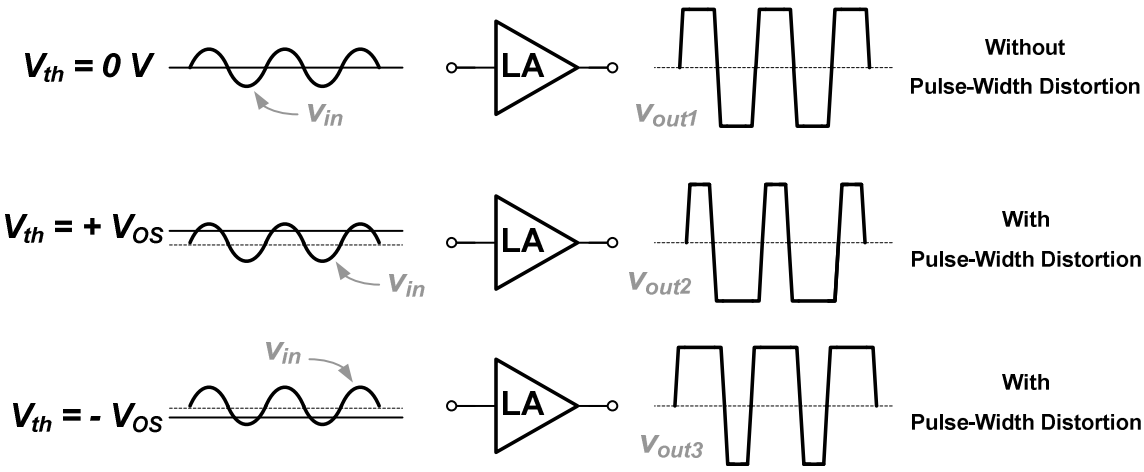


Figure 4-1 LA output waveform with and without offset voltage.

AM-to-PM Conversion

A limiting amplifier converts the input small signal to the output logic level and is a non-linear system. If the amplitude of input signal is not constant, then it will result in phase disturbance or so-called jitter in output signal of limiting amplifier. Typically, the delay variation resulted from AM-to-PM conversion will be less than ±10% of the bit time. That is about ±40 ps and ±10 ps for 2.5 Gbps and 10 Gbps, respectively.

4.2 Limiting Amplifier Architecture

4.2.1 Architecture Comparison

Typically, the limiting amplifier usually consists of several fully differential wide-band stages. According to the variety of cascading gain cells, limiting amplifiers can be classified into following four categories.

Identical Linear Amplifiers [12]-[14]

For limiting amplifier, that identical cascaded gain cell is a solution to solve the trade-offs between gain, bandwidth, and power consumption. For simplification, a limiting amplifier cascading identical gain cells (Figure 4-2(a)) is commonly used.

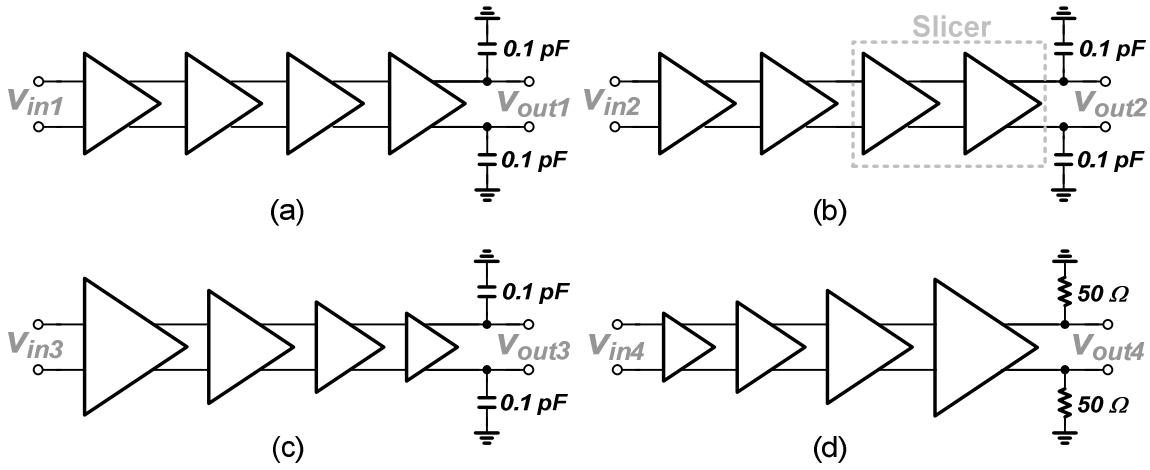


Figure 4-2 Limiting amplifier output with and without offset voltage.

Linear Amplifiers + Slicers [15]

In the limiting amplifier the signal can be seen as small-signal operation in the front several stages; whereas large-signal operation in the later stages. In other words, the later stages typically sense sufficiently large input swings, thereby experiencing switching and operating in the large-signal mode. Therefore, the stage's rising time and falling only depend on its output RC time constant. As shown in Figure 4-5(b), the slicer with low impedance is utilized to accelerate voltage switch and balance rising and falling time at high voltage level.

Inverse Scaling Technique [16]

As shown in Figure 4-5(c), to drive a small on-chip load, the cascaded amplifier can be inverse scaling. The input capacitance is usually lager than that of output. By inverse scaling technique, the bandwidth due to output node will be improved and so as limiting amplifier.

Tapered Buffer [17]

If an amplifier is to deliver signals to 50 W loads, then it must employ high currents and large output transistors in the last stage. As illustrated in Figure 4-5(d), the cascade must be tapered in device dimension and bias current from the first to the last so as to maintain a wideband while delivering high output current.

4.2.2 Analysis of Stage Number

Conventional post limiting amplifier is comprised of identical cascaded gain cells. Assuming each gain cell can be approximated by a two-pole amplifier, it can be described as:

$$A(s) = \frac{A_S \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{4-1}$$

where A_S is the DC gain of single stage.

For a given limiting amplifier with total gain of A_T and -3dB bandwidth of ω_T, then it will be implemented by cascading N-stage, identical, two-pole gain cells with ζ of $\sqrt{2}/2$ for maximally-flat bandwidth. Then, the gain (A_S), -3dB bandwidth (ω_S) and unity-gain bandwidth of single gain cell can be derived as:

$$A_S = A_T^{1/N} \tag{4-2}$$

$$\omega_S = \left(2^{1/N} - 1\right)^{-1/4} \times \omega_T \tag{4-3}$$

$$\omega_U = \left(2^{1/N} - 1\right)^{-1/4} \times \omega_T \times \left(A_T{}^{2/N} - 1\right)^{1/4} \tag{4-4}$$

The single stage gain can be reduced along with the increasing of the number of gain stages, while the -3 dB bandwidth of each gain cell should be increased accordingly. When the number of stage is increasing, it turns out that the gain bandwidth product can be relaxed. But it would lead to a higher input-referred noise if the conversion gain of gain cell is too small.

Besides, if the current consumption in each stage is proportional to the square of its unity gain bandwidth, the total power dissipation will also be increased for more stages in cascade.

$$Power \propto N \cdot \omega_U^2 \propto N \cdot \omega_T^2 \cdot \left(2^{1/N} - 1\right)^{-1/2} \cdot \left(A_T{}^{2/N} - 1\right)^{1/2} \tag{4-5}$$

Figure 4-3 shows the case when the linear gain contributed by the front several stage of LA is 25 (or 28dB) and bandwidth is 3.2 GHz. Also, all the parameters are normalized in Figure 4-3. It can be intuitively understood that as the number of cascaded stage increases, the gain provided by each gain stage decreases. In the meantime, the bandwidth provided by each gain stage increases. In addition, the power consumption increases proportionally when stage number is larger than three. Take power dissipation into consideration, we are forced to make a compromise between speed and power consumption. Thus, a 2-stage or 3-stage linear amplifier in front of LA has lower power dissipation and its unity-gain bandwidth is also feasible in 0.18-μm CMOS technology.

At last, a 3-stage amplifier with lower gain in each stage is chosen in this design rather than a 2-stage amplifier because the Miller effect should not be ignored.

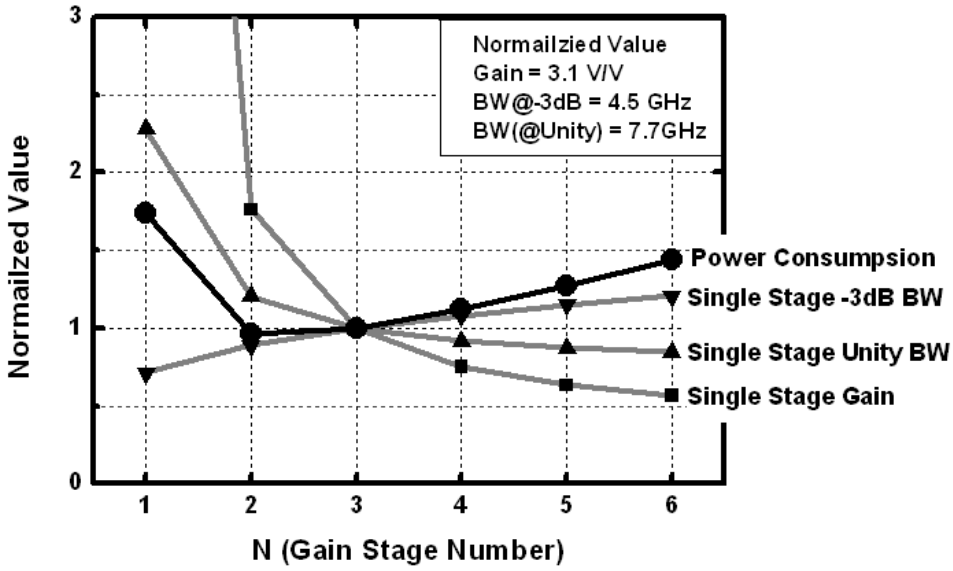


Figure 4-3 Normalized LA's power consumption versus the number of stages.

4.3 Limiting Amplifier Implementation

The architecture of post limiting amplifier is shown in Figure 4-4. Excluding the DC offset cancellation network, the limiting amplifier is composed of a subtractor (SUB) in the front and 5 gain stages consisting of 3 stages in linear amplified and 2 stages in slicer amplified. The subtractor not only exhibits lower input capacitance for TIA to be capability of high-speed operation, but also blocks the DC offset voltage from limiting amplifier and imbalanced signal from TIA.

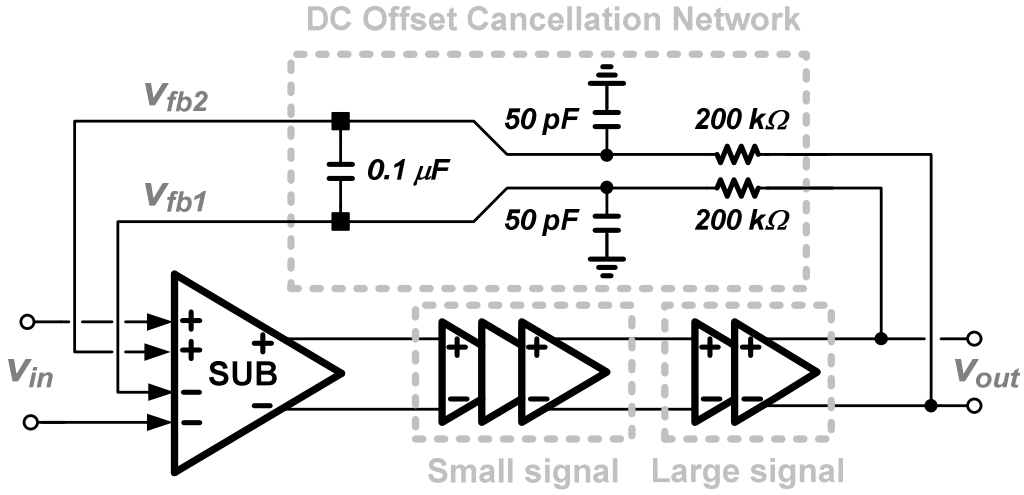


Figure 4-4 Limiting amplifier is composed of SUB and 5 gain cells.

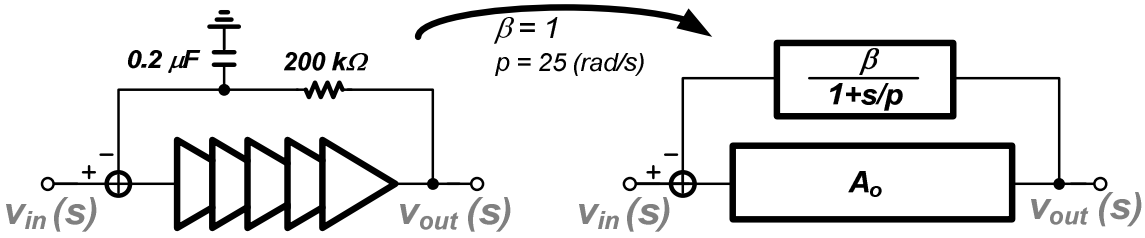


Figure 4-5 Feedback type limiting amplifier architecture.

4.3.1 DC Offset Cancellation Network

Besides of offering additional voltage gain, offset cancellation is another important key function in limiting amplifier design. The offset voltage may cause incorrect data regeneration and decrease the sensitivity.

Feedback type offset cancellation is adopted in this design for its minimum circuit overhead at signal path. The less overhead means the amplifier can operate at a higher speed. Figure 4-5 shows the diagram of the feedback type architecture. From the view of high frequency signal, it is an opened loop associated with the gain cells, because LPF has a lower -3dB frequency than input signal, usually on the order of several kHz. But, from the view of low frequency signal (like DC offset), it's a closed loop. The offset signal is fed back negatively and subtracted from the input. By using negative feedback, the equivalent offset voltage is divided by a factor of loop gain 1+Aβ.

Assume the feedback path of the limiting amplifier has a pole of $s = -p$, then the transfer function of the limiting amplifier can be described as:

$$\frac{v_{out}(s)}{v_{in}(s)} = \frac{A_o}{1 + A_o\left(\frac{\beta}{1+s/p}\right)} = \frac{A_o(s+p)}{s + p(1+A_o\beta)} \tag{4-6}$$

$$\Rightarrow \begin{cases} s = 0, \ \dfrac{v_{out}(s)}{v_{in}(s)} \approx \dfrac{A_o p}{p(1+A_o\beta)} \approx \dfrac{1}{\beta} & (4\text{-}7) \\ s = \infty, \ \dfrac{v_{out}(s)}{v_{in}(s)} \approx \dfrac{A_o s}{s} \approx A_o & (4\text{-}8) \end{cases}$$

where the A_o denotes the gain of the 5-stage gain cells.

Thus, the (4-7) and (4-8) mean that a signal at relative low frequency or the input offset voltage of LA, its gain is about 1; on the other hand, a signal at relative high frequency or the TIA output ac signal, its gain is about A_o. It is obviously that offset voltage will not be amplified by limiting amplifier which only amplifiers the ac signal from TIA.

4.3.2 Gain Cell Design

The schematic of the gain cell is depicted in Figure 4-6. Unlike the conventional Cherry-Hooper amplifier [12], the active feedback increases the GBW because it does not resistively load the transimpedance gain cell. Thus, no peaking inductor is needed. The Cherry-Hooper amplifier with active feedback can be simplified in Figure 4-7. The transfer function is given by:

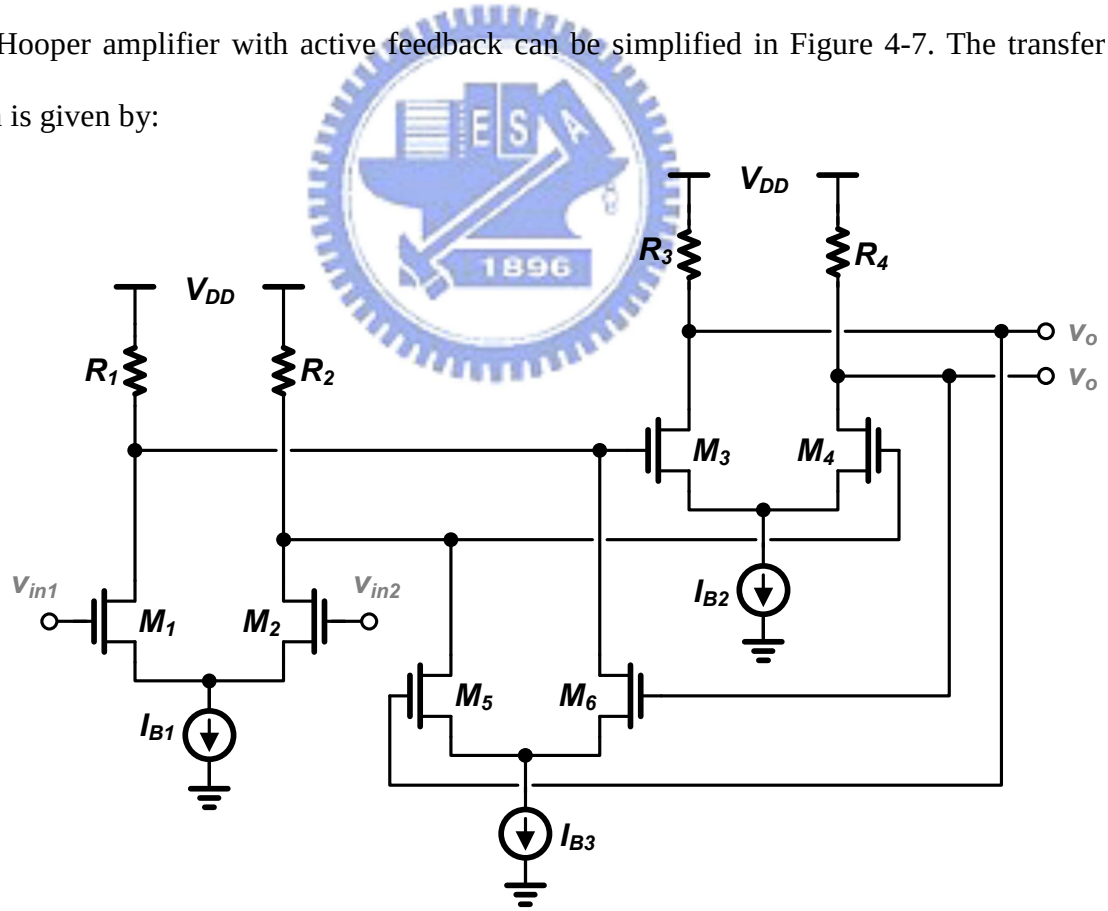


Figure 4-6 Gain cell in the limiting amplifier.

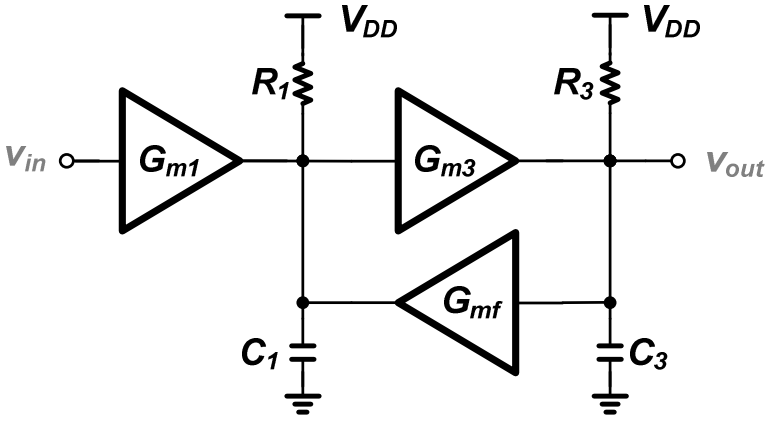


Figure 4-7 Active feedback architecture.

$$H_{GC}(s) = \frac{v_{out1} - v_{out2}}{v_{in1} - v_{in2}} = \frac{A_{v0}\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{4-9}$$

where

$$A_{v0} = \frac{G_{m1}G_{m2}R_1R_2}{1 + G_{m2}G_{mf}R_1R_2} \tag{4-10}$$

$$\zeta = \frac{1}{2}\frac{R_1C_1 + C_2R_2}{\sqrt{R_1R_2C_1C_2\left(1 + G_{m2}G_{mf}R_1R_2\right)}} \tag{4-11}$$

$$\omega_n^2 = \frac{1 + G_{m2}G_{mf}R_1R_2}{R_1R_2C_1C_2} \tag{4-12}$$

For a maximally-flat Butterworth response, let ζ be equal to $\sqrt{2}/2$. Then, $\omega_{3dB} = \omega_n$, and we have

$$A_{v0}\omega_{-3dB}^2 = \frac{G_{m1}G_{m2}}{C_1C_2} \Rightarrow A_{v0}\omega_{-3dB} = \frac{G_{m1}G_{m2}}{C_1C_2}\frac{1}{\omega_{-3dB}} \tag{4-13}$$

Since $G_{m1}/C_1 \sim G_{m2}/C_2 \sim \omega_T \sim 2\pi f_T$, (4-13) can be rewrite as

$$A_{v0}\omega_{-3dB} = \omega_T\frac{\omega_T}{\omega_{-3dB}} \Leftrightarrow A_{v0}f_{-3dB} = f_T\frac{f_T}{f_{-3dB}} \tag{4-14}$$

This result reveals that the active feedback increases the GBW beyond the technology f_T by a factor equal to the ratio of f_T and the cell -3dB bandwidth.

Moreover, the subtractor, depicted in Figure 4-8, is also based on the Cherry-Hooper amplifier with active feedback. Compared to Figure 4-7, I_{B1a}, I_{B1b} and $(L/W)_{M1,2}$ will reduce to

half if to keep the current consumption and transistor overdrive voltage. Thus, it is given

$$H_{SUB}(s) = H_{IN}(s) - H_{FB}(s) \tag{4-15}$$

$$H_{IN}(s) = \frac{v_{out1} - v_{out2}}{v_{in1} - v_{in2}} = \frac{1}{2} \times H_{GC}(s) \tag{4-16}$$

$$H_{FB}(s) = \frac{v_{out1} - v_{out2}}{v_{fb1} - v_{fb2}} = \frac{1}{2} \times H_{GC}(s) \tag{4-17}$$

where $H_{SUB}(s)$ is the transfer function of subtractor, while $H_{IN}(s)$ and $H_{FB}(s)$ represent the subtractor gain due to TIA and DC offset cancellation network, respectively.

To summarize the subtractor, it not only delivers a path for the DC offset voltage been cancelled, but also reduces the TIA's output capacitance for TIA to be capability of achieving higher bandwidth owing to half transistor size.

Figure 4-9 to Figure 4-13 show the limiting amplifier post-simulated results. To minimize ISI induced data jitter, the limiting amplifier is design as voltage gain of 47 dB, while the front 3 stages deliver voltage gain of 29 dB and -3 dB bandwidth of 3.1 GHz.

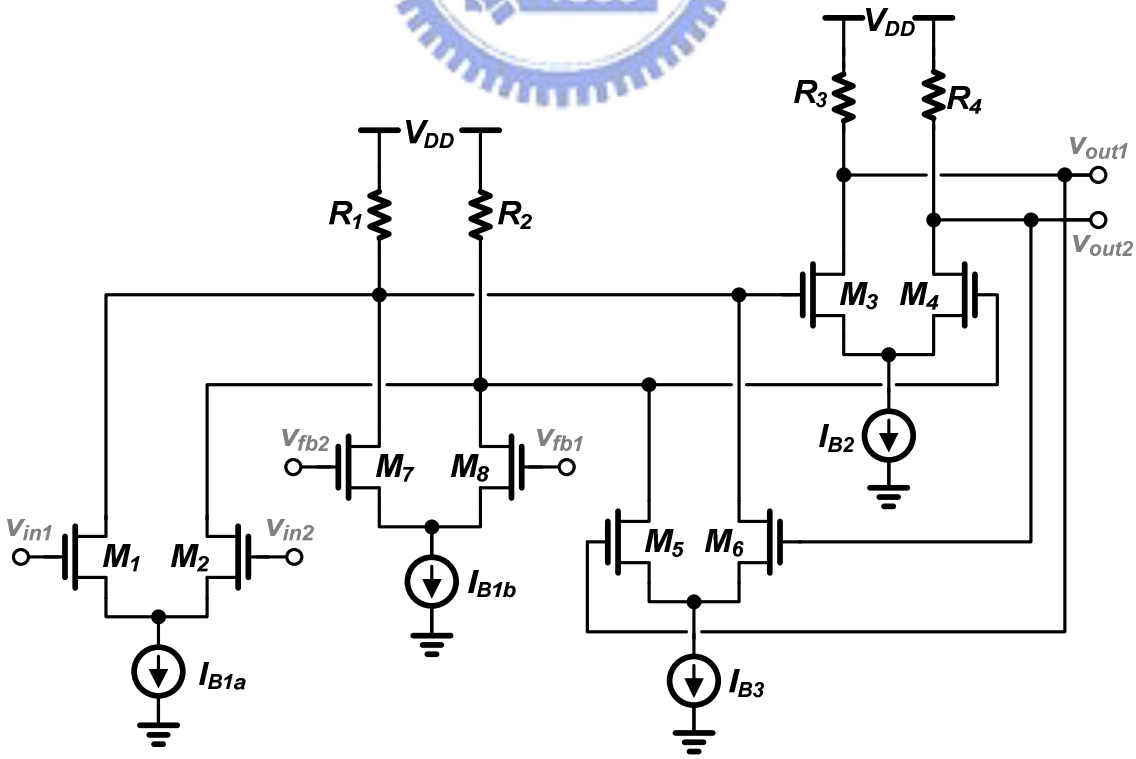


Figure 4-8 Subtractor schematic in the limiting amplifier.

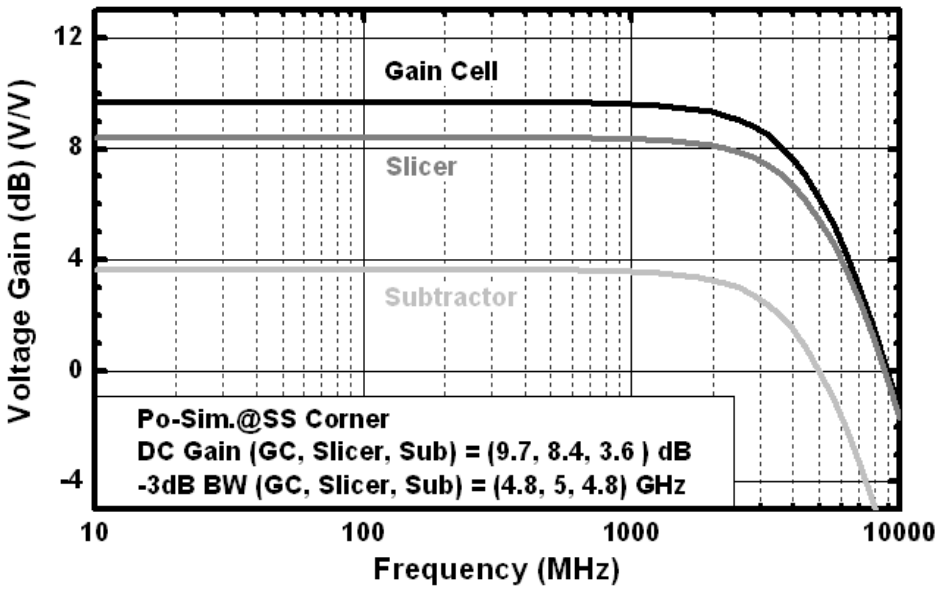


Figure 4-9 Magnitude responses of subtractor, gain cell and slicer.

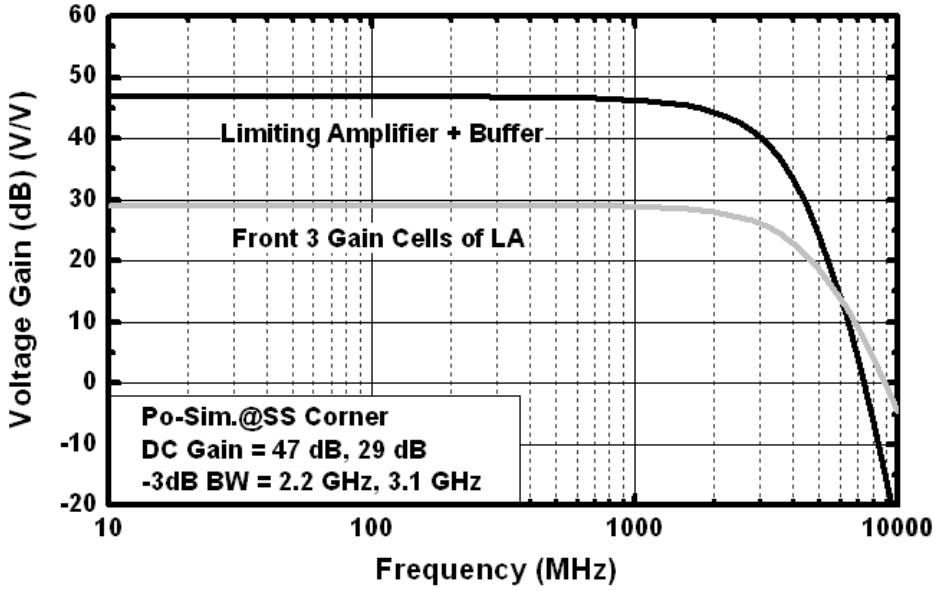


Figure 4-10 Magnitude responses of LA and front 3 stage.

And the gain of a subtractor, a gain cell and a slicer are 3.6 dB, 9.7 dB and 8.4 dB, while the -3 dB bandwidth is 4.8 GHz, 4.8GHz and 5GHz, respectively. The group delay variation of LA with buffer is about ±15 ps from 10 MHz to 2.5 GHz. Besides, the input-referred noise is about 1.6 mV_{rms} if the noise-bandwidth is about 2.5 GHz.

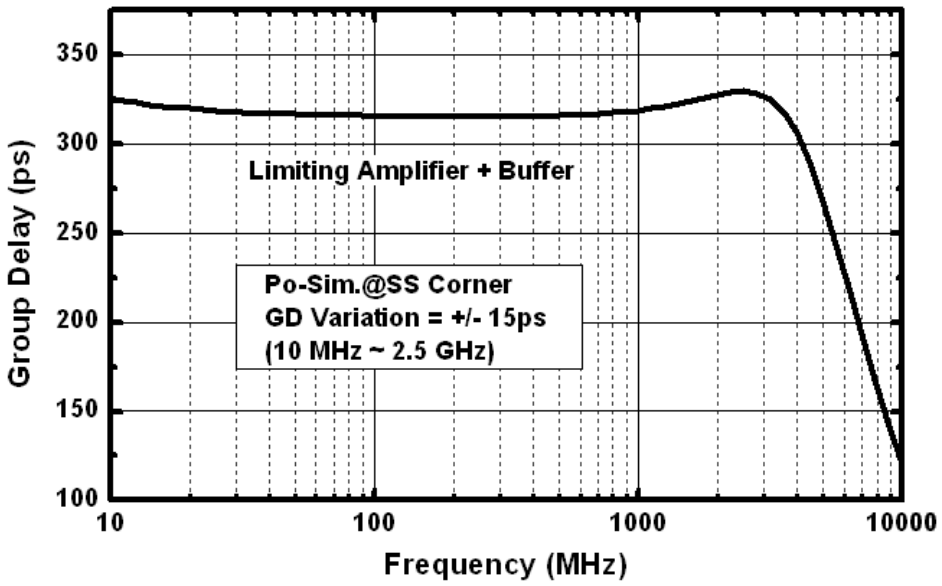


Figure 4-11 Group delay of LA.

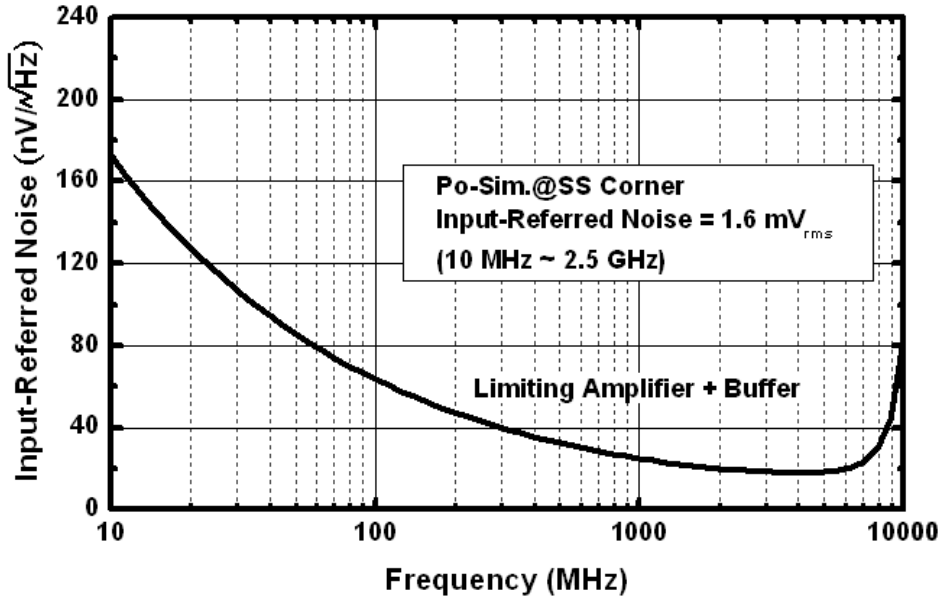


Figure 4-12 Input-referred noise of LA.

4.4 Summary

According to the post-layout simulated results, the limiting amplifier is able to operate for 3.2 Gbps data rate. It has a voltage gain of 47 dB (including 29 dB linear gain), group delay less than +/- 15 ps, input-referred noise about 1.6 mV_{rms}.

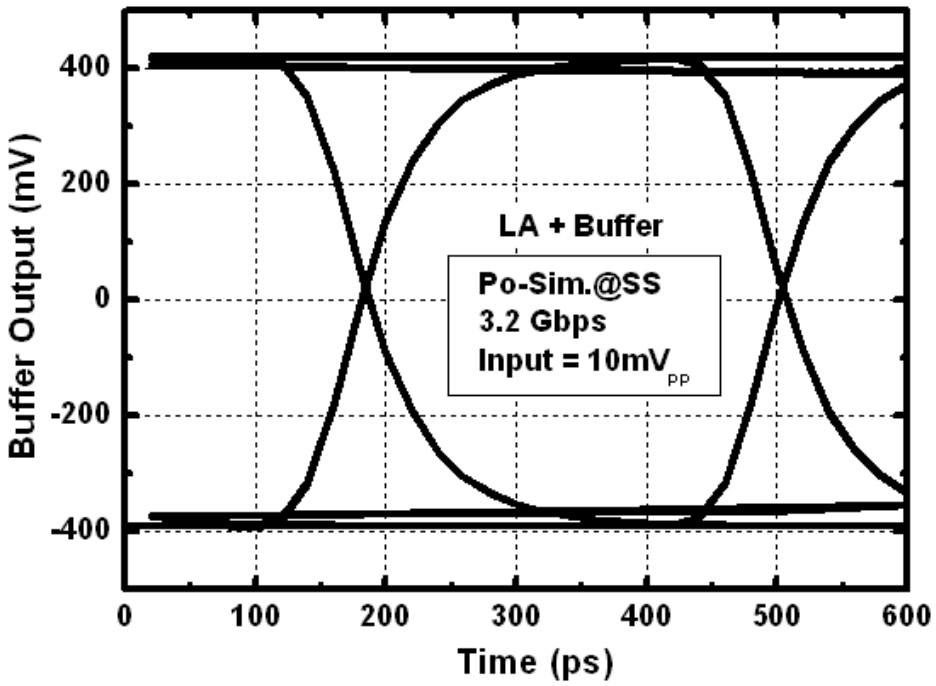


Figure 4-13 Simulated eye diagram of LA.

Table 4-1 Post-layout simulated results (RCC) of limiting amplifier.

	Specifications	***@ SS Corner***
Gain (front 3-stage)	28 dB	29 dB
LA Gain	44 dB	47 dB
- 3dB BW (front 3-stage)	3.125 GHz	3.1 GHz
Group Delay Variation	N.A.	+/- 15 ps
Power Consumption	N.A.	92 mW

Table 4-1 lists the simulated results of the limiting amplifier with a subtractor in the front, a DC offset cancellation network, 5-stage gain cell limiting amplifier (including 3-stage linear gain cell and 2-stage slicer gain cell).

Chapter 5

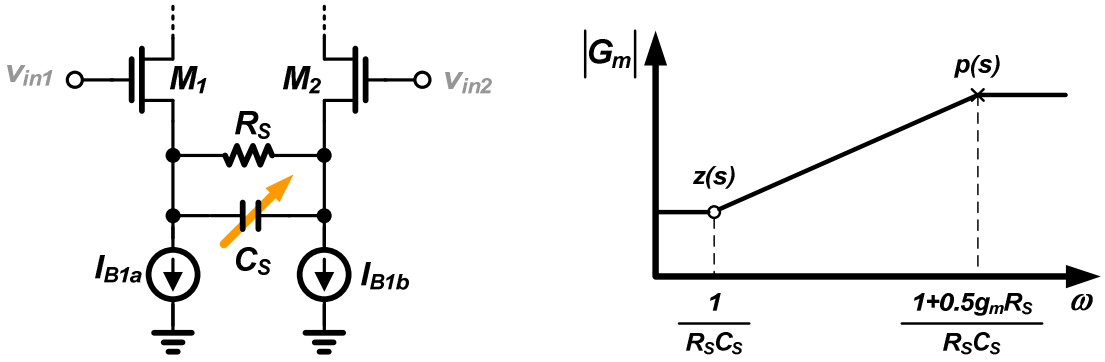
Adaptive Equalizer and Buffer

To compensate the bandwidth roll-off of a photodetector, a high-pass filter will be designed. In order to compensate the roll-off automatically, an equalizer with adjustable zero, two slope detectors and an error amplifier are adopted. In this chapter, an adaptive equalizer will be discussed first. Following equalizer, the high-speed output buffer is described in section 5.2.

5.1 Equalizer Circuit

To compensate the bandwidth degradation of SML detector, a high-pass filter will be designed. Typically, we can use the capacitance/resistance source degeneration, as shown in Figure 5-1, to create a zero, and the equivalent transconductance of this differential amplifier is given by:

$$G_m = \frac{g_{m1,2}}{1+g_{m1,2}\left(\frac{R_S}{2}\,//\,\frac{1}{2sC_S}\right)} = \frac{g_{m1,2}\left(sR_SC_S+1\right)}{sR_SC_S+\frac{g_{m1,2}R_S}{2}+1} \qquad (5\text{-}1)$$



(a) (b)

Figure 5-1 (a) Capacitance/resistance degeneration, (b) frequency response..

In the above equation, it contains a lower frequency zero located in $1/(R_S C_S)$, and a higher frequency pole located in $(1 + g_{m1,2}R_S/2)/(R_S C_S)$, thus it seems like a high-pass filter.

The equalizer [18] is shown in Figure 5-2. In contrast to the gain cells, it introduces a tunable zero in the transconductance stage of the Cherry-Hooper amplifier. As discuss before, the bandwidth of the SML photodetector is about 1.6 GHz. To compensate the bandwidth degradation of SML detector, the zero of equalizer should be adjusted around 1.6 GHz so as to cover bandwidth variations and fulfill the requirement of high speed operation.

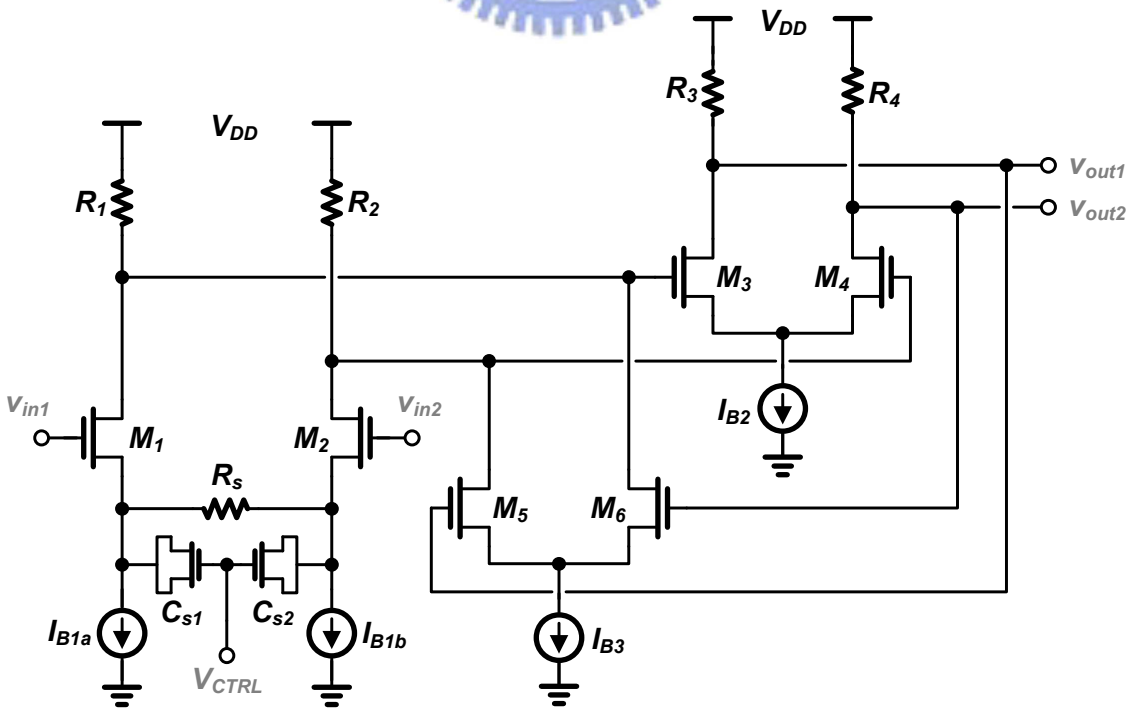


Figure 5-2 The equalizer circuit.

Adaptive Equalizer & Slope Detector

The schematic of adaptive equalizer is shown in Figure 5-3. The equalizer provides additional zero to compensate the bandwidth degradation caused by the photodetector. The zero location is adjusted by a feedback control loop which detects the edge slope of the output waveforms in the last two stages. In the slope detector, compare the steep slope of input differential signals with the slow one, the output averaging voltage is higher when steep slope signal is applied. The slope detector followed by an error amplifier which provides a low frequency pole to make sure a stable loop and delivers a DC signal to equalizer.

The slope detector can be realized as shown in Figure 5-3. It consists of a differential amplifier with the drain node connected to the V_{DD}. When a differential signal (v_{inx} or v_{iny}) is applied to the gates of the differential amplifier (M_{1x}, M_{2x} or M_{1y}, M_{2y}), it looks like transient time detector. In addition, its output voltage is higher if the differential input slope is steeper, and vice versa. For example (see Figure 5-4), if the slop of v_{iny} is steeper than v_{inx}, the average voltage of v_{outy} is higher than v_{outx}. After amplified by the error amplifier, V_{CTRL} drops and the zero of equalizer goes higher. On the other hand, if the slop of v_{inx} is steeper than v_{iny}, the average voltage of v_{outy} is lower than v_{outx}, V_{CTRL} arises and the zero of equalizer goes lower and peaking more.

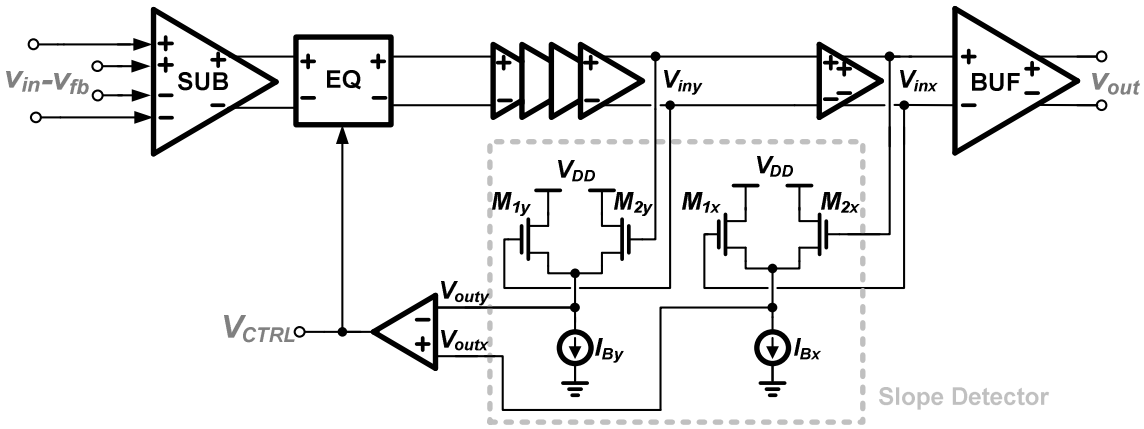


Figure 5-3 Adaptive equalizer.

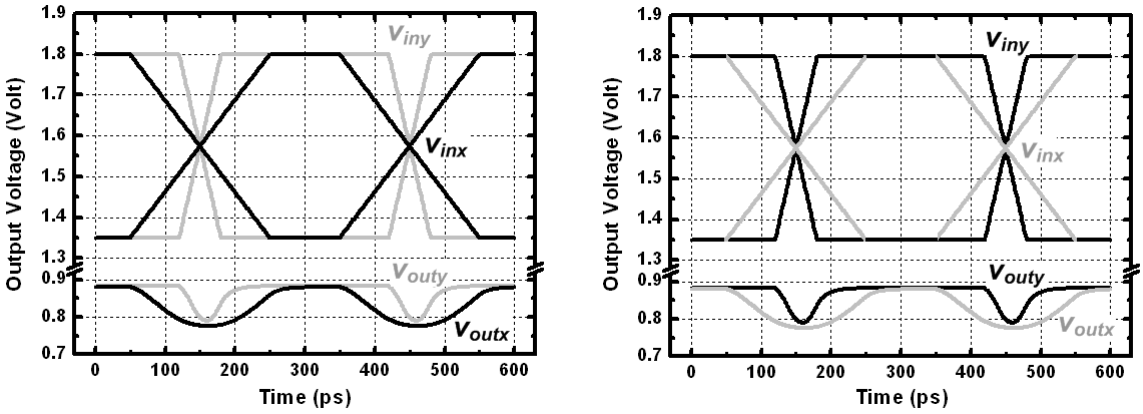


Figure 5-4 Transient simulation of the slope detector.

How much output voltage drop as a pair of differential signal is applied to slope detector? Assume the input voltage swing of slope detector is, v_{swing}, from V_{DD} - v_{swing} to V_{DD}. The output has minimum voltage as M_{1X} and M_{2X} drift equal current. Thus, it can be described as:

$$v_{\min} = V_{CMO} - V_{GS} = \left(V_{DD} - \frac{v_{swing}}{2} \right) - \left(\sqrt{\frac{I_B}{\mu_n C_{OX}} \frac{L}{W}} + V_t \right) \tag{5-2}$$

On the other hand, the output has the maximum voltage as either of M_{1X} or M_{2X} is off. At that time, it can be described as:

$$v_{\max} = V_{DD} - V_{GS} = V_{DD} - \left(\sqrt{\frac{2I_B}{\mu_n C_{OX}} \frac{L}{W}} + V_t \right) \tag{5-3}$$

And the output swing of the slope detector is

$$V_{\max} - V_{\min} \approx \frac{V_{swing}}{2} - 0.4 \sqrt{\frac{I_B}{\mu_n C_{OX}} \frac{L}{W}} \tag{5-4}$$

The above equation means the output voltage swing depends on the tail current, transistor size and input voltage swing.

For a slow transition of either polarity, the coupled-source node voltage is minimum value when the differential input is 1 or 0. And the response of any input transient is a negative pulse. However, a faster transient will have smaller pulse amplitude due to its short period of changing state.

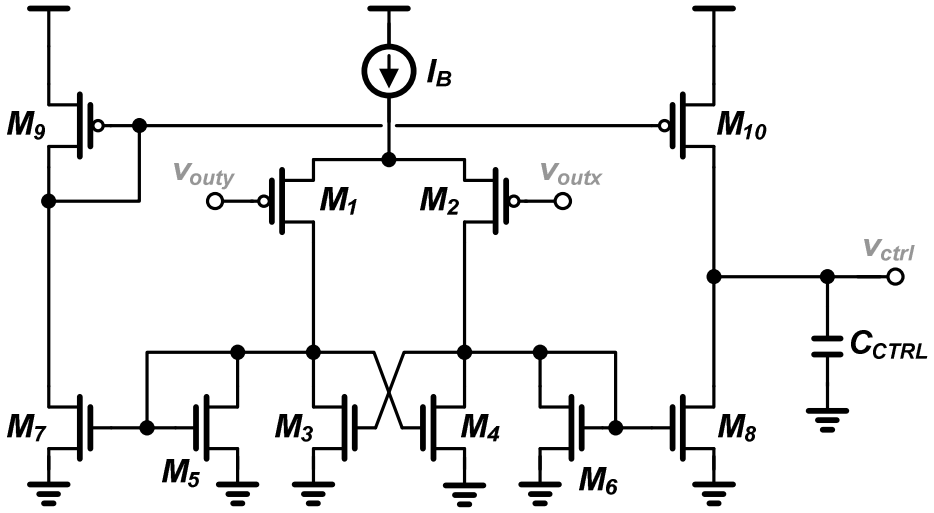


Figure 5-5 Two stage error amplifier.

Error Amplifier

As depicted in Figure 5-5, the error amplifier is a two-stage amplifier. The differential inputs are connected to the slope detector's outputs which have common-mode voltage about 0.8 V, so that the PMOS input stage is adopted in the error amplifier. To enhance the gain of the input stage, the negative impedance technique (M_3 and M_4) is used at its loading. In general, the conductance of (M_3 and M_4) is always 0.4 to 0.9 times than that of diode loading (M_5 and M_6) due to a stable condition. Besides, the second stage is designed to make output swing as large as possible. Thus, the DC gain of the error amplifier can be described as:

$$A_0 = \frac{v_{ctrl}}{v_{outx} - V_{outy}} = \left(\frac{g_{m1,2}}{g_{m5,6} - g_{m3,4}} \right) \left[g_{m7,8} \left(r_{o7,8} // r_{o9,10} \right) \right] \tag{5-5}$$

And the dominant pole is located in the output node that is

$$f_{-3dB} = \frac{1}{2\pi \left(r_{o7,8} // r_{o9,10} \right) C_{CTRL}} \tag{5-6}$$

5.2 Output Buffer

Impedance matching

In order to prevent the echoes or ISI, the impedance of each ends will be matched. To take an example of our OEICs, the buffer output travels on the PCB and transmission line to reach the sampling scope (see Figure 5-6). Because the transmission line has characteristic impedance of 50 Ω and the input impedance of the scope is 50 Ω, the guide line on PCB will be designed characteristic impedance of 50 Ω, and output impedance of the buffer as well.

Input Capacitance

The input capacitance of output buffer will be designed as small as possible. A large input capacitor directly contributed to the preceding stage and may degrade the bandwidth. Thus, a buffer with small input capacitance will be designed to relax the specifications of LA.

Bandwidth

In addition, the bandwidth of output buffer will be designed as high as possible to prevent bandwidth degradation of systems. Typically, the output impedance will be small.

Power Consumption

With a typical impedance level of 50 Ω, the output buffers or drivers must provide a large output current so as to produce enough voltage swing. Thus, it gets more and more important so as to lead the growing demand of low power consumption buffers.

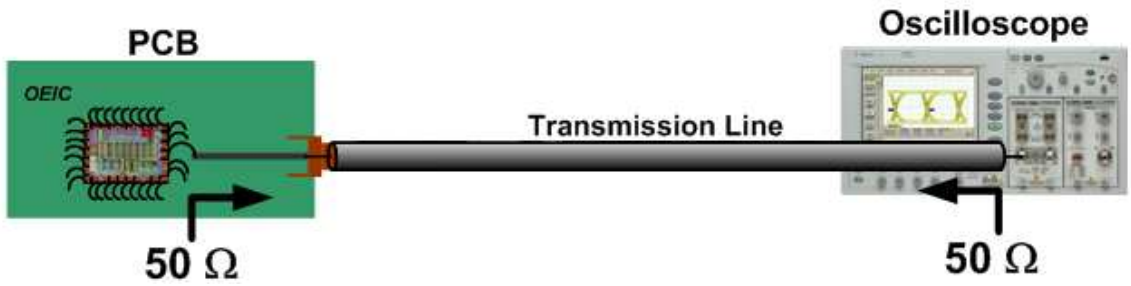


Figure 5-6 Connection of this OEIC and an oscilloscope through a transmission line.

5.2.1 Output Buffer Implementation

In the following, the output buffer implementations will be discussed. This includes the open-drain output buffer, simple differential output buffer and f_T-doubler output buffer.

Open-Drain Output Buffer

As illustrated in Figure 5-7, the buffer exhibits relatively high output impedance which isn't matched to the 50 Ω. At higher speeds, such mismatches create significant reflections that travel back to the buffer, see a high impedance mismatch at the near end, are reflected again, and reach the far end with some delay with respect to the original signal. As a result, the reception may experience ISI. The simulated eye diagram for a data rate of 10 Gbps in 0.18-μm technology is shown in Figure 5-8(a). The differential output waveform is subjected to severe ISI so as to destroy eye diagram. Its can be described as:

$$A_1 = \frac{v_{out}}{v_{in1} - v_{in2}} = g_{m1,2} R_{TL} \tag{5-7}$$

where $g_{m1,2}$ is the tranconductance of M_1 and M_2, and R_{TL} is transmission line's characteristic impedance, 50 Ω.

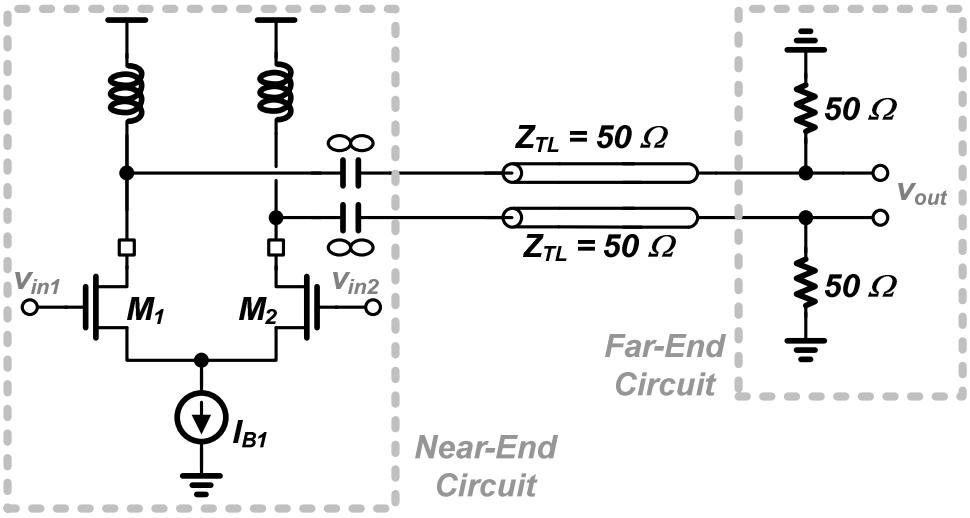


Figure 5-7 Open-drain output buffer.

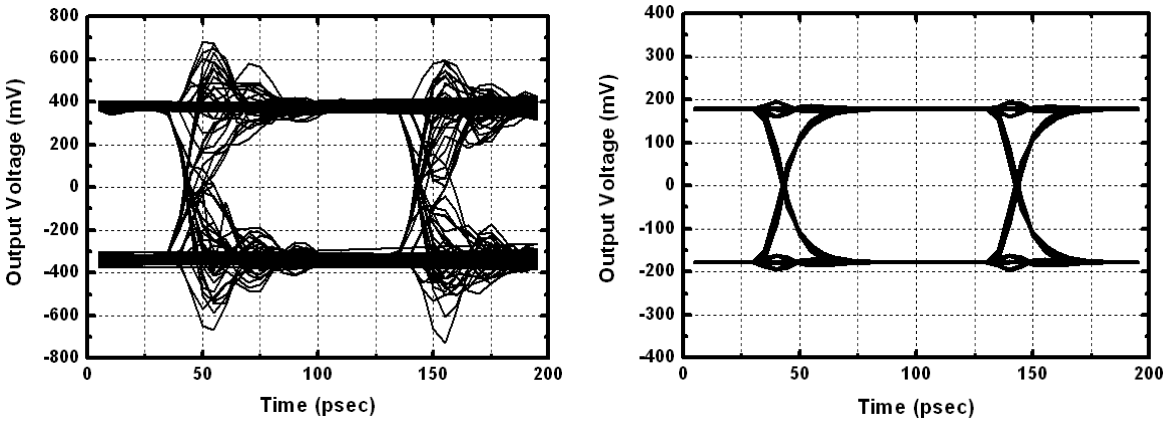


Figure 5-8 Open-drain output buffer.

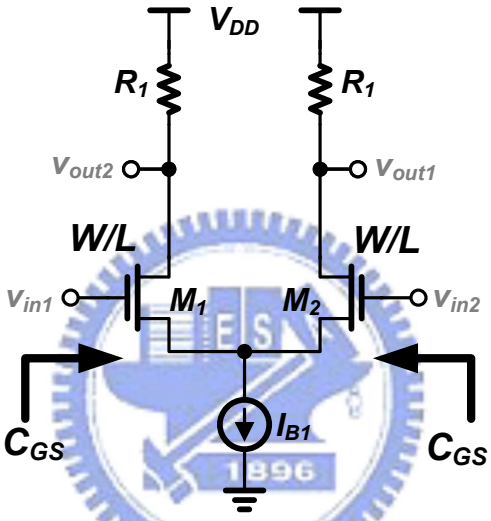


Figure 5-9 A simple differential stage.

Simple Differential Output Buffer

As shown in Figure 5-9, the output buffer can also implemented by a simple differential amplifier with 50 Ω load for near-end termination. Compared to the open-drain buffer, it minimizes the reflections form the near-end. However, the 50 W load reduces the gain to be 0.5 times that of open-drain buffer with constant current consumption.

The gain of a simple differential output buffer can be described as:

$$A_2 = \frac{v_{out}}{v_{in1} - v_{in2}} = g_{m1,2}\left(R_L \,//\, R_{TL}\right) = \frac{g_{m1,2} R_{TL}}{2} \qquad (5\text{-}8)$$

The simulated eye diagram is shown in Figure 5-8(b). Compared to Figure 5-8(a), the eye diagram opens very clearly, but the differential output swing is reduced to about ±200 mV.

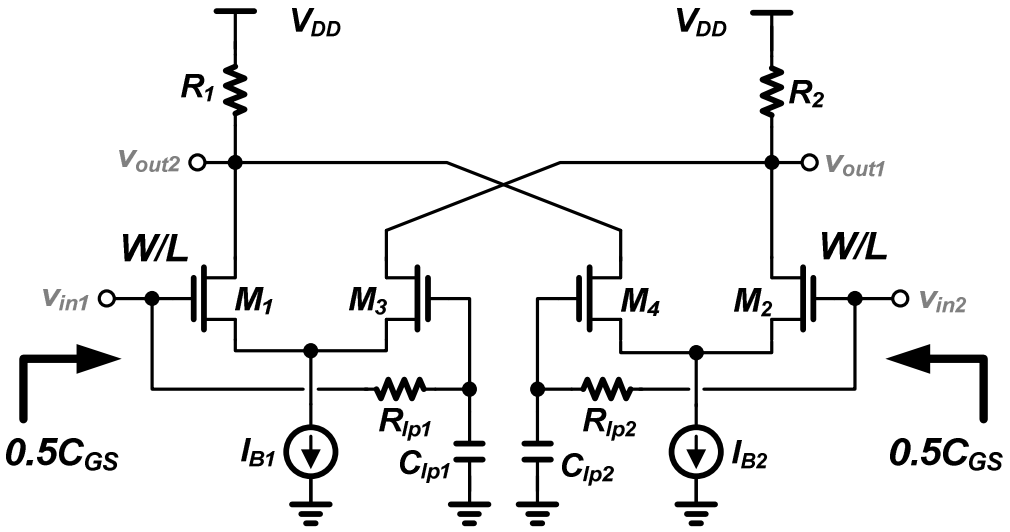


Figure 5-10 F_T-doubler output buffer.

F_T -Doubler Output Buffer

For output buffer, large transistor size is necessary to achieve such a large current. Unfortunately, the large size will produce substantial parasitic capacitance that will decrease the signal bandwidth. To alleviate the load to preceding gain stages, a f_T-doubler [12] circuit shown in Figure 5-10 is adopted. Compare f_T-doubler with a simple differential stage with the same drive capability, one can get the idea that f_T-doubler has smaller input capacitance.

The gain of f_T-doubler output buffer can be also described as:

$$A_3 = \frac{v_{out}}{v_{in1} - v_{in2}} = \frac{g_{m1,3}\left(R_L // R_{TL}\right)}{2} + \frac{g_{m2,4}\left(R_L // R_{TL}\right)}{2} = \frac{g_{m1,2,3,4} R_{TL}}{2} \qquad (5\text{-}9)$$

The above equation denotes that its DC gain is the same as that of a simple differential amplifier. But, its current consumption is larger than a simple differential amplifier by 2 times and output capacitance as well.

5.2.2 Output Buffer Comparison

Table 5-1 and Table 5-2 list the comparisons between the three types of output buffers, which are open-drain output buffer, simple differential output buffer and f_T-doubler output

buffer, with the same gain and with the same output swing.

In our designs, the impedance matching is very important because the data rate is above 3 Gbps with PRBS signal. Thus, to get rid off the ISI due to microwave reflection in the output, the open-drain output buffer is not suitable for our design.

Besides, in order to relax the specifications of LA, the f_T-doubler is chosen owing to its low input capacitance.

Table 5-1 Buffer's performance comparison with the same DC gain.

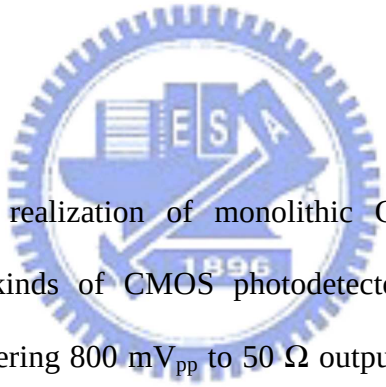
	Near-End Termination	***Input Capacitance***	***Output Capacitance***	***Power***
Open-Drain	No	0.5 C_{GS}	0.5 C_{OUT}	0.5 P_S
Simple Differential	Yes	C_{GS}	C_{OUT}	P_S
F_T-Doubler	Yes	0.5 C_{GS}	2 C_{OUT}	2 P_S

Table 5-2 Buffer's performance comparison with the same output swing.

	Near-End Termination	***Input Capacitance***	***Output Capacitance***	***DC Gain***
Open-Drain	No	0.5 C_{GS}	0.5 C_{OUT}	2 A_2
Simple Differential	Yes	C_{GS}	C_{OUT}	A_2
F_T-Doubler	Yes	0.25 C_{GS}	C_{OUT}	0.5 A_2

Chapter 6

Optical Receiver Realizations



This chapter presents the realization of monolithic CMOS optical receiver analog front-ends (AFE) with two kinds of CMOS photodetectors. Both two optical receiver front-ends are capable of delivering 800 mV_{pp} to 50 Ω output loads after optical to electrical conversion. Moreover, they are implemented in a standard 0.18 μm digital CMOS technology.

Section 6.1 illustrates that the first optical receiver front-end which integrates a SML detector, a TIA, and a post limiting amplifier on a single chip. Also, the OEIC architecture, simulated results and measured results will be discussed.

We propose and utilize a lateral PIN detector emulated by P^+diffusion / P-well / N^+diffusion interleaved architecture and surrounded by N-well and deep N-well to enhance the PD's responsivity and bandwidth. In section 6.2, the second monolithically-integrated receiver front-end is introduced. It also integrates the novel lateral PIN detector, a TIA, and a limiting amplifier on a single chip.

6.1 A 3.125 Gbps AFE with SML Detector

6.1.1 SML Detector

An approach of fully CMOS optical receiver with high speed operation is by employing SML detector. According to the simulated results, the responsivity is about 62 mA/W, while -3 dB bandwidth is about 2.1 GHz by the SML detector which consists of 10 N-well/P-substrate dark detectors (size: 2.1 μm x 65 μm) and 10 N-well/P-substrate illuminated detectors (size: 2.1 μm x 65 μm) interleaved. To characterize more accurately the performance of the SML detector, it was integrated with on-chip transimpedance amplifier for measurement.

The experimental results are shown in Figure 6-1. The measured -3 dB bandwidth is about 1.6 GHz. Compared to the N-well/P-substrate PN junction PD, whose -3 dB bandwidth is about 10 MHz. In other words, the SML detector can improve the photodetector bandwidth by more than 2 orders. However, its bandwidth is still insufficient for a receiver operated above 3 Gbps.

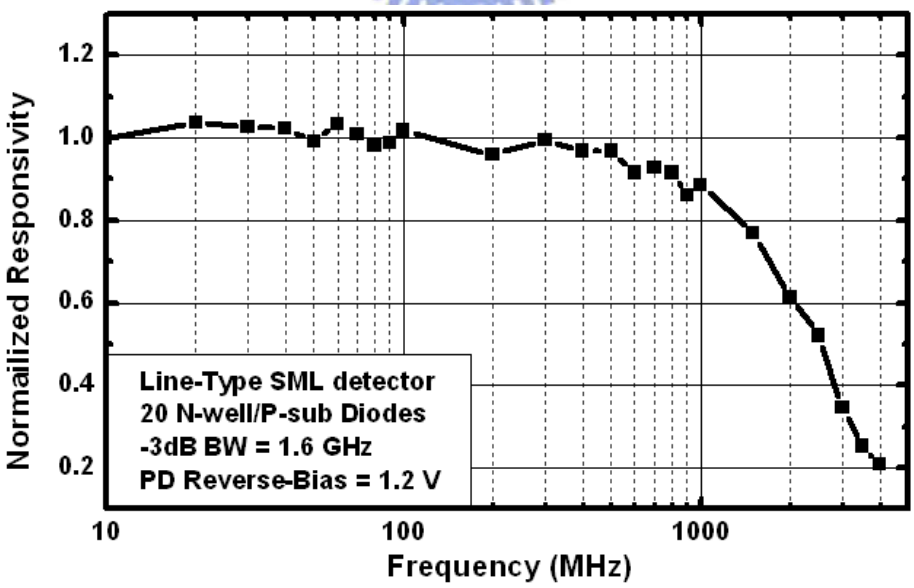


Figure 6-1 Measured magnitude response of SML detector.

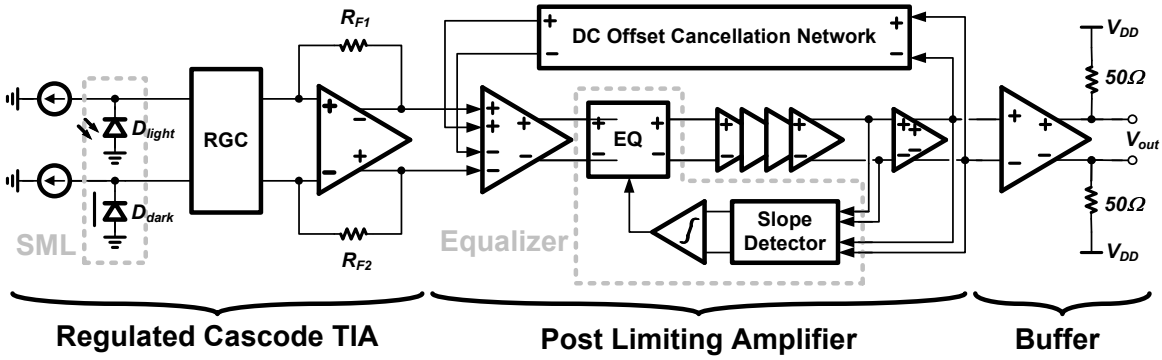


Figure 6-2 Optical receiver front-end architecture.

6.1.2 Architecture

This section describes the design of a 3.125 Gbps optical receiver, which monolithically integrates a photodetector (PD), a TIA and a post limiting amplifier (PA) in a generic 0.18-μm CMOS technology. The architecture of the optical receiver is shown in Figure 6-2.

High speed operation is achieved by utilizing SML detector incorporating with adaptive analog equalizer. In order to achieve an operating speed above 3 Gbps, adaptive equalizer is also adopted to compensate the modest frequency response of the SML detector which is measured 1.6 GHz in -3dB bandwidth.

The transimpedance amplifier with a RGC stage at the input node is capable of tolerance the large photodetector capacitance. The simulated results (in section 3.3) show the TIA provides a conversion gain of about 60 dBΩ, and a -3dB bandwidth of about 2.9 GHz to compromise between input-referred noise and ISI.

The five-stage limiting amplifier with 3-stage linear amplifier and 2-stage slicer (in section 4.3) is able to switch the signal at data rate 3.125 Gbps. Also, the f_T-doubler output buffer with smaller input capacitance is utilized to relax the specifications of the limiting amplifier.

To the authors' knowledge, this is the fully integrated CMOS optical receiver that exhibits the highest operating speed reported to date. Besides, due to a relatively low responsivity of the SML detector, no automatic gain control circuit is needed in this design.

6.1.3 Test Chip

The layout of this optical receiver front-end with SML detector is shown in Figure 6-3. This chip is implemented by 0.18 μm one-poly six-metal CMOS process, and measured 0.99 μm by 0.71 μm which is dominated by the limiting amplifier. It exhibits 30 I / O pads, and the pad descriptions are listed in Table 6-1. There are 22 pads connected to neither V_{DD} or G_{ND}, 3 pads (#1, #3 and #21) connected to large bypass capacitance of 0.1 μF, 2 output pads (#19 and #20) connected to the AC coupling capacitance of 0.1 μF and delivering the output signals to sampling scope, Agilent 86100C, 1 pad (#10) being the input signal to control the zero location of the equalizer in case that the adaptive function fails, 1 pad (#11) connected to the variable resistance of 20 kΩ to adjust the input biasing current to the correct operating point, and the other 1 pad (#16) being unused.

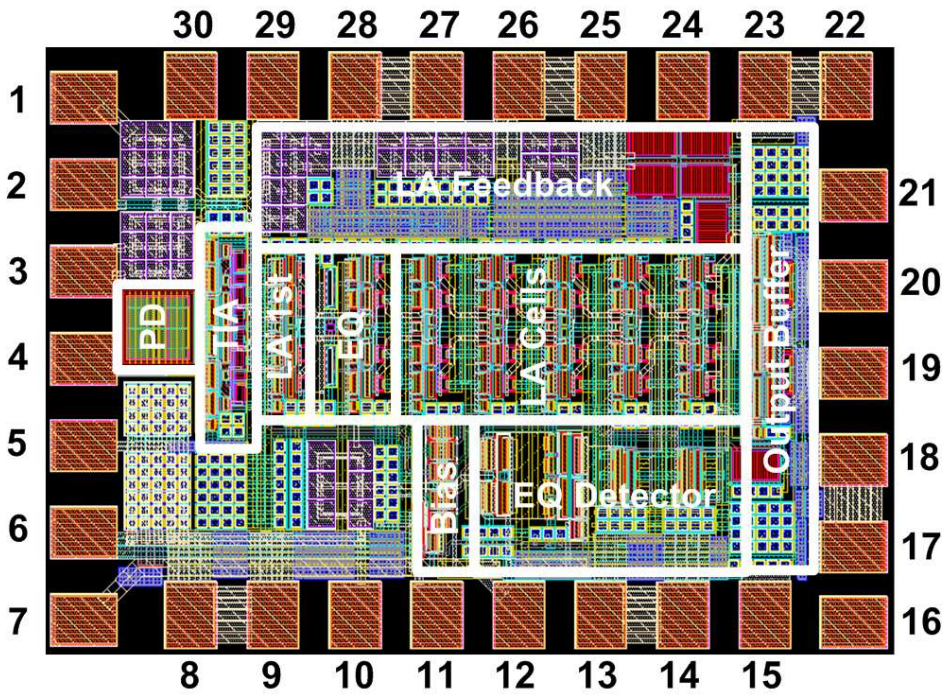


Figure 6-3 Chip layout of OEIC with SML detector.

Table 6-1 The pad descriptions of OEIC with SML detector.

PAD #	Description	PAD #	Description
1	V_{FB1}, to bypass capacitance	**16**	Unused pad
2	NMOS body, to G_{ND}	**17**	Ft-doubler V_{DD}
3	V_{FB2}, to bypass capacitance	**18**	Ft-doubler V_{DD}
4	TIA G_{ND}	**19**	V_{OUT1}, output signal
5	TIA V_{DD}	**20**	V_{OUT2}, output signal
6	NMOS body, to G_{ND}	**21**	V_{LP}, bypass capacitance
7	PMOS body, to V_{DD}	**22**	Ft-doubler G_{ND}
8	LA G_{ND}	**23**	Ft-doubler G_{ND}
9	LA G_{ND}	**24**	NMOS body, to G_{ND}
10	V_{CTRL}, EQ control voltage	**25**	LA G_{ND}
11	R_{BIAS}, to 20 kΩ variable res.	**26**	LA G_{ND}
12	Biasing Circuit V_{DD}	**27**	LA V_{DD}
13	LA V_{DD}	**28**	LA V_{DD}
14	LA V_{DD}	**29**	TIA V_{DD}
15	NMOS body, to G_{ND}	**30**	TIA G_{ND}

The measurement setup is shown as Figure 6-4. The OEIC is mounted on a printed circuit board for measurement. The eye diagrams and the bit error rate performance are characterized using Anritsu MP1800. The pattern generator in the Anritsu MP1800 sends a 2^{31}-1 PRBS test pattern to modulate an 850-nm New Focus 10 Gbps VCSEL as a light source. VSCEL generates the 850-nm wavelength optical light which is guided by the multimode fibers and Cascade lightwave probe (fixed in the RF-1 Cascade probe station) to the photodetector on the OEIC. Between VCSEL and lightwave probe, the optical power is attenuated by OZOptics digital attenuator for input sensitivity measurement. After amplifying the photocurrent, the OEIC sends a pair of differential output signal back to the Anritsu MP1800 for bit-error-rate test. At the same time, Anritsu MP1800 sends the unity-gain buffer output and trigger signal to the Agilent 86100C for eye diagram measurement.

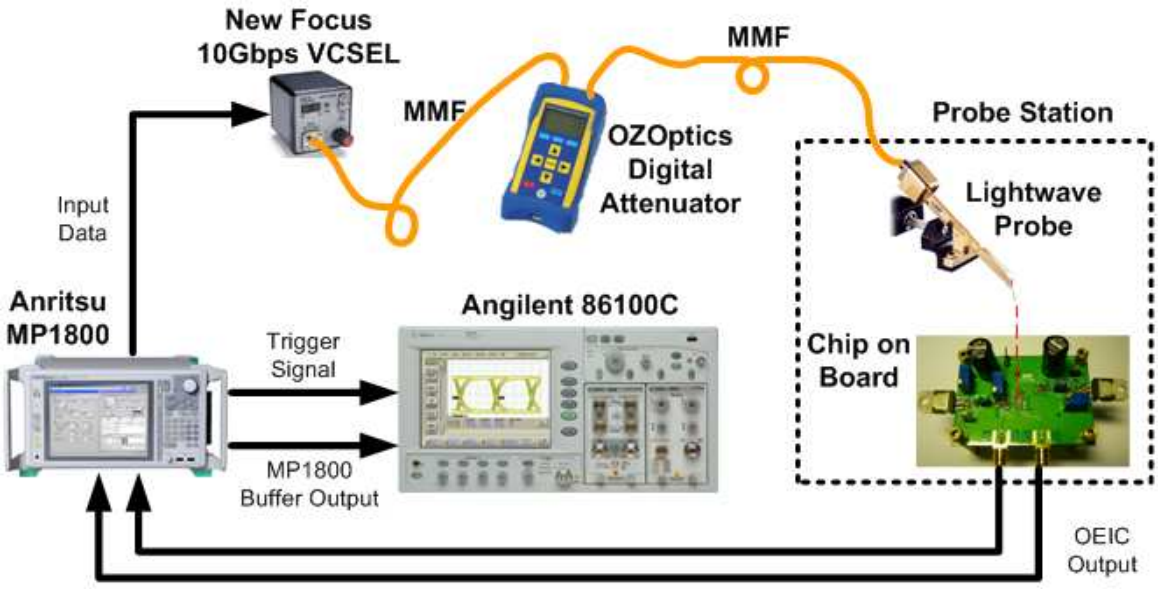


Figure 6-4 Measurement setup.

6.1.4 Measurement Results

The chip micrograph is shown in Figure 6-5. Implemented in a generic 0.18-μm CMOS technology, the total chip area is about 710 μm by 990 μm. The area of photodetector is 65 μm by 65 μm to comply with the diameter of the multi-mode fiber.

The TIA is powered with a 3.3 V supply to provide a sufficient voltage headroom for the photodetector, while the limiting amplifier is operated under a single 1.8 V supply. The total power dissipation is 175 mW, among which 30 mW is consumed by the output buffer. By cascading transimpedance amplifier and limiting amplifier on a single chip, the optical receiver provides a conversion gain of 110 dBΩ. The overall $f_{H\text{-}3dB}$ is about 2.46 GHz, which is limited by the photodetector. It is capable of delivering 800 mV_{pp} differential voltage swings to 50 Ω output loads directly.

The bit error rate performance is summarized in Figure 6-6. As the responsivity of the photodetector is only about 62 mA/W, the input sensitivity levels with BER less than 10^{-12} at 2.5 Gbps and 3.125 Gbps are about -5.8 dBm and -4.2 dBm respectively. Figure 6-7 and Figure 6-8 show the measured eye diagrams at 2.5 Gbps with the maximum input power, -3

dBm, and the input sensitivity level (-5.8 dBm). The data jitters are about 16.64 ps_{rms} (111.11 ps_{pp}) and 19.79 ps_{rms} (133.33 ps_{pp}), respectively. In addition, Figure 6-9 and Figure 6-10 shows the measured eye diagrams at 3.125 Gbps with -3 dBm, and the input sensitivity level (-4.2 dBm). The data jitters are about 17.04 ps_{rms} (108.44 ps_{pp}) and 16.86 ps_{rms} (120.89 ps_{pp}), respectively.

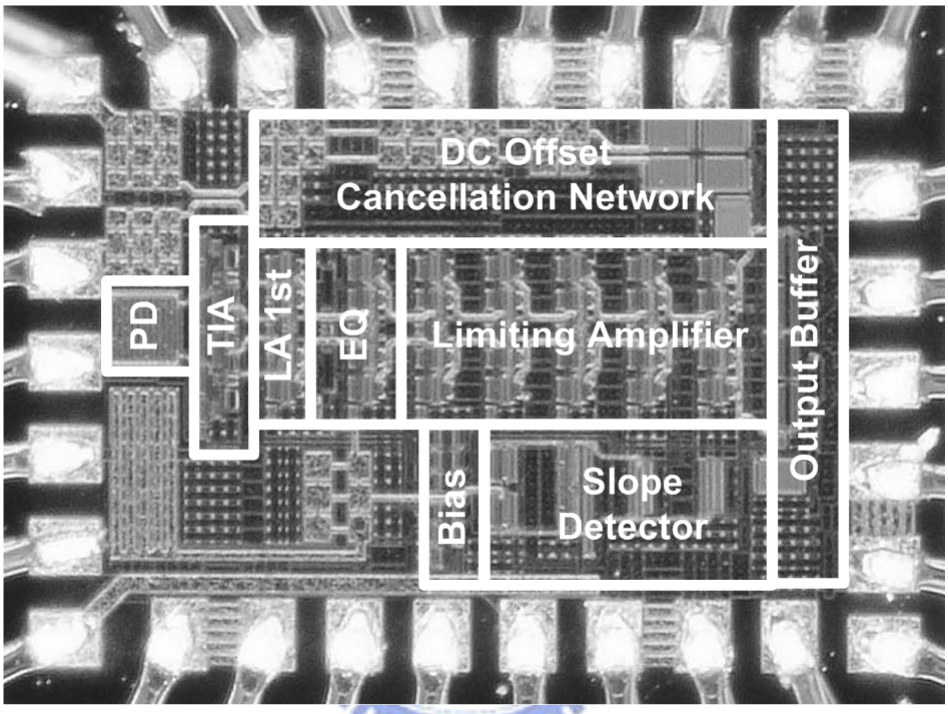


Figure 6-5 Chip micrograph of OEIC with SML detector.

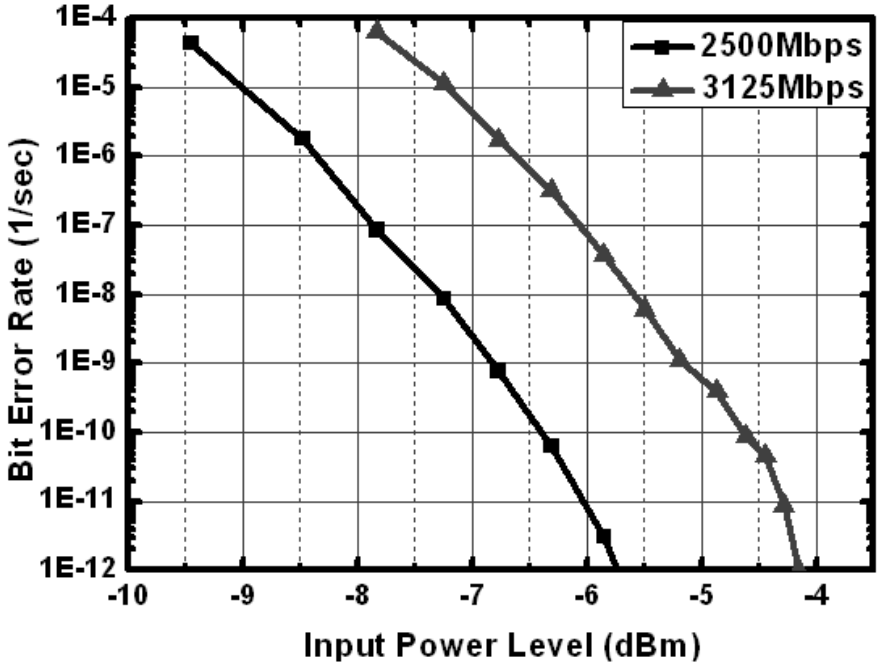


Figure 6-6 Measured bit error rate performance of the OEIC.

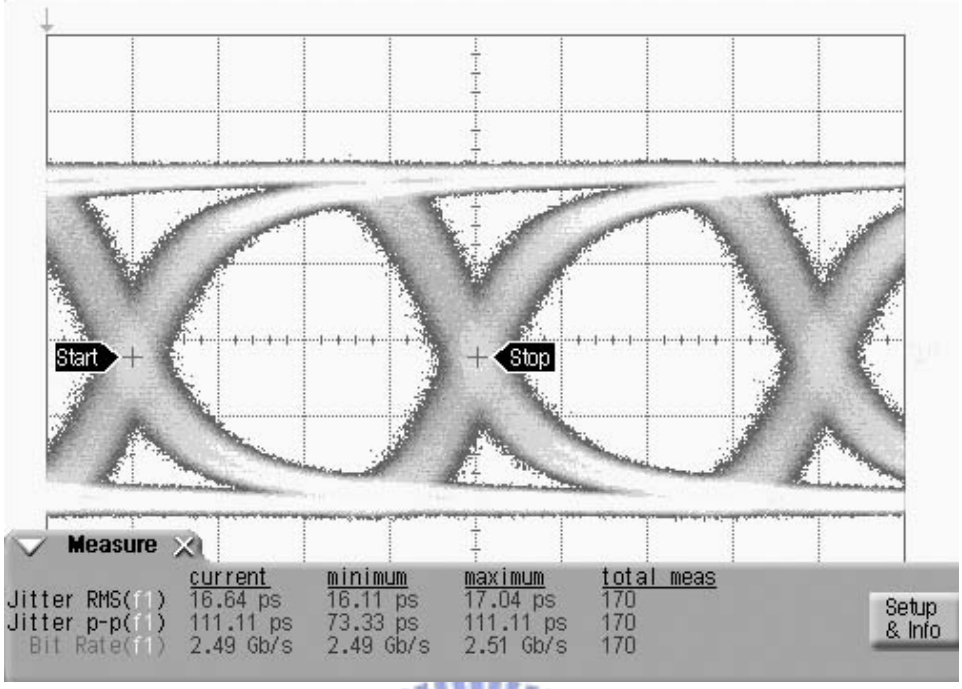


Figure 6-7 Eye diagram at 2.5 Gbps with the maximum input power, -3 dBm.

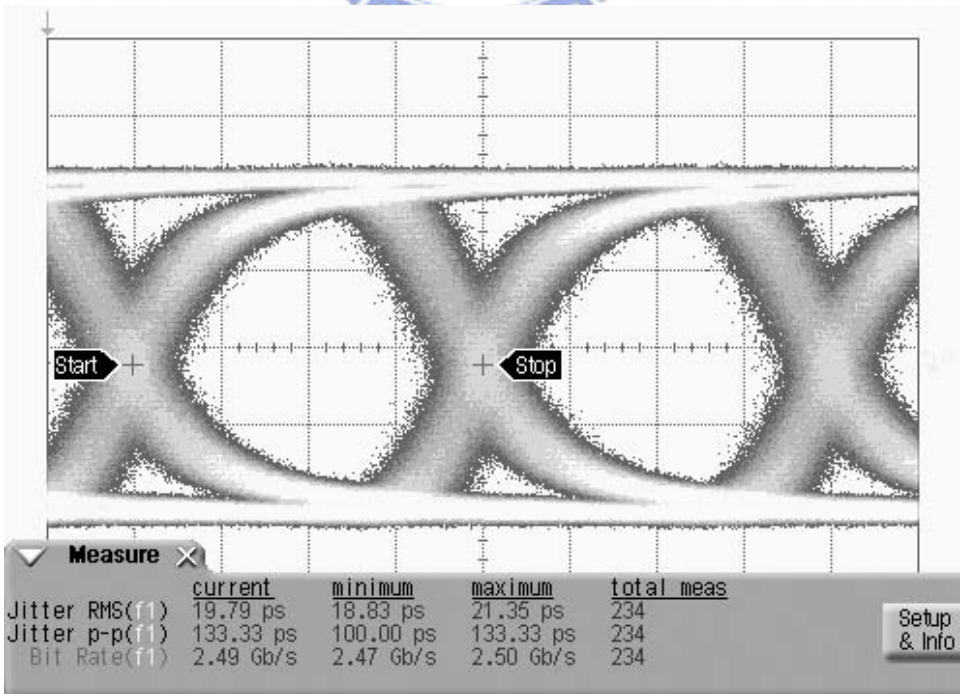


Figure 6-8 Eye diagram at 2.5 Gbps with sensitivity level, -5.8 dBm.

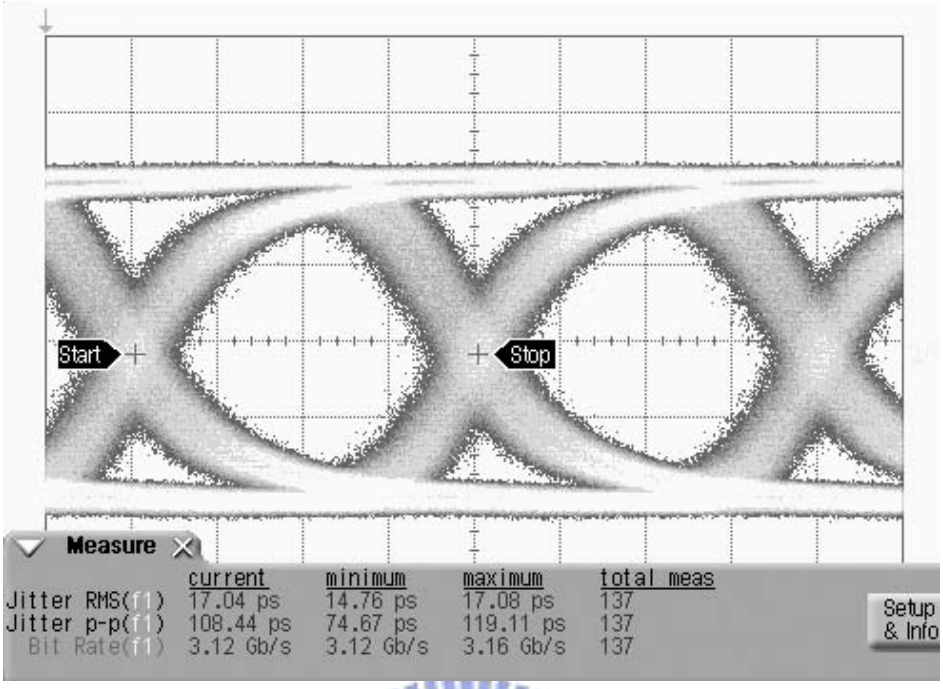


Figure 6-9 Eye diagram at 3.125 Gbps with the maximum input power, -3 dBm.

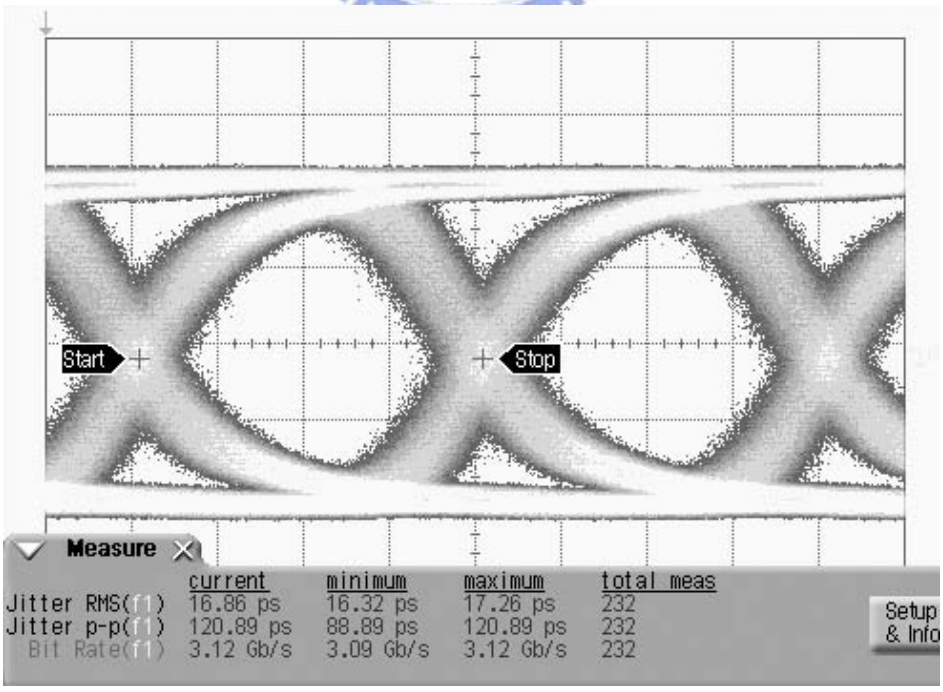


Figure 6-10 Eye diagram at 3.125 Gbps with sensitivity level, -4.2 dBm.

6.2 A 2.5 Gbps AFE with PIN Detector

6.2.1 PIN Detector

As shown in Figure 2-9, the PIN detector is 50 μm × 50 μm in active area and consists of 13 P-I-N fingers, the P+ and N+ stripes are 1.45-μm wide, separated by a 0.5-μm wide P-well region. Thus a reasonable low (~ 2 to 6 V) reverse biased voltage (V_R) is sufficient to deplete the P-well region of the photodetector for a high speed operation. According to the simulated results, the responsivity is about 73 mA/W, while -3 dB bandwidth is about 1.9 GHz.

6.2.2 Architecture

This section describes the design of a 2.5 Gbps optical receiver, which monolithically integrates a PD, a TIA and a limiting amplifier in a generic 0.18-μm digital CMOS technology. A novel PIN detector is proposed and adopted in the design without technology modification. The architecture of fully integrated optical receiver is shown in Figure 6-11. The incoming signal is converted to a photo current by an on-chip PIN detector, and regenerated to a voltage signal of 800 mV_{pp} by a transimpedance amplifier (TIA), a limiting amplifier (LA). To alleviate bandwidth degradation by parasitic capacitance of photodetector, a regulated cascode

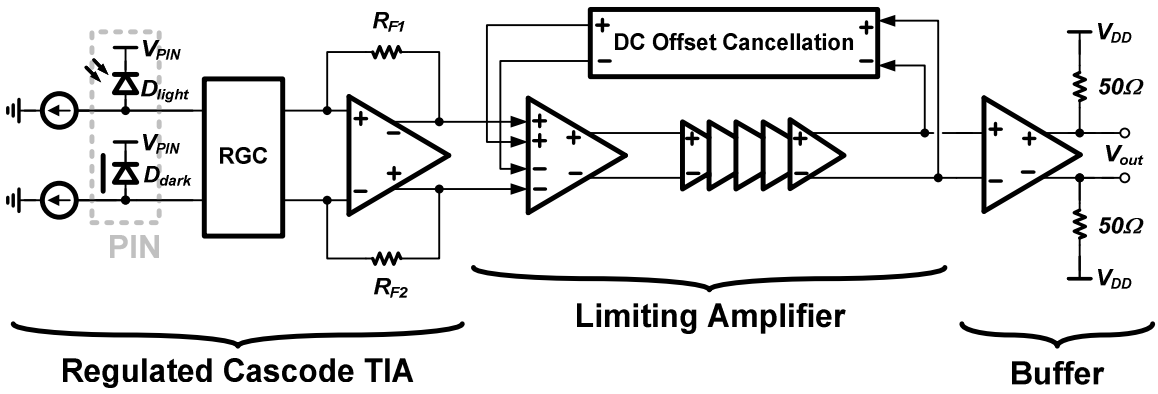


Figure 6-11 Optical receiver architecture

(RGC) topology is adopted as the input stage. In addition, the responsivity of this PIN detector is not large enough to have an automatic gain control circuit in this design.

The transimpedance amplifier with a RGC stage at the input node is capable of tolerance the large photodetector capacitance. The simulated results (in section 3.3) show the TIA provides a conversion gain of about 60 dBΩ, and a -3dB bandwidth of about 2.9 GHz to compromise between input-referred noise and ISI.

The five-stage limiting amplifier with 3-stage linear amplifier and 2-stage slicer (in section 4.3) is able to switch the signal at data rate 2.5 Gbps. Also, the f_T-doubler output buffer with smaller input capacitance is utilized to relax the specifications of the limiting amplifier.

6.2.3 System Simulation Results

Figure 6-12 to Figure 6-15 show the post-simulated results of the OEIC with PIN detector in the front. The overall OEIC has a gain of 107 dB, -3 dB bandwidth of 2.0 GHz. The group delay variation of OEIC with PIN detector and output buffer is about ±23 ps from 10 MHz to 2.5 GHz. Besides, the input-referred noise is 2 mV_{rms} if the noise-bandwidth is 2.5 GHz.

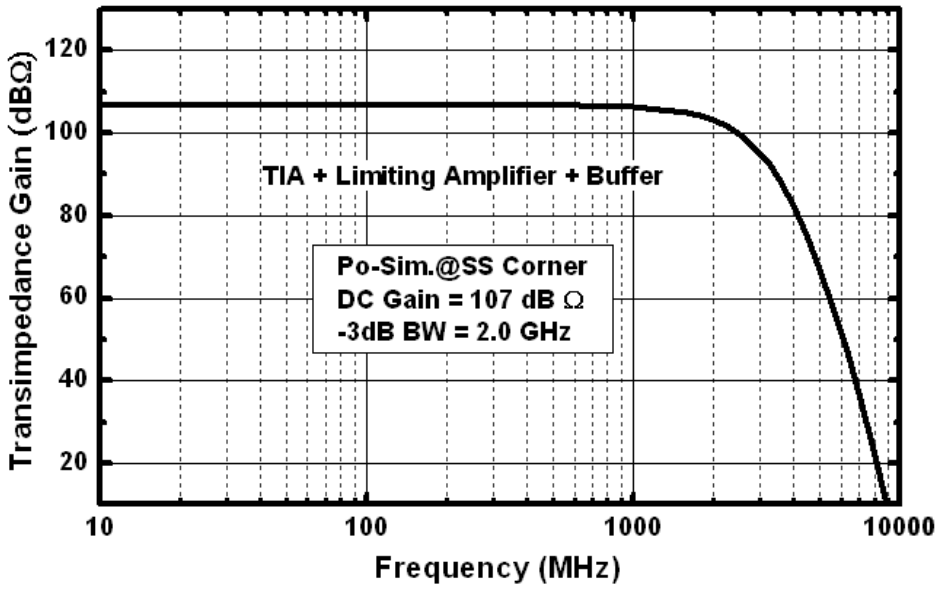


Figure 6-12 Magnitude responses of OEIC with PIN detector.

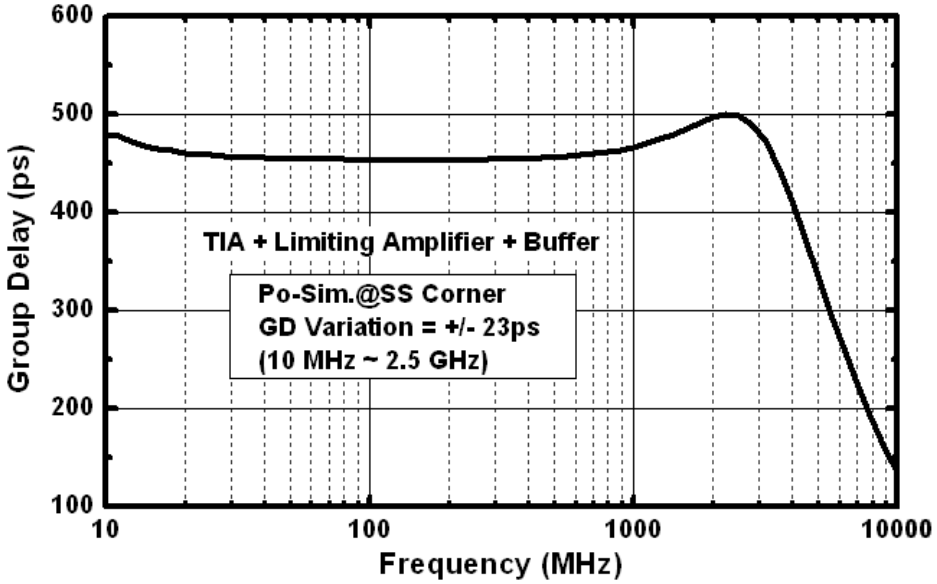


Figure 6-13 Group delay of OEIC with PIN detector.

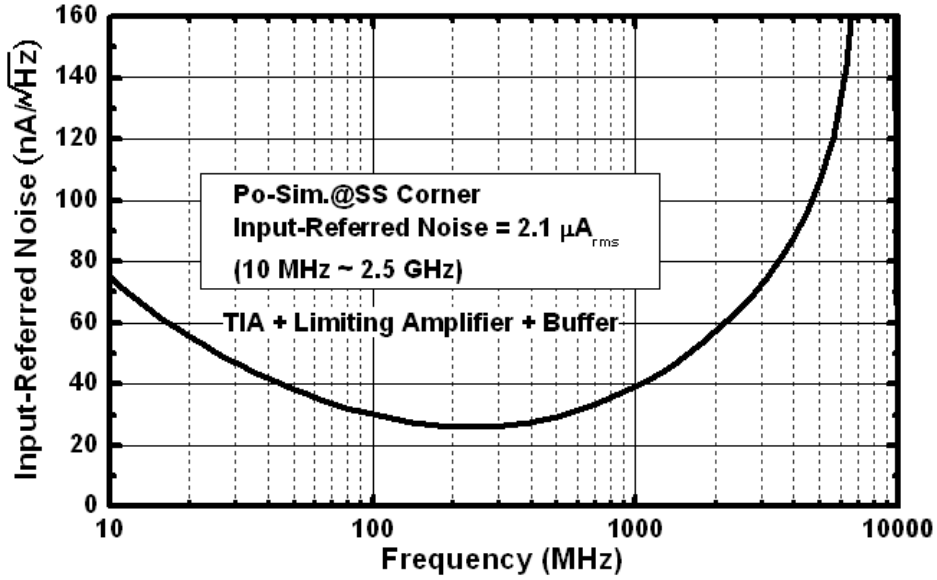


Figure 6-14 Input-referred noise of OEIC with PIN detector.

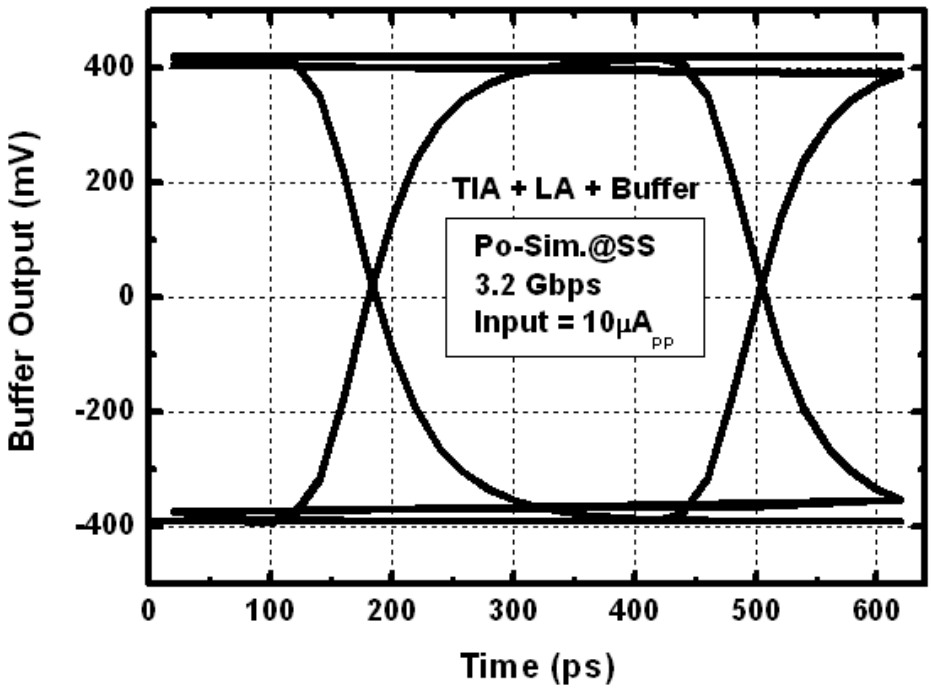


Figure 6-15 Post-Simulated eye diagram for OEIC with PIN detector.

6.2.4 Test Chip

This OEIC is mounted on a printed circuit board for measurement. To measure the sensitivity and eye diagram of this OEIC, the measurement setup is the same as Figure 6-4.

The layout of this optical receiver with PIN detector is shown in Figure 6-16. This chip is implemented by 0.18 μm one-poly six-metal CMOS process, and measured 0.86 μm x 0.62 μm which is dominated by the limiting amplifier. It exhibits 27 I / O pads, and the pad descriptions are listed in Table 5-2. There are 19 pads connected to neither V_{DD} or G_{ND} , 2 pads (#3 and #4) for PD reversed-bias, 3 pads (#1, #2 and #19) connected to large bypass capacitance of 0.1 μF, 2 output pads (#16 and #18) connected to the AC coupling capacitance of 0.1 μF and delivering the output signals to sampling scope, Agilent 86100C, 1 pad (#10) connected to the variable resistance of 20 kΩ to adjust the input biasing current to the correct operating point.

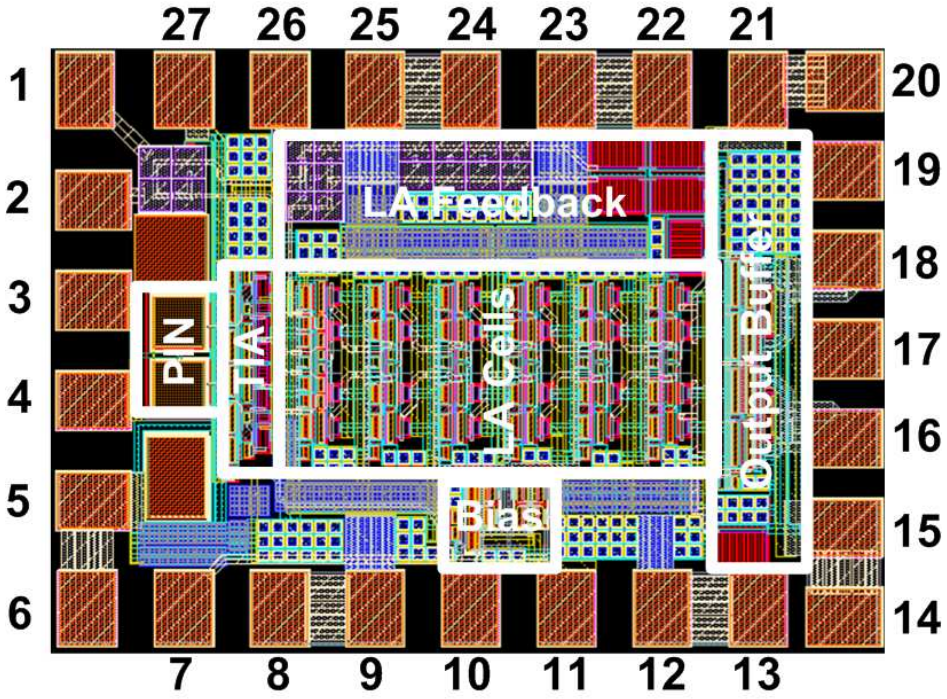


Figure 6-16 Chip layout of OEIC with PIN detector.

Table 6-2 The pad descriptions of OEIC with PIN detector.

PAD #	Description	PAD #	Description
1	V_{FB1}, to bypass capacitance	**15**	Ft-doubler V_{DD}
2	V_{FB2}, to bypass capacitance	**16**	V_{OUT1}, output signal
3	PIN N-well, toV_{PD}	**17**	NMOS body, to G_{ND}
4	PIN N^+diff, toV_{PD}	**18**	V_{OUT2}, output signal
5	NMOS body, to G_{ND}	**19**	V_{LP}, bypass capacitance
6	NMOS body, to G_{ND}	**20**	Ft-doubler G_{ND}
7	PMOS body, to V_{DD}	**21**	Ft-doubler G_{ND}
8	LA G_{ND}	**22**	LA G_{ND}
9	LA G_{ND}	**23**	LA G_{ND}
10	R_{BIAS}, to 20 kΩ variable res.	**24**	LA V_{DD}
11	Biasing Circuit V_{DD}	**25**	LA V_{DD}
12	LA V_{DD}	**26**	TIA V_{DD}
13	LA V_{DD}	**27**	TIA G_{ND}
14	Ft-doubler V_{DD}		

6.2.5 Measurement Results

The TIA and limiting amplifier are operated under 3.3 V and 1.8 V supply, respectively. The total power dissipation is 138 mW, among which 30 mW is consumed by the output buffer. By cascading transimpedance amplifier and limiting amplifier on a single chip, the optical receiver provides a conversion gain of 107 dBΩ. The overall $f_{H\text{-}3dB}$ is limited by the photodetector. It is capable of delivering 800 mV_{pp} differential voltage swings to 50 Ω output loads directly. The chip micrograph is shown in Figure 6-17. Implemented in generic 0.18-μm CMOS technology, the total chip area is about 860 μm by 620 μm.

When the PIN diode is reverse-biased in the low voltage (2 V) and high voltage (6 V) modes, the bit-error-rate performance was summarized in Figure 6-18 and Figure 6-19, respectively. The input sensitivity level of the optical receiver is improved by less than 2 dB for lower speed operation (1.25 Gbps) in the high voltage operating mode, implying that no avalanche mechanism is found in the PIN detector. Also, under high voltage operating mode, the input sensitivity level for bit-error-rate less than 10^{-12} at 1.25 Gbps and 2.5 Gbps are about -10 dBm and -7 dBm, respectively.

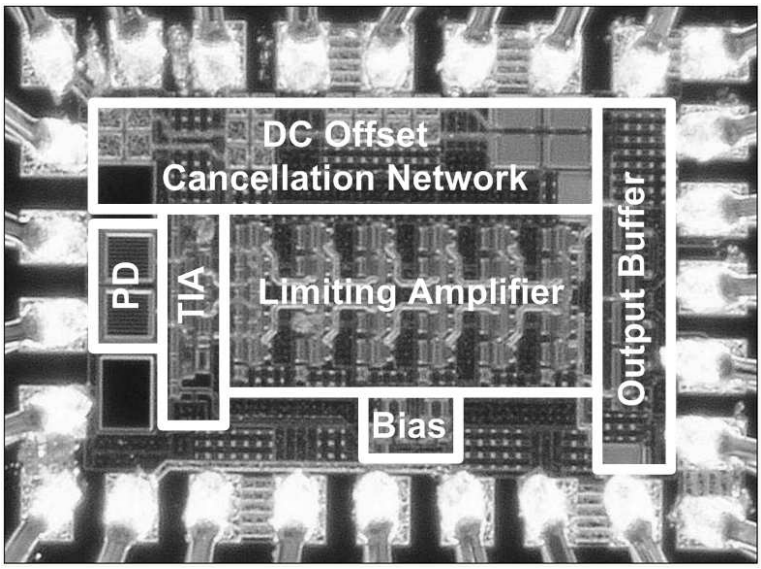


Figure 6-17 Chip micrograph.

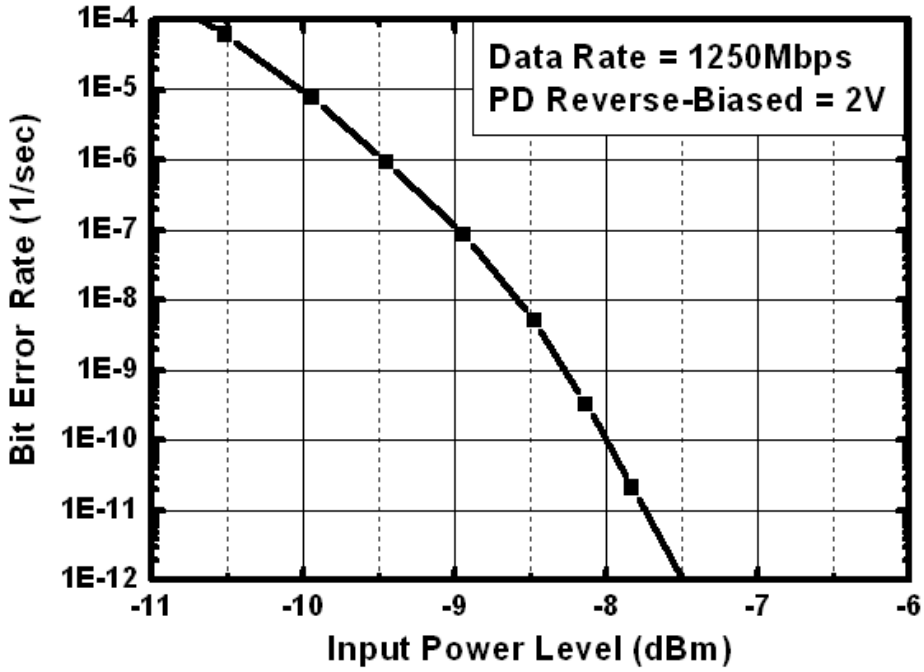


Figure 6-18 Measured BER performance @2V PD reversed-bias.

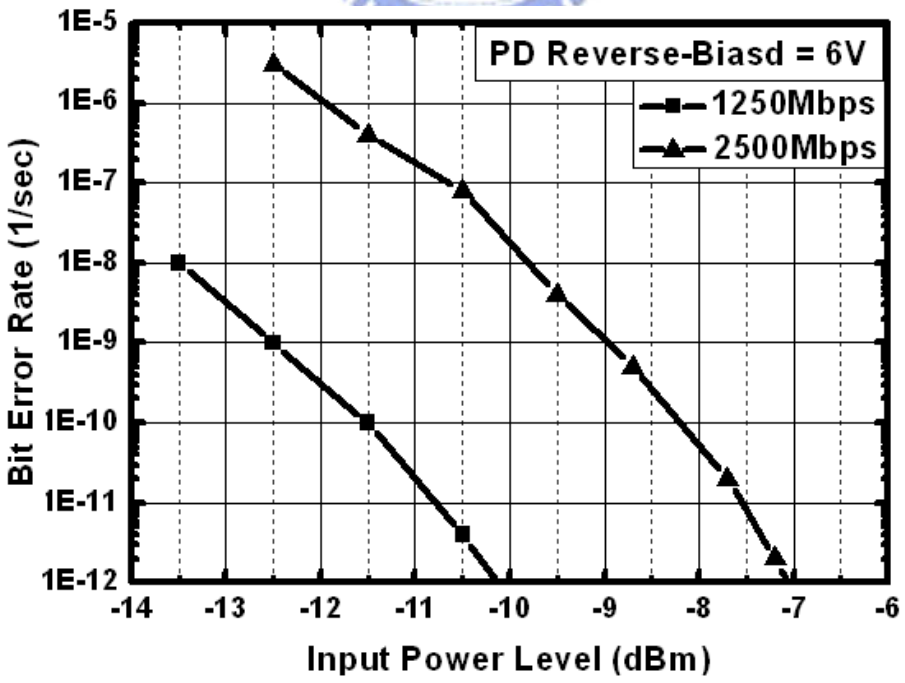


Figure 6-19 Measured BER performance @6V PD reversed-bias.

Figure 6-20 and Figure 6-21 shows the measured eye diagrams in the high voltage operating mode for 1.25 Gbps and 2.5 Gbps with the input sensitivity level -10 dBm and -7 dBm, respectively. The data jitters are about 24.5 ps_{rms} (184.9 ps_{pp}) and 30.96 ps_{rms} (204.44 ps_{pp}), respectively.

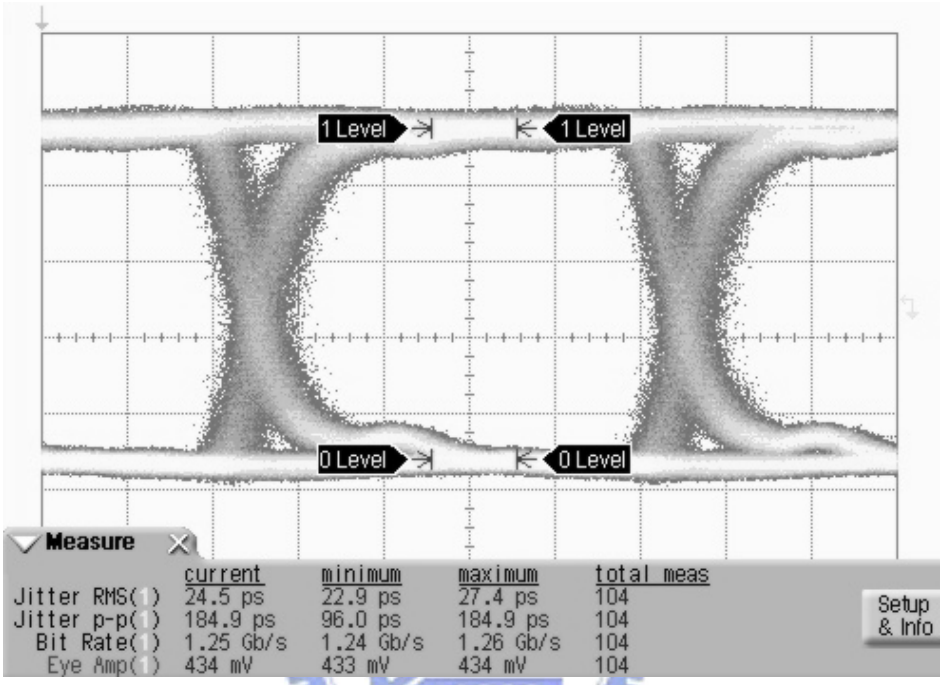


Figure 6-20 Eye diagrams at 1.25 Gbps with sensitivity level, -10 dBm.

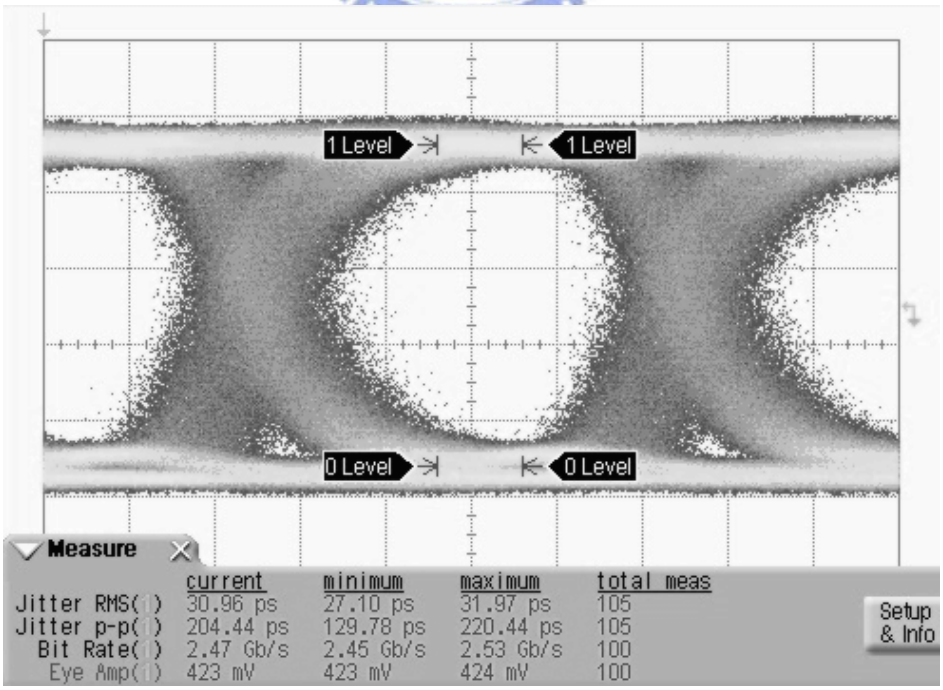


Figure 6-21 Eye diagrams at 2.5 Gbps with sensitivity level, -7 dBm.

Table 6-3 Performance benchmark.

	[6]	[19]	[2]	The 1st Work	The 2nd work
Wavelength	850 nm				
Architecture	PD+TIA+EQ	PD+TIA+LA	PD+TIA+LA	PD+TIA+EQ+LA	PD+TIA+LA
PD Type	N-well / P-sub	N-well / P-sub SML			P^+ / P-well / N^+ PIN
Maximum Speed	3 Gbps	2 Gbps	0.5 Gbps	3.125 Gbps	2.5 Gbps
Sensitivity	-19dBm@3Gbps ($BER=10^{-11}$)	-10dBm@1.25Gbps ($BER=10^{-11}$) -7dBm@2Gbps ($BER=10^{-11}$)	-8dBm@0.5Gbps ($BER=3x10^{-12}$)	-5.8dBm@2.5Gbps ($BER=10^{-12}$) -4.2dBm@3.125Gbps ($BER=10^{-12}$)	-10dBm@1.25Gbps ($BER=10^{-12}$) -7dBm@2.5Gbps ($BER=10^{-12}$)
Power Dissipation	TIA + EQ (34mW) Buffer (16mW)	TIA + LA (34mW) Buffer (17mW)	TIA (17mW) LA (34mW)	TIA (16mW) LA + EQ (129mW) Buffer (30mW)	TIA (16mW) LA (92mW) Buffer (30mW)
Output Swing	N.A.	250 mV_{PP}	100 mV_{PP}	800 mV_{PP}	800 mV_{PP}
Technology	0.18 μm CMOS Technology				

6.3 Performance Benchmark

Table 6-3 summarizes the performances of the state of the art and our own designs. In the row of wavelength, the 850-nm wavelength optical light is used by all of us.

In the row of architecture, the optical receiver integrates the PD, the TIA and LA on a single chip except for [6] in Table 6-3. Since [6] has not integrated the limiting amplifier, it has not shown the output swing voltage in the reported journal. Also, the output swing of our OEICs is larger then [19] and [2] by 3.2 times and 8 times, respectively. Thus, the power consumption of our OEICs is also large, and most of the power is dissipated by the limiting amplifier.

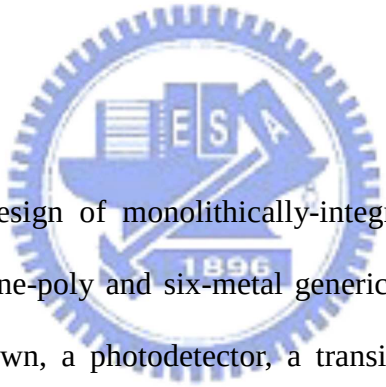
In the row of maximum speed, our OEIC with SML detector is the most high-speed in the table.

Compared with the same SML detector in [19], [2] and our 1st OEIC, the sensitivities are about the same. Nevertheless, [6] has the sensitivity level of -19 dBm with the BER less than 10^{-11} owing to the high responsivity PD and complicatedly equalizer. Because the different equalizers and different weighting in [6], the OEIC may suffer from PVT variation and low yield rate.

Compared to the equalizer of [6], ours only exits a zero which is to compensate the roll-off of the SML detector. Besides, our OEICs are high integrated owing to a PD, a TIA and a LA on a single chip.

Chapter 7

Conclusion



This thesis describes the design of monolithically-integrated optical receiver front-end fabricated in TSMC 0.18μm one-poly and six-metal generic CMOS technology. To achieve small form factor and cost-down, a photodetector, a transimpedance amplifier and a post limiting amplifier are fully integrated in a single chip. Furthermore, the design methodology and implementation techniques of optical receiver were presented. Major research results can be summarized as follows.

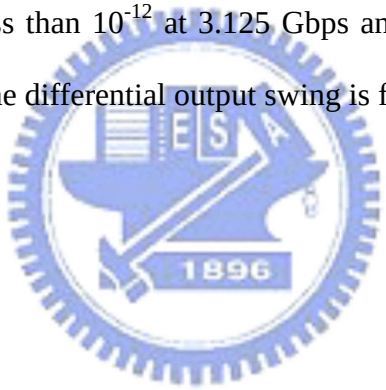
First, two gigabit-per-second photodetectors are implemented for high-speed operation in the optical communication. One is the spatially modulated light (SML) detector consisting of a row of photodetectors alternatively covered and uncovered with light-blocking materials; the other is the novel PIN detector emulated by P^+diffusion / P-well / N^+diffusion interleaved architecture.

Second, a trans-impedance amplifier with high-speed operation is demonstrated. The bandwidth is enhanced by the following techniques. (i) A low input impedance TIA is

implemented by regulated cascode gain stage composed of a common gate amplifier with its gate controlled by a negative local feedback loop. (ii) A Shunt-Shunt feedback technique is adopted to reduce the impedance of each node in TIA.

Third, a limiting amplifier is accomplished. A Cherry-Hooper circuit structure with active feedback is realized to achieve high-speed operation owing to its higher gain-bandwidth product. Further, a f_T-doubler output buffer is designed to reduce the capacitive load to the preceding stage.

Finally, an adaptive equalizer with a zero is incorporated to enhance the system bandwidth. The zero can be adjusted by a feedback control loop which detects the edge slope of signal waveforms. The two OEICs are implemented in a 0.18 μm digital CMOS process, the input sensitivity levels with BER less than 10^{-12} at 3.125 Gbps and 2.5 Gbps are about -4.2 dBm and -7 dBm respectively, and the differential output swing is fixed at 800 mV_{pp}.



Appendix A

PCB Layout

Figure A-1 shows PCB layout by using Allegro, and Figure A-2 shows the board measured 60 mm x 42 mm with all the components soldered as well. The critical high-speed output signal paths are routed as short as possible to reduce the parasitic capacitance on the PCB.

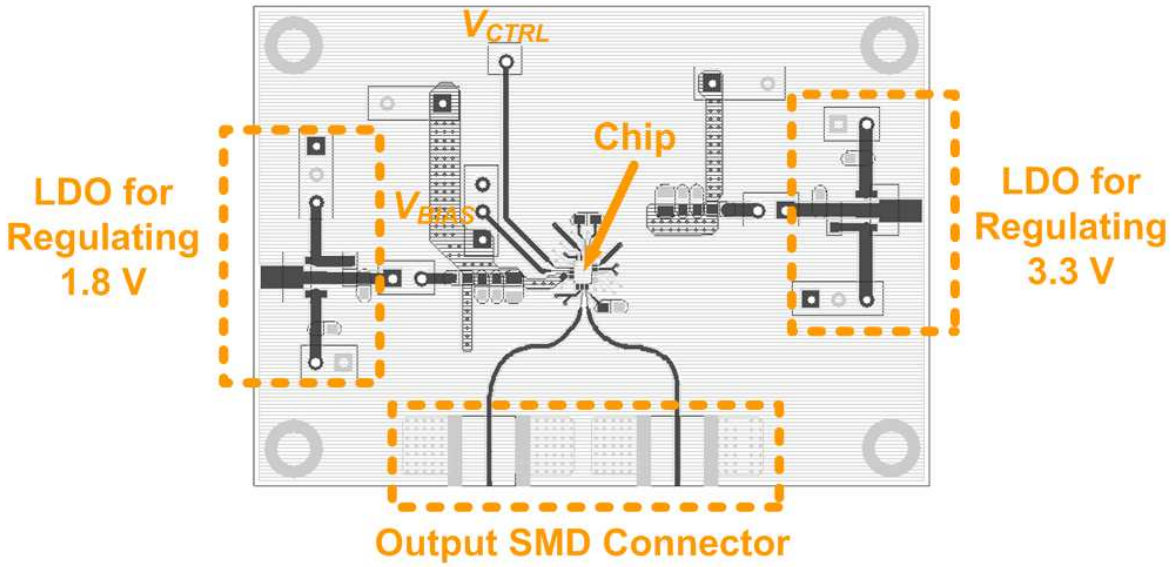


Figure A-1 Top layer of the PCB layout composed of 4 layers with RF-4.

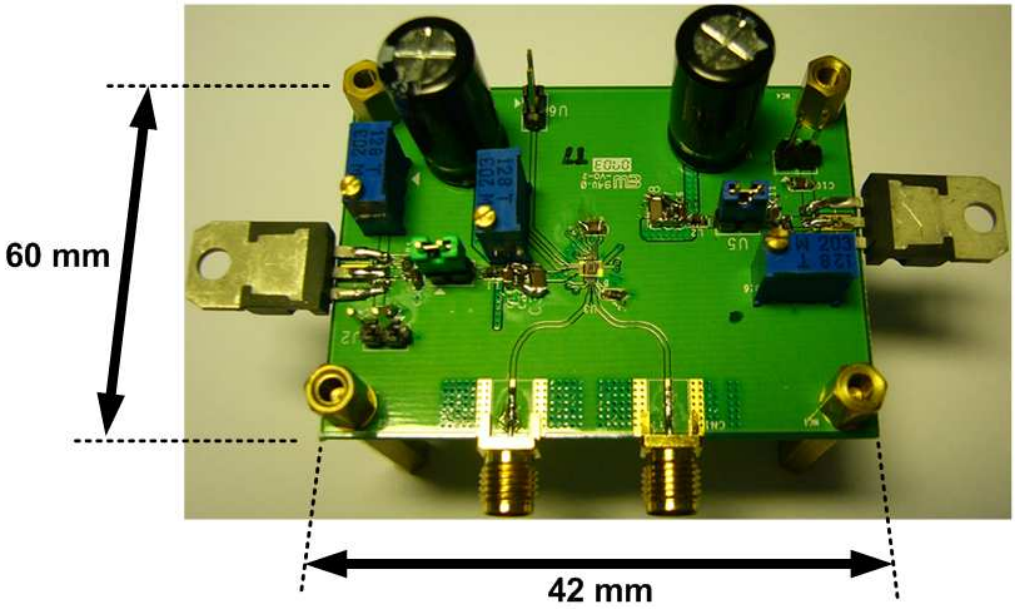


Figure A-2 The PCB photograph measured 60 mm x 42 mm.

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