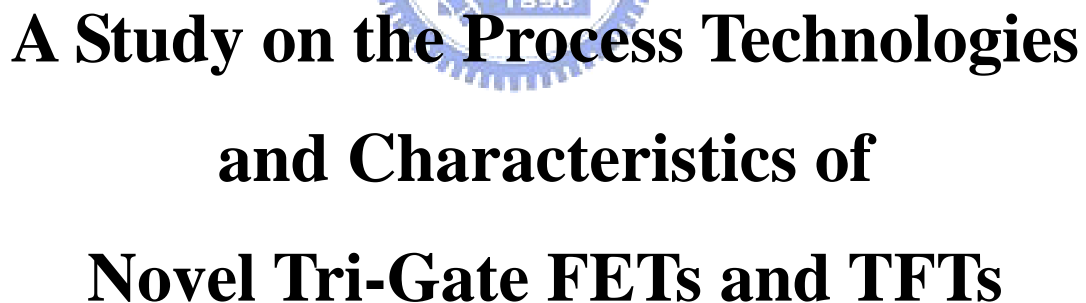
國 立 交 通 大 學

電子工程學系電子研究所

博 士 論 文

新穎三閘極電晶體與薄膜電晶體之製程技術與特性研究



A Study on the Process Technologies and Characteristics of Novel Tri-Gate FETs and TFTs

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中華民國 九十五 年　四 月

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博士論文

A Dissertation

Submitted to Department of Electronics Engineering
and Institute of Electronics
College of Electrical Engineering and Computer Science
National Chiao-Tung University

In Partial Fulfillment of the Requirements

for the Degree of
Doctor of Philosophy
in Electronics Engineering
2006
Hsinchu, Taiwan, Republic of China

中華民國 九十五 年 四 月

新穎三閘極電晶體與薄膜電晶體
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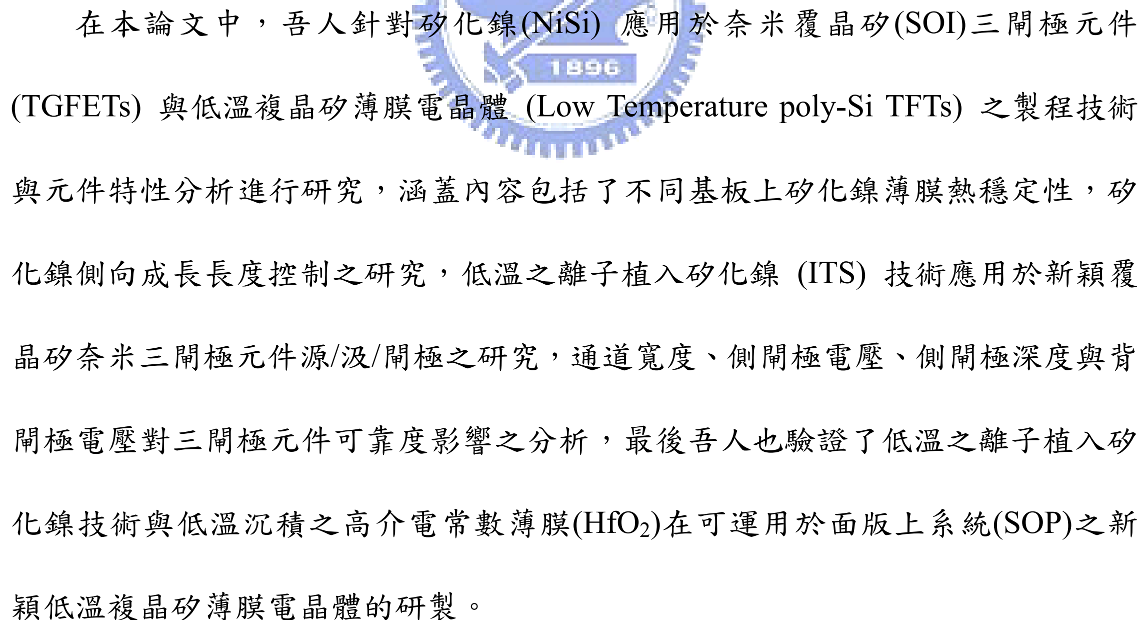
摘要



在本論文中，吾人針對矽化鎳(NiSi) 應用於奈米覆晶矽(SOI)三閘極元件(TGFETs) 與低溫複晶矽薄膜電晶體 (Low Temperature poly-Si TFTs) 之製程技術與元件特性分析進行研究，涵蓋內容包括了不同基板上矽化鎳薄膜熱穩定性，矽化鎳側向成長長度控制之研究，低溫之離子植入矽化鎳 (ITS) 技術應用於新穎覆晶矽奈米三閘極元件源/汲/閘極之研究，通道寬度、側閘極電壓、側閘極深度與背閘極電壓對三閘極元件可靠度影響之分析，最後吾人也驗證了低溫之離子植入矽化鎳技術與低溫沉積之高介電常數薄膜(HfO_2)在可運用於面版上系統(SOP)之新穎低溫複晶矽薄膜電晶體的研製。

首先，在本論文中，我們驗證了在氧化矽基板(SiO_2) 上之矽化鎳薄膜，因無多餘之矽成分，所以有較佳之熱穩定性。同時，運用了特殊之四端點片電阻測試結構也驗證了運用兩階段退火方式可以有效控制矽化鎳之側向成長長度。

其次，我們更將低溫兩階段退火(300°C+600°C)的矽化鎳薄膜與低溫離子植入矽化鎳 (ITS) 製程運用於新穎 25 奈米覆晶矽三閘極元件之源/汲極部分。此新穎元件有數個優異之製程與電特性：(1) 因為運用了兩階段式退火，可以有效的控制矽化鎳之側向成長至邊壁 (spacer) 之下方，避免了矽化鎳過度成長。(2) 而運用了離子植入矽化鎳技術可以避免了離子植入對通道矽之損傷，降低離子活化熱製程 (600°C, 30min)，有降低漏電流之優點。(3) 此外，修正矽化鎳之蕭基特位障(modified Schottky-barrier)源/汲極接面可提升元件之驅動電流(driving current)與降低漏電流之功效。

此外，我們也針對三閘極元件可靠度進行分析。發現當通道寬度(channel width)縮小時，不但側向閘極 (side-gate) 電壓可以有效的降低通道電場與分散熱電荷之方向，較平整之矽化鎳前緣亦有改善元件可靠度之功用。而較深之側向閘極深度與較窄之通道寬度結構也可以遮蔽來自背閘極電壓之電場亦可有效降低底部氧化層 (buried oxide) 內部電荷與介面電荷對元件可靠度造成之影響。

其次，為了減少復晶矽空乏效應對元件特性退化之影響並簡化製程步驟。我們提出了新型全矽化鎳閘極修正蕭基特位障源/汲極覆晶矽元件(FUSI MSB FD-SOI)。此新型元件具有(1) 可消除復晶矽空乏效應。(2) 可同步利用低溫離子植入矽化鎳技術於源、汲、閘極工程。(3)運用離子植入矽化鎳技術不但可以改變了閘極之功函數(work function) ，同時可以與修正蕭基特位障源/汲極製程相容，以簡化製程步驟。對運用於未來之高速元件與高頻電路中相深具潛力。

接著，我們也驗證了低溫離子植入矽化鎳技術可以進一步運用於低溫複晶矽薄膜電晶體之源/汲極工程之製作。由製程角度觀之，低的熱運算可以增加產能；而由電特性角度觀之，可有效降低源/汲極寄生阻抗 (1.35KΩ-cm)並同時提升薄膜

電晶體之開關電流比、開關速度、工作電壓、電子遷移率以及可靠度等特性。此外，優異的短通道特性 (Short channel effect) 更是適合應用於奈米級之低溫複晶矽薄膜電晶體。

最後，我們也製作出了一種新型的具低溫沈積之高介電常數介電層複晶矽薄膜電晶體 (HfO_2 TFTs)。其運用了低溫成長(400°C)之氧化鉿薄膜(HfO_2) 為閘極介電層，可以有效的降低了有效氧化層厚度 (EOT) 至 7.3 奈米。故與傳統之薄膜復晶矽電晶體相比較，其顯示較佳的元件電特性：開關電流比接近 10^7，快速的開關特性 (S.S.~0.28V/Dec)、低閘極電壓 (0.3V) 等特性。與奈米等級通道寬度多閘極結構相結合應用後亦極適於運用於未來之面板上系統 (SOP)。

A Study on the Process Technologies and Characteristics of Novel Tri-Gate FETs and TFTs

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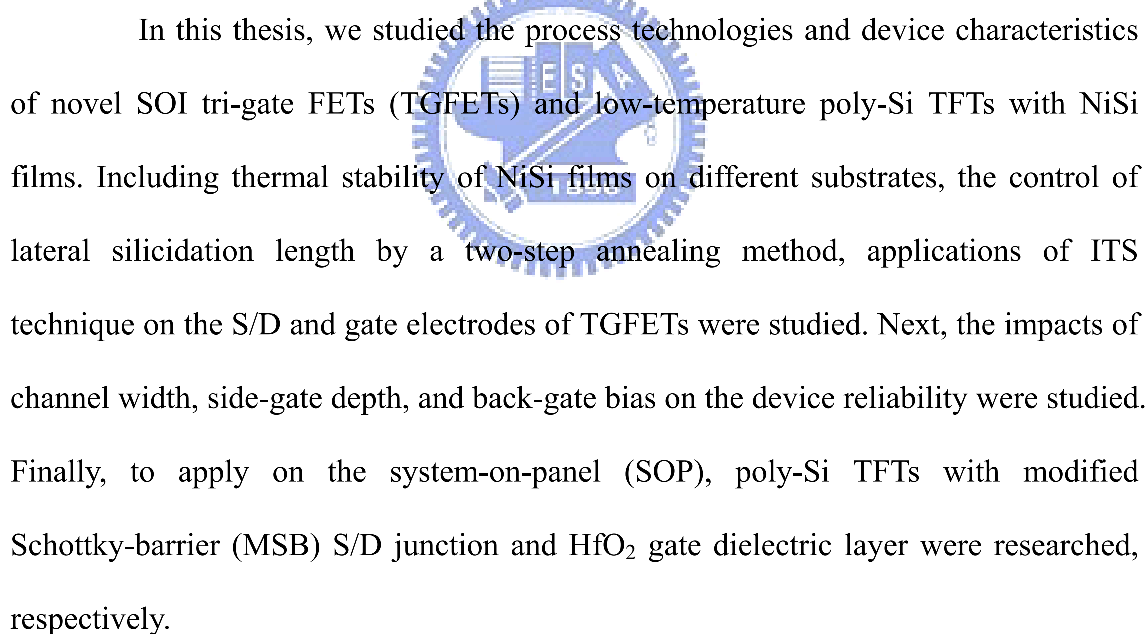
Abstract



In this thesis, we studied the process technologies and device characteristics of novel SOI tri-gate FETs (TGFETs) and low-temperature poly-Si TFTs with NiSi films. Including thermal stability of NiSi films on different substrates, the control of lateral silicidation length by a two-step annealing method, applications of ITS technique on the S/D and gate electrodes of TGFETs were studied. Next, the impacts of channel width, side-gate depth, and back-gate bias on the device reliability were studied. Finally, to apply on the system-on-panel (SOP), poly-Si TFTs with modified Schottky-barrier (MSB) S/D junction and HfO_2 gate dielectric layer were researched, respectively.

First of all, we demonstrated that the NiSi films on the SiO_2 substrate, without the excess Si atoms, have superior thermal stability. At the same time, using a special four-terminal sheet resistance test structure, the two-step annealing method was also found to well control the lateral silicidation length.

Next, a novel 25nm modified-Schottky-barrier (MSB) SOI TGFET with

NiSi S/D electrodes was fabricated by the low temperature two-step (300^oC+600^oC) NiSi silicidation and ITS technique. In this MSB TGFETs, low S/D external resistance, well-controlled NiSi profile, low temperature activation process, low S/D leakage current, and the high driving current owing to the MSB junction fabricated by ITS technique were also demonstrated.

Besides, the reliability issues of TGFETs were also detail investigated. As the channel width reduces, not only the side-gate bias could effectively reduce the electric field in the channel and disperse the direction of hot-carriers, but the flatness of narrow silicide front-end was also another plausible reason that the device reliability could be enhanced. Moreover, deeper side-gate depth (D_{EXT}) with narrower channel width structure was also demonstrated to shield the electric field from back-bias and then relaxed the influence of defects in the interface and bulk region of buried oxide.

To solve the device performance degradation caused by poly-Si gate depletion effect while simplify the fabrication process, we also suggested the novel FUSI gate structure on the MSB FD-SOI devices by the same ITS technique. Using the ITS technique, the S/D and gate electrode could be fabricated easily at the same time. During this process, the poly-gate depletion could be suppressed; the work function could be suitable tuned. More important, this gate electrode engineering could be compatible with the fabrication process of MSB S/D junction. To conclude, these novel devices could be applied on high-speed device and radio-frequency circuits.

In this thesis, we also illustrated the ITS technique on the fabrication of S/D electrodes of low-temperature poly-Si TFTs. For fabrication process, because of the low thermal budget, the throughput could be improved effectively. For electrical characteristics, smaller S/D parasitic resistance, larger I_{on}/I_{off} current ratio, smaller subthreshold swing, smaller operation voltage, higher effective field mobility, and

stable reliability were approached. Moreover, because of the superior short channel characteristics, the novel FSD TFTs were suggested to scale down to the nano-scale regime.

Finally, a novel poly-Si TFT using a low-temperature and thin high-k (HfO_2) film as gate dielectric was fabricated. In this device, the effective oxide thickness (EOT) could be scaled down to 7.3nm, and low gate leakage current could be maintained. The electrical characteristics including I_{on}/I_{off} (~10^7), subthreshold swing (~0.28V/Dec), and threshold voltage (0.3V) were also approached. Combining the HfO_2 gate dielectric with thin EOT and the ultra-narrow channel width structure, the novel HfO_2 TFT was also verified to the future system-on-panel (SOP) applications.

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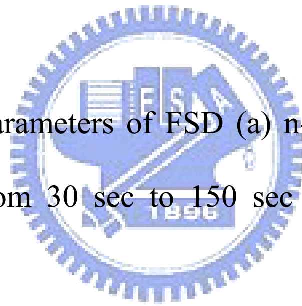

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Chapter 5

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Fig.5-5 Transfer characteristics of n-TGFETs with L_g=130nm, W_f=40nm, and T_{Si}=40nm and various V_b increases from -21V to 21V (step=1V).

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Chapter 6

Fig.6-1 Key fabrication process steps of n-and p-channel FUSI-ITS-gate MSB FD-SOI devices.

Fig.6-2 Key fabrication process steps of n-and p-channel polycide-gate MSB

FD-SOI devices.

Fig.6-3 Schematic figures of (a) FUSI-ITS-gate, (b) polycide-gate MOS capacitance structures.

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Fig.6-14 Comparisons of driving currents for n-channel FUSI-ITS and polycide MSB FD-SOI devices with $L_g/W=1\mu m/1\mu m$.

Chapter 7

Fig.7-1 Key fabrication steps OF the proposed FSD TFTs.

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Fig.7-5 Typical transfer characteristics of SB n- and p-TFTs after NH_3 plasma treatment.

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Fig.7-16 (a)Cross-sectional TEM figure of FSD TFTs after 750°C for 30seconds activation. (b) and (c) are the EDX analysis data of point “A” and “B” in (a).

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Fig.7-18 Extraction of R_{Sh} of S/D/G electrode after 600 ºC for 30, 90, and 150 sec annealing.

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Fig.7-20 Driving current degradation of FSD and CN n-TFTs with the stress gate voltage. The stress conditions are at V_{ds}=20V and various V_g from 6 to 26V with step is 2V.

Fig.7-21 Forward mode transfer characteristics of (a) FSD and (b) CN n-TFTs before and after hot-carrier application. The stressing conditions was Vg=6V and V_{ds}=20V for a stress time of 3600s. The size of TFT W/L=5μm/5μm.

Fig.7-22 Reverse mode transfer characteristics of (a) FSD and (b) CN -TFTs before and after hot-carrier application. The stressing conditions was Vg=6V and V_{ds}=20V for a stress time of 3600s. The size of TFT W/L=5μm/5μm.

Fig.7-23 Time dependence of forward mode maximum transconductance ($\Delta G_m/G_m$) degradation of FSD and CN n-TFTs after various hot-carrier stressing time. The stressing conditions was V_g=6V and V_{ds}=20V for a stress time of 3600s. The size of TFTs W/L=5μm/5μm.

Fig.7-24 Forward mode transfer characteristics of (a) FSD and (b) CN nTFTs before and after self-heating application. The stressing conditions was V_g=20V and V_{ds}=20V for a stress time of 3600s. The size of TFT W/L=5μm/5μm.

Fig.7-25 Reverse mode transfer characteristics of (a) FSD and (b) CN n-TFTs before and after self-heating application. The stressing conditions was V_g=20V and V_{ds}=20V for a stress time of 3600s. The size of TFT W/L=5μm/5μm.

Chapter 8

Fig.8-1 Key fabrication process of HfO_2 poly-Si n-TFTs.

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Fig.8-5 (a) Output and (b) transfer characteristics of HfO_2 and SiO_2 n-TFTs with L_g=1mm and W_g=0.1mm after a 30min NH_3 plasma treatment.

Fig.8-6 The V_{th} roll-off phenomena of n-TFTs (W_g=1μm) with HfO_2 ($T_{phys.}$=27.7nm) and SiO_2 ($T_{phys.}$=25nm and 45nm).

Fig.8-7 Transfer characteristics of HfO_2 n-TFTs with a fixed L_g=1μm and three different channel width (W_g) of 1μm, 0.3μm to 0.1μm was measured at V_{ds}=0.1V.

Fig.8-8 (a) I_{on} and I_{off}, (b) G_m and S.S. and (c) V_{th} variations of HfO_2 n-TFTs with a fixed L_g=1μm and various channel width.

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Chapter1

Introduction

1-1 The Evolution of CMOS

In 1963, the first CMOS circuit was invented by Frank Wanlass [1-1]. Then, some twenty-five years latter, it became the predominant technology in very large scale integrated circuits. To approach the benefits such as high performance, high operation speed, high device density, low power consumption, and low manufacturing costs, the dimension downsizing of CMOS becomes the principled trend for the last few decades. This trend basically traced back to the Moore's Law, the observation by Gordon Moore in 1965 , which was often stated as the doubling of transistor performance and quadrupling of the number of devices on a chip every three years [1-2]. Following the Moore's law, by 1992, the Semiconductor Industry Association (SIA) has been first published the technology roadmap for semiconductors. This roadmap represents a consensus outlook of industry trends, taking history as a guide. In 2003, the roadmap pointed out that the technology will step to 45 nm node beyond 2010, as shown in Fig.1-1 [1-3]. It is well known that the major challenges of extending CMOS beyond 45nm node are the suppression of poor short-channel effects (SCE) attributed to the insufficient gate-controllability and the abnormal large leakage current due to the ultra-thin gate dielectric. Therefore, to alleviate these issues, two avenues have been suggested: new non-classical structures and new materials.

Non-classical CMOS structure includes transport-enhancement FETs,

ultra-thin-body (UTB) SOI FETs, and 3-dimensional structure FETs (3D FETs) such as double-gate FETs and multi-gate FETs (MGFETs) [1-3]. In the transport-enhancement FETs, the carrier mobility could be enhanced by the mechanical strain in the channel layer or by the judicious choice of crystal orientation and current transport direction [1-4]. However, material defects, junction leakage current, process compatibility, and operating temperature are still issues. For the UTB SOI FETs, the ultra-thin lightly-doped body could effectively reduce the leakage current while enhance the driving capability. Nevertheless, the requirement of low-defect ultra-thin body and controllability of threshold voltage (V_{th}) are still problems [1-5]. Quantum confinement also limits the improvement in performance. Therefore, 3D FETs including double-gate FETs (such as FinFETs) and MGFETs (such as tri-gate FETs) attracted many attentions in these years [1-6]-[1-7]. Especially, MGFET is the plausible solution beyond the 45nm technology node.

1-2 Why Multi-Gate FETs?

Why the multi-gate FET (MGFETs) is the most attractive candidate structure beyond the 45 nm technology node ? Taking the tri-gate FET (TGFET) as an example, although the fully-depleted SOI transistors have the advantages resided in the simplicity of the process (close to bulk planar process), the compactness of the layout (same as for bulk planar), and competitive with a similarly-scaled, aggressive bulk CMOS technology at the same technology node. Nevertheless, to scale the dimension of the active silicon channel region of the fully-depleted (FD) SOI transistors is still the major challenge [1-8]. In the case of single-gate FDSOI devices, the silicon body thickness (T_{Si}) needs to be about a third of the electrical gate length in order to maintain full substrate depletion under gate control [1-9]. Moreover, the

threshold voltage (V_{th}) could also be affected by the Si thickness variation [1-10]. Scaling this device to 30 nm gate length dimensions, for example, requires a 3σ-thickness uniformity of 1 nm on a silicon film thickness of 10 nm, which is presently hard to achieve.

Double-gate FET is one of the 3D FET structures, the typical one is the FinFET, in which the current flows horizontally (parallel to the plane of the substrate) between the source and drain along the two opposite vertical channel surfaces. The width of the vertical silicon fin should be narrow (smaller than the channel length) to provide adequate control of the SCE.

A lithographically defined gate straddles the fin, forming self-aligned, electrically connected gate electrodes along the sidewalls of the fin. The principal advantage with this structure is the planar bulk-like layout and process compatibility. The major challenge is the width of the thin fins should be thicker than a half of the gate length.

To further relax the gate length constrain of FinFETs, TGFETs were simulated and fabricated [1-11]-[1-13]. They have not only been reported to show fully depleted behavior at thickness dimension greater than that of the single-gate FD SOI and FinFET, but also relaxes the acquirement of high Si fin etching process of FinFETs and of the active layer thickness uniformity of single-gate FD SOI devices. Therefore, the TGFET has emerged as a very promising candidate among single-, double-, and multi-gate ones in the end of ITRS roadmap. The comparison among the 3D FETs are summarized in Table.1-1 [1-3].

1-3 Modified-Schottky-Barrier (MSB) TGFETs

Although the TGFET has been considered as a candidate structure beyond

45nm technology node, some technical problems such as shallow source/drain (S/D) junction formation, the source/drain and gate (S/D/G) electrode parasitic resistance (R_p) reduction, and the process temperature compatibility between the high-dielectric constant dielectric (high-κ) and S/D activation still exist. In conventional bulk CMOS, to suppress the large R_p at S/D electrode, many silicide technologies have been suggested in the past twenty years. However, the silicidation of S/D region is a great-skill work. Improper silicidation scheme may result in unacceptable high leakage current due to the numerous consumption of the heavily doped regions [1-15]. The resultant I-V characteristics and contact resistance may be degraded. Furthermore, it is very hard to fabricate sub-0.1μm junctions by means of conventional high temperature activation process [1-16]. On the other hand, Schottky barrier source/drain structure has been suggested in 1994 by J. R. Tucker et al., [J. R. Tucker, APL, p.618, 1994], and have been demonstrated to release the acquirement of R_p and preserve the short extension length [1-14]. Nevertheless, not only the abnormally high contact resistance attributed to the Schottky-barrier (SB) junction at source-side can degrade the driving capability, but the small SB at drain-side also results in high off-state leakage current [1-17].

Therefore, to solve those problems, in this thesis, the implant-to-silicide (ITS) technique is suggested to fabricate nano-scale TGFETs. This ITS technique has been proposed as a promising solution to form sub-0.1 shallow junctions at low temperature and has been investigated widely in the 90' decade [1-18]-[1-21]. It uses a silicide film to act as an ion-implantation damage basin and thus the process temperature can be greatly reduced. The silicide film also acts as an energy barrier for the implanted ions and thus shallow junctions can be obtained using the implanted silicide film as solid diffusion source. This merit is especially important and useful for

p^+n junctions because boron is a very light element and is a fast diffuser in silicon.

1-4 ITS Technique on Fully-Silicide Gate Electrodes

To suppress the SCE while control the V_{th} well, except the device structure modification such as TGFETs and Schottky-barrier S/D, the gate controllability enhancement by metal gate electrode and high-κ gate dielectric are also possible solutions [1-22].

Recently, fully silicided poly-Si (FUSI) gate has been proposed to replace the conventional doped poly-Si gate to solve the gate depletion problem while release the thermal stability issue of high-κ gate dielectric [1-23]. From the characteristics perspective, Ni-silicide FUSI gate has several advantages such as low-silicidation temperature, low sheet resistance, low stress and an intrinsically mid-gap workfunction (WF) [1-24].

Recently, the ITS process has been demonstrated as an effective method to adjust the work function of Ni-FUSI gate while removing the NiSi phase and crystal orientation influences [1-25]-[1-26]. In order to preserve the advantages of Ni-FUSI gate while simplify the process integration and stabilize the work function, integrate FUSI gate and MSB S/D structure by ITS process on FD-SOI devices should be an ideal approach. Consequently, not only the NiSi gate work function could be adjusted by the dopant piled-up at the interface between the NiSi/gate dielectric, the low S/D parasitic resistance could also be preserved. Moreover, the process issues such as implantation damage of gate dielectric, the S/D/G silicidation depth, and the thermal budget consideration are all effectively improved.

1-5 ITS Technique on Poly-Si TFTs

Besides the CMOS, poly-Si thin-film transistor is another important and popular semiconductor device to be applied to the active-matrix-driven flat panel display (FPD). To enhance the switching characteristics while reduce the amount of external interconnections, pixel-driving circuits monolithically integrated on the display panel substrate to form the system-on-panel is the future trend [1-27]. In order to integrate peripheral driving circuits on the same glass substrate, a low-temperature process (~600°C) without compromising device performance should be developed. The conventional long post-ion-implantation annealing used to activate dopants and remove implantation damages is carried out in a furnace system at around 600°C for 12-24 hours after the source/drain implantation [1-28]. This is an unacceptable thermal budget.

On the other hand, the use of a thinner active layer to obtain higher driving current, lower off-state leakage current, and superior short channel characteristics has been reported [1-29]-[1-30]. Because of the temperature restriction and the thin active layer structure, the high R_p from thin source/drain (S/D) regions would degrade device performance such as driving capability and effective field effect mobility (μ_{FE}). To reduce the S/D R_p of poly-Si TFTs while preserve the benefit of thin-active layer structure and restrict the process beyond 600°C, also it is possible to apply the NiSi and ITS technique to form S/D electrode to the poly-Si TFTs and named fully-silicided S/D TFTs (FSD TFTs). Similar to the MSB TFGET, this novel FSD TFT (FSD TFT) structure has the fully-silicided source/drain and ultra-short source/drain extension (SDE) at the interface of silicide and inverted channel by the implant-to-silicide (ITS) technique. Forming a fully silicided source/drain by the low

temperature self-aligned salicide technique, the R_p of FSD TFTs can be decreased dramatically. Adding an extension doping in the silicon by the ITS technique at about 600°C not only drastically improves the contact resistance at the Ni-silicide/poly-Si junction but also abbreviates the source/drain extension length and avoids the silicide spiking effect.

To further enhance the switching characteristics of poly-Si TFTs, similar to the CMOS process, a thin and high-quality gate dielectric layer is required for future poly-Si TFTs. A major problem in gate dielectric layer on the poly-Si TFTs is local breakdown due to the rough silicon surface [1-31]. Because of this problem, gate dielectric layer on the poly-Si TFTs has to be deposited thicker than necessary to overcome the surface roughness, which reduces TFT drivability. For TFTs with a sub-micron scale, a thick gate dielectric could also degrade the other electrical characteristics. Recently, hafnium dioxide (HfO_2) becomes a candidate of future high-κ gate dielectric material in MOSFET due to its high κ value (15~25), wide bandgap, and acceptable band alignment [1-32]-[1-33]. Therefore, we also use HfO_2 as gate dielectric layer of poly-Si TFTs for the first time.

1-6 Thesis Organization

In the first chapter of this dissertation, we briefly review the revolution of the novel nano-CMOS and the shortcomings of current poly-Si TFTs technology. For CMOS, the advantages and necessity of integrating TGFETs structure, NiSi material, and ITS technique are also stated. For poly-Si TFTs, we also suggested that the fully silicided S/D and HfO_2 gate dielectric could effectively improved the device characteristics.

To implement and verify these concept, in chapter 2, a thorough study on

the characteristics of NiSi line including the sheet resistance and lateral silicidation rate are performed. The thermal stability of NiSi on four different substrates, amorphous-Si, poly-crystalline-Si, crystalline-Si, and silicon dioxide, are also demonstrated for the first time.

In chapter 3, the fabrication process and electrical characteristics of the proposed novel TGFETs featuring with modified-Schottky-barrier (MSB) S/D structure are demonstrated. The MSB S/D process not only lowers the S/D process temperature, but also reduces the R_p of S/D/G electrodes. Moreover, because of the ultra-low activation temperature, the ultra-shallow S/D extension length could be controlled easily and the proposed devices have better electrical characteristics than that with conventional implantation and activation technology.

In chapter 4, the reliability characteristics of n- and p-channel MSB TGFETs are investigated in detail. As devices scale down, the immunity of hot-carrier stress for n-channel and negative-bias-temperature stress for p-channel devices became significantly. However, for the TGFETs with ultra-nano fin width and multiple gate electrodes, the degradation phenomenon and mechanisms are very different from those of the conventional CMOS. In the chapter 4, the relationship among the reliabilities, fin width, and silicide front-edge roughness will be discussed.

In chapter 5, we extend the reliability studies of n-channel TGFETs to the back gate bias (V_b) effect. Because of the poor qualities of buried oxide in the SIMOX wafer, the V_b effect not only affects the basic I-V characteristics of SOI devices, the reliability characteristics are also influenced seriously. In this chapter5, we demonstrate that for the TGFET with narrow fin width, the effects of V_b effect on I-V characteristics and reliabilities could be relaxed by the small bottom interface area between Si fin/buried oxide and the electrical field shielding effect by the side-gate

extension length.

In chapter 6, the fabrication process and electrical characteristics of n-and p-channel FD SOI devices featuring with the fully-silicide gate electrode (FUSI) and MSB S/D electrode using the ITS technique are demonstrated for the first time. It is confirmed that the FUSI gate can eliminate the poly-depletion effect. Moreover, using the ITS technique to the FUSI gate not only relax the thermal stability issues of high-k gate dielectric, but also adjust the work function effectively.

In chapter 7, we report the process and characteristics of FSD poly-Si TFTs. The same advantage of higher driving current due to the low S/D resistance as the conventional salicide TFTs is obtained. The effects of process conditions on electrical characteristics of the proposed devices are discussed thoroughly. Besides, the hot-carrier characteristics of the proposed FSD poly-Si TFTs are also addressed.

In chapter 8, we integrate poly-Si TFTs with HfO_2 gate dielectric. The characteristics of the HfO_2 TFTs are described and compared to the conventional SiO_2 TFTs with the same physical gate dielectric thickness. The recorded effective gate oxide thickness of 7.314nm for poly-Si TFT is demonstrated. Both the NH_3 plasma treatment and narrow width effects numerously improve the characteristics of the HfO_2 TFTs.

Finally, in the chapter 9, we summarize important conclusions achieved in this dissertation. Some future works worthy to study continuously are recommended.

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Table1-1 Comparisons of non-classical CMOS.

Device types	**Transport-enhanced FETs**	**UTB-SOI FET**	**FinFETs**	**TGFETs**
Advantages	High mobility	1.Improved 2.subthreshold slope No floating body	1. Higher drive current 2. Improved subthreshold slope 3. Improved short channel effect	1.Higher drive current 2.2x thicker fin allowed
Particular Strength	High mobility without change in device architecture	1.Low diode leakage 2. Low junction capacitance 3. No significant change in design with respect to bulk	Relatively easy process integration	Thicker Si body possible
Potential Weakness	1. Material defects & diode leakage 2. Process compatibility & thermal budget 3.Operating temperature	1.very thin silicon required with low defect density 2. V_{th} adjustment difficult 3. Selective epi required for elevated S/D	1. Fin thickness less than the gate length 2. Fin shape & aspect ratio	1.Limited device width 2.Corner effect
Scaling Issues	Bandgap usually smaller than Si	Control of Si film thickness	Sub-lithographic fin thickness required	Sub-lithographic fin thickness required
Impact on I_{on}/I_{off}*@	Improved by 20–30%	Improved by 15–20%	Improved by 20–30%	Improved by 20–30%
Impact on CV/I*@	Lowered by 15–20%	Lowered by 10–15%	Lowered by 15–20%	Lowered by 15–20%

***=from MASTAR assuming $E_{eff}/2$ and S.S.=65mV/Dec, @=compare to bulk**

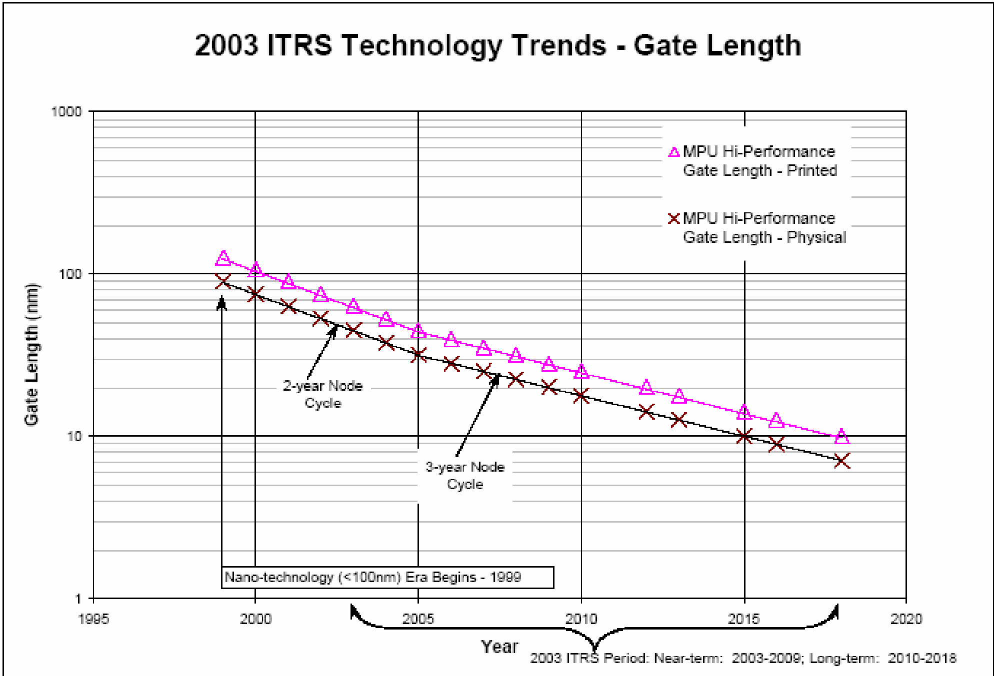
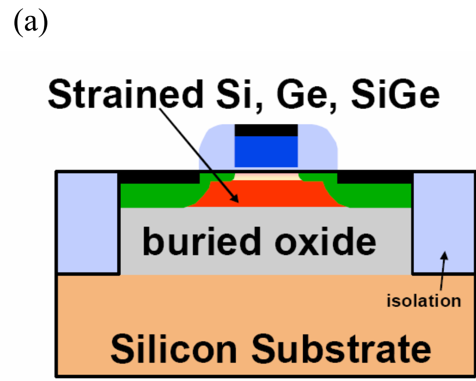
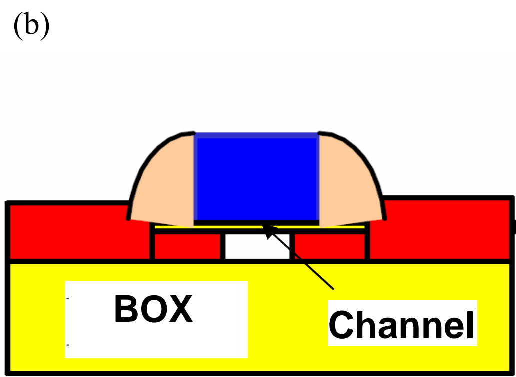


Fig.1-1 ITRS 2003 gate-length trends

(a)



(b)



(c)

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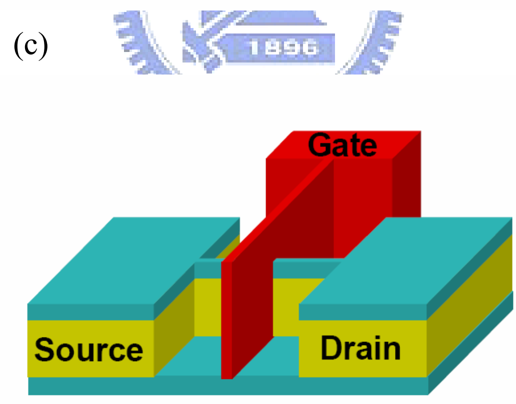


(d)

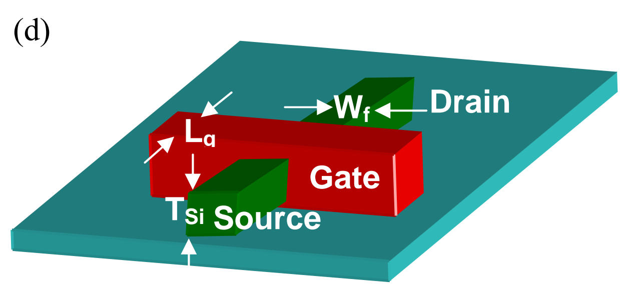


Fig.1-2 Schematic figures of (a) transport-enhanced FETs, (b) UTB SOI FETs, (c) FinFETs, and (d) TGFETs.

Chapter2

Fundamental Characteristics of NiSi Film

2-1 Background and Motivation

2-1-1 Why Nickel Silicide?

Many noble and refractory metals interact with silicon to form stable silicide phase. These silicides, such as Ti, Co, Pt, and Ni, have fairly low resistivity and good high temperature stability, as shown in Table 2-1 [2-1]. Before introducing a silicide into integrated circuits, many process related properties of the silicide must be considered carefully to select the most suitable silicide. The processes properties include low resistivity, ease of formation, ease of pattern definition, minimum silicon consumption, high thermal stability, less film stress, good adhesion, no metal-compound formation, low contact resistance, smooth surface and silicide/silicon interface, no lateral growth, ease selective etching, no contamination to device, wafer, or equipment, and high barrier height for Schottky applications. No single silicide can meet these requirements all together. For example, PtSi reveals low resistivity but it suffers from poor thermal stability, whereas WSi_2 shows excellent thermal stability but its resistivity is relatively high [2-1].

Among the metal silicides, titanium disilicide ($TiSi_2$) and cobalt disilicide ($CoSi_2$) are widely used in salicide process in industry because of their good thermal stability and low electrical resistivity. However, some critical drawbacks limit their applications to the future ULSI technology. It has been reported that Ti may react with

implanted dopants to form compounds such as Ti-B and Ti-As, making $TiSi_2$ a very ineffective diffusion source for boron or arsenic [2-2]-[2-3]. The narrow process window due to the high temperature requirement for the phase transformation from the high resistivity C49 phase to the low resistivity C54 phase (>800°C) and the decrease of silicide agglomeration temperature with the scale down of the silicide thickness (<900°C) is the fatal wound. When the linewidth is scaled down below 2μm, there is a steeply increase in sheet resistance in the narrow $TiSi_2$ lines because the lack of nucleation center in the nanolines causes incomplete transformation from C49 to C54 $TiSi_2$ phase. The C49 structure is characterized by small grain (0.2μm) and larger resistivity (60-80 μΩ-cm) while the C54 structure features a large grain as compared with the line width and lower resistivity (10-16 μΩ-cm). The increase of sheet resistance for the $TiSi_2$ line with decreasing linewidth limits the feature of $TiSi_2$ salicide in below-0.1μm CMOS application. In addition, the creep-up phenomenon during the formation of $TiSi_2$ silicide may form a bridge between the gate and source/drain regions, causing device failure [2-1] & [2-4].

Unlike $TiSi_2$, $CoSi_2$ relaxed the linewidth impact on sheet resistance and creep up phenomenon. Thus, $CoSi_2$ has been extensively used in the deep sub-micron process technology. In addition, $CoSi_2$ has several advantages over $TiSi_2$, such as better stability in the presence of dopants, better plasma etching resistance, and less film stress because of its excellent lattice match with Si (-1.2% at room temperature). However, high Si consumption (Co: Si: $CoSi_2$=1nm: 3.63nm: 3.49nm) during the formation of $CoSi_2$ silicide is the major drawback, which restricts the vertical scaling for $CoSi_2$ to achieve shallow junction [2-5]. Other drawbacks, such as junction spiking of $CoSi_2$-contacted shallow junction due to its sensitivity to native oxide and oxygen-contained environment needs a more complex silicidation process, such as

capping a passivation film during silicidation [2-6]-[2-7].

Recently, Nickel monosilicide (NiSi) has been recognized as a promising candidate for a contact metal in the sub-90 nm technology nodes. It is almost confirmed that the 65nm process will use NiSi to replace $CoSi_2$. For Ni film on a Si substrate (assuming infinite supply of Si material), there are three Ni silicide phases, Ni_2Si, NiSi and $NiSi_2$, formed in sequence at temperature of 250, 350 and 750 ^oC, respectively [2-5]. Among the three Ni silicide phases, NiSi has the lowest resistive phase with an electrical resistivity of 14-20$\mu\Omega$-cm, which is comparable to that of $TiSi_2$ and $CoSi_2$. NiSi doesn't show adverse resistivity dependence on linewidth or creep-up phenomenon [2-8]. Moreover, NiSi has a lower formation temperature than $TiSi_2$ and $CoSi_2$, making it suitable for the low-temperature process in future device fabrication. The further advantage of NiSi relies on its smaller Si consumption (0.82 nm Si for 1 nm NiSi) compared to the formation of $CoSi_2$ (1.04 nm Si for 1 nm $CoSi_2$) and $TiSi_2$ (0.9 nm Si for 1 nm $TiSi_2$) [2-5], which facilitates the formation of shallow junction at the silicide/Si contact. Besides, NiSi has the properties of low NiSi/Si contact resistance, wide process windows (350-750) ^oC, and low film stress. It is almost confirmed that NiSi will be used to replace $CoSi_2$ in the coming 65nm process.

2-1-2 Motivation

Due to the low resistivity, low silicidation temperature and low silicon consumption, the NiSi could also be compatible with the fabrication process of poly-Si TFTs to reduce the S/D parasitic resistance [2-9]. Therefore, the physical mechanism and electrical characteristics of NiSi films on poly-Si film such as thermal stability, Ni diffusion length, and silicide phase stability attract more attentions than that on the bulk Si wafer. Up to now, the fully silicide (FUSI) structure, in which NiSi

contacted gate dielectric directly, has been proposed to prevent the poly-depletion effect and boron penetration while enhance the gate-controllability [2-10]-[2-12]. Nevertheless, except the thermal stability of NiSi on the c-Si substrate, that on the other substrates such as SiO_2, poly-Si, and α-Si has not been studied thoroughly. Therefore, in this chapter, we will examine the thermal stability of NiSi on different substrates first.

The silicide lateral growth rate during silicidation process is also an important issue especially for the use on the non-conventional device structures such as multi-gate (MG) FETs and poly-Si TFTs. In these cases, the Si volume at S/D region is limited; therefore, different Ni/Si thickness ratios would affect the final phase of silicide, device performance, and reliability, particularly in the condition with excess amounts of Ni atoms. For example, excess amounts of Ni films would consume more Si, and then, destroy the S/D junction [2-13]-[2-15]. For the nano Si islands such as the S/D of MGFET structures, owing to the excess Ni atoms on the isolation region, it is very hard to predict the exact final NiSi thickness and control the lateral growth length. To overcome these problems, it is urgent to develop a correct silicidation process to suppress the redundant silicide formation and control the silicide lateral growth well.

In this chapter, first of all, the thermal stability of NiSi on the bulk-Si, poly-Si, α-Si, and SiO_2 substrate were studied. Then, a novel 2-step silicidation method was introduced, which could effectively relax the excess silicidation. To find an optimum condition in order to apply the Ni silicide on the source/drain and gate region at the same simultaneously; silicides were grown at different rapid thermal annealing (RTA) conditions to compare with the 2-step silicidation method. Finally, the lateral silicidation rates at these different silicidation conditions were also studied

carefully.

2-2 Samples Preparation and Experimental Procedures

2-2-1 NiSi Films on Bulk Substrate

First of all, the NiSi was formed on the bare-Si wafer. The substrate was B-doped p-type (100)-oriented silicon wafer with 20Ω-cm nominal resistivity. Before Ni deposition, wafers were immersed into a 100:1 diluted HF (DHF) solution after RCA clean and then were spun dry without DI water rinse to prevent the native oxide formation as shown in Fig.1(a). This process is called HF-treatment. Then, a 25 nm-thick Ni film was sputtering deposited on the bare-Si substrate in a dc sputtering system with a base pressure of less than $2x10^{-8}$ torr using a Ni target as shown in Fig.2-1(b). The chamber pressure during Ar sputtering was kept at 10^{-3} torr with a deposition rate of about 1 nm/sec. To extract the silicidation rate, samples were rapid thermal annealed at different temperature for different time in N_2 ambient to form Nickel monosilicide (NiSi) as shown in Fig.2-1(c). The unreacted Ni film was selectively etched using the H_2SO_4:H_2O_2 (3:1) solution at 75~80^oC, as shown in Fig.2-1(d). The sheet resistance (R_{sh}) was then measured.

2-2-2 NiSi Films on Different Substrates (poly-Si, α-Si, and SiO_2)

Besides on c-Si substrate, NiSi films were also formed on three different substrates including α-Si, poly-Si, and SiO_2 substrates to study the influence of substrate material on silicide resistivity, thermal stability, and phase transformation. To prepare these three substrates, a 500nm thermally oxide was grown on c-Si

substrate at first as shown in Fig.2-2(b). Un-doped poly-Si layers were deposited to 45 and 150 nm thick in a LPCVD system at 620°C as shown in Fig.2-2(c). For the α-Si substrate, similarly, a 150nm thick α-Si layer was deposited in the same LPCVD system at 550°C. After RCA cleaning and HF-treatment, a 25nm thick Ni film was deposited on all samples. For the poly-Si(45nm)/SiO_2(500nm)/Si substrate, because the Si/Ni thickness ratio (T_{Si}/T_{Ni}) is smaller than 1.83, the poly-Si layer could be consumed completely during silicidation, as shown in Fig.2-2(d). Since the silicide directly contacts to the SiO_2 layer, it becomes the NiSi/SiO_2 sample. For the samples with 150nm thick poly-Si and α-Si , the Si layers were not fully consumed and the silicide layer contact the poly-Si and α-Si layer, respectively, as also shown in Fig.2-2(d). They become the NiSi/poly-Si and NiSi/a-Si samples, respectively. Similar to the fabrication process of NiSi/c-Si samples, the unreacted Ni film was selectively etched using the H_2SO_4:H_2O_2 (3:1) solution as shown in Fig.2-2(e). The sheet resistances (R_{sh}) of silicide films on different substrates were then measured.

2-2-3 Lateral Silicidation

In order to extract the lateral growth length of silicide (L_S), a special test structure was designed. Fig.2-4(a) and (b) show the schematic cross-sectional view and top view of the test structure, respectively. It is basically a four-terminal bridge resistor. The central part is capped with a dielectric hardmask layer, SiO_2 in this work, to avoid silicidation. The total length of the silicided segments between the two voltage sensing arms is fixed at $L_{silicide}$=20μm and the length of hardmask (L_{oxide}) is ranging from 0.1 to 2μm. According to equivalent circuit of the test structure shown in Fig.2-4(c), because of the fixed $L_{silicide}$, the variation of total R_{sh} would be

dominated by the variations of L_S and poly-Si ($R_{poly\text{-}Si,in}$). By plotting the measured resistance versus the L_{oxide}, the L_{ST} can be extracted correctly. The process flow to fabricate the test structure is described below.

A 45 nm thick insitu-doped poly-Si film was deposited in a LPCVD system at 620 ^oC on Si wafer covered by a 500nm thermally grown SiO_2 film, as shown in Fig.2-3(c). After the poly-Si layer being patterned by e-beam lithography, a 100nm thick tetra-ethoxy-silane (TEOS) SiO_2 was deposited in a LPCVD system as a hardmask and dopants were then activated at 950°C for 20sec, as shown in Fig.2-3(d). Then the TEOS SiO_2 hardmask was patterned to different widths by the same e-beam lithography system. Following dipping in the DHF solution for 1minute, a 25nm thick Ni film was deposited, as shown in Fig.2-3(e). Finally, samples were annealed in a RTA system at 500 or 600 ^oC for different periods. A 2-step annealing method was also used to study its ability to reduce excess silicidation. In the 2-step annealing method, samples were first annealed at a high-vacuum chamber at 300°C for 1hr, and then the unreacted Ni was removed selectively. Then, a 600°C RTA was performed, as shown in Fig.2-3(f). After annealing, not only the poly-Si regions not covered by the TEOS SiO_2 hardmask have been transformed to Ni silicide entirely, owing to the excess Ni films($T_{Si}/T_{Ni} < 1.83$), silicide will laterally grow into the hardmask capped region to some extent. Before Silicidation, the actual hardmask length (L_{OXIDE}) was measured by in-line SEM. As shown in Fig.2-5, the actual L_{OXIDE} is about 48 nm smaller than the designed L_{OXIDE} on mask.

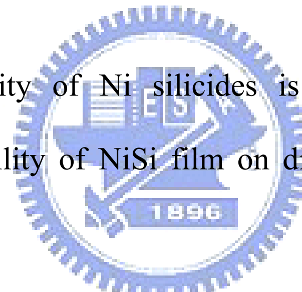
2-2-4 Material Analysis

The sheet resistance (R_{sh}) of silicide film can reflect the phase transition and agglomeration induced by thermal annealing. The R_{sh} of silicide film was measured

by four-point probe and that of silicide line was extracted from the four-terminal bridge resistor using a semiconductor parameter analyzer of model Agilent 4156C. The surface morphology of silicide and the linewidth of poly-Si and silicide nanolines were inspected by in-line and cross-sectional scanning electron microscopy (SEM), respectively. The silicide phase was identified by X-ray diffraction (XRD). Transmission electron microscopy (TEM) analysis was used to inspect the silicide micro-structure and to determine the poly-Si/silicide interface.

2-3 Results and Discussions

2-3-1 Thermal Stability of NiSi films on Different Substrates



The thermal stability of Ni silicides is important. Therefore, in this sub-section, the thermal stability of NiSi film on different substrates are discussed carefully.

Fig.2-6(a) shows the R_{sh} of Ni silicide on c-Si substrate after annealing at 300-800 ^{o}C for 30sec. It is observed that the R_{sh} decreases from 12.65 to 5, 4.36, and 4.37Ω/□, after annealing at 300, 400, 500, and 600°C, and it maintains at 5Ω/□ after annealing at 700°C for 30 sec. However, after annealing 800°C for 30 sec, the R_{sh} increases drastically to 16.88Ω/□. Therefore, for c-Si substrate, the process window of NiSi is from 400 to 700 ^{o}C. The high R_{sh} after annealing at 300 ^{o}C and 800 ^{o}C is attributed to the Ni_2Si phase and agglomeration of NiSi, respectively [2-16]. Moreover, as shown in Fig.2-6(b), after annealing at 600°C for different time (from 5sec to 60sec), a 10 sec annealing reduces the R_{sh} of NiSi to 4.23Ω/□, and longer annealing time maintains the same value. The R_{sh} of samples measured before and after the removal of unreacted Ni are almost the same. This result implies that all of

the Ni atoms react with Si as the annealing time is longer than 10sec and the reaction is dominated by the Ni diffusion-limited mechanism [2-17]. For the annealing time shorter than 10 second, the R_{sh} before removing the unreacted Ni is lower than that after removing the Ni because Ni atoms do not all consumed in such a short period at 600 ^{o}C.

The thermal stability of Ni silicide films on poly-Si, α-Si, and SiO_2 substrates are compared in Fig.2-7. Except the SiO_2 substrate samples, the R_{sh} of the other samples increase as the annealing temperature increases from 550 to 750 ^{o}C. Especially for the film on α-Si substrate, the R_{sh} is about twice higher than the R_{sh} of the others at 550°C, and increases to 10.5Ω/□ at 600°C. According to that reported by M. C. Poon et. al.[2-16], similar to the silicide on the c-Si substrate, the reason of the increase of R_{sh} for Ni silicide on α-Si substrate could be attributed to the silicide phase transformation from NiSi to $NiSi_2$. Because of the higher free energy of α-Si than c-Si and poly-Si, the threshold temperature of phase transformation reduces to 550°C [2-13]. For the Ni silicide film on poly-Si substrate, the R_{sh} maintains at 4.3Ω/□ after annealing at 600°C for 30sec. However, the R_{sh} of poly-Si samples increase obviously after annealing at temperatures higher than 650°C.

In order to understand the R_{sh} degradation mechanism of Ni-silicide on poly-Si substrate, SEM was employed to inspect the cross-sectional and planar structure. The SEM micrographs are shown in Fig.2-8 and Fig.2-9. It is clear that agglomeration happened after a 750°C annealing. Strictly speaking, the Ni silicide on poly-Si substrate becomes morphologically unstable at temperature higher than 650°C, because of the additional driving force for morphological changes induced by the grain boundary energy of the poly-Si. It has been demonstrated that the Si grain growth could be enhanced by the presence of the silicide, which provides a fast

diffusion path for transport of material. And therefore, grain-growth of poly-Si would cause severe roughness of the Ni silicide/poly-Si interface, and even inversion and mixing of the two layers. The silicide surface deformation, inversion, and mixing were all demonstrated in the cross sectional SEM micrographs shown in Fig.2-9 demonstrate. Fig.2-10 shows the results of XRD analysis. For the Ni silicide on poly-Si substrate, even annealed at temperatures higher than 700^oC, the $NiSi_2$ phase is not detected. Therefore, the degradation of NiSi on the poly-Si substrate could be attributed to the silicide-enhanced-grain-growth mechanism [2-16]. Similar to the degradation mechanisms for the silicide on poly-Si substrate, for silicide on α-Si substrate, by an excess free energy ranging from 11 to 20 kJ/mol, Ni diffused quickly and then the $NiSi_2$ forms at a relatively low temperature of about 500^oC [2-17].

It is very singular that the R_{sh} of NiSi is almost constant for the silicide on SiO_2 substrate after annealing at temperature up to 750^oC. Form the planar SEM micrographs shown in Fig.2-8(c) and (d), agglomeration does not happen after annealing at 600 and 750^oC. Moreover, the XRD results for the silicide on the SiO_2 substrate shown in Fig.2-10 indicates that even under 750^oC annealing, phase transformation does not occur. Therefore, the superior thermal stability of Ni silicide on SiO_2 substrate may be explained by the limited Si thickness. Since there isn't any excess Si under silicide layer, neither agglomeration nor silicide-enhanced grain growth could take place.

2-3-2 Controllability of Ni Silicide Lateral Formation

Besides the thermal stability of Ni silicide, the well-control of lateral formation length is another important issue. For Ni silicide applied on the S/D electrodes, the poor control of lateral silicide formation (L_S) would degrade the

devices performance by junction spiking induced by silicide protrusion or precipitation in to the depletion region, steeply increased the interface state between Si/SiO_2, and also degraded the hot-carrier reliability characteristics. Moreover, for applying on the poly-Si gate electrode, several detrimental effects also induced by the poor lateral silicidation controllability including the degradation of gate oxide breakdown voltage, the increasing of the SiO_2 bulk trap density, and the interface state induced by the mechanical stress of the silicide[2-18]-[2-19]. Therefore, in this section, the optimum process condition for the control of the L_S was also researched.

The R_{sh} variations were extracted from the four-terminal test structure shown in Fig.2-4. The average value of R_{sh} of NiSi and poly-Si from 10 measures are 8.52Ω/□ and 77.03Ω/□, respectively. As shown in the Fig.2-12, when the L_{oxide} increases from 0.2, 0.3, 0.4, 0.5, 1, and 2μm, the increasing rate of R_{sh} almost maintains at about 600Ω/μm. The ultra-small R_{sh} of the structure as L_{oxide} =0.1μm could be attributed to the silicide lateral bridging and the off-set between the real and mask oxide length.

To determine the optimum silicidation conditions, three different annealing conditions including one-step 500°C RTA, one-step 600°C RTA, and 2-setp annealing (300°C 1hr in vacuum chamber + 600°C RTA) were performed for different RTA time (10, 30, 60 sec). According to the Fig.2-13, as the annealing time of the one-step 600°C RTA increases from 10 to 60sec, the L_S increases precipitously from 30.11nm to 103.69nm. When the RTA temperature reduces to 500°C, the L_S reduces due to the slower reaction-rate that the Ni diffusion rate in silicide region decreases with the decrease of temperature (diffusion-limited silicide reaction mechanism) [2-17]. It should be noted that among of three conditions, the 2-step silicidation method is almost insensitive to the RTA time. When the RTA time increases from 10 to 60sec,

the L_S slightly increases from 43.2, 46.5, to 47.9nm. During the 1st step 300°C annealing, Ni_2Si is formed; then, following the removal of the unreacted Ni, the 2nd step RTA annealing transform the phase from Ni_2Si to NiSi. Because of the residue Ni atoms have been removed after the 1st annealing, excess silicidation, i.e. significant lateral growth could be avoided.

The line width dependence of L_S is shown in Fig.2-13(b). As the line width (W) decreases, because of the fixed Si volume, the L_S increases. Due to the diffusion-limited silicide reaction, although the L_S is shorter at lower annealing temperature, the control of L_S is hard. Take the 500°C annealing as an example, as the W decreases from 4μm to 1μm, the L_S dramatically increases from 20.8nm to 28.2nm. It is explained that the lower annealing temperature could retard the silicide reaction rate; nevertheless, the hard-control of L_S due to difference line width still exist. Apparently, for the samples annealed at 600°C, drastic increase of L_S and the impact of line width on L_S are observed. The results indicate that annealing temperature, line-width, and Ni/Si ratio determine the L_S. To release this dependence, for the samples with 2-step annealing, because of the removal of the unreacted Ni right after the 1st low temperature annealing step, the L_S is almost independent of the line width. To emphasize the linewidth independence, the L_S of samples with 2-step annealing for different annealing times are shown in Fig.2-13(c). Despite of the different RTA times and line widths, the values of L_S are almost the same to each other.

To confirm the validity of the extraction method of L_S, the cross-sectional TEM micrographs of the test structure with 4μm width and annealed by RTA at 500°C for 10sec are shown in Fig.2-14(a) and (b). The 17nm L_S is very close to the 19nm extracted by electrical measurement.

2-4 Conclusions

In this chapter, before applying the Ni silicide to the novel MGFETs and poly-Si TFTs with limited Si volume, the thermal stability of Ni silicide on different substrates including c-Si, poly-Si, α-Si, and SiO_2 and the control of lateral silicidation are investigated comprehensively.

For the thermal stability, because of the high free-energy of the interface between NiSi/α-Si, the thermal stability is poor (around 550°C); moreover, because of the faster diffusion rate of the α-Si, the phase transformation from NiSi to $NiSi_2$ is the dominant degradation mechanism. For the Ni silicide on poly-Si substrate, silicide-enhanced Si grain-growth dominates the silicide degradation. Silicide surface deformation, structure inversion, and structure mixing happened as the annealing temperature rose from 600, 700, to 750°C. On the contrary, for the Ni silicide on SiO_2 substrate, no excess Si or poly-Si grain-boundary under the silicide; therefore, neither the phase transformation nor the silicide agglomeration could occur even under 750°C annealing. This characteristic is benefit to the fully-silicide gate and fully silicided S/D applications.

An electrical method is proposed to extract the silicide lateral growth. A 2-step annealing method (1st annealing in a vacuum chamber at 300°C + 2nd annealing in a RTA system at 600°C) is demonstrated to be insensitive to the RTA time and almost independent of the linewidth. This method will be employed in the following chapters.

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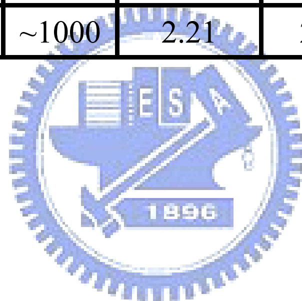
Table2-1 Basic properties of some silicides.

Silicide	**Thin film resistivity(μΩ–cm)**	**Stable on Si up to (°C)**	**nm of Si consumed per nm of metal**	**nm of resulting silicide per nm of metal**	**Barrier height to n-Si(eV)**	**Film stress(dyne/cm)**
PtSi	28-35	~750	1.12	1.97	0.84	$1x10^{10}$
$TiSi_2$(C54)	13-16	~900	2.27	2.51	0.58	$1.5x10^{10}$
$TiSi_2$(C49)	60-70	x	2.27	2.51	x	x
Co_2Si	~70	x	0.91	1.47	x	x
CoSi	100-150	x	1.82	2.02	x	x
$CoSi_2$	14-20	~950	3.64	3.52	0.65	$1.2x10^{10}$
NiSi	14-20	~650	1.83	2.34	x	$6x10^{9}$
$NiSi_2$	40-50	x	3.65	3.63	0.66	x
WSi_2	30-70	~1000	2.53	2.58	0.67	x
$MoSi_2$	40-100	~1000	2.56	2.59	0.64	x
$TaSi_2$	35-55	~1000	2.21	2.41	0.59	x



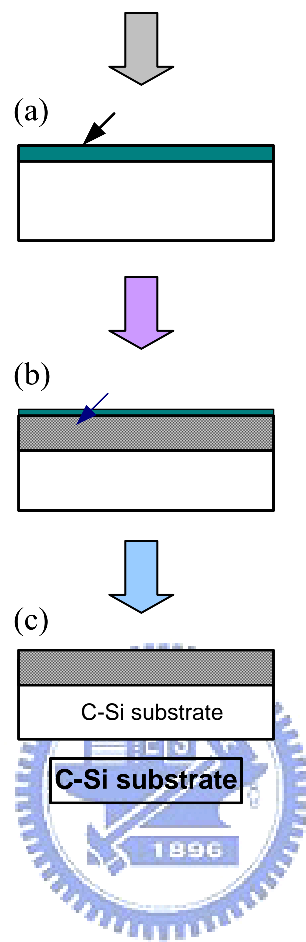


Fig.2-1 Main process steps of the sample of Ni-silicide on c-Si substrate.

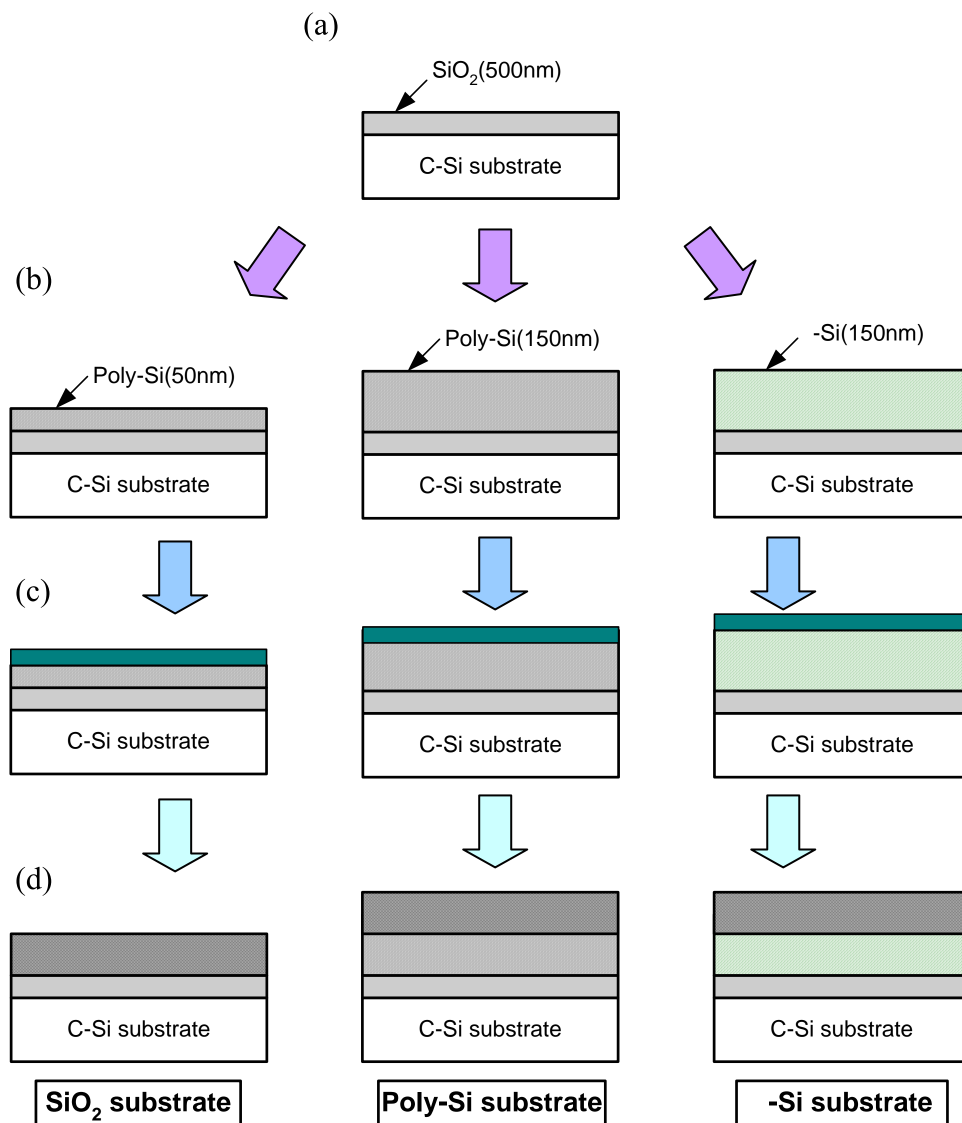


Fig.2-2 Main process steps of the samples of Ni silicide on (a) SiO_2, (b) poly-Si, and (c) α-Si substrate.

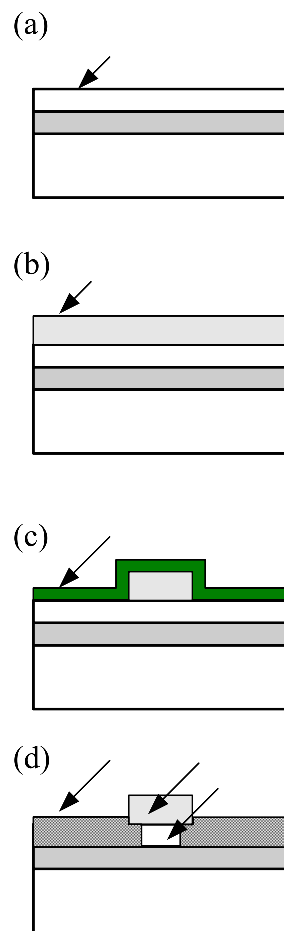


Fig.2-3 Main process steps of the test structure used to extract the silicide lateral growth (L_S).

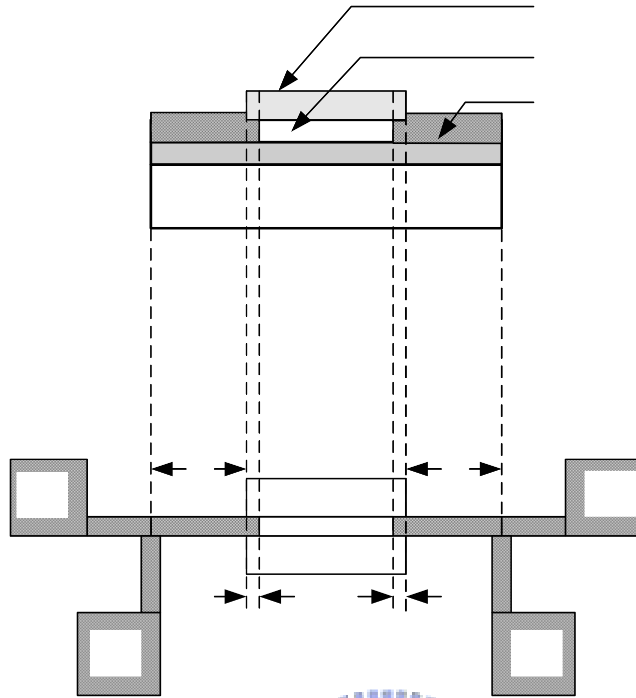


Fig.2-4 Cross-sectional and plane views of the test structure used to extract the silicide lateral growth (L_S).

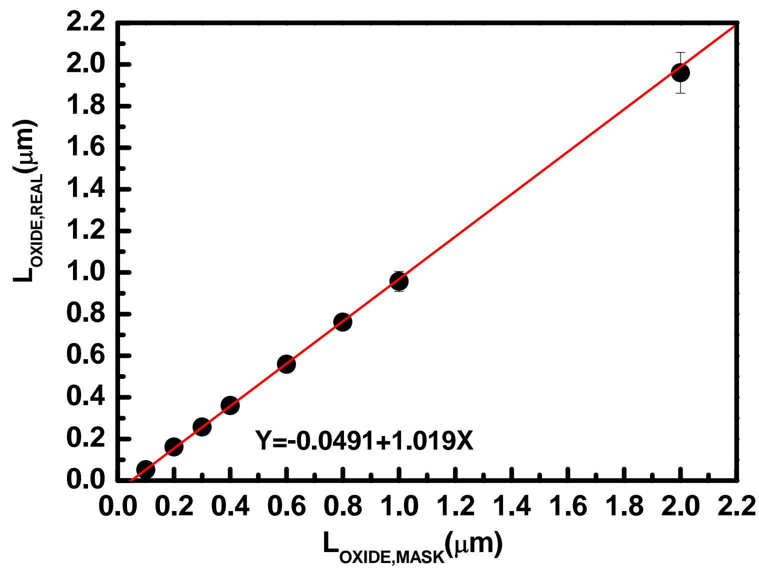


Fig.2-5 Correlation between the actual length and the designed length of the hardmask.

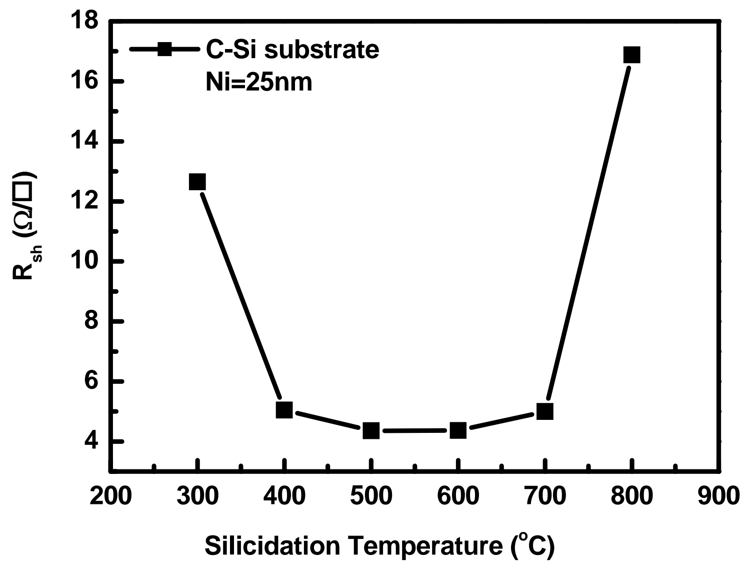


Fig.2-6(a) Sheet resistance of Ni silicide on c-Si substrate after annealing at different temperatures.

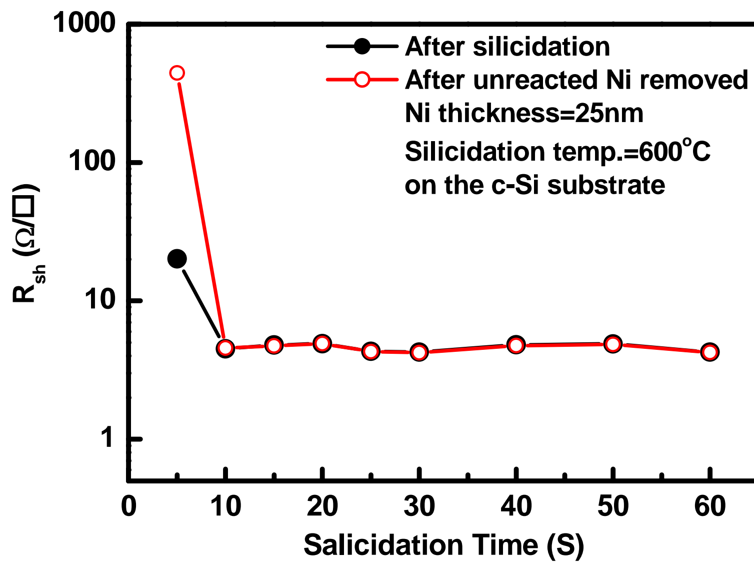


Fig.2-6(b) Sheet resistance of Ni silicide before and after the removal of the unreacted Ni after annealing at 600°C for different times.

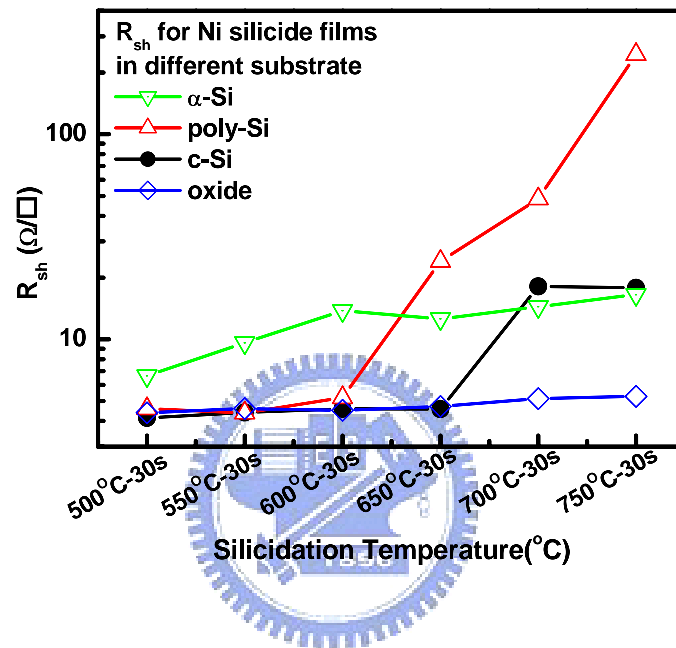


Fig.2-7 Sheet resistance of Ni silicide on c-Si, poly-Si, α-Si, and SiO_2 substrates after annealing at different temperatures.

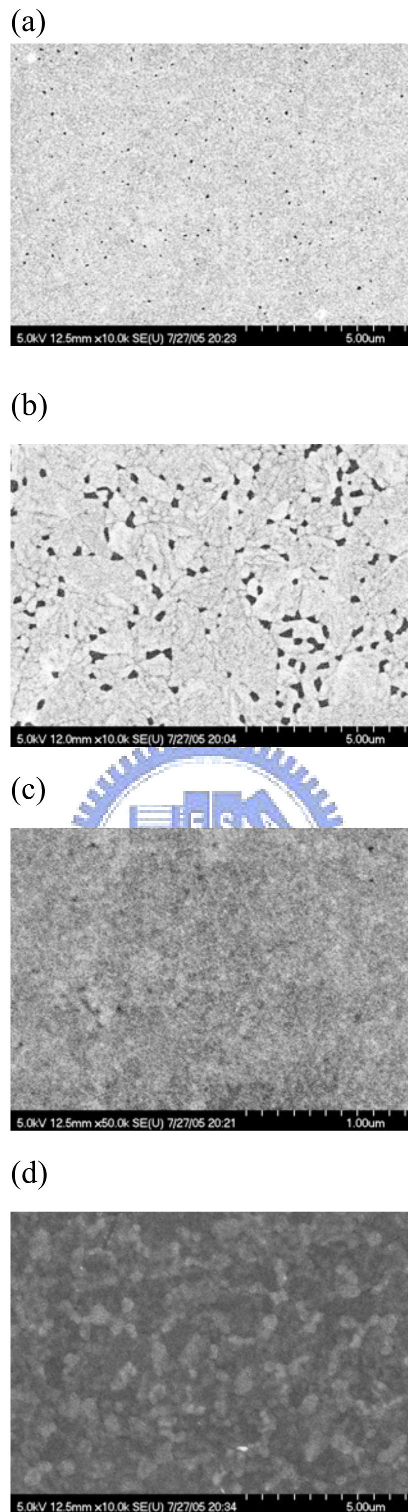
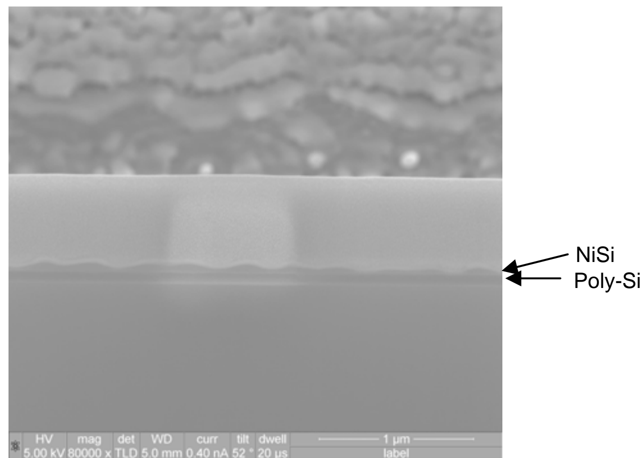
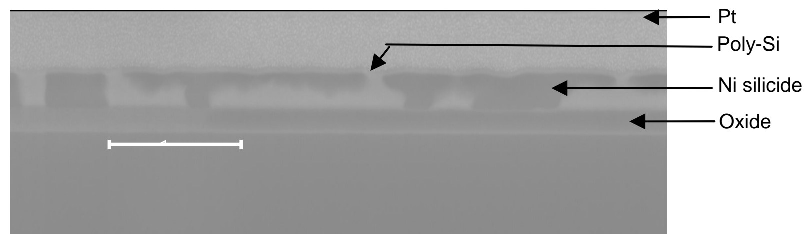


Fig.2-8 Planar SEM micrographs of Ni silicide (a) on poly-Si substrate after 600°C, 30sec annealing, (b) on poly-Si substrate after 750°C, 30sec annealing (c) on SiO_2 substrate after 600°C, 30sec annealing, (d) on SiO_2 substrate after 750°C, 30sec annealing.

(a)



(b)



(c)

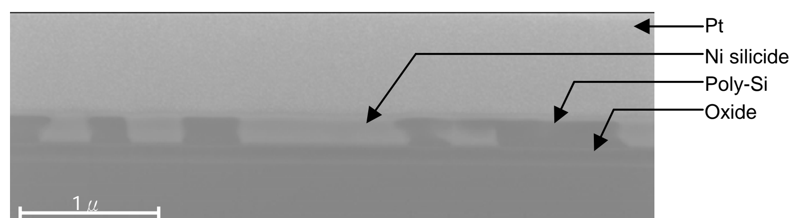


Fig.2-9 Cross-sectional SEM images of Ni silicide on poly-Si substrate after (a) 600°C, 30sec annealing, (b) 700°C, 30sec annealing, and (c) 750°C, 30sec annealing.

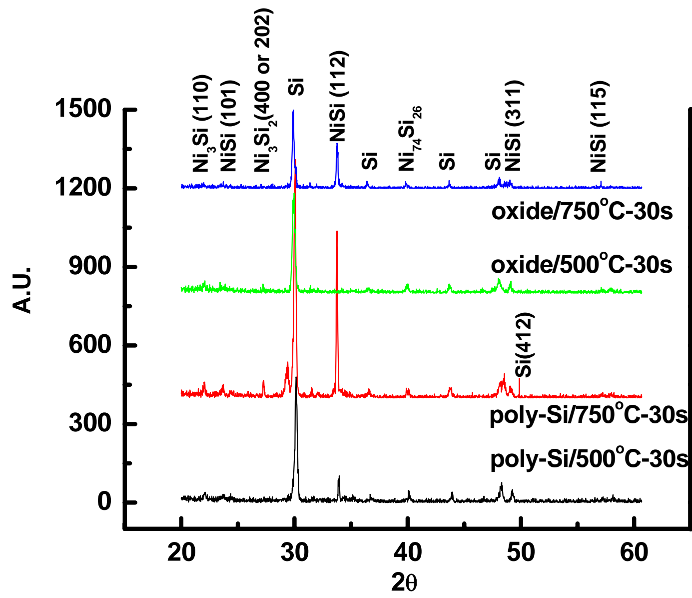


Fig.2-10 XRD spectra of Ni silicide on poly-Si and SiO_2 substrates after annealing at 600°C and 750°C for 30sec.

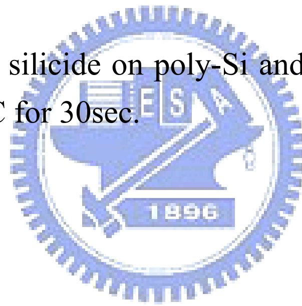


Fig.2-11 Schematic resistance distribution of the test structure shown in Fig.2-4.

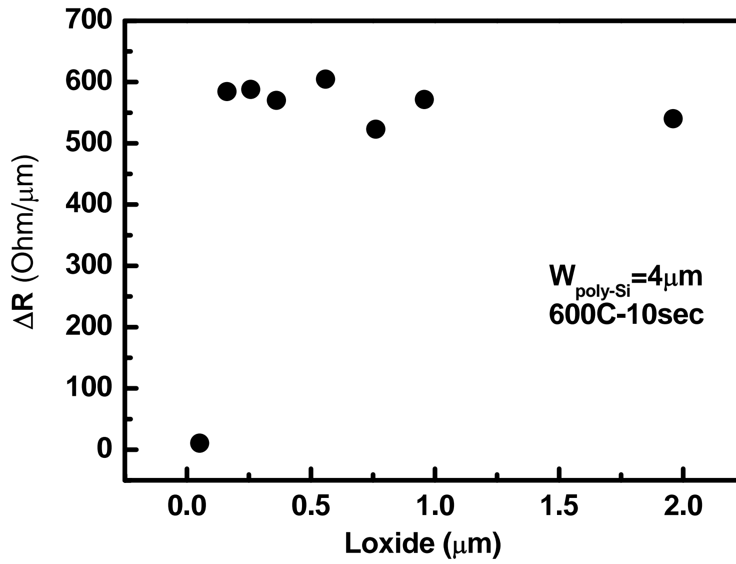


Fig.2-12 Sheet resistance variation of the 4μm wide test structure as a function of L_{oxide}.

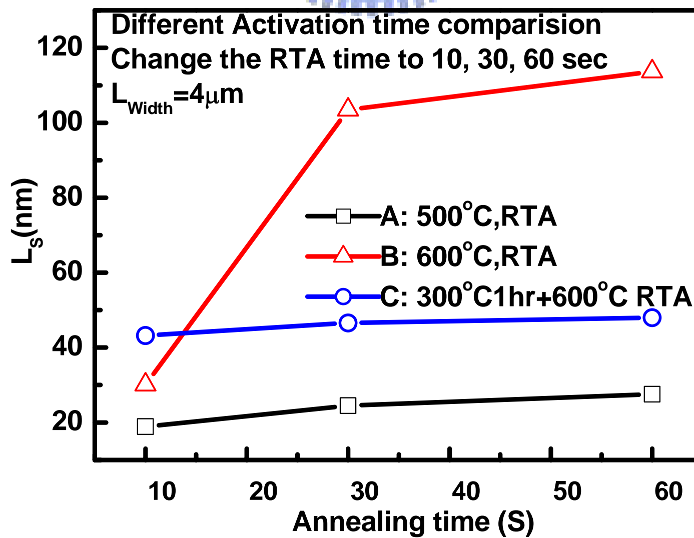


Fig.2-13(a) Lateral growth (L_S) of Ni silicide on poly-Si substrate after annealing at different conditions for different times.

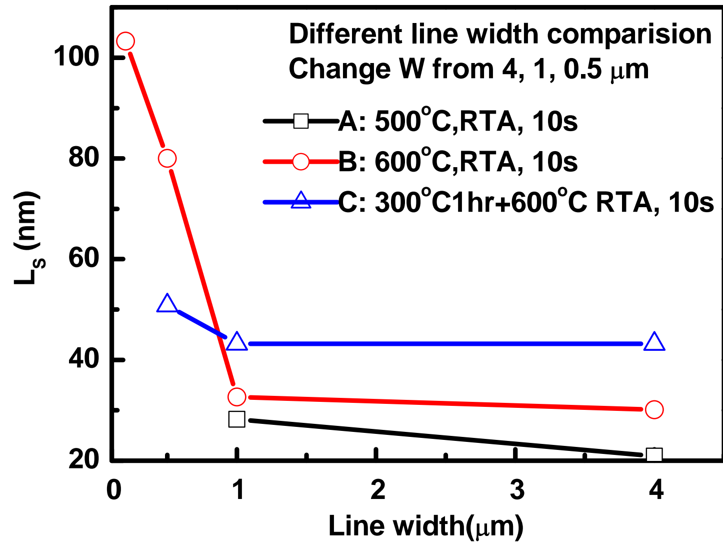
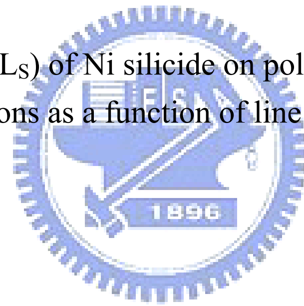


Fig.2-13(b) Lateral growth (L_S) of Ni silicide on poly-Si substrate after annealing at different conditions as a function of line width (W).



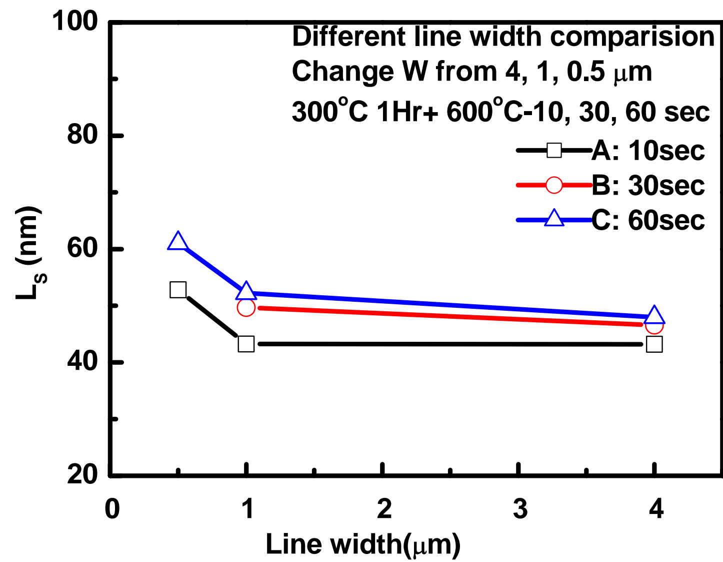


Fig.2-13(c) Lateral growth (L_S) of Ni silicide on poly-Si substrate after 2-step annealing for different times as a function of line width (W).

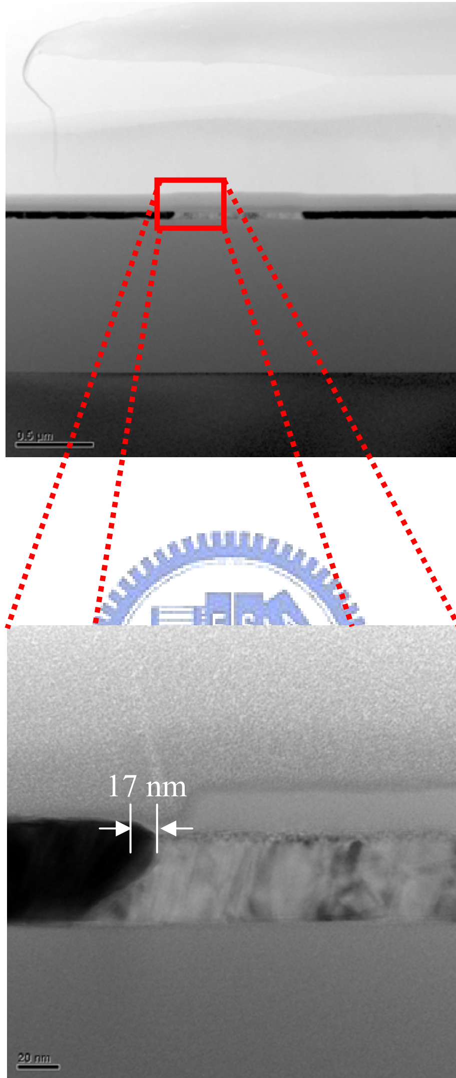


Fig.2-14 Cross-sectional TEM images of the test structure of Ni silicide on poly-Si substrate after RTA at 500°C for 10 sec (line width=4μm).

Chapter 3

Fabrication and Characterization of Tri-Gate (TG) FETs with Modified-Schottky-Barrier (MSB) Source/Drain

3-1 Background and Motivation

The first Schottky barrier MOSFET (SB-MOSFET) utilizing metal silicide to replace the heavily doped silicon within the source/drain regions was proposed in 1968 [3-1]. Compared with conventional MOSFET, SB-MOSFET had several advantages including easy processing, ultra-shallow junction, low source/drain (S/D) external resistance, low thermal budget, and excellent short channel effect immunity. In 1983, the Schottky barrier PMOS was proposed to eliminate the latch-up effect [3-2, 3-3]. However, the drawbacks of high drain leakage current attributed to the thermionic emission current and low driving capability due to the abnormally high Schottky barrier height made it impractical [3-4, 3-5]. Subsequently, asymmetric Schottky MOSFET with Schottky barrier source junction and p-n drain junction was shown to solve the leakage current issue [3-6]. However, the problem of low driving current left unsolved. Furthermore, the asymmetric device is difficult to be scaled down.

Recently, nano-scale SB-MOSFETs were proposed so that the driving capability could be improved by the gate fringing field due to the short spacer length [3-7]. Nevertheless, previous problems still existed for those nano-scale

SB-MOSFETs. For example, the gate fringing field could not suppress the Schottky barrier height effectively, so that the on-state current (I_{on}) of SB-MOSFET was still lower than that of the conventional MOSFET. A method of reducing this barrier by using complementary silicide (PtSi for PMOS and ErSi for NMOS) on bulk or SOI substrate has been suggested [3-7]-[3-8]. However, the process to form complimentary-silicide was more complex than that to form single silicide, and the abnormally high off-state leakage current (I_{off}) due to the thermionic injection and GIDL-like effect were still problems [3-9]. Adding a metal field-plate over the MOSFET was shown to be effective in reducing the off-state leakage current (I_{off}) by suppressing thermionic-injection from the drain contact; nevertheless, it required an additional voltage supply and sacrificed device density [3-10]. The SOI structure with fully silicided S/D and doped S/D extension (SDE) fabricated by a conventional process was also reported to have proper electrical characteristics [3-11]. Nevertheless, it was basically a conventional MOSFET with identical thermal budget.

To overcome the drawbacks of SB-MOSFETs while keeping the advantages of low S/D external resistance and low temperature process, a new MSB TGFET with ultra-short source/drain extension (SDE) using an implant-to-silicide (ITS) process was proposed [3-12]. Adding an extension doping in the silicon drastically improves Schottky limit for I_{on} by thinning and reducing the SB at the source/body junction at on-state. The gate wraps around the rectangular silicon fin from three sides, so that a significantly high driving current and excellent short channel characteristics could be achieved at the same feature size [3-13]. Furthermore, the proposed MSB device also showed significantly lower I_{off} than the conventional SB device because of the thick SB at the drain/body junction during off-state.

The key process developed in this thesis is a two-step low-temperature (<

600°C) annealing technique, which has been verified in chapter 2 to control the lateral silicidation process well. Here, not only the detailed fabrication of MSB TGFETs using ITS technique was suggested, but a detailed study on the I-V characteristics of the MSB TGFET with various fin thicknesses was also carried out. Next, based on these studies, the conduction mechanisms for on-state and off-state were proposed. The temperature impact on the electrical characteristics was studied and the leakage current mechanism was analyzed. Finally, the uniformity dependence of SDE region related to the electrical characteristics, including drain-induced barrier lowing (DIBL) and subthreshold swing (S.S) were also investigated.

3-2 Device Fabrication

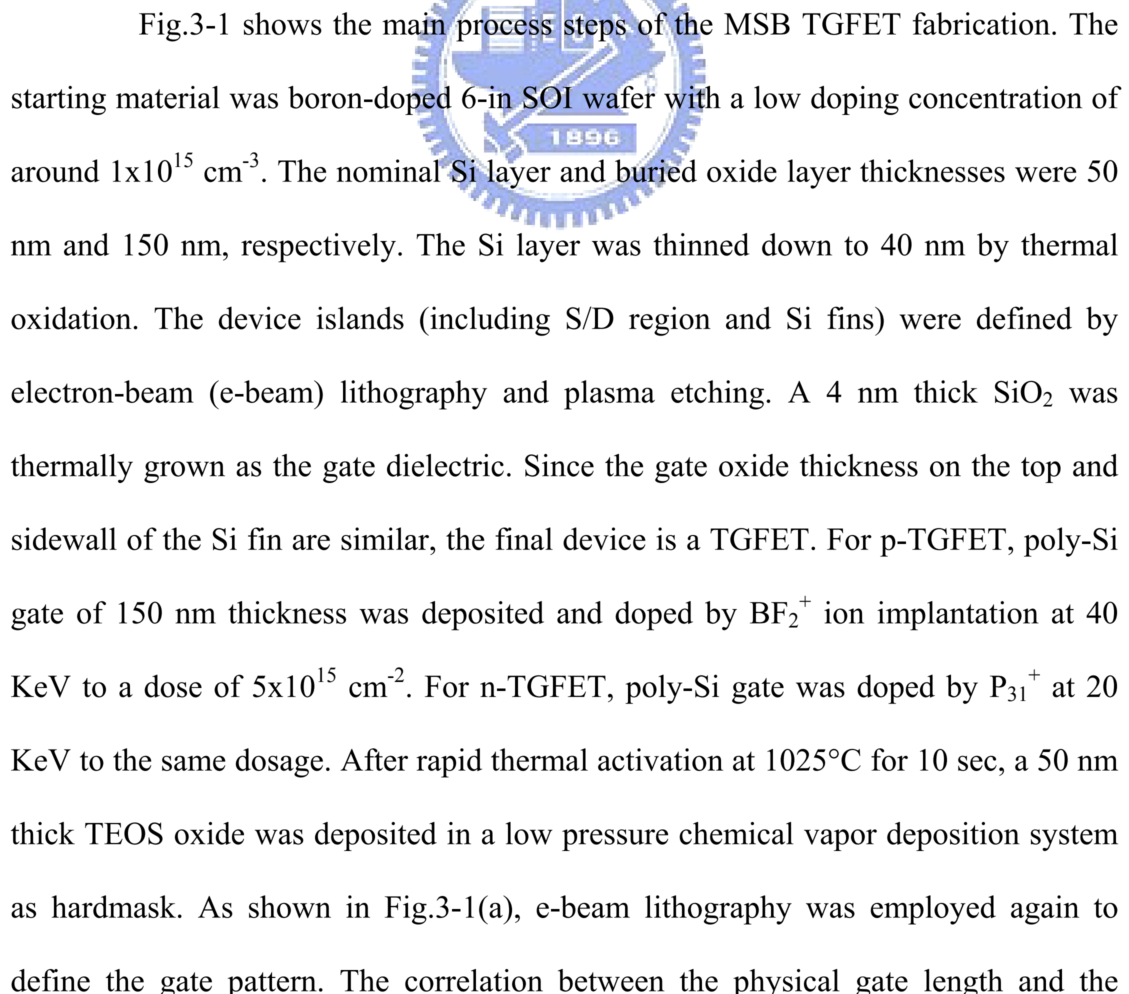


Fig.3-1 shows the main process steps of the MSB TGFET fabrication. The starting material was boron-doped 6-in SOI wafer with a low doping concentration of around 1×10^{15} cm^{-3}. The nominal Si layer and buried oxide layer thicknesses were 50 nm and 150 nm, respectively. The Si layer was thinned down to 40 nm by thermal oxidation. The device islands (including S/D region and Si fins) were defined by electron-beam (e-beam) lithography and plasma etching. A 4 nm thick SiO_2 was thermally grown as the gate dielectric. Since the gate oxide thickness on the top and sidewall of the Si fin are similar, the final device is a TGFET. For p-TGFET, poly-Si gate of 150 nm thickness was deposited and doped by BF_2^+ ion implantation at 40 KeV to a dose of 5×10^{15} cm^{-2}. For n-TGFET, poly-Si gate was doped by P_{31}^+ at 20 KeV to the same dosage. After rapid thermal activation at 1025°C for 10 sec, a 50 nm thick TEOS oxide was deposited in a low pressure chemical vapor deposition system as hardmask. As shown in Fig.3-1(a), e-beam lithography was employed again to define the gate pattern. The correlation between the physical gate length and the

layout length on mask is shown in Fig.3-2. The gate length as short as 25nm can be obtained repeatedly. Following gate patterning, a SiO_2 (10nm)/Si_3N_4 (30nm) composite spacer was formed, as shown in Fig.3-1(b). The hardmask on poly-Si was etched away during spacer etching. Self-aligned Nickel silicide (Ni-Salicide) process was then performed and the resulting structure is shown in Fig.3-1(c). The sheet resistance (R_{sh}) of the silicide layer is about 10Ω/□ as measured by a four-point sheet resistance measurement stage. This silicidation process is the key process step for the MSB TGFET and is discussed extensively in the next section.

To modify the characteristics of the Schottky barrier, for MSB p-TGFETs, BF_2^+ ions were implanted to silicide at 30 KeV to a dose of 5×10^{15} cm^{-2}, followed by a furnace annealing at 600 °C in a N_2 ambient for 30 min. For MSB n-TGFETs, the implantation condition changed to P_{31}^+ at 20KeV for 5E15cm^{-2}. To study the dose effect, MSB devices with different S/D doses of 5×10^{14} cm^{-2} were also fabricated. The silicide layer acts as a stop layer for the implanted ions and as a solid diffusion source for the lateral diffusion of ions into the silicon region to form an ultra-short SDE. Monte-Carlo simulation shows that the straggling distribution of P_{31}^+ and BF_2^+ ions were only 9nm and 8 nm, which were both shorter than the lateral growth of silicide [3-14]. Hence, all of the implanted ions were confined in the silicide region and the channel region was not damaged. It has been reported that the ITS process forms a modified Schottky junction with characteristics between a pn junction and a pure Schottky junction [3-15][3-17]. Since the ion implantation does not directly damage the Si layer, the junction would be free of crystalline defects and low junction leakage current could be expected. During the post-implantation annealing, boron atoms were diffused out of the silicide and piled up at the Si/silicide interface to form an ultra-short SDE uniformly as indicated in Fig.3-1 (d). In this ITS technique, since the

annealing temperature is not determined by the annihilation of ion implantation induced damages, the thermal budget is greatly reduced.

Typical inter layer dielectric deposition, contact hole patterning, and Al metallization completed the fabrication process. For comparison, a simple Schottky barrier (SB) TGFET without the ITS process step and conventional (CN) TGFET without S/D silicidation were also fabricated. The post S/D implantation annealing was performed at 1025°C for 20 sec in a N_2 ambient for the CN TGFET.

3-3 Results and Discussions

3-3-1 2-Step Ni Silicidation Method

As stated in chapter-2, Ni reacts with Si to form Ni-rich silicide at temperatures as low as 200°C, so the Ni-silicide is typically formed by one-step rapid thermal annealing at 400-600°C for 30-60 sec. The unreacted Ni can be selectively removed using a H_2SO_4+H_2O_2 mixture. Since the dominant diffuser during silicide formation is Ni, the Ni-silicide is confined at the Si region and the gate to S/D isolation can be controlled easily. However, as the Si region becomes small, a large number of Ni atoms can be supplied from the Ni film deposited on the isolation region. It has been reported that excess silicidation occurs in the conventional one-step rapid thermal annealing at 500~600℃ due to the fast diffusion of Ni atoms from regions at isolated layer surrounding the small silicon region [3-18]. In bulk CMOS, the failure modes are poly-Si gate depletion and S/D junction leakage current. In the TGFET devices, excess silicidation may result in different failure modes such as S/D short, gate dielectric degradation, etc.

According to the volume ratio of Ni/Si, a 22 nm thick Ni film was deposited

by a DC sputtering system to completely convert the 40 nm thick Si to silicide. Fig.3-3 shows the cross-sectional transmission electron micrograph of an MSB device after one-step rapid thermal silicidation at 600°C for 30 seconds. As expected, no silicide was observed on the sidewall spacer. However, because of the difficulty of the controllability of the silicidation, the poly-Si gate was fully silicided and the silicide extended from S/D into the channel region, and then the whole channel region was converted to silicide and the gate was directly shorted to S/D. This result confirms the L_S extracted in chapter-2. The S/D to gate leakage current was measured for all devices. Because the Ni-silicide grows so fast, it is hard to correctly estimate the right Ni film thickness and annealing time to consume the suitable Si volume at 500~600°C one step annealing. Although the reduction of the annealing temperature is another way to improve the controllability of the lateral and excess silicidation, the influences of the thermal process following the silicidation cannot be neglected.

To completely convert the Si layer in the S/D region into silicide with suitable lateral growth and without excess silicidation, a two-step annealing technique proposed in chapter-2 must be employed. Initially, the wafer deposited with 22 nm thick Ni film was annealed in vacuum chamber at 300°C for 60 min to form Ni_2Si at the S/D and the poly-Si gate regions. Due to the diffusion-limited silicidation mechanism at low temperature we used, the slower Ni diffusion from the surrounding regions and the slight excess silicidation have been demonstrated in chapter 2. After selective removal of unreacted Ni, the wafer was rapidly thermally annealed in ambient N_2 at 600°C for 30 sec. During this annealing step, there was no excess Ni atoms surrounding the small active region, so, the excess silicidation problem was avoided. Fig.3-4 shows R_{sh} of Ni silicide on the Si-substrate after the 1st annealing and the 2nd annealing, respectively. It is clear that after the 2nd annealing, the R_{sh} is almost

constant and insensitive to the annealing time as the 1st annealing time is longer than 30min at 300°C. Fig.3-5(a)-(c) shows the schematic layout and cross-sectional TEM micrographs of the MSB TGFET with gate length (L_g) of 25 nm, fin thickness (W_f) of 40 nm, and fin height (T_{Si}) of 40 nm. The thickness and lateral growth of silicide are well controlled, and it is confirmed that the SDE was defect-free.

Fig.3-6 shows the electron diffraction pattern at the positions of A, B (S/D region), and C (gate region) indicated in Fig.3-5(b). The silicide phases at the gate region and S/D region were identified as NiSi and $NiSi_2$, respectively. This phase difference is presumably caused by the differing stresses in the S/D region and gate region [3-19].

The doping profile of the ultra-short SDE is critical. However, since the volume of the SDE is so small, neither Secondary Ion Mass Spectroscopy (SIMS) nor Spreading Resistance Profiling (SRP) could be applied. The spatial resolution of Scanning Capacitance Microscopy (SCM) was also not sufficient. Kelvin Probe Force Microscopy (KPFM) with a carbon nano-tube probe might be a solution but great efforts would be needed to implement this technique [3-20]. Therefore, we could not correctly determine the doping profile of the SDE at this moment. However, electrical characteristics of the MSB devices shown in the next subsection clearly support the existence of the SDE.

3-3-2 Electrical Characteristics and Mechanisms of MSB Devices

Schottky barrier (SB) devices were suggested as the promising candidate devices because of its ultra-low process temperature, ease of fabrication, and scalability down to 10 nm-node. However, the poor I-V characteristics of SB devices still need to be reinforced. In this work, the sub-100nm SB TGFETs (L_g=49nm,

W_f=60nm, and T_{Si}=40nm) were also fabricated. Fig.3-7(a) and (b) show the typical transfer and output characteristics of the conventional SB TGFETs, respectively. The obvious leakage current at off-state, abnormal high threshold voltage, poor subthreshold characteristic, and low I_{on} were observed. It is well known that the I_{on} for SB devices was suppressed by the Schottky barrier height at source-side Schottky junction. More clearly, the carriers injected from source to channel are reduced owing to the high and wide Schottky-barrier. On the other hand, abnormally high I_{off} was supplied by the minority carrier injection from the drain-side Schottky junction to the channel. Therefore, the threshold voltage at V_{ds}=50mV($V_{th,lin}$) of n- and p-channel SB devices are about 0.95V and -1.3V, respectively, and the driving current at V_{ds}=1V ($I_{on,sat}$) are about 1.84 μA and 1.83 μA, respectively, as listed in Table 3-1. Moreover, due to the height of Schottky barrier, the "sublinear" phenomenon is pronounced in the linear region, as shown in Fig.3-7(c). To clarify the turn-on/turn-off mechanisms of SB devices, the schematic band diagrams for p-SB devices were shown in Fig.3-9(a) and (b).

Fig.3-8(a) and (b) show the typical transfer and output characteristics, respectively, of the long channel MSB devices with L_g=W_f = 1μm and T_{Si} = 40 nm. It is clearly that the poor characteristics of conventional SB devices including dreadful threshold characteristics and sublinear phenomenon in the linear region are all disappeared. The detailed devices parameters are also summarized in Table.3-2. Taking the p-channel device as example, the $V_{th,lin}$ can be down to 0.1V, the subthreshold swing (S.S.) about 62 mV/Dec is closed to the ideally value, and the $I_{on,sat}$ is also raised to ~72.6 μA/μm . For our SB TGFET, the large channel-S/D offset should be the dominant mechanism for the poor characteristics, although the effect of Schottky barrier cannot be ignored. For the MSB TGFET, the ultra-shallow SDE

bridges channel and S/D silicide. Furthermore, the Schottky barrier thickness, i.e. the carrier injection resistance from source to channel, is reduced by the high concentration of ultra-short SDE. Therefore, the “sublinear” phenomenon is not observed.

According to the above observations, band diagrams of p-channel devices at the on-state and off-state are schematically illustrated in Fig.3-10(a) and (b), respectively. When the device operates at the on-state, the high concentration ultra-short SDE effectively thins out the Schottky barrier width between source silicide and the inverted channel so that the holes can tunnel through the barrier much more easily. On the other hand, when the device operates at the off-state, due to the ultra-short SDE, the modified Schottky barrier at the drain contact is wider and higher than the conventional SB devices, so it can effectively block electron tunneling. Therefore, the proposed MSB device exhibits excellent on/off performance.

3-3-3 Electrical Characteristics of MSB TGFETs

Fig.3-11(a) and (b) present the transfer and output characteristics of MSB n- and p-TGFETs with L_g=25nm, W_f=40nm, and T_{Si}=40nm. Taking the p-TGFETs as examples, the $I_{on,sat}$ of the 25 nm MSB p-TGFET at $|V_{ds}| = |V_g-V_{th}| = 1$ V exceeds 108 μA/μm under the definition of channel width W= 2*T_{Si} + W_f, or 325 μA/μm under the definition of channel width W= W_f. It should be noted that the I_{on} could be further improved by shorter spacer length and thinner gate oxide thickness.

Moreover, even with ultra-short channel length around 25nm, by inserting an ultra-short SDE to modify the Schottky barrier property, the MSB p-TGFET can turn on more steeply and it had an extremely high I_{on}/I_{off} current ratio, exceeding 10^9. This 25 nm MSB p-TGFET also shows superior subthreshold characteristics with a

swing of 83 mV/decade and a drain-induced-barrier-lowering (DIBL) of 235 mV/V. These values are closed to the 3-dimensional simulation results and could be further improved by reducing of the fin height and fin thickness to get better gate controllability [3-12]-[3-21].

The n-type MSB devices also have better characteristics than that of the n-type SB ones. However, because of the lower diffusion constant of Phosphorus in silicide and Si than that of Boron dopant, the shorter SDE region and the SB-like characteristics such as slightly "sublinear" phenomena, worse subthreshold characteristics smaller $I_{on,sat}$ and higher I_{off} are observed for the 25nm MSB n-TGFETs.

To further demonstrate the improvement of MSB TGFETs, the transfer characteristics of MSB, SB and CN TGFETs with L_g= 49 nm, W_f= 60 nm, and T_{Si}= 40 nm are compared in Fig.3-12. The detailed parameters are also summarized in Table.3-4. The poor driving capability of the CN TGFET can be explained by the high S/D resistance due to the un-silicided S/D region. The better DIBL of the MSB TGFET than that of the CN TGFET confirms the advantage of the low thermal budget of the MSB process. The 49 nm MSB TGFET shows an excellent subthreshold swing (60.4 mV/decade), excellent DIBL (39 mV/V), and extremely high I_{on}/I_{off} current ratio ($>10^9$). These results are better than those reported from conventional and SB TGFETs. Conversely, in the case of SB TGFET, a typical ambipolar operation is observed. For the p-channel operation, the SB TGFET has poor subthreshold swing and an I_{on}/I_{off} current ratio of lower than 10^3. It has been proposed that the effective Schottky barrier height of thin-body SOI SB TGFET is higher than that of the bulk SB MOSFET due to quantum confinement in the direction normal to the channel so that the I_{on} is low [3-5]. The effective Schottky barrier height at the off-state is lowered by

the GIDL-like mechanism, which makes the off-state characteristic of the SB TGFET undesirable [3-9].

Besides the short channel effect of TGFETs which has been studied numerically and experimentally by several research groups [3-23 and3-25], in this work, the width impact on the device parameter variations are also researched. Pei et al. proposed that in order to suppress SCE, the fin thickness must be less than one third of the channel width [3-23]. Chau et al. reported that to maintain full substrate depletion, the Si body thickness should be about 1/3 or 2/3 of the gate length in the case of single gate or double gate structures, respectively [3-24]. In the case of a tri-gate structure, the required Si body thickness becomes equal to the gate length [3-25]. In fact, the threshold channel length depends on the gate structure and the fin concentration. Fig.3-13 shows the subthreshold swing of the p-channel MSB and CN TGFETs as a function of fin thickness with L_g=49 nm and 130 nm. The CN TGFETs shows weak fin thickness dependence, which is quite different from the results in some earlier reports [3-23]-[3-25], which may be explained by the low fin concentration employed in this work. Here, the top gate alone can fully deplete the channel, so the fin thickness does not clearly affect the SCE apparently. The subthreshold swing of the CN TGFETs is worse than that of the MSB TGFETs in Fig.3-13, which may result from the higher interface state density induced by boron penetration.

For the MSB TGFET, thinner fin thickness results in lower subthreshold swing. However, the extent of improvement differs for MSB and CN TGFETs. Furthermore, the 130 nm MSB TGFETs exhibit better subthreshold swing than the 49 nm MSB TGFETs at all fin thicknesses. Since the CN TGFETs do not show this phenomenon, it cannot be explained by the gate control capability. We suspect that

this unusual phenomenon is related to the S/D silicidation.

Fig.3-14(a) and (b) show the plane-view TEM micrographs of the MSB TGFETs with W_f=49 nm and 200 nm, respectively. The silicided narrow fin shows a bamboo structure and only a single grain exists at the front edge of the S/D region. As the fin thickness becomes larger, the S/D region consists of multiple grains. This multi-grain structure results in a non-uniform front edge of the silicide, which in turn results in a non-uniform front edge of the ultra-short SDE, as shown schematically in Fig.3-15. As the channel length is short, a minimal non-uniformity of the S/D junction front edge clearly affects the device subthreshold characteristic. This postulation is also supported by the weak fin thickness dependence of subthreshold swing for the CN TGFETs shown in Fig.3-13 because the CN TGFETs have a smooth S/D junction front edge. For thin fin devices, the CN TGFETs show worse swing than the MSB ones. The high external resistance of the un-silicided S/D of the CN TGFETs could explain this phenomenon.

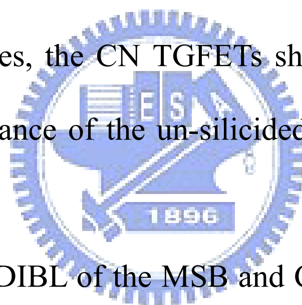


Fig.3-15 shows the DIBL of the MSB and CN TGFETs as a function of fin thickness, indicating a trend similar to the swing. It can be observed that with suitable combination of channel length and fin thickness, MSB TGFETs can be achieved with an excellent performance of nearly ideal subthreshold swing of 60.4 mV/decade and DIBL of 39 mV/V.

3-3-4 Leakage Current Mechanisms of MSB Devices

To further understand the conduction mechanism of the off-state leakage current, the I-V characteristic of the p-channel MSB TGFET with L_g= 65 nm was measured at different temperatures from 100 K to 500 K, as shown in Fig.3-17. At room temperature, the MSB TGFET exhibits a subthreshold swing of 78 mV/decade

at V_{ds}=-1V and extremely high I_{on}/I_{off} current ratio, exceeding 10^9. The I_{off} decreases at lower temperatures, so that the I_{on}/I_{off} current ratio well exceeding 10^{10} and the subthreshold swing better than 74 mV/decade are achieved at 100 K. The Arrhenius plot of I_{off} for the 65 nm MSB and CN TGFET at V_{ds}=-1 V and V_g-V_{th}=0.75 V are shown in Fig.3-18. The activation energies are 0.51 eV and 0.54 eV for MSB and CN TGFET, respectively. The fact that there is almost the same activation energy implies that the MSB junction is very close to the pn junction and the low temperature process of 600°C is sufficient to drive dopants out of the silicide. Since the S/D implantation does not directly damage the Si region of the MSB TGFET and the CN TGFET experiences high temperature post-S/D implantation annealing, the low activation close to half of the energy gap cannot be explained by the defects in the Si region. The leakage current mechanism of pn junction formed by the ITS process has been investigated in the literature [3-15]-[3-22]. Since the Si region is almost defect-free, the area component of leakage current is dominated by the diffusion mechanism even at room temperature. However, the peripheral component of leakage current is dominated by the surface generation current due to the surface states at the isolation edge within the depletion region. For a square junction with area smaller than 10 μm^2, the leakage current will be dominated by the peripheral component at temperatures lower than 200°C. For fully depleted SOI devices, the junction area $T_{Si}xW_f$ is very small. The leakage current would be dominated by the surface generation current due to the surface states at the interface between gate oxide/Si and buried oxide/Si, so the low activation energy becomes reasonable. It is thus proposed that to further reduce the I_{off} of MSB TGFET, the interface quality of gate oxide and buried oxide must be improved.

3-4 Conclusions

This paper demonstrates a novel high performance MSB TGFETs with several unique features such as fully silicided S/D, ultra-short SDE, defect free S/D junction, and low temperature processing. A two-step Ni-salicide process is developed to completely convert the Si layer at the S/D region to silicide with controlled lateral silicidation. By inserting an ultra-short SDE using the ITS technique, the Schottky barrier is modified so that the barrier width is suppressed at the on-state and is increased at the off-state. In addition, the triple gate wrapping around the fin also effectively diminished the Schottky barrier by the gate-fringing effect. With a 4 nm thick gate oxide, the I_{on}/I_{off} current ratio over 10^9 is achieved, and the room temperature subthreshold swings of 25 nm and 49 nm MSB TGFETs are as low as 83 and 60.4 mV/decade, respectively. These values are close to the theoretical limitations. The I_{on} of the 25nm MSB p-TGFET at $|V_{ds}| = |V_g-V_{th}| = 1$ V is higher than 108 μA/μm or 325 μA/μm, depending on the definition of channel width. The I_{on} of 108 μA/μm is lower than the conventional devices. However, if we consider the actual deriving capability of devices with the same layout width, the I_{on} of the MSB p-TGFET, 325μA/μm, will be compatible with that of conventional planar MOSFETs. The contact resistance between silicide and heavily doped Si region increases greatly in the TGFET due to the nano-scale contact area, and this resistance may degrade device performance if not carefully controlled. Therefore, the contact resistance of the MSB junction must be examined so that the limitation of MSB TGFET can be well understood. Test wafers for extracting the contact resistance of the lateral MSB junction are currently being processed and the impact of contact resistance on device performance is under evaluation by 3-dimensional simulators. These results will be

reported later.

Activation energy analysis indicates that the SDE effectively modifies the Schottky barrier, resulting in excellent electrical characteristics. The same activation energy of the low thermal budget MSB TGFETs and high thermal budget CN TGFETs confirms that the MSB junction is very close to the pn junction and the low temperature process of 600°C is sufficient to drive dopants out of silicide. Since the leakage current of drain junction at the off-state is dominated by the surface generation current due to the surface states at the gate oxide/Si and buried oxide/Si interface, it is thus proposed that to further reduce the I_{off} of MSB devices, the interface quality of gate oxide and buried oxide must be improved.

Structural analysis shows that as the fin width becomes larger than the silicide grain size, the multi-grain structure results in a rough front edge of the MSB junction, which in turn degrades the short channel device performance. This result indicates that the MSB process is suitable for TGFETs.

Beyond the 65 nm technology node, it is predicted that the metal gate and high-κ gate dielectric must be employed to improve the device characteristics continuously. Furthermore, thermal stability between metal gate and high-κ dielectric is a critical issue because that the conventional S/D process requires a high temperature annealing of at least 900°C. Since the MSB process temperature is around 600°C, the thermal stability issue is relaxed and the interfacial layer formation at high-κ dielectric and Si interface is also reduced. Furthermore, the low thermal budget produced by the ultra-short SDE helps device scale-down. It can thus be considered that the MSB TGFET is a very promising nano-device.

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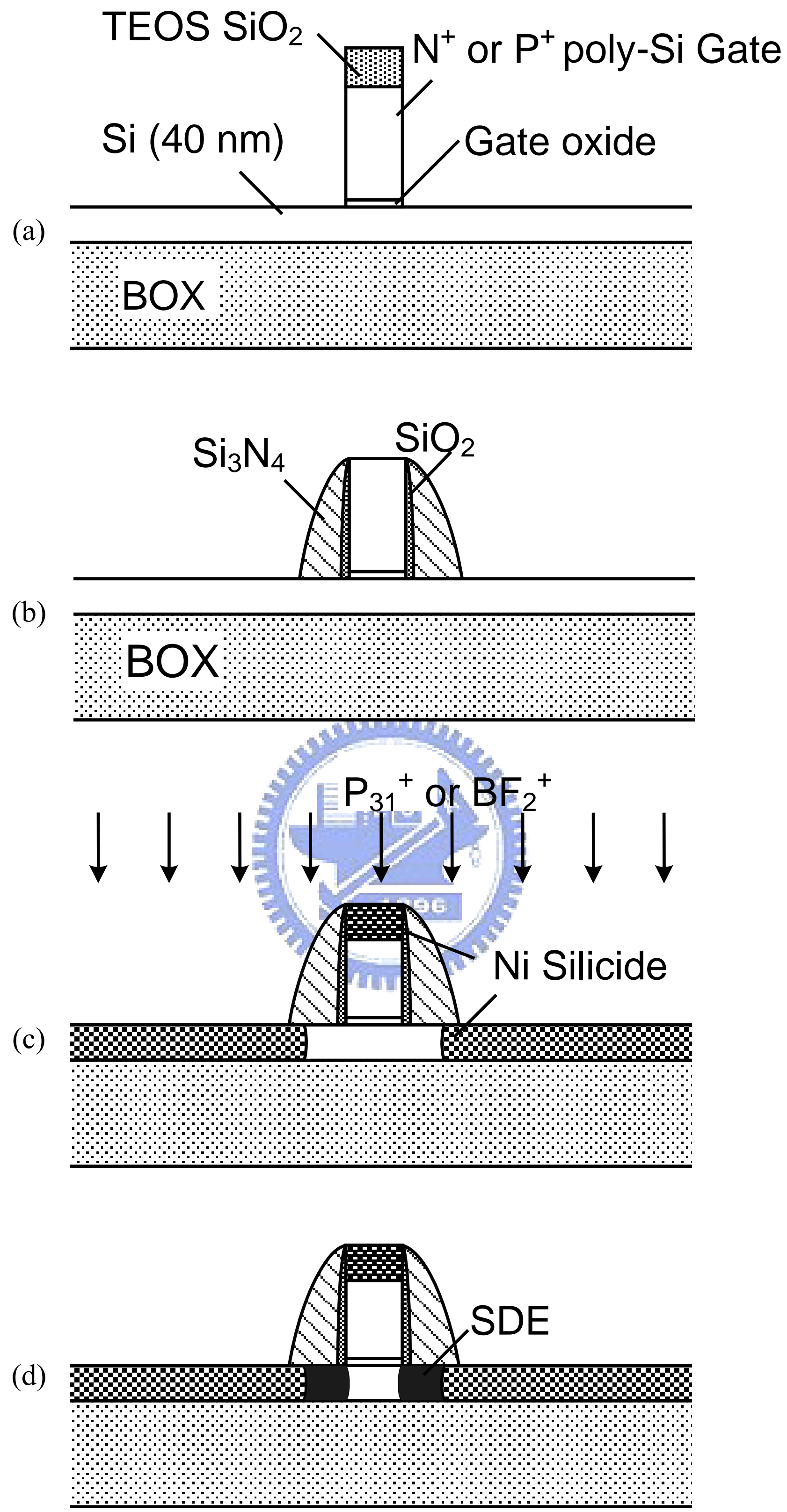

Fig.3-1 Main steps of fabrication process for MSB n- and p-TGFETs.

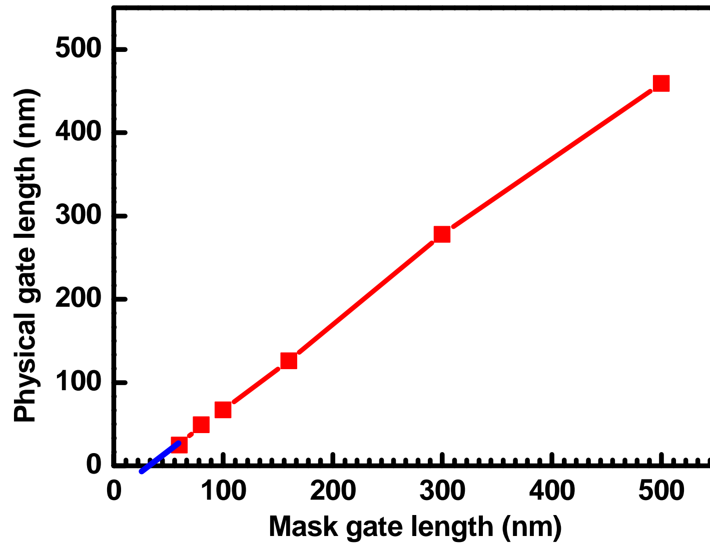

Fig.3-2 Correction between the mask and physical gate length.

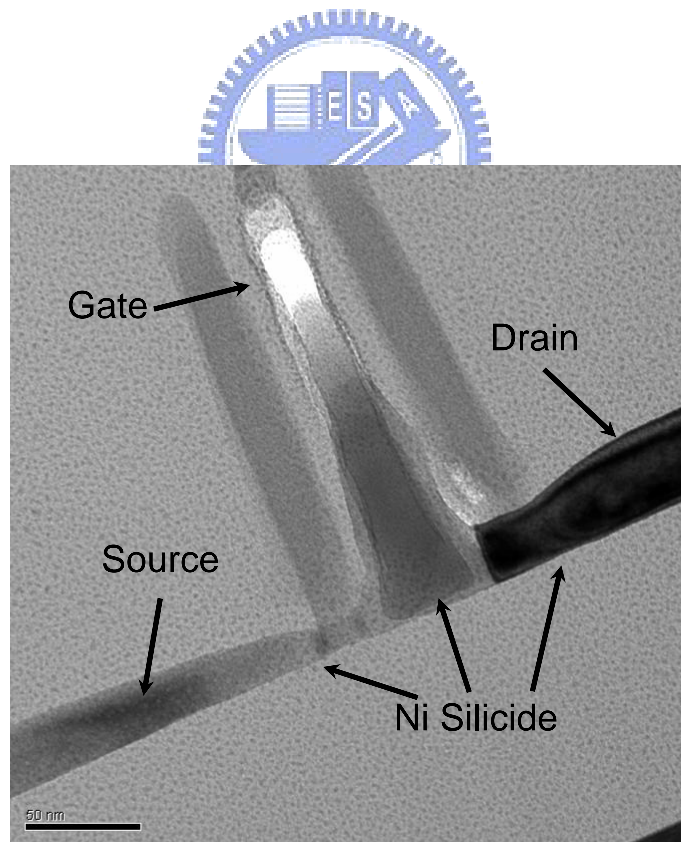

Fig.3-3 Cross-sectional transmission electron micrograph of the 25 nm MSB TGFET fabricated by one-step rapid thermal silicidation at 600°C for 30 seconds.

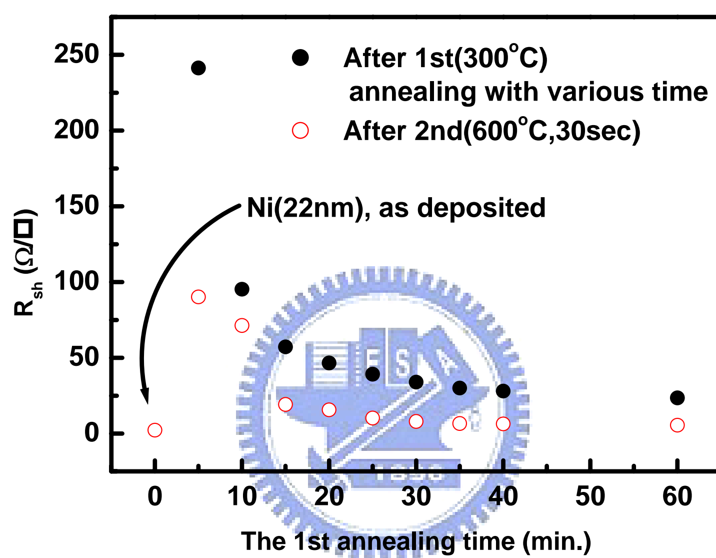

Fig.3-4 The sheet resistance (R_{sh}) of Ni-silicide film on c-Si substrate after 1st and 2nd annealing.

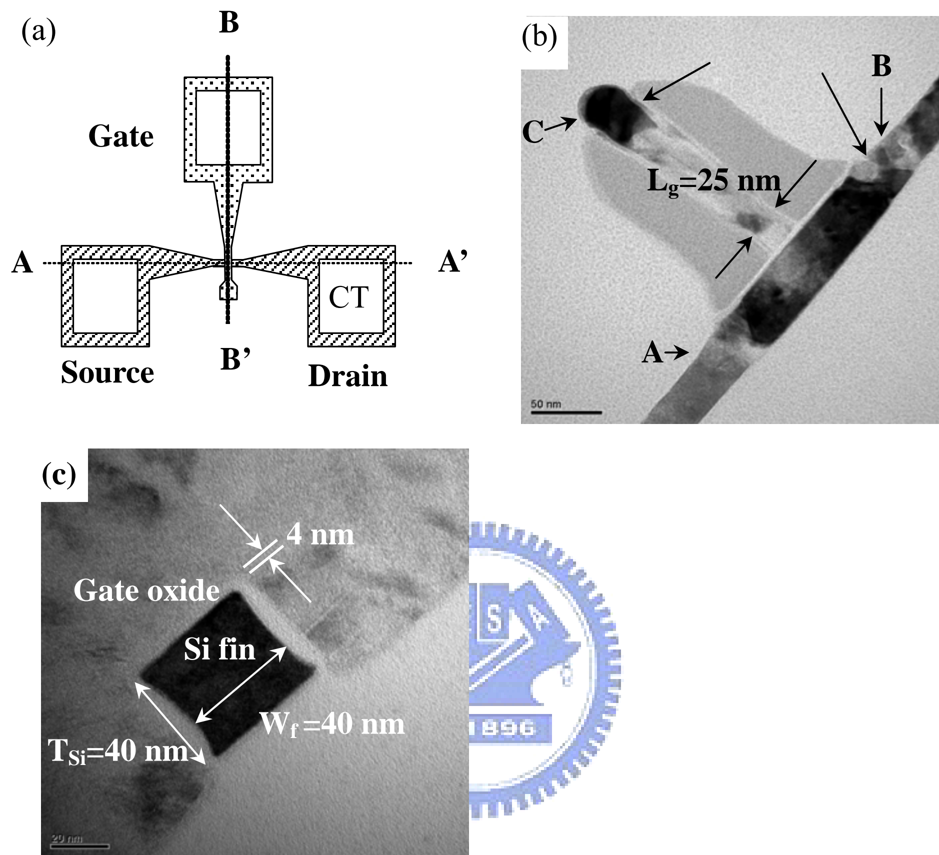

Fig.3-5 Schematic layout and cross-sectional TEM micrographs of the MSB TGFET with gate length (L_g) of 25 nm, fin thickness (W_f) of 40 nm, and fin height (T_{Si}) of 40 nm.

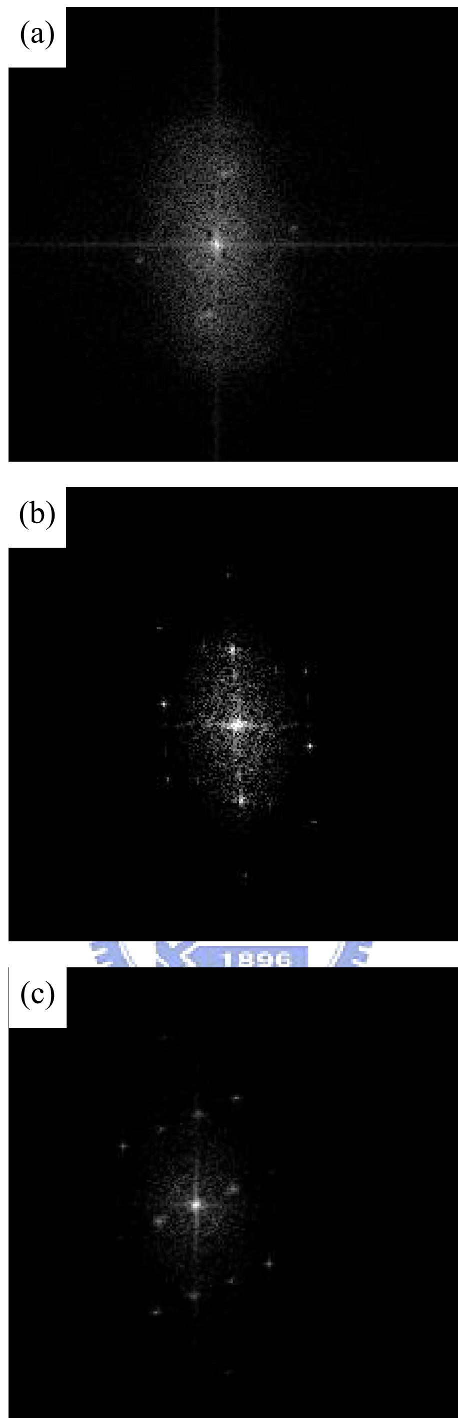

Fig.3-6 Electron diffraction pattern at the positions of A, B (S/D region), and C (gate region) indicated in Fig.3-4(b). The silicide phases at the gate region and S/D region were identified as NiSi and $NiSi_2$, respectively.

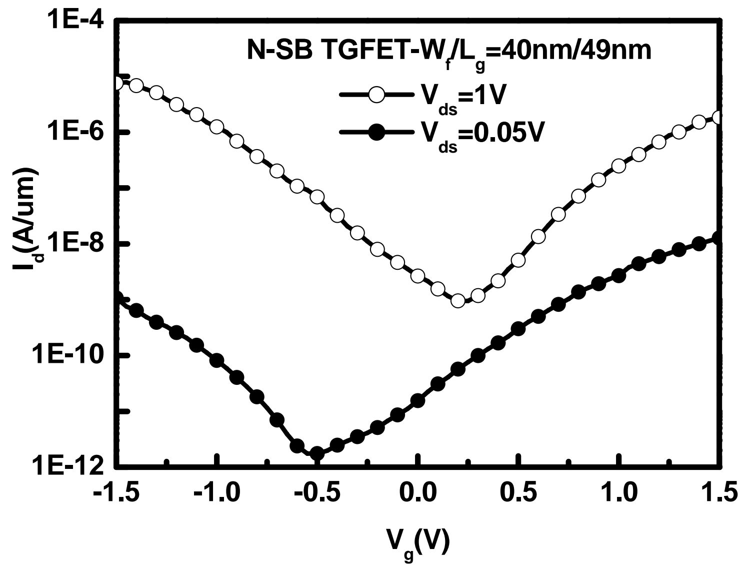

Fig.3-7(a) Transfer characteristics of SB n-TGFTEs with L_g=49nm, W_f=40nm, and T_{Si}=40nm, respectively.

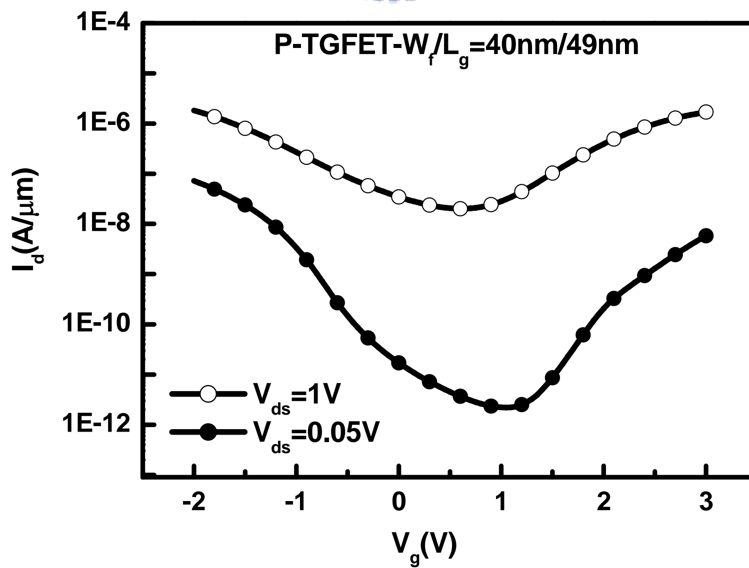

Fig.3-7(b) Transfer characteristics of SB p-TGFETs with L_g=49nm, W_f=40nm, and T_{Si}=40nm, respectively.

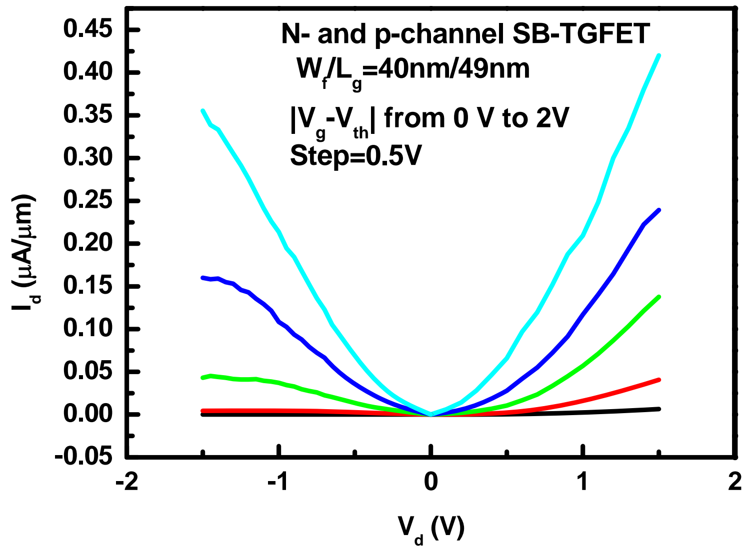

Fig.3-7(c) Output characteristics of SB n- and p-TGFETs with L_g=49nm, W_f=40nm, and T_{Si}=40nm, respectively.

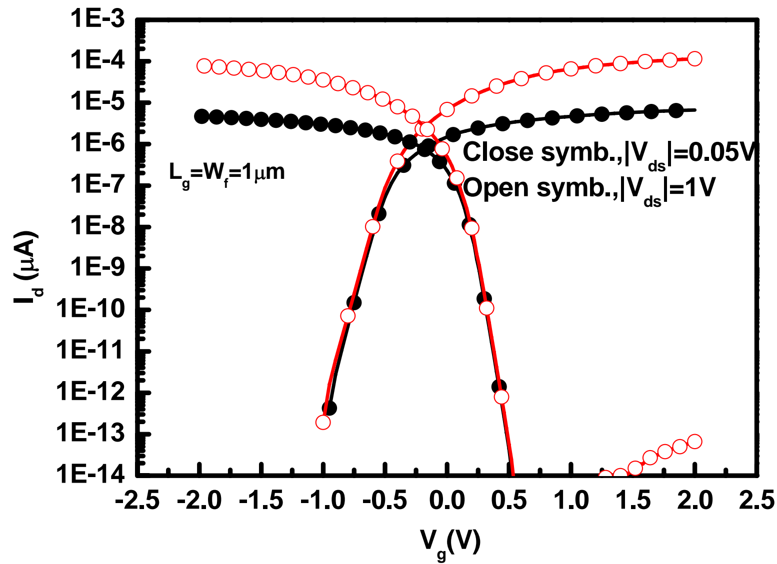

Fig.3-8(a) Transfer characteristics of MSB n-and p-channel Devices with L_g=W_f=1 μm and T_{Si}=40nm, respectively.

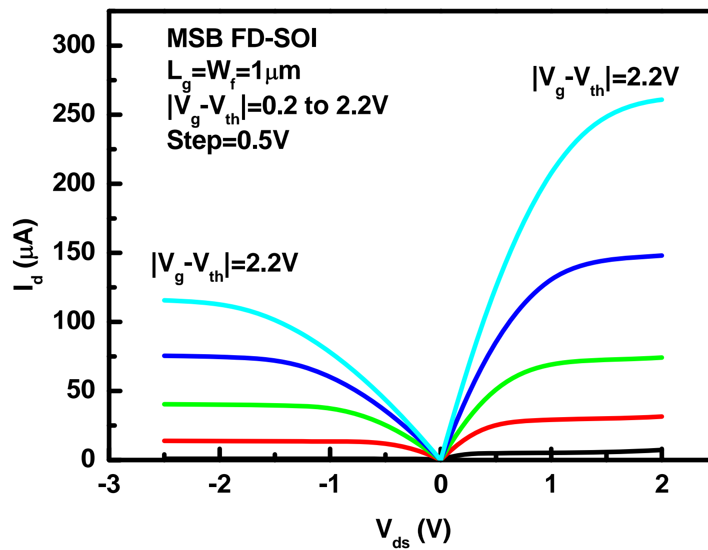

Fig.3-8(b) Output characteristics of MSB n-and p-channel Devices with L_g=W_f=1 μm and T_{Si}=40nm, respectively.

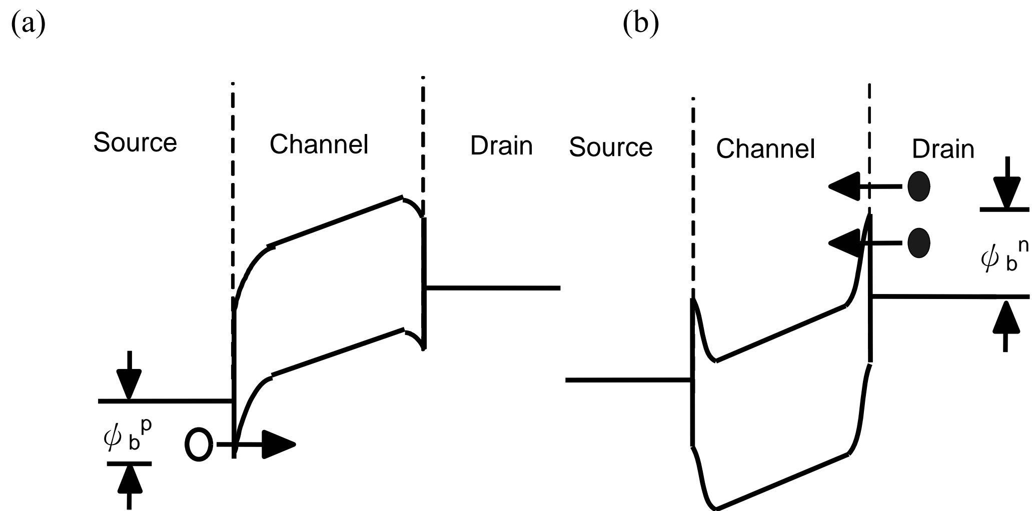

Fig.3-9 (a) On-state and (b) off-state schematic band diagrams of SB devices.

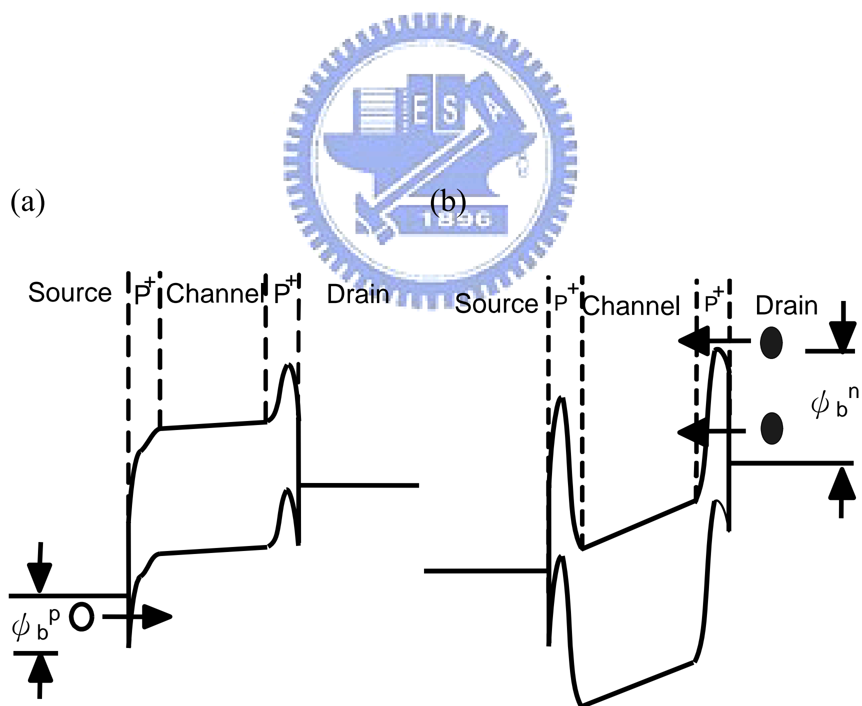

Fig.3-10 (a) On-state and (b) off-state schematic band diagrams of MSB devices.

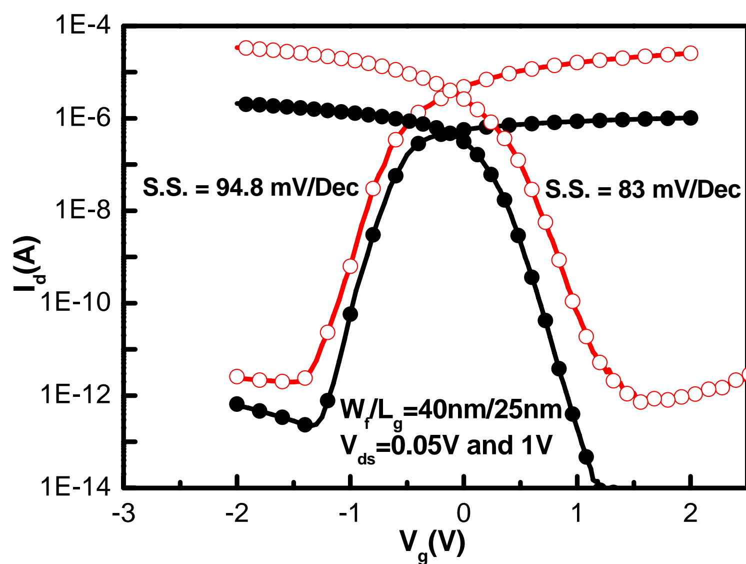

Fig.3-11(a) Transfer characteristics of MSB n-and p-TGFETs with L_g=25nm, W_f=40nm, and T_{Si}=40nm, respectively.

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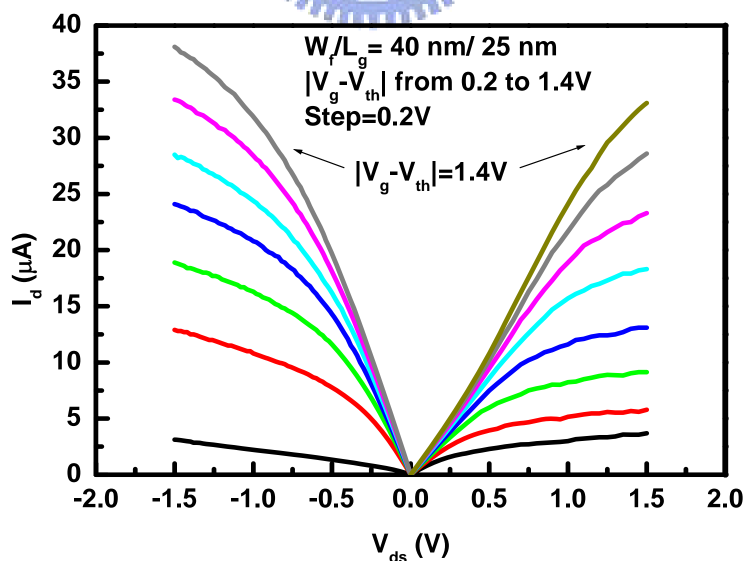


Fig.3-11(b) Output characteristics of MSB n-and p-TGFETs with L_g=25nm, W_f=40nm, and T_{Si}=40nm, respectively.

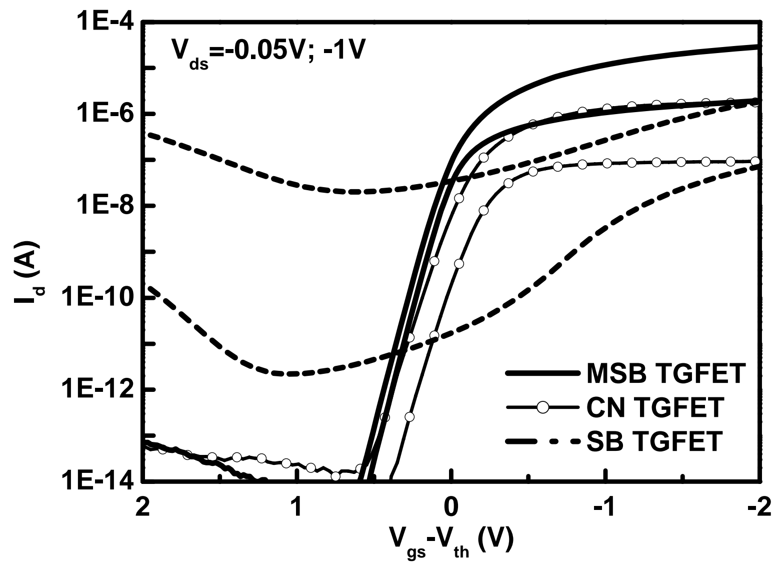
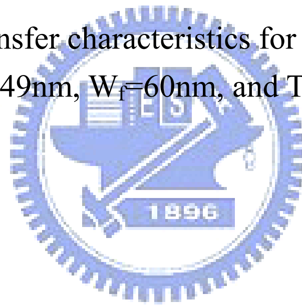


Fig.3-12 Comparisons of transfer characteristics for MSB, SB, and conventional p-TGFET with L_g=49nm, W_f=60nm, and T_{Si}=40nm, respectively.



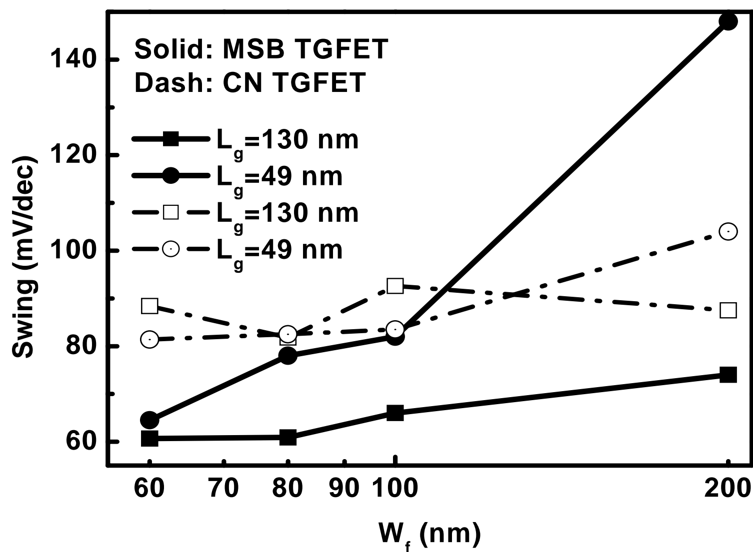


Fig.3-13 Subthreshold swing of MSB and CN TGFETs with different fin thicknesses as L_g = 130 nm and 49 nm.

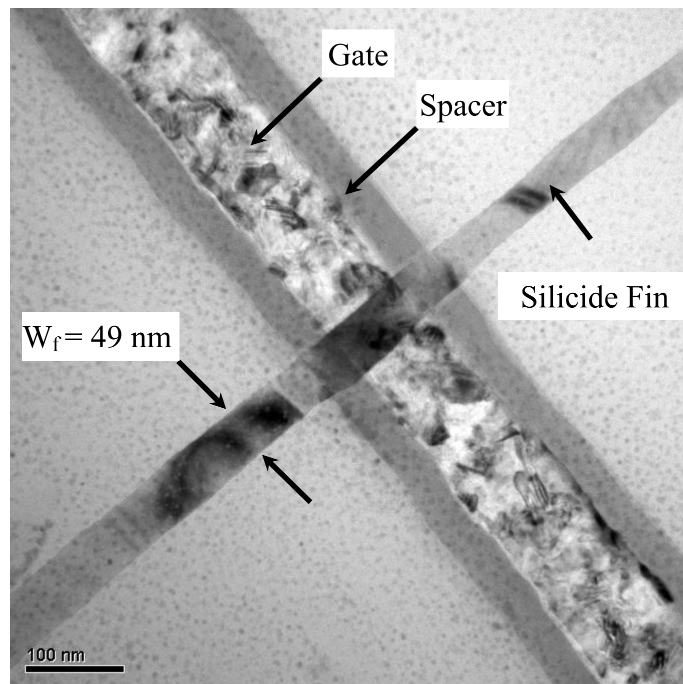
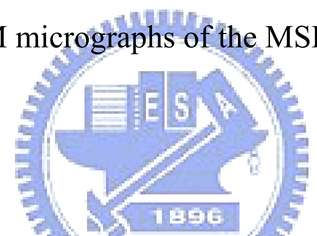


Fig.3-14(a) Plane view TEM micrographs of the MSB TGFETs with W_f=49nm.



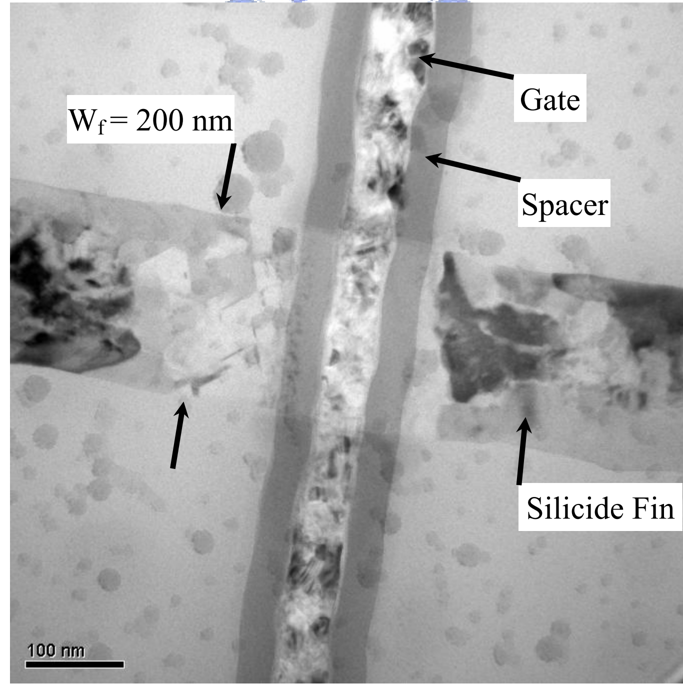


Fig.3-14(b) Plane view TEM micrographs of the MSB TGFETs with W_f=200nm.

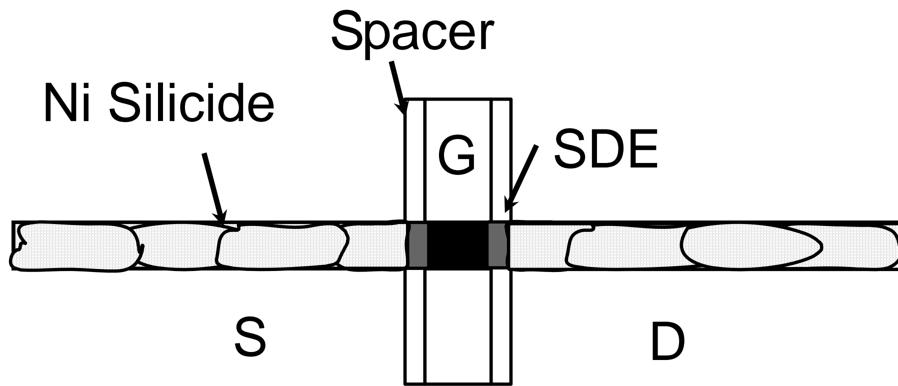


Fig.3-15(a) Schematic drawing of the grain structure at the S/D region and the SDE profile of the MSB TGFETs with W_f=49nm.

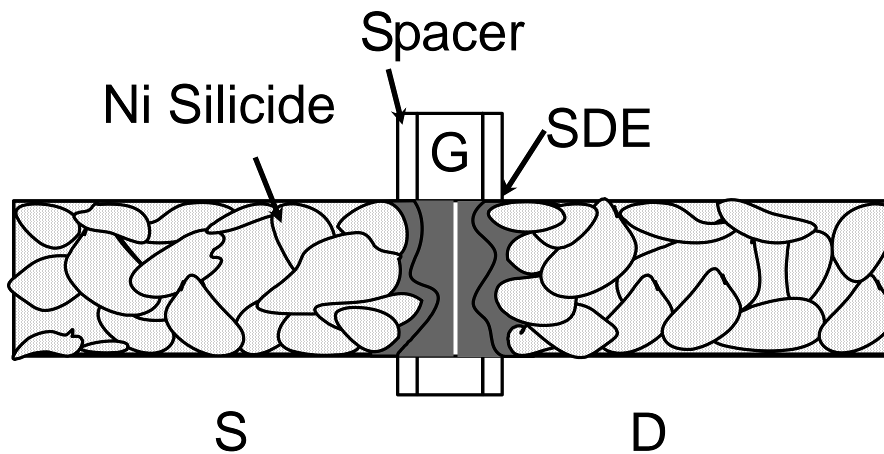


Fig.3-15(b) Schematic drawing of the grain structure at the S/D region and the SDE profile of the MSB TGFETs with W_f=200nm.

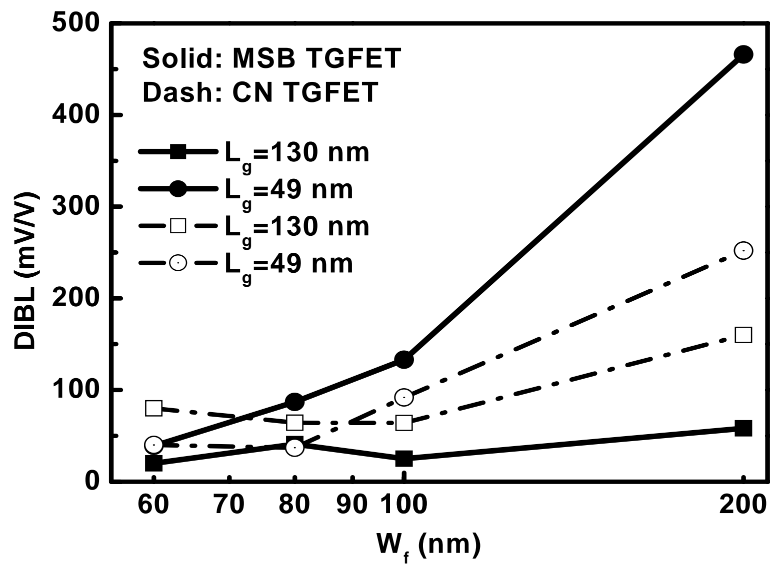


Fig.3-16 Drain-induced-barrier-lowering of MSB and CN TGFETs with different fin thicknesses as L_g=130nm and 49nm.

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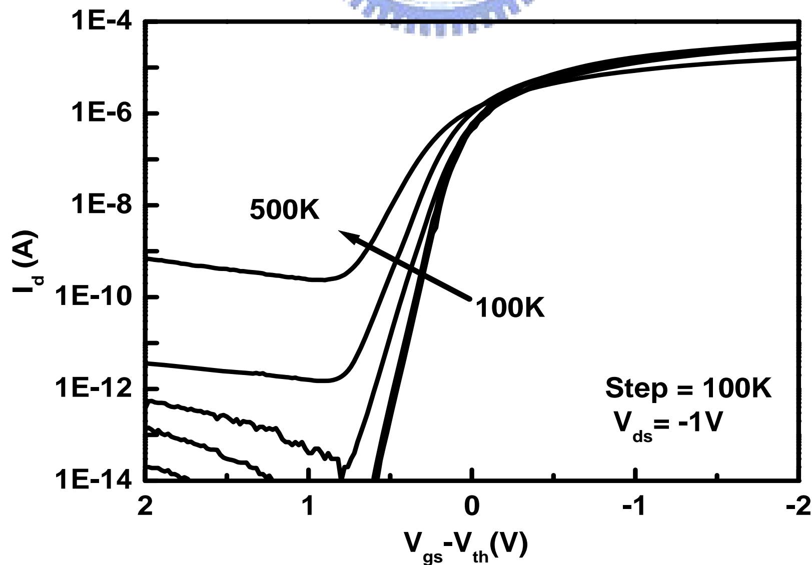
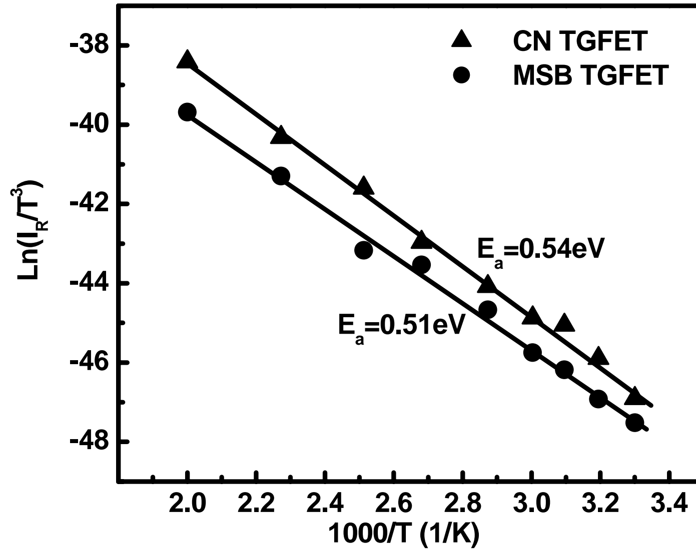


Fig.3-17 Transfer characteristics of the MSB TGFET with L_g=65nm W_f=60nm, and T_{Si}=40nm measured at temperatures from 100K to 500K.



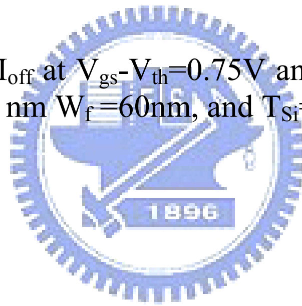


Fig.3-18 Arrhenius plots of I_{off} at V_{gs}-V_{th}=0.75V and V_{ds}=-1V of the MSB and CN TGFETs with L_g=6 nm W_f =60nm, and T_{Si}=40nm.

Chapter4

Impact of Geometry on the Reliability of Tri-Gate FETs (TGFETs)

4-1 Introduction

Reliability issues have been serious concerns for CMOS technologies for the last three decades [4-1]. The most important one is the hot-carrier injection (HCI). The general model of HCI is that the hot-carriers are arisen from the high field at the edge of the drain junction, which accelerates the inversion-layer carriers, if the carriers have sufficient energy, and then cause damages by impact-ionization localized at the drain region [4-2]. Generally speaking, for n-channel bulk devices, hot-carriers generated by impact ionization can lead to substrate current and device breakdown. On the contrary, injection of hot-carriers into gate dielectric causes a gate current and leads to degradation of devices parameters such as driving current (I_{on}), transconductance (G_m), and threshold voltage (V_{th}) [4-3]. As the device dimension is shrunk down to sub-micron regime, following either the field constant scaling rule or the quasi voltage constant scaling rule, reliability issues have gained importance. In the constant field scaling, the peak electric field in device increases because of the increase in doping concentration. In the quasi-constant voltage scaling, which is more common, the channel length is scaled more aggressively than the supply voltage, and this enhances the hot-carrier issues [4-4].

On the other hand, for sub-micron p-channel devices, not only the hot-carrier immunity but also the negative-bias-temperature-instability (NBTI) must

be considered [4-5]. Various experimental studies show that positive charges are created both at the SiO_2/Si interface and in the gate oxide under negative gate bias stressing, thereby causing the threshold voltage shift and the channel mobility degradation. One of the most widely accepted models is the reaction-diffusion model that attributes NBTI induced degradation to the de-passivation of the Si-H bonds at the SiO_2/Si interface and the diffusion of hydrogen related species away from the interface [4-6]-[4-7].

The reliability issues of the non-planar multi-gate (MG) FETs are more complex than the conventional bulk CMOS because of the unique structure of narrow width, thin Si active layer, and multiple interfaces. Taking the FinFET structure as an example, Y. K. Choi et. al., suggested that as the fin width decreases, the hot electron energy can be relaxed due to the vertical electric field induced by the side-gate electrode [4-8]. Besides, the Si orientation of fin side, the sharpness of fin corner, and the etching process of Si fin also affects the reliability of the FinFETs [4-9]. However, up to now, the thorough discussion of dimensional impact on the reliability issues for triple-gate FETs (TGFETs) is still required.

In this chapter, we clarify the reliability characteristics of n- and p-TGFETs. The influences of non-planar structures and particular S/D extension processes on the reliability are also studied deeply. First, the instability mechanisms and degradation phenomena due to fin width effect and the silicide front-end roughness effect are all investigated in detail with various bias stress conditions. Then, the long-term reliability of the proposed n- and p-TGFETs stressed at HCI and NBTI conditions are both projected. The superior HC reliability of the devices with narrower fin is confirmed. The 3-dimensional simulation is also applied to demonstrate that the proper balance and decrease of total electric field in the narrow fin is the major reason

of extraordinary hot carrier immunity in TGFETs. Finally, as the gate length (L_g) decreases, the quite exceedingly uniform of the SDE region in the narrow fins is also regarded as a possible mechanism of excellent HC reliability of TGFETs.

4-2 Experiments

Detail fabrication processes for the MSB n- and p-TGFETs studied in this chapter have been described in chapter-3. The fully depleted devices were fabricated on a SIMOX substrate with 150nm thick buried oxide (BOX), 40nm thick Si active layers (T_{Si}), 4nm thick thermally grown gate oxide, and 40nm composite SiO_2/Si_3N_4 spacer. After NiSi was formed at S/D contact, the SDE in the devices between silicide and channel was formed by implant-to-silicide process (ITS) and furnace annealing at 600°C for 30 min.

To investigate the relationship between geometry and reliability of the proposed MSB n- and p-TGFETs, first of all, we must determine the worst stress condition for HCI among three different HC degradation mechanisms according to three different stress bias conditions including $V_g \sim V_{th}$ (parasitic bipolar transistor), $V_g=1/2V_{ds}$ (maximum substrate current), and $V_g=V_{ds}$ (maximum gate current) [4-10]-[4-11]. After the worst bias condition being confirmed, the finding of the most serious degradations of device parameters including threshold voltage (V_{th}), transconductance (G_m), and driving current (I_{on}) are also important. In this way, before the analysis, the geometry dependence of HC immunity, the degradation of V_{th}, G_m, and I_{on} would also be measured, extracted, and compared to each other to find the worst ones. Then, the reliability of devices with different geometry could be investigates according to the worst stress condition and the most serious degradation parameter. It should be noted that all of the HC stress experiments were performed at 300K. The degradations of the

G_m, V_{th}, and I_{on} were measured in the linear region (V_g=1V and V_{ds}=50mV). At last, to identify the degradation mechanism more clearly, the electric field distribution in Si fin was simulated using ISE TCAD for TGFETs with various W_f/T_{Si} ratios [4-12]. The roughness of the silicide front with W_f=40 nm and 200 nm were also examined by planar view transmission electron microscopy (TEM) inspection.

The p-TGFETs were also stressed at NBTI conditions. In NBTI conditions, as shown in Fig.4-1, the S/D and back-gate bias (V_b) were grounded and the front gate was stressed with different negative biases at 125 °C. Then, the degradation of threshold voltage (V_{th}), transconductance (G_m), and driving current (I_{on}) were all measured at linear region (V_g=1V and V_{ds}=50mV). Similar to the analysis procedure of HCI, the worst degradation parameters, the NBTI degradation mechanisms, and the geometry impact are all examined.

4-3 Results and Discussions

4-3-1 Worst HC Stress Conditions for TGFETs

First, the worse bias condition for HC stress was determined for p-TGFETs. In the case of bulk Si MOSFETs, the relevant operation regimes are the maximum substrate current (V_g=1/2V_{ds}) and the maximum gate current (V_g=V_{ds}) conditions. However, for SOI transistors, hot carriers can also be generated by the action of the parasitic bipolar transistor (PBT) which strongly affects the electrical properties in the low gate voltage range (V_g=V_{th}) [4-13]. Here, for p-TGFETs, in order to determine the worst bias condition, the degradation of G_m, V_{th}, and I_{on} after 10000s stress at various bias conditions (V_g=$V_{th,}$ V_g=V_{ds}/2, V_g=V_{ds}) were shown in Fig. 4-2 (a)-(c). The V_{ds} was fixed at -2.2V. It is observed that at lower V_g bias (V_g~V_{th}), the device

aging decreases with the reduction of gate voltages. S. H. Rean et al. have demonstrated that it could be mainly associated to the slightly alleviative PBT effect due to the decrease of the impact ionization rate for whole channels and fully-depleted structure [4-10]. Especially at $V_g=V_{th}$, it is worth to mention that small reverse aging occurs due to an electron current injection into the gate oxide. Therefore, the worst case of V_{th}, G_m, and I_{on} degradation is induced by hot holes and determined to be at $V_g=V_{ds}$ condition.

To understand the degradation mechanism more clear, the time-dependence power-law plot ($\Delta=At^n$) for I_{on} degradation ($\Delta I_{on}/I_{on}$) vs. stress time with various stress conditions was also displayed in Fig. 4-3. It is clear that the exponent n (slope in a log-log plot) obtained are 0.4 at $V_g=V_{ds}$, 0.55 at $V_g=1/2V_{ds}$, and 0.64 at $V_g\sim V_{th}$. Sinha et al. have reported that electron or hole injection alone causes a power law with n~0.25 and both electron and hole injection in the meantime leads to ~0.5 value for SIMOX devices. In this work, for devices stressed at $V_g=V_{ds}$, the n value about 0.4 shows that the devices are damaged by both electron and hole injection [4-13].

On the other hand, to determine the worst bias condition of n-TGFETs, the parameters aging for n-TGFETs with L_g=130nm, W_f=60nm, T_{si}=40nm stressed at various bias conditions including $V_g=V_{ds}$, $V_g=1/2V_{ds}$, and $V_g=V_{th}$ were examined. Several reports have demonstrated that for n-channel FD SOI devices, the parameters degradation at $V_g=V_{ds}$ is worse than those at $V_g=1/2V_{ds}$ which is attributed to the interface traps generation [4-14]-[4-15]. Therefore, we just examined the stress conditions at $V_g=V_{th}$ and $V_g=V_{ds}$, and show the results of I_{on}, V_{th}, and G_m degradations in Fig.4-4(a)-(c), respectively. It is observed that the worst degradation appears at the $V_g=V_{ds}$ stress condition. The parameters variations including decrease of G_m and I_{on} and increase of V_{th} state that the electron trapping in the oxide and

interface state generation dominate the degradation mechanisms.

According to the results shown in Fig.4-2 and Fig.4-4, the worst bias conditions for both n- and p-TGFETs are both at the $V_g=V_{ds}$ bias condition, the maximal gate leakage current condition owing to the interface-state generation. Moreover, because of G_m is the maximum aging parameters among the three parameters (V_{th}, G_m, and I_{on}) at $V_g=V_{ds}$, it is used as a pointer to study the device reliability.

After determining the worst stress condition, the G_m degradation of n- and p-TGFETs under different V_{ds} are shown in Fig.4-5(a) and (b), respectively. As the V_{ds} increases, the G_m degrades more precipitous because more interface-states are generated by the high electric field supplied by the V_{ds} and V_g.

4-3-2 Narrow Width Effect on HC Reliability for TGFETs

For bulk CMOS with shallow trench isolation (STI) structure, as the channel width scales down, the higher vertical electric field would appeared at the isolation edge may worsen the HC degradation [4-16]. Different from bulk devices, for non-planar multi-gate devices, shrinking the channel-width (W_f) down would suppress the HC degradation effectively. Y.-K. Choi et al. have reported that the double-gate FinFETs with narrow fin width (W_f) would relax the HC degradation for the first time [4-7]. This phenomenon could be attributed to the more uniform transverse electrical field in Si due to the side-gates; therefore, the energy of hot carrier induced by impact-ionization at drain side would be reduced and the HC degradation would be relaxed effectively. In this sub-section, to understand the impact of fin width (W_f) reduction on the HC immunity characteristics of TGFETs, the degradation of device parameters under several $V_g=V_{ds}$ stress conditions were tracked

over time for n- and p-TGFETs with two different gate length (L_g=130nm, and 49nm) and various W_f (40, 60, 80, 100, 200 nm) for 10,000 sec.

Fig.4-6(a) and (b) show the linear region (V_g=1V and V_{ds}=50mV) G_m and I_{on} degradations of p-TGFETs, respectively. Perhaps due to the sharp Si fin corner, the mechanical stress induced by S/D silicide, and the non-optimized gate oxide; the resistance of the HCI for p-TGFETs is slightly worse than that reported by others [4-17]. It is observed that the degradation of p-TGFETs with wider W_f is more serious than that of devices with narrower W_f. The HC lifetimes of the p-TGFET devices with different L_g (49 and 130 nm) and W_f are plotted against the reciprocal of the stress voltage in Fig.4-7(a). The lifetime is defined as the stress time to reach 10% degradation in G_m because that G_m is the most degradable parameters among I_{on}, V_{th}, and G_m. As shown in the Fig.4-7(a), p-TGFETs with both L_g=49nm and 130nm meet the 10-yr lifetime requirement under normal operating condition at V_{ds}=-1 V. The extrapolated operation voltages to 10-years lifetime of devices with two different L_g as a function of W_f are shown in Fig.4-7(b). It is surprising that when the W_f decreases from 200 nm to 60 nm, the allowable operation voltage of the device with L_g= 130 nm increases steeply from -1.33V to -1.67V. For the devices with L_g= 49 nm, the allowable voltage increases from -1.04V to -1.61V.

The similar trend is also observed for n-TGFETs. Fig. 4-8(a) shows that the n-TGFETs with L_g=130nm meet the 10-yr lifetime requirement under normal operating condition at V_{ds}= 1 V. As W_f decreases from 200nm to 60 nm, the allowable operation voltage to 10-yrs lifetime requirement increases obviously from 1.41V to 1.61V. Moreover, even under the V_g=V_{th} stress condition, as W_f decreases from 100nm to 40nm, the allowable operation voltage to 10-yrs lifetime requirement also increases obviously from 2.13V to 2.423V, as shown in Fig.4-8(b).

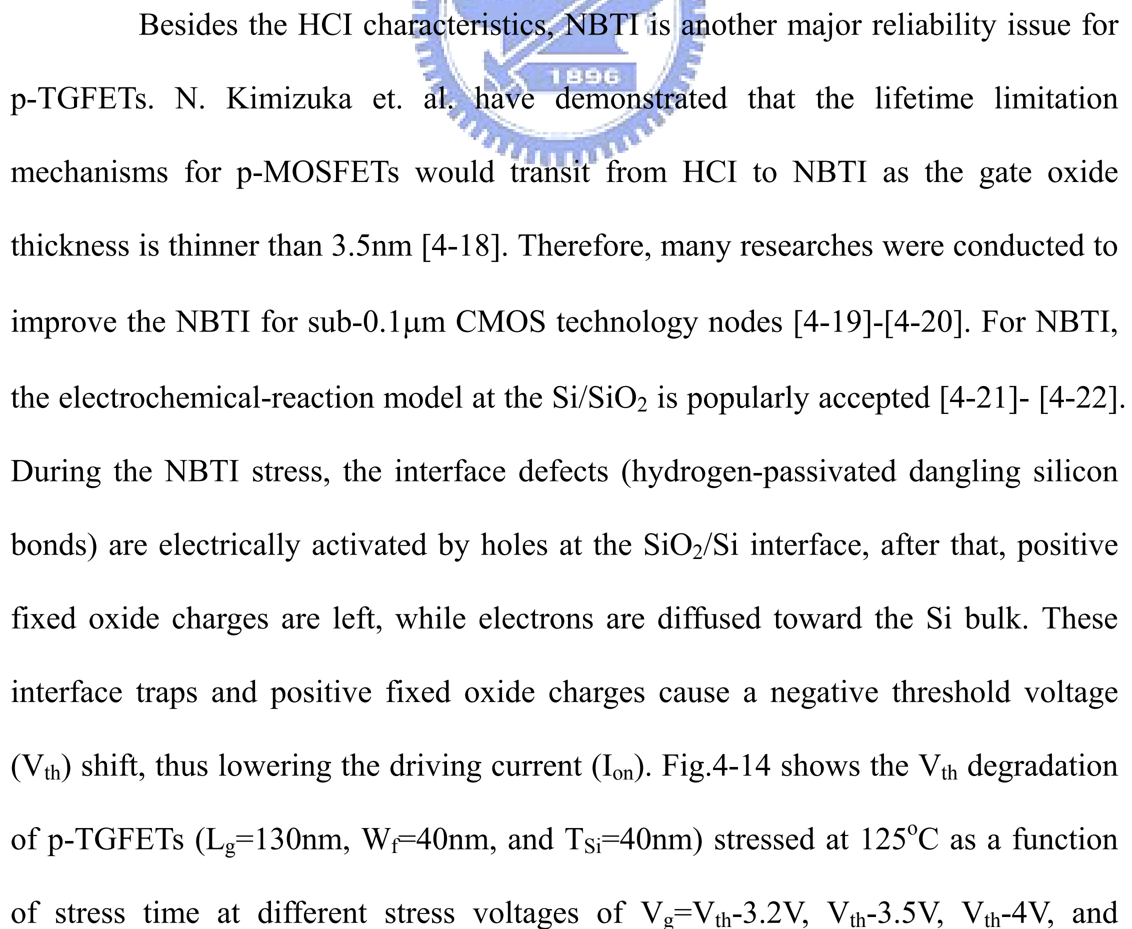
4-3-3 Mechanisms of W_f Dependent HCI for TGFETs

In order to explain the HC degradation dependence on $W_{f,}$ two-dimensional electric field simulation of Si fins with different ratio of W_f/T_{Si} was performed. The potential distribution and electric field direction in Si fin of the TGFET biased at V_g=-2.3 V with W_f=200nm and 40nm are shown in Fig.4-9 and 4-10, respectively. Obviously, as the fin becomes wider, almost the energetic hot carriers are accelerated toward the top gate oxide as shown in Fig.4-9(b). Nevertheless, in the narrow fin, the side-gate electrodes relax the electric field apparently due to the different direction of electric fields induced by the top gate and the two side-gates, as shown in Fig.4-10(b). To observe the electric field distribution in the Si fins with different W_f, the electric field cut-lines at the positions of 5nm (AA' line) and 30nm (BB' line) below the top SiO_2 interface are shown in Fig 4-11(b) and (c), respectively. It should be noted that the electric field along AA' cut-line is larger than that along that along the BB' cut-line owing to the unbalanced vertical electric field along AA' from the top and the two side-gate electrodes. Nevertheless, the narrower fin still has a smaller electric field along both the cut-line of AA' and BB'. Especially along the BB' line, not only the top gate electric field is almost shielded by the two side-gates but the electric field from the side-gates is cancelled out to each other. To speak directly, as the W_f decreases from 200nm to 20nm, the electric field at the center of the BB' line decreases dramatically from 1589V/cm to 393V/cm. According to these results, the electric field in narrower fin is distinctly smaller than that in wide fin so that the hot carriers' energy is reduced effectively.

Another important observation from Fig.4-7(a) and (b) is the allowable operation voltage decrease apparently with the decrease of L_g when the W_f increases

from 100nm to 200nm. In order to explain the different HC degradation rates of the devices with different L_g, it is postulated that the roughness of SDE may affect the HC immunity. The TEM micrographs and schematic drawings of the MSB TGFETs with W_f of 200 and 40 nm are shown in Fig4-12(a) and (b), respectively. When the W_f becomes wider, not only the microstructure of the silicided fin changes from bamboo structure to multi-grain structure, but the silicide/Si interface becomes rougher. Therefore, the uniformity of channel length of the wider devices degrades more than that of the narrower ones. As the wide W_f device shown in Fig.4-13(a), because the channel length along A-A' is shorter than that along B-B', the lateral electric field at A is higher than that at B so that the HCI of wide device becomes poor.

4-3-4 NBTI Phenomena and Mechanisms for p-TGFETs



Besides the HCI characteristics, NBTI is another major reliability issue for p-TGFETs. N. Kimizuka et. al. have demonstrated that the lifetime limitation mechanisms for p-MOSFETs would transit from HCI to NBTI as the gate oxide thickness is thinner than 3.5nm [4-18]. Therefore, many researches were conducted to improve the NBTI for sub-0.1μm CMOS technology nodes [4-19]-[4-20]. For NBTI, the electrochemical-reaction model at the Si/SiO_2 is popularly accepted [4-21]- [4-22]. During the NBTI stress, the interface defects (hydrogen-passivated dangling silicon bonds) are electrically activated by holes at the SiO_2/Si interface, after that, positive fixed oxide charges are left, while electrons are diffused toward the Si bulk. These interface traps and positive fixed oxide charges cause a negative threshold voltage (V_{th}) shift, thus lowering the driving current (I_{on}). Fig.4-14 shows the V_{th} degradation of p-TGFETs (L_g=130nm, W_f=40nm, and T_{Si}=40nm) stressed at 125°C as a function of stress time at different stress voltages of V_g=V_{th}-3.2V, V_{th}-3.5V, V_{th}-4V, and

V_{th}-4.5V. The larger V_{th} degradation is observed at the higher V_g stress bias, which could be attributed to the incremental change in gate electric field E_{ox} and hole-traps concentration [4-23].

The correlation between the fin width and the device parameters degradation are shown in Fig.4-15(a)-(c). The V_{th}, G_m, and I_{on} degradation of p-TGFETs depends on W_f. Similar to the bulk CMOS, attributed to the interface-state generation and hole-traps in the oxide, after NBT stressing, not only the I_{on} and G_m degrade, but the V_{th} shifts to negative direction. It is strange that steep parameters degradations are observed at the narrower fin rather than at the wider fin under the same stress condition. Two mechanisms including the side-surface effect and band-bending effect are suggested to explain this observation [4-23]-[4-24].

It is well known that TGFETs have different trap state density at the interface for each channel due to different crystal orientations, and crystal orientation dependence of NBTI has been reported [4-19], [4-25]. The TGFETs we proposed has (100) top surface and (110) side-surface. The (110) side surface originally has more dangling bonds than the (100) top surface. Moreover, mesa etching process for active silicon may induce extra trap states on the side channel surface. The increase of trap-states degrades NBTI. As the fin width decreases, the area ratio of side-surface to gate oxide/Si interface rises, the trap states density also increases, and then the NBTI degrades.

In addition to the side-surface effect, H. Lee et al. suggested that the stronger band bending effect is a plausible reason of NBTI degradation in the FinFETs. In the FinFET, owing to the lack of body contacts, when the negative bias applied, the electrons generated by NBT stress would be pushed back to the center of the silicon fin and accumulated there. As the fin width decreases, the energy band

bending due to the accumulated electrons at the center of the silicon fin becomes steeper. The sharper energy-band bending at the narrower fin reflected the increase of holes concentration at the interface and accelerated device degradation.

However in our p-TGFETs, because of the thick oxide (T_{ox}=40nm), the degradation attributed to NBTI is slighter than that attributed to HC injection. Therefore, even the trend of geometry effect on NBTI is opposite to that on HCI, in our p-TGFETs, the HCI is still the dominant device degradation mechanism.

4-4 Conclusions

In this chapter, the impact of geometry on the reliability of TGFETs is investigated. The interface-state generation was identified as the major mechanism at first; furthermore, the worst stress condition was determined to be V_g=V_{ds} for both n- and p-TGFETs.

Next, the geometric effect of HC degradation of the devices was studied carefully. The narrower the Si fin width is, the better the HC immunity is. We demonstrated that the electric field in fins induced by the top and the two side-gates dominate the HCI of the TGFETs by two-dimensional TCAD simulation. As the fin width decreases, the net electric field in Si fin induced by side-gate bias is balanced off and shielding the electric field induced by the top-gate. Therefore, the direction of hot-carriers changes from toward top gate to toward side-gate. Furthermore, the energy of hot carrier is also reduced effectively.

On the other hand, the roughness of SDE regions was also suspected to affect the HCI, especially for devices with wide W_f and short L_g. As the result, in the devices with L_g=49 nm, the uniform SDE diffused from the bamboo-like silicided fin relieves the HC degradation in the narrow fin devices.

Besides the HCI, NBTI also affects the reliability of p-TGFETs. The W_f dependence of NBTI is very different from that of HCI degradation - the narrow fin device exhibit worse NBTI than the wide fin device. Two explanations, the worse side-surface effect and the band-bending effect, were suggested. First, for the narrow fin p-TGFETs, the high area ratio of (110) side-surface to (100) top-surface could raise the trap-state density and then exacerbate the NBTI degradation. The other mechanism could be attributed to that the more holes rushed to the SiO_2/Si interface owing to the steeper band-bending induced by the electron accumulation at the center of narrower fin. However, in the proposed devices, the thick oxide may slightly relax the NBTI degradation and the HCI degradation is still the main degradation mechanisms for the proposed p-TGFETs.

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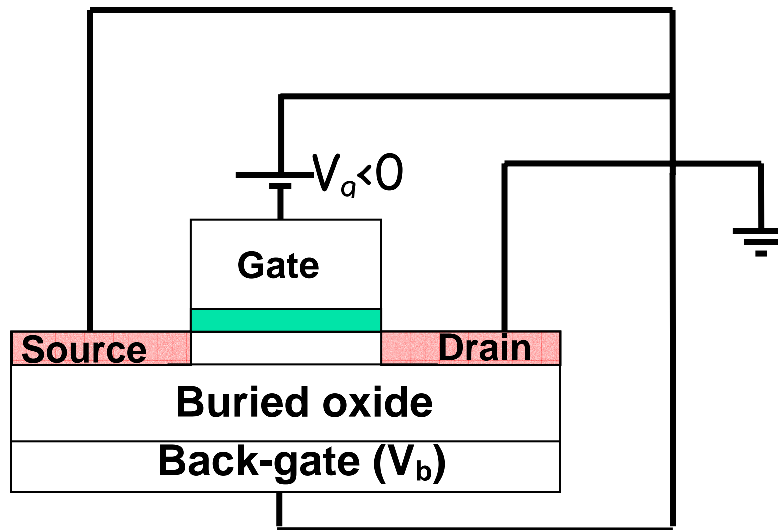


Fig.4-1 Schematic diagram of NBT stress conditions for p-TGFETs. The source, drain, and back-gate are connected to ground. And then, the stress voltage is applied to the gate electrode (V_g).

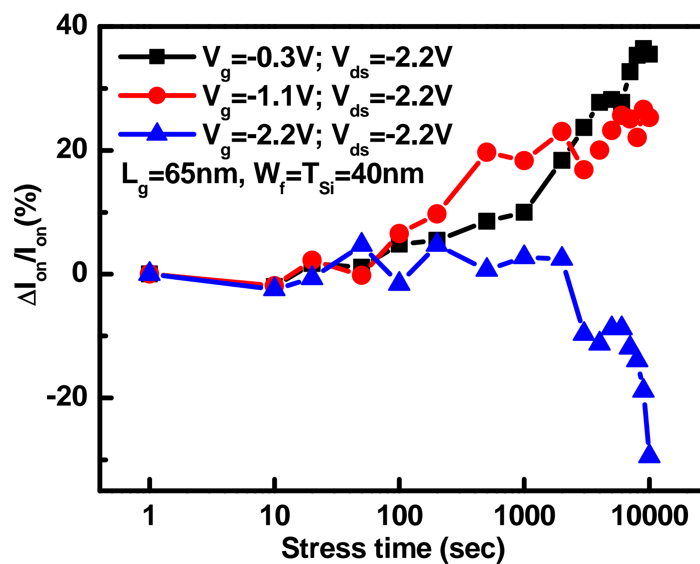


Fig.4-2(a) I_{on} degradation of p-TGFETs (L_g=65nm, W_f=40nm, T_{Si}=40nm) for stress voltages of V_g=V_{th}, V_g=1/2V_{ds}, and V_g=V_{ds}=-2.2V.

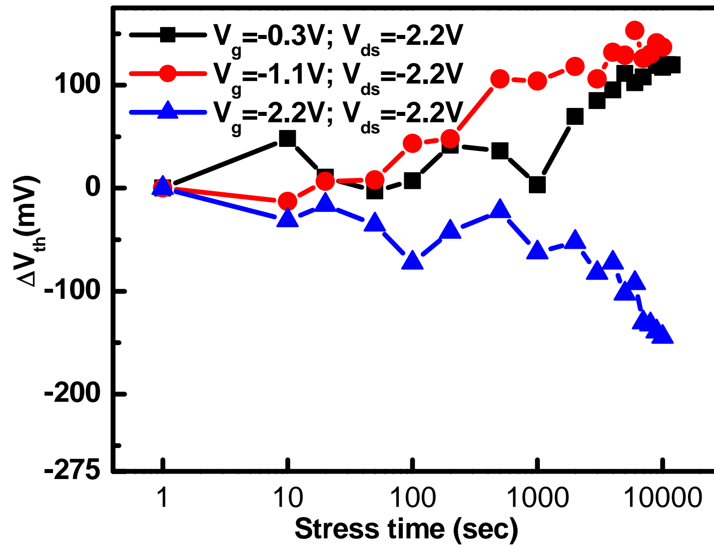
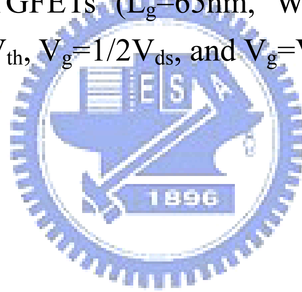


Fig.4-2(b) V_{th} shift of p-TGFETs (L_g=65nm, W_f=40nm, T_{Si}=40nm) for stress voltages of V_g=V_{th}, V_g=1/2V_{ds}, and V_g=V_{ds}=-2.2V.



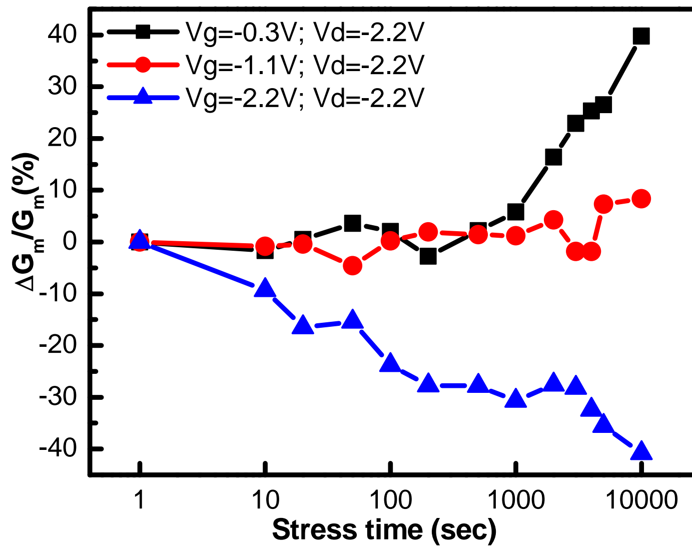


Fig.4-2(c) G_m variations of p-TGFETs (L_g=65nm, W_f=40nm, T_{Si}=40nm) for stress voltages of V_g=V_{th}, V_g=1/2V_{ds}, and V_g=V_{ds}=-2.2V.

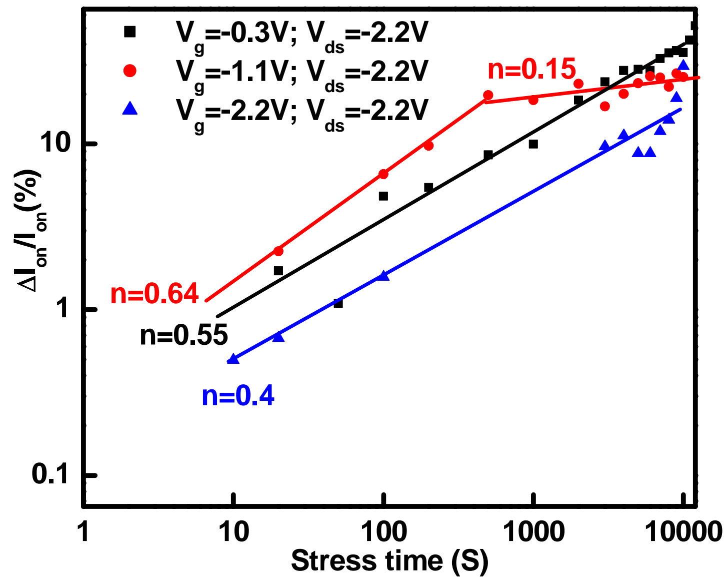


Fig.4-3 Time-dependence power-law plot of $\Delta I_{on}/I_{on}$ vs. stress time for p-TGFETs with L_g=65nm, W_f=40nm, and T_{Si}=40nm stressed at V_g=V_{th},, 1/2V_{ds}, and V_{ds}, respectively.

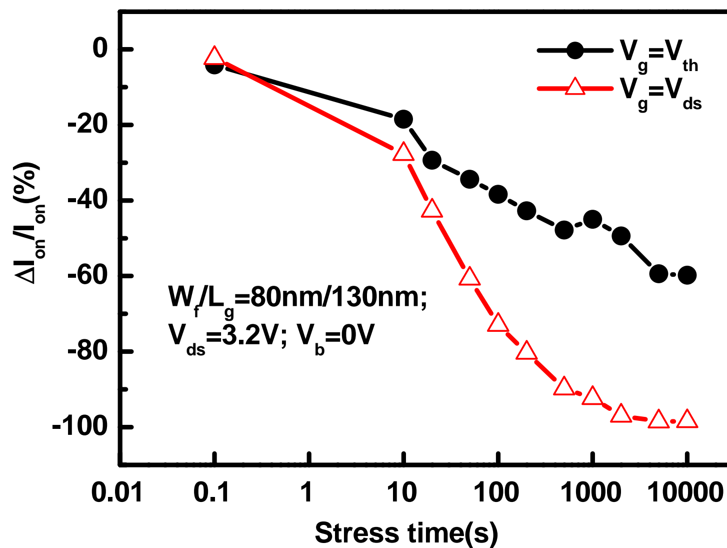


Fig.4-4(a) I_{on} degradation of nTGFETs (L_g=130nm, W_f=80nm, T_{Si}=40nm) for stress conditions of V_g=V_{th} and V_g=V_{ds}=-3.2V.

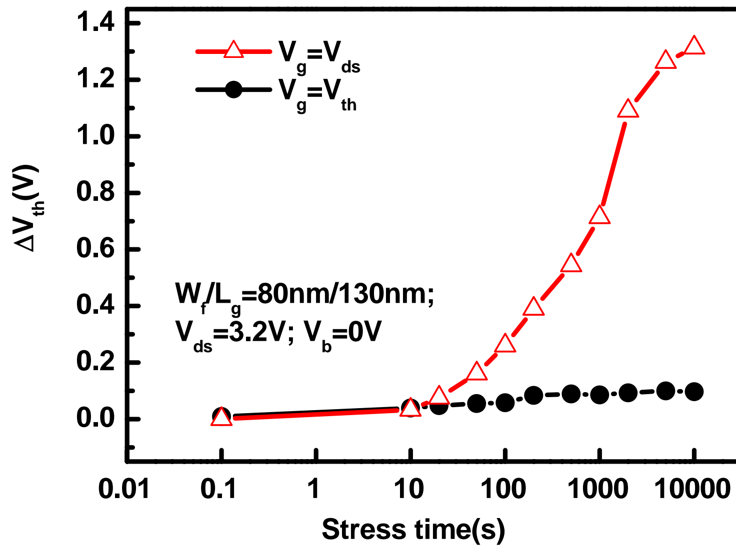
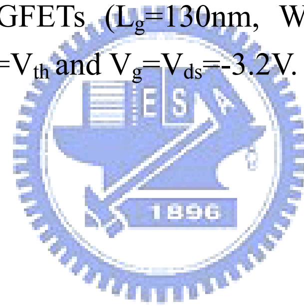


Fig.4-4(b) V_{th} shift of nTGFETs (L_g=130nm, W_f=80nm, T_{Si}=40nm) for stress conditions of V_g=V_{th} and V_g=V_{ds}=-3.2V.



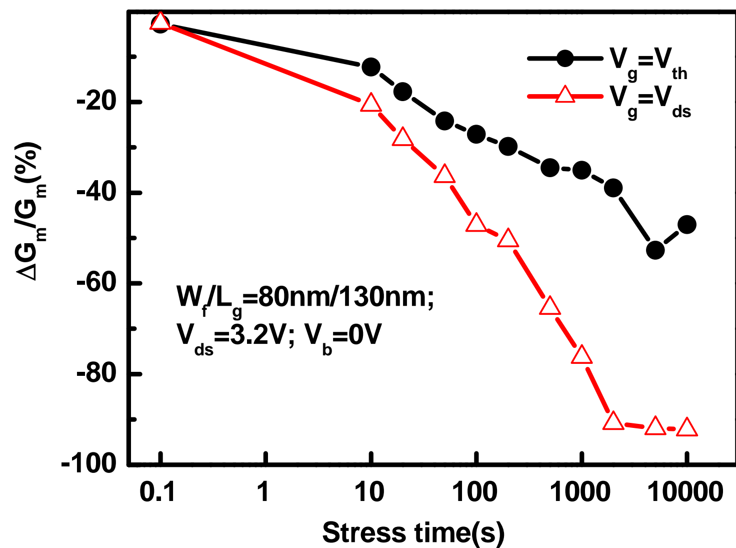


Fig.4-4(c) G_m variations of n-TGFETs (L_g=130nm, W_f=80nm, T_{Si}=40nm) for stress conditions of V_g=V_{th} and V_g=V_{ds}=-3.2V.

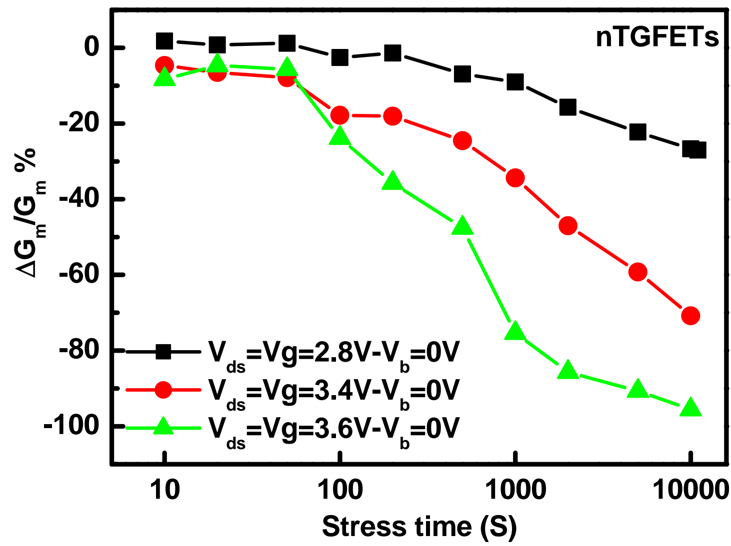
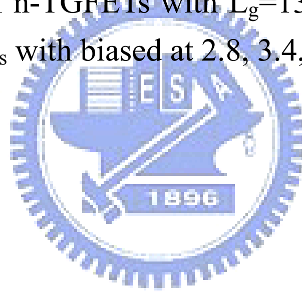


Fig.4-5(a) G_m degradation of n-TGFETs with L_g=130nm, W_f=60nm, and T_{Si}=40nm stressed at V_g=V_{ds} with biased at 2.8, 3.4, and 3.6V.



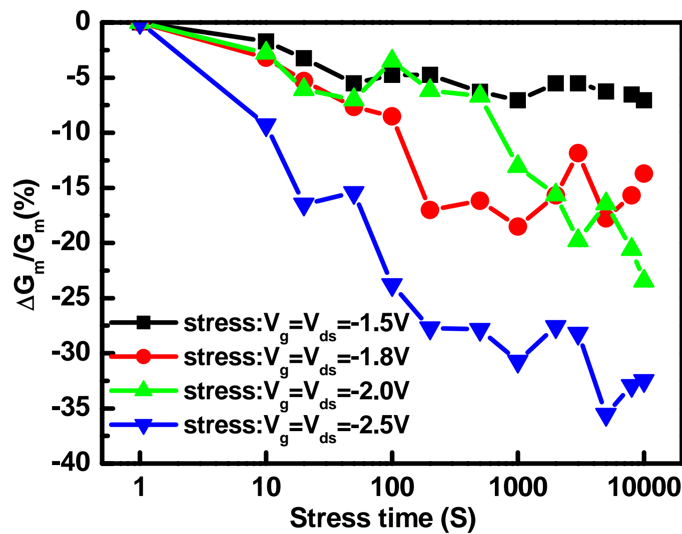


Fig. 4-5(b) G_m degradation of p-TGFETs with L_g=65nm, W_f=40nm, and T_{Si}=40nm stressed at V_g=V_{ds} with biased at -1.5, -1.8, -2, -2.2, and -2.5 V.

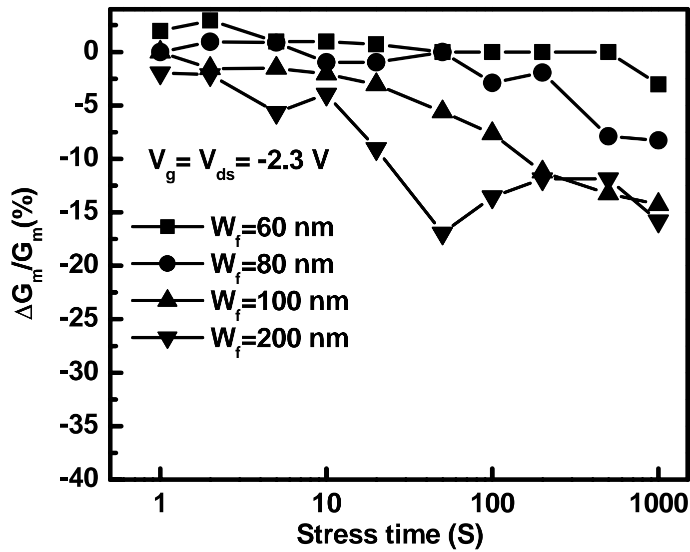
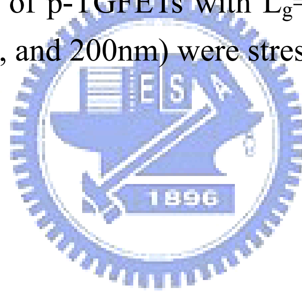


Fig. 4-6(a) G_m degradation of p-TGFETs with L_g=49nm, T_{Si}=40nm, and different W_f (60, 80, 100, and 200nm) were stressed at V_{ds}=V_g=-2.3V.



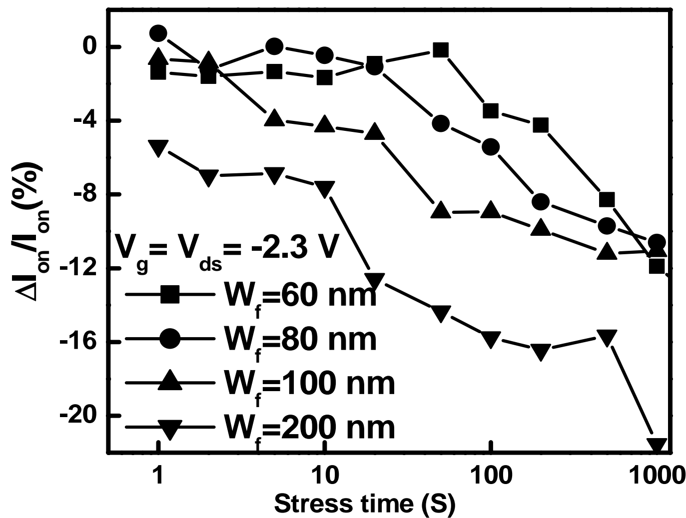


Fig. 4-6(b) I_{on} degradation of p-TGFETs with L_g=49nm, T_{Si}=40nm, and different W_f (60, 80, 100, and 200nm) were stressed at V_{ds}=V_g=-2.3V.

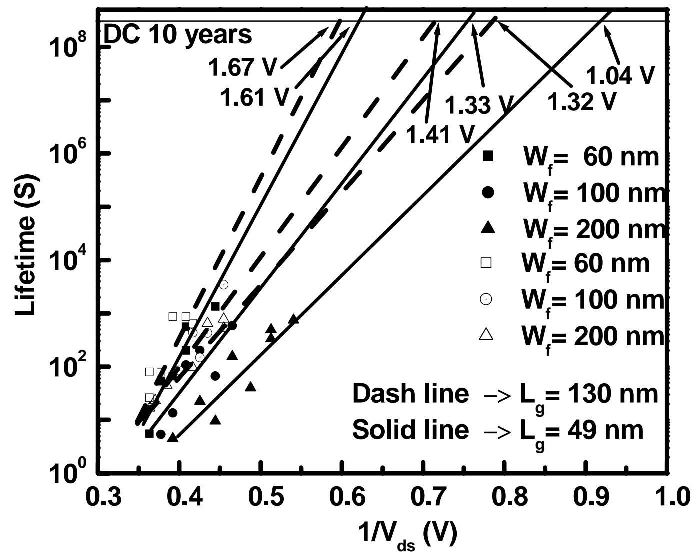
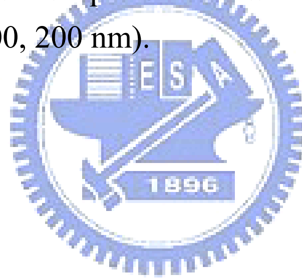


Fig.4-7(a) Lifetime prediction of p-TGFETs with two L_g (130 and 49nm) and several W_f (60, 100, 200 nm).



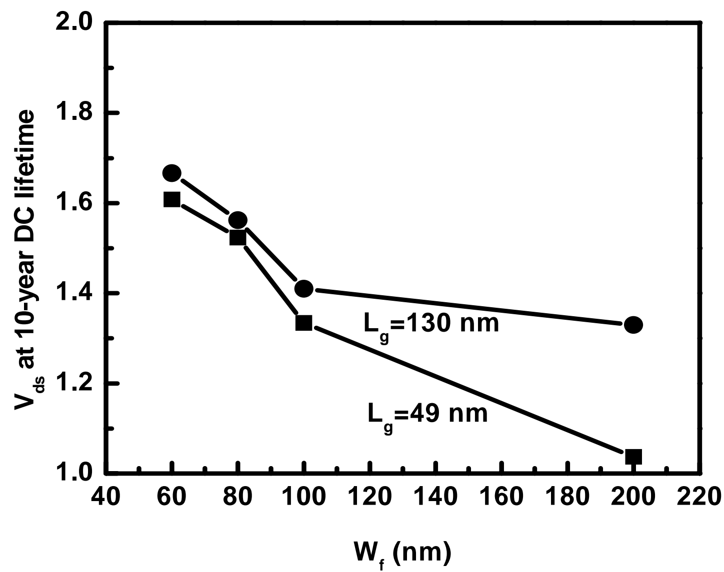


Fig.4-7(b) Operation voltage at 10-yr DC lifetime vs. different W_f.

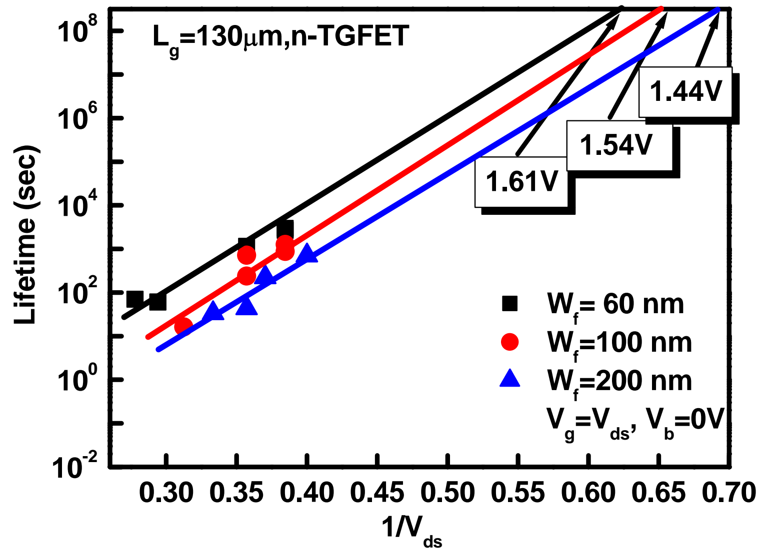


Fig. 4-8(a) N-TGFETs lifetime prediction with different W_f stressed at $V_g=V_{ds.}$

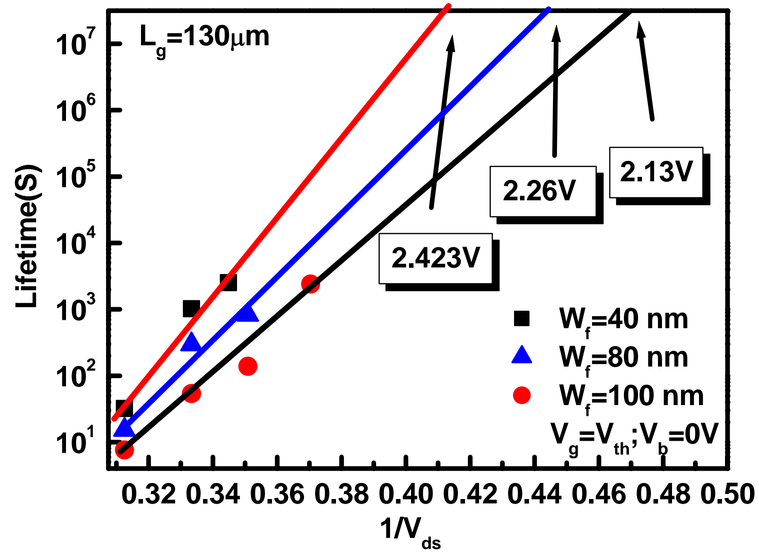


Fig. 4-8(b) N-TGFETs lifetime prediction with different W_f stressed at $V_g=V_{th}$.

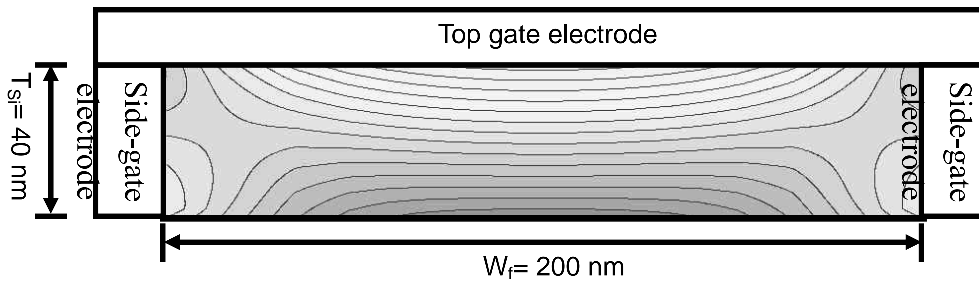


Fig.4-9(a) Potential contour of Si fin with W_f=200nm and T_{Si}=40nm stressed at V_{ds}=V_g=2.3V.

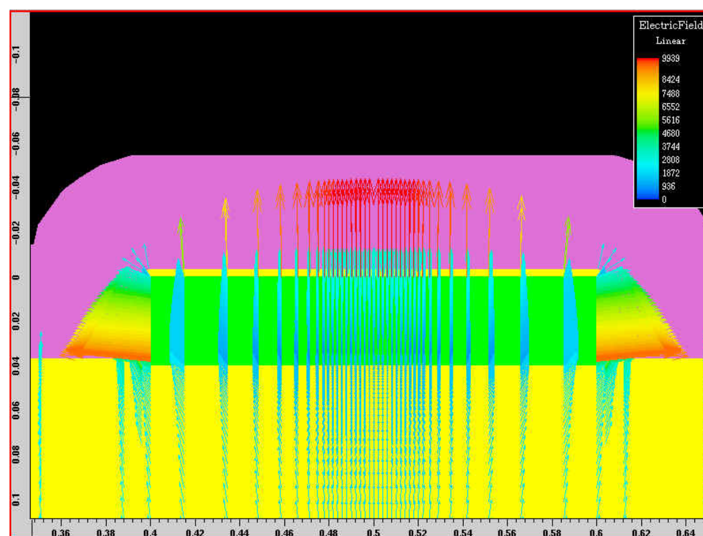


Fig.4-9(b) Electrical field direction of Si fin with W_f=200nm and T_{Si}=40nm stressed at V_{ds}=V_g=2.3V.

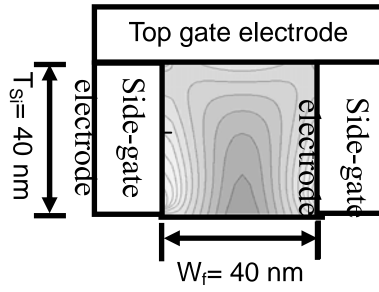


Fig. 4-10(a) Potential contour of Si fin with W_f=40nm and T_{Si}=40nm stressed at V_{ds}=V_g=2.3V.

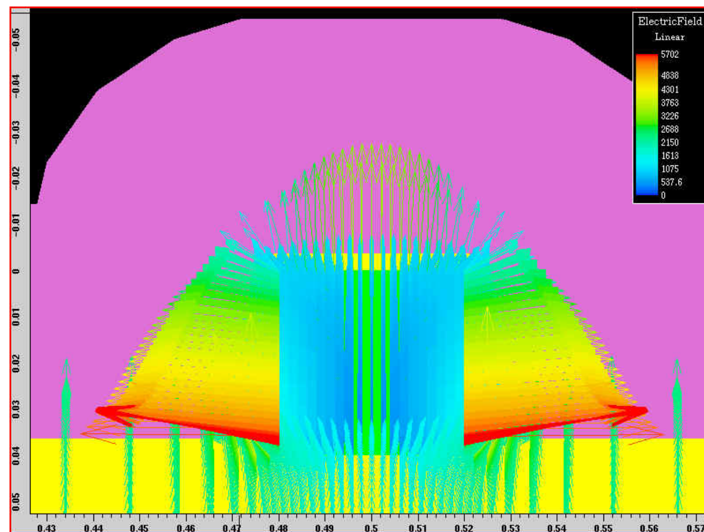


Fig. 4-10(b) Electrical field direction of Si fin with W_f=40nm and T_{Si}=40nm stressed at V_{ds}=V_g=2.3V.

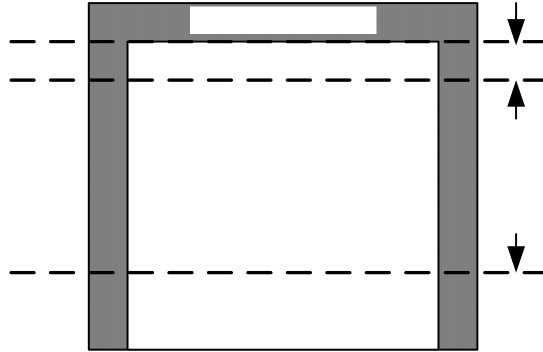
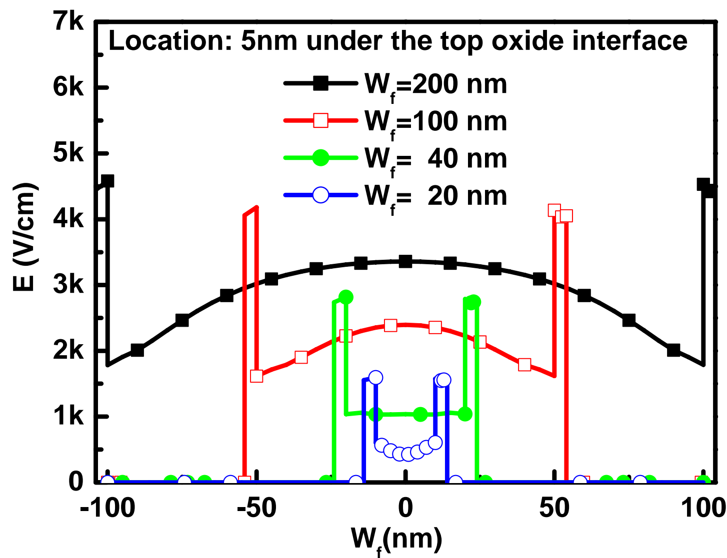


Fig.4-11(a) Cross-sectional schematic view of Si fin with W_f=T_{Si}=40nm. The AA' and BB'cut-line is at 5nm and 30nm under the top interface between SiO_2/Si.



A'

Fig.4-11(b) Electric field strength along AA' cut-lines for Si fin with different W_f increasing from 20 to 200nm.

B'

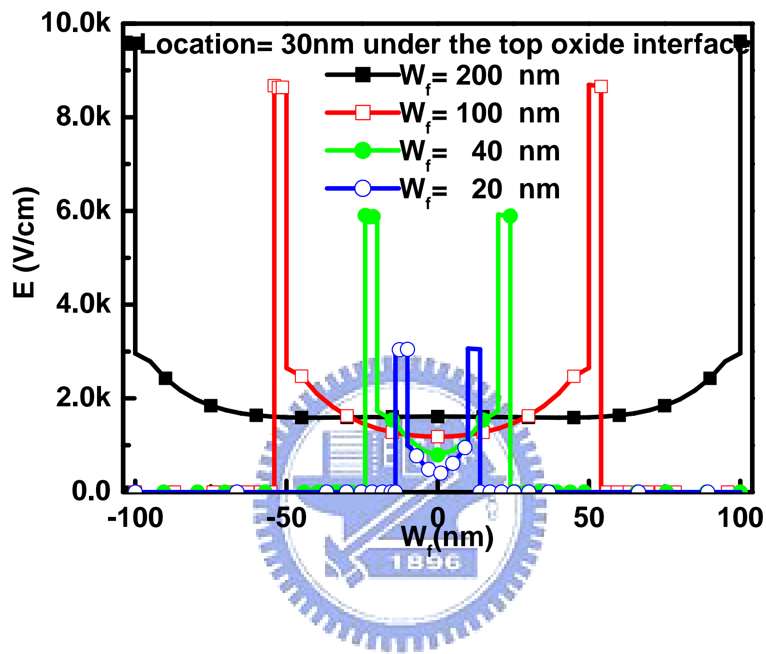


Fig.4-11(c) Electric field strength along BB'cut-lines for Si fin with different W_f increasing from 20 to 200nm.

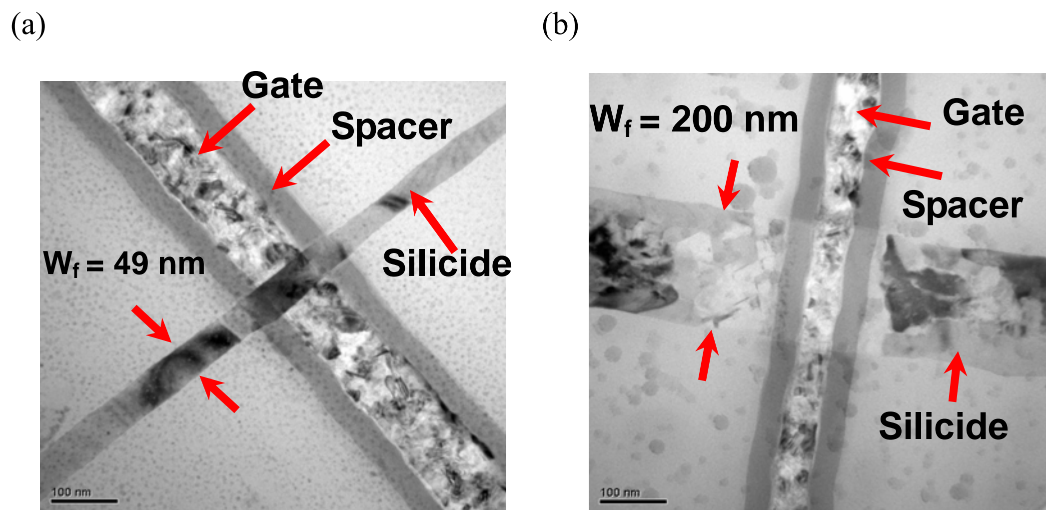


Fig.4-12 TEM planar views of Si fin with (a) W_f=200, L_g=49nm and (b) W_f=40nm, L_g=49nm.

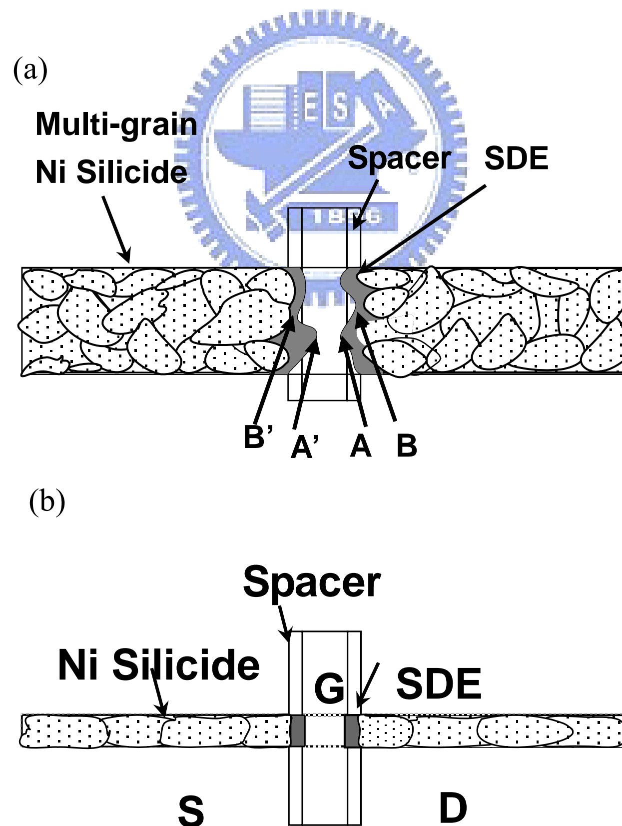


Fig.4-13 Schematic planar views of Si fin with (a) W_f=200, L_g=49nm and (b) W_f=40nm, L_g=49nm.

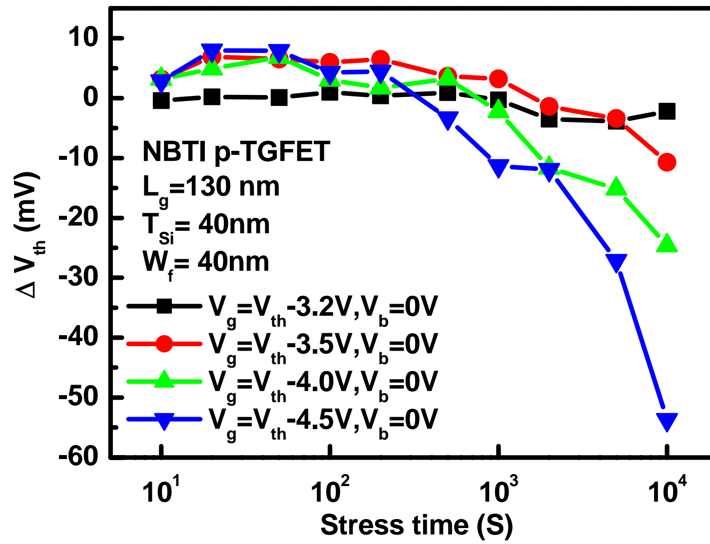
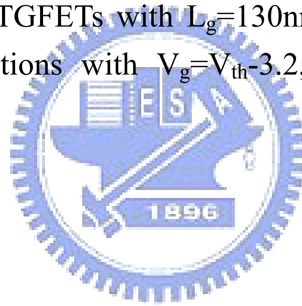


Fig.4-14 Shift of V_{th} for p-TGFETs with L_g=130nm, W_f=40nm, and T_{Si}=40nm at NBTI stress conditions with V_g=V_{th}-3.2, V_{th}-3.5, V_{th}-4, and V_{th}-4.5V, respectively.



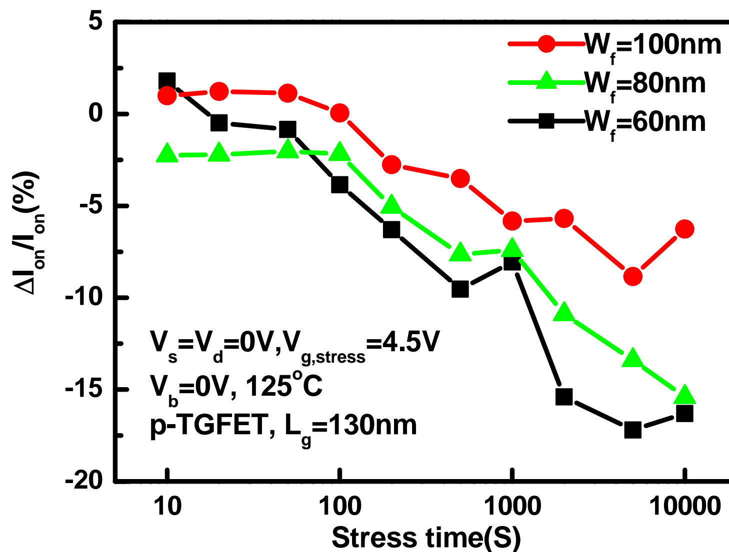


Fig.4-15(a) I_{on} degradation of p-TGFETs with L_g=130 nm, and T_{Si}=40nm and several W_f(60, 80, and 100nm) stressed at V_g=-4.5V and V_d=V_s=0V.

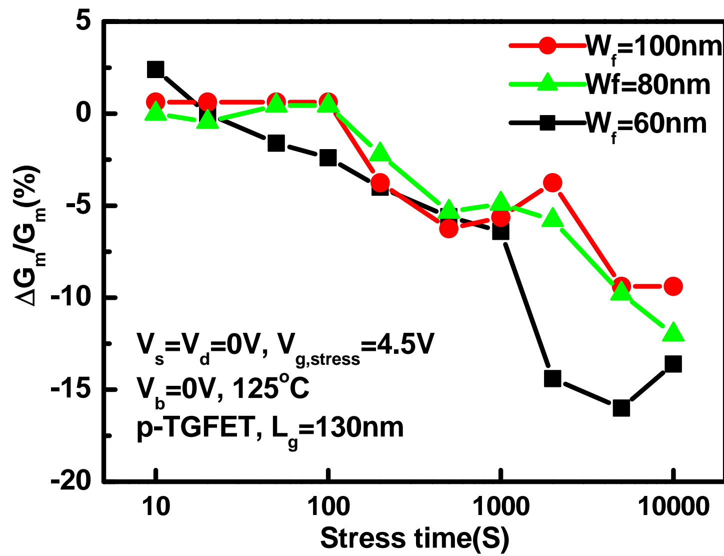
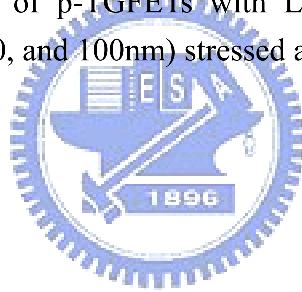


Fig.4-15(b) G_m degradation of p-TGFETs with L_g=130 nm, and T_{Si}=40nm and several W_f(60, 80, and 100nm) stressed at V_g=-4.5V and V_d=V_s=0V.



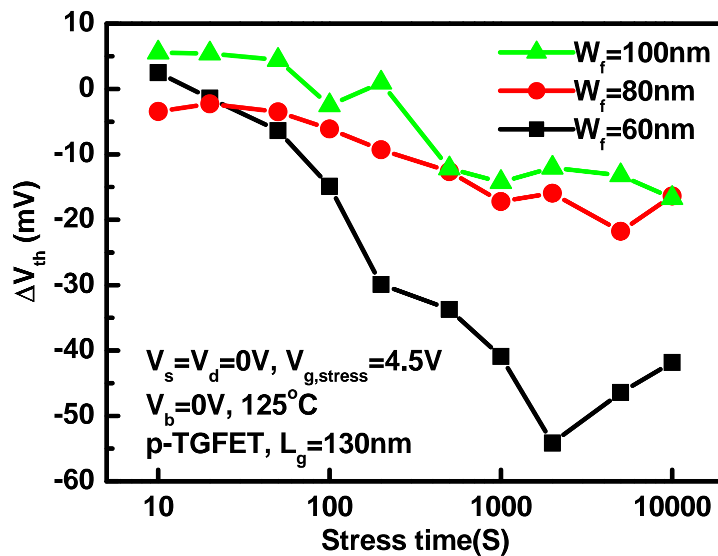


Fig.4-15(c) V_{th} degradation of p-TGFETs with L_g=130 nm, and T_{Si}=40nm and several W_f(60, 80, and 100nm) stressed at V_g=-4.5V and V_d=V_s=0V.

Chapter 5

Back-Gate Bias Effects of Tri-Gate FETs (TGFETs)

5-1 Introduction

After discussing the basic I-V characteristics in chapter 3 and reliability issues including hot-carrier immunity (HCI) and negative-bias-temperature-immunity (NBTI) in chapter 4, we cannot neglect the important charge coupling effect generated by back-gate bias on the performance and reliability characteristics of TGFETs.

For the conventional fully-depleted (FD) SOI device structure, besides the top gate oxide, the buried oxide layer (BOX) is directly contacted with the active region. First, because of the thin SOI films, the basic electrical characteristics such as threshold voltage (V_{th}), transconductance (G_m) and subthreshold swing (S.S.) of FD SOI are typically influenced by the charge coupling between the front and back gates (V_b). Second, due to the bad quality of BOX, large amount of oxide-traps (N_{ot}) and interface-state at the Si/BOX interface would affect the device characteristics and low-frequency (1/f) noise characteristics [5-4]-[5-5]. Especially for the V_{th}, H. K. Lim et. al suggested that as the V_b decreases from positive to negative, on the n-channel FD-SOI, the bottom interface between Si-channel/buried oxide (BOX) will transfer from depletion into accumulation, and therefore, the V_{th} will increase and then saturate [5-1]. As the bottom interface is at the strong accumulation mode, the sensitivity of V_{th} to V_b could be relaxed and the short channel effect for FD-SOI channel length under 0.1μm can be effectively suppressed [5-2]. With optimum

designed buried oxide thickness, it is surprising that the serious DIBL induced by drain voltage penetration through buried oxide to Si channel could also be reduced. By M. Noguchi et. al., a suitable back-gate bias making the interface of Si/buried oxide at weak accumulation mode could improve the V_{th} fluctuation from to the variations of Si film thickness of FD-SOI devices [5-3].

However, in 1989, D. C. Mayer et. al. reported that the Si/bottom oxide interface trap-states and the bottom oxide traps could be varied by high substrate-voltage stressing or irradiation [5-6]. It should be noted that the HC degradation of the SOI is also strongly correlated with the electrically active defects at the Si/buried oxide interface. Especially for the SIMOX wafers used in this work, which have worse quality of buried oxide and high interface-state between Si channel and buried oxide than the BESOI wafers, the reliability of FD-SOI may be more serious [5-7]-[5-8]. Therefore, the method to suppress the V_b coupling to the front-channel attract a lot of interesting. A simple method is to raise the channel doping [5-9]. Nevertheless, the aggravated floating body effect and the Si thickness sensitivity are drawbacks. The novel devices using a different substrate such as Silicon-on-nothing (SON) substrate was also suggested. However, the complicated fabrication process has to be overcome [5-10]. Recently, many novel high performance fully-depleted (FD) non-planar multi-gate FETs (MGFETs), such as double gate, tri-gate, and omega FinFETs were developed as prospective architectures in the nano-regime[5-11]-[5-13]. These novel devices, with more number of gates than conventional single-gate FD-SOI devices, should have different back-gate bias coupling impact owing to their peculiar structure. However, up to now, according to our knowledge, the research about the back-gate bias coupling impact on the MGFETs is still required.

In this chapter, first of all, the effect of back-gate bias on basic I-V characteristics of TGFETs is reviewed and then the excess-side gate effect is also discussed carefully. Besides the demonstration of back-gate bias coupling effect on the basic I-V characteristics, the impacts of back-gate bias on the reliabilities of TGFETs such as HCI for n-TGFET is also described. It is also demonstrated that the TGFETs with narrower Si fin width have better resistance against the effect of back-gate bias by not only the smaller back-interface area but also the electric field shielding by the deep D_{EXT}.

5-2 Experiments

Detail fabrication processes for the n-TGFETs used in this chapter have been described in chapter 2 and 3. These devices were fabricated on SIMOX substrate with 150nm thick buried oxide (BOX), 40nm thick Si active layers (T_{Si}), 4nm thick thermally grown gate oxide, and 40nm composite SiO_2/Si_3N_4 spacer. After NiSi was formed at S/D contact, the SDE in the devices between silicide and channel was formed by implant-to-silicide process (ITS) and furnace annealing at 600°C for 30 min [5-14]. After the devices was fabricated, 500nm thick Al was deposited on the back-side of wafers in a thermal coator as back-gate contact.

Prior to reliability stress, we first examined the front-channel device characteristics as a function of back-gate bias (V_b). The parameters including V_{th}, G_m, S.S. were extracted at V_{ds}=0.05 and 1V, while V_b changed from -20V to 20V. The V_{th} is defined as the gate voltage at which the drain current reaches 10 nA*W_f/L_g, where L_g is the drawn gate length and W_f is the drawn Si fin width. In order to study the relationship between fin width (W_f) and V_b, the gate length was fixed at L_g=130 nm and W_f was changed from 500nm to 40 nm.

The impact of V_b on the HCI of the proposed n-TGFET with different V_b at 25°C was evaluated at the worst bias condition (V_g=V_{ds}) which has been confirmed in the previous chapter. The schematic connections for HCI measurements for TGFETs were shown in Fig.5-1. To clarify the electrical field variations induced by V_b and the shielding effect due to different D_{EXT}, the 3-diemntional (3D) electric field distribution in Si fin was simulated for n-TGFET with various W_f/T_{Si} ratios and D_{EXT} by the ISE TCAD program [5-15]. The schematic cross-sectional structure and the TEM micrograph of the TGFETs with L_g=130nm, W_f=40nm, and T_{Si}=40nm is shown in Fig. 5-2 (a) and (b), respectively. The excess-gate (D_{EXT}) is indicated clearly. The front gate oxide and buried oxide thickness is 4nm and 150nm, respectively. It should be noted that the D_{EXT} in our devices is around 8nm.

5-3 Results and Discussions

5-3-1 Effects of Back-Gate (V_b) Bias on Large Size n-TGFETs

The basic I-V characteristics of n-TGFETs with different V_b are studied. To avoid the dimension issue; therefore, the transfer characteristics of a large n-TGFETs with L_g=10μm, W_f=10μm, and T_{Si}=40nm biased at V_{ds}=0.05V and different V_b (from-20V increases to 20V) are shown in Fig.5-3. The extracted parameters including S.S., V_{th}, and G_m are shown in Fig.5-4 (a), (b), and (c), respectively.

From Fig. 5-4 (a), the smallest S.S. of the device with L_g=W_f=10μm is about 66 mV/decade at about V_b=-7V where the back-channel is at depletion mode [5-17]. As the V_b shifts to negative direction, the S.S. increases steeply first, and than stay at around 85 mV/Dec. On the other hand, as the V_b shifts to positive direction, the S.S. raises thoroughly. The variations of S.S. of devices with different V_b could be

attributed to the change of bottom interface-state. It can be seen that as V_b becomes more positive, for example at V_b=20V, the bottom interface should be at inversion mode; then, a lot of inverted charges would be induced by V_b and be out of control by V_g. Current flow through the bottom channel so that the V_g can not turn off the device effectively and S.S. increases. In the Fig. 5-3, we can find the abnormal large leakage current flow at off-state.

On the other hand, as the V_b shifted toward negative direction, the bottom interface is transmitted from depletion mode to accumulation mode and cannot easily turn off by V_g again. Therefore, S.S. value is also increased. From Fig.5-4(a), we find that the V_b transition point is at about -13V. As V_b becomes more negative than -13V, because the surface channel is independent of V_b, the S.S. maintains at about 85 mV/Dec.

As the bottom interface is at depletion mode, it is known that the subthreshold characteristic is greatly influenced by the back-gate bias according to T. Earst's report [reference]:

$$S.S._{front} = 2.3\frac{kT}{q}\left(1+\frac{C_{ox,buried}}{C_{Si}+C_{ox,buried}}\frac{C_{Si}}{C_{ox,front}}\right)$$
$$= 2.3\frac{kT}{q}(1+\frac{t_{ox,front}}{t_{ox,buried}}) \sim 61.3 \qquad \text{----------------------(5-1)}$$

The discrepancy between the ideal and measured S.S. could be attributed to the bottom interface trap-states and oxide-traps. Similar to the mechanism of S.S. variations, as V_b becomes more negative, V_{th} increases until the bottom interface enters accumulation mode. After this point, V_{th} becomes independent of V_b, and making V_b more negative will not change V_{th} any more. It should be noted that because the occurrence of the inverted bottom channel makes the V_{th} decreases continuously, we can not exactly confirm the classical front and back gate coupling

relationship [5-1].

Similar S.S. effect, for the G_m degradation shown in Fig.5-4(c), where the V_b induces an inverted or accumulated back-channel: as the vertical electric field increases significantly as the bottom channel changes from depletion mode to accumulation mode or inversion mode, the V_g can't control the bottom interface-state, the G_m is reduced by a factor of two (from 13 μS to 6.3 μS) [5-16].

5-3-2 Effects of Back-Gate (V_b) Bias on Narrow Width n-TGFETs

After reviewed the effect of V_b on the characteristics of large size n-TGFETs, we now discuss the effects of V_b on the ultra narrow width n-TGFETs. Not only the transfer characteristics but the variations of device parameters including S.S., V_{th} , and G_m of n-TGFETs with a fixed L_g (130nm) and different W_f are extracted at V_{ds}=0.05V and various V_b from 20V to -20V, as shown in Fig. 5-5 and Fig.5-6(a)-(c). For comparison, the transfer characteristics of a bottom channel device with L_g=130nm, W_f=60nm, T_{Si}=40nm, and buried oxide thickness=150nm is shown in Fig.5-7. For the bottom channel device, by using the quasilinear function ($I_d/G_m^{1/2}$) proposed by Ghibaudo [5-18], the bottom channel threshold voltage (V_{thb}) given by the intercept with the horizontal axis is about -3.4V.

The parameters variation of S.S. of the narrow channel width n-TGFETs is very similar to those of large dimension ones. At V_b positive condition, owing to the inversion mode at bottom interface, the S.S. becomes large apparently. Especially for wide devices, such as the device with W_f=500nm, the S.S. will be larger than 500mV/Dec with V_b larger 3V. Therefore, to focus on the S.S. change at depletion and accumulation mode, we didn't show the devices with S.S. larger than 500 mV/Dec in Fig.5-6(a). It should be noted that for the V_{th} variations, piecewise slope is observed in

Fig.5-6(b). To state it clear, the V_{th} variation of n-TGFETs with W_f=80nm was selectively showed in the inset figure of Fig.5-6(b) separately. In the inset figure, the transient behavior was obviously displayed. By Lim and Fossum's model, this transient behavior could be attributed to the change of bottom interface from inversion to accumulation state and made a small V_{th} discontinuity [5-1]. The discontinuity ($\sim 2\Phi_F$), observed in inset of Fig.5-6(b), is about 1.3V, larger than the theoretical values (0.64V), and could be attributed to the interface trap-states, oxide-traps and the variation of oxide thickness.

On the other hand, according to the classical front and back gate coupling model [5-10], the relationship between the V_{th} and V_b could be applied to the wide n-TGFET devices:

$$\Delta V_{th} \cong -\frac{t_{ox,front}}{t_{ox,buried}} \Delta V_b = -A \Delta V_b \quad \text{------(5-2)}$$

We can set the ratio between $t_{ox,front}$ and $t_{ox,buried}$ as a value "A" and show this value of n-TGFETs with W_f=80nm in the inset figure of Fig.5-6(b). However, in Fig.5-6(b), this slope "A" is not the same value for wide and narrow channel n-TGFETs. To illustrate this phenomenon more clearly, the slope "A" is plotted versus W_f in Fig.5-9. As the W_f decreases from 1000nm to 100nm, the "A" value almost decreases linearly with the reduction of bottom interface area. But, as W_f under 100nm, the "A" value decreases steeper than that of W_f wider than 100nm.

Moreover, from Fig.5-6(c), the G_m variations of n-TGFETs with different W_f were also showed. Two G_m peaks (peak "C" and "B") were clearly appeared at V_b=0 and -8V, respectively. For the n-TGFETs with W_f=1000nm, the G_m value at "C" is almost doubles time higher than that at "B". According to T. Ernst's report, this

ratio is attributed to the double-gate operation from front-gate and back-gate [5-17]. To clear, as shown in Fig. 5-7, at V_b around 0V, the G_m peak of the back-channel devices happened, and then the G_m peak "C" is the sum of front-channel and back-channel operation. And then, at point "B", where the back-channel devices is almost turned-off, the G_m peak "C" is only resulted from front-channel operation. It is interesting that the devices with narrower width decreases from 1000nm to 60nm, the G_m value ratio at point "C" over "B" decreases from 2 to 1.4, as shown in Fig. 5-7. It is also described that the decrease of width could suppress the influence from back-gate device.

As the W_f becomes smaller than 100nm, for the V_{th} vs. V_b plot, the sharp reduction of "A" is observed. Moreover, for the G_m of the devices with smaller W_f, the V_b effect is relaxed obviously.

These observations for different parameters cannot be explained by the reduction of the bottom area between Si/BOX alone. The effectively shielding effect by the D_{EXT} also plays an important role. To understand the role of the D_{EXT}, the electric field distributions of TGFETs biased with different W_f and D_{EXT} combinations are simulated by the ISETCAD too and are shown in Fig.5-9(a)-(d). The devices is biased at V_g=3V and V_b=-20V. It is clear from Fig.5-9(a) to (c) that the electric field due to the back-gate bias is screened by the electric field by the D_{EXT} bottom corner, especially for the deep D_{EXT} (16nm) devices. On the other hand, as the W_f is widened to 200nm, the D_{EXT} shielding efficiency is reduced, as shown in Fig.5-9 (d). To conclude, the narrow TGFETs with deep D_{EXT} and narrow W_f can relax the variations of the V_b effect effectively.

5-3-3 Effect of V_b on HCI of n-TGFETs

Besides the effect on DC characteristics, V_b also plays an important role of the reliability of n-TGFET devices. D. C. Mayer et al. have reported that the parameters of front-gate FD-SOI devices could be associated with fixed charge accumulation and fast interface trap-state generation at bottom interface between Si/BOX [5-3], [5-19], [5-20]. It is also illustrated that additional bottom interface trap-states and fixed-oxide-traps could be generated by radiation or high-voltage stress [5-21]. Therefore, finding a method to screen the influence of these traps is important.

In this sub-section, first of all, to demonstrate the effects of buried oxide charges and bottom interface states on the front channel operation, n-TGFETs were stressed with or without V_b bias under HCI conditions of $V_{ds}=V_g=3.2V$. The HCI conditions of $V_{ds}=V_g=3.2V$ has been confirmed as the worst HCI case in chapter 4. Fig.5-11 (a) and (b) show the ΔG_m and ΔV_{th} over the fresh parameters of devices after stressing at $V_{ds}=V_g=3.2V$ and $V_b=0$ or V_b floating. A noticeable difference is observed on the ΔG_m between $V_b=0$ and V_b floating stress conditions. As stressed at V_b floating condition, the G_m decreases fast as the stress time increased. On the contrary, as stressed at $V_b=0$, the G_m increases at initial stage and then turns over after a period of stress time. From the plot of ΔV_{th} versus stress time, for the devices stressed at $V_b=0V$, the slope of the power-law curves (n) is about 0.66, which corresponds to both the electron and hole carriers injection. On the contrary, for the devices stressed at V_b floating, the n value is 0.33. Since this value is close to 0.25, either electron or holes injection dominates the devices degradation [5-12]-[5-13].

Next, to clarify the effect of V_b on the degradation mechanism of HCI distinctly, stresses under alternating injection modes were performed. Fig.5-12(a) and (b) show the experiment procedure and stress conditions for n-TGFETs with a fixed

dimension (L_g=130nm, W_f=100nm, and T_{Si}=40nm), respectively. After the transfer characteristics of a fresh device being measured at forward and reverse mode (source/drain swapped), a positive V_b stress was performed at V_{ds}=V_g=3.2V and V_b=5V for 100second and the transfer characteristics (forward/reverse mode) were measured again. This is named as "P1" node. After P1 node, a negative V_b stress at V_{ds}=V_g=3.2V and V_b=-10V for 100second was performed and then the transfer characteristics (forward/reverse mode) were measured again to finish one cycle. This is named as "N1" node. After 5 cycles, the device parameters including V_{th} shift, G_m and I_{on} degradation were all extracted and shown in Fig.5-13(a), (b) and (c), respectively.

The positive V_{th} shift after the device being stressed at positive V_b conditions indicates that the impact ionization generated hot-electron injection into the front gate oxide, hot-holes injection into the BOX, and electron trapping at bottom-interface are the three most possible degradation reasons.

After a negative V_b stress cycle; nevertheless, the V_{th} will be all recovered to the original values. This result implies that after a negative stress, the holes injected into the BOX and electrons trapped at the bottom interface during the former positive V_b stress are neutralized by the carrier-injection with oppositive charges. It is interesting that during the interchange of positive and negative V_b stress, the V_{th} shift would almost disappear, and the G_m and I_{on} degradation could be almost recovered at reverse mode. This phenomena means the degradation induced by positive or negative V_b stress could be suppressed by the oppositive type carrier injection [5-13] Even the V_{th}, G_m, I_{on} degradation can be relaxed after interchange of negative and positive V_b stress, these parameters still degrade due to the continuous generation of interface state after a long time stress. The faster G_m and I_{on} degradation of the devices after

swapping the S/D electrode also proves that the generated interface trap-states during the hot-carrier stress is near the drain side. More importantly, the strong influence from the poor buried oxide and bottom interface quality of the devices on the SIMOX substrate on the HCI by the different sign of V_b is confirmed here again.

To clarify the effect of back-gate bias more carefully, a V_b from -30V to 5V was applied during the HC stress condition (V_{ds}=V_g=3.2V) for n-TGFETs (L_g=130nm, W_f=80nm). Fig.5-14(a) and (b) show the G_m degradation and V_{th} shift results, respectively. From the G_m degradation results, the devices degrade fast after stressing with the absolute V_b smaller than 5V. As the V_b shifts to more negative, both the G_m degradation and V_{th} shift present a turnover phenomenon. Hot-holes injection into the buried oxide could explain this observation clearly. Fig.5-15 illustrates the effect of V_b schematically. During the HC stress with higher negative V_b, hot-holes have higher energy to penetrate into the buried oxide. During measurement, the hot-holes in the buried oxide would act as a virtual gate and could enhance G_m and reduce V_{th}, as shown in Fig.5-15. However, as the stress time is extended, these hot-holes would graduate generate acceptor-like interface trap states at the buried oxide/Si interface and front gate/Si channel interface. And the coulombian scattering induced by acceptor-like interface trap-states would efficiently degrade the G_m seriously and shift the V_{th} positively again. We also show the forward/reverse mode transfer characteristics of the bottom-channel devices (L_g=130nm and W_f=100nm) before and after HC stress for 3000second at V_{ds}=V_g=3.2V and V_b=-20V in Fig.5-16(a) and (b), respectively. At forward mode, the G_m reduction (10%), I_{on} reduction (19%), I_{off} increase, and S.S. increase at forward mode could be attributed to the generation of interface trap-states. At reverse mode, all of the parameters are also degraded, for example, G_m decreases 7% and I_{on} decreases 20%. This similar degradation degree of

device parameters at forward/reverse mode measurement also pointed out that the interface-states were not only generated near the drain-side, but along the channel.

5-3-4 Combination of the Impact of V_b and W_f on HCI of n-TGFETs

In previous sub-sections, both the narrow-width (W_f) effect and V_b effect on the HCI of n-TGFETs have been demonstrated. In this sub-section, we investigate the combination of both effects on nTGFETs. It is demonstrated that the narrow-width TGFETs with ultra-small bottom gate area and deep D_{EXT} side-gate structure could have superior resistance to the V_b.

The results of G_m degradation of n-TGFETs with a fixed L_g (130nm) and different W_f (40, 60, 100, 200 nm) stressed at V_{ds}=V_g=-32 V and V_b=-20V are shown in Fig.5-17(a). It has been proved that the turn-over curves of G_m and V_{th} degradation for n-TGFETs is attributed to the virtual gate generated by positive buried oxide charges during HC stress with negative back-gate bias. It is clear that the device with W_f equal to 200nm has the highest percentage of positive G_m shift (26%). For the ones with W_f=40 nm, because of the reduction of the bottom interface area between Si/BOX, the maximum positive G_m shift is only 15%. The maximum positive G_m degradation is plotted as a function of W_f also in Fig.5-17(b) at two different Vb. It is clear that the narrower the Wf is, the lower the positive Gm degradation is. The extended side-gate may be the possible reason. The electrical field distribution simulated by the ISE TCAD shown in Fig.5-10 could be used to explain this result again. For device with 40 nm W_f, the influence of electrical field induced by V_b is much smaller than that of 200 nm device. In the narrower devices, not only the reduction of the bottom area ratio to the front-gate oxide interface but also the strong shielding effect attributed to the D_{EXT} terminate the penetration of field lines from the

back gate effectively. Therefore, the maximum positive G_m degradation due to the high negative V_b during hot-carrier stress is improved with the reduce of W_f apparently.

5-4 Conclusions

The effects of V_b on the basic I-V characteristics, HCE of n-TGFETs were investigated distinctly.

First, for the basic I-V characteristics, the V_b bias would affect the state of bottom interface between the Si-channel and buried oxide, and then modify the performance of the front channel of TGFETs. Especially as the back interface is at depletion mode, the front channel directly contacts to the bottom interface, the front gate would have superior controllability than that as the back interface is at accumulation or inversion mode.

Next, for devices after HCI stress, back-gate would accelerate the hot carriers into the buried oxide and generate interface state and fixed charges in the buried oxide, and then complex the parameters degradation such as G_m and V_{th}. The D_{EXT} length and channel width show strong influence on the V_b effect. Deepening the D_{EXT} would effectively screen the electric field induced by back-gate bias. For narrow TGFETs, not only the bottom interface area could be reduced but the distance between the side gates would be also shirked; therefore, D_{EXT} had stronger screening effect than the wider ones.

To summarize, the mechanisms of V_b effect on basic IV and reliability of TGFETs have been demonstrated in detail. The V_b effect can be avoid effectively by the TGFETs with narrow-width and deep D_{EXT} structure.

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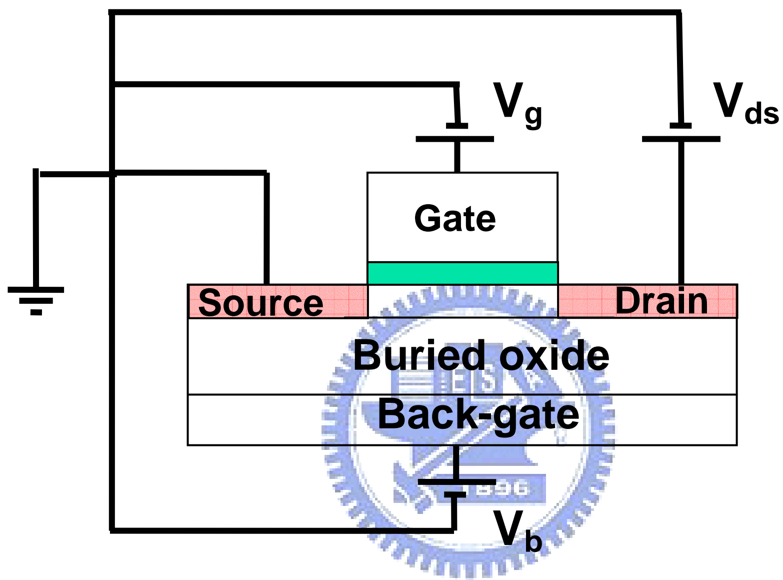


Fig.5-1 Schematic views of HCI measurement for TGFETs with a fixed V_{ds}, V_g, and various $V_{b.}$

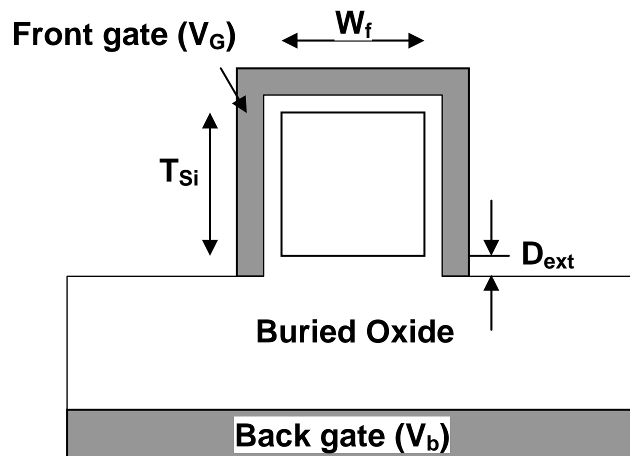


Fig.5-2(a) Schematic cross-sectional view of TGFETs stressed with front-gate (V_g) and back-gate bias (V_b).

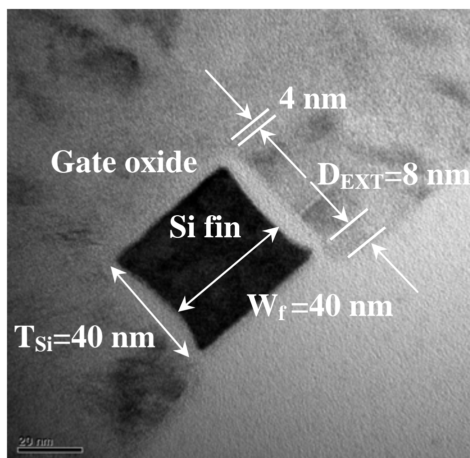


Fig.5-2(b) TEM cross-sectional view of TGFETs with L_g=130nm, W_f=40nm, and T_{Si}=40nm. The front gate oxide and buried oxide thickness is 4nm and 150nm, respectively. The excess gate length (D_{EXT}) is 8nm.

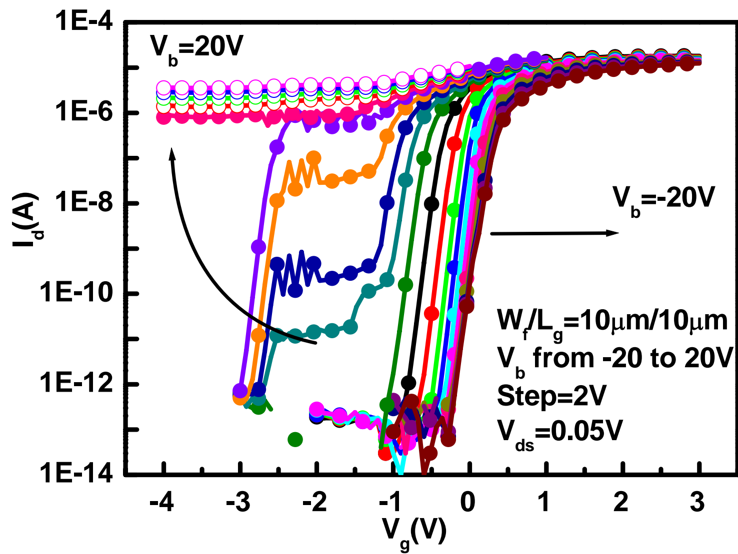
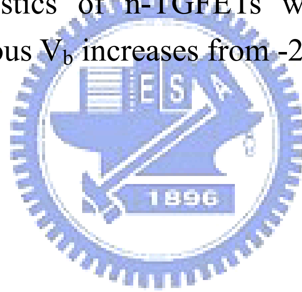


Fig.5-3 Transfer characteristics of n-TGFETs with L_g=10μm, W_f=10μm, and T_{Si}=40nm and various V_b increases from -20V to 20V (step=2V).



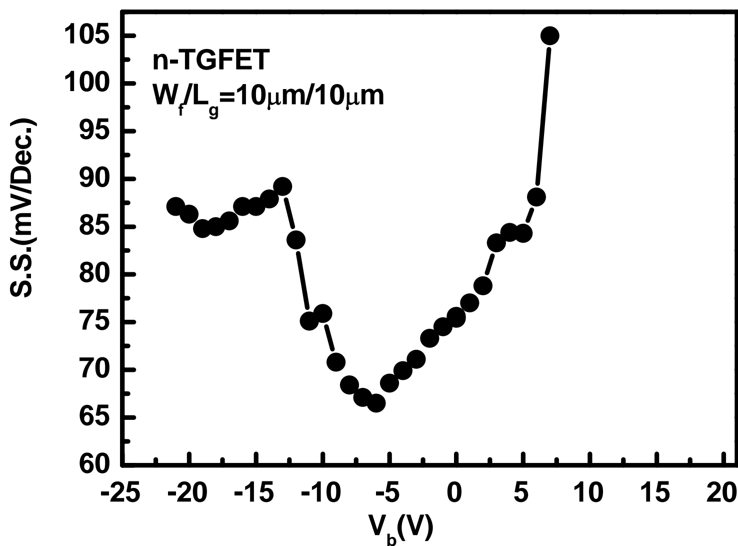


Fig.5-4(a) S.S. variations of n-TGFETs with L_g=10mm, W_f=10mm, and T_{Si}=40nm different V_b (from -21 to 21 V, step=1V).

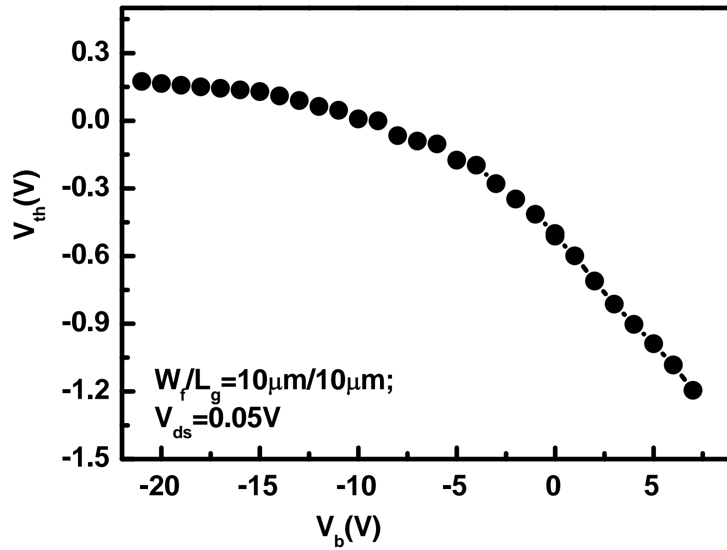


Fig.5-4(b) V_{th} variations of n-TGFETs with L_g=10mm, W_f=10mm, and T_{Si}=40nm different V_b (from -21 to 21 V, step=1V).

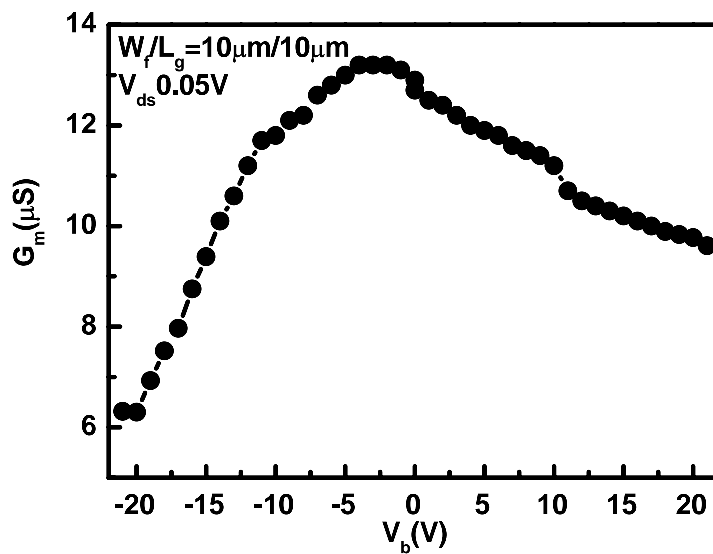


Fig.5-4(c) G_m variations of n-TGFETs with L_g=10mm, W_f=10mm, and T_{Si}=40nm different V_b (from -21 to 21 V, step=1V).

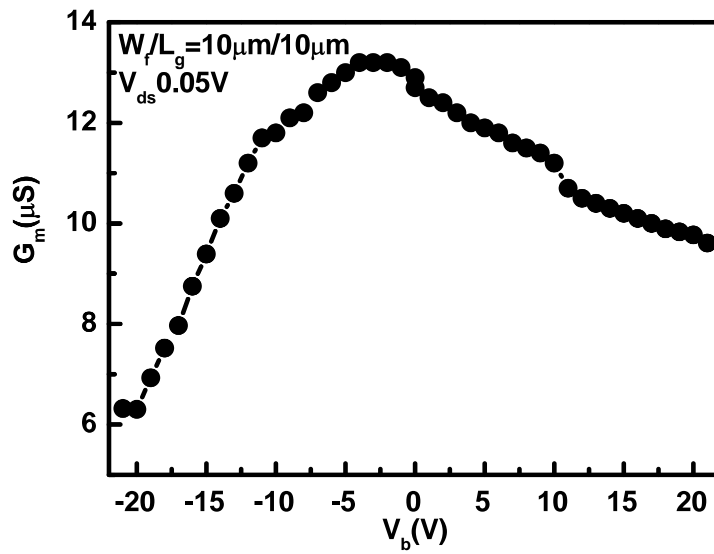
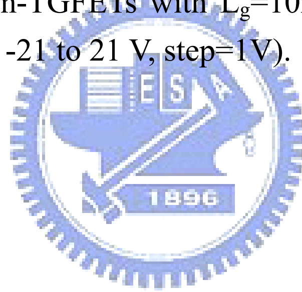


Fig.5-4(c) G_m variations of n-TGFETs with L_g=10mm, W_f=10mm, and T_{Si}=40nm different V_b (from -21 to 21 V, step=1V).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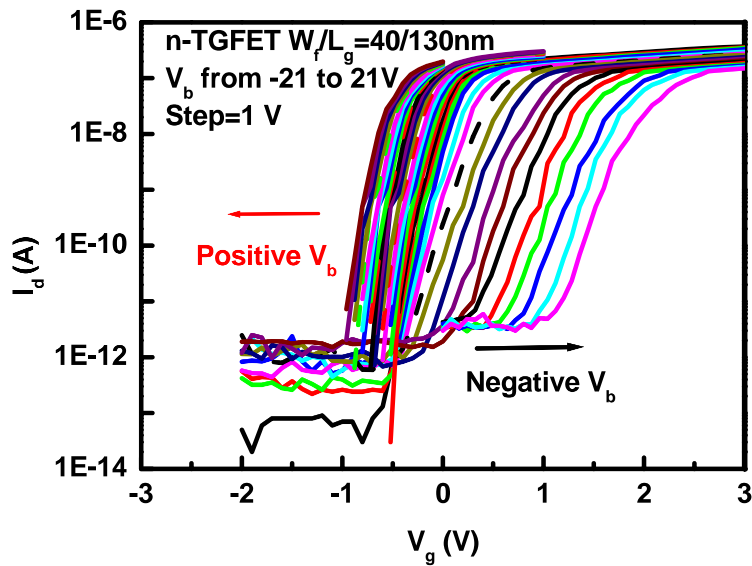
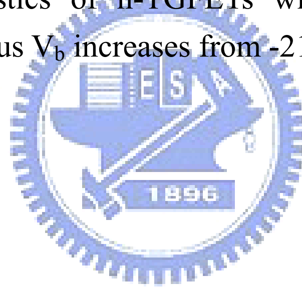


Fig.5-5 Transfer characteristics of n-TGFETs with L_g=130nm, W_f=40nm, and T_{Si}=40nm and various V_b increases from -21V to 21V (step=1V).



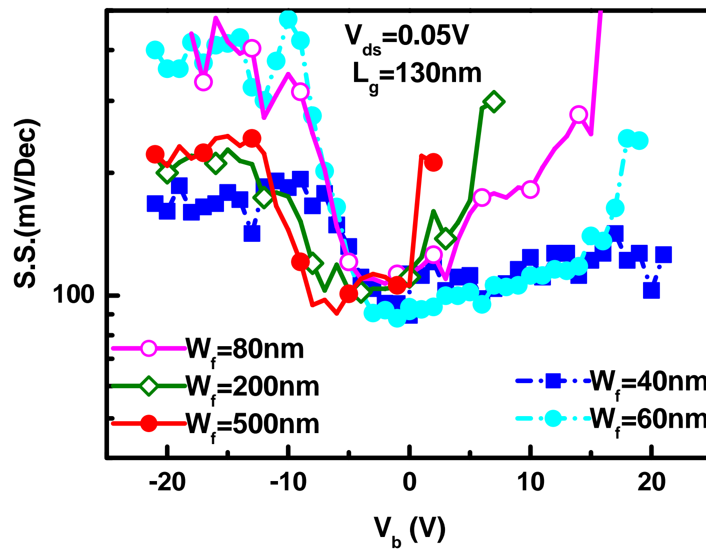


Fig.5-6(a) S.S. variations of n-TGFETs with L_g=130nm, T_{Si}=40nm, various W_f(60, 80,200,500, and1000 nm) and different V_b (from -21 to 21 V, step=1V).

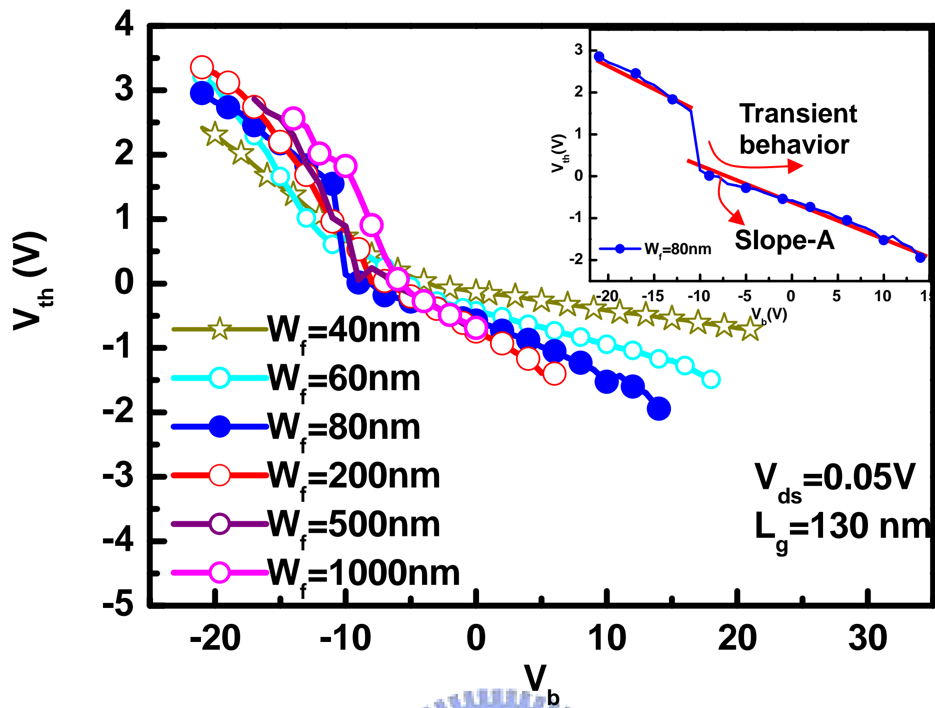


Fig.5-6(b) V_{th} variations of n-TGFETs with L_g=130nm, T_{Si}=40nm, various W_f (60, 80, 200, 500, and 1000 nm) and different V_b(from -21 to 21 V, step=1V). The inset figure shows the V_{th} variations of devices with W_f=80nm and slope "A" separately.

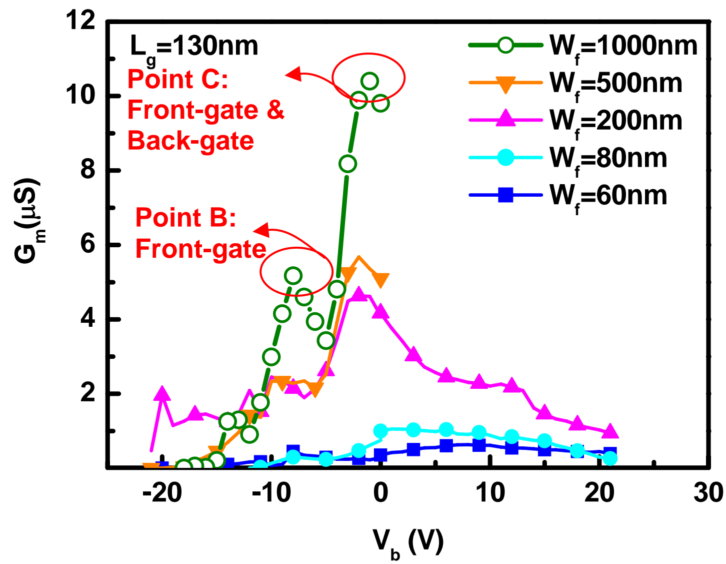
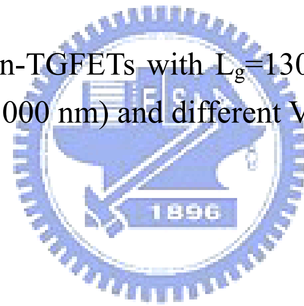


Fig.5-6(c) G_m variations of n-TGFETs with L_g=130nm, T_{Si}=40nm, various W_f (60, 80,200,500, and 1000 nm) and different V_b(from -21 to 21 V, step=1V).



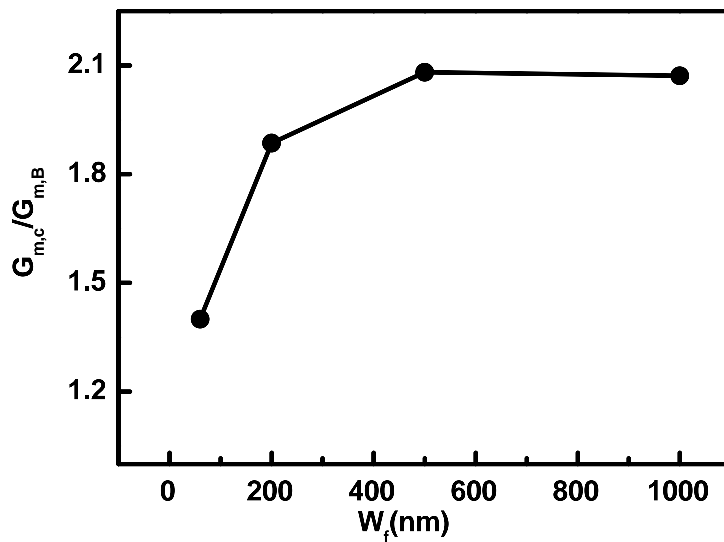


Fig.5-7 G_m peak ratio between point "C" and "B" in Fig.5-6(c).

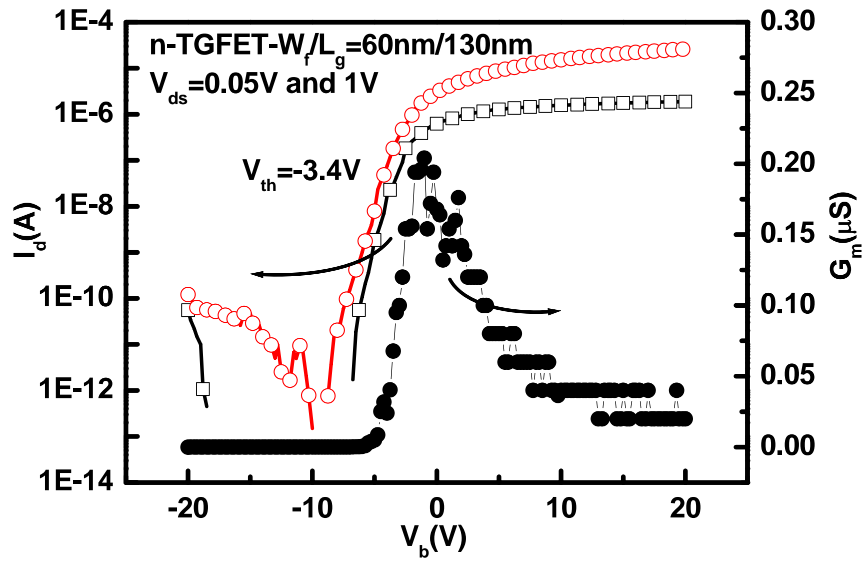


Fig.5-8 Transfer characteristics of back channel n-TGFETs devices with L_g=130nm, W_f=60nm, T_{Si}=40nm and buried oxide thickness=150nm.

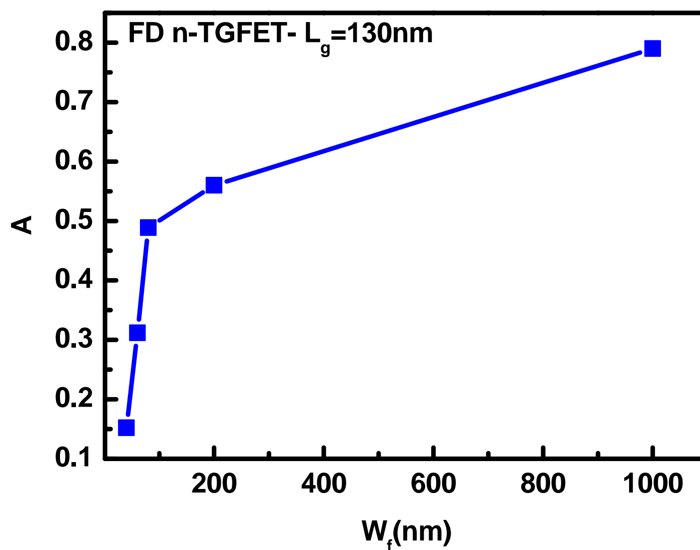


Fig.5-9 Transfer characteristics of back channel n-TGFETs devices with L_g=130nm, W_f=60nm, T_{Si}=40nm and buried oxide thickness=150nm.

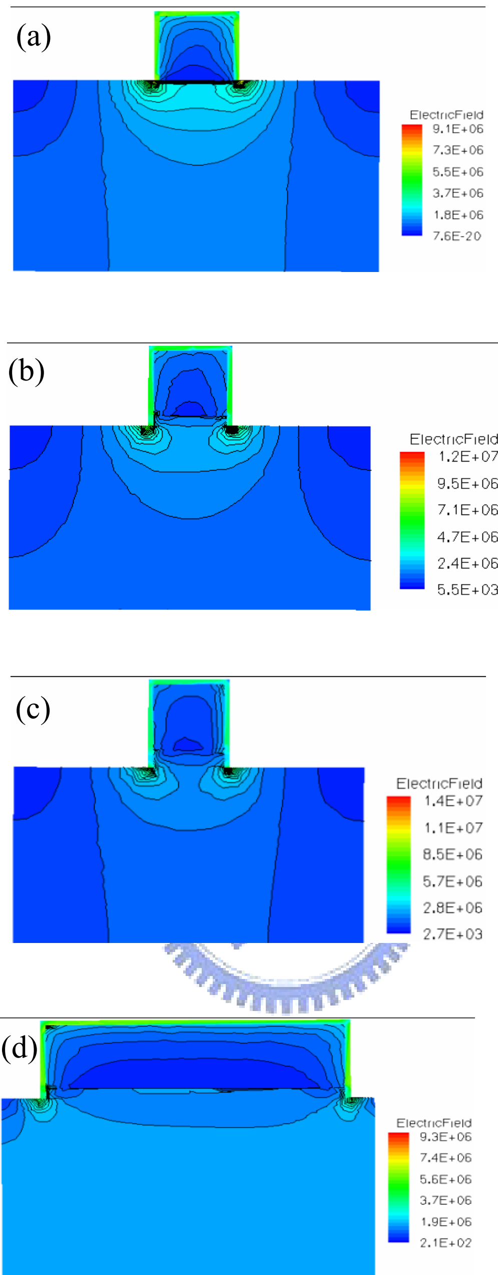


Fig.5-10 The cross-sectional electric field simulation with V_{ds}=V_g=3.2V, and V_b=-10V for devices with a fixed L_g (130nm) and T_{Si} (40nm) and various W_f and D_{EXT} (a) W_f=40nm, D_{EXT}=0nm, (b) W_f=40nm, D_{EXT}=8nm, (c) W_f=40nm, D_{EXT}=16nm, and (d) W_f=200nm, D_{EXT}=16nm.

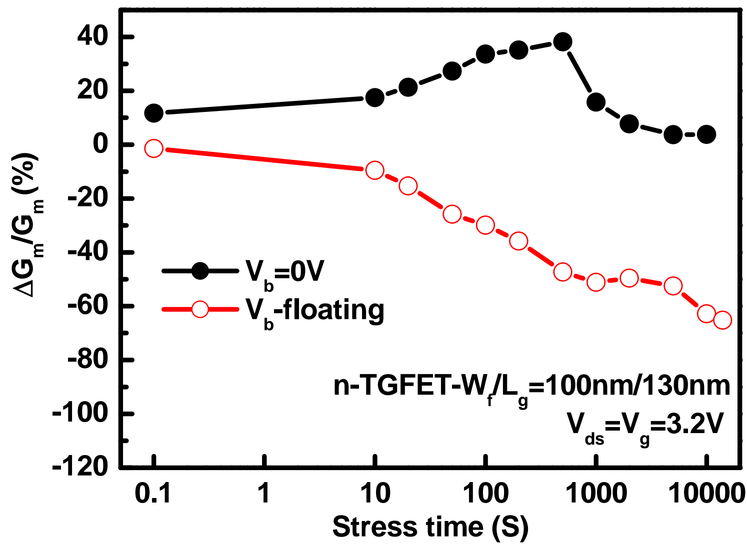
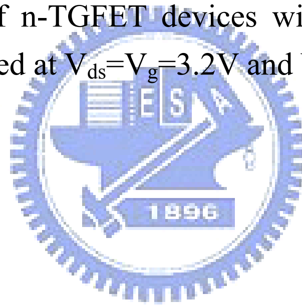


Fig.5-11(a) G_m variations of n-TGFET devices with L_g=130nm, W_f=100nm, and T_{Si}=40nm stressed at V_{ds}=V_g=3.2V and V_b=0 or floating.



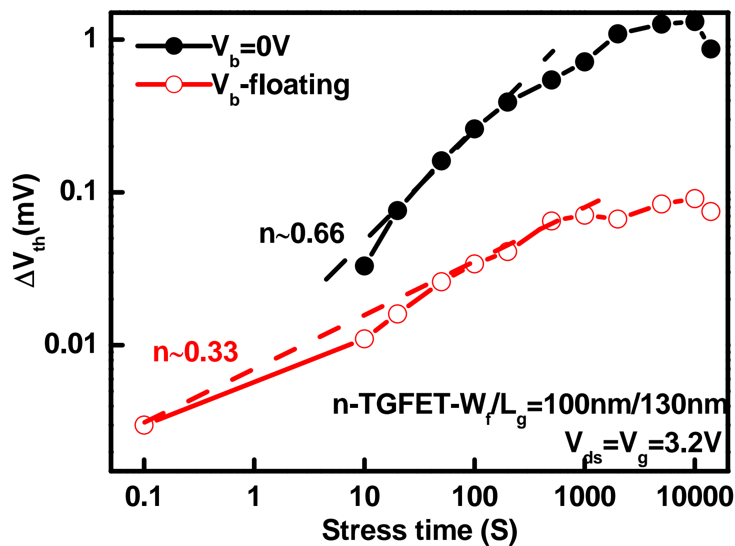


Fig.5-11(b) V_{th} variations of n-TGFET devices with L_g=130nm, W_f=100nm, and T_{Si}=40nm stressed at V_{ds}=V_g=3.2V and V_b=0 or floating.

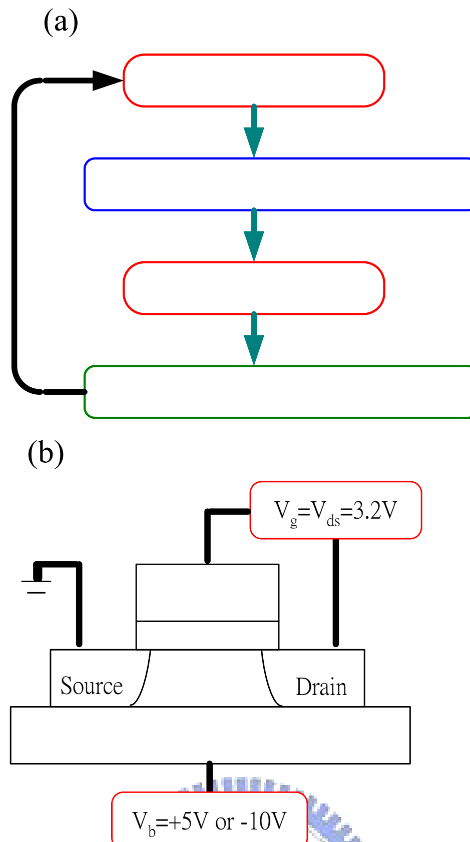


Fig.5-12 Schematic photos of (a) process cycle for HCI measurement and (b) HCI stress conditions of devices.

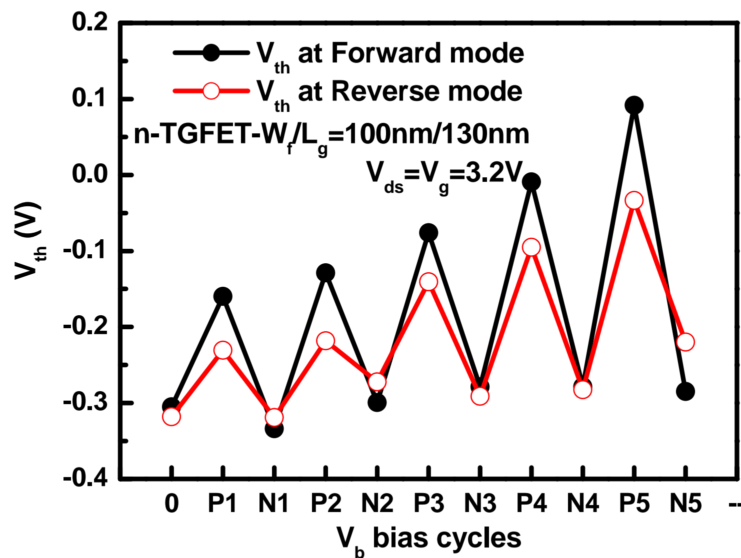


Fig.5-13(a) V_{th} variations of n-TGFET with L_g=130nm, W_f=100nm, and T_{Si}=40nm after stressed at V_{ds}=V_g=3.2V and V_b=-10 V (N) or 5V (P).

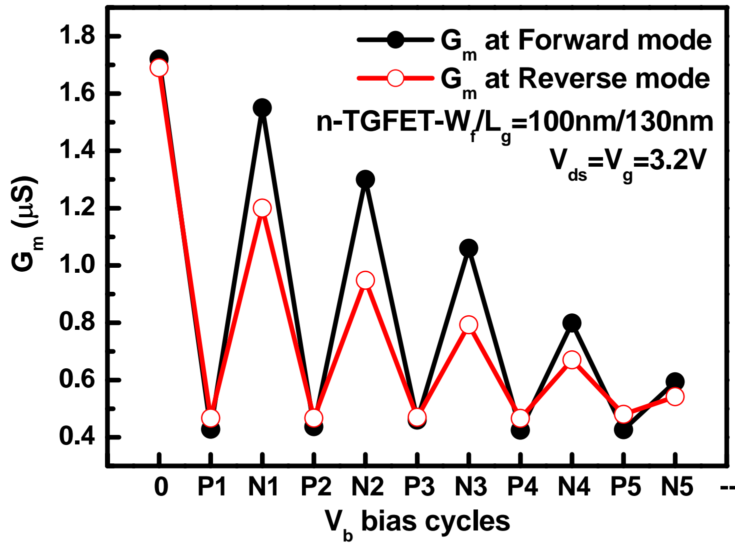
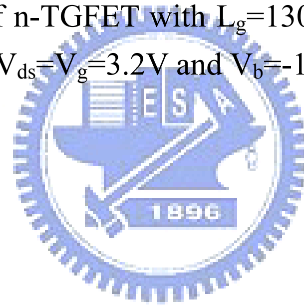


Fig.5-13(b) G_m variations of n-TGFET with L_g=130nm, W_f=100nm, and T_{Si}=40nm after stressed at V_{ds}=V_g=3.2V and V_b=-10 V (N) or 5V (P).



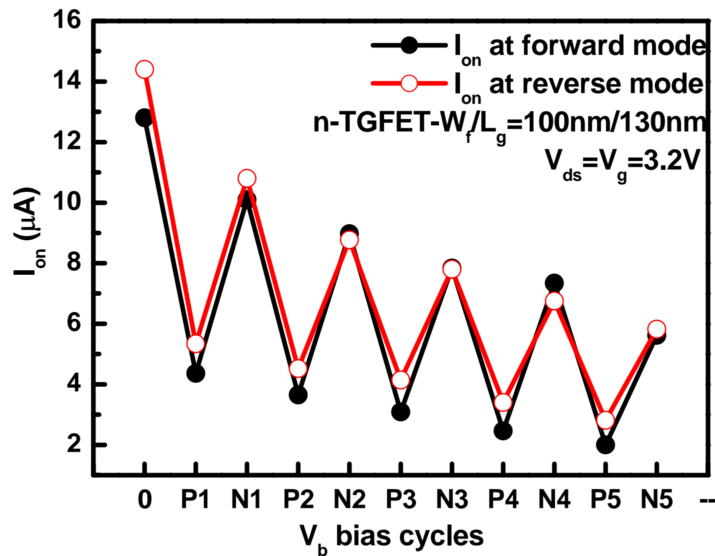


Fig.5-13(c) I_{on} variations of n-TGFET with L_g=130nm, W_f=100nm, and T_{Si}=40nm after stressed at V_{ds}=V_g=3.2V and V_b=-10 V (N) or 5V (P).

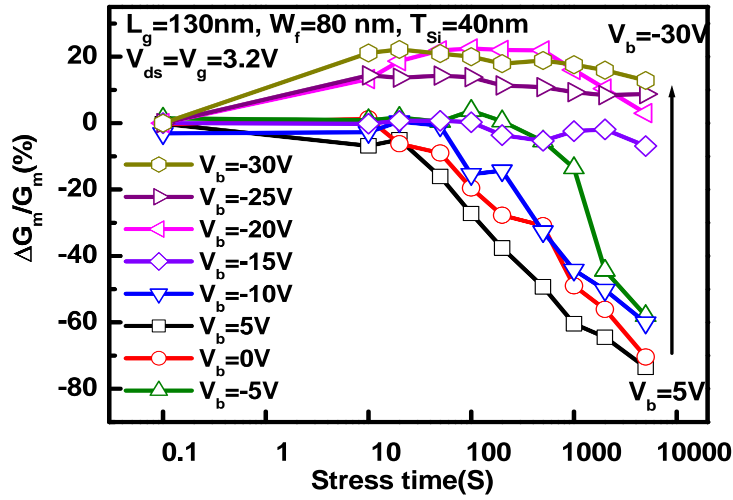


Fig.5-14(a) G_m degradation of n-TGFET devices with L_g=130nm, W_f=80nm, and T_{Si}=40nm after stressed at V_{ds}=V_g=3.2V and different V_b (from -30 to 5 V, step=5V).

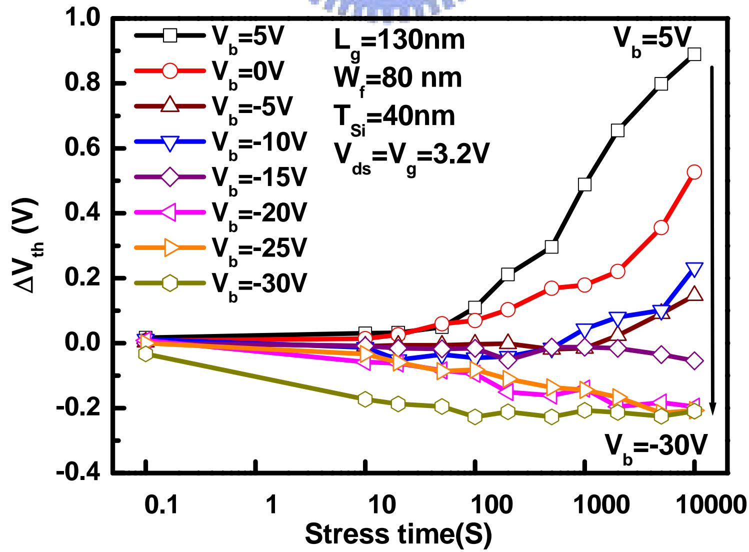


Fig.5-14(b) V_{th} degradation of n-TGFET devices with L_g=130nm, W_f=80nm, and T_{Si}=40nm after stressed at V_{ds}=V_g=3.2V and different V_b (from -30 to 5 V, step=5V).

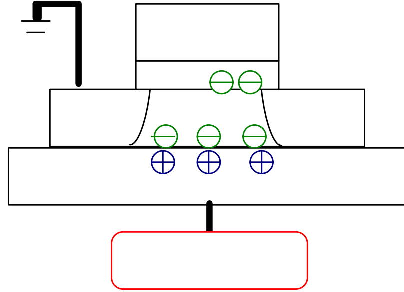


Fig.5-15 Schematic views of virtual back-gate effect after HCI stressed with negative back-gate bias.

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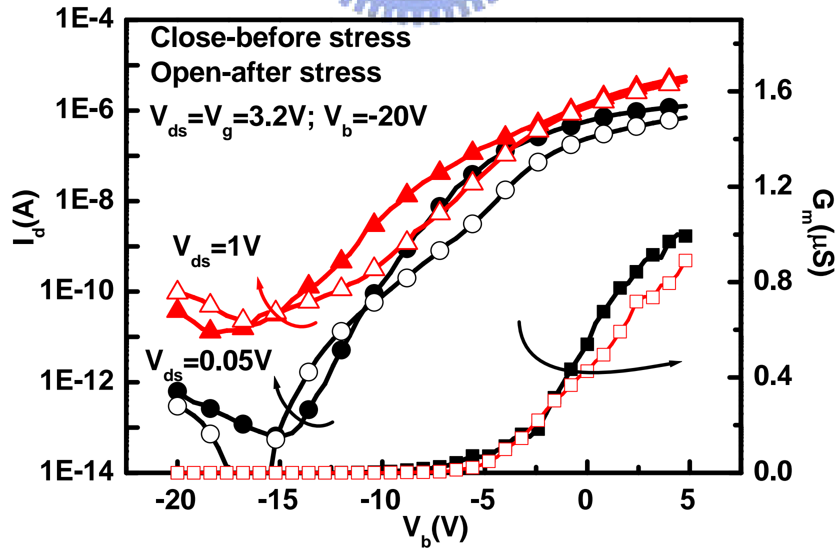


Fig.5-16(a) Forward mode transfer characteristics of back channel n-TGFETs devices (L_g=130nm, W_f=100nm, T_{Si}=40nm and BOX=150nm) before/after stressed with V_{ds}=V_g=3.2V, V_b=-20V for 3000second.

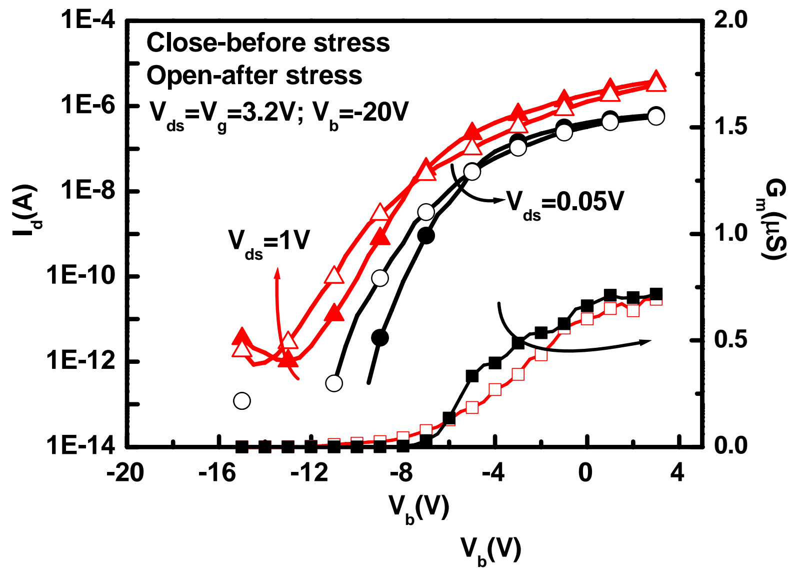


Fig.5-16(b) Reverse mode transfer characteristics of back channel n-TGFETs devices (L_g=130nm, W_f=100nm, T_{Si}=40nm and BOX=150nm) before/after stressed with V_{ds}=V_g=3.2V, V_b=-20V for 3000second.

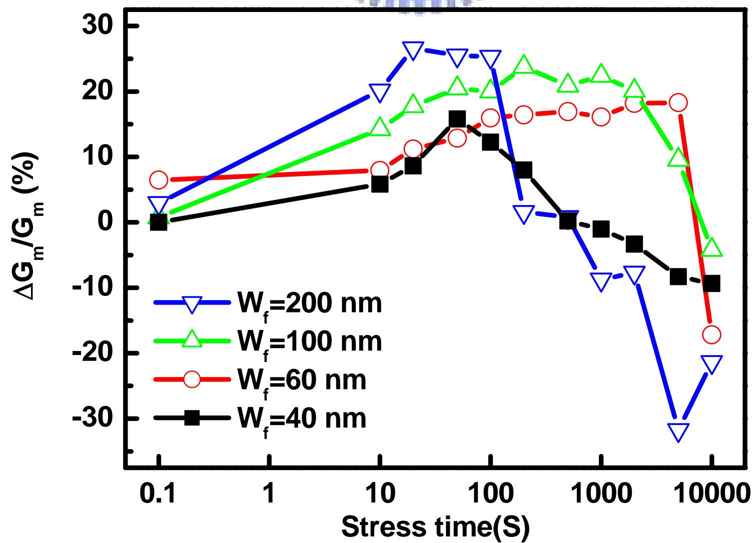


Fig.5-17(a) G_m variations vs. stress time of n-TGFETs with a fixed L_g=130nm and T_{Si}=40nm and various W_f (40, 60, 100, 200nm) stressed with V_{ds}=V_g=3.2V and V_b=-20V.

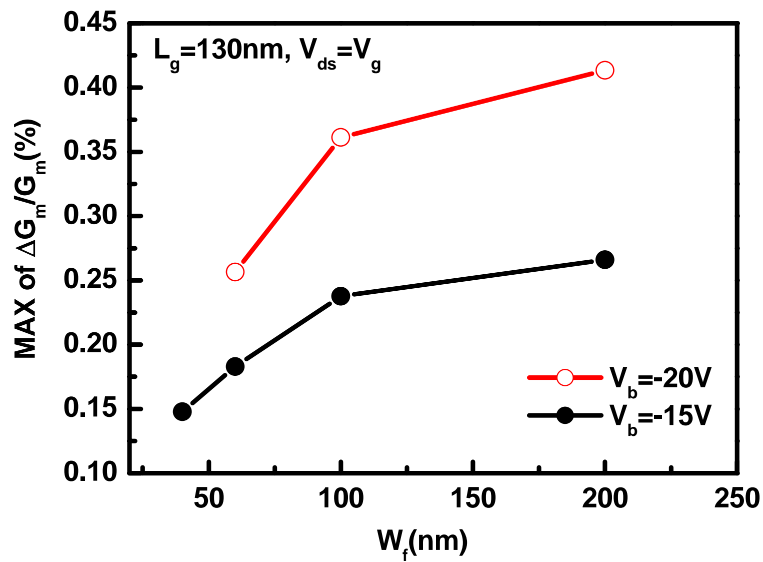
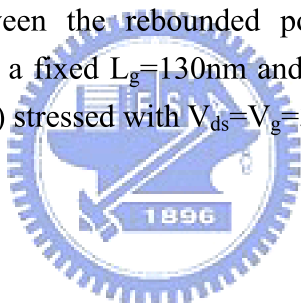


Fig.5-17(b) The ratio between the rebounded point and the initial values of n-TGFETs with a fixed L_g=130nm and T_{Si}=40nm and various W_f (40, 60, 100, 200nm) stressed with V_{ds}=V_g=3.2V and V_b=-20V.



Chapter 6

The Fabrication and Characteristics of FD-SOI Devices with FUSI-gate and MSB S/D Junction

6-1 Introduction

Up to now, multi-gate FETs (MGFETs) and fully-depleted silicon-on-insulator (FD-SOI) devices have been demonstrated to have better horizontal scalability than traditional bulk transistors [6-1]-[6-2]. As the device scaling scales down to nano-meter scale, several critical issues for the fully-depleted SOI (FD-SOI) devices must be solved. The First first difficulty issue is the parasitic resistance reduction. The silicide technique, the raised S/D process, and the ITS technique proposed in previous chapters were suggested asare possible solutions [6-2]-[6-3]. Second, similar to bulk CMOS, the short-channel effect (SCE) attributed to the disappointing gate controllability owing the poly-depletion effect is another critical issue for FD-SOI.

For conventional FD-SOI devices, to suppress the SCE while control the V_{th} well, asymmetric dual-type poly-Si gates or the heavily body doping process are generally used to correct the V_{th} [6-4]-[6-6]. For asymmetric dual-type poly-Si gates, some drawbacks such as high gate parasitic resistance, poly-Si gate depletion, and boron penetratation into channel still exist and can obstruct the device vertical scaling down [6-7]-[6-9]. Beyond 45nm node, to consider the process temperature of high-κ gate dielectric, the high temperature poly-Si activation step is another problem. On the other hand, for heavily doping doped body, the strong transverse field and dopant

fluctuation would degrade the device performance such as lower carrier mobility and V_{th} variation [6-2]. Therefore, to scale the device down while controlling the V_{th} well, metal-gate with proper work function (WF) and undoped-body structure is the future-trend for of the FD-SOI [6-10]-[6-11].

Several metal gate electrodes have been suggested for bulk CMOS devices. For example, dual metals intermixing or alloy techniques, such as Ti-Ni or Ru-Ta, were both suggested as simple techniques to alter the WF [6-12]-[6-13]. The instability of the alloy composition and complexity of process integration are questions.

Recently, fully silicided-poly-Si (FUSI) gate technique was suggestedhas been proposed to replace the conventional heavily doped poly-Si and as metal gate material on the bulk and FD-SOI devices [6-14]. From the characteristics perspective, FUSI gate, especially for Ni silicide, which has many advantages including the low temperature process, the low sheet resistance, the low stress of formation, and an intrinsically mid-gap WF [6-15], has already became become a promising gate electrode material in the nano-regime.

It should be noted that, for to applying on to bulk CMOS, an apparent drawback of Ni FUSI gate is that the WF can be tuned just over a narrow range by segregating the appropriate impurities into the silicide silicide/gate oxide interface (SIIS technique) after the S/D junction process formation [6-16]-[6-17]. For lightly doped or undoped- body FD-SOI; on the contrary, a little adjustment of Φ_m from mid-gap is enough to satisfy the V_{th} requirement [6-11].

Form the process integration perspective, there are some critical issues of for the Ni FUSI process such as the stability of NiSi phases, the stability of crystal orientation, the integration between FUSI gate , S/D process, and high-κ gate

dielectric layer [6-18]-[6-21].

In order to preserve the advantages of NiSi FUSI gate while simplify the process integration and stabilize the WF tuning, in this chapter, the FUSI gate and MSB S/D structure combined by with the Implantimplant-to-silicide (ITS) process on a FD-SOI device was will be demonstrated at for the first time.

The ITS process, in which the poly-Si is ahead transferred to Ni silicide and then followed by implantation and activation process, has is confirmed suggested asto be a thne effective method to adjust the WF while removing the NiSi phase and crystal orientation influences [6-16],[6-22].

To conclude, in this chapter, we showed the fabrication process and I-V characteristics for the first time that Ni FUSI gates in combination with modified-Schottky-barrier (MSB) S/D FD-SOI devices by implant-to-silicide (ITS) technique.

6-2 Detailed Process

In order to demonstrate the characteristics enhancement by FUSI-gate, two set of devices including the FUSI-ITS-MSB (type A) and polycide-MSB (type B) FD-SOI devices were fabricated at the same time. The process flows of type A and type B devices are schematically drawn in Fig.6-1 and 6-2, respectively. For bBoth the type A and B FD-SOI devices, the starting materials were boron-doped 6-in SOI wafers with a low doping concentration of around $1x10^{15}$ cm^{-3}. The nominal Si layer and buried oxide layer thicknesses were 50 nm and 150 nm, respectively. The Si layer was thinned down to 40 nm by a thermal oxidation process. The device islands (including S/D and Si channel region) were defined by electron-beam (e-beam) lithography and plasma etching. A 4 nm thick SiO_2 was thermally grown as the gate

dielectric, as shown in Fig.6-1(a) and Fig. 6-2(a). Following the 40 nm thick undoped poly-Si film deposition, e-beam lithography was employed again to define the gate pattern. It should be noted that the thicknesses of the deposited poly-Si were was 40 nm and 150 nm for type A and type B devices as shown in Fig.6-2(a) and 6-2(b), respectively. Then, for type B devices, an implantation to a dose of $5x10^{15}cm^{-2}$ and activation at 950°C for 20 s by a RTA system were applied to dope the poly-Si. Following the gate patterning process, a SiO_2 (10nm)/Si_3N_4 (30nm) composite spacer was formed, as shown in Fig.6-1(c) and 6-2(c). Next, a 25nm thick Ni film was deposited by a PVD system. The 2-step self-aligned Nickel silicide (Ni-Salicide) process was then performed and the resulting structure is shown in Fig.6-1(d) and 6-2(d). The purpose and condition of the 2-step silicidation process have been described in chapter 3. The sheet resistance (R_{sh}) of the silicide layer is about 6Ω/□ as measured by a four-point sheet resistance measurement stageinstrument. Next, tThe dopants were implanted into the silicide at S/D/G region (P_{31}^+ for n-type and BF_2^+ for p-type) at 10keV with doses of $1x10^{15}$ cm^{-2}. All devices were activated at 600°C for 30 min as shown in Fig.6-1(d) and Fig.6-2(d), respectively. The devices can be probed directly now.

For comparison, simple MOS capacitors with type A and B gate electrodes were was also fabricated and wereas shown in Fig.6-3(a) and (b), respectively. The flat-band voltage (V_{FB}) and the equivalent oxide thickness (EOT) were determined extracted by CVC model fitting to the from C-V curve measured C-V curves at 100 KHz and extracted by the CVC fitting model [6-23]. The effective WF (Φ_m) was then extrapolated from the V_{FB}-EOT plot.

6-3 Results and Discussions

6-3-1 Characteristics of the FUSI-ITS Capacitances

First of all, the C-V curves of the type A MOS capacitor with P_{31}^{+} doses of 0 and 1x10^{15} cm^{-2} and type B MOS capacitor are displayed in Fig.6-4. For type A capacitors, as the doses of P_{31}^{+} increases from 0 to 1x10^{15} cm^{-2}, the V_{FB} values shift toward the negative direction. Assuming that the V_{FB} shift as all the result of effective work function variation; , the extracted effective work function of the three capacitors are shown in Fig.6-5. The ITS process shifts the work function of type A capacitor from 4.54eV to 4.37eV, i.e. 0.17V toward the conduction band. This value is still higher than the work function of type B capacitor by 0.17 eV and is not suitable for bulk n-MOSFETs. However, it is enough for FD SOI n-MOSFETs.

Three major mechanisms including different crystal orientation due to different Ni/Si atomic ratio, impurity pile up, and residual poly-Si layer were have been proposed as to explain the work function modulation of FUSI gatedetermining factors [6-16]. To clarify the original physical mechanisms of the observed work function modulation of the type A capacitors in this work, SIMS, XRD, and TEM analyses were employed.

The SIMS depth profiles of the type A capacitors doped with Phosphorousphosphorous (P_{31}^{+}) or Boronboron (B_{11}^{+}) to a dose of 1x$10^{15}$$cm^{-2}$ were shown in the Fig.6-6(a) and (b), respectively. After annealing, the concentrations of Phosphorous phosphorous and Boron boron at the NiSi/SiO_2 interface increases obviously. To extract the silicide phase of the FUSI-gate, the XRD-data spectra of as-silicidationsilicided, as-implanted, and after-annealinged process samples are shown in Fig.6-7. After implantation, all Ni-silicide phases disappeared due to the amorphorization of silicide film induced by ion-implantation. However, the XRD

spectra of samples before implantation and after activation are almost identical to each other. It should be noted that no other phases such as $NiSi_3$ or $NiSi_2$ are observed. Therefore, in this work, the silicide phase isn't affected by the species. Finally, the cross-sectional TEM micrograph of the type A capacitor after activation is shown in Fig.6-8. It is clear that all of the poly-Si was fully transformed to Ni silicide. No residual poly-Si layer is found in this sample, .

Without the evidence of phase-change and poly-Si- residualresidues, it is concluded that the dopant piled-up at the interface between the silicide and gate oxide is the major mechanism for the work function modulation in this work.

6-3-2 Characteristics of FUSI-ITS FD-SOI Devices Characteristics

After the confirmation of work function tuning of FUSI-gate by ITS technique, in this sub-section, characteristics of the type A FD-SOI devices, FUSI-gate integrated with MSB-S/D junction, are demonstrated. Fig.6-9 shows the cross-sectional TEM micrograph of the type A FD-SOI devices. After careful selection of the poly-Si thickness and S/D Si thickness, the S/D and gate can be fully-silicided simultaneously. The transfer characteristics of both n- and p-channel type A FD-SOI devices are shown in the Fig.6-10. For comparison, the n-channel and p-channel type B FD-SOI devices are shown in Fig.6-11. The gate length (L_g) and gate width (W) are both 1μm, and the Si thickness is about 40nm. The measured and extracted device parameters are also summarized in Table 6-1 and 6-2. Because of the suppression of gate-depletion, the FUSI-gate devices can not only induce more inversion charges but also have better controllability than the polycide-gate devices. Taking n-channel device as an example, as listed in Table 6-1, while the gate material changed from n^+-polycide to FUSI-gate, the subthreshold swing (S.S.) at V_{ds}=0.05V

decreases from 79.4 to 78.1mV/Decade, the transconductance (G_m) at V_{ds}=1V increases from 114 to 145.2μS, and the drain-induced-barrier-lowering (DIBL) also reduces from 0.2 V/V to about 0.1V/V. Moreover, the driving current (I_{on}) at V_g-V_{th}=1V is also slightly increased from 5.5 x10^{-5} to 5.65x10^{-5} μA. It is important that for the n-channel devices, the ratio of driving current at V_g=1V to that at V_g=0V can be raised from 34 to 2.83x10^4 as the gate electrode changed from polycide to FUSI due to the V_{th} positive shift. The increment of ratio also proved that the FUSI gate electrode devices could be suitable applied on to the low-power requirement circuits.

Although the V_{th} difference is obviously for the A and B type devices. It should be noted that the V_{th} of the n-channel type A FD-SOI device is just 0.17 V and slightly negative than the estimation estimated V_{th} value of device with the same WF (4.35V) and the same channel doping concentration (1x10^{15}cm^{-3}). The similar trend also occurred on the p-channel A-type devices. In the p-channel type A device, the shift of V_{th} and S.S. degradation is more negative and serious than that of n-channel one, respectively. Because of the similar negative shift of V_{th} for n- and p-channel devices, the positive oxide trap charges may be the plausible most possible reason, but more evidence should be needed to demonstrate prove it.

To examine the effect of ITS technique on the S/D junctions, the transfer characteristics of pure FUSI gate SB SOI devices without any implantation or activation process are shown in Fig.6-12. The obvious ambipolar characteristic is attributed to the abnormal Schottky-barrier at S/D junction and has been described discussed in the chapter 3.

The typical output characteristics of type A FD-SOI devices are shown in Fig. 6-13. The driving current of n-and p-channel devices with L_g=W=1μm are is

about 171 and 64.4 μA/μm, respectively. Because of the ITS technique, the Schottky barrier height at S/D region are is also suppressed. Therefore, the "sublinear" phenomenon disappears.

The output curves characteristics for n-channel type A and type B FD-SOI devices are compared in Fig.6-14. It is demonstrated that due to the better gate controllability, at the same V_g-V_{th} voltage, the type A device exhibits better driving capability. For example, at V_g-V_{th}=0.8V, the driving current can be raised about 20 % while as the gate is changed from polycide gate to FUSI gate. At higher gate voltages, nevertheless, the current ratio between these two devices decreases. The self-heating effect owing to the large current and the poor thermal conducting buried SiO_2 layer may be the plausible reasons [6-21].

6-4 Conclusions

In this chapter, we demonstrate for the first time that the FD-SOI CMOSFETs with the FUSI-gate and MSB S/D junctions can be easily fabricated by the ITS technique simultaneously. After adjusting the poly-Si thickness at gate region and the active layer thickness at S/D region, the G/S/D electrodes can be fully-silicided under the same process condition. Using the ITS technique, not only the MSB junction could be fabricated at S/D region to enhance the I-V characteristics, but also the work function can be tuned effectively by the dopant piled-up at the interface between silicide and SiO_2 layer. Because of the effective adjustment of work function, for n-channel devices, the $V_{th,lin}$ could be shifted from -0.2V to 0.17V and that of the p-channel ones could be shifted from 0.041V to -0.47V. Excellent I_{on}/I_{off} ratio can also be achieved for both n- and p-channel devices. Because of the suppression of poly-depletion effect, for n-channel devices, the driving current can be

raised about 20% at V_g-V_{th}=0.8V.

It is thus concluded that the FUSI-ITS-MSB FD-SOI devices would be a very promising devices in the near future.

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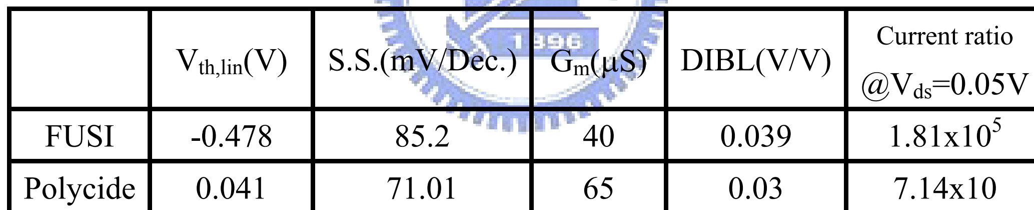
Table6-1 Device parameters of n-channel FUSI-ITS and polycide gate MSB FD SOI devices.

	$V_{th,lin}$(V)	S.S.(mV/Dec.)	G_m(μS)	DIBL(V/V)	Current ratio @V_{ds}=0.05V
FUSI	0.17	78.1	145.2	0.1	$2.83x10^4$
Polycide	-0.2	79.4	114	0.2	34

Table6-2 Device parameters of p-channel FUSI-ITS and polycide gate MSB FD-SOI devices.



	$V_{th,lin}$(V)	S.S.(mV/Dec.)	G_m(μS)	DIBL(V/V)	Current ratio @V_{ds}=0.05V
FUSI	-0.478	85.2	40	0.039	$1.81x10^5$
Polycide	0.041	71.01	65	0.03	7.14x10

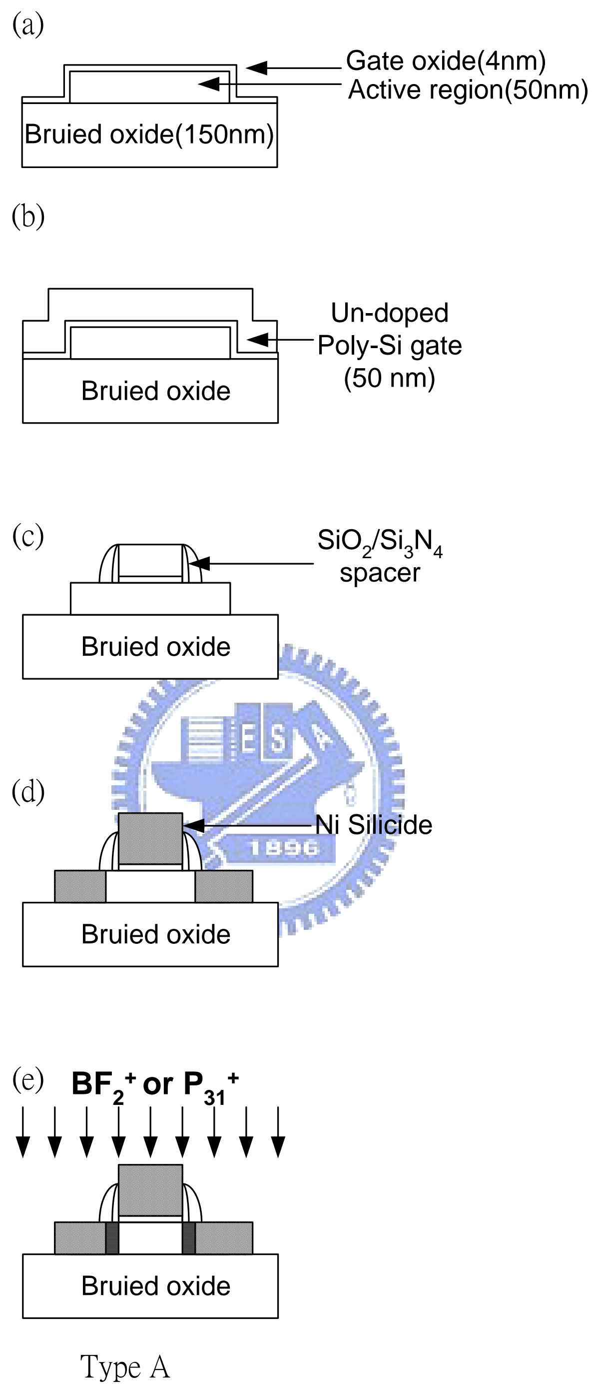


Fig.6-1 Key fabrication process steps of n-and p-channel FUSI-ITS-gate MSB FD-SOI devices.

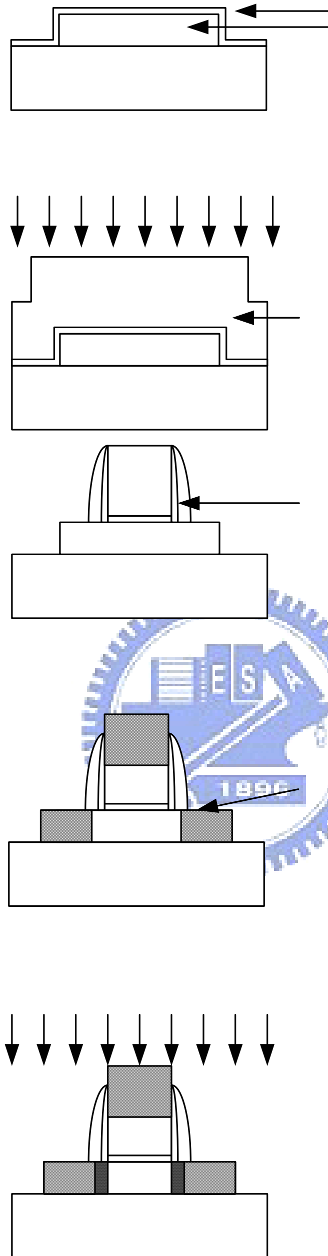
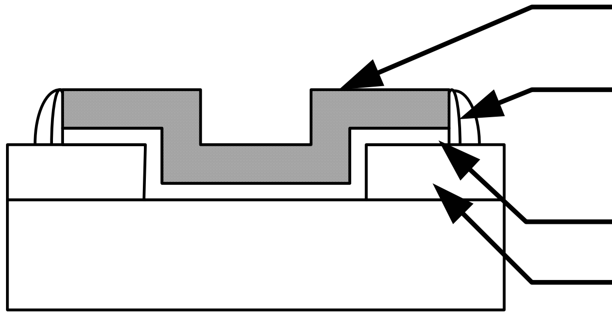


Fig.6-2 Key fabrication process steps of n-and p-channel polycide-gate MSB FD-SOI devices.

(a)



(b)

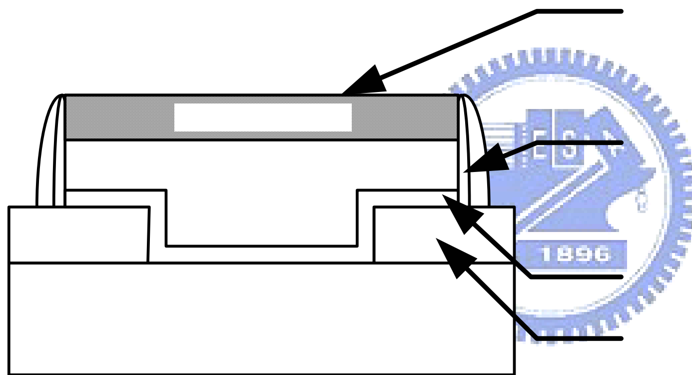


Fig.6-3 Schematic figures of (a) FUSI-ITS-gate, (b) polycide-gate MOS capacitance structures.

Si subs

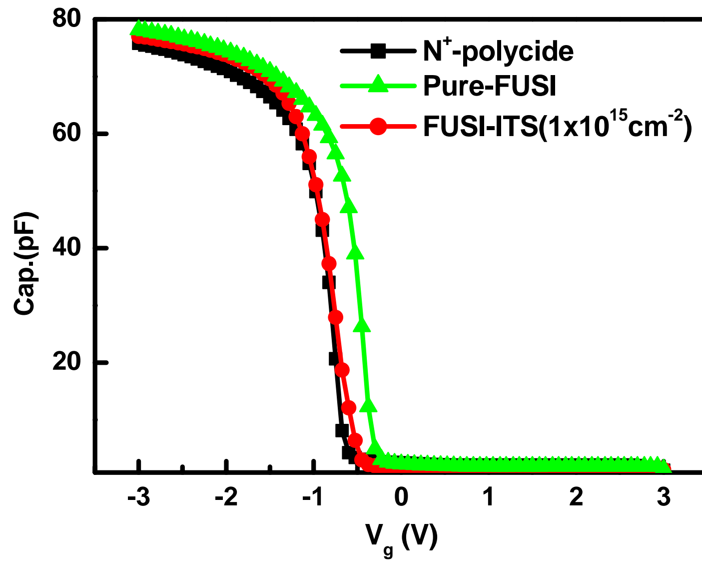
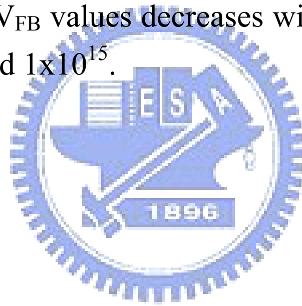


Fig.6-4 C-V Curve of Ni-Polycide and FUSI-ITS gated MOS-capacitances. For FUSI-ITS gate, the V_{FB} values decreases with the increasing of P_{31}^{+} dopants from w/o implant and $1x10^{15}$.



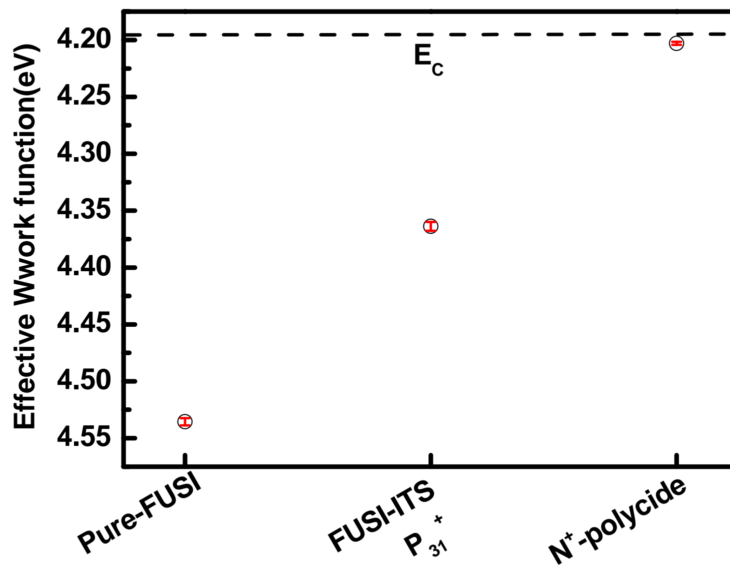


Fig.6-5 Extracted work function (Φ_m) of the NiSi and polycide gate on SiO_2.

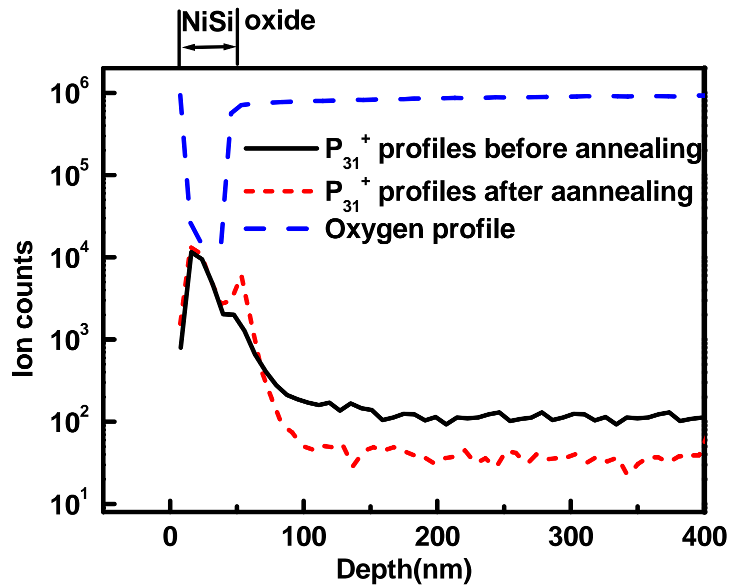
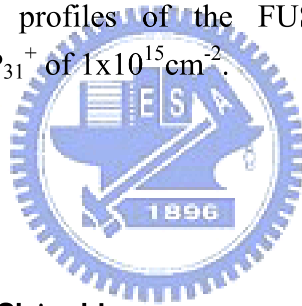


Fig.6-6(a) SIMS in-depth profiles of the FUSI-ITS-gate MOS-capacitances implanted with P_{31}^+ of $1x10^{15}cm^{-2}$.



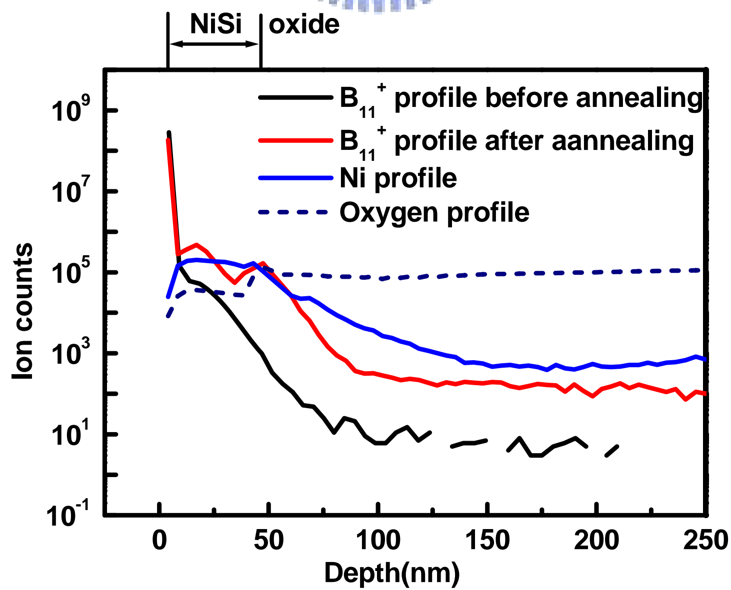


Fig.6-6(b) SIMS in-depth profiles of the FUSI-ITS-gate MOS-capacitances implanted with BF_2^+ of $1x10^{15}cm^{-2}$.

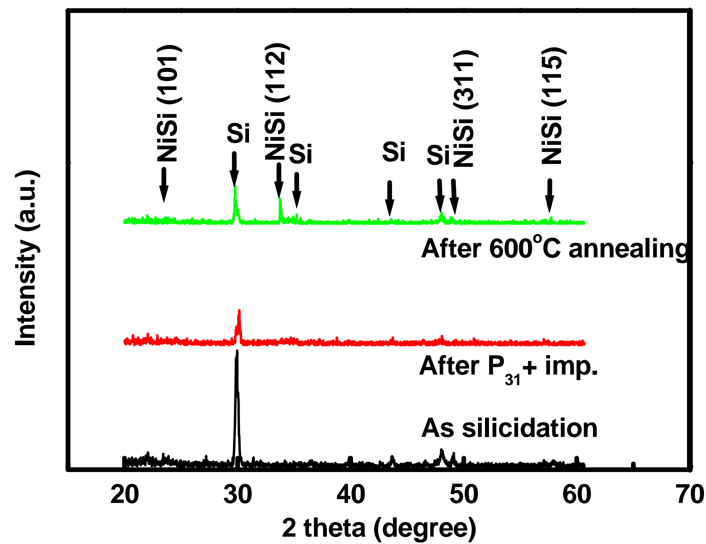


Fig.6-7 XRD profiles of FUSI-ITS samples after silicidation, P_{31}^{+} implantation, and annealing at 600°C for 30 min., respectively. The film structures after silicidation and annealing are almost the same and without any influences of impurity species.

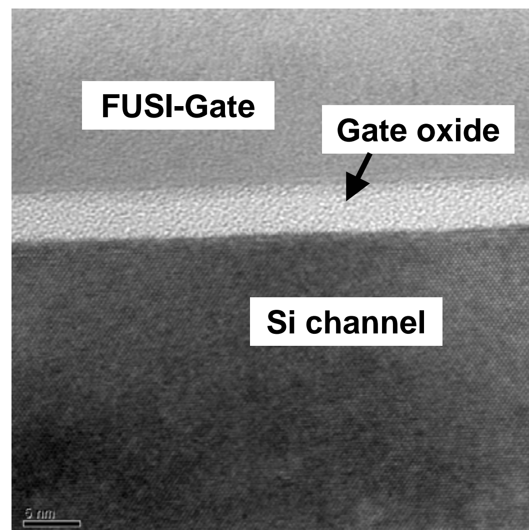


Fig.6-8 Cross-sectional TEM figure of FUSI-ITS-gate MOS-capacitances. The perfect Ni-silicide/gate oxide interface was showed; while, no residual poly-Si islands was found.

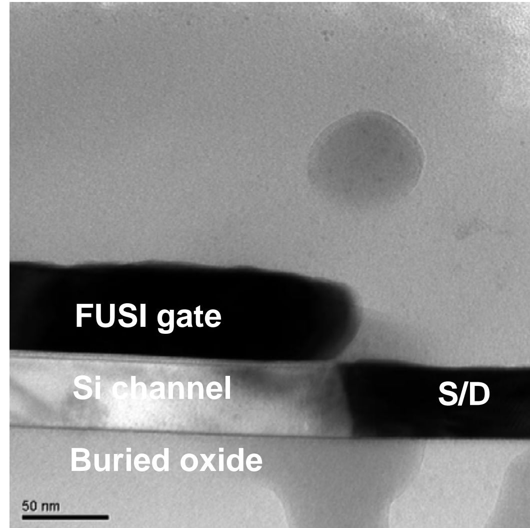
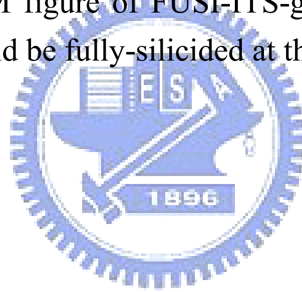


Fig.6-9 Cross-sectional TEM figure of FUSI-ITS-gate MSB FD-SOI devices. The S/D/G electrode could be fully-silicided at the same time.



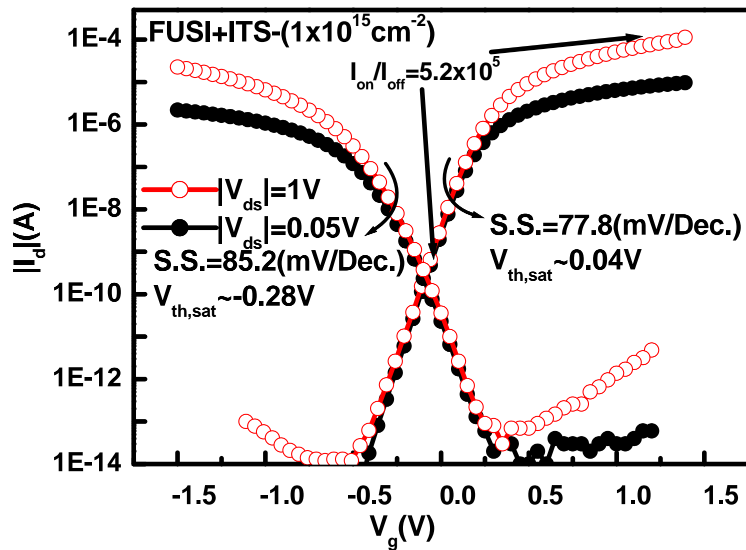


Fig.6-10 Transfer characteristics of n-and p-channel FUSI-ITS-gate MSB FD-SOI devices.

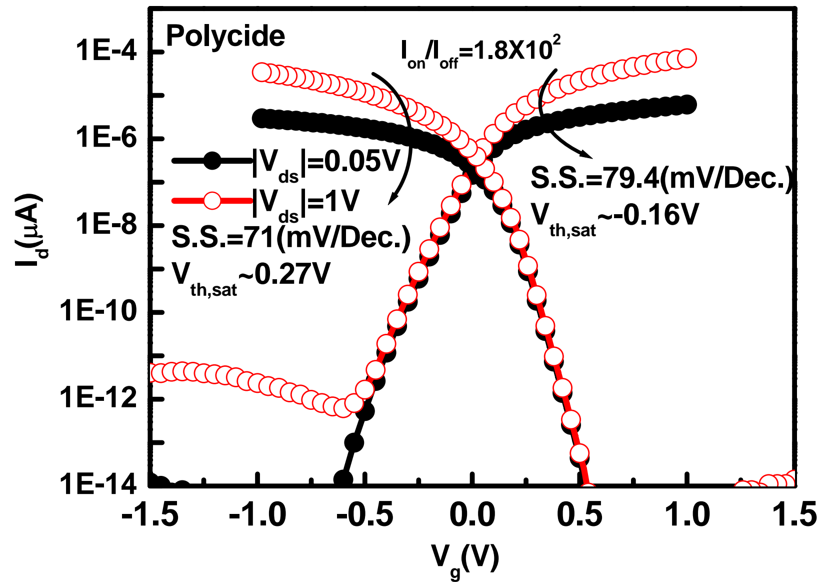
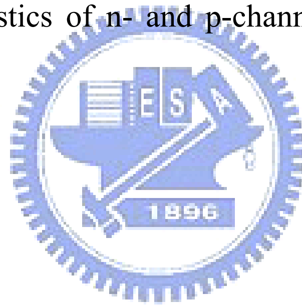


Fig.6-11 Transfer characteristics of n- and p-channel polycide-gate MSB FD-SOI devices.



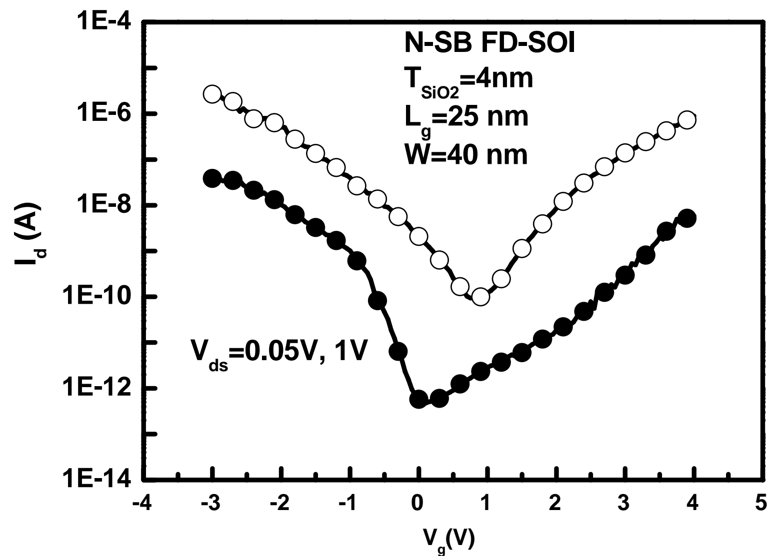


Fig.6-12 Transfer characteristics of FUSI Schottky-barrier FD-SOI device without any implantation process.

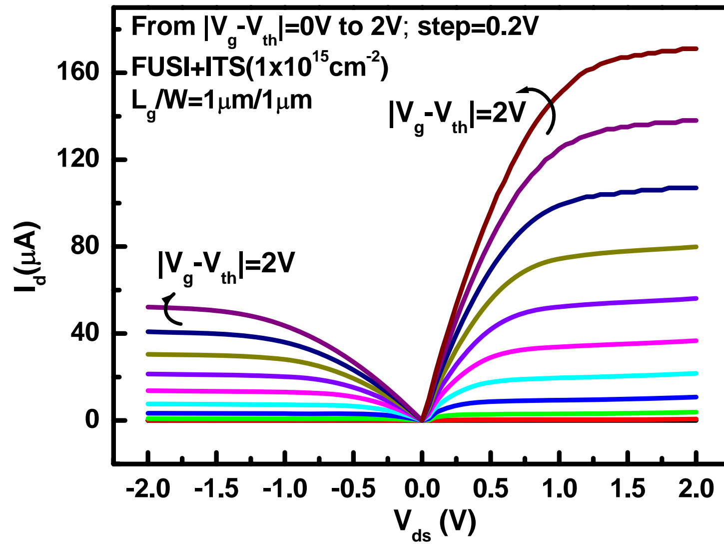


Fig.6-13 Output curves of n-and p-channel FUSI-ITS-MSB FD-SOI devices with $L_g/W=1\mu m/1\mu m$.

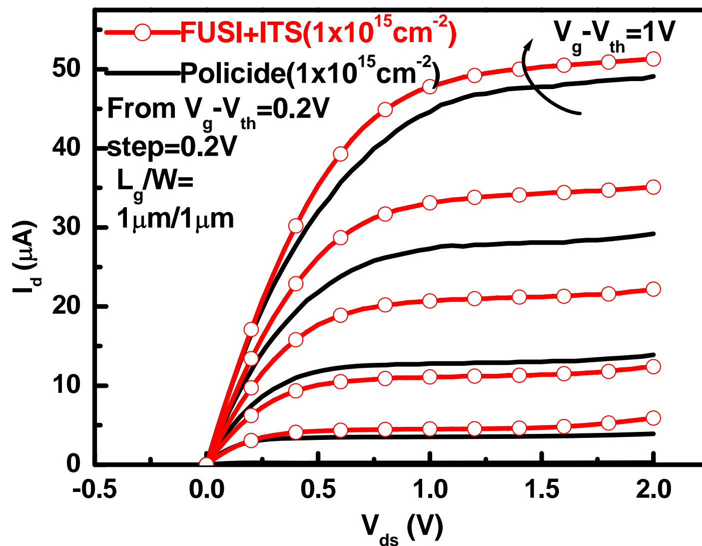


Fig.6-14 Comparisons of driving currents for n-channel FUSI-ITS and polycide MSB FD-SOI devices with $L_g/W=1\mu m/1\mu m$.

Chapter 7

Fabrication and Characteristics of FSD Poly-Si TFTs

7-1 Introduction

Polycrystalline thin-film transistors (poly-Si TFTs) are attractive for many applications including the active matrix liquid crystal display (AMLCD) and active matrix organic light emitting diode display (AMOLED) [7-1]-[7-2]. In order to integrate peripheral driving circuits on the same glass substrate, a low-temperature process (~600°C) without compromising device performance should be developed. Therefore, a long post-ion-implantation annealing which is used to activate dopants and remove implantation damages is carried out using a furnace system at around 600°C for 12-24 hours after the source/drain implantation. The prolonged process time causes low throughput in the fabrication of conventional (CN) poly-Si TFTs. To overcome this drawback, dopant activation at higher temperature of above 700°C in a rapid thermal annealing (RTA) system has been suggested to improve the activation efficiency and throughput. Nevertheless, the high temperature process violates the low temperature requirement. Thus, poly-Si TFTs suffer from a substantial trade-off between performance and throughput.

On the other hand, the use of a thinner active layer to obtain a higher driving current, lower off-state leakage current, and superior short channel characteristics has been reported [7-3]-[7-4]. Nevertheless, the high parasitic resistance due to thin source/drain (S/D) regions degrades device performance such as

driving capability and effective field-effect mobility (μ_{FE}). Especially for the AMOLED, the high S/D parasitic resistance not only reduces the brightness but also enlarge the fluctuations of brightness [7-5]. To reduce this parasitic resistance, various methods such as raised source/drain, SiGe raised source/drain, and tungsten-clad source/drain techniques were proposed [7-6]-[7-8]. Ni-salicide TFTs structure with process similar to the salicide-CMOS was also proposed to reduce the S/D parasitic resistance [7-9]. However, in order to suppress the leakage current induced by source/drain silicide spiking of salicide TFTs, not only the poly-Si at source/drain cannot be fully consumed to maintain a proper S/D junction, but also an excess mask is needed to block the gate electrode. At the same time, the long dopant activation time is still an issue in the process of salicide TFTs.

In previous chapters, high performance and reliable TGFETs have been demonstrated with MSB S/D junction. The MSB S/D junction reduces the S/D series resistance and reduces the thermal budget effectively. It is thus very straightforward to apply the similar technique to TFTs.

To reduce the S/D series resistance of CN TFTs while more efficiently improves the throughput, we proposed a novel fully-silicided S/D TFTs (FSD TFTs) with fully-silicided source/drain and ultra-short source/drain extension (SDE) at the interface of silicide and inverted channel by the implant-to-silicide (ITS) technique [7-10]-[7-15]. Forming a fully silicided source/drain by the low temperature self-aligned salicide technique, the parasitic resistance of FSD TFTs can be decreased dramatically. Adding an extension doping in the silicon by the ITS technique at about 600°C, on the other hand, not only drastically improves the contact resistance at the Ni-silicide/poly-Si junction but also abbreviates the source/drain extension length and avoids the silicide spiking effect. This concept has been approved in n- and p-channel

FinFETs and the preliminary results have been reported [7-16-[7-17].

In this chapter, we demonstrate that both n-channel and p-channel FSD TFTs can be fabricated simultaneously. The detailed fabrication process of the FSD TFTs will be described. After NH_3 plasma treatment, the characteristics of the proposed FSD TFTs are presented and discussed using CN TFTs and simple Schottky barrier (SB) TFTs as comparisons. Furthermore, the impact of activation temperature and time of the ITS process on the characteristics of FSD TFTs are also illustrated and analyzed. Excellent short channel effect is also demonstrated.

7-2 Detail Device Fabrication Steps

Fig.7-1 shows the key fabrication steps of the proposed FSD TFTs. Briefly, the fabrication was begun by depositing an amorphous Si (α-Si) layer of 50 nm thick at 550ºC in a low-pressure chemical vapor deposition (LPCVD) on 6-inch Si wafers capped with a thermal oxide layer of 1 um thick. The deposited *a*-Si layer was then crystallized by a solid-phase recrystallization (SPC) method at 600ºC in a N_2 ambient for 24 hours. After patterning the active region, a 45 nm thick CVD gate oxide and a 100nm thick poly-Si layer were deposited. The poly-Si layer was then patterned to form the gat electrode, as shown in Fig.7-1 (a). Then, a 100 nm thick CVD oxide layer was deposited and etched to form a sidewall spacer abutting the poly-Si gate, as shown in Fig.7-1 (b).

Afterwards, a self-aligned silicidation process was performed to form the fully silicided source/drain. A thin Ni layer of 25 nm thick was deposited on the wafer. After a rapid-thermal annealing at 500ºC for 40 sec in a N_2 ambient, a wet etching step in a H_2SO_4/H_2O_2 solution was then used to selectively remove the unreacted Ni. Ni-silicide was also formed on poly-Si gate simultaneously, as shown in Fig.7-1(c).

The fully silicided source/drain region shows a sheet resistance (R_{sh}) of about 7 Ω/□; whereas the nonsilicided S/D region shows an R_{sh} of about 800Ω/□. Since the poly-Si gate was also partially silicided, the gate resistance was also obviously improved by a factor of 100 compared with a nonsilicided poly-Si gate. It should be noted that the 2-step annealing process must be use to fabricate nano-scale MSB FD SOI devices because both the channel length and spacer length are very short while 1-step annealing can be used in this chapter because the channel length of TFTs in this chapter is much longer than that of SOI devices in chapter 3.

Next, implant-to-silicide (ITS) process was employed to form a shallow S/D extension (SDE) region. BF_2^+ ions were implanted to silicide at 35 KeV with $5x10^{15}cm^{-2}$ for p-channel FSD TFTs (FSD p-TFTs) and P_{31}^+ ions were implanted to silicide at 30KeV $5x10^{15}cm^{-2}$ for n-channel FSD TFTs (FSD n-TFTs). The high implantation dose is used to increase the dopant concentration of the SDE region and preserve the S/D junction characteristics [7-10, 7-12, and 7-14]. Dopants were then diffused out of silicide to form an ultra-short SDE at the channel-S/D interface by a low temperature rapid thermal annealing process in N_2 ambient at temperatures of 600, 650, 700 and 750ºC for 30, 90, and 150 sec. Because of the low solid state solubility of phosphorous and boron atoms in Ni silicide, they diffused out and piled up at the Si/silicide interface to form a ultra-short SDE as shown in Fig.7-1(d) [7-10]-[7-13]. Finally, typical inter layer dielectric deposition, contact hole patterning, and Al metallization completed the fabrication process.

The cross-sectional transmission electron microscopy (TEM) image of the proposed FSD TFTs activated at 600ºC for 30 sec in a N_2 ambient is shown in Fig.7-2 (a). From the results of energy dispersive spectrometer (EDS) analysis at the points A and B labeled in Fig. 7-2(a), it is observed that the silicided S/D doesn't growth into

the channel region and a phosphorous doped SDE region is formed. Although we could not distinguish the oxide spacer edge from the oxide passivation layer, the silicide lateral growth length (L_S) could still be extrapolated by R_{sh} measured by the four-terminal R_{sh} test structure discussed in chapter 2. It is noted that as the annealing time increases, because of the limited Ni layer thickness, the growth rate of L_S becomes slowly. Then, after a 500°C annealing at 30 sec, the average L_S from ten samples is about 26.3nm. This value is consistent with the structure shown in the TEM micrograph of Fig.7-2.

Monte Carlo simulation showed that the ions straggle distribution of BF_2^+ and P_{31}^+ are only 8 nm and 9 nm at 30 and 35 KeV, respectively, which are extremely shorter than the lateral silicide length [7-16]-[7-17]. Therefore, the ion implantation process does not damage Si layer directly. Then, the junction would be almost free of implantation damage and low junction leakage current could be expected.

For comparison, CN TFTs were fabricated, as schematically shown in Fig.7-3(a). The S/D was implanted after gate patterning followed by an activation annealing at 600ºC for 12hrs without silicidation. Simple SB TFTs without the ITS process step were also fabricated. The schematically cross-sectional structure is shown in Fig.7-3(b). In order to improve the I-V characteristics, while maintain the advantages of high throughput process of FSD TFTs, a short time NH_3 plasma treatment in a plasma-enhanced CVD (PECVD) system at 350ºC for 30 minutes was employed to effectively reduce trap-density and improve interface quality of channel region.

I-V characteristics of the fabricated devices were measured using a semiconductor parameter analyzer of model Agilent 4156C. Various device parameters, including the threshold voltage (V_{th}), subthreshold swing (S.S.), and

field-effect mobility (μ_{FE}) were extracted at a drain voltage of $|V_{ds}|$= 0.1V. The threshold voltage is defined as the gate voltage at which yields a drain current (I_d) of 1 nA/μm. The maximum and minimum values of I_{ds} at $|V_{ds}|$= 5V are designated as I_{on} and I_{off}, respectively.

7-3 Results and Discussions

7-3-1 Basic Characteristics of FSD, CN, and SB TFTs

Fig.7-4 compares the typical transfer characteristics of FSD and CN TFTs, both n- and p-channel. The nominal channel length (L) and channel width (W) are 4 μm and 1 μm, respectively. The key device parameters are summarized in Table 7-1(a). Obvious improvement in device characteristics is obtained for FSD n-TFTs in comparison with CN n-TFTs. As listed in Table 7-1, the S.S. decreases from 0.68 to 0.45 V/Dec, the μ_{FE} increases from 16.9 to 141.5 cm^2/V-sec, and the I_{on}/I_{off} ratio increases from 1.4×10^7 to 3.3×10^7. Excellent FSD p-TFTs are also obtained after NH_3 plasma treatment. For the CN TFTs, the small driving current can be attributed to the large parasitic resistance (R_p) at non-silicided source/drain. On the other hand, the superior driving capability of the FSD devices is resulted from the low series resistance due to the fully-silicided S/D and the low contact resistance of the SDE region. Since the ion implantation process does not damage poly-Si layer directly, the junction would be free of crystalline defects. Therefore, the I_{off} of FSD TFTs is almost identical to (for n-channel) or smaller (for p-channel) than that of the CN TFTs; even though a very low thermal budget (600℃, 30 sec) ITS process. It has been reported that the reverse leakage current of a P^+/N diode is smaller than that of N^+/P diode with the same ITS process, which is attributed to the faster diffusion coefficient of Boron

than that of Phosphorous in Si and NiSi [7-10]-[7-14]. For the FSD p-TFT, the SDE is wide enough and the SDE region is not damaged by S/D implantation so that the I_{off} of FSD p-TFT is lower than that of the CN p-TFT. For the FSD n-TFT, the shorter SDE region due to the slower diffusion rate of Phosphorous may be depleted at high V_{ds} so that the I_{off} is higher than that of the CN ones.

Fig.7-5 shows the transfer characteristics of SB n-TFT and SB p-TFT. The nominal channel length and channel width are 4 μm and 1 μm, respectively. For the SB TFTs, although the R_p of the S/D electrode can be effectively reduced by the fully-silicide S/D structure, low driving current is observed because of the abnormal high carrier injection resistance between silicide and channel at on-state. Moreover, at off-state, abnormal high leakage current attributed to the field emission and thermionic emission of carriers from the drain is also predicted. For example, at n-channel SB TFTs, at off state, holes at drain will inject through the Schottky barrier at interface of silicide/channel and then into channel. Similar phenomena could also be deduced at p-channel devices [7-18]. The measured as well as extracted key device parameters are listed in Table.7-1(b). To summarize briefly, the proposed FSD devices have superior characteristics to SB, and CN ones

7-3-2 Effect of Implantation Dose

In order to reveal the effect of dopant concentration on the devices performance, the transfer and output characteristics of FSD devices implanted of P_{31}^{+} with 5×10^{12}, 5×10^{13} cm^{-2} were also shown in Fig.7-6(a), (b) and (c), respectively. As the FSD TFTs with a dose of $5 \times 10^{12} cm^{-2}$, the I_{on} is strongly limited at just 0.2μA/μm at V_g=15V and the I_{off} is 200pA/μm at V_g=-5V, respectively. As the devices implanted with $5 \times 10^{13} cm^{-2}$, the I_{on} is strongly enhanced to 4.4μA/μm at V_g=15V and the I_{off} is

suppressed to 18pA/μm at V_g=-5V, respectively. The poor output characteristics of FSD TFTs with a low dose of 5x10^{13}cm^{-2} were also shown in Fig.7-6 (c). The devices implanted with fewer doses would reduce the carrier concentration at SDE region, and then, the high and wide SB junction would dominate the I-V characteristics. Especially for the devices operated at linear-state (V_{ds}=0.1V), the I_{on} was almost limited by the SB, and then stayed at a constant value. The "sublinear" curves in the output characteristics of FSD TFTs with 5x10^{12} cm^{-2} could also prove it. Operating at V_{ds}=5V, the higher V_{ds} could assist more carriers to tunnel into the channel to enlarge the I_{on}; however, it couldn't avoided that the abnormally high I_{off} due to the carriers injected into channel from drain-side induced by a large V_{ds}. The measured as well as extracted key devices parameters are also summarized in Table.7-2. Only the FSD TFTs with heavily dose could almost suppress the influence from SB at S/D junction.

7-3-3 S/D Parasitic Resistance Extraction

Figure 7-7 shows the typical output characteristics (I_d-V_{ds}) of the FSD and CN nTFTs with 5x10^{15}cm^{-2} implantation doses at several different gate voltages with W/L = 1μm/4μm. Obviously, FSD TFTs exhibit a higher driving current than CN ones, especially under high gate bias. It is because that the channel resistance becomes smaller at high gate bias; hence, the dominant resistance is the S/D parasitic resistance (R_p) [7-9]. The linear region R_p can be extracted by plotting the width-normalized on-state resistance (R_{on}) versus channel length [7-18]. In Fig.7-8 (a), all of the R_{on}-L lines merge at about L= 0.31 μm and have a residual value of a gate-voltage independent R_p of 1.35 KΩ-μm. In Fig.7-8 (b), the extracted R_p of CN TFTs is 17.63 KΩ-μm, which is about 13 times larger than that of FSD TFTs. Besides the R_p variations, because of the smaller thermal budget, the ΔL (the different between the

mask channel length and the effective channel length) of FSD devices (ΔL=0.31μm) is smaller than that of CN TFTs ones (ΔL=0.35μm). As a result, the FSD n-TFTs have smaller R_p and better turn-on characteristics than the CN ones.

7-3-4 Effects of Activation Temperature

The activation temperature is the most important process parameters to form SDE and activate dopants in the ITS process. To avoid the influence of dopants segregation, a heavy dose of $5x10^{15}cm^{-2}$ was used to study the effect of activation temperature [7-20]. The transfer characteristics of FSD n-TFT and p-TFT experienced different activation temperatures without NH_3 plasma treatment are shown in Fig.7-9 (a) and (b), respectively. The extracted device parameters of FSD n- and p-TFTs are listed in Table 7-3 (a) and (b), respectively.

It should be noted that as the activation temperature increases from 600°C to 750°C, both the characteristics of n- and p-channel devices degraded obviously. Clearly, the devices activated at 600ºC and 650ºC result in the best performance for both FSD n- and p-TFTs. The slight deviation of V_{th}, S.S., μ_{FE}, as well as I_{on}/I_{off} current ratio may come from the process deviation. By increasing the RTA temperature to higher than 650ºC, the degradation of absolute value of V_{th}, S.S., $\mu_{FE,}$ and N_t extracted using the modified Levinson's method are clearly observed [7-21]-[7-22]. However, the off-state current (I_{off}) slightly decreases with the increase of RTA temperature. It is well known that the I_{off} of TFT device is dominated by the quality of the S/D junction [7-23]. The continuous reduction of I_{off} implies that the higher activation temperature results in longer diffusion length and higher dopant concentration of SDE.

In order to distinctly clarify the degradation mechanisms of devices with high annealing temperature, not only the R_s but also the effective trap-state density (N_t) of source/drain and gate electrode with different activation temperature are extracted and shown in Fig. 7-10 and 7-11, respectively. As shown in Fig. 7-10, at the gate electrode, as the annealing temperature increases from 600 to 750ºC, the R_{sh} increases singularly from ~6.3 Ω/□ to 23.2 Ω/□. Oppositely, at the S/D electrode, the R_{sh} remains stable at about 7 Ω/□ even after 750ºC annealing.

From the Fig.7-11, the N_t raises steeply as the activation temperature increases, especially at the temperature larger than 650°C. Moreover, from the Fig.7-12, the J_g vs. V_g plots of FSD TFTs with various activation temperatures are also demonstrate that the higher activation temperature could also degrade the gate leakage properties. For example, at V_g=15V, the leakage current density (J_g) would increases from 2.05 μA/cm^2 to 7.24 μA/cm^2 with the temperature increasing from 600°C to 750°C.

Therefore, since the S/D integrity is maintained, the device degradation mechanism can be indeed related to the gate electrode. On the other hand, from the material analysis, according to the SEM images of silicide at gate region, as shown in the Fig.7-13 (a)-(d), we also demonstrated that the silicide agglomeration occurs at gate electrode after annealing above 650ºC.

The X-ray diffraction (XRD) spectra of the silicide gate electrode after various annealing conditions are shown in Fig.7-14. The main phase of Ni silicide is NiSi after 600 ºC annealing. Nevertheless, after 750 ºC annealing, both NiSi and $NiSi_2$ were detected. It is known that the thermal stability of Ni-silicide is not as good as that of Ti-silicide or Co-silicide [7-24]-[7-27]. Annealing at temperature higher than 700℃ usually results in agglomeration of Ni-silicide [7-10]. Especially for the

silicide/poly-Si stack structure, to reduce the silicide surface energy and the grain boundary energy of the poly-Si, not only the agglomeration but the silicide inversion and intermixing phenomenon are also occurred at lower temperature annealing than that of silicide on crystalline-Si substrate [7-28]-[7-29]. It has been postulated that the layer inversion and intermixing of silicide at silicide/poly-Si gate electrode may degrade gate dielectric because of the difference in thermal expansion between silicide and poly-Si [7-30]-[7-31]. Moreover, from the dark field TEM micrograph and EDX spectrum of gate electrode for FDS TFT after 750°C RTA for 30 seconds were also shown in Fig.7-15 (a)-(c). After annealing, the polycide gate electrode was transferred to fully silicided gate electrode, and very few poly-Si islands were separated by the silicide regions.

After annealing at temperatures higher than 650 ºC, both the extracted R_{sh} and the SEM images show that the S/D electrode was maintained perfectly. However, both the extracted R_p and the difference between the drawn channel length and the effective channel length (ΔL) rose as the annealing temperature increased. As annealing temperature increases from 600°C to 750°C, the R_p increases from 1.35 KΩ-μm to 13 KΩ-μm; at the same time, the ΔL also rises from 0.13 to 1.03 μm. It means that not the S/D electrode but the interface between the S/D/channel junctions degrade and severely affect the devices characteristics. To extract the mechanism distinctly, the TEM micrograph and EDX spectrum of FSDTFT after 750°C for 30second annealing were displayed in Fig.7-16 (a)-(c). It must be pointed out that the silicide grows deeply into the channel (~0.45μm).

Although the S/D electrode was fully-silicide structure, the inversion and intermixing couldn’t appear. However, at the interface between S/D and channel, the silicide at S/D could still contact with poly-Si directly. Therefore, not only the silicide

was grown deeply into the channel region but also the S/D junction characteristics, SDE doping concentration were possibly degraded. Moreover, because of the silicide contact the gate dielectric directly from S/D and gate electrode, the mechanical stress may be the plausible reason of worse I_d-V_g curve at higher temperature annealing. And therefore, the I_d-V_g, J_g-V_g, and R_{on}, and ΔL characteristics were deteriorated distinctly after annealing with temperature higher than 650°C.

As the activation temperature increases, combining the effect of silicide intermixing at gate electrode and the silicide deep extension at the S/D junction, the N_t and R_p increase, and therefore, the absolute value of V_{th} and S.S. increases and that of μ_{FE} decrease for both n- and p-TFTs.

7-3-5 Effects of Activation Time

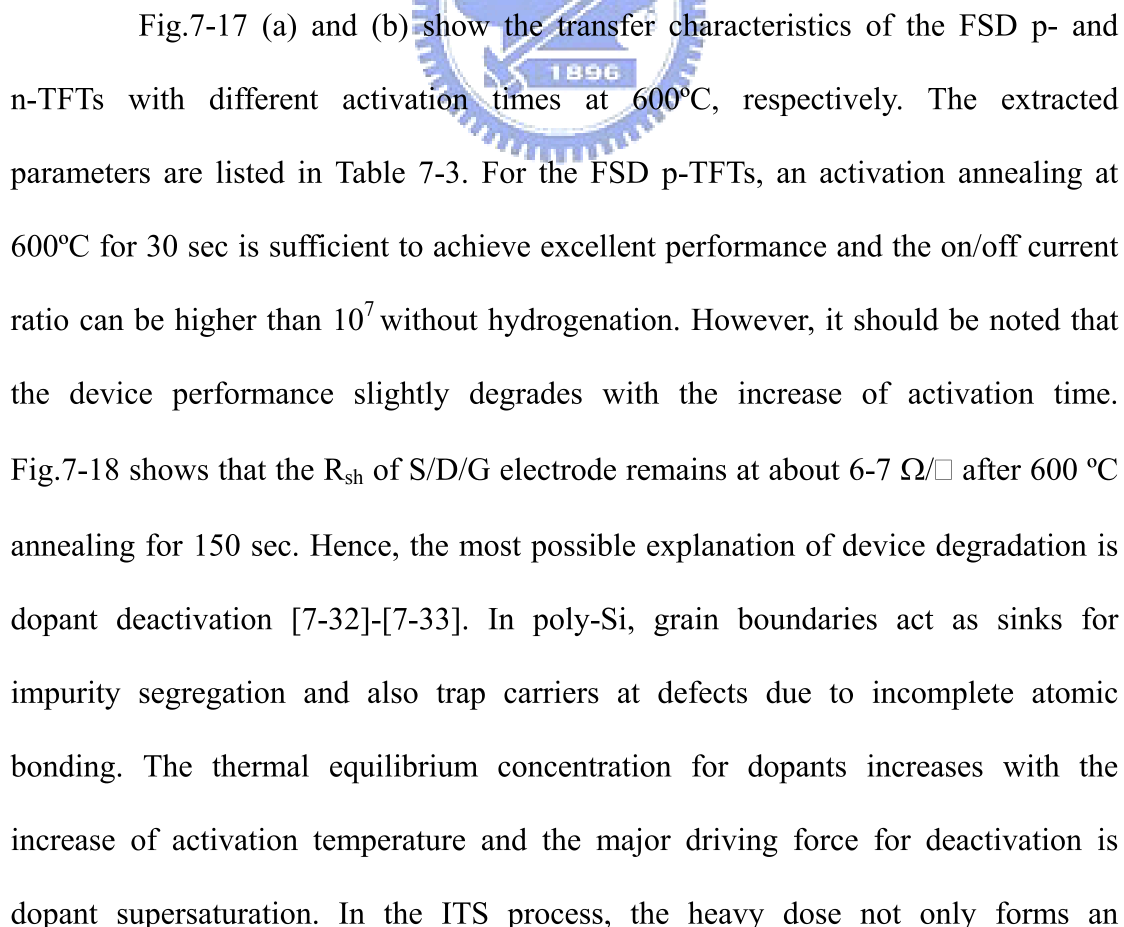


Fig.7-17 (a) and (b) show the transfer characteristics of the FSD p- and n-TFTs with different activation times at 600ºC, respectively. The extracted parameters are listed in Table 7-3. For the FSD p-TFTs, an activation annealing at 600ºC for 30 sec is sufficient to achieve excellent performance and the on/off current ratio can be higher than 10^7 without hydrogenation. However, it should be noted that the device performance slightly degrades with the increase of activation time. Fig.7-18 shows that the R_{sh} of S/D/G electrode remains at about 6-7 Ω/□ after 600 ºC annealing for 150 sec. Hence, the most possible explanation of device degradation is dopant deactivation [7-32]-[7-33]. In poly-Si, grain boundaries act as sinks for impurity segregation and also trap carriers at defects due to incomplete atomic bonding. The thermal equilibrium concentration for dopants increases with the increase of activation temperature and the major driving force for deactivation is dopant supersaturation. In the ITS process, the heavy dose not only forms an

ultra-short SDE but also fills grain boundaries in the short activation time. More activated dopants fill grain boundaries with the longer activation time and dopants deactivate during cool-down from activation temperature to room temperature. Dopant deactivation reduces the concentration of the SDE, and therefore, can explain the degradation of some device performances including V_{th}, S.S., μ_{FE} and I_{on}.

For the FSD n-TFTs, similar to the FSD p-TFTs, an ultra-short SDE is also formed after a short activation time of 30 sec. Unlike boron, phosphorus has small diffusivity [7-34]. A 30 sec activation may be insufficient to form an intact SDE. By increasing the activation time, dopants diffuse out of silicide and all of the Ni-silicide grains are surrounded by SDE. Therefore, some device characteristics such as S.S. and I_{off} are improved. For the reduction of mobility and I_{on}, dopant deactivation is still a possible reason. Although I_{on} slightly reduces, the I_{on}/I_{off} current ratio increases with the increase of activation time. This is explained by the obvious reduction of I_{off}. According to this discussion, a 30 sec RTA is a suitable activation time for both FSD n- and p-TFTs.

7-3-6 Short Channel Behavior

The short channel effect (SCE) of the FSD and CN TFTs (both n and p-channel) as evaluated by the threshold voltage drop with channel length reduction is shown in Fig.7-19. The ΔV_{th} here is defined as the differences between the V_{th} of short channel devices and the V_{th} of a 10 μm device. Because of long dopant diffusion length ascribed to long activation time and fewer grain boundary in the short channel devices, the V_{th} of CN n-TFTs reduces from 7.11 to 2 V and that of CN p-TFT reduces from -8.1 to -3.9 V as channel length decreases from 10 μm to 1.2 μm obviously [7-35]. On the contrary, in the FSD TFTs, the strongly resist of V_{th} roll-off

are found for both n- and p-TFTs. As channel length decreases from 10μm to 1.2 μm, the V_{th} of FSD n-TFTs just slightly reduces from 5 to 4 V and that of FSD p-TFTs reduces from -7.5 to -5 V. The excellent short channel effect of FSD devices can be attributed to not only the shorten SDE by the low thermal budget ITS process, but also the SDE/silicide effective trap-state density [7-36]-[7-37].

7-3-7 Reliability Issues of FSDTFTs

As poly-Si TFT technology becomes mature for SOP applications, not only high-speed operation but also high reliability is required. However, the presence of grain boundaries in the channel of the transistor enhances significantly the local electric field near the drain junction, generating energetic hot-carriers from impact ionization [7-38]-[7-39]. As a result, oxide carrier trapping and generation of interface states and grain-boundary defects cause long-term performance instability, and therefore, reliability becomes a major limiting factor for the design of TFTs circuits [7-40]-[7-41].

In this section, the CN and FSD TFTs with W/L=5μm/5μm were used. The I_{on} was measured at V_{ds}=5V and V_g=15V, while the I_{off} was measured at V_{ds}=5V and V_g=-5V, respectively. Moreover, to check the worst stress condition of the FSD and CN n-TFTs, devices were stressed at V_{ds}=20V with various V_g (from 6V to 26V) for 3600 seconds, and then, the degradation of I_{ds} is shown in the Fig. 7-20. Mainly, two degradation regions can be recognized in this figure. One involves the degradation caused by self-heating due to the high current stress condition ($V_g \geq V_{ds}$). The other involves the hot-carrier injection originating from the high drain electric field at the stress condition of $V_{ds} >> V_g > V_{th}$. For the high current stress condition, the degradation rate increases with the increase of stress current, but for the hot carrier stress

condition, the degradation rate depends on the strength of the drain electric field [7-42]. It can be seen that the most serious degradation occurs at V_g=6V for both CN and FSD TFTs owing to the hot-carrier stressing. The I_{on} of FSD TFTs decays 30% and that of CN ones decays 35%. At the self-heating stress condition (V_g=V_{ds}), the I_{on} of FSD TFTs doesn't show the obviously degradation but that of CN ones decay about 15%. Therefore, the reliability of FSD TFTs is better than that of CN ones at either hot-carrier or self-heating stressing conditions.

To clarify the degradation mechanism clearly, forward and reverse mode measurement were used before and after the device stressing at hot-carrier and self-heating stressing conditions. For the forward mode measurement, after hot-carrier stressing, in which the drain was connected to the positive voltage and the source was grounded. On the other hand, for the reverse mode, the roles of source and drain were switched.

Fig. 7-21 (a) and (b) illustrate the typical degradation phenomena of FSD and CN TFTs caused by hot carrier effect, respectively. For the device degradation caused by the hot-carrier effect, the V_{th} and S.S. were almost unchanged after stressing. However, the I_{on}, I_{off} and G_m were all degraded. Wu et. al., suggested that the creations of strain-bond tail states near the drain-side is the dominant mechanism [7-43]. For poly-Si TFTs under hot carrier stress, N. D. Young also pointed out that the hot holes injecting into the gate oxide near the drain junction caused by high electric field is also accompanied with high drain bias stress [7-39]. However, for both FSD and CN n-TFTs, under the hot-carrier stress, the V_{th} is slightly positive shifted and I_{off} current raises, and therefore, the effects of hot-hole trapping in the oxide are screening by the interface state generated near the drain junction, i.e. the interface state generated near the drain-side caused by the breaking of weak Si-H and Si-Si

bonds is the dominant degradation mechanism in hydrogenated poly-Si TFTs under hot-carrier stress [7-44].

In the reverse mode measurement, this interface state generation near drain-side in the forward mode cannot be screened by the drain-voltage again. Therefore, in the Fig.7-22(a) and (b), the reverse mode measurement results of FSD and CN TFTs show the seriously degradation of V_{th}, I_{on}, S.S. and G_m.

Although the degradation mechanisms of FSD TFTs under hot-carrier stress are very similar to that of CN TFTs, the FSD TFTs have better resistivity to the electric stress than that of the CN ones. To demonstrate it, in the Fig.7-23, a dual power-law time dependence of the G_m degradation of the form At^n is observed for both FSD and CN TFTs indicates the presence of two degradation mechanisms. Several papers have pointed out that n=0.2 corresponds to single electron or hole hot-carrier injection and n=0.5 is typical for both electron and hole injection [7-45]. Moreover, F. V. Farmakis also pointed out that for n~0.5 in TFTs is owing to the trap-state generation in the poly-Si grain-boundary and interface-state together with both electron/hole carriers injection [7-45].

For CN TFTs, the n values transited from n~0.47 to n~0.2 after about 50~100sec stressing demonstrates that the generated states at the poly-Si/SiO_2 interface and grain-boundaries are the dominant degradation mechanism at the early stages of the degradation process. As the stress process proceeds further, the carrier trapping in the oxide then dominates the degradation mechanism. For FSD TFTs, similar transition also appeared quickly about 20~50sec stressing and slightly earlier than that of CNTFTs. Moreover, the second n-value is just about 0.1 and almost saturated. The quickly saturation of defects could be explained by the better poly-Si quality near drain-junction of FSD TFTs. Although the activation process of FSD

TFTs with ultra-low thermal budget, the dopant didn't implant and damage the poly-Si directly, that may be the plausible reason.

Next, we also show the results of forward mode measurement of FSD and CN TFTs before and after self-heating stress were also showed in the Fig. 7-24(a) and (b), respectively. It should be noted that for the FSD TFTs, after stressing, the I_{on} and G_m increases, I_{off}, V_{th}, and S.S. decreases could be attributed to the hole-trapping in the gate oxide near the drain-side. However, for the CN TFTs, the I_{on}, I_{off}, V_{th}, G_m, and S.S. are all degraded. It is also attributed to that the interface state generated near drain sides in the CN TFTs could screen the hole-trapping effect effectively. In the Fig. 7-25 (a) and (b), the result of reverse-mode measurement of FSD and CN TFTs before and after stressing at self-heating stress conditions is also displayed. It is also showed that for CN n-TFT, under self-heating stress, the S.S. and V_{th} degraded, and then, the deep-state creation at the mid-gap dominates the degradation [7-43].

Therefore, for FSD TFTs, not only have superior I-V characteristics, but also, have strong resistivity to the electrical stressing attributed to the implant-damage-free poly-Si films.

7-4 Conclusions

Besides the applications of ITS technique on the TGFETs, in this chapter, the concept of high performance FSD n- and p-TFTs with ultra-low parasitic resistance fully silicide S/D and ultra-short SDE by simple, low-temperature ITS process has been proposed. Moreover, we reported that both FSD n- and p-TFTs can be fabricated simultaneously. Detailed fabrication process, basic device characteristics, as well as the impact of activation temperature and time of ITS process are all discussed. It is demonstrated that as the annealing temperature becomes higher than

650ºC, the silicide inversion and intermixing occurs at gate electrode and then the electrical characteristics of FSD TFTs degrade. Device degradation due to dopant deactivation of long activation time is also observed. Since the ITS process does not damage the active layer and most dopants are fast diffuser in Ni-silicide, annealing at 600ºC for 30 sec is sufficient to produce excellent FSD n- and p-TFTs.

The experimental results show that the proposed devices not only depictly improves turn-on characteristics by successfully reducing the S/D parasitic resistance but also maintain the low off-state leakage current. Superior short channel characteristics are also observed, which is explained by the low thermal budget ultra-shallow SDE. The reliability results also show that the proposed FSD TFTs have slightly better immunity to the electrical stressing than the CN TFTs. Using the novel implant-damage-free ITS process, the poly-Si films quality can be maintained after S/D extension process, and therefore, during stressing, the state-creation can be avoided effectively.

Therefore, the proposed FSD TFTs are ideally suitable for implementing high-density and high performance driver circuits on the glass panel for AMLCD, AMOLED, and system-on-panel applications.

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Table.7-1 Extracted device parameters of (a) FSD & CN TFTs and (b) SB TFTs.

(a)

	$V_{th,lin}$ (V)	S.S. (V/Dec)	μ_{FE} (cm^2/ V-sec)	I_{on}/I_{off} @V_{ds}=5V
FSD n-TFT	3.4	0.45	141.5	$3.3x10^7$
CN n-TFT	3.6	0.68	16.9	$1.4 x10^7$
FSD p-TFT	-6.3	0.72	55.2	$2.2 x10^7$
CN p-TFT	-6.4	0.85	10.7	$1.3 x10^5$

(b)

	$V_{th,lin}$ (V)	S.S. (V/Dec)	μ_{FE} (cm^2/ V-sec)	I_{on}/I_{off} @V_{ds}=5V
SB n-TFT	5.1	0.97	49.6	$3.1 x10^4$
SB p-TFT	-9.3	0.55	21.4	$2.63 x10^6$

Table7-2 Extracted device parameters of FSD n-TFTs with $5x10^{15}cm^{-2}$, $5\ x10^{13}cm^{-2}$ and $5\ x10^{12}cm^{-2}$.

	$V_{th,lin}$ (V)	S.S. (V/Dec)	μ_{FE} (cm^2/ V-sec)	I_{on}/I_{off} @V_{ds}=5V
$5x10^{15}cm^{-2}$	3.4	0.45	141.5	$3.3x10^7$
$5\ x10^{13}cm^{-2}$	3.6	0.68	6.7	$7.3x10^5$
$5\ x10^{12}cm^{-2}$	X	0.985	0.75	$1.3\ x10^4$

Table7-4 Extracted device parameters of FSD (a) n- and (b) p-TFTs after different annealing temperatures from 600ºC to 750ºC for 30sec without NH_3 plasma treatment.

(a)

RTA Temperature (ºC)	$V_{th,lin}$ (V)	S.S. (V/Dec)	μ_{FE} (cm^2/ V-sec)	I_{on}/I_{off} @V_{ds}=5V
600ºC	7.18	1.6	70.6	1.77 x10^6
650ºC	4.7	1.4	49.9	2.13 x10^6
700ºC	16.96	1.88	7.3	5.41 x10^5
750ºC	>20	2.18	0.4	1.66 x10^4

(b)

RTA Temperature (ºC)	$V_{th,lin}$ (V)	S.S. (V/Dec)	μ_{FE} (cm^2/ V-sec)	I_{on}/I_{off} @V_{ds}=5V
600ºC	-6.7	1	33.6	1.52 x10^7
650ºC	-8.5	1	35	6.8E x10^6
700ºC	-15.3	1.2	9.7	8.6 x10^5
750ºC	-19.5	2.8	2.9	1.1 x10^5

Table7-5 Extracted device parameters of FSD (a) n- and (b) p-TFTs after different activation times from 30 sec to 150 sec at 600ºC without NH_3 plasma treatment.

(a)

RTA Time (sec)	$V_{th,lin}$ (V)	S.S. (V/Dec)	μ_{FE} (cm^2/ V-sec)	I_{on}/I_{off} @V_{ds}=5V
30	7.2	1.6	70.6	1.8 x10^6
90	6.2	1.5	57.6	3 x10^6
150	8.3	1.2	33.9	1 x10^7

(b)

RTA Time (sec)	$V_{th,lin}$ (V)	S.S. (V/Dec)	μ_{FE} (cm^2/ V-sec)	I_{on}/I_{off} @V_{ds}=5V
30	-6.7	1	33.6	1.5 x10^7
90	-7.1	1	40.1	1.2 x10^7
150	-10.6	1.3	20.7	5.2 x10^6

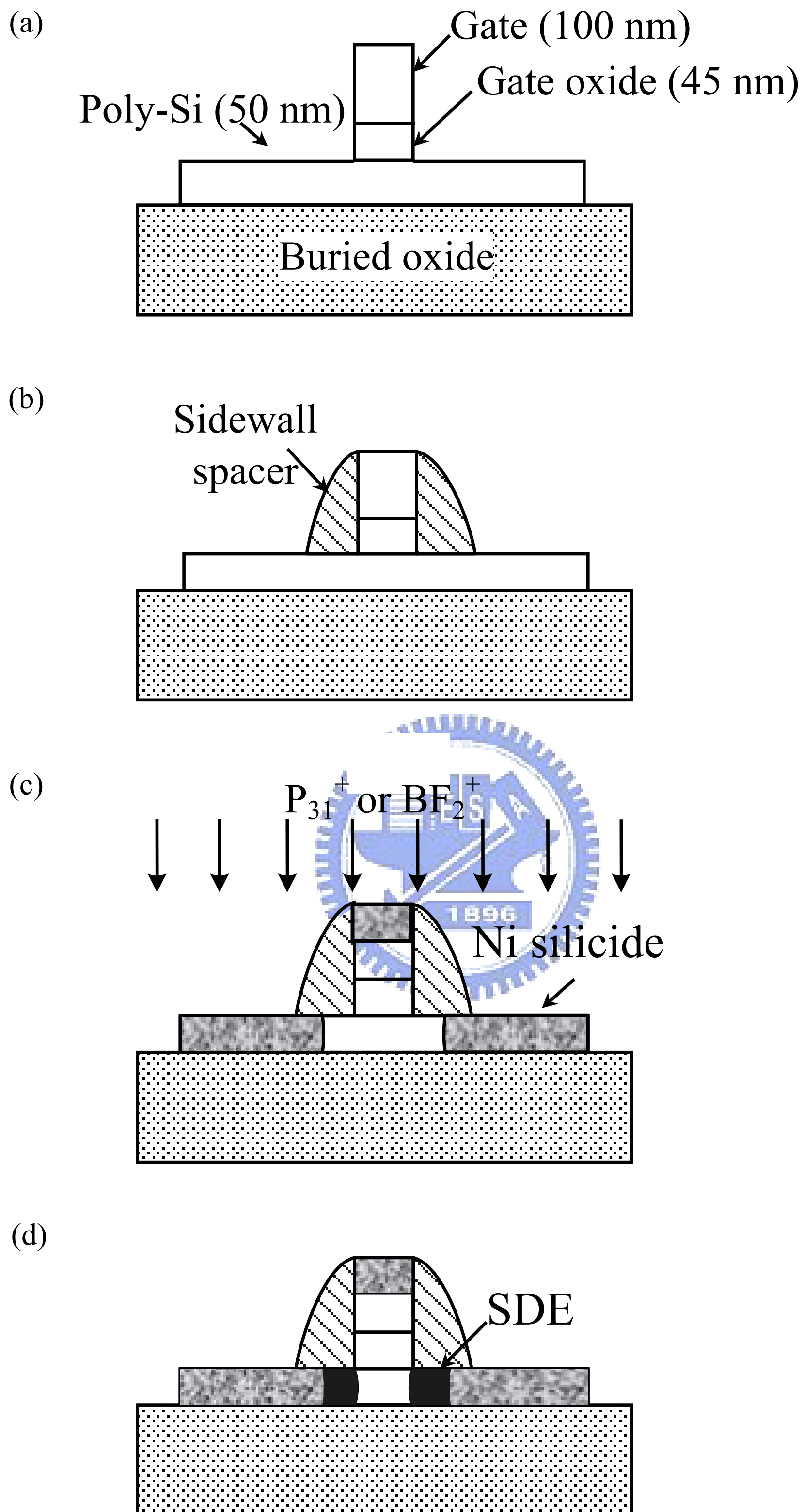
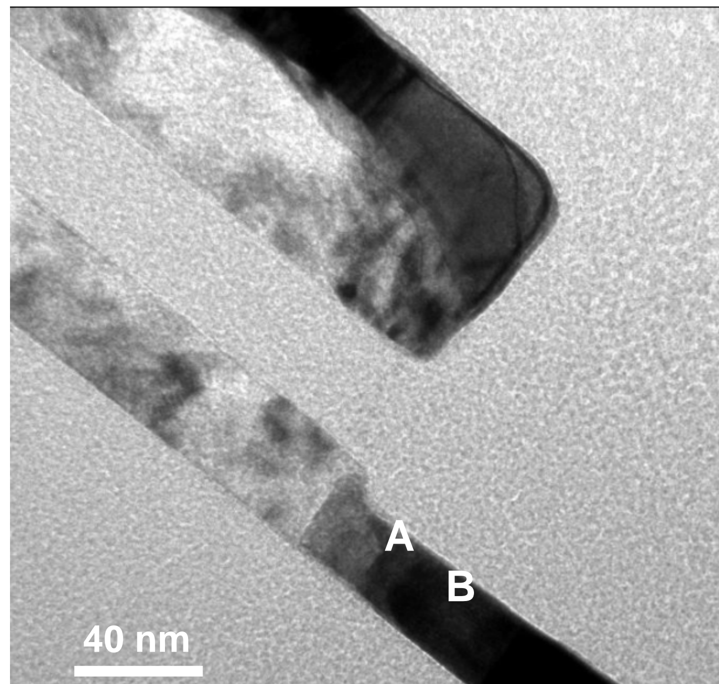
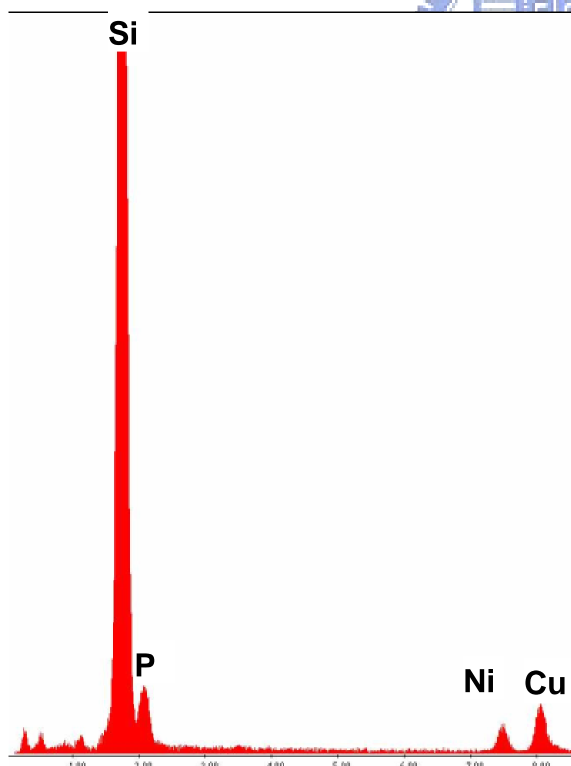


Fig.7-1 Key fabrication steps OF the proposed FSD TFTs.

(a)



(b)



(c)

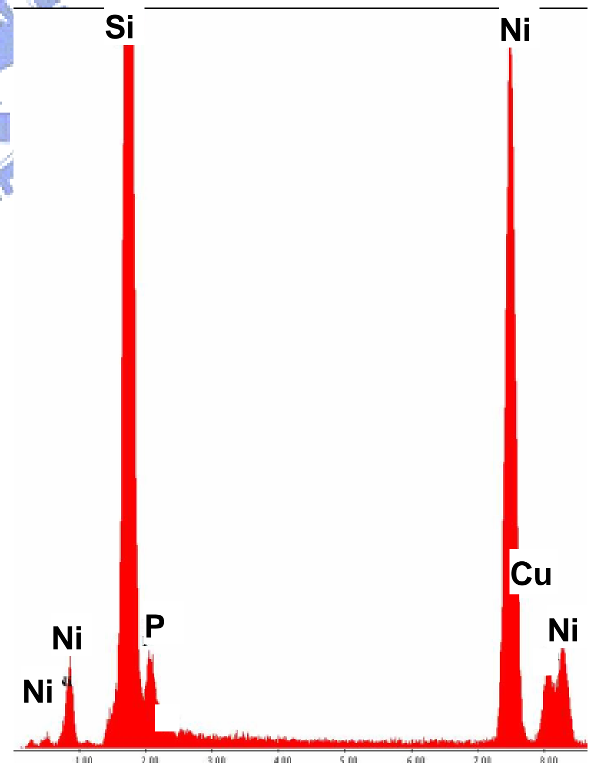
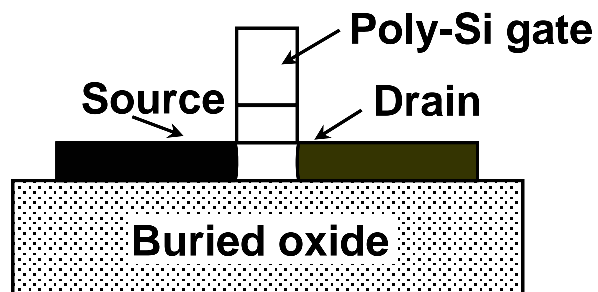


Fig.7-26 Cross-sectional transmission electron microscopy (TEM) image of the proposed FSD TFTs activated at 600ºC for 30 sec in a N_2 ambient. (b) The EDX analysis data of point “A”.(c) The EDX analysis data of point “B”.

(a)



(b)

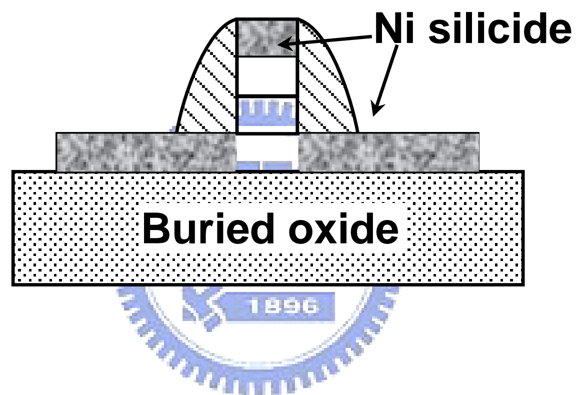


Fig.7-3 Schematic cross-sectional drawings of (a) CN TFTs and (b) SB TFTs.

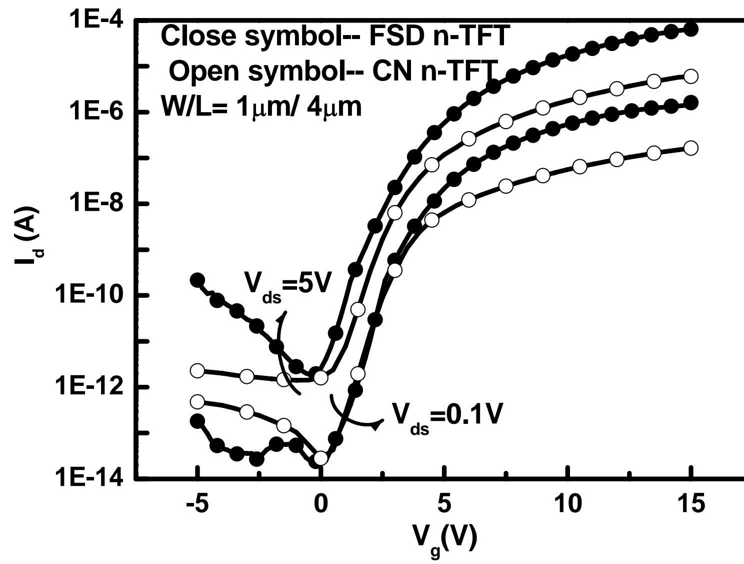


Fig.7-4(a) Typical transfer characteristics of FSD and CN n-TFTs after NH_3 plasma treatment.

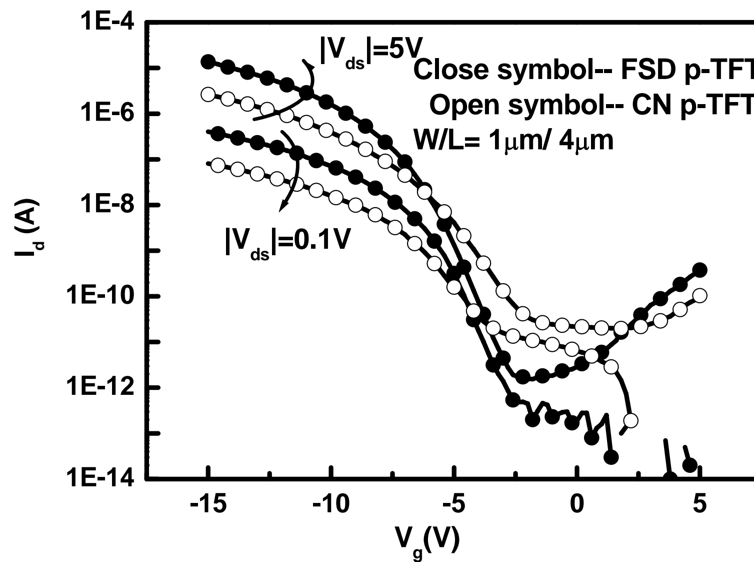


Fig.7-4(b) Typical transfer characteristics of p-channel FSD and CN p-TFTs after NH_3 plasma treatments.

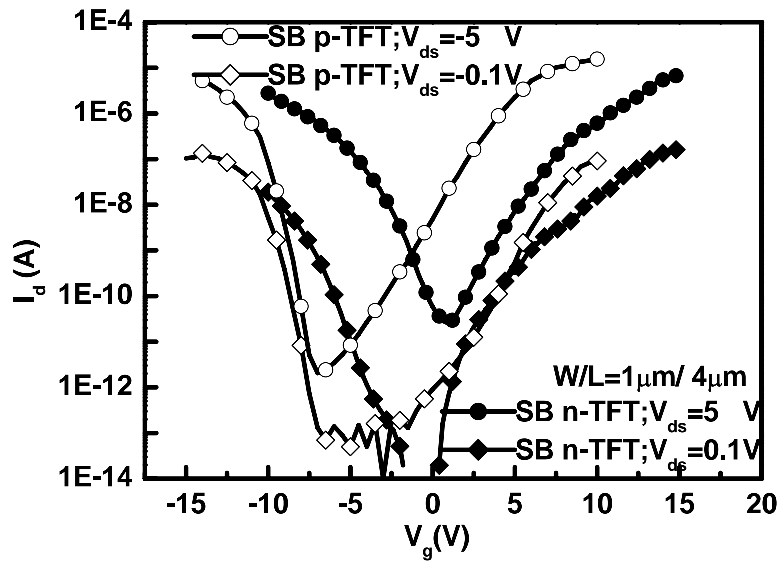


Fig.7-5 Typical transfer characteristics of SB n- and p-TFTs after NH_3 plasma treatment.

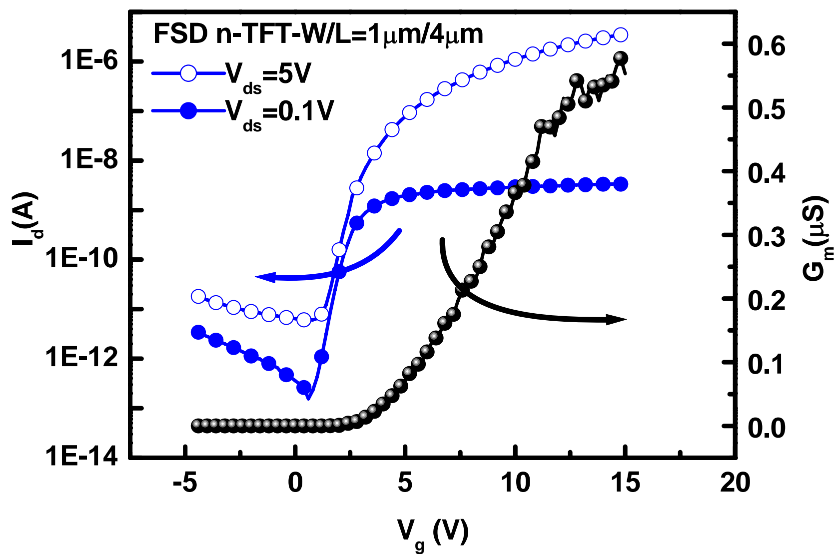


Fig.7-6(a) Typical transfer characteristics of FSD n-TFTs implanted P_{31}^{+} with $5x10^{12}cm^{-2}$.

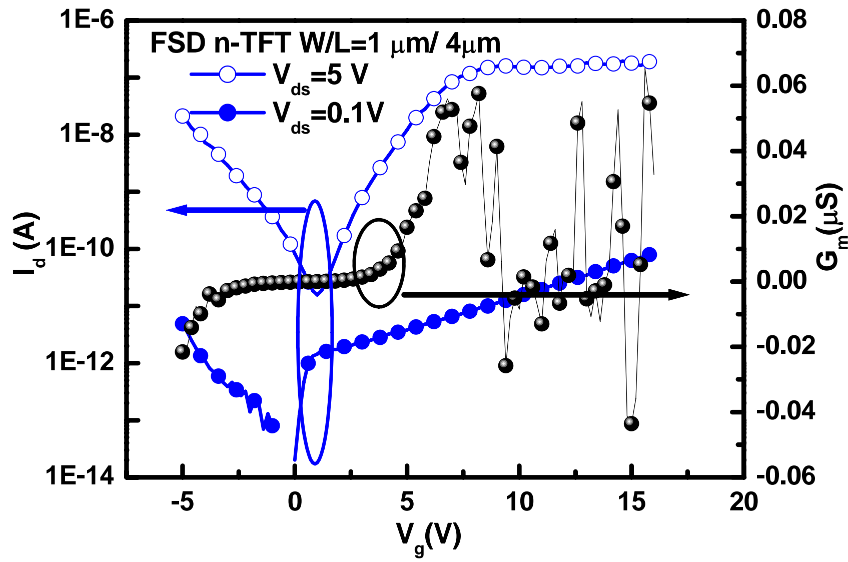


Fig.7-6(b) Typical transfer characteristics of FSD n-TFTs implanted P_{31}^{+} with $5x10^{13}cm^{-2}$.

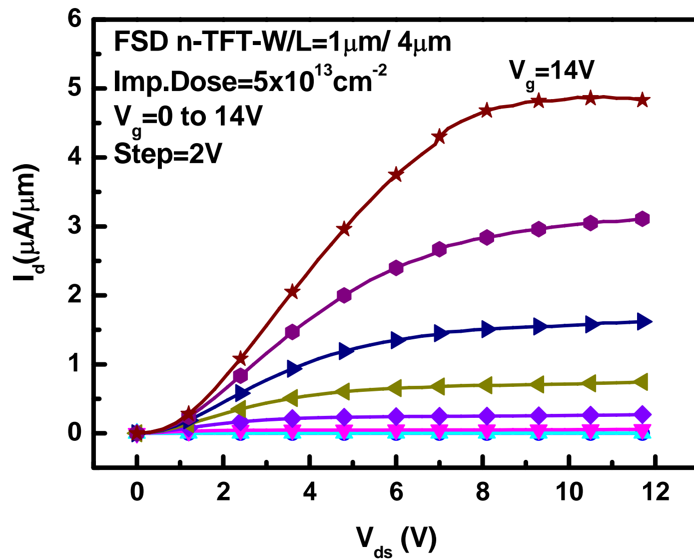


Fig.7-6(c) Output characteristics of FSD n-TFTs implanted P_{31}^{+} with $5x10^{13}cm^{-2}$.

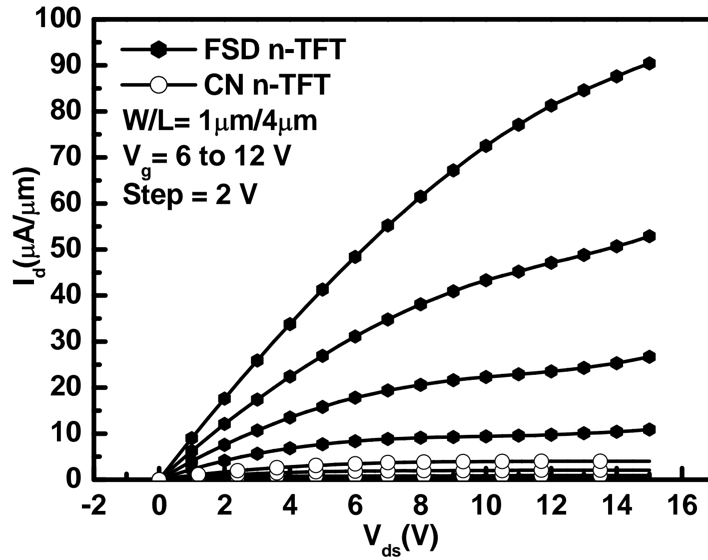


Fig.7-7 Comparison of output characteristics between a FSD and CN n-TFT with W/L=1μm/4μm.

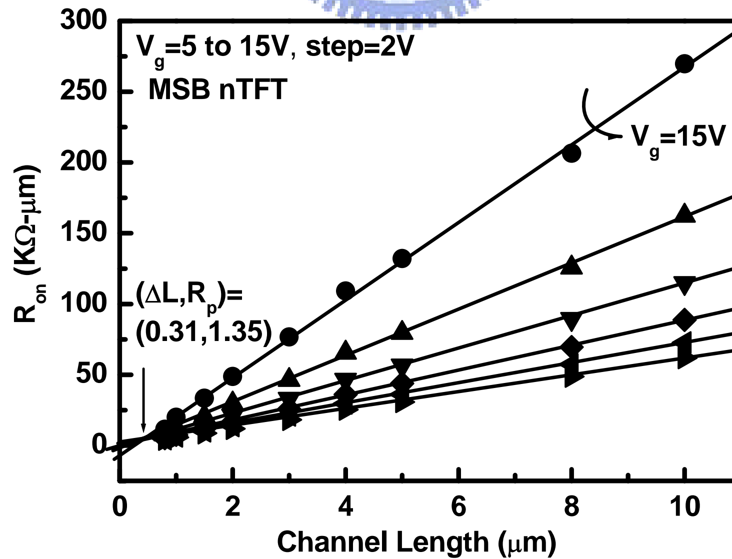


Fig.7-8(a) Parasitic resistance (R_p) of FSD TFT, in the linear region, is also extracted by plotting the width-normalized on-state resistance (R_{on}) versus channel length (L).

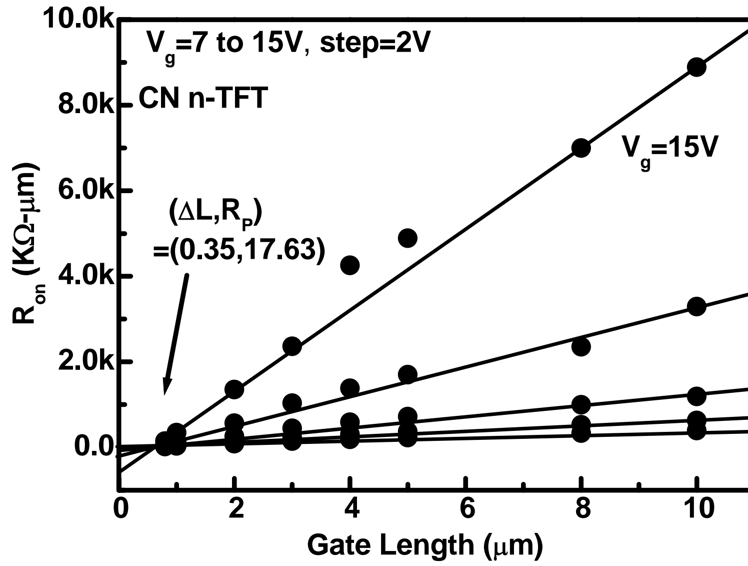


Fig.7-8(b) Parasitic resistance (R_p) of CN n-TFTs, in the linear region, is also extracted by plotting the width-normalized on-state resistance (R_{on}) versus channel length (L).

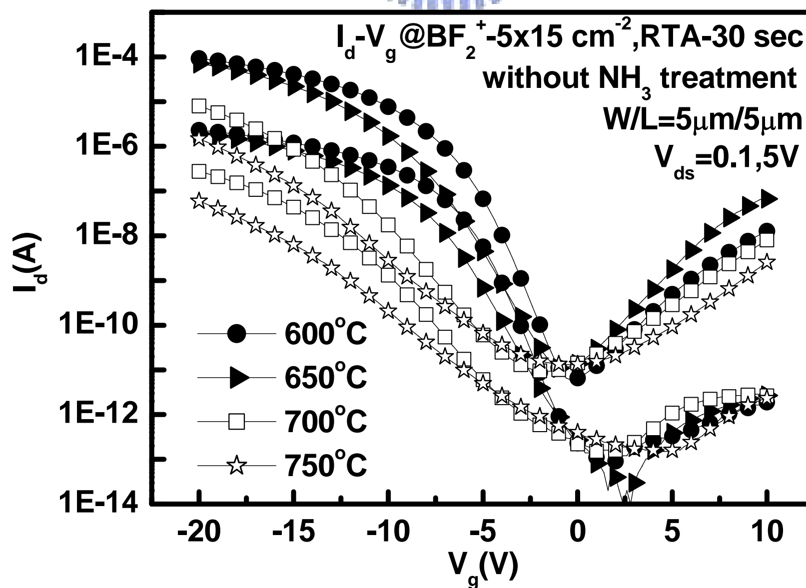


Fig.7-9(a) Transfer characteristics of FSD p-TFTs activated at different temperatures (600, 650, 700, and 750 ^{0}C).

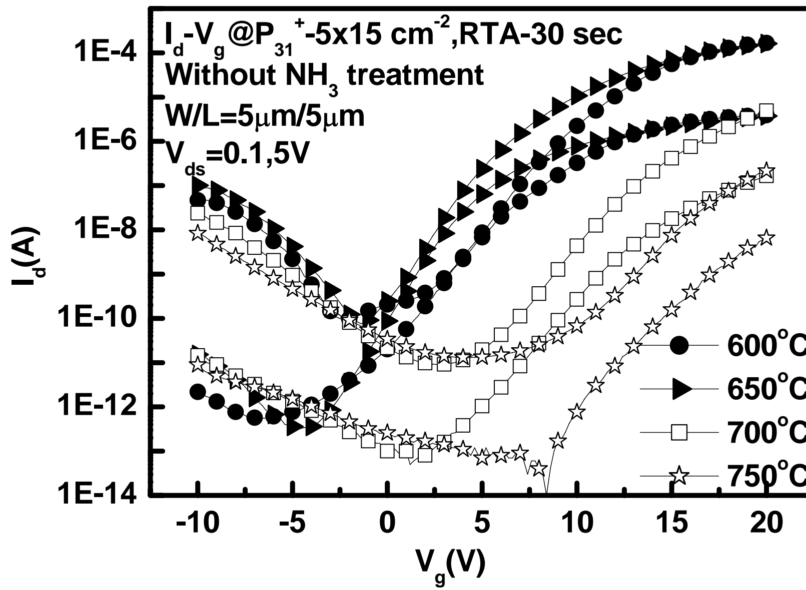


Fig.7-9(b) Transfer characteristics of FSD n-TFTs activated at different temperatures (600, 650, 700, and 750 ^{0}C).

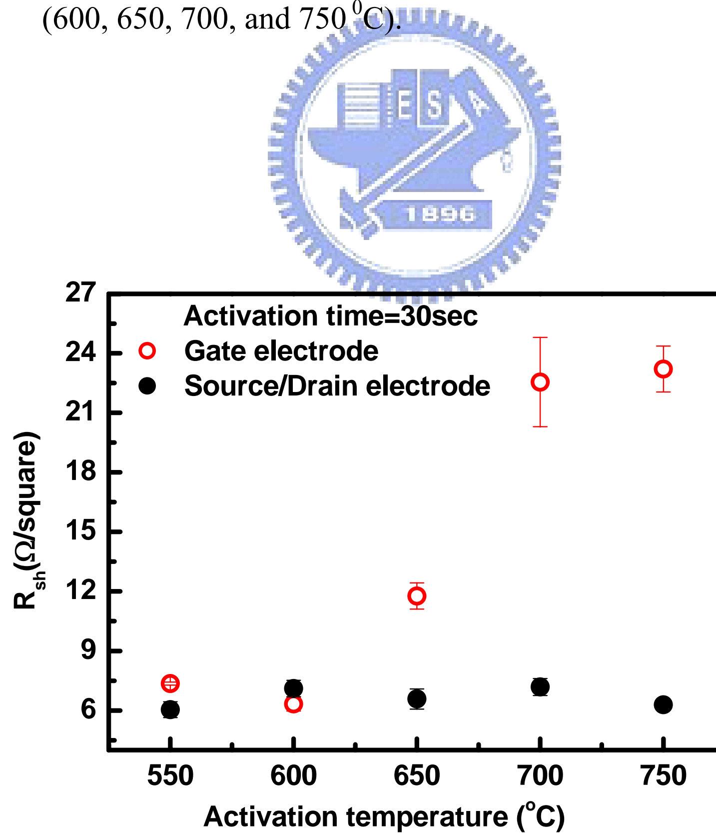


Fig.7-10 Sheet resistance (R_{sh}) comparison between the silicide at S/D and gate electrode activated at different temperature (550, 600, 650, 700, 750 ^{0}C for 30seconds).

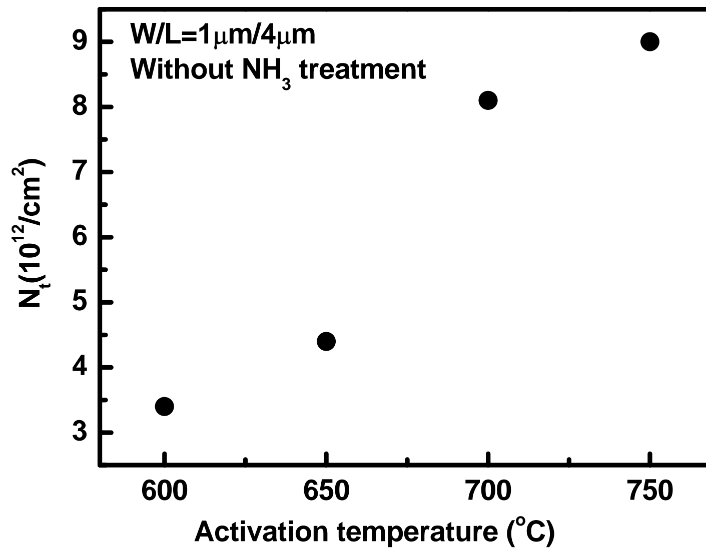
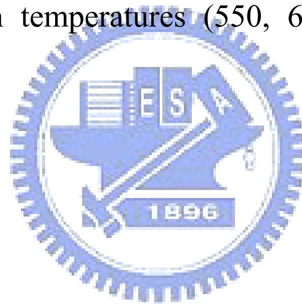


Fig.7-11 Effective trap-state density (N_t) of source/drain and gate electrode with different activation temperatures (550, 600, 650, 700, and 750 ^{0}C for 30seconds).



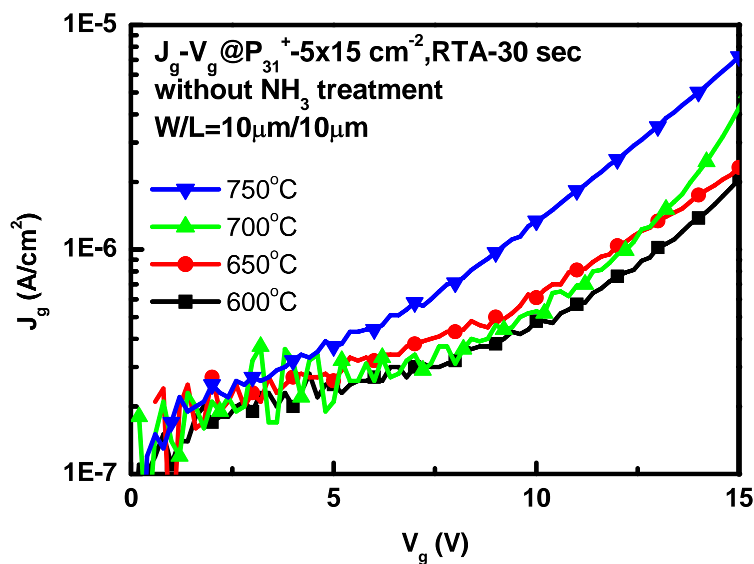
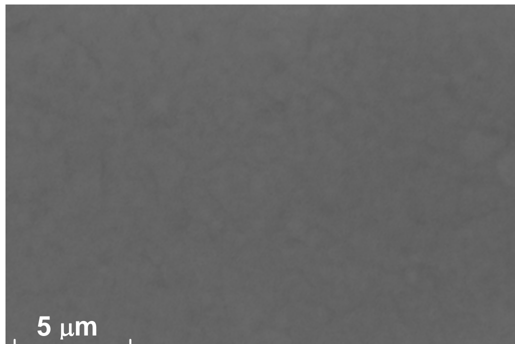
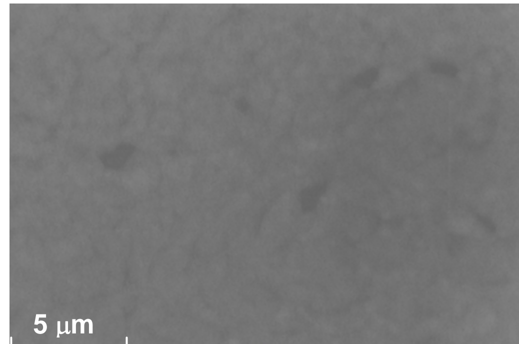


Fig.7-12 J_g-V_g leakage current plots of FSD TFTs activated at different temperatures (600, 650, 700, and 750 ^{0}C).

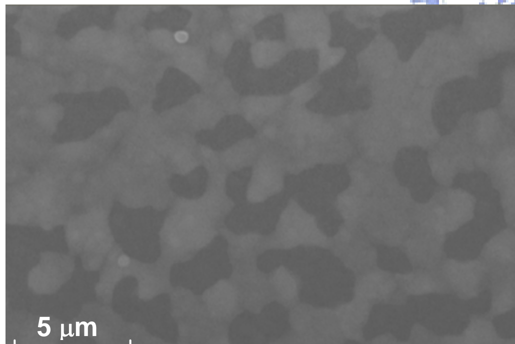
(a) 600 °C



(b) 650 °C



(c) 700 °C



(d) 750 °C

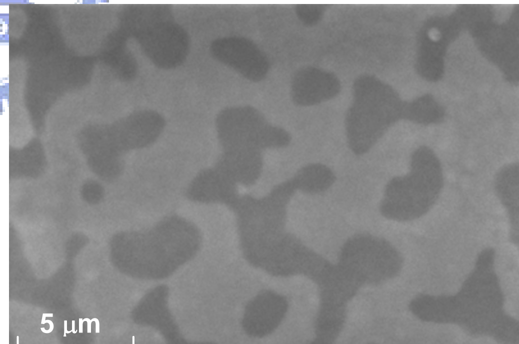


Fig.7-13 SEM images of Ni silicide on the poly-Si/oxide substrate activated at (a) 600°C, (b) 650°C, (c) 700°C, and (d) 750°C for 30sec.

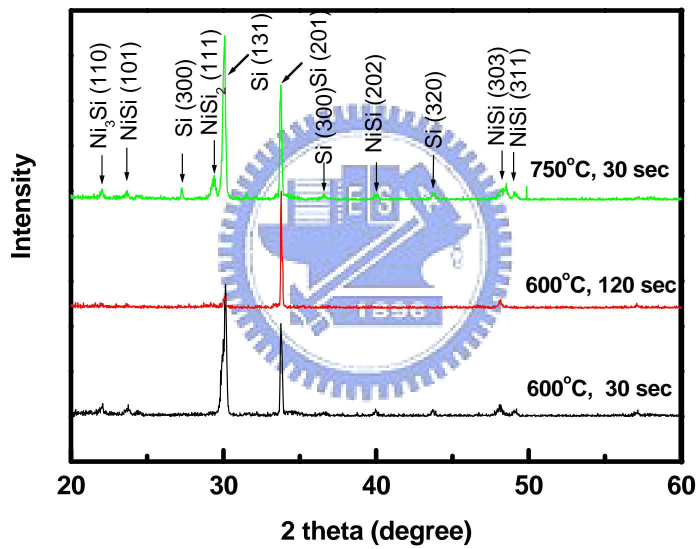
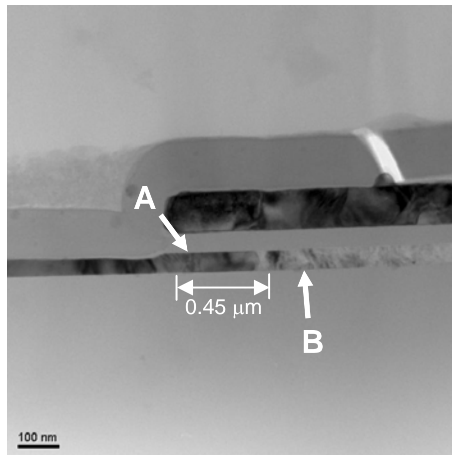
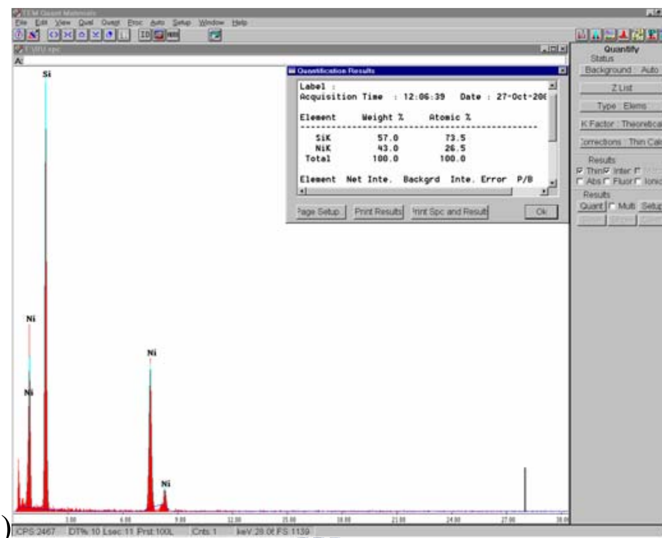


Fig.7-14 X-ray diffraction (XRD) spectra of the silicide on the poly-Si gate electrode after 600°C for 30s, 600°C for 120s, and 750°C for 30s annealing conditions.

(a)



(b)



(c)

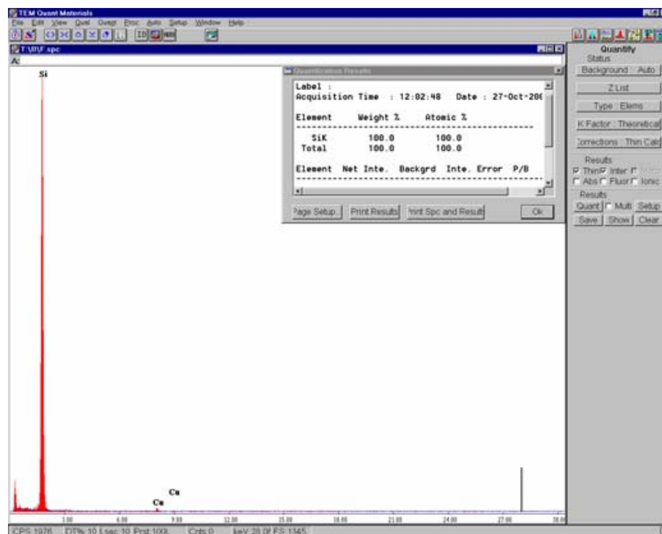
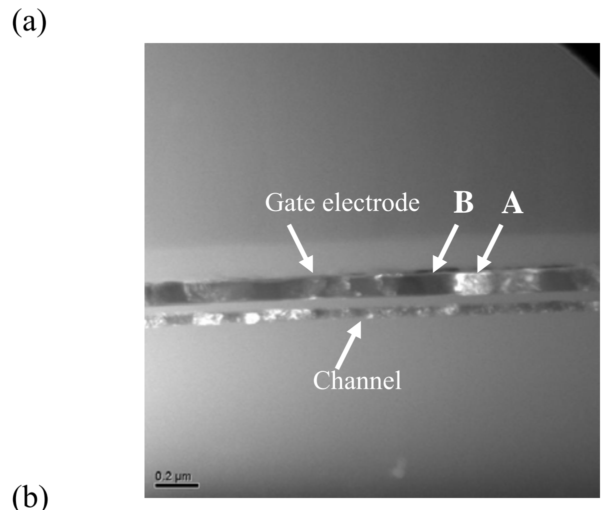
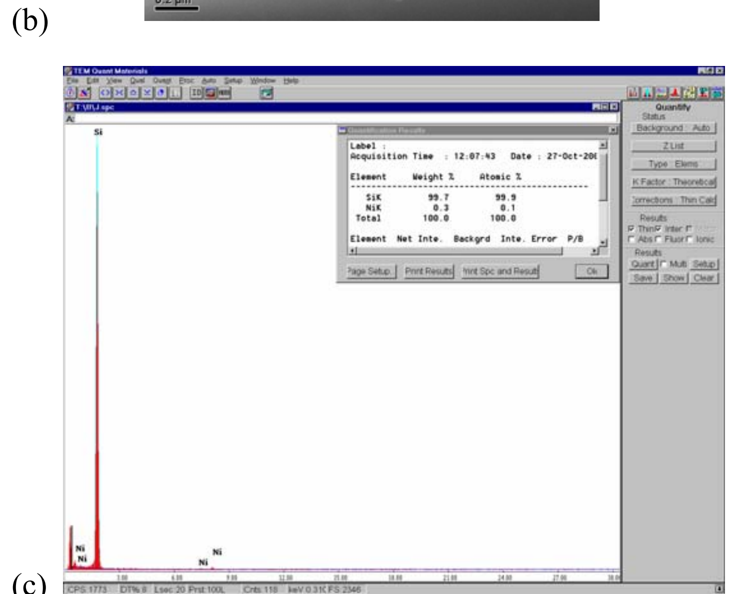


Fig.7-15 (a) Cross-sectional TEM figure of FSD TFTs after 750°C for 30seconds activation. (b) and (c) are the EDX analysis data of point "A" and "B" in (a).

(a)



(b)



(c)

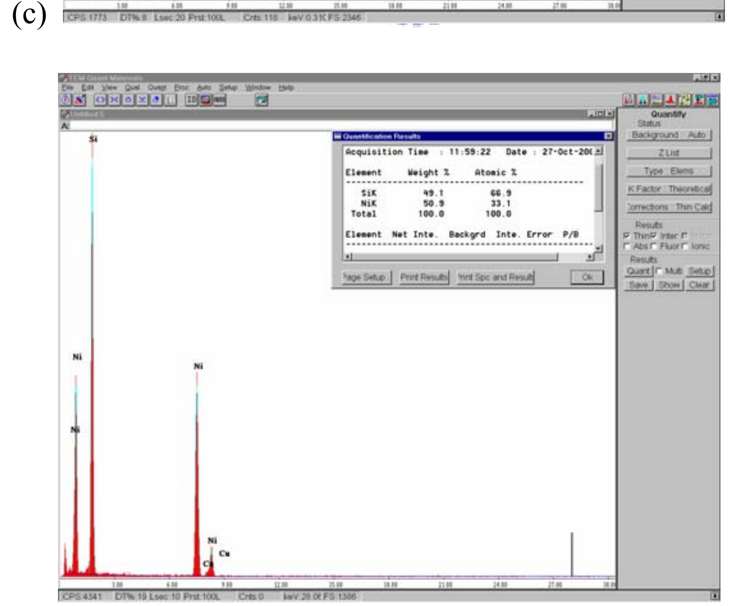


Fig.7-16 (a)Cross-sectional TEM figure of FSD TFTs after 750°C for 30seconds activation. (b) and (c) are the EDX analysis data of point “A” and “B” in (a).

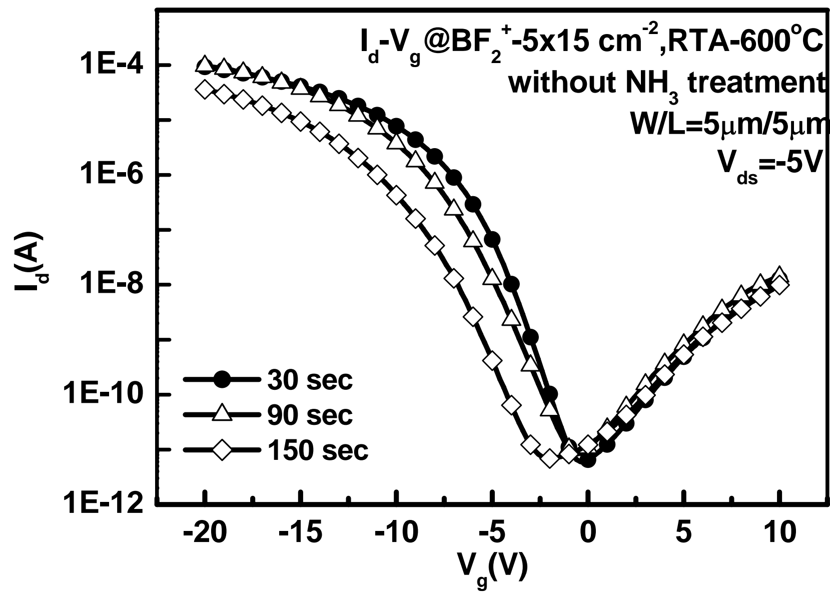


Fig.7-17(a) Transfer characteristics of FSD p-TFTs with different RTA activation time (30, 90, 150 seconds) at 600ºC, respectively.

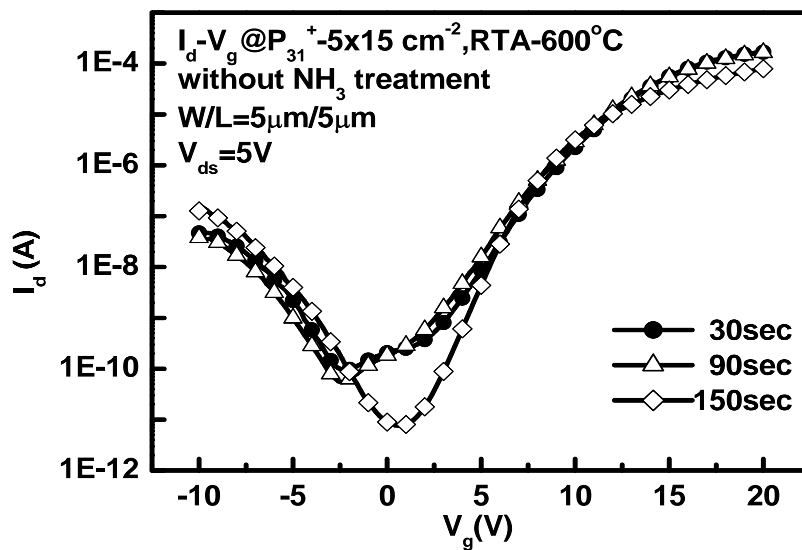


Fig.7-17(b) Transfer characteristics of FSD n-TFTs with different RTA activation time (30, 90, 150 seconds) at 600ºC, respectively.

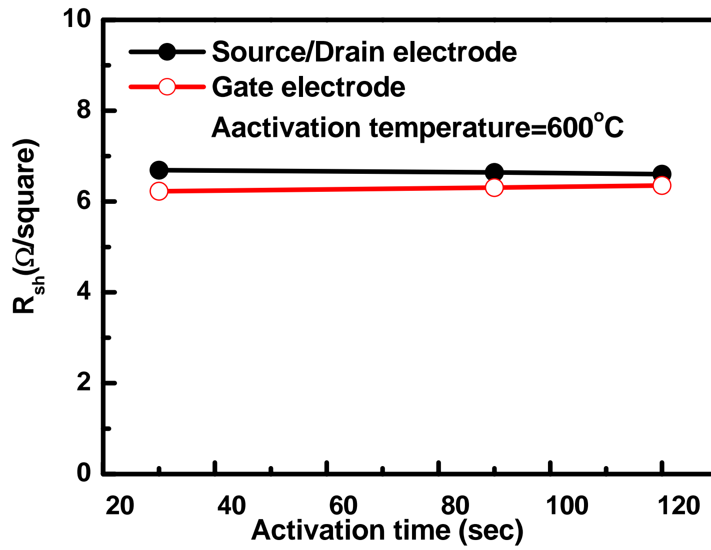


Fig.7-18 Extraction of R_{Sh} of S/D/G electrode after 600 ºC for 30, 90, and 150 sec annealing.

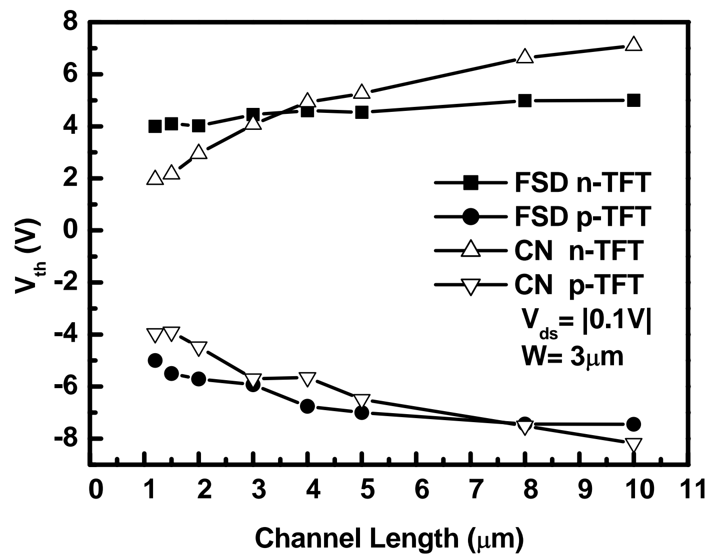


Fig.7-19 V_{th} roll-off characteristics of FSD and CN n- and p-TFTs with W=3μm.

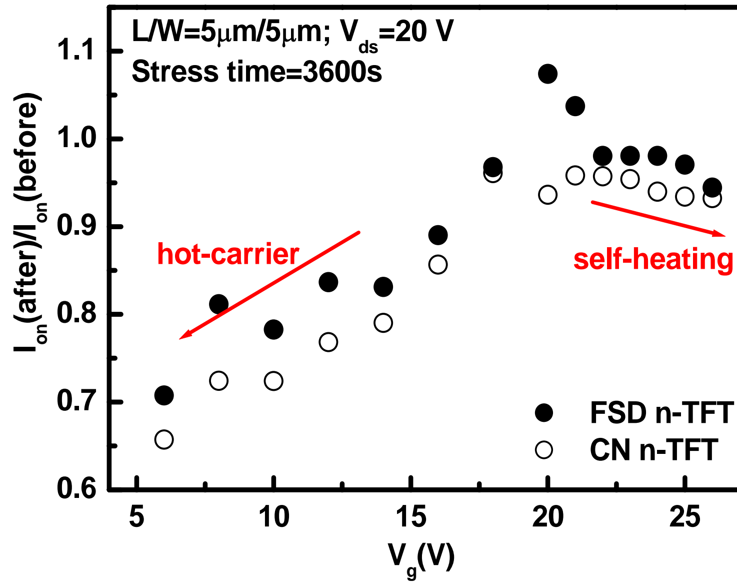


Fig.7-20 Driving current degradation of FSD and CN n-TFTs with the stress gate voltage. The stress conditions are at V_{ds}=20V and various V_g from 6 to 26V with step is 2V.

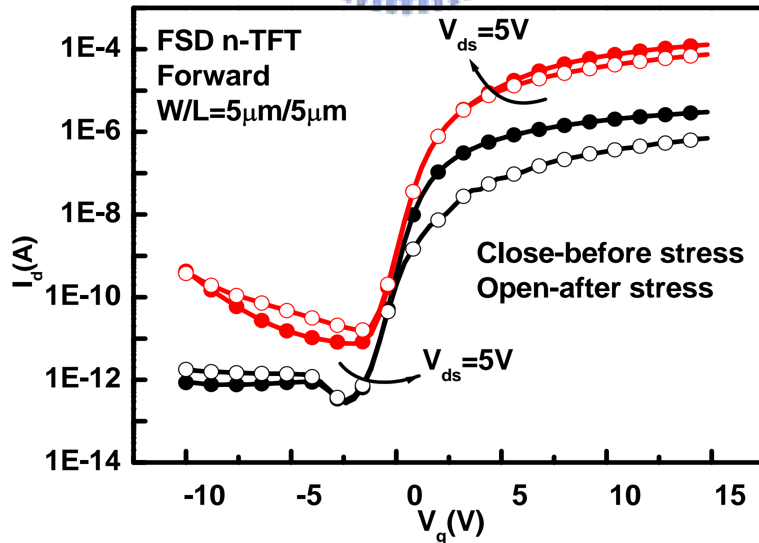


Fig.7-21(a) Forward mode transfer characteristics of FSD n-TFT before and after hot-carrier application. The stressing conditions was V_g=6V and V_{ds}=20V for a stress time of 3600s. The size of TFT W/L=5μm/5μm.

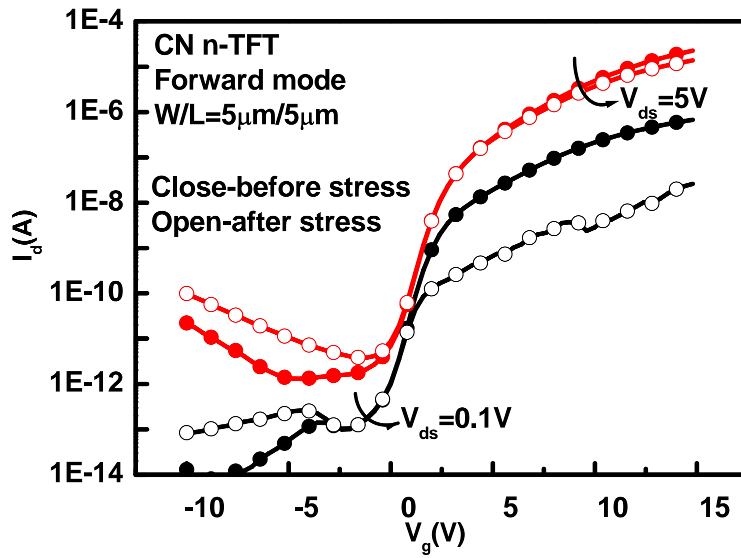


Fig.7-21(b) Forward mode transfer characteristics of CN n-TFTs before and after hot-carrier application. The stressing conditions was V_g=6V and V_{ds}=20V for a stress time of 3600s. The size of TFT W/L=5μm/5μm.

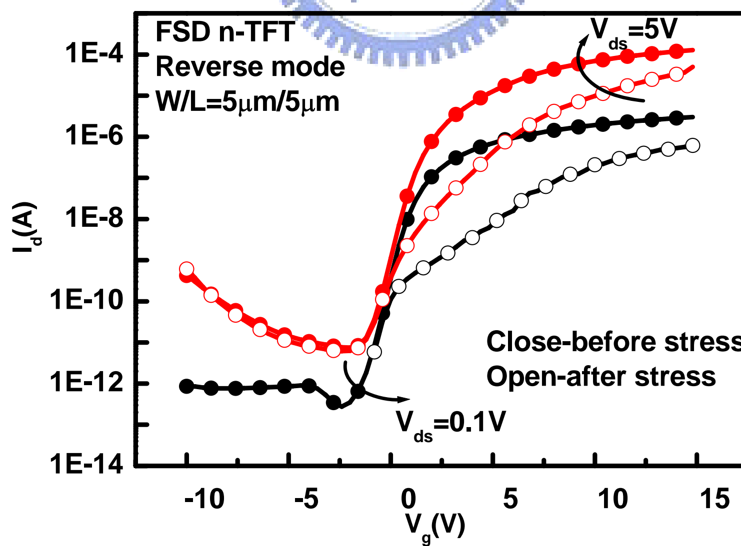


Fig.7-22(a) Reverse mode transfer characteristics of FSD n-TFTs before and after hot-carrier application. The stressing conditions was V^g=6V and V_{ds}=20V for a stress time of 3600s. The size of TFT W/L=5μm/5μm.

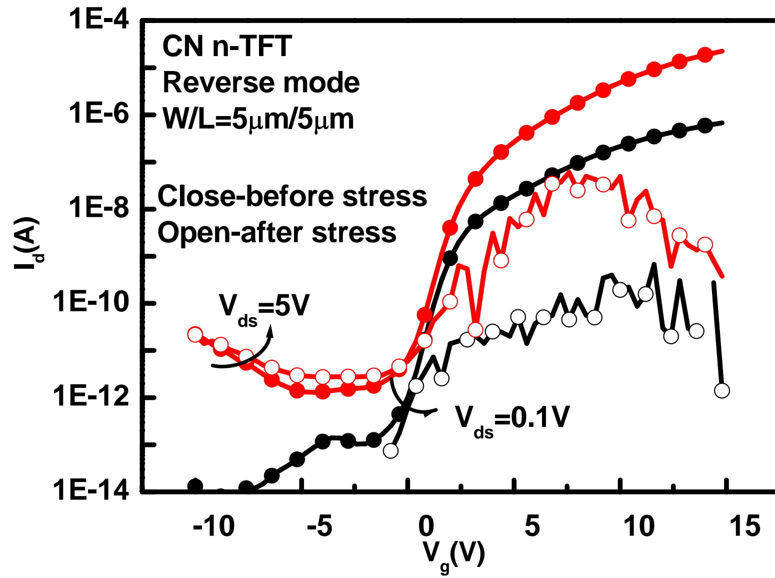


Fig.7-22(b) Reverse mode transfer characteristics of CN n-TFTs before and after hot-carrier application. The stressing conditions was V_g=6V and V_{ds}=20V for a stress time of 3600s. The size of TFT W/L=5μm/5μm.

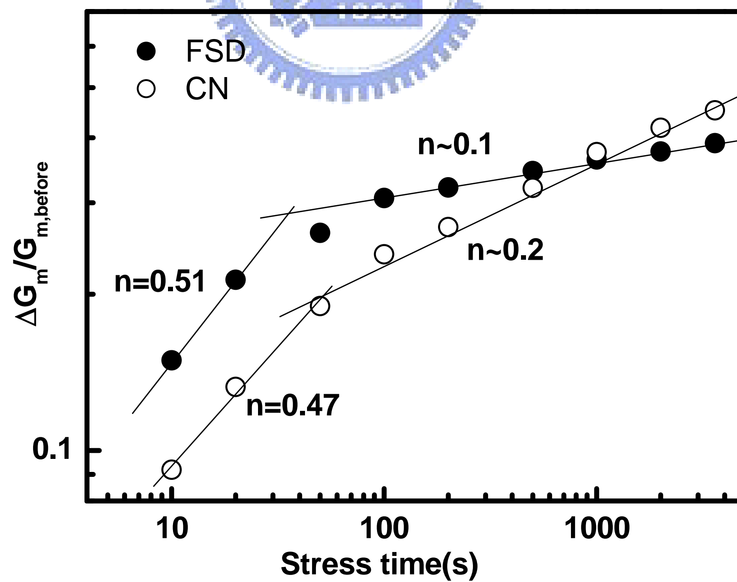


Fig.7-23 Time dependence of forward mode maximum transconductance ($\Delta G_m/G_m$) degradation of FSD and CN n-TFTs after various hot-carrier stressing time. The stressing conditions was V_g=6V and V_{ds}=20V for a stress time of 3600s. The size of TFTs W/L=5μm/5μm.

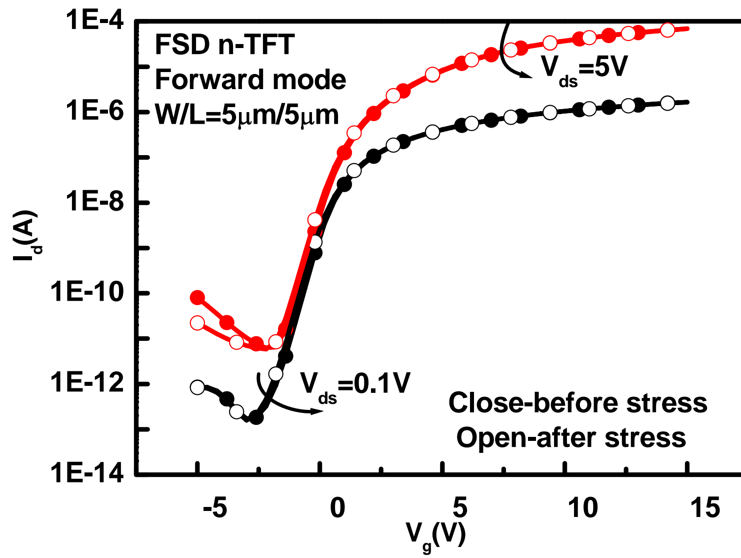
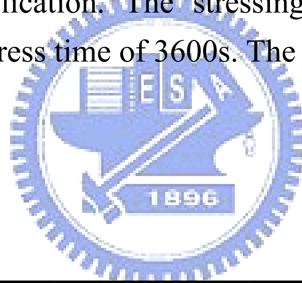


Fig.7-24(a) Forward mode transfer characteristics of FSD n-TFTs before and after self-heating application. The stressing conditions was V_g=20V and V_{ds}=20V for a stress time of 3600s. The size of TFT W/L=5μm/5μm.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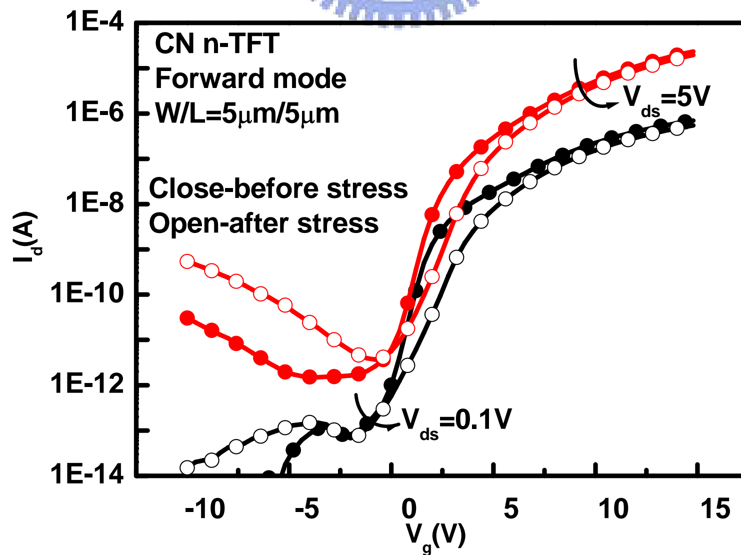


Fig.7-24(b) Forward mode transfer characteristics of CN n-TFTs before and after self-heating application. The stressing conditions was V_g=20V and V_{ds}=20V for a stress time of 3600s. The size of TFT W/L=5μm/5μm.

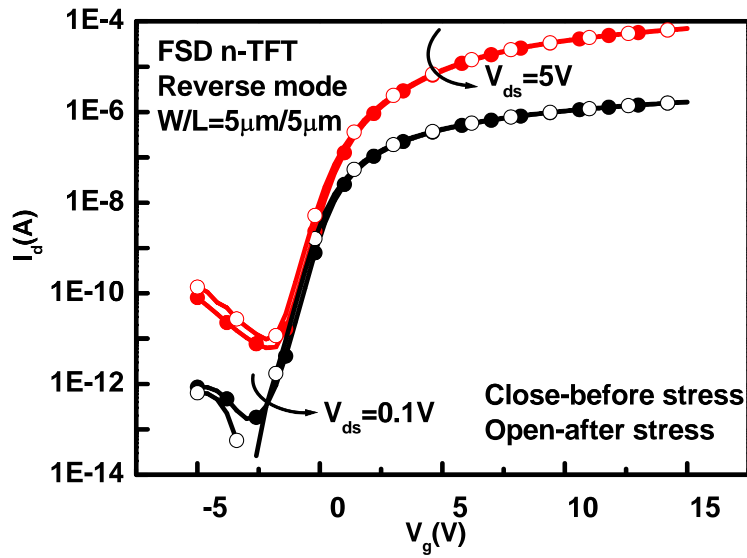
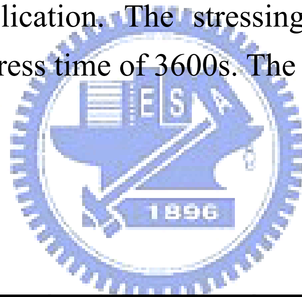


Fig.7-25(a) Reverse mode transfer characteristics of FSD n-TFTs before and after self-heating application. The stressing conditions was V_g=20V and V_{ds}=20V for a stress time of 3600s. The size of TFT W/L=5μm/5μm.



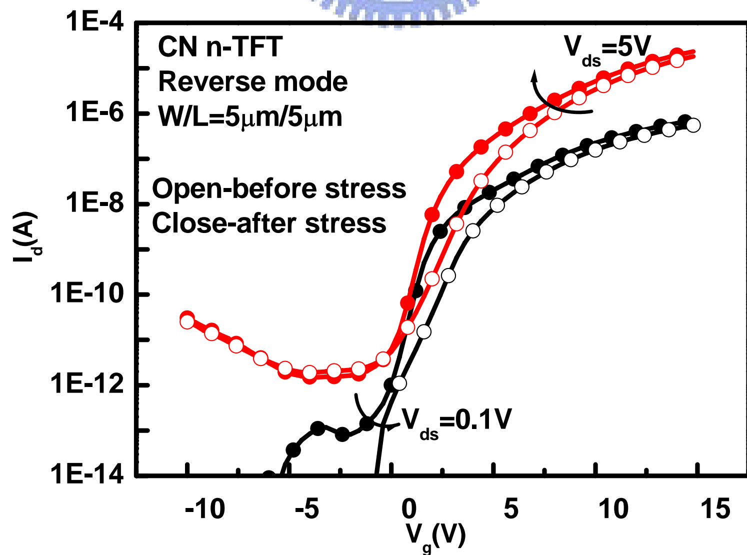


Fig.7-25(b) Reverse mode transfer characteristics of CN n-TFTs before and after self-heating application. The stressing conditions was V_g=20V and V_{ds}=20V for a stress time of 3600s. The size of TFT W/L=5μm/5μm.

Chapter 8

Fabrication and Characteristics of poly-Si TFTs with High-κ Gate Dielectric

8-1 Introduction

Low-temperature poly-Si (LTPS) thin-film transistors (TFTs) have been used as pixel and driving ICs in active-matrix liquid crystal displays (AMLCDs) [8-1]. Recently, to realize system-on-panel (SOP), integrating driving ICs on the glass substrate are required [8-2]. However, it is a challenge to develop high-performance TFTs for both pixel TFTs and driving circuits [8-3]. To drive the liquid crystal, pixel TFTs operate at high voltages with low gate-leakage currents. In contrast, high-speed display driving circuits require TFTs to operate at low voltages and high driving currents, with a low threshold voltage, and a small sub-threshold slope. To satisfy the high driving current, low threshold voltage, superior subthreshold characteristics requirement of driving and pixel TFTs, not only the reduction of S/D parasitic resistance but also the enhancement of gate controllability is suggested. In chapter 7, the FSD technique has been demonstrated to effectively reduce the parasitic resistance (R_p) of TFTs. In this chapter, the gate dielectric engineering of poly-Si TFTs is also studied. In the conventional CMOS scaling theory, thinner gate oxide is used to increase the driving current, which is also valid for TFTs. Unfortunately, for conventional gate dielectrics (i.e. SiO_2 or Si_3N_4), a thinner gate dielectric may induce higher gate leakage current and degrade the TFT characteristics significantly [8-4]. In the previous studies, to preserve the physical

gate dielectric thickness while increasing the gate capacitance density and improving the mobile carrier density in channel region, several new high-κ gate dielectrics materials such as Al_2O_3 and Ta_2O_5 were suggested [8-5]-[8-6]. However, the Al_2O_3 κ value of 9-10 is not high enough and the improvement of device performance is not apparent [8-7]. On the other hand, due to narrow bandgap, it is necessary to use a thick Ta_2O_5 as gate dielectric in TFTs to reduce the gate leakage current [8-8]. Therefore, the increase of gate capacitance density is limited. Recently, the hafnium dioxide (HfO_2) becomes a candidate of future high-κ gate dielectric material in MOSFET due to its high κ value (15~25), wide bandgap, acceptable band alignment, and superior thermal stability with poly-Si [8-9]-[8-10].

In this chapter, we integrated a high-κ HfO_2 gate dielectric layer with TFTs for the first time. First of this chapter, the detail process of the proposed HfO_2 TFTs will be described. Second, a short time NH_3 plasma treatment is also suggested to improve the characteristics of HfO_2 TFTs. And then, the superior I-V characteristics including the C-V, I_d-V_g, I_d-V_{ds}, and I_g-V_g will be presented. Next, the side-channel effect induced by the side-gate at the ultra-narrow width HfO_2 TFTs is also demonstrated. The side-gate enhances the gate-controllability and screens the electric field encroachment from the drain electrode. Finally, the short-channel effect including V_{th} roll off, S.S. degradation, drain-induced-barrier-lowering (DIBL), and kink effect could be suppressed obviously.

8-2 Devices Fabrication Process

The fabrication started by depositing a 50nm amorphous Si (α-Si) layer at 550 °C by a low-pressure chemical vapor deposition (LPCVD) system on Si wafers

capped with a 1 μm thick thermal oxide layer, as shown in Fig.8-1(a). The deposited α-Si layer was then recrystallized by solid phase crystallization (SPC) process at 600 °C for 24 hrs in a N_2 ambient. Next, in order to fabricate narrow width devices to enhance the gate controllability and reduce the influence of grain boundary defects, electron beam lithography (EBL) and reactive ion etching (RIE) were used to pattern the device active islands [8-11]-[8-12]. The narrowest channel width is 0.1 μm. Then, after removing native oxide by dipping in diluted HF solution, a HfO_2 thin film was deposited in a metal organic chemical vapor deposition (MOCVD) system at 400 °C as gate dielectric. Oxygen and Argon were used as reactant and transmission gases with flow rates of 1000 and 200 sccm, respectively. The total pressure in the chamber is fixed at 5 mbar and the injection frequency is 3 Hz. Another 200 nm α-Si layer was deposited at 550 °C in a LPCVD system and then was patterned to form gate electrode, as shown in Fig.8-1 (b). Because of the thermal budget during the α-Si layer deposition process, the amorphous HfO_2 layer could be crystallized to poly-type structure, and then formed the rough top interface between gate electrode layer and HfO_2 film. Next, a self-aligned phosphorous ion implantation was performed at 60 KeV to a dose of 5×10^{15} cm^{-2} to dope source/drain region and gate electrode, as shown in Fig.8-1 (c). After a 300 nm thick SiO_2 passivation layer was deposited by a plasma enhanced chemical vapor deposition (PECVD) system at 350°C, the contact holes were formed by a 2-step wet etching process, as shown in Fig.8-1(d). First, the 300 nm oxide layer was etched by BOE solutions. Then, to raise the HfO_2/SiO_2 selectivity, the HfO_2 film was etched by an IPA: HF (volume ratio~95:5) mixture [8-13]. Additional annealing for dopants activation was performed at 600°C for 12 hrs in a N_2 ambient. Finally, typical Al metallization completed the fabrication process, as shown in Fig.8-1 (e). In order to enhance the device performance, a NH_3 plasma

treatment at 350°C in a PECVD system, the same as to that in chapter 7, was also performed here. The effect of different exposure time to passivate the defect states was also performed before measurements [8-14]. To comparison, poly-Si TFTs with a 25 and 50 nm tetra-ethoxy-silane (TEOS) SiO_2 deposited by a LPCVD system were also fabricated with the same process flow.

To extract the effective oxide thickness (EOT) of the gate dielectric and the κ value of the HfO_2 dielectric, a simple MOS capacitor structure (n^+ poly-Si/ dielectric/p-substrate) was also fabricated. The substrate doping concentration was $2x10^{15}cm^{-3}$, and poly-gate was doped with P_{31}^+ to a dose of around $5x10^{15}cm^{-2}$. For electrical analysis of the MIS capacitance, a precision impedance meter of model Agilent 4284 was used for C-V measurements. High- frequency C-V measurement was performed at 100 KHz with a small ac signal of V_{rms}=30mV. In general, the bias voltage is swept from inversion mode to accumulation mode. The equivalent oxide thickness (EOT) of gate dielectric was also extracted by the curve-correction method [8-15].

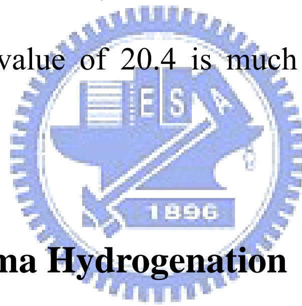
Moreover, the I-V curves measurements, and parameters definition and extraction are the same as that shown in Chapter 7. Finally, for material analysis, cross-sectional Transmission Electron Microscopy (TEM) was employed to extract the exact physical HfO_2 thickness. Detail analysis conditions and results will be discussed in the next sections.

8-3 Results and Discussions

8-3-1 Basic Characteristics of HfO_2

Fig.8-2 (a) and (b) show the schematic drawing of the HfO_2 gate dielectric

TFT and the cross-sectional TEM micrograph of the gate structure, respectively.. It is clear that the physical thickness of HfO_2 film is about 27.7 nm and the thin interfacial layer between the HfO_2/poly-Si active layer of about 2nm is also shown in the inset of Fig.8-2 (b). The interfacial layer is SiO_2-like and can increase the EOT of gate dielectric. The high-frequency C-V curves of MOS capacitors with HfO_2 and SiO_2 gate dielectrics measured at 100 KHz are shown in Fig.8-3. After replacing the SiO_2 dielectric to HfO_2 film, the capacitance at accumulation mode increases from 12.2pF (@ V_g=-15V) to 54pF (@ V_g=-5V) with the same area of 102.5x102.5 μm^2. The EOT, calculated by the CVC program suggested by J. R. Hauser et. al., of the samples decreases from 25nm to 7.314 nm by changing SiO_2 to HfO_2 layer assuming the dielectric constant of the interfacial layer is 3.9 [8-15]. It is the thinnest EOT of TFTs up to now. The extracted κ value of 20.4 is much closed to the values had been reported [8-16]-[8-17].



8-3-2 Effect of NH_3 Plasma Hydrogenation

The NH_3 plasma passivation has been used to promote the electrical properties of poly-Si TFT popularly [8-18]-[8-19]. It was found that the poly-Si TFTs after NH_3 plasma passivation exhibit significantly superior device characteristics and hot-carrier reliability to those with the hydrogen-plasma or without any passivation. The hydrogen passivation of the defect states to terminate the dangling bonds in the grains and at the grain boundaries in the channel region is the major mechanisms. In previous chapter, it has been demonstrated that the characteristics of FSD TFTs can be improved greatly by NH_3 plasma treatment. In this section, for HfO_2 TFTs, the influences of NH_3 plasma treatment were studied carefully through the typical transfer, output, and gate leakage characteristics of the HfO_2 n-TFTs.

The typical transfer, output, and gate leakage characteristics of HfO_2 n-TFTs (L_g=1μm and W_g=0.1μm.) with various NH_3-plasma exposure time from 0 to 6 hrs are displayed in Fig.8-4 (a) to(c). The detailed parameters of HfO_2 nTFTs with various NH_3 plasma exposure time are listed in Table.8-1. It is obvious that similar to the conventional SiO_2 poly-Si TFTs, the NH_3 plasma treatments can effectively improve the performance of the HfO_2 TFTs. Moreover, as the NH_3 plasma exposure time increases, the TFT's performance can be improved continuously, such as I_{on} and G_m, S.S., and V_{th} becomes 8.39μA and 2.4 μS, 0.243 V/Decade, and -0.342V, respectively, for devices after 4 hrs NH_3-plasma treatment. However, as the NH_3 plasma exposure time increases from 2hrs to 6hrs the improvement of V_{th} and S.S. become saturated [8-20]. Furthermore, from the Fig.8-4 (b), as the NH_3 plasma exposure time increases, the defects at grain boundary near the drain-side were passivated, and then the kink-effect induced by the defects near the drain-side is suppressed [8-21].

It is interesting that similar to poly-Si TFTs with the SiO_2 gate dielectric, the I_g reduction was also happened after plasma treatment, as shown in Fig.8-4 (c). For the SiO_2 gate dielectric, the nitrogen ions incorporated into SiO_2 was not occurred; therefore, the interface states fixed by hydrogen ions are the major reason of the I_g reduction. On the other hand, for HfO_2 ones, if the nitrogen was also incorporated with the HfO_2, the capacitance would decay as the NH_3 plasma exposure time increases. However, we didn't find this phenomenon in C-V measurement. Furthermore, by the results of second ions mass spectrometry (SIMS) analysis, the phenomena of nitrogen piled-up at the interface between the gate-dielectric/poly-Si layer wasn't occurred. Therefore, the plausible reason of the gate leakage suppression is the reduction of interface states by the hydrogenization during the NH_3 plasma

treatment [8-22]. To improve the I-V characteristics between HfO_2 and SiO_2 poly-Si TFTs while preserving the throughput of device fabrication, all the I-V comparison between HfO_2 and SiO_2 poly-Si TFTs were taken placed after a 1hr NH_3 plasma treatment.

8-3-3 Basic I-V Characteristics of HfO_2 TFTs

After an effective dielectric constant (~20.4) and EOT (~7.314nm) of HfO_2 being obtained by measuring the capacitance samples, the basic I-V characteristics of TFTs with HfO_2 and SiO_2 dielectric were also extracted. Fig.8-5 (a) shows the typical output characteristics for the HfO_2 and SiO_2 TFTs with the physical gate dielectric thickness ($T_{physical}$) of 27.7nm and 25nm, respectively. The drawn channel length (L_g) and channel width (W_g) are 1 μm and 0.1 μm, respectively. Obviously, the driving current of HfO_2 TFT (about 136 μA/μm) is 5 times higher than that of SiO_2 TFT (about 26.7 μA/μm) at V_{ds}= 6V and V_g=5V. Fig.8-5(b) also depicts the transfer characteristics of HfO_2 and SiO_2 TFTs at V_{ds}=0.1 and 1V. It The measured as well as the extracted devices parameters are summarized in Table8-2. As the gate dielectric of SiO_2 is replaced by HfO_2, V_{th} decreases from 1.2 V to ~0.3 V, S.S. decreases from 0.64 to 0.28 V/Dec, and I_{on}/I_{off} increases from 5.4×10^6 to 9.7×10^6. Although the gate leakage current density of HfO_2 TFTs is almost 1 μA/cm^2 at V_g=5V, it is surprising that this value is still lower than that of SiO_2 TFTs by more than 2 times. The high gate capacitance density resulted from the high-κ gate dielectric could still effectively improve the performance of high-κ TFTs. Moreover, for devices with the same EOT, the drawback of high gate leakage current density of HfO_2 devices could be improved more effectively than that of SiO_2 ones because of the thicker physical thickness of

HfO_2 [8-23]-[8-24]. The EOT of HfO_2 TFTs at on-state is only 7.314 nm, which is ultra-thin for applying on TFTs. The slightly lower effective mobility of HfO_2 TFTs may be due to additional scattering from high-κ dielectric. The off-state current of the HfO_2 TFTs increases more rapid than that of the SiO_2 TFTs as the gate voltage decreases continuously. This phenomenon is explained by the higher electric field near drain side due to thinner EOT of the HfO_2 TFTs. It could be relaxed by LDD or GOLDD structures [8-25]-[8-26].

8-3-4 Short Channel Effect

To examine the short channel effect of TFTs with different gate dielectrics, the threshold voltages (V_{th}) roll-off of HfO_2 and SiO_2 TFTs with W_g=1μm are compared in Fig.8-6. For poly-Si TFTs, the threshold voltage roll-off phenomena is dominated by the decreasing of number of grain boundary as the devices scale down [8-27]. For the long channel poly-Si TFTs, the large number of grain boundaries in the channel raises the threshold voltage and degrades effective mobility [8-28]. The HfO_2 TFTs with ultra-thin EOT and large gate capacitance density can speedily fill the trap-states at grain boundary and turn on the devices fast; therefore, not only release the grain boundary effect but also lower the threshold voltage effectively. Therefore, for poly-Si TFTs with L_g=10 μm, the V_{th} would decreases from 7.2V to 2.35V, while the gate dielectric changed from 45nm SiO_2 to 27.7 nm HfO_2. Moreover, the V_{th} roll-off from L_g=10 μm to 1μm would also relax from 3.3V to 2.78V as the gate dielectric is changed from 25nm SiO_2 to 27.7nm HfO_2.

8-3-5 Narrow Width Effect

Although the HfO_2 TFT has several advantages on I-V characteristics such as superior V_{th} controllability, high I_{on}/I_{off} current ratio, and excellent subthreshold swing, anomalous leakage current at the off-state still limits the application of poly-Si TFTs as switching devices. The dominant mechanism by which the leakage current in poly-Si TFTs is induced involves the field emission of carriers in grain boundary traps, due to the high electric field near the drain junction [8-29]. These grain-boundary not only affect the off-state leakage current, but also degrade the other electrical characteristics including V_{th}, S.S. G_m, I_{on}, and reliability, especially when the device dimension is scaled down [8-30]-[8-31]. Therefore, reducing the number of polysilicon grain-boundary defects in the channel region of TFTs will drastically enhance the performance of poly-Si TFTs. Several studies have reported that scaling the channel width down could effectively reduce the grain-boundary defects in channel. Recently, Y.-C. Wu et al., also suggested that, at on-state, the narrow-width poly-Si TFTs would turn on steeply by the side-channel induced by the side-gate voltage [8-32] And then, the short channel effect in the narrow width TFTs was also relaxed. Moreover, at off-state, the narrow-channel was also effectively shielded by the side-gate from the encroachment of electrical field from the drain-side, and then the leakage current at off-state could also be suppressed indistinctly. However, because of the thick gate dielectric applied to the narrow width poly-Si TFTs to avoid the gate leakage problem, the I-V characteristics of poly-Si TFTs could not be raised more. Here, using HfO_2 as gate dielectric, the gate controllability was enhanced; therefore, the advantages of narrow width were also enhanced as could as possible. Fig.8-7 shows the typical transfer characteristics of HfO_2 TFTs with a fixed L_g=1μm and three different channel width (W_g) of 1μm, 0.3μm to 0.1μm. As the channel width decreases from 1μm to 0.1μm, the device characteristics such as the I_{on} (increases

from 1.23 μA/μm to 3.35 μA/μm), the S.S. (decreases from 0.542 to 0.373 V/Decade), the G_m (increases from 0.443 to 0.711 μS/μm),and the DIBL (decreases from 0.542V to 0.4V) are all improved obviously. Fig.8-8 (a)-(c) also show the characteristics of HfO_2 TFTs with L_g=1μm with various W_g. It is clear that as the W_g decreases from 10μm to 0.1μm, the I_{off} decreases obviously from 900 pA/μm to 9 pA/μm, and the I_{on} increases from 10μA/μm to almost 40 μA/μm. Moreover, the G_m and S.S. were also enhanced as the W_g becomes narrow. As W_g is shirked to 0.1um, the S.S. could be reduced to almost 0.3 V/Dec. Both the side-gate effect and the grain-boundary defects reduction contribute to these phenomena. More importantly, as shown in Fig.8-8(c), the V_{th} roll-off due to the L_g scaled-down was also relaxed. In poly-Si TFTs, the V_{th} roll-off could be attributed to the electrical field encroachment from the drain side through the buried oxide. For the narrow-width TFTs, at off-state, the electrical field from drain side could be shielded by the side-gate. And therefore, not only I_{off} and S.S. characteristics are enhanced; the V_{th} roll-off is also suppressed.

8-4 Conclusions

High performance TFTs with HfO_2 as gate dielectric which provides thin EOT and high gate capacitance density are demonstrated for the first time. Compared with the TFTs with SiO_2 as gate dielectric, the electrical characteristics including threshold voltage, subthreshold swing, on/off current ratio, carrier mobility, as well as V_{th} roll-off are effectively improved. Moreover, the narrow-width HfO_2 TFTs with superior turn-on and -off characteristics were also demonstrated. It is interesting that the side-gate could generate excess side-channel at on-state and also screen the electric field induced by the drain voltage through the buried oxide at off-state. These

results suggest that narrow-width TFTs with a HfO_2 gate dielectric is a good candidate for the system-on-panel (SOP) applications.

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Table8-1 Device parameters of HfO_2 TFTs with different hydrogen passivation time at V_{ds}=1V.

NH_3 treatment time(hrs)	V_{th} (V) (@I_d=10μA/μm)	G_m	S.S. (V/Dec)	I_{on} (μA)	I_{on}/I_{off} (10^6)
0	1.451	1.73	480.11	2.46	2.27
1	-0.064	2.07	388.13	6.75	7.03
2	-0.25	2.14	284.17	7.86	2.75
4	-0.446	2.37	288.4	8.82	8.8
6	-0.342	2.4	243.2	8.39	1.09

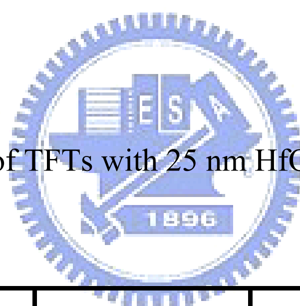


Table8-2 Device parameters of TFTs with 25 nm HfO_2 or SiO_2 as gate dielectric.

Gate dielectric	V_{th} (V)	S.S. (V/Dec)	μ_{FE}(cm^2/V-sec)	I_{on}/I_{off} (@ V_{ds}=1V)
HfO_2 ($T_{physical}$ =27.7 nm) (EOT =7.3 nm)	0.3	0.28	39	9.7×10^6
LPCVD SiO_2 ($T_{physical}$ =25 nm) (EOT =31 nm)	1.2	0.64	50	5.4×10^6

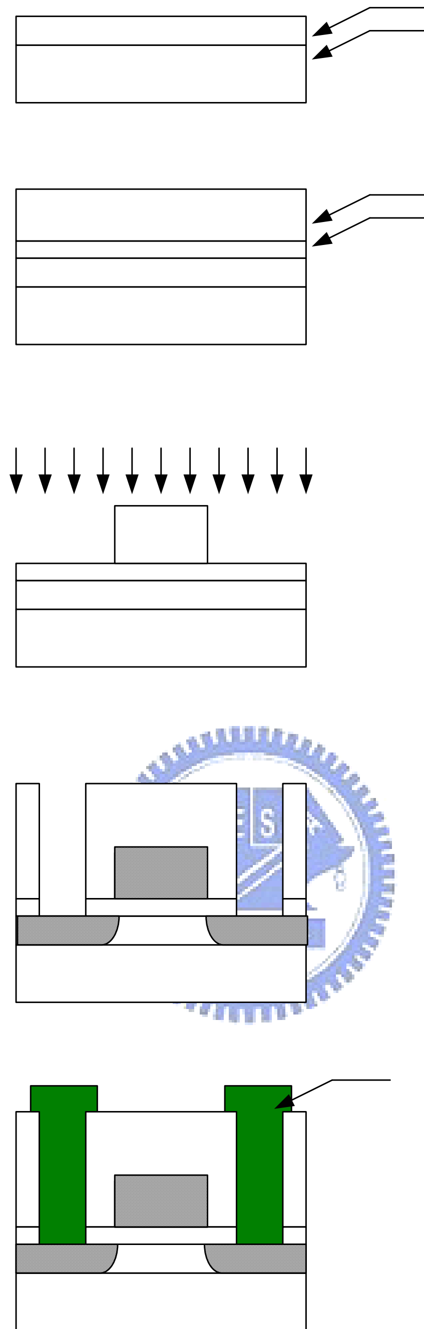
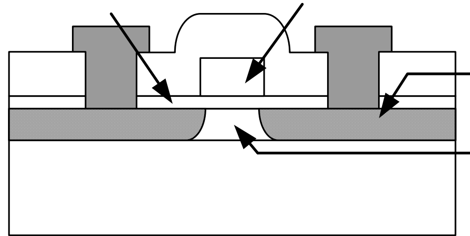


Fig.8-1 Key fabrication process of HfO_2 poly-Si n-TFTs.

(a)



(b)

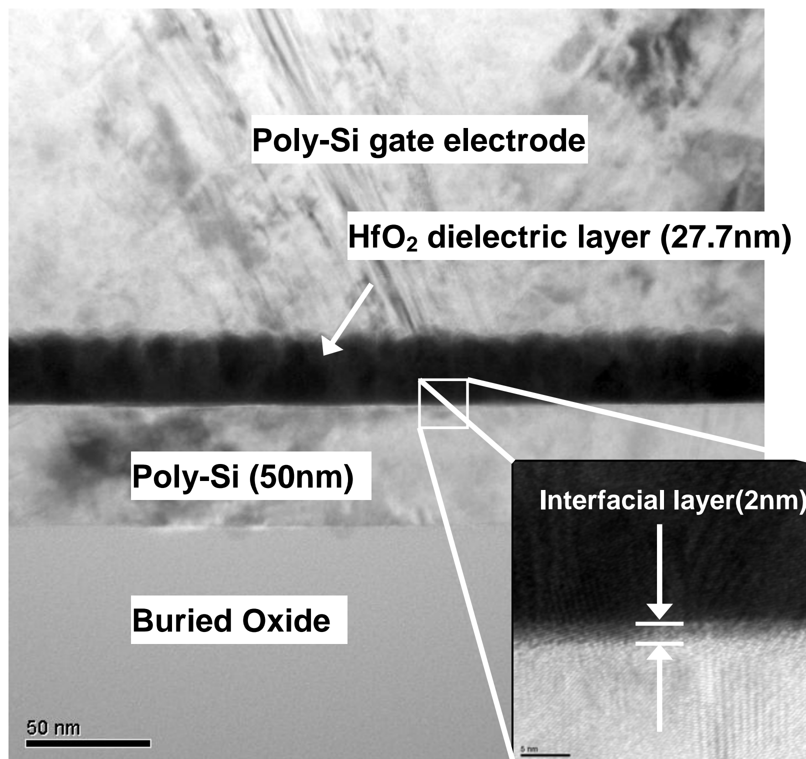


Fig.8-9 (a) Schematic and (b) TEM of HfO_2 poly-Si n-TFTs. The physical thickness of HfO_2 is equal to 27.7nm, and that of the bottom interfacial layer is about 2nm.

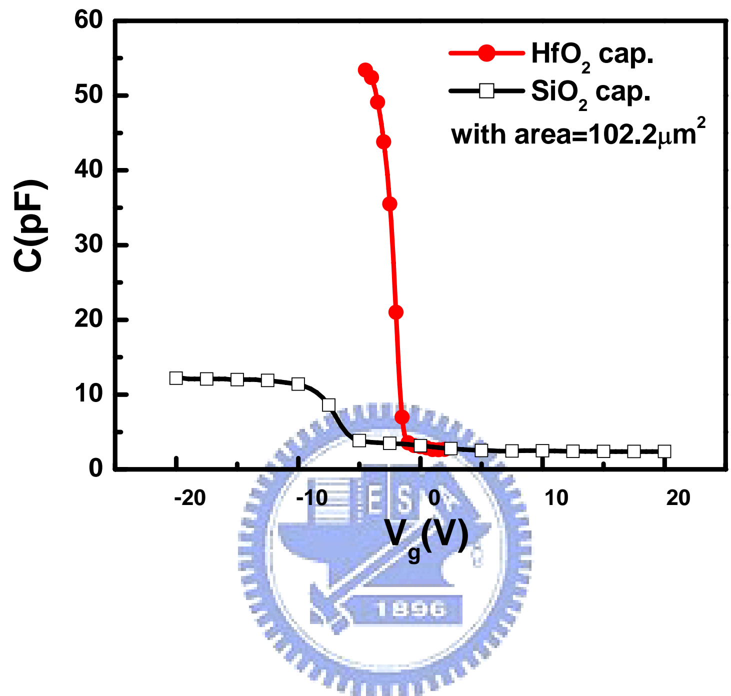


Fig.8-10 Measurement data of high-frequency (100KHz) capacitances of HfO_2 and SiO_2 capacitance.

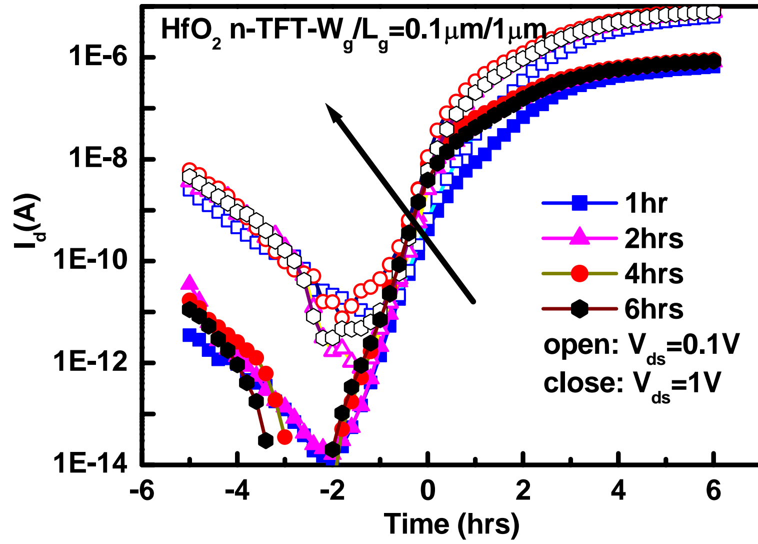


Fig.8-4(a) Transfer characteristics of HfO_2 n-TFTs (L_g=1μm and W_g=0.1μm) with different NH_3 passivation time from 0 to 6 hrs.

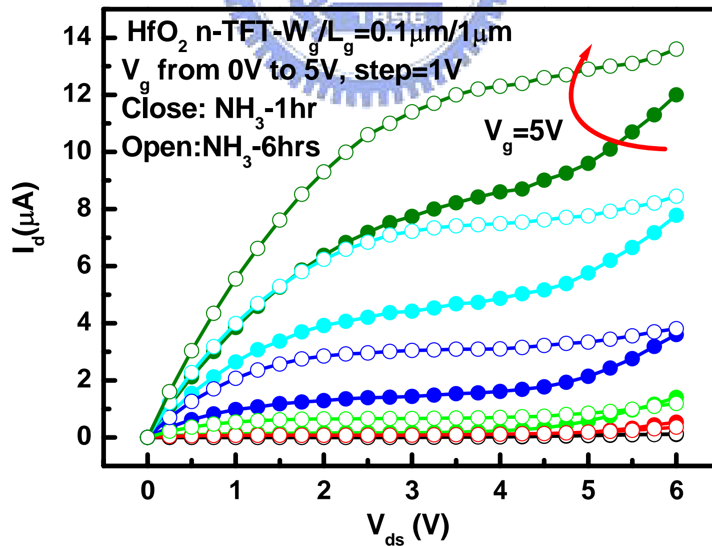


Fig.8-4(b) Output characteristics of HfO_2 n-TFTs (L_g=1μm and W_g=0.1μm) with different NH_3 passivation time from 1 to 6 hrs.

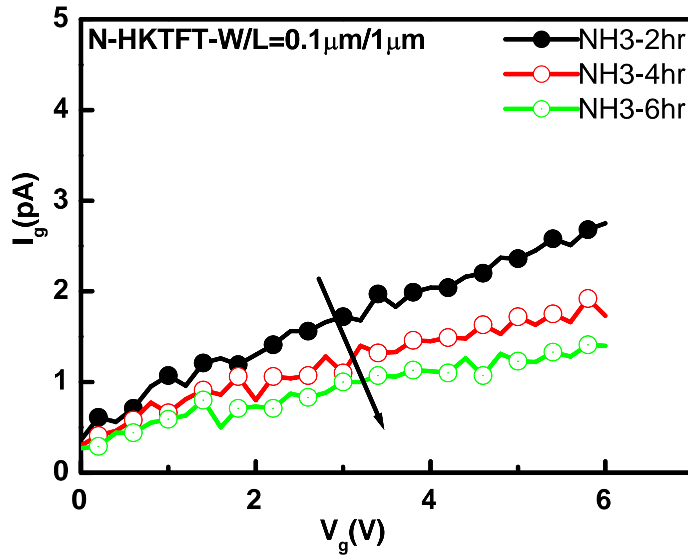


Fig.8-4(c) I_g-V_g characteristics of HfO_2 n-TFTs (L_g=1μm and W_g=0.1μm) with different NH_3 passivation time with 2, 4, and 6 hrs.

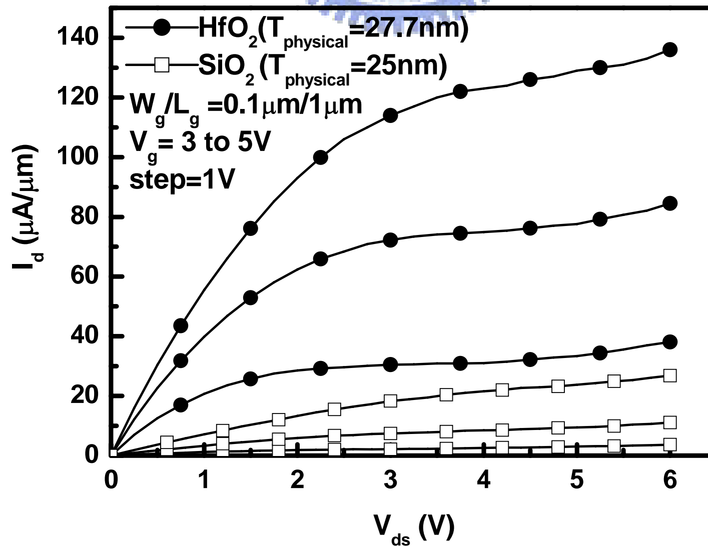


Fig.8-5(a) Output characteristics of HfO_2 and SiO_2 n-TFTs with L_g=1μm and W_g=0.1μm after a 30min NH_3 plasma treatment.

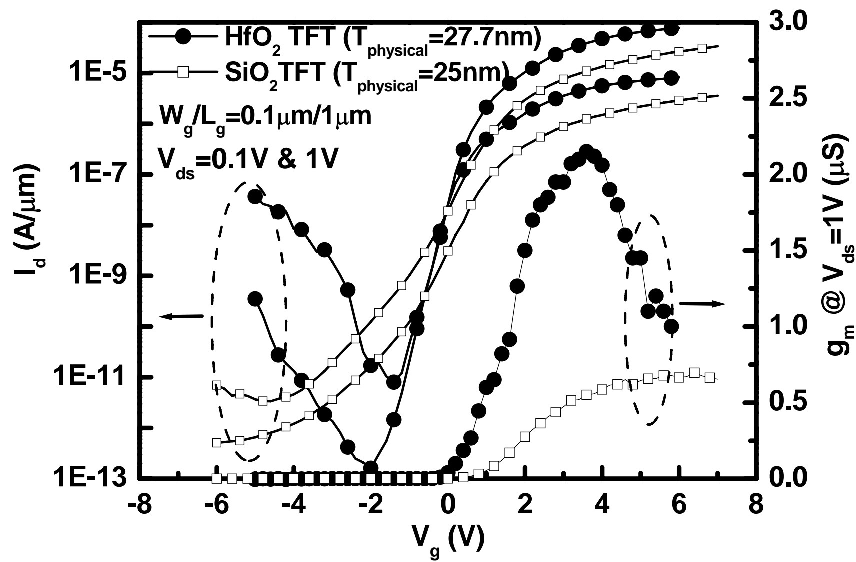


Fig.8-5(b) Transfer characteristics of HfO_2 and SiO_2 n-TFTs with L_g=1mm and W_g=0.1mm after a 30min NH_3 plasma treatment.

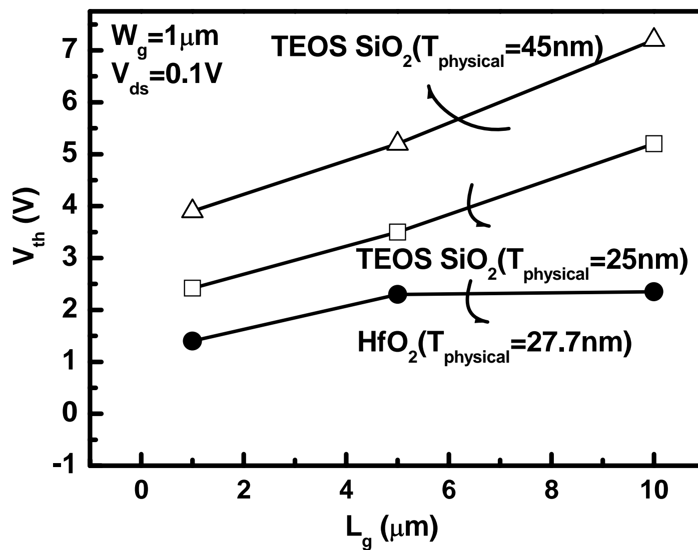


Fig.8-6 V_{th} roll-off phenomena of n-TFTs (W_g=1μm) with HfO_2 ($T_{phys.}$=27.7nm) and SiO_2 ($T_{phys.}$=25nm and 45nm).

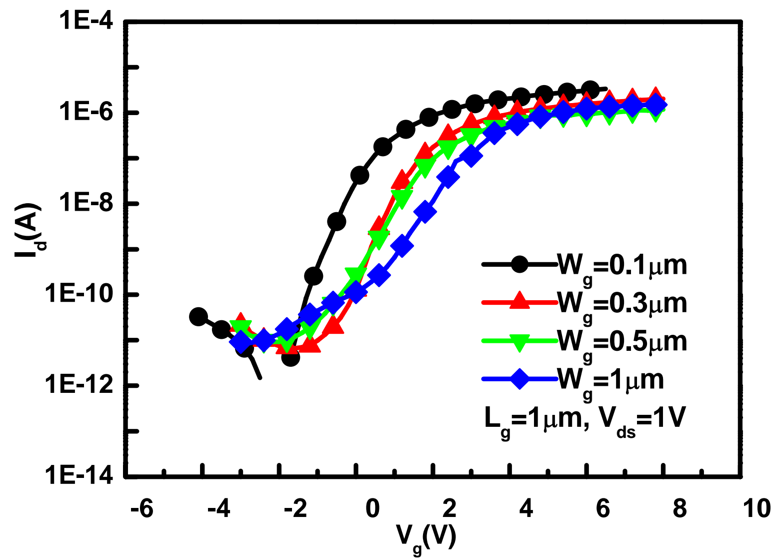


Fig.8-7 Transfer characteristics of HfO_2 n-TFTs with a fixed L_g=1μm and three different channel width (W_g) of 1μm, 0.3μm to 0.1μm was measured at V_{ds}=0.1V.

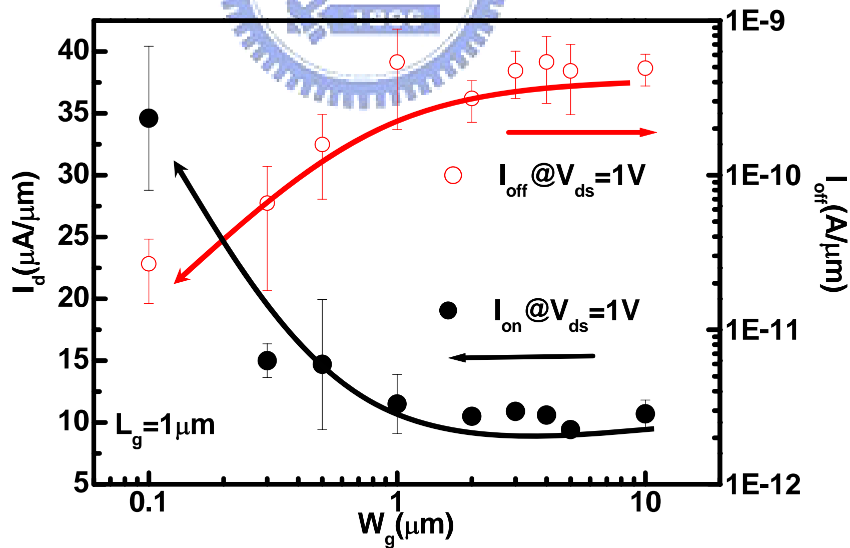


Fig.8-8(a) I_{on} and I_{off} variations of HfO_2 n-TFTs with a fixed L_g=1μm and various channel width.

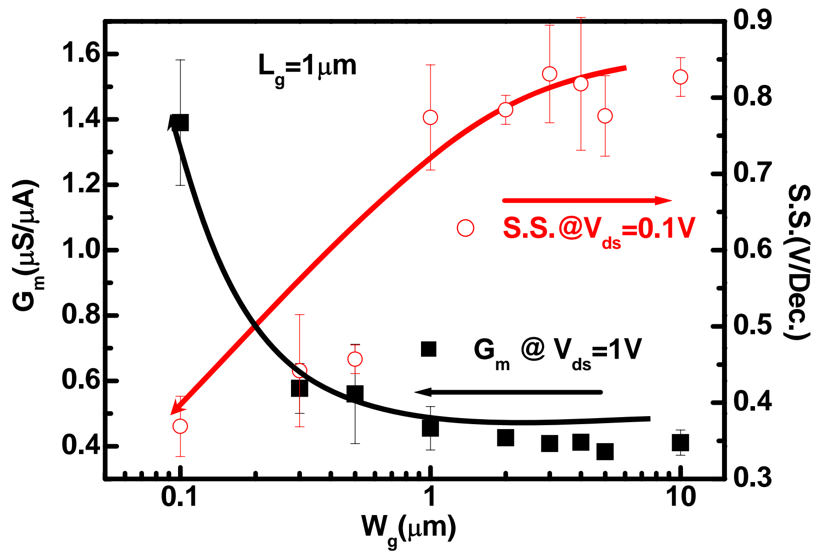


Fig.8-8(b) G_m and S.S. variations of HfO_2 n-TFTs with a fixed L_g=1μm and various channel width.

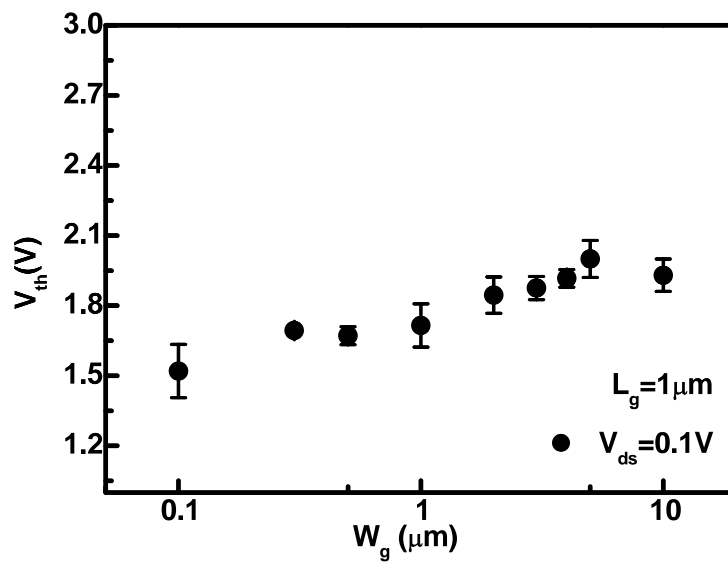


Fig.8-8(c) V_{th} variations of HfO_2 n-TFTs with a fixed L_g=1μm and various channel width.

Chapter 9

Summary, Conclusions, and Future Works

9-1 Summary and Conclusions

In this thesis, first of all, several characteristics of NiSi films were studied in chapter 2. Then, in chapter 3, the novel 25nm MSB TGFETs were demonstrated using ITS technique. Reliability issues of TGFETs including channel-width and back-gate dependence were also illustrated in chapter 4 and chapter 5, respectively. Next, in chapter 6, we also first proposed a novel ITS-FUSI MSB S/D FD-SOI structure with fully-silicided S/D/G electrode and WK tuning by ITS technique. Finally, the novel technique (ITS) and high-κ (HfO_2) material were also separately applied on poly-Si TFTs as S/D electrode and gate dielectric layer for the first time in chapter 7 and chapter 8. Several important results are obtained and summarized as follows:

1. In chapter 2, first of all, we clarified that the NiSi on the SiO_2 substrate have best thermal stability among different substrates including c-Si, poly-Si, α-Si and SiO_2. It could be attributed that on the SiO_2 substrate, no excess Si atoms exist; therefore, Ni silicide film has excellent thermal stability. The R_{sh} of this sample could be maintained constant ~5.2 Ω/□ at 750°C while without any phase transformation or agglomeration analyzed by XRD and SEM. Therefore, the NiSi on SiO_2 substrate is a feasible way to apply on the sub-micron CMOS integration.(Chapter 2)

2. A two-step silicidation way (a 300°C annealing followed by a 600°C RTA annealing) was investigated to suitable control the lateral silicide growth length (D_{EXT}) well to apply on the source/drain region of nano-scale devices. The D_{EXT} was extracted by an unique four terminal sheet resistance. It should be noted that using the two-step annealing method, the D_{EXT} was insensitive to the RTA conditions while maintained at around 40nm even after 60sec 600°C annealing. (Chapter 2).

3. We demonstrated a novel high performance 25 nm MSB TGFETs with several unique features such as fully silicided S/D, ultra-short SDE, defect free S/D junction, and low temperature processing. A two-step Ni-salicide process studied in chapter 2, was used here to completely convert the Si layer at the S/D region to silicide with acceptable lateral silicidation. Next, using an ITS technique, an ultra-short SDE could be performed and the Schottky barrier is modified so that the barrier height and width is suppressed at the on-state and broaden at the off-state, respectively. In addition, the triple gate wrapping around the fin also effectively diminished the Schottky barrier by the gate-fringing effect. Therefore, even with a 4nm thick oxide, the subthreshold swings of 25 nm MSB n- and p-TGFETs are as low as 94 and 83 mV/decade, respectively. The I_{on} of the 25nm MSB n- and p-TGFET at $|V_{ds}|$ = 1 V are about 412.5 μA/μm and 492.5 μA/μm. (By the conventional definition of channel width) (Chapter 3)

4. The geometric effect of HCI and NBTI degradation of TGFETs were both studied carefully. As the TGFETs with narrower Si fin, the better HCI were found. We demonstrated that the equilibrium of electric field in fins induced by the top and the two side-gates relaxed the HCI of the TGFETs by TCAD

simulation. As the fin width decreases, the net electric field in Si fin induced by side-gate is balanced off and shielding the electric field formed by the top-gate. Therefore, the hot carrier's direction was changed from top to side-gate-dielectric by the side-gates. Furthermore, the hot carrier energy was also effective reduced. Therefore, predominately reduces the HC degradation of the devices. Moreover, the roughness of SDE regions was also confirmed to affect the HCI, especially for devices with wide W_f and short L_g. As the result, in the devices with narrowest W_f equaled to 40 nm, the uniform SDE diffused from the bamboo-like silicide fin obviously relieves the HC degradation. (Chapter 4)

5. Besides the HCI, NBTI also affects the reliability of p-TGFETs. On the contrary of HCI in p-TGFETs, the narrower fin devices have worse NBTI resistivity than that with wider fins. Two reasons were suggested to explain this result. First, the higher interface state at (110) side-surface is the major reason dominates the NBTI. For the narrower fin p-TGFETs, the higher area ratio of (110) side-surface to (100) top-surface could raise the trap-state density and then exacerbate the NBTI degradation. The other mechanism could attribute to the more holes rushed to the SiO_2/Si interface owing to the steeper band-bending induced by the electrons accumulation in the center of narrower fin. However, in the proposed devices, the thick oxide may slightly relax the NBTI degradation. The HCI degradation is the main degradation mechanisms for the proposed p-TGFETs. (Chapter 4)

6. In the chapter 5, the V_b impact on the basic I-V characteristics, HCE of n-TGFETs were both presented distinctly. It is also demonstrated that the variation of V_b bias would affect the state of interface between the Si-channel and buried oxide, and then change the performance of front channel TGFETs.

Moreover, HC stressed with the alternation of positive and negative V_b was also used to demonstrate that V_b would attract the hot carriers to the buried oxide and create interface trap-states and fixed oxid-charges in the buried oxide, and then complex the parameters such as the variation of G_m and V_{th}. (Chapter 5)

7. The deep side-gate length (D_{EXT}) and narrow channel width were also apparently found to reduce the V_b effect. Deeper the D_{EXT} would extend the front gate voltage more and effectively screen the electric field induced by V_b and then relaxed the influence of V_b bias effect for I-V and reliability characteristics. For narrow TGFETs, not only the bottom interface area could be reduced but the distance between the D_{EXT} would be also shortened. Therefore, a stronger screening effect existed in the narrow TGFETs than that in the wider ones. (Chapter 5)

8. We also demonstrated that the FD-SOI devices with the FUSI-ITS gate and MSB S/D junctions could easily be fabricated by the ITS technique at the same time. After adjusting the height of S/D/G Si layer, the S/D/G electrodes were fully-silicided at the same time. Using the same ITS technique, not only the MSB junction could be fabricated at S/D sides to enhance the I-V characteristics; at the gate electrode, the WK was also tuned effectively by the dopant piled-up at the interface between the FUSI/SiO_2 layer. Because of the effective adjustment of WK, for n-channel devices, the V_{th} could be shifted from about -0.2V to 0.17V and that of p-channel ones could also be shifted from 0.041V to -0.47V, respectively. Moreover, The I_{on}/I_{off} ratio can also be raised from 34 and 71.4 to 2.83×10^4 and 1.81×10^5 for n- and p-channel devices, respectively. On the other hand, because of the suppression of poly-depletion effect, for n-channel devices, the driving current also raised about 20% at V_g-V_{th}=0.8V. (Chapter 6)

9. We also demonstrated the high performance FSD poly-Si n- and p-TFTs with ultra-low parasitic resistance fully silicide S/D and ultra-short SDE by simple, low-thermal budget ITS process has been proposed. Moreover, we reported that both FSD n- and p-TFTs can be fabricated simultaneously. Because of the NiSi S/D contact region and modified Schottky-barrier junctions, the R_p could be reduced from 7.63 KΩ-μm to 1.35 KΩ-μm as the devices changed from CN TFT to FSD ones. Moreover, the devices parameters including I_{on}, S.S., G_m, and V_{th} roll-off effect are all enhanced. On the other hand, since the ITS process does not damage the active layer and most dopants are fast diffuser in Ni-silicide, annealing at 600ºC for 30 sec is sufficient to produce excellent FSD n- and p-TFTs and maintain the sufficiently low I_{off}. (Chapter 7)

10. The thermal stability and device reliability issues of FSD TFTs were also demonstrated. First, for the thermal stability, as FSD TFT fabricated under 650°C, it has excellent I-V characteristics. On the contrary, as it fabricated above 650°C, the device degraded attributed to the inversion and intermixing of the NiSi and poly-Si at the gate electrode. For the reliability issues, similar to the CN ones, the worst degradation conditions of FSD TFTs happened as the devices stressed at hot-carrier stress conditions. ($V_{ds}>V_g-V_{th}$) It is surprise, although, that the FSD TFTs just activated with 600°C around 30sec by a RTA, also have excellent resistance to shot-carrier stress. (Chapter 7)

11. High performance TFTs with HfO_2 as gate dielectric which provides thin EOT and high gate capacitance density are demonstrated for the first time. Compared with the TFTs with SiO_2 as gate dielectric, the electrical characteristics including threshold voltage, subthreshold swing, on/off current ratio, carrier mobility, as well as V_{th} roll-off are effectively improved. Moreover, the

narrow-width HfO_2 TFTs with superior turn-on and -off characteristics were also demonstrated. It is interesting that the side-gate could generate excess side-channel at on-state and also screen the electric field induced by the drain voltage through the buried oxide at off-state. These results suggest that narrow-width TFTs with a HfO_2 gate dielectric is a good candidate for the system-on-panel (SOP) applications. (Chapter 8)

9-2 Future Works

Followings are the topics suggested for further research.

1. In chapter 2, future works can concentrate on fabricating an ultra-nano silicide line. Moreover, the impact on the electrical characteristics of silicide line attributed by mechanical stress induced by different substrates and spacer materials and process are interesting for future research.
2. In chapter 3, MSB TGFETs, although, has been demonstrated with well controlled SDE region. Nevertheless, the length and doping concentration of SDE are still a mystery. It is attributed to the ultra-small area of SDE; therefore, some methods are required to directly measure it. On the other hand, the source/drain contact resistance is still large owing to the small silicide/Si contact area. To improve it, non-fully silicided S/D structure is a plausible category to increases the driving current.
3. In chapter 3, to further improve the performance of TGFETs, the strain technique can be applied on it. Recently, the effect of embedded-SiGe source/drain, SiNx liner, and memorized SiN_x are popularly researched on bulk, planar, FinFET SOI devices. For TGFETs, with three-gate around the Si fins, it is interesting that the strain-technique can raise the device characteristics more

than other devices. Moreover, the temperature-related strength of stress variation is another interesting issue.

4. In chapter 3, RF devices research is also suggested. For the MSB TGFETs with excellent SDE length control, the capacitance between the gate-electrode over source/drain could be effectively suppressed.

5. In chapter 3, for TGFETs, the properties of side-channel have strong impact on the devices characteristics including I-V, mobility, and reliability. It is also suggested to focus on the topics of improved TGFET layout and process. Changing the devices orientation or adding hydrogen smoothing process are the possible solutions.

6. In chapter 4 and 5, for TGFETs, corner effect is well known to be positive influence of the driving current. Nevertheless, stronger electric field induced by sharp corner may degrade the reliability characteristics. It is very interesting to clarify the corner shape impact on the reliability and suppress it by fabrication process, dimension issues, and back-gate bias.

7. In chapter 6, although the FUSI-MSB n- and p-FD SOI devices have been fabricated by an ITS technique. Continuous scaling to nano-scale is future work. Moreover, the mechanical stress impact on the gate oxide properties and reliability issues induced by the silicide formation on the S/D/G at the same time is another interesting topic, especially for the nano-scale devices.

8. In chapter 7, it is important to improve the thermal stability of FSD TFTs. Using dual material silicide, e.g., Pt, by co-sputtering technique should be investigated in the near future.

9. In chapter 8, for HfO_2 TFTs, the reliability and stability are another interesting issue. In the ultra-HfO_2 film, applied on the bulk nano-CMOS, strong

interface-and dielectric bulk states effect are found on the reliability and stability. Therefore, SiO_2/HfO_2 gate dielectric stack is suggested to apply on CMOS devices. On the TFT, it is also interesting to find the related mechanism and solve it.

10. In chapter 8, for HfO_2 TFTs, to apply on the 3-dimensional circuits, the characteristics of nano-scale poly-Si HfO_2 TFTs should also be suggested. Eventually, the nano-HfO_2 TFT combined with silicide technique is also the plausible structure in the future.