國 立 交 通 大 學

電子工程學系　　電子研究所碩士班

碩 士 論 文

互補金氧半正交相位壓控震盪器

設計與誤差補償技術

Design of CMOS Quadrature VCO with Mismatch Compensation Technique

研 究 生:李漢健　　Han-Jian Lee

指導教授:溫瓌岸 博士　Dr. Kuei-Ann Wen

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中華民國九十六年六月

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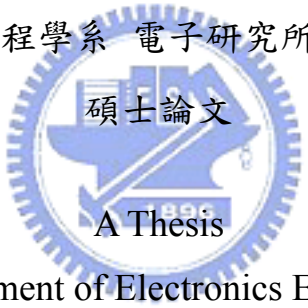

碩士論文

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中文摘要

本論文主要討論正交相位壓控震盪器的相位誤差，提出共模的方式分析電路中的不匹配所造成的相位誤差，並設計一補償電路以減輕電路中的不匹配所造成的相位誤差。藉由共模相位誤差補償電路，相位誤差與鏡像拒斥比各改善了 1.5 度及 4.7 分貝。壓控震盪器的 Verilog-A 模型亦被建立。當以 Verilog-A 模型取代實際電路模擬時，時間可節省至 1/300。

Design of CMOS Quadrature VCO with Mismatch Compensation Technique

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Abstract

This thesis discusses the phase error of QVCO. The phase error of QVCO due to mismatch is analyzed with common-mode model. Efficient compensation circuit is proposed to alleviate the common mode phase error of the QVCO. With the common-mode compensation circuit, the QVCO phase error and image rejection ratio (IRR) are improved about 1.5 degrees and 4.7dB for 2.63GHz carrier frequency, respectively. VCO Behavior model was also built in Verilog-A. Simulation time can be saved by replacing transistor-level circuit with behavioral model (300:1).

誌　　謝

To My Family

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Chapter 1
Introduction

1.1 Motivation

In-phase and quadrature-phase imbalance of RF front-end limits the achievable operating SNR at OFDM receivers [1]. Such I/Q imbalance causes inter-channel interference (ICI) of OFDM and seriously degrades the performance at higher data rate [2]. I/Q imbalance is basically any mismatch between I and Q branches and dominated by the mismatch of quadrature LO signals. There are several ways to generate quadrature phase, such as polyphase filter, double frequency VCO with divide by two circuit and quadrature VCO. As polyphase filter implementation needs large area and double frequency VCO phase noise is poor, quadrature VCO (QVCO) is often used to generate I/Q carrier for the transceiver. However, mismatch of transistors and passive components still affects QVCO phase error.

Figure 1.1 shows the conventional QVCO. In Figure 1.1, if differential outputs of the

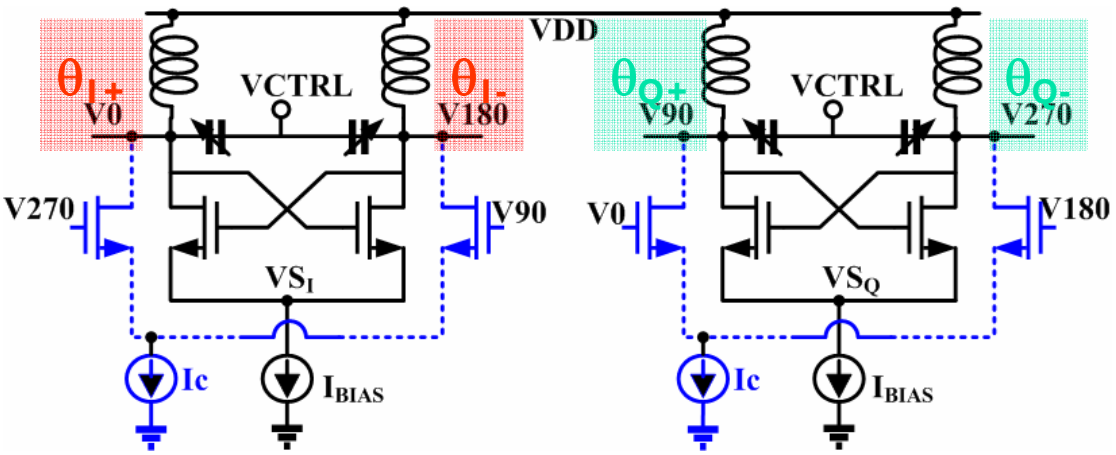


Figure 1. 1 Conventional Quadrature VCO.

QVCO have four phases, θ_{I+}, θ_{I-}, θ_{Q+} and θ_{Q-}, ideally there is 90 degrees phase difference between $\theta_{I+/-}$ and $\theta_{Q+/-}$ at VCO oscillation frequency. As common-mode nodes (VS_I, VS_Q) of each VCO oscillate at the second harmonic of VCO frequency, the phase difference between two VCO common-mode nodes at the second harmonic of VCO frequency can be expressed as $\theta_{shift\_2nd\_freq} = (\theta_{I+} + \theta_{I-})-(\theta_{Q+}+\theta_{Q-})$. If the differential-mode phase error $\Delta\theta$ occurs at VCO oscillation frequency, $\theta_{shift\_2nd\_freq}$ equals to $((\theta_{I+} + \theta_{I-})-(\theta_{Q+}+\theta_{Q-}))+\Delta\theta$. Thus the differential-mode phase error at oscillation frequency is distributed and can be observed at second harmonic frequency in common-mode. So phase error compensation in common-mode can alleviate I/Q phase imbalance and compensation technique might be developed based on common mode analysis.

Although there are several variations of QVCO architecture (conventional, second harmonic coupling, transformer and series coupling stages.), the conventional one shows the basic technique and understanding how the conventional QVCO works

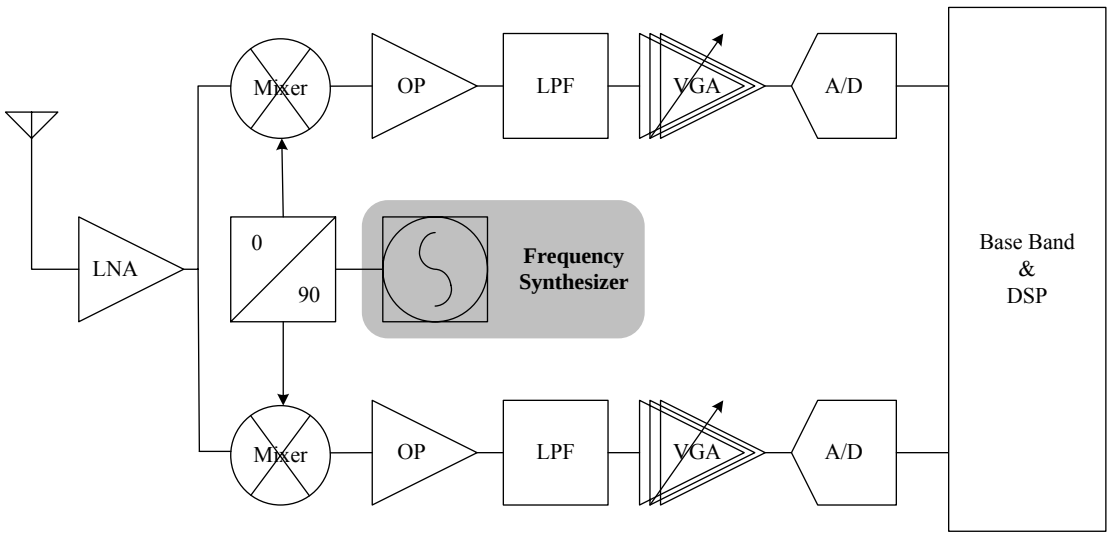


Figure 1. 2 The direct-conversion architecture for WiMAX transceiver

help to analyze and propose other architectures. Figure1.2. illustrates a WiMAX transceiver architecture consisting a direct-conversion transmitter and receiver.

One of the advantages of direct-conversion architecture for receivers (in Figure1.2) is that there is no image problem, and it does not require an image-reject filter. This is because the frequency of the RF signal is exactly equal to the frequency of the LO signal. However direct-conversion receivers have some issues which should be mitigated carefully, such as DC offsets, I/Q mismatch, even-order distortion, and flicker noise. In order to achieve the goal of the RF-SOC, we choose the direct-conversion architecture to design the system.

The frequency synthesizer must provide a clean and stable LO tone. As QVCO is a core circuit in the frequency synthesizer, its phase error and phase noise determine transceiver's I/Q mismatch and EVM. Minimize phase error and phase noise is an issue in proposing the QVCO.

1.2 Design Specifications

1.2.1 Frequency Range

IEEE 802.16e [3] partitions the spectrum from 2 to 6 GHz into 8 groups and employs OFDM in each band to transmit different data rates as different modulation schemes. The band allocation is shown in Figure 1.3. The design is focus on frequency band groups between 2.305GHz and 2.69GHz.

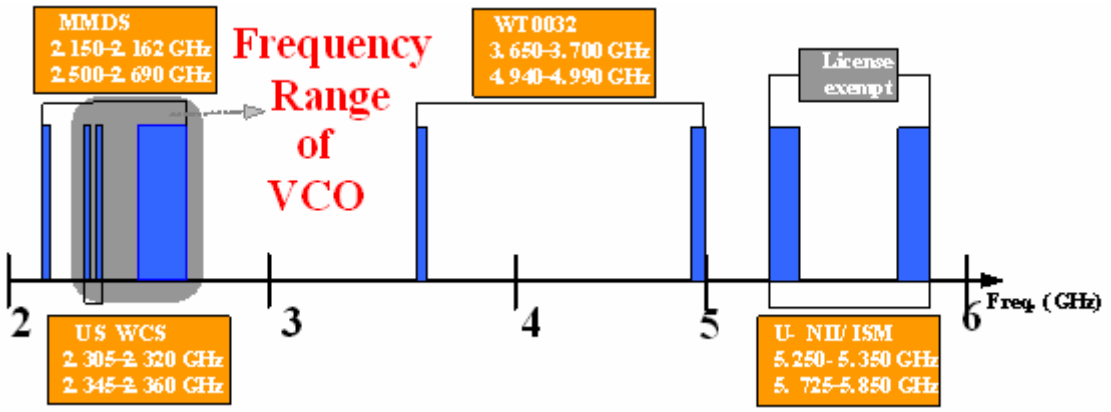


Figure 1. 3 The Multi-Band WiMAX OFDM frequency band plan.

1.2.2 Phase Noise

To derive the phase noise specification of the VCO, consider the following equation [4] [5]:

$$\text{RMS phase error} = \frac{180}{\pi} \cdot \sqrt{2 \cdot \int_0^{\infty} L(f)df} \tag{1.2}$$

$$L(f) = 20\log \frac{(\text{RMSnoise}) \cdot \frac{\pi}{180}}{\sqrt{f_C \cdot (1+10^{p/10}) + 10^{p/10} \cdot 2}} \tag{1.3}$$

L(f) is the in-band phase noise density (dBc/Hz), *p* is the peaking of *k*, f_C is the loop bandwidth of the phase lock loop. The rms phase noise from 0 Hz up to infinity in the WiMAX proposal should be below 1 degree rms. Assuming that p is zero and the loop bandwidth is 100 kHz, in order to achieve the integrated phase noise below 1 degrees rms, the phase noise should below -88.2dBc/Hz. The result can be calculated via the following equation.

$$k = 20\log\frac{(1)\cdot\frac{\pi}{180}}{\sqrt{100k\cdot(1+10^{0/10})+10^{0/10}\cdot 2}} = -88.2(dBc/Hz) \qquad (1.4)$$

As phase-locked loop out-band noise is dominated by VCO and is reduced 20 dB per decade, phase noise at 1MHz offset can be calculated as -108.2dBc/Hz. Consider that the divider ratio N raises out-band phase noise level by 20logN, VCO phase noise specification at 10kHz and 1MHz offset are -70 dBc/Hz and -120 dBc/Hz, respectively. The overall design specification of the VCO for WiMAX standard is shown in Table 1.1. The power consumption is designed as small as possible.

Table 1.1 Overall design Specification of the VCO

Parameters	**Specification**
Frequency range	2305MHz~2690MHz
Phase Noise	< -70dBc/Hz@10kHz
	< -120dBc/Hz@1MHz
Supply Voltage	1.2V, 1V
Process	UMC 0.13, 0.09-μm CMOS

1.3 QVCO topologies

The conventional QVCO has the trade off between phase error and phase noise, as shown in Fig.2.1. There are several QVCO topologies were invented for improving both phase error and phase noise, like Top-Series (TS), Bottom-Series (BS), Injection Locking (IL) and Common-Mode Inductive Coupling. They are introduced as the following:

1.3.1 Conventional QVCO

As shown in Figure 1.1, the quadrature phase is generated by using coupling stages. While the coupling current is injected into the output node, the QVCO oscillation frequency is shifted from the VCO alone oscillation frequency. As each LC tank has the highest impendence at VCO alone oscillation frequency, the frequency shift results in the phase noise degrading. In section 2.1 and 2.2, the conventional QVCO will be discussed in detail.

1.3.2 Top-Series (TS) QVCO

TS QVCO is shown in Figure 1.4 [6]. As their coupling stages are in series with VCO transconductance stages, the phase error is almost constant whether the ratio between transconductances of VCO and coupling stages. That means that the phase noise can be improved without the expense of poor phase error.

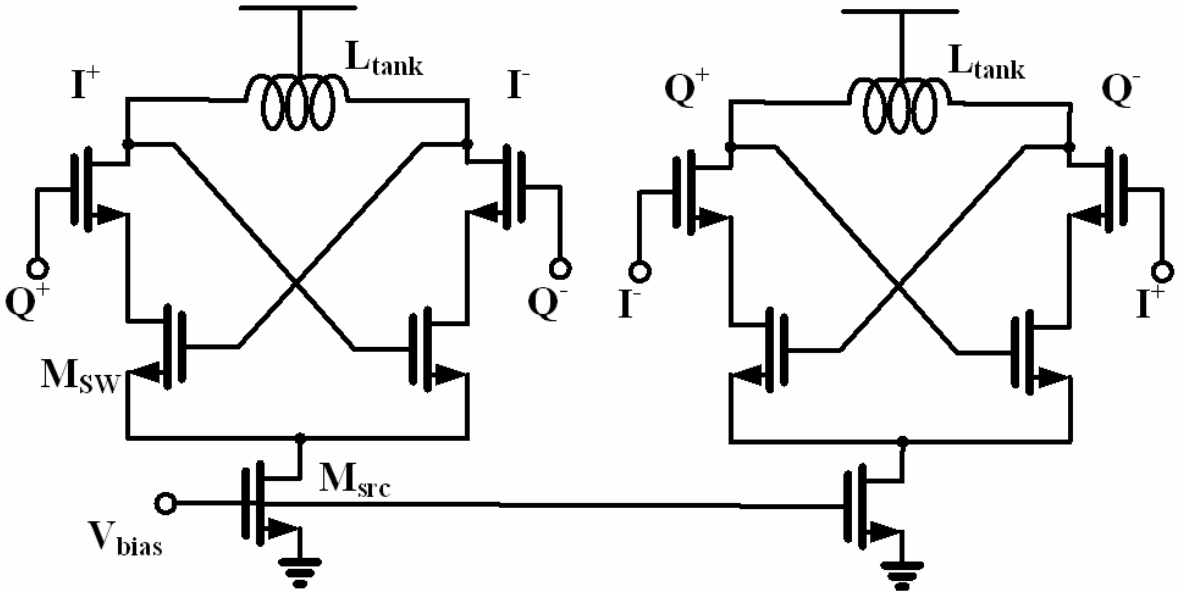


Figure 1. 4 Top-series quadrature VCO[6].

1.3.3 Bottom-Series (BS) QVCO

BS QVCO is shown in Figure 1.5 [7]. The coupling stages are also in series with VCO transconductance stages. As the coupling stages' common-mode impendence is lower than TS QVCO, the phase noise performance is a little higher than TS QVCO.

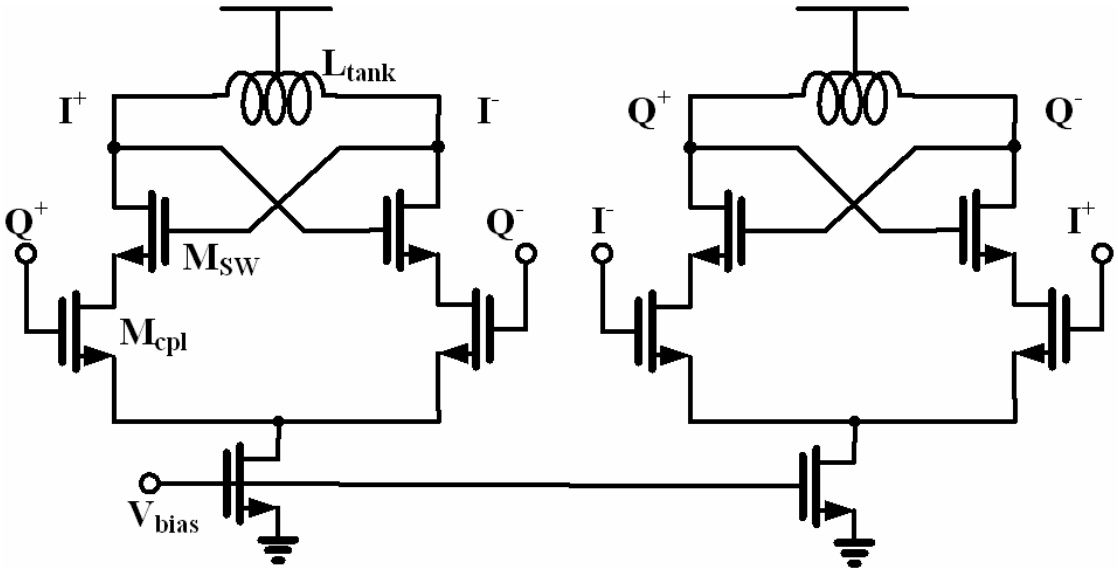


Figure 1. 5 Bottom-series quadrature VCO [7].

1.3.4 Injection Locking(IL) QVCO

IL QVCO is shown in Figure 1.6 [8]. Instead of coupling stages, the master VCO oscillates at the double frequency of the slave VCOs and the common-mode nodes of slave VCOs are out of phase. Slave VCO's phase noise is 6dB lower than master VCO's phase noise ideally.

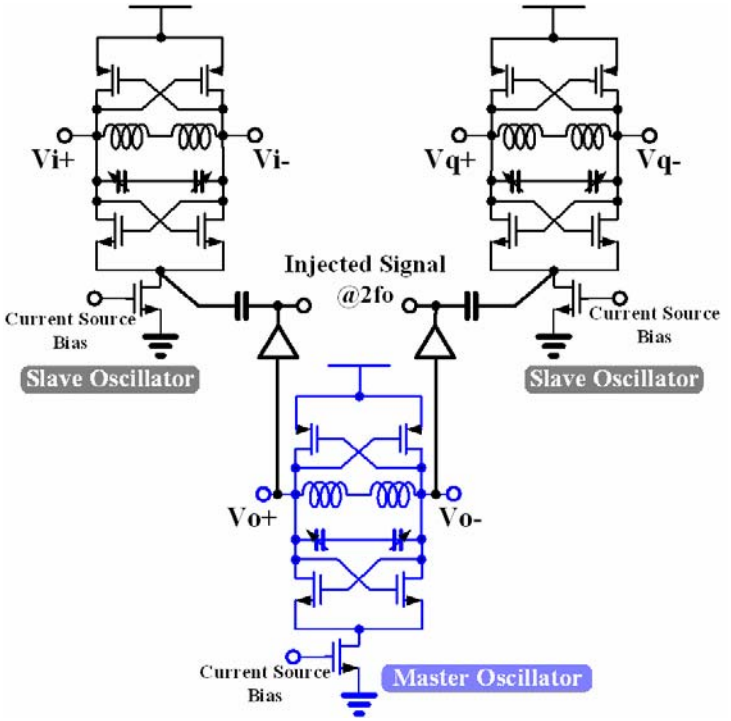


Figure 1. 6 Injection locking quadrature VCO [8].

1.3.4 Common-Mode Inductive Coupling QVCO

Common-Mode Inductive Coupling QVCO is shown in Figure 1.7 [9]. Compared to traditional QVCO, coupling stages are replaced by the transformer. Common-mode nodes of two VCOs are out of phase and four VCO outputs are quadrature. The phase noise is suppressed by the LC tanks which provide high impendence at second harmonic frequency.

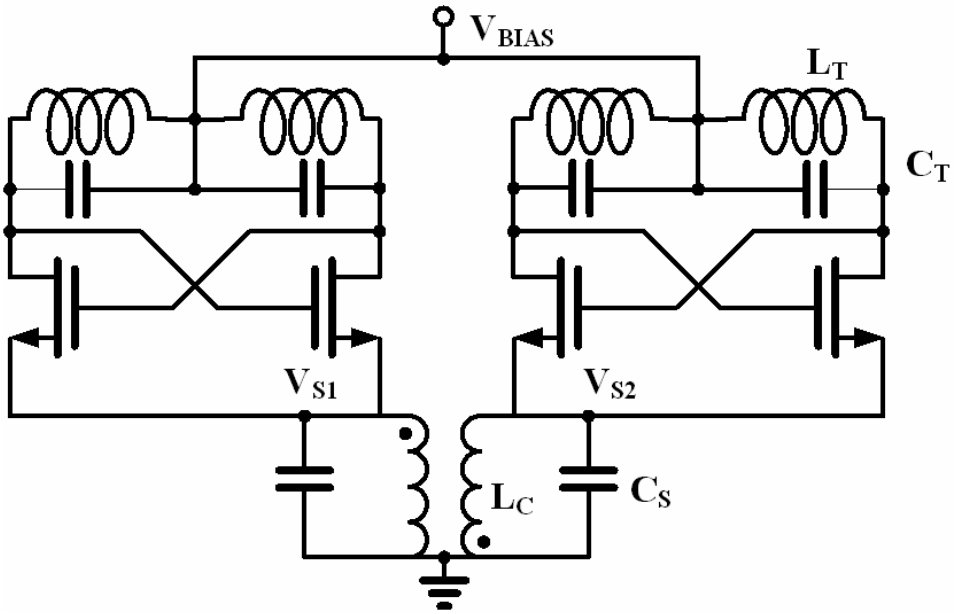


Figure 1. 7 Top-series quadrature VCO [9].

1.3.5 Summary

Table 1.2 summarizes QVCO topologies' advantages and disadvantages. If the same phase error performance is requested, the conventional QVCO phase noise is poor. However, other topologies get better performance at the expense of output swing, power consumption or area size.

Table 1.2 QVCO topologies summary.

QVCO topologies	Advantage	Disadvantage
Conventional	Simple	Bad phase noise
Top-Series (TS)	The coupling transistors don't contribute noise	Low output swing
Bottom-Series (BS)	Cross-coupled transistors don't contribute noise	Low output swing
Injection Locking(IL)	Slave VCO phase noise will be better than master VCO about 6dB	High power Large size
Common-Mode Inductive Coupling	Second order harmonic will be suppressed	Large size

1.4 Organization

This thesis describes the design of LC quadrature voltage-controlled oscillator with phase error mismatch compensation technique. Chapter 1 introduces the motivation, specifications of VCO for the WiMax applications and QVCO topologies. In Chapter 2, common-mode mismatch on the phase accuracy in this work is analysized. Chapter 3 presents the phase error compensation techniques in the proposed QVCO. The implementations of the quadrature-phase VCO are described in Chapter 4, including the QVCO, compensation circuit, and the single-sideband mixer. The layout, the testing setup, and measurement results of the quadrature voltage-controlled oscillator are also presented. Chapter 4 also presents the behavioral model of the VCO for saving simulation time. Chapter 5 gives the conclusions and the future works.

Chapter 2

Analysis of QVCO with Common-Mode Technique

2.1 Differential-Mode Model of QVCO

Figure 2.1 shows the conventional QVCO. Several papers [10][11] discuss trade off between phase noise and phase error base on QVCO differential mode (DM) model, as depicted in Figure 2.2. Transconductances of VCO and coupling stage are represented by G_m and G_{mc}, respectively. As the phase of a loop is 360 degrees, each

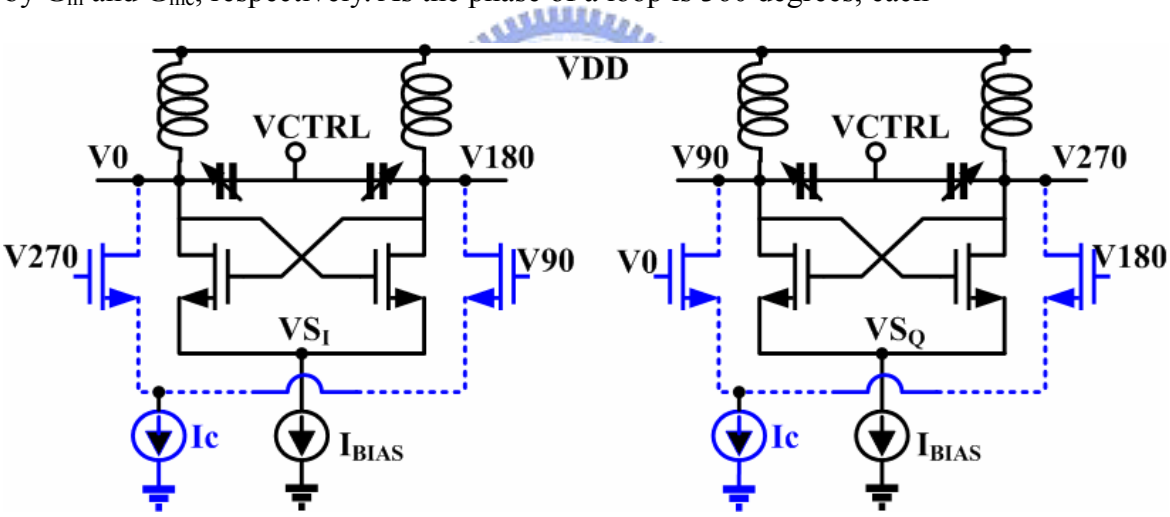


Figure 2. 1 Conventional Quadrature VCO.

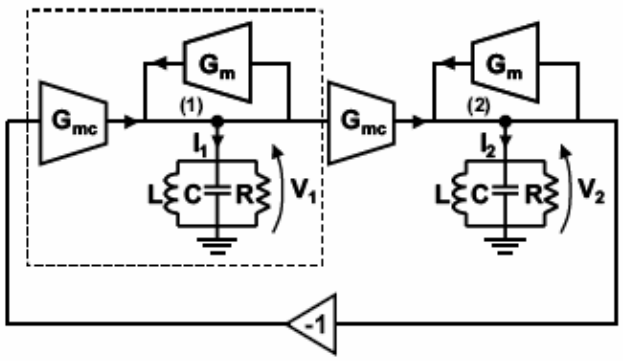


Figure 2. 2 QVCO differential mode model [10].

stage including VCO and coupling stage achieves 90 degrees phase shift. In [10], the phase error and phase noise of QVCO are analyzed with the phasor diagram of the currents injected into the two tanks. The link between phase derivation $d\theta$ and frequency derivation $d\omega$ is the derivative of the admittance angle at oscillation frequency ω_{osc} :

$$d\omega = \frac{\omega_{osc}}{2Q} \cdot \left(1 + m^2\right) \cdot d\theta = \frac{\omega_{osc}}{2Q} \cdot \sqrt{1 + m^2} \cdot \frac{1}{2} \cdot \frac{i_n R}{A_0} \tag{2.1}$$

where Q is the tank quality factor and m is the differential-mode transconductance ratio of coupling pair to that of VCO core pair. The phase noise and phase error are expressed as

$$L(\omega_m) = \frac{kT}{C} \cdot \frac{\omega_{osc}}{Q} \cdot \frac{1+m^2}{2} \cdot \frac{1}{\omega_m^2} \cdot \frac{1+F_Q}{A_0^2}. \tag{2.2}$$

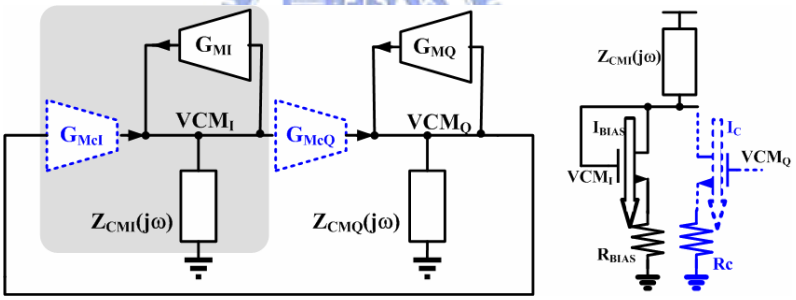
$$d\phi = \frac{Q}{m^2} \cdot \frac{d\omega}{\omega_{osc}}. \tag{2.3}$$

where phase noise $L(\omega_m)$ and phase error $d\phi$ are functions of m. $F_Q=(1+m)F$, where F is noise factor of the stand-alone VCO. ω_m and A_0 represent the offset frequency and output amplitude, respectively [10]. As transconductance ratio decreases, better phase noise can be achieved but with the penalty of poor phase accuracy.

2.2 Common-Mode Model of QVCO

For ideal QVCO, the common mode nodes of VCOI and VCOQ see the second harmonic of oscillation frequency and the phase difference should be 180 degrees. Any mismatch between VCOI and VCOQ causes phase mismatch in the common mode and therefore quadrature phase errors occur. Minimizing common-mode phase error helps to improve quadrature phase accuracy.

Figure 2.3(a) shows common-mode (CM) model of a QVCO. $Z_{CM}(j\omega)$ represents LC tank impedance. Figure 2.3(b) shows one stage of CM model, as grey part in Figure 2.3(a). Assume there is impedance and common-mode transconductance mismatches in



(a) (b)

Figure 2. 3 Common-mode model: (a) QVCO, (b) VCO_I and coupling stage.

VCO_I and VCO_Q. The impedance $|Z_{CMQ}(j\omega)|$ can be expressed as $|Z_{CMI}(j\omega)/(1+\varepsilon)$ and ΔG_M is the common-mode transconductance mismatch. At the output common mode nodes V_{CMI} and V_{CMQ}, they can be expressed by

$$V_{CMI} = (-G_{McI}V_{CMI} - G_{McI}V_{CMQ})Z_{CMI}(j\omega)$$
$$V_{CMQ} = (-G_{McQ}V_{CMQ} - G_{McQ}V_{CMI})Z_{CMQ}(j\omega). \quad (2.4)$$

The ratio between VCM_Q and VCM_I is

$$\frac{VCM_Q}{VCM_I} = \frac{-\Delta G_M}{2G_{McI}} + (\frac{-\varepsilon}{2}) \cdot (\frac{G_{MI}}{G_{McI}}) \pm \left[\left(\frac{\Delta G_M}{2G_{McI}} + (\frac{\varepsilon}{2}) \cdot (\frac{G_{MI}}{G_{McI}}) \right)^2 + \frac{G_{McQ}}{G_{McI}} \right]^{\frac{1}{2}} \quad (2.5)$$

While ΔG_M and ε are both zero, the ratio between VCM_Q and VCM_I is -1 or +1. If VCO and coupling stage share the current source, both VCO common mode will be in phase for the same source terminal and (2.5) equals to +1. If separate current sources are used for VCO and coupling stage, (2.5) equals to -1 meanwhile VCM_Q and VCM_I are out of phase. Usually separate current sources are prefer for modifying the current ratio when measuring QVCO, (2.5) can be modified as (2.6).

$$\frac{VCM_Q}{VCM_I} = \frac{-\Delta G_M}{2G_{McI}} + (\frac{-\varepsilon}{2}) \cdot (\frac{G_{MI}}{G_{McI}}) - \left[\left(\frac{\Delta G_M}{2G_{McI}} + (\frac{\varepsilon}{2}) \cdot (\frac{G_{MI}}{G_{McI}}) \right)^2 + \frac{G_{McQ}}{G_{McI}} \right]^{\frac{1}{2}} \quad (2.6)$$

In (2.6), we can see the common-mode mismatch only results in magnitude error between VCO_I and VCO_Q. The VCM_I and VCM_Q modulate the varactors in VCOs and therefore introduce common-mode phase error in VCM_I and VCM_Q as magnitude error can be derived by using (2.6), as expressed in (2.7).

$$\Delta V = V_{CMI} - V_{CMQ} \tilde{=} \left(-1 + \frac{\Delta G_{Mc}}{2G_{McI}} + \left[\frac{G_{McQ}}{G_{McI}} \right]^{\frac{1}{2}} + (\frac{\varepsilon}{2}) \cdot (\frac{G_{MI}}{G_{McI}}) \right) \cdot V_{CMI} \quad (2.7)$$

The relationship between the second harmonic output common-mode amplitude and the first harmonic different-mode amplitude can be assumed as

$$VCM_{I\_2\omega_{OSC}} = \frac{\frac{1}{2} VDM_{I\_\omega_{OSC}}}{\sqrt{1 + jQ(\frac{\omega}{\omega_{OSC}} - \frac{\omega_{OSC}}{\omega})}} \quad (2.8)$$

Thus the phase error can be derived, as (2.9).

$$d\theta_{2nd\_osc} = \frac{Q}{m^2}\cdot\frac{d\omega}{\omega_{osc}} \cong \frac{K_{VCO\_instant}VDM_I}{3m^2\omega_{osc}}\cdot\left(\frac{\Delta G_M}{2G_{McI}} + (\frac{\varepsilon}{2})\cdot(\frac{G_{MI}}{G_{McI}})\right) \quad (2.9)$$

where VDM_I represents different-mode output swing at VCO oscillation frequency. The phase error $d\theta_{2nd\_osc}$ is inversely proportional to coupling stage common-mode transconductance G_{McI}.

Now current source finite resistance is taken into consideration. From Figure 2.3 (b), the term $\Delta G_M/G_{McI}$ can be re-derived as

$$\frac{\Delta G_M'}{G_{McI}'} = \frac{\Delta G_M}{G_{McI}}\cdot\frac{1}{1+(\Delta G_M + G_{MI})R_{BIAS}}\cdot\frac{1+G_{McI}R_C}{1+G_{MI}R_{BIAS}} \quad (2.10)$$

(2.9) can be modified as

$$d\theta_{2nd\_osc} = \frac{Q}{m^2}\cdot\frac{d\omega}{\omega_{osc}} \cong \frac{K_{VCO\_instant}V_{DMI}}{3m^2\omega_{osc}}\cdot\left(\frac{\Delta G_M'}{2G_{McI}'} + (\frac{\varepsilon}{2})\cdot(\frac{G_{MI}'}{G_{McI}'})\right) \quad (2.11)$$

Where $\frac{\Delta G_M'}{G_{McI}'} = \frac{\Delta G_M}{G_{McI}}\cdot\frac{1}{1+(\Delta G_M + G_{McI})R_{BIAS}}\cdot\frac{1+G_{McI}R_C}{1+G_{MI}R_{BIAS}}$

$\frac{G_{MI}'}{G_{McI}'} = \frac{G_{MI}}{G_{McI}}\cdot\frac{1+G_{McI}R_C}{1+G_{MI}R_{BIAS}}$

The phase error $d\theta_{2nd\_osc}$ is inversely proportional to coupling stage common-mode transconductance G_{McI}. While no transconductance mismatch occurs in QVCO, R_{BIAS}/R_C equals to G_{McI}/G_{MI} and $(1+G_{McI}R_C)/(1+G_{MI}R_{BIAS})$ equals to one.

In QVCO design, the transconductance ratio m is set to a small value for better phase noise. As derived in (2.11), the terms $K_{VCO\_instant}$ and $(1+G_{McI}R_C)/(1+G_{MI}R_{BIAS})$ can be minimized to reduce the phase error. Therefore, the switch capacitor array and the compensation circuit are used to reduce $K_{VCO\_instant}$ and $(1+G_{McI}R_C)/(1+G_{MI}R_{BIAS})$, respectively.

Chapter 3
Common-Mode Compensation Technique

To minimize phase error is an issue in designing the QVCO without degrading the phase noise. This chapter will introduce the proposed phase error mismatch compensation technique.

3.1 The Compensation Circuit

From (2.11), the common-mode phase error $d\theta_{2nd\_osc}$ can be minimized by reducing the equivalent resistance (R_C) seen at the source node of the coupling stage. A compensation circuit is proposed to reduce R_C and $d\theta$ as shown in Figure 3.1. VCO_Q was compensated by the same circuit and Figure 3.1 only shows VCO_I.

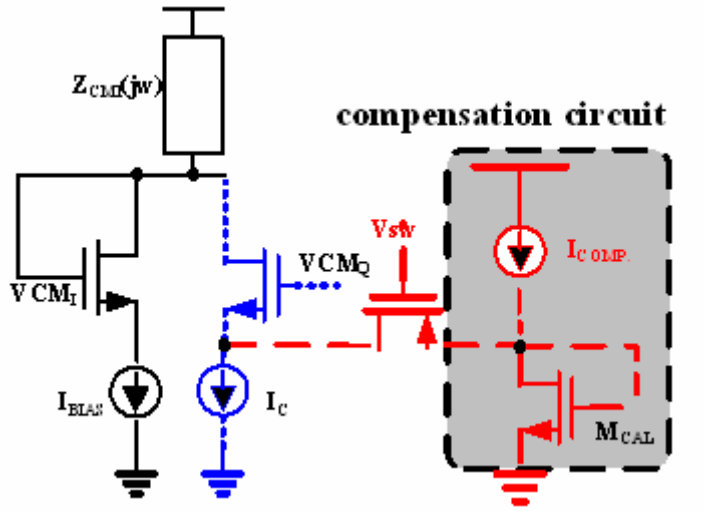


Figure 3. 1 VCO_I and its coupling stage with the compensation circuit.

Transistor M_{CAL} is self-biased and the additional current source is used to make the bias point the same. The MOS switch is used for measurement comparison. When switch is turned on, the circuit compensates the phase error mismatch. Figure 3.2 shows the equivalent model of Figure 3.1, current sources are replaced by resistances. Transistor M_{CAL} is self-biased and R_{SW} and R_X represent the switch and the loading of M_{CAL}, respectively. At the source node of the coupling stage transistor, equivalent resistance is changed to $[R_C//R_{SW}+(R_X//1/G_{MCAL})]$ represented by R_C'. Thus the phase error with compensation can be expressed as

$$d\theta_{compensate} = d\theta \cdot \frac{1+G_{MI}R_C}{1+G_{MI}R_C'} \tag{3.1}$$

Phase error is improved $(1+G_{MI}R_C)/(1+G_{MI}R_C')$ times than original one. The compensation circuit only influences common-mode property of QVCO and differential-mode performance of QVCO remains the same.

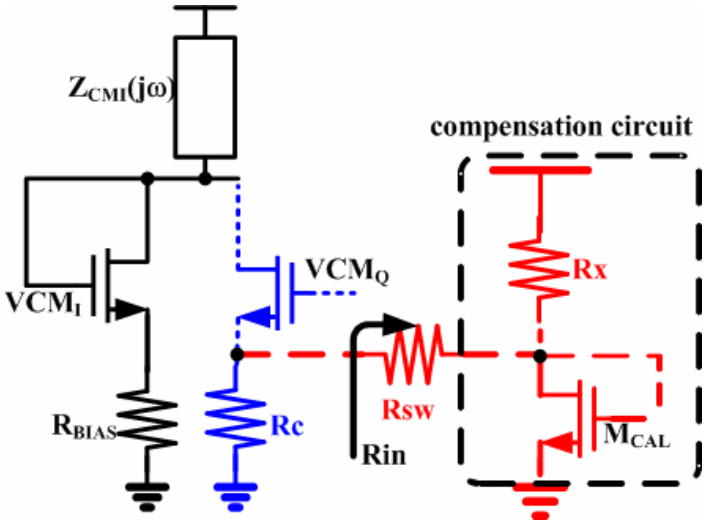


Figure 3. 2 VCO_I and its coupling stage with the compensation circuit.

3.2 Simulation Results

3.2.1 Schematics

To verify the analysis, a QVCO with a compensation circuit is designed in a UMC 90nm CMOS process. Figure 3.3 shows quadrature voltage-controlled oscillator. The transconductance stages are consist of PMOS transistors for low flicker noise and stable output common mode.

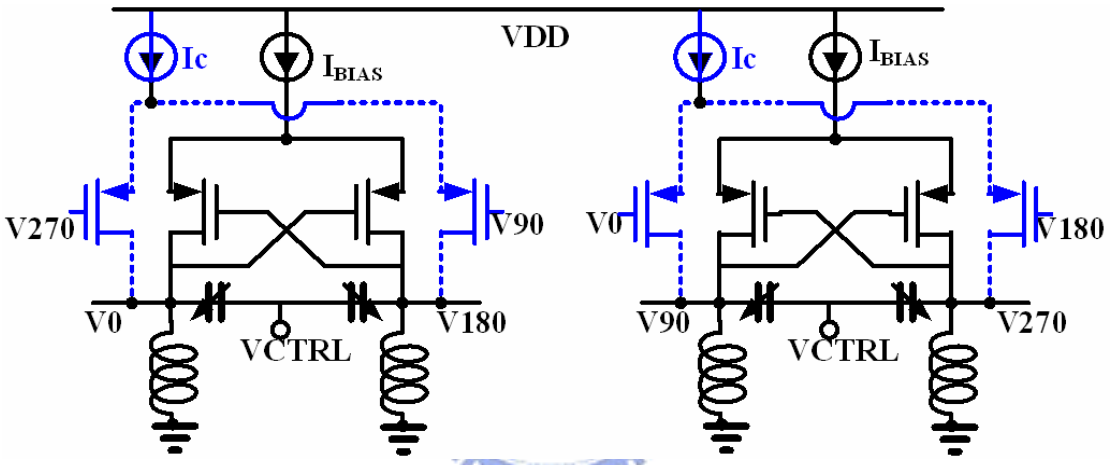


Figure 3. 3 Quadrature voltage-controlled oscillator.

The compensation circuit with VCO_I and coupling stage (Common-mode model) is shown in Figure 3.4.

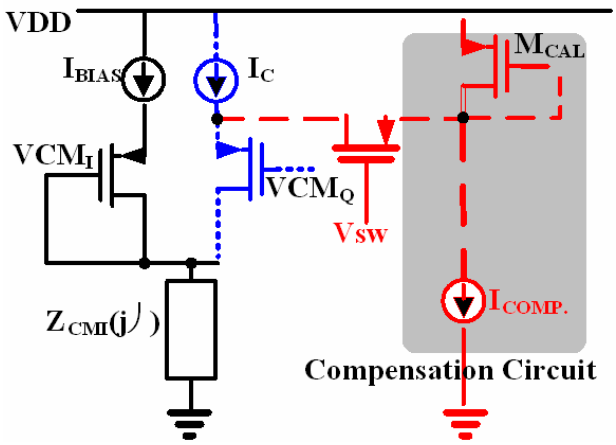


Figure 3. 4 The compensation circuit.

As QVCO phase error is often characterized by image-rejection ratio (IRR) in measurement, a passive mixer is also included. (IRR=10log(0.25((AmplitudeError / Amplitude)^2+(PhaseError)^2))[12]) The passive single side band mixer is depicted in Figure 3.5 [6]. While measurement, The BB signal will be generated by the signal generator. The balun and polyphase RC filter are also used to change the BB signal into quadrature phase. The connection of QVCO and the SSB mixer is shown in Figure 3.6.

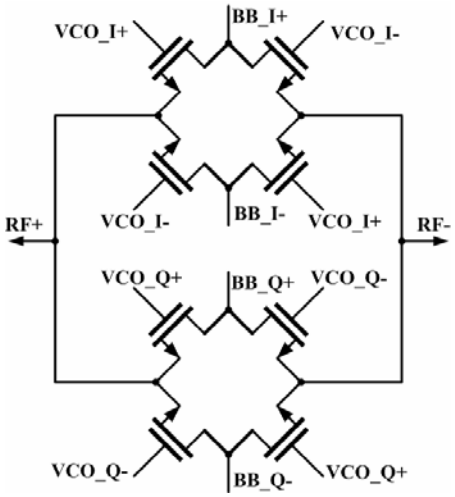


Figure 3. 5 The SSB passive mixer.

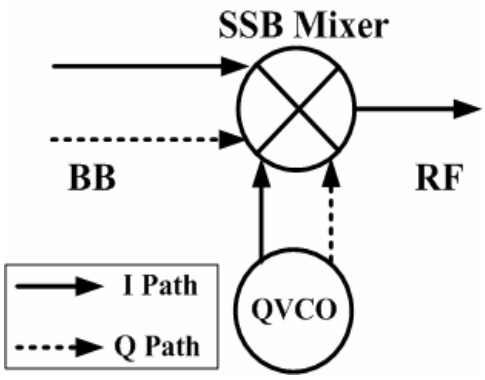


Figure 3. 6 The connection of QVCO and SSB mixer.

3.2.2 Simulation Results

Figure 3.7 shows the oscillation frequency versus control voltage. The frequency range is parted into 8 bands by the capacitor switch. The control voltage ranges from 0V to 1V and oscillation frequency ranges from 2.24-GHz to 2.82-GHz. The QVCO and the compensation circuit consume 5.5mA and 1.1mA from a 1V power supply, respectively.

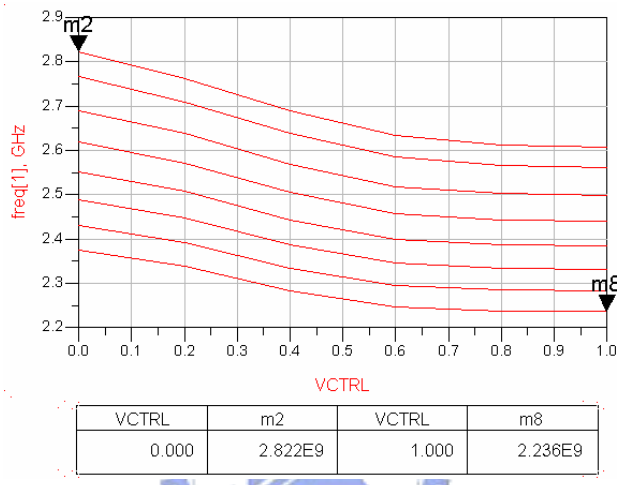


Figure 3. 7 Oscillation frequency versus control voltage.

Figure 3.8 shows the phase noise of QVCO at 2.63-GHz. Phase noise is about -76dBc/Hz and -125dBc/Hz at 10-kHz and 1-MHz offset frequency, respectively.

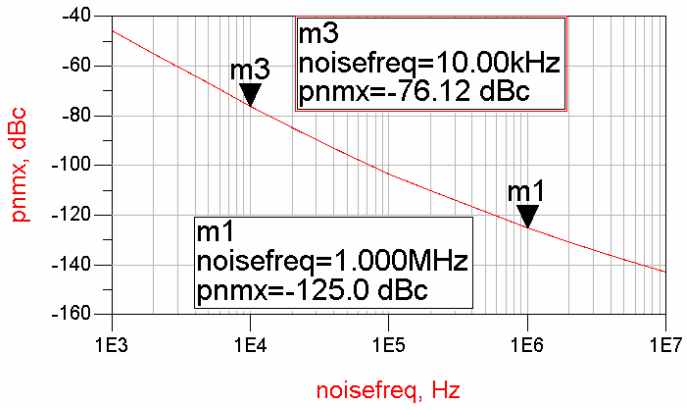
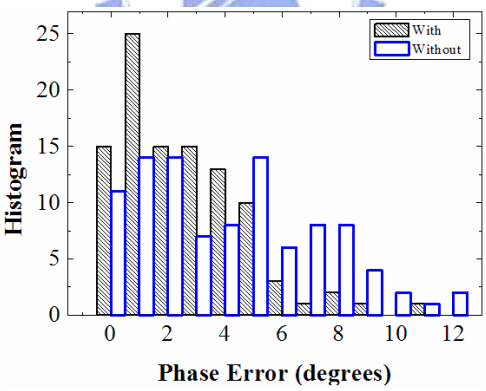
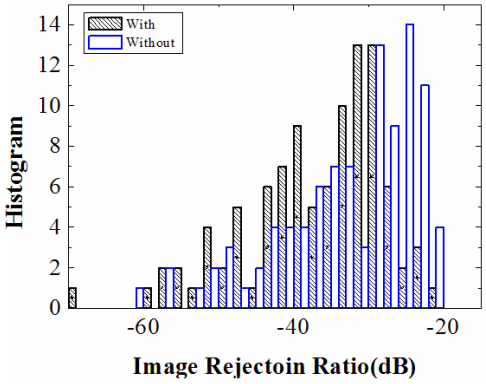


Figure 3. 8 Phase noise at 2.63-GHz.

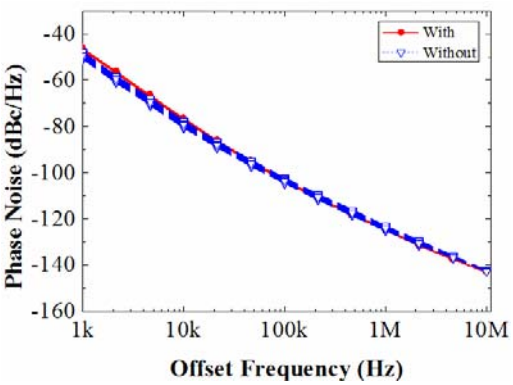
Monte Carlo simulation considering 0.5% transistor width variation is performed to validate the compensation circuit. Figure 3.9 shows simulation results of QVCO with and without the compensation circuit. Figure 3.9(a) shows phase error histogram. Figure 3.9(b) shows IRR histogram. IRR is estimated by measuring two tone's difference in harmonic simulation. From Figure 3.9(a) and Figure 3.9(b), historgrams trend left as the compensation circuit works. Figure 3.9(c) shows VCO phase noise. The phase noise results are almost the same, with or without compensation circuit. Table 3.1 summarizes the Monte Carlo simulation performance. This compensation circuit improves phase error of 1.5 degrees without degrading phase noise at 1MHz offset frequency for 2.63 GHz carrier frequency.



(a)



(b)



(c)

Figure 3. 9 Monte Carlo simulation results: (a) phase error histogram, (b) IRR histogram and (c) phase noise.

Table 3.1 Simulation result summary

Monte Carlo result comparison – With / Without the compensation circuit			
		With	Without
Phase Error	Mean (degree)	2.63	4.10
	Standard deviation (degree)	2.16	3.06
IRR	Mean (dB)	-37.42	-32.68
	Standard deviation (dB)	10.72	11.17
Phase Noise@1MHz	Mean (dBc/Hz)	-125.02	-124.68

Chapter 4
Implementations

4.1 Layout

4.1.1 Layout Considerations

The layout of differential high-frequency circuits should be as symmetric as possible. The active component should be as close as possible. The coupling effect should be concerned at high frequency, since degrades the performance of the layout. The circuit may need some shielding techniques on layout. An easy way is to use an additional ground or DC path inserted between two sensitive signals.

Additional large capacitances can insert between bias lines and ground to make the bias voltage more stable. Guard rings can help to isolate the sensitive device from the substrate noise from other circuits.

4.1.2 Layout of The First QVCO

The first QVCO transconductance stages consist of NMOS and PMOS transistors. The frequency range is parted into two bands by the capacitor switch. Figure 4.1 shows the schematic of the first QVCO fabricated in UMC 0.13um CMOS technology.The layout of the 1st QVCO is shown in Figure 4.2. The total chip area is 1464×997um^2.

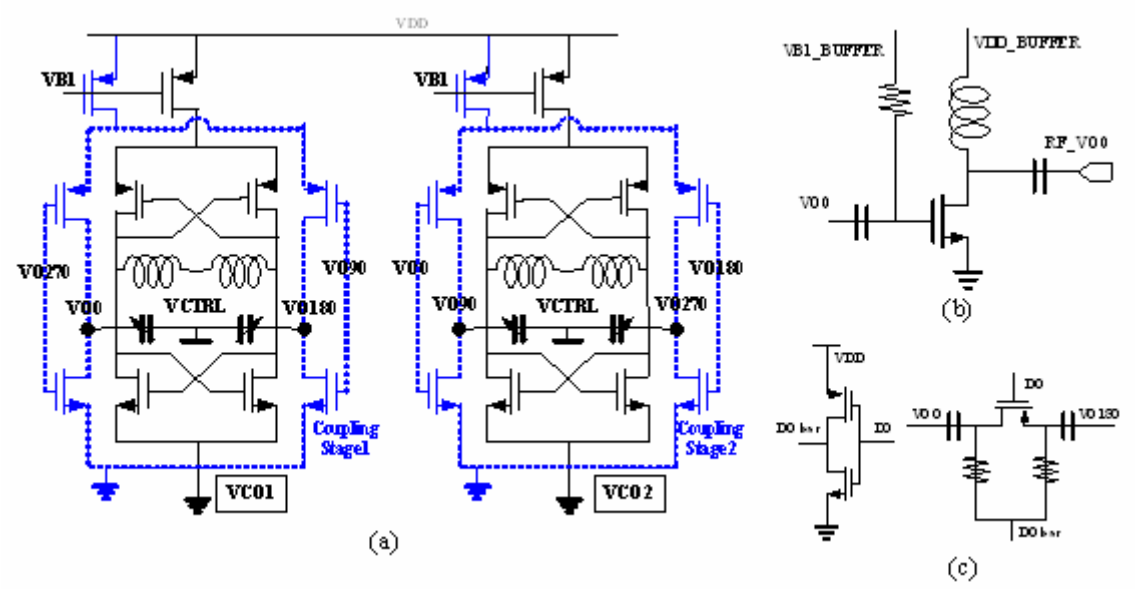
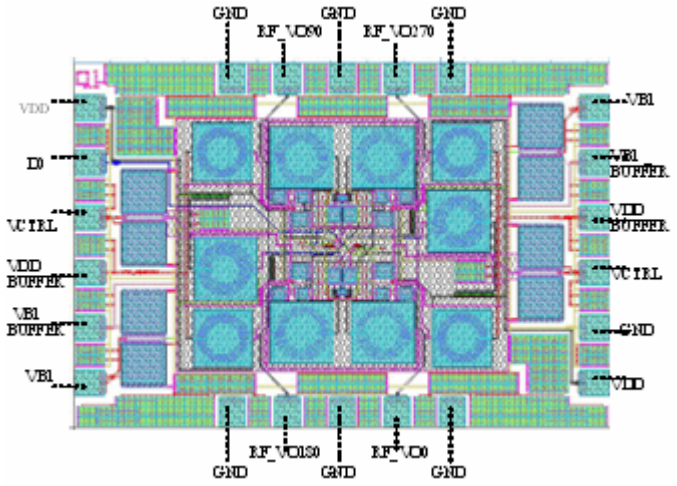
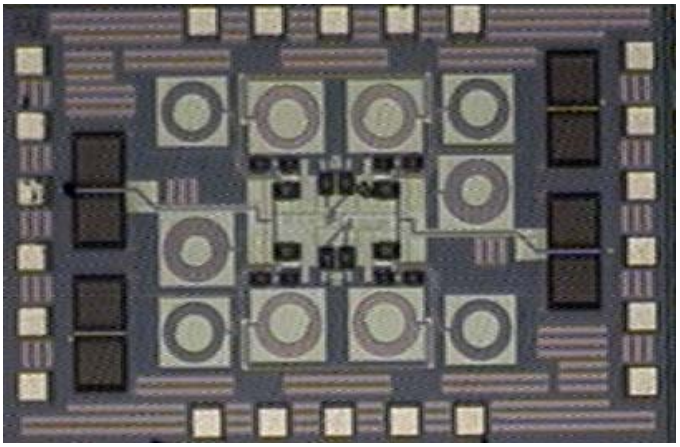


Figure 4. 1 Schematic of the 1st QVCO: (a) QVCO, (b) Buffer and (c) the capacitor switch.



(a)



(b)

Figure 4. 2 The 1st QVCO: (a) layout and (b) die photograph.

4.1.3 Layout of The Second QVCO and The Compensation Circuit

The layout of the 2nd QVCO and the compensation circuit are shown in Figure 4.3. The SSB mixer and 3-stage poly phase filter are also included. The total chip area is 1305×1290um^2. This design is fabricated in UMC 90-nm CMOS technology.

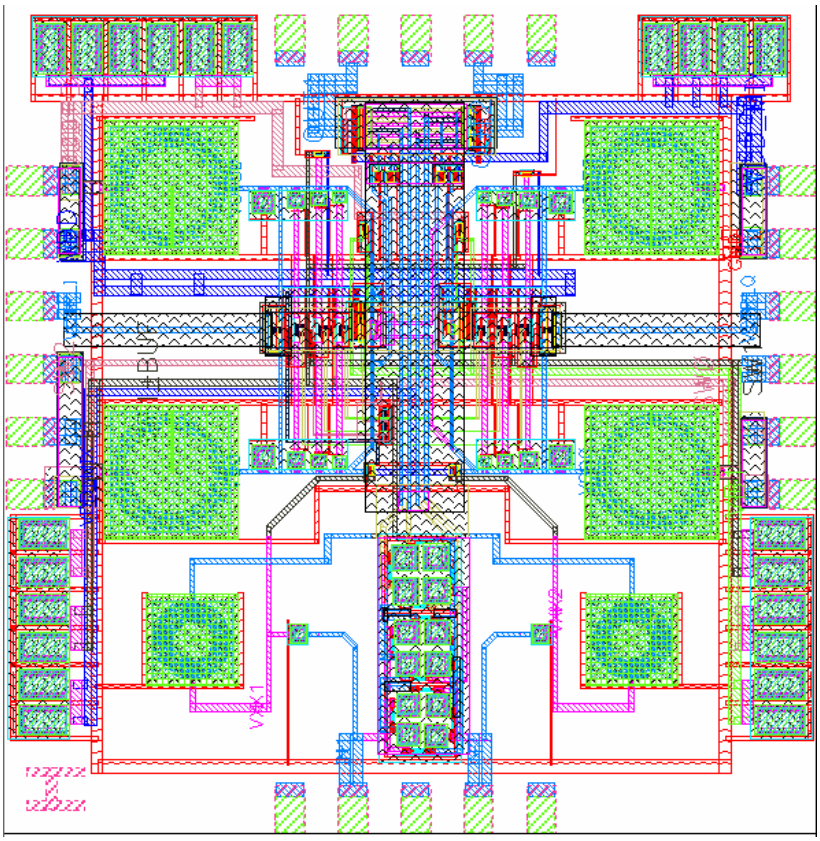


Figure 4. 3 Layout of the 2nd QVCO and the compensation circuit.

4.2 Measurement

The first QVCO is measured on the wafer and fabricated in UMC 0.13-μm CMOS technology. Both the equipments and environments of the on-wafer measurement are provided by NDL.

4.2.1 The First QVCO

Testing Setup

Figure 4.4 shows the testing setup for the phase noise and spectrum measurement of the quadrature voltage-controlled oscillator. It consists of a spectrum analyzer, two high-frequency ground-signal-ground-signal-ground (GSGSG) probes, two DC probes and a power supply box. One of the oscillator outputs is connected to the spectrum analyzer. And other outputs are terminated by a load having an impedance of 50 Ω.

Figure 4. 4 Testing setup for the quadrature voltage-controlled oscillator.

Measurement Results

The measured output spectrum at a frequency of 2.495-GHz is shown in Figure 4.5. The output power including the cable loss is about -39.8dBm.

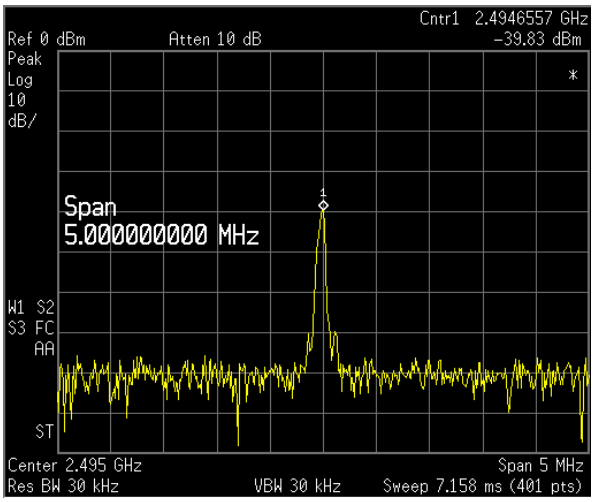


Figure 4. 5 Measured output spectrum of the on-wafer QVCO.

The tuning characteristic of the QVCO is measured by stepping the control voltage and measuring the corresponding output frequency with the spectrum analyzer. The oscillation frequency remains almost the same (variation<10-MHz) while changing the control voltage. The QVCO consumes 9.6mW from 1.2 V supply including output buffers.

Figure 4.6 shows the phase noise measurement of the on-wafer quadrature voltage-controlled oscillator at a offset frequency of 1-MHz. (Note: The carrier frequency is 2.495-GHz and the control voltage is 0.4V) the measured phase noise is -33.7dBc/Hz at 10-kHz frequency offset and -99.35dBc/Hz at 1-MHz frequency offset. Table 4.1 shows the phase noise at 10-kHz and 1-MHz versus control voltage.

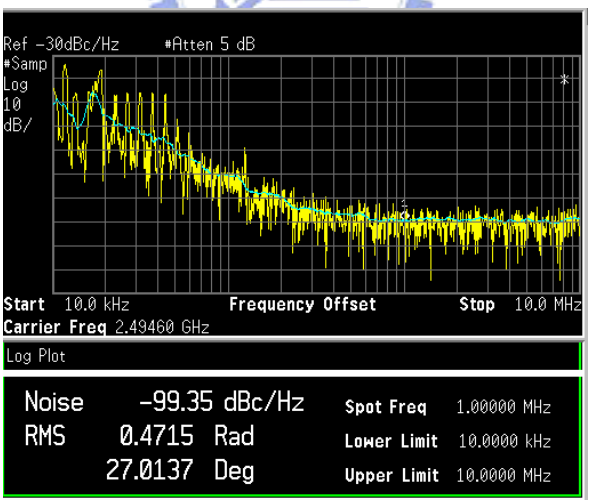


Figure 4. 6 Measured phase noise of the on-wafer QVCO.

Table 4.1 Phase Noise (dBc)@10kHz/1MHz versus Control Voltage.

Vctrl(V)	0	0.2	0.4	0.6	0.8	1.0	1.2
Switch off	-35.2 -94.1	-45.8 -88.9	-51.6 -93.7	-37.6 -87.2	-34.5 -86.5	-33.6 -91.3	-31.3 -89.4
Switch on	-44.5 -96.8	-57.9 -98.2	-33.7 -99.4	-48 -92.3	-43.4 -91.6	-48.4 -96.5	-37.8 -91.4

Table 4.2 summaries the first QVCO performance. The DC power consumption of buffer is large due to VCO output bias point is changed. As the ouput buffer is drived by the VCO output bias point, the CMOS transconductance VCO has more common mode variation than only NMOS/PMOS transconductance VCO. All power supplies and DC bias voltages are ideal voltage sources in simulation. The on-chip regulators should be added between the power lines.

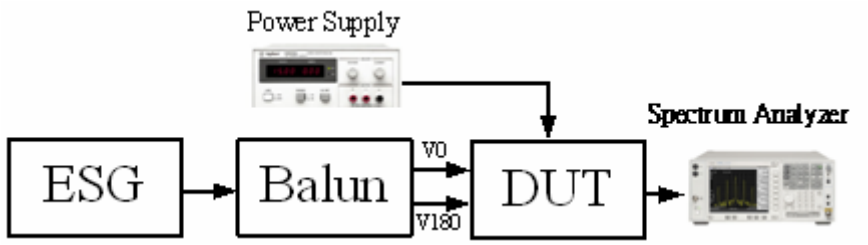
Table 4.2 The 1st QVCO performance summary.

	Pre-Sim.	Post-Sim.	measurement
Tuning Range(GHz)	2.27~2.72	2.281~2.704	2.485~2.495
Phase noise@1MHz (dBc)	-116.9dBc (at 2.7GHz)	-116.1dBc (at 2.7GHz)	-86.5dBc (at 2.485GHz)
Output Power: Core / Buffer (dBm)	1.6 / -2.4 (at 2.7GHz)	1.56 / -2.6 (at 2.7GHz)	X / -40 (at 2.485GHz)
DC power consumption: Core / Buffer (mW)	2.94 / 3.13	2.95 / 3.22	2.4 / 7.2
FOM (VCO alone)	-180.3	-179	-150.6

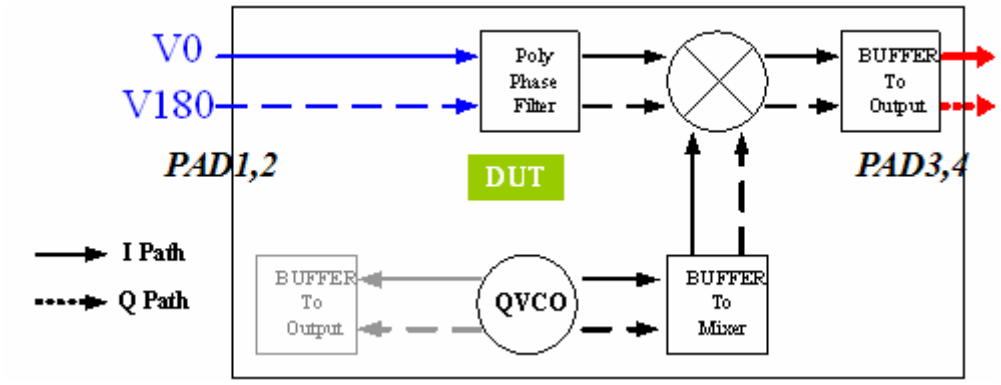
$$note: FOM = L\{f_{offset}\} - 20\log(\frac{f_0}{f_{offset}}) + 10\log(\frac{P_{DC}}{1mW})$$

4.2.2 The Second QVCO and The Compensation Circuit Testing Setup

The testing setup for the measurement of the image rejection ratio is shown in Figure 4.7. It consists of a spectrum analyzer, two high-frequency ground-signal-ground-signal-ground (GSGSG) probes, a DC probe, an ESG, a balun, and a power supply box. The balun can convert the single-ended input signal to the differential output signal.



(a)



(b)

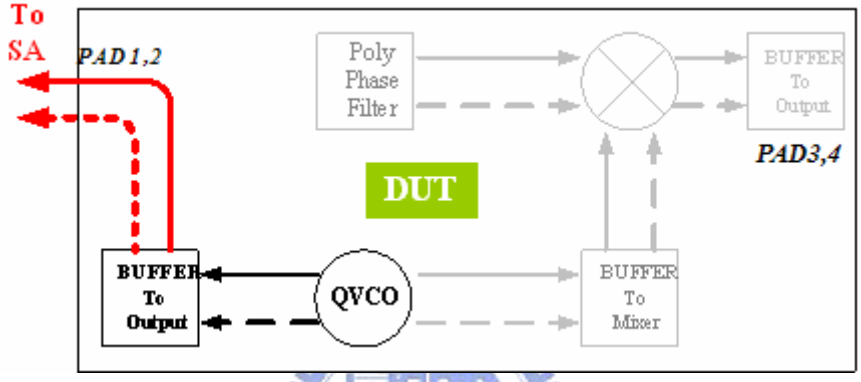
Figure 4. 7 Testing setup for the image rejection ratio: (a) instrument connection (b) device under test.

There are four signal pads in the device under test, where pad1&2 connect to the poly phase filter and pad3&4 connect to the mixer output buffer. As shown in Fig.4.7(b), the buffer connecting to pad1&2 is off and the other buffer is active. One of the mixer buffer outputs is connected to the spectrum analyzer. And the other outputs are terminated by a load having an impedance of 50 Ω.

Figure 4.8 shows the testing setup for the phase noise and spectrum measurement of the quadrature voltage-controlled oscillator. It consists of a spectrum analyzer, a high-frequency ground-signal-ground-signal-ground (GSGSG) probe, a DC probe and a power supply box. One of the oscillator outputs is connected to the spectrum analyzer. And other outputs are terminated by a load having an impedance of 50 Ω. In the device

under test, the buffer connecting to the pad1&2 is active. The mixer and other buffers are off, as shown in Fig 4.8(b).

(a)



(b)

Figure 4. 8 Testing setup for VCO performance: (a) instrument connection, (b) device under test.

Measurement Results

This part will be finished soon when the wafer is back. Table 4.3summaries the second QVCO simulation performance.

Table 4.3 The 2nd QVCO performance summary.

	Pre-Sim.	Post-Sim.
Tuning Range(GHz)	2.27~2.82	2.21~2.79
Phase noise@1MHz (dBc)	-125dBc (at 2.63GHz)	-122.3dBc (at 2.63GHz)
Output Power: Core / Buffer (dBm)	4.68 / -1.4 (at 2.63GHz)	4.3 / -2.3 (at 2.63GHz)
DC power consumption: core / Comp. CKT (mW)	5.5 / 1.1	5.6 / 1.1
FOM (VCO alone)	-186	-183.1

4.2.3 Summary

Table 4.4 summaries the QVCO performance compared with other papers. The work1 and the work2 are designed in UMC 0.13um and 90nm CMOS technology, respectively.

Table 4.4 The QVCO performance summary.

	Tech. (CMOS)	Phase noise [dBc@Hz]	Freq. [GHz]	Freq. Range [GHz]	Power Consumption [mW]	Area [umxum]	FOM [dBc/Hz]
Kenneth K. O 05' JSSC [3]	0.18um	-134@1M	2.42	2.4~2.44 4.7, 5	4.6	800 x800	-195.2
Charles G. 05' JSSC [4]	0.18um	-70@10k	5.32	Not listed	13.5	Not listed	-173.21
Lin Jia,…IEEE MAWC Letters 06'[5]	0.25um	-80@10k -134@1M	2.2	2.05~2.25	8.4	Not listed	-178.56 -191.6
Ting-Yueh Chih 05'IEEE APMC[6]	0.18um	-135@3M -126@3M	2.74 5.49	2.35~2.75 4.8~5.8	5.4 8	800 x500	-188.3 -183.7
Work1 (post-Sim.)	0.13um	-59.6@10K -116.1@1M	2.7	2.281~ 2.704	2.95	1464 x997	-164 -179
Work1 (measurement)	0.13um	-34.5@10k -85.5@1M	2.485	2.485~ 2.495	2.4	1464 x997	-138.6 -150.6
Work2 (post-Sim.)	90nm	-73.1@10k -122.3@1M	2.63	2.21~2.79	5.6	1305 x1290	-173.6 -183.1
Spec.		-70@10k -120@1M		2.3~2.7			

$$note: FOM = L\{f_{offset}\} - 20\log(\frac{f_0}{f_{offset}}) + 10\log(\frac{P_{DC}}{1mW})$$

The performance of work1 doesn't meet the specification; there are some modifications in work2 to improve the phase noise. The CMOS transconductance stages are replaced by the PMOS only transconductance stage, thus the output common-mode is more stable and more overdrive voltage can be available for the current source transistor. So

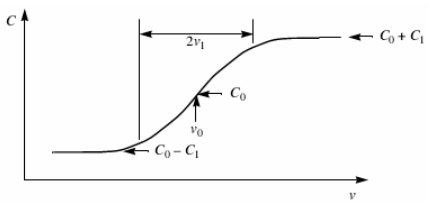
the thermal noise of the current source transistor is reduced. The frequency range is parted into 8 bands in work2 rather than 2 bands in work1. The power consumption is raised for reducing the inductor value, thus the percentage of fixed capacitors is also raised and there is less frequency variation. The phase noise is improved about 10dB at 10-KHz.

4.3 Behavioral Model

The electronic characteristics should be added in the behavioral model, thus transistor circuits can be replaced by the behavior model. Harmonic and transient simulations should be run with the same behavior model. In this section, 0.13um CMOS QVCO is modeled in Verilog-A and the comparison will be shown.

4.3.1 Varactor

Capacitor value of the varactor varies with the control voltage. It is nonlinear and two boundary values exist, as shown in Figure 4.9(a) [13]. The varactor characteristics can be modeled with log function and turning points. The Verilog-A code is shown in Figure 4.9(b). Figure 4.10 shows the post-simulation and Verilog-A simulation results.



(a)

```
analog begin
   v = V(p,n);
   if (v>v0)
      //q = c0*v + c1*v1*ln(cosh((v - v0)/v1));
      q = c0*v + c1*v1*ln(cosh((v - v0)/v1));
   if (v<=v0)
      //q = c0*v + c2*v2*ln(cosh((v - v0)/v2));
      q = c0*v + c2*v2*ln(cosh((v - v0)/v2));

   I(p, n) <+ ddt(q);
end
```

(b)

Figure 4. 9 The varactor characteristics: (a) Capacitor value versus the control voltage [13], (b) verilog-A code.

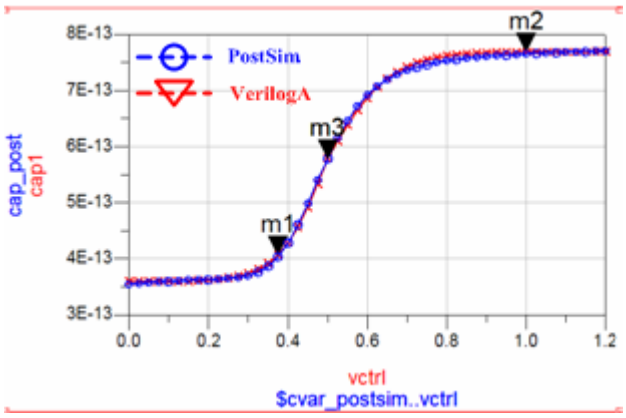


Figure 4. 10 Varactor model simulation result: capacitor versus control-voltage.

To quantize the model accuracy, root mean square error (RMSE) is used here.

$$\text{RMSE: Root Mean Square Error} = \sqrt{\left[\frac{1}{n}\sum_{i=1}^{n}\left(y_1[i]-y_2[i]\right)^2\right]}$$

The RMSE of varactor Verilog-A model is 4.57fF.

4.3.2 Inductor of LC Tank

The inductor of LC tank is modeled by excracting the passive components. The schematic is shown in Figure 4.11. Simulation results are shown in Figure 4.12. RMSEs of imagine part and real part are 21pH and 0.19 Ω, respectively.

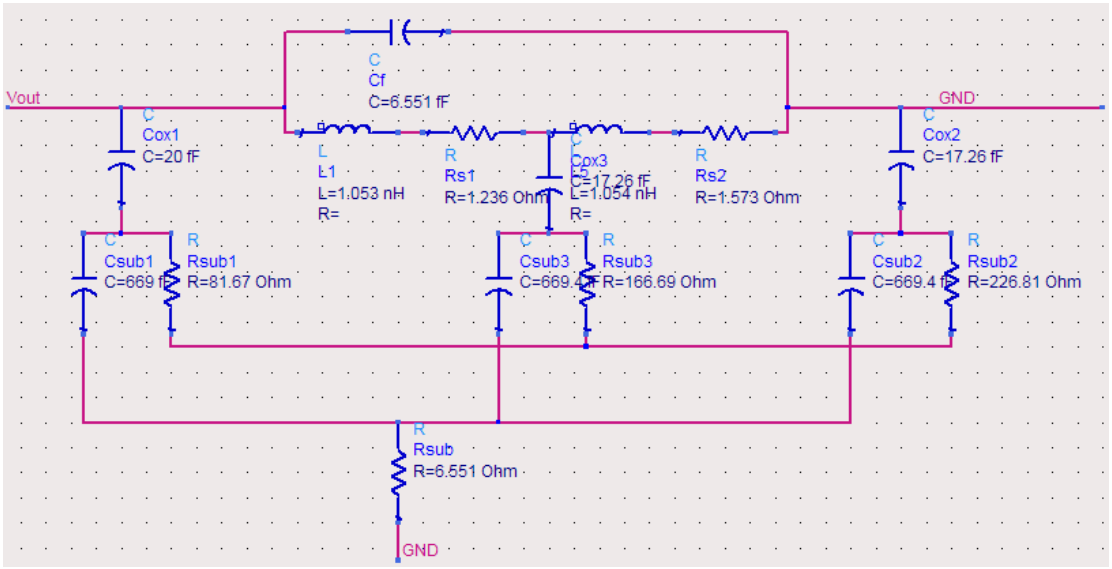
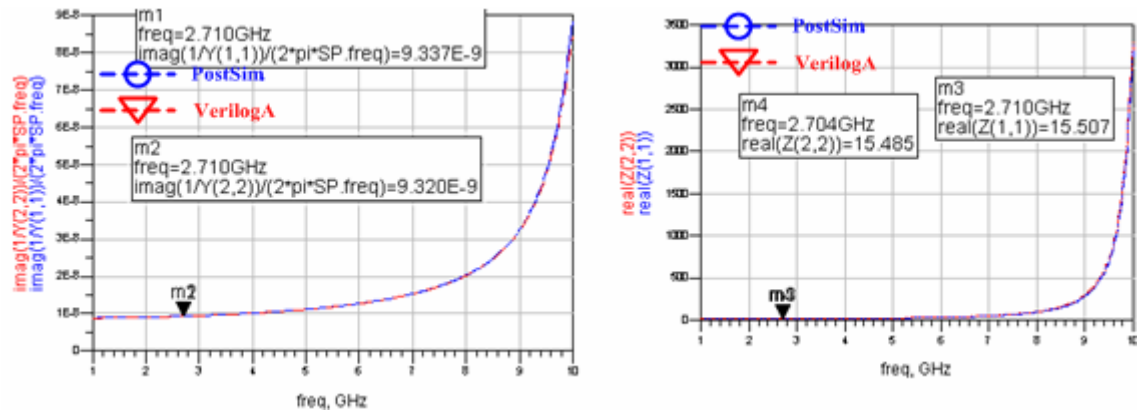


Figure 4. 11 The Inductor model.



(a) (b)

Figure 4. 12 Inductor model simulation results: (a) imagine part, (b) real part.

4.3.3 Transconductance Stage

VCO oscillates for constant transconductance and coverages to steady state while the transconductance equals to the LC tank resistance. The transconductance versus the output amplitude is shown in Fig.4.13, where R_p represents the LC tank resistance. The Verilog-A code is shown in Figure 4.14. Noise source is also added in the transconductance stage to model the phase noise, as shown in Figure 4.15.

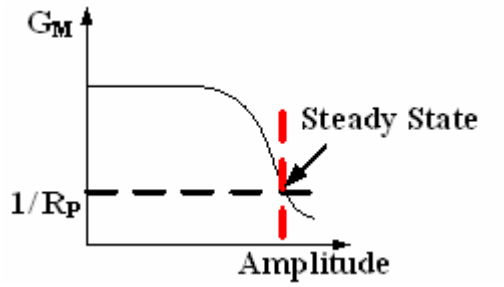


Figure 4. 13 The transconductance versus the output amplitude.

```
if ( abs(V(in, gnd)) > Vsat )
   temp1 = gm_DC+(((1/Rp)-gm_DC)/(Vmax-Vsat))*(abs(V(in))-Vsat);

if ( abs( V(in, gnd) ) <= Vsat )
   temp1 = gm_DC;
```

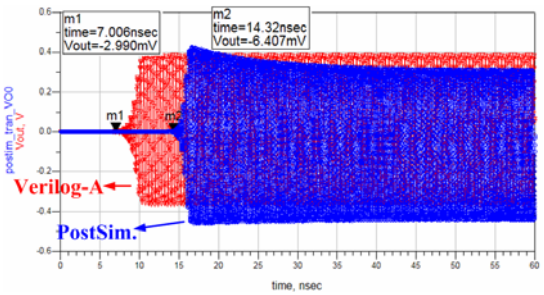
Figure 4. 14 The transconductance Verilog-A code.

```
I(out, gnd) <+ temp1*V(in, gnd)+noise_table({1e2, 1e-12, 1e3, 1e-15,1e4, 1e-16,1e5, 1e-17, 1e6,1e-22});
```

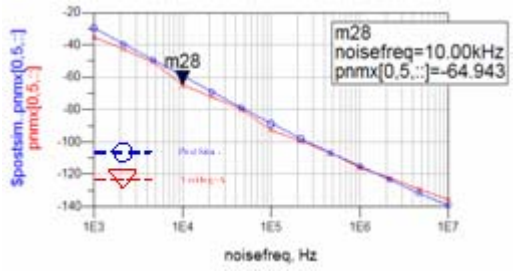
Figure 4. 15 Noise source Verilog-A code.

4.3.4 Simulation Results

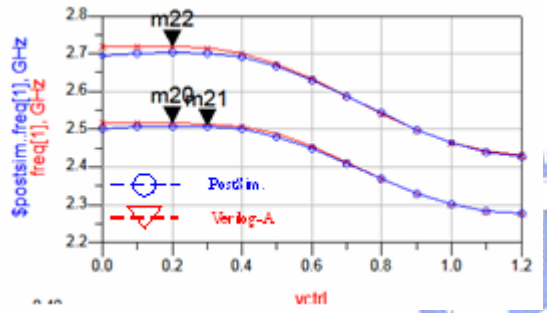
There is very small current (~nA) injected into to VCO output to set the initial condition while running simulation. Fig.4.16 shows the simulation results of transient,



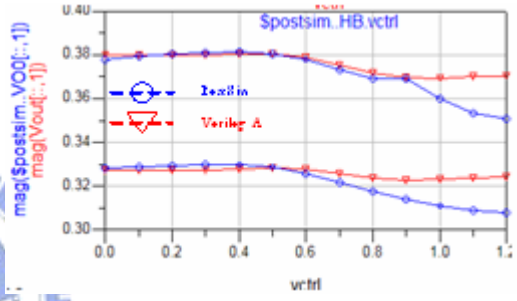
(a)



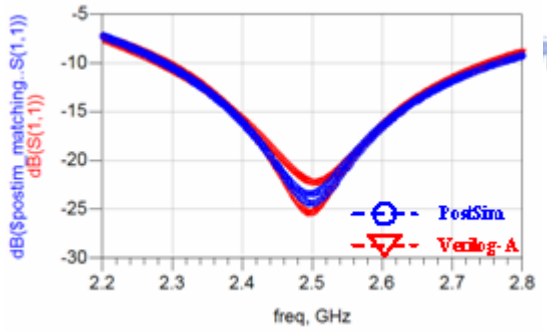
(b)



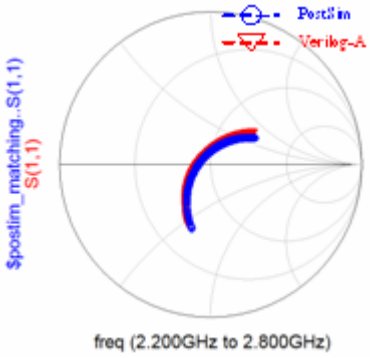
(c)



(d)



(e)



(f)

	(b)	(c)	(d)	(e)	(f)
RMSE	3.15dB	9.21MHz	50.7mV	0.44dB	0.014 Ω/0.05 Ω (real/imag)

Figure 4. 16 Simulation results : (a) transient, (b) phase noise, (c) oscillation frequency versus control voltage, (d) output power versus control voltage, (e) output matching in magnitude and (f) output matching smith chart.

harmonic and output matching. In Fig.4.16(a), behavior model starts to oscillate about 7ns earlier than post-simulation result. Simulation time of post-simulation and behavioral model is listed in Table 4.5.

Table 4.5 Comparison of simulation time (second).

	Transient	Harmonic
Verilog-A	17	29.45
Post-Sim.	262	9549.73

Chapter 5
Conclusions and Future Works

5.1 Conclusions

The phase error of QVCO is analyzed with the common-mode model and efficient compensation circuit is proposed to alleviate the common mode phase error of the QVCO. The QVCO is implemented and oscillates from 2.21-GHz to 2.79-GHz. The phase noise is -122.3dBc/Hz at 1-MHz offset frequency at 2.63-GHz. With the compensation circuit, the QVCO phase error and image rejection ratio (IRR) are improved about 1.5 degrees and 4.7dB for 2.63-GHz carrier frequency, respectively.

VCO behavior model was built in Verilog-A. Harmonic simulation time can be saved by replacing transistor-level circuit with the behavioral model (300:1). The behavior model can be used for harmonic and transient simulation.

5.2 Future Work

Size variation in the compensation circuit still affects the bias point and changes the VCO characteristics. At low offset frequency, phase noise degrades for low impendence at the common-mode node. New architecture could be proposed to improve disadvantages.

VCO output power is not modeled exactly for the nonlinear transconductance characteristic, which can be analyzed in detail to improve the behavioral model accuracy.

Appendix

A.1 Phase error derivation

The tank impendence frequency characteristic is shown is Figure A.1. As common-mode nodes oscillate at second-harmonic frequency, (2.8) can be derived as (A.1).

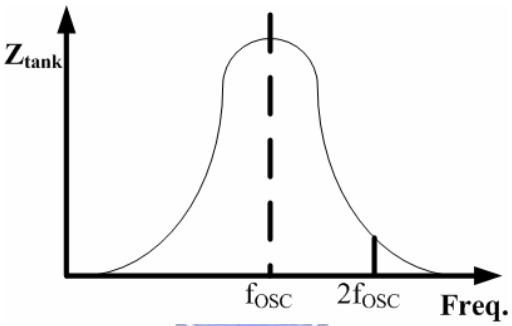


Figure A.1 Tank impendence characteristic.

$$\left|Z_{\tan k}(jf)\right| = \frac{Z_{f_{OSC}}}{\sqrt{1+jQ[\frac{f}{f_{OSC}}-\frac{f_{OSC}}{f}]}} \tag{A.1}$$

$$VCM_{I\_2\omega_{OSC}} = \frac{\frac{1}{2}VDM_{I\_\omega_{OSC}}}{\sqrt{1+jQ(\frac{\omega}{\omega_{OSC}}-\frac{\omega_{OSC}}{\omega})}} \tag{2.8}$$

Thus (2.7) can be modified as (A.2).

$$\begin{aligned}\Delta V = VCM_I - VCM_Q &\tilde{=} \left(-1+\frac{\Delta G_{Mc}}{2G_{McI}}+\left[\frac{G_{McQ}}{G_{McI}}\right]^{\frac{1}{2}}+(\frac{\varepsilon}{2})\cdot(\frac{G_{MI}}{G_{McI}})\right)\cdot VCM_I \\ &= \frac{0.5VDM_I}{\sqrt{1+1.5Q^2}}\left(-1+\frac{\Delta G_{Mc}}{2G_{McI}}+\left[\frac{G_{McQ}}{G_{McI}}\right]^{\frac{1}{2}}+(\frac{\varepsilon}{2})\cdot(\frac{G_{MI}}{G_{McI}})\right)\end{aligned} \tag{A.2}$$

As $d\theta = \int \Delta\omega\, dt == \int (2\pi \cdot K_{VCO} \cdot \Delta V)\, dt$, the magnitude error in common-mode results in frequency shift and phase error. Thus the phase error can be derived, as (A.3).

$$d\theta_{2nd\_osc} = \frac{Q}{m^2}\cdot\frac{d\omega}{\omega_{osc}} = \frac{Q}{m^2}\cdot\frac{1}{\omega_{osc}}\cdot 2K_{VCO}\cdot\frac{0.5VDM_I}{\sqrt{1+1.5Q^2}}\cdot\left(-1+\frac{\Delta G_{Mc}}{2G_{McI}}+\left[\frac{G_{McQ}}{G_{McI}}\right]^{\frac{1}{2}}+(\frac{\varepsilon}{2})\cdot(\frac{G_{MI}}{G_{McI}})\right)$$

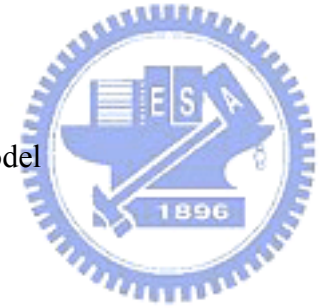
$$=\frac{K_{VCO\_instant}VDM_I}{3m^2\omega_{osc}}\cdot\left(-1+\frac{\Delta G_{Mc}}{2G_{McI}}+\left[\frac{G_{McQ}}{G_{McI}}\right]^{\frac{1}{2}}+(\frac{\varepsilon}{2})\cdot(\frac{G_{MI}}{G_{McI}})\right)\cong\frac{K_{VCO\_instant}VDM_I}{3m^2\omega_{osc}}\cdot\left(\frac{\Delta G_M}{2G_{McI}}+(\frac{\varepsilon}{2})\cdot(\frac{G_{MI}}{G_{McI}})\right) \quad (A.3)$$

A.2 Verilog-A code

```
// Varactor Model
//

`include "constants.vams"
`include "disciplines.vams"

module veriloga_varactor_0103(p, n);
        inout p, n;
        electrical p, n;
        parameter real c0 = 0.5e-12 from (0:inf);       // nominal capacitance (F)
        parameter real v0 = 0.463;                      // voltage for nominal capacitance (V)
        parameter real c1 = 0.40268e-12 from [0:inf);       // maximum capacitance change
from nominal (F)
        parameter real v1 = 0.537 from (0:inf);         // voltage change for maximum
capacitance (V)
        parameter real c2 = 0.13718e-12 from [0:inf);       // maximum capacitance change
from nominal (F)
        parameter real v2 = 0.263 from (0:inf);         // voltage change for maximum
capacitance (V)
        real q, v;


    analog begin
            v = V(p,n);
            if (v>v0)
                //q = c0*v + c1*v1*ln(cosh((v - v0)/v1));
                q = c0*v + c1*v1*ln(cosh((v - v0)/v1));
```

```
            if (v<=v0)
                //q = c0*v + c2*v2*ln(cosh((v - v0)/v2));
                q = c0*v + c2*v2*ln(cosh((v - v0)/v2));

             I(p, n) <+ ddt(q);
        end
endmodule




// Inductor Model
//

`include "constants.vams"
`include "disciplines.vams"

module veriloga_inductor(n1, n5, n11);

    inout n1, n5, n11;
    electrical n1, n5, n11;
    parameter real    Cox1 = 20e-12 from [0:inf);
    parameter real    Cf = 6.551e-15 from [0:inf);
    parameter real    L1 = 1.053e-9 from [0:inf);
    parameter real    Rs1 = 1.236 from [0:inf);
    parameter real    Cox3 = 17.26e-15 from [0:inf);
    parameter real    Rs2 = 1.573 from [0:inf);
    parameter real    L2 = 1.054e-9 from [0:inf);
    parameter real    Cox2 = 17.26e-15 from [0:inf);

    parameter real    Csub1 = 669e-15 from [0:inf);
    parameter real    Rsub1 = 81.67 from [0:inf);
    parameter real    Csub2 = 669.4e-15 from [0:inf);
    parameter real    Rsub2 = 226.81 from [0:inf);
    parameter real    Csub2 = 669.4e-15 from [0:inf);
    parameter real    Rsub2 = 166.69 from [0:inf);
    parameter real    Rsub = 6.551 from [0:inf);

analog begin
```

```
    I(n1,n5) <+ Cf*ddt(V(n1,n5)) + V(n4,n5)/Rs2;
    V(n1,n3) <+ L1*ddt(I(n1,n2)) + Rs1*I(n2,n3);
    V(n3,n5) <+ L2*ddt(I(n3,n4)) + Rs2*I(n4,n5);

    I(n1,n6) <+ Csub1*ddt(V(n6,n10))+V(n6,n9)/Rsub1;
    I(n3,n7) <+ Csub3*ddt(V(n7,n10))+V(n7,n9)/Rsub3;
    I(n5,n8) <+ Csub2*ddt(V(n8,n10))+V(n8,n9)/Rsub2;

    I(n10,n11) <+
Csub1*ddt(V(n6,n10))+Csub3*ddt(V(n7,n10))+Csub2*ddt(V(n8,n10));

    end
endmodule
```



```
//Transconductance stage    model

`include "constants.vams"
`include "disciplines.vams"


module veriloga_Gm_0103(gnd, in, out);
inout gnd;
input in;
output out;
electrical gnd, in, out;
parameter real Gm_eq = 0;
parameter real gm_DC = -4e-3;
parameter real Rp = 1e3;
parameter real Vmax = 0.4;
parameter real Vsat = 0.15;

real temp1, temp2;

analog begin
```

```
   if ( abs(V(in, gnd)) > Vsat )
        temp1 = gm_DC+(((1/Rp)-gm_DC)/(Vmax-Vsat))*(abs(V(in))-Vsat);

   if ( abs( V(in, gnd) ) <= Vsat )
        temp1 = gm_DC;

     I(out, gnd) <+ temp1*V(in, gnd)+noise_table({1e2, 1e-12, 1e3, 1e-15,1e4,
1e-16,1e5, 1e-17, 1e6,1e-22});

end

endmodule
```

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1. Han-Jian Lee, Che-Sheng Chen, Wen-Shen Wuen and Kuei-Ann Wen, “A Mismatch Compensation Circuit for CMOS Quadrature VCO Phase Error,” accepted by 2007 International Symposium on Signals,Systems, and Electronics (ISSSE 2007), Montréal CA, Apr. 2007.

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