國　立　交　通　大　學

電子工程學系　電子研究所碩士班

碩　士　論　文

具有四相位電壓控制震盪器用在超寬頻帶頻率合成器的互補式金氧半導體鎖相迴路

CMOS Phase Lock Loop with Quadrature Voltage-Controlled Oscillator for Ultra Wide Band (UWB) Frequency Synthesizer

研 究 生：許晏維

指導教授： 吳重雨　博士

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研究生： 許晏維　　Student: Yen-Wei Hsu

指導教授：吳重雨 博士　　Advisor: Dr. Chung-Yu Wu

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摘要

具有超寬操作頻率高傳輸速率由 IEEE 802.15 TG3a 制定的超寬頻通訊系統已被視為次世代通訊系統的主軸。在最近幾年，7128-MHz 附近的頻帶中，已有 7.5-GHz 的頻寬由美國國家通訊委員會(FCC)釋出作為高速短距離通訊系統使用。此頻帶具有可應用在高達數百-百萬位元等級的高傳輸速率無線個人網路(WPAN)以及點對點傳輸的潛力.

此論文中介紹了一個應用在超寬頻帶的全頻帶頻率產生的系統結構和其中的一個有兩級環式震盪器的鎖相迴路電路實現。此全頻帶頻率產生的系統中包含了使用最少數目的 SSB 混波器、統一的輸出級以及兩個固定除數的鎖相迴路等電路並且使用了 0.13-um CMOS 技術來設計。藉由使用兩級的環式震盪器，所需要的操作頻率不需要額外的電路而可以容易的達到，且環式震盪器具有高度的整合性。進一步來說，在 IC 中它可以節省更多的功率消耗和晶片面積。本電路的輸出相位雜訊在 1 MHz 偏差下是 -117.6 dBc/Hz 而功率頻譜是-0.313 dBm。在 1.2-V 的電源下，當震盪器輸出在所需的頻率 7128 MHz 時，其直流的功率消耗是 12.42 mW。而頻率可以調整的範圍在控制

電壓 1.1 V~0.1 V 時，是 5.8 GHz~8.8 GHz。

除了震盪器電路，除頻器電路是在不同的操作頻率下選擇不同的的電路架構以節省功率的消耗。而相位頻率偵測器是使用一般的結構並且在操作頻率 500 MHz 以下都可以正確的工作。而充電幫浦的充放電流不匹配比率在控制電壓 1.1 V~0.1 V 時，都在 4 %以下。最後的迴路濾波器是由國家半導體提供的程式來設計的二階濾波器，並由 Matlab 寫的程式來做二次驗證已求其相位極限(phase margin)大於 60 度。在預估輸出負載在 100 fF 下，整個鎖相迴路所消耗的功率大約是在 29 mW，頻道內的突波抵抗程度是-53dBc。

CMOS Phase Lock Loop with Quadrature Voltage-Controlled Oscillator for Ultra Wide Band (UWB) Frequency Synthesizer

Student: Yen-Wei Hsu Advisor: Dr. Chung-Yu Wu

Department of Electronic Engineering &
Institute of Electronics
National Chiao Tung University

Abstract

In the next-generation wireless communication as UWB applications, high data rate transmission with a wide operating frequency spectrum is expected to be realized by 802.15.3a Task Group specification. Over the past few years, the 7.5-GHz frequency spectrum divided into 14 bands around 7128 MHz has been released by FCC for unlicensed use in high-speed and short-range communication systems. It has great potential in application of high data-rate wireless personal–area network (WPAN), high speed WLAN and point-to-point link, with possible data rate of hundreds of megabits per second.

In this thesis, a full-band frequency spectrum generation scheme for UWB applications and a phase lock loop with two-stage ring oscillator are presented. The proposed full-band

frequency spectrum generation scheme which consists of the least single-side-band mixers, a unified output port, and two division-number fixed PLL. The higher output frequency PLL is designed by using 0.13-um CMOS technology. Utilizing a two-stage ring oscillator, the operating frequency of the PLL can be achieved effortlessly without other circuit component. It also has high integration for ICs. Furthermore, it saves more power consumption and chip area in integrated circuits. The output phase noise of the oscillator is -117.6 dBc/Hz at 1 MHz offset and the power spectrum is -0.313 dBm. The power consumption of the two-stage ring oscillator is 12.42 mW from 1.2-V power supply at the required output frequency 7128 MHz. The tuning range of the oscillator is 5.8 ~8.8 GHz under 1.1~0.1 control voltage.

Besides oscillator, the divides are chosen different architectures for different operation frequencies to economize on power consumption. Phase and frequency detector is using the conventional structure that cost small power consumption and could function correctly under operation frequency 500 MHz. The mismatching ratio of the proposed current-match charge pump is 4 % under the control voltage 0.1V~1.1V. Finally, the loop filter is designed by the loop filter design software from National Semiconductor as second order structure and double check with Matlab code to let the phase margin higher than 60 degrees. The overall power consumption of the proposed PLL is around 29 mW at estimation output loading 100 fF. The in band spur rejection is -53 dBc.

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Chapter 1
Introduction

1.1 Background

Over the past few decades, wireless communication systems have been under significant development and are more closely related to our daily life than ever before. In the digital home of the not-too-distant future, people will be sharing photos, music, video, data and voice among networked consumer electronics, PCs and mobile devices throughout the home and even remotely. Users will be able to stream video content from a PC or consumer electronics (CE) device -- such as a camcorder, DVD player or personal video recorder -- to a flat screen HDTV (high-definition television) display without the use of any wires.

A leading candidate for enabling this capability is ultra wideband (UWB), a wireless technology designed for high data-rate and low power consumption.

Traditional radio transmissions have a significant difference between UWB radio transmissions. It is that traditional systems transmit information by varying the power level, frequency, and/or phase of a sinusoidal wave. UWB transmissions transmit information by generating radio energy at specific time instants and occupying large bandwidth thus enabling a pulse-position or time-modulation. UWB pulses can be sent sporadically at relatively low pulse rates to support time/position modulation, but can also be sent at rates up to the inverse of the UWB pulse bandwidth. Pulse-UWB systems have been demonstrated at channel pulse rates in excess of 1.3 giga-pulses per second using a continuous stream of UWB pulses, supporting forward error correction encoded data rates in excess of 675 M bit/s.

One of the valuable aspects of UWB radio technology is the ability for a UWB radio system to determine "time of flight" of the direct path of the radio transmission between the transmitter and receiver at various frequencies. This helps to overcome multi path propagation, as at least some of the frequencies pass on radio line of sight. With a cooperative symmetric two-way metering technique distances can be measured to high resolution as well as to high accuracy by compensating for local clock drifts and stochastic inaccuracies.

Another valuable aspect of pulse-based UWB is that the pulses are very short in space (less than 60 cm for a 528 MHz wide pulse, less than 23 cm for a 1.3 GHz bandwidth pulse), so most signal reflections do not overlap the original pulse, and thus the traditional multipath fading of narrow band signals does not exist. However, there still is multipath propagation and inter-pulse interference for fast pulse systems which can be mitigated by coding techniques.

Ultra-Wideband (UWB) may be used to refer to any radio technology having bandwidth exceeding the lesser of 528 MHz or 20% of the arithmetic center frequency, according to Federal Communications Commission (FCC). A Report and Order by the FCC authorizes the unlicensed use of UWB in 3.1–10.6 GHz. The FCC power spectral density emission limit for UWB emitters operating in the UWB band is -41.3 dBm/MHz. This is the same limit that applies to unintentional emitters in the UWB band, the so called Part 15 limit [1].

Deliberations in the International Telecommunication Union Radiocommunication Sector (ITU-R) have resulted in a Report and Recommendation on UWB in November of 2005. National jurisdictions around the globe are expected to act on national regulations for UWB very soon. Other national regulatory bodies apparently are somewhat reluctant to allow common unlicensed use. More than four dozen devices have been certified under the FCC rules, the vast majority of which are radar, imaging or locating systems. UWB is making the transition from laboratories to standardization, a key step toward the development of

real-world products. The brief summary and comparisons of the UWB application and other communication standards are listed in the Table 1.1 below.

Table 1.1 The summary and comparison of the UWB application and other communication standards.

	UWB	WiFi	WiMax	Bluetooth
Data rate (bits/sec)	480 M	<54 M	<70 M	<1 M
Bandwidth (GHz)	3.1~10.6	2.4	3~11	2.4
Transmission distance (m)	<20	<100	<70k	<10

It is a tough task to grasp the analog and high frequency character in RF circuit design. Much more problems and issues we are facing than we expected. We all need to pay more efforts and time to get advancement. Through this way, we can make the world more convenient and comfortable as well as the motivation of our endeavors.

1.2 Reviews of MB-OFDM UWB Synthesizer

A frequency synthesizer is an electronic system for generating any of a range of frequencies from a single fixed oscillator. They are found in many modern devices, including radio receivers, mobile telephones, radiotelephones, walkie-talkies, CB radios, satellite receivers, GPS systems, etc.

Frequency synthesizers used in commercial radio receivers are largely based on phase-locked loops or PLLs. Many types of frequency synthesizer are available as integrated circuits, reducing cost and size. High end receivers and electronic test equipment use more sophisticated techniques, often in combination.

A phase locked loop does for frequency what the Automatic Gain Control does for voltage. It compares the frequencies of two signals and produces an error signal/frequency which is proportional to the difference between the feedback frequency and reference/input frequency. The error signal is used to drive a voltage-controlled oscillator (VCO) which creates an output frequency. The output frequency is fed through a frequency divider back to the input of the system, producing a negative feedback loop. If the output frequency drifts, the error signal will increase, driving the frequency in the opposite direction so as to reduce the error. Thus the output is locked to the frequency at the other input. This input is called the reference and is derived from a crystal oscillator, which is very stable in frequency. Fig 1.1 below shows the basic elements and arrangement of a PLL based frequency synthesizer.

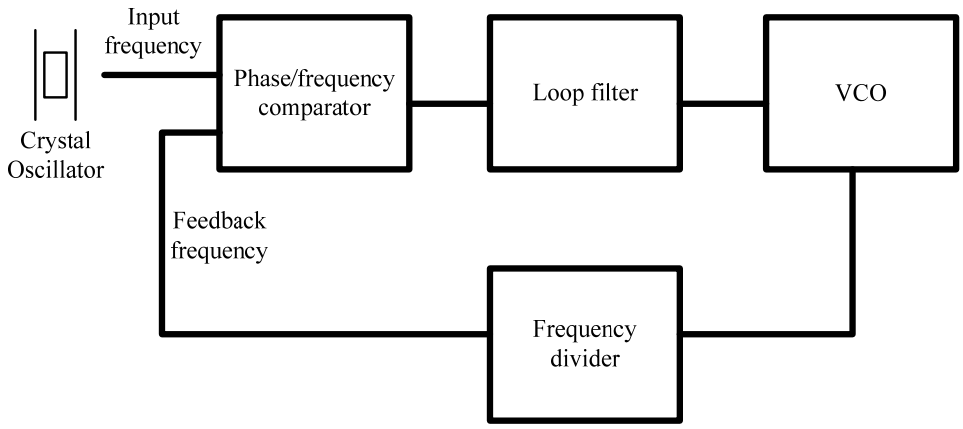


Figure 1.1 The architecture of the phase lock loop

However, in MB-OFDM UWB system, it is somehow different from the above mentioned narrow band synthesizer. As a result, the wide operating bandwidth over 3.1~10.6

GHz and fast switching time less than 9.47ns (that will be mentioned at chapter 2) cannot be attained by only one PLL. It is supposed to have a wideband character or multiple switched circuits used to work at various frequency bands, and more than one single carrier frequency is required in the receiver and transmitter. Besides, we cannot ignore the out-of-band distortion that should be taken into consideration and analyzed.

By carefully investigating the UWB frequency synthesizer, the frequency switching time is the most difficult issue. How to let the frequency band change to the other frequency band cannot be solved only tuning the PLL's output frequency. That is because the settling time of PLL is much more than 9.47ns. One of the solutions is to construct as many PLLs as the frequency bands you use [2], [3] as figure 1.2 circumscribed below. However, as the frequency bands extending and frequency planning groups growing, it is costly and impractically in many applications. Some recently published works have been designed based on many frequency bands and less chip space. They will be discussed in subsequent sections.

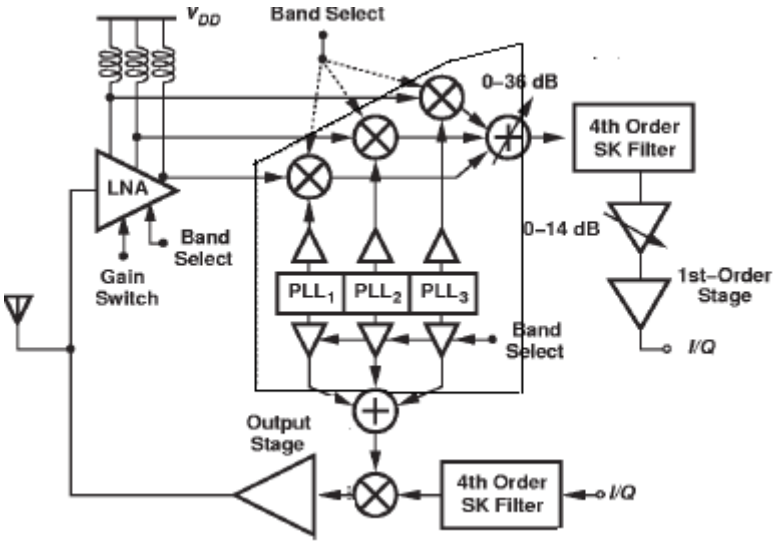


Figure 1.2 The architecture of the many PLLs as each band's synthesizer

1.2.1 UWB Synthesizers

As UWB synthesizer is evolving continuously, several main architectures have been generalized. These architectures are mainly toward full-band frequency synthesizer that may be extended to or already achieve the goal. Be sure that the complete frequency synthesizer of UWB system should be the quadrature phase output. The followings are representative reviews of the state-of-the-art UWB frequency synthesizers.

- A 3-to-8-GHz Fast Hopping Frequency Synthesizer [4]

This paper has accomplished a 9-band (the whole bands is 14) frequency synthesizer, and it provide an architecture that can extend to achieve a full-band frequency synthesizer. The frequency planning rules will be clearly explained and analyzed in the chapter 2. Please allow me analyzing the paper's frequency planning algorithm first. The following figure 1.3 is the architecture that how it achieve the full-band frequency planning.

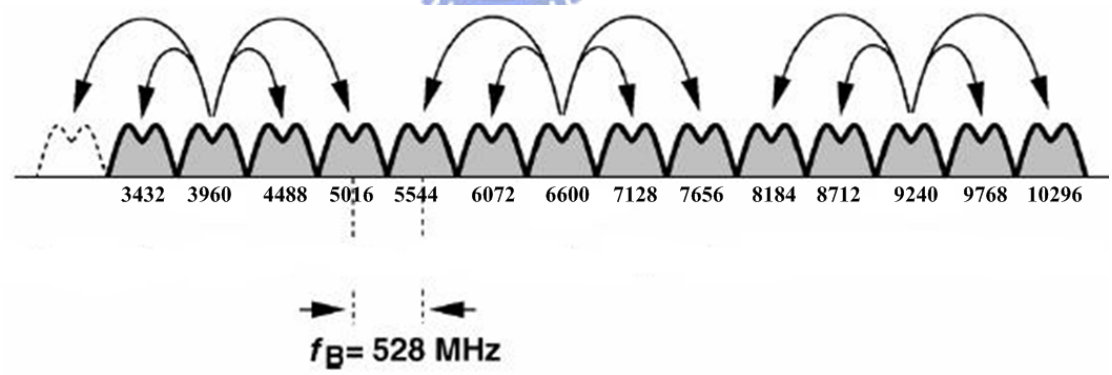


Figure 1.3 The block diagram of the [4]'s full-band frequency planning

Its idea is to generate three basic bands by the first circle. Then generate the spacing frequency (528 MHz) and double spacing frequency (1056 MHz). From the basic frequency, it can extend to upper or lower frequency bands by adding or subtracting the one or double spacing frequency to cover the 14 bands. The realization of circuit block diagram is in the

following figure 1.4.

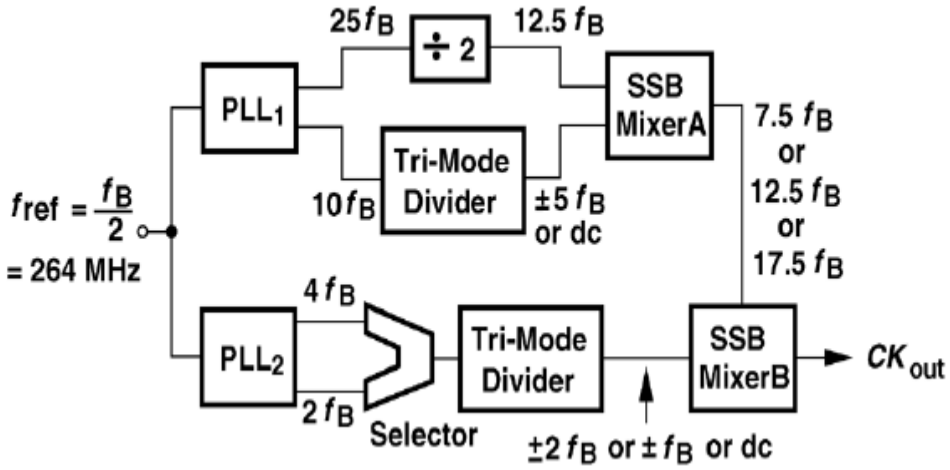


Figure 1.4 The circuit block diagram of [4]

As you see in figure 1.4, the first PLL's output signals through the divide-by-2 or tri-mode divider generate the signal $12.5f_B$ and the $\pm 5f_B$ (f_B is 528 MHz). Then the two signals through the single-side-band MixerA produce the three basic bands in the figure 1.3 ($7.5f_B$=3960 MHz, $12.5f_B$=6600 MHz, $17.5f_B$=9240 MHz). The second PLL generates the two signals $4f_B$ and $2F_B$. By frequency selector and tri-mode divider, the signals become the one, double or dc spacing frequencies ($\pm 2f_B$=$\pm$ 1056 MHz, $\pm f_B$=$\pm$ 528 MHz or dc=0 MHz) called extending frequency. Finally, through single-side-band MixerB, the basic bands and the extending frequency can cover the full-band of the UWB specifications.

The disadvantage of this architecture is the divide-by-2.5 in the first PLL hard to implement at first. Second, the single-side-band MixerB must operate over very wide frequency (from 3960 to 9240 MHz basically). It's difficult to realize the circuit single-side-band MixerB by TSMC 0.18 μm processing technology. Because of that, this paper only implements only the two basic bands that cover 3 to 8 GHz.

■ A 14-band Frequency Synthesizer for MB-OFDM UWB Application [5]

This paper is the first implementation of the full-band frequency synthesizer by CMOS 0.18 μm process. We will first describe the frequency planning algorithm, and then analyze the block diagram of the circuit implementation. The following figure 1.5 is the architecture that how it achieve the full-band frequency planning.

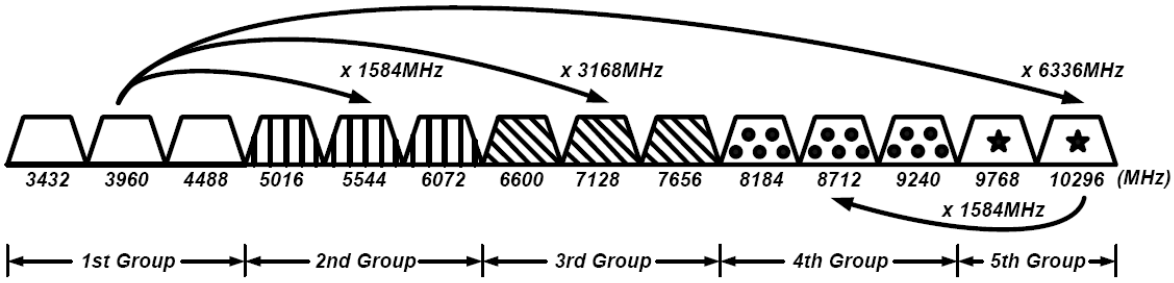


Figure 1.5 The block diagram of the [5]'s full-band frequency planning

Its idea is to generate the fundamental band at 3960MHz of the 1st Group. Then we generate the extending frequencies 1584 MHz, 3168 MHz, 6336 MHz as extending frequency A, 528 MHz as extending frequency B, and extra 1584 MHz as extending frequency C. The fundamental band can extend to cover 1st Group by extending frequency B, or cover 2nd, 3rd or 5th Group by using extending frequency B first and then using extending frequency A. Finally, it can cover the 4th Group by using extending frequency B first, then using extending frequency A, and extending frequency C at last. For example, if you want to get the frequency band 8184 MHz, you should let the fundamental band subtract the extending frequency B (528 MHz) as band 3432 MHz first. Second, the band 3432 MHz adds the extending frequency A (6336 MHz) as 9768 MHz. Finally, the band 9768 MHz subtracts the extra extending frequency C (1584 MHz) to the band 8184 MHz we expect.

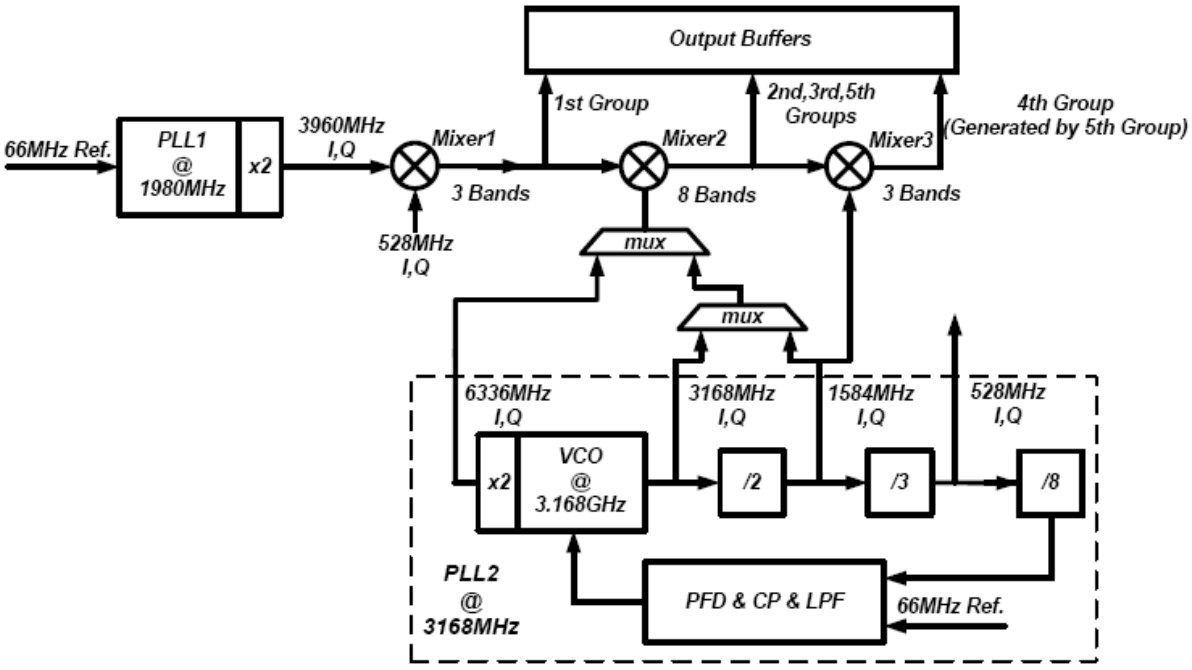


Figure 1.6 The circuit block diagram of [5]

The circuit block diagram realization is on the above figure 1.6. It generates the fundamental band (3960 MHz) by the first PLL and the other extending frequencies are generated by PLL2. By using the single-side-band (SSB) Mixer1, the 1st Group band frequencies would be achieved. The 2nd, 3rd, and 5th Group band frequencies would be produced through the SSB Mixer2 through the selection of the extending frequency chosen by the multiplexer. The last 4th Group band frequencies would be generated at the output of the last SSB Mixer3. That will cover the whole full-band frequency planning.

Although this paper's algorithm of frequency planning avoids the mixers operating at wide frequency range, the extra mixer is used. It costs more passive component wasting chip area and power dissipation. Mixers also generate the spurs at the in-band/out-band that let the spur specification worse. Further more, it increases the complexity of the circuit that the integration of the system would be more difficult.

■ A 1.5V UWB Frequency Synthesizer Design [6]

This thesis is the first implementation of UWB frequency synthesizer in our research group ICS LAB. It let the old specification of the UWB frequency planning realized by TSMC CMOS 0.18 μm process. Although the rules of UWB frequency planning are changed now, it still has the value of reference. There is the figure 1.7 of circuit block diagram below.

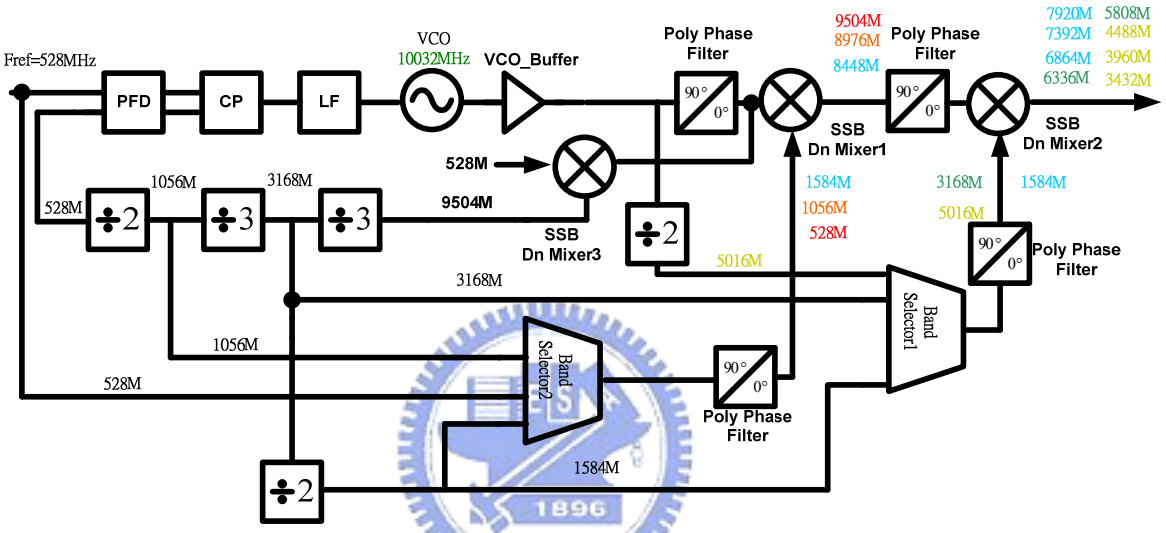


Figure 1.7(a) The circuit block diagram of [6]

The frequency planning algorithm is that only one PLL generates the highest frequency band (10032 MHz). Then it divides the highest frequency to other extending frequencies (9504 MHz, 3168 MHz, 1056 MHz, and 528 MHz). Through the SSB Mixer1 and SSB Mixer2, the whole frequency bands would be produced to cover the full-band frequency planning. The frequency generation is signed on the figure1.8 below.

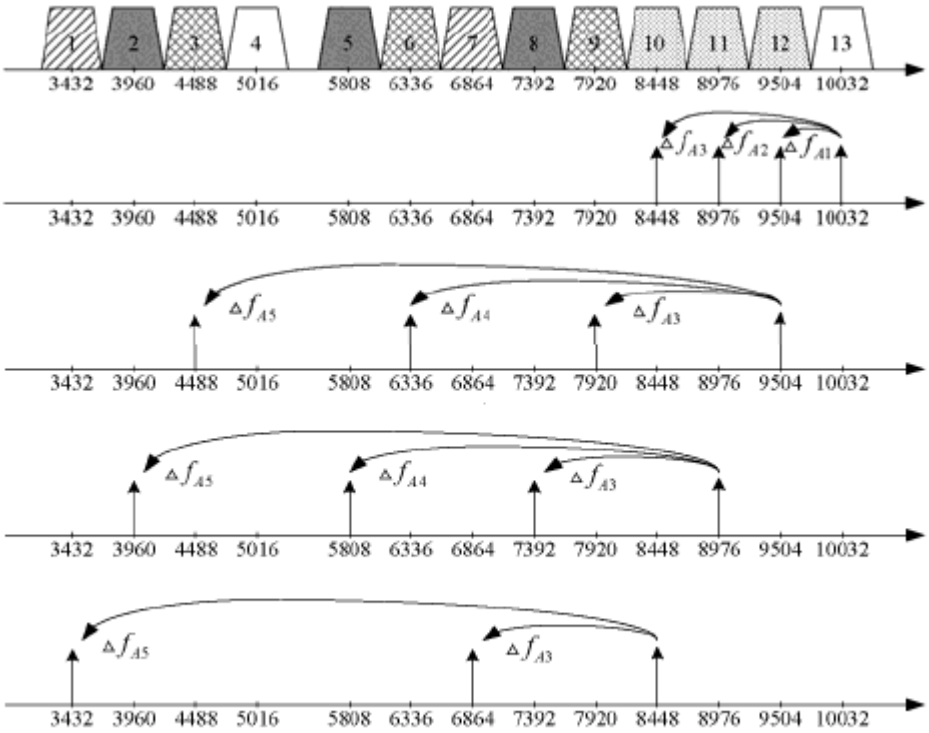


Figure 1.7(b) The diagram of the [6]'s full-band frequency planning

In order to cover the full-band planning, there is a mixer used in the PLL. It not only increases the risk of PLL's locking problem, but also generates the spurs in output of PLL. It both increases the chip area and the power consumption, and the complexity become great issues. The PLL's VCO is simple complementary LC tank structure that serves with only differential output signals not quadrature ones. It is forced to provide a poly phase filter to generate quadrature phase output. However, the poly phase filter is hard to design precisely that it cannot tolerate the frequency drifting from the VCO. The passive component of poly phase filter not only costs the area but also easily drifts in the chip process. There are three poly phase filter used in the architecture that may cause huge variations.

The architecture's output is not integrated to one that cannot be integrated to receiver or transmitter. Different outputs also hard to measure the switching time of changing the

frequency bands. There is still one point it didn't achieve that it is not a quadrature phase output. Transceiver is needed the quadrature phase output as LO signals. Although it is not perfect architecture, it only uses one PLL that saves a lot of chip area and power consumption.

■ A 3-to-10 GHz CMOS Frequency Synthesizer for MB-OFDM UWB system [7]

This paper is the second implementation of UWB frequency synthesizer in our research group ICS LAB. It is realized by the TSMC CMOS 0.18 μ m process. It completely covers the UWB full-band frequency planning. The following figure 1.8 is the full-band frequency planning diagram of it.

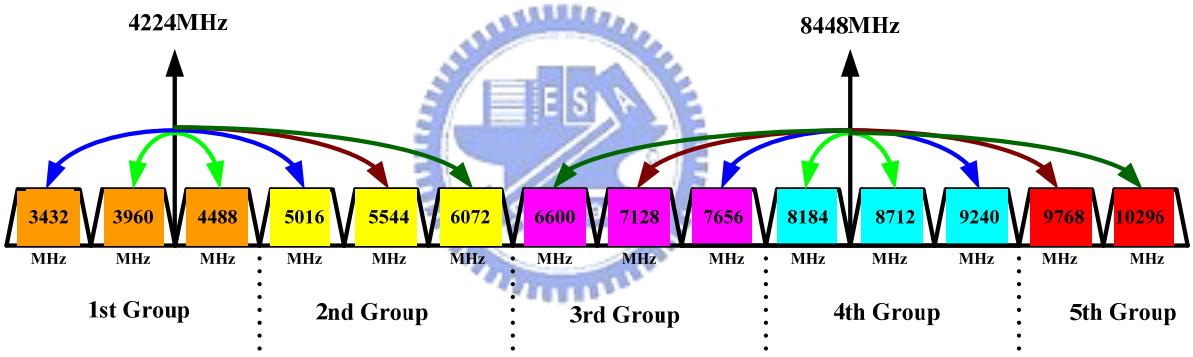


Figure 1.8 The block diagram of the [7]'s full-band frequency planning

Its idea is to generate the fundamental frequencies (not the central frequency bands in UWB specification) at 8448 MHz, and 4224 MHz. Then it generates the extending frequencies 1848 MHz, 1320 MHz, 792 MHz, and 264 MHz as extending frequencies. The two fundamental frequencies can extend to cover the whole full-band frequency planning by adding or subtracting the extending frequencies. For example, if you want to get the frequency band 7128 MHz, you should let the fundamental frequency 8448 MHz subtract the extending frequency 1320 MHz to the band 7128 MHz we expect.

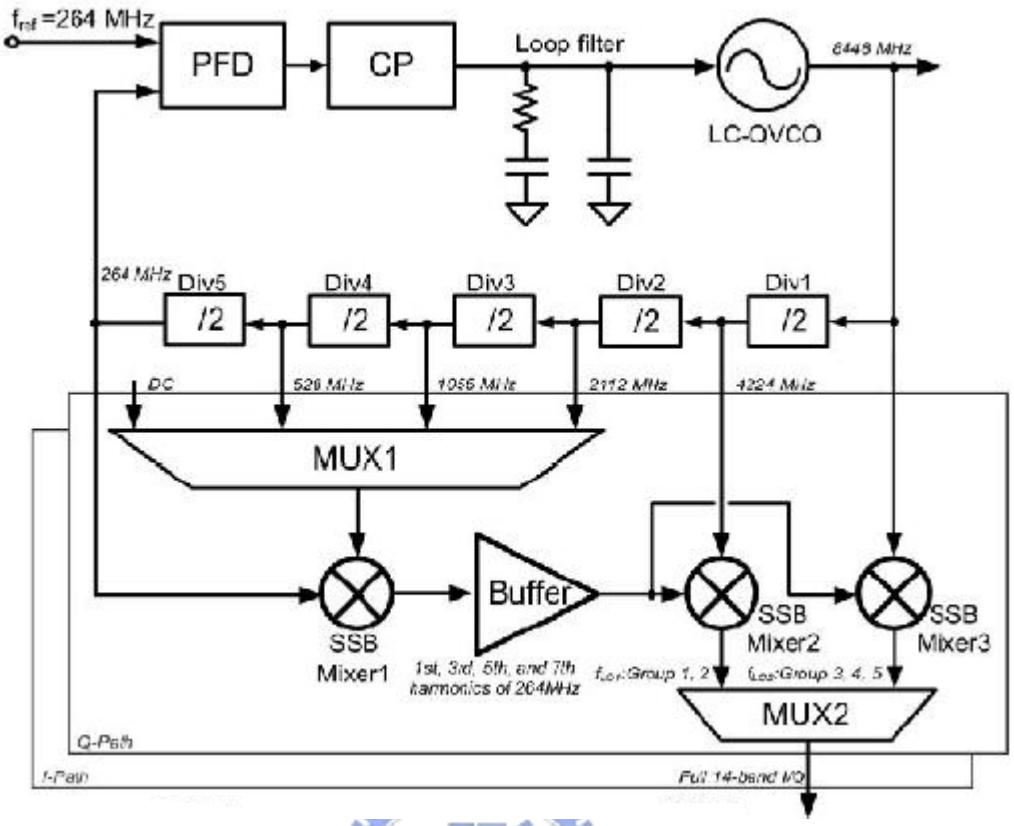


Figure 1.9 The circuit block diagram of [7]

The circuit block diagram realization is on the above figure 1.9. It generates the fundamental frequencies (8448 MHz, and 4224 MHz) by the output of PLL and the first divider-by-2 (Div1). Then the left dividers-by-2 (Div2~Div5) produce the other half frequencies each by each to get the signals 2112 MHz, 1056 MHz, 528 MHz, and 264 MHz. In order to produce the extending frequencies, we let the signals produced from dividers-by-2 circuits (Div2~Div5) add or subtract the reference frequency 264 MHz. We can get the extending frequencies 1848 MHz (2112 MHz-264 MHz), 1320 MHz (1056 MHz+264 MHz), 792 MHz (528 MHz+264 MHz), and the 264 MHz itself by using SSB Mixer1. The 1st Group and 2nd Group would be covered by the SSB Mixer2, and the 3rd Group, 4th Group, and 5th Group would be achieved by the SSB Mixer3. To get the quadrture phase output, the replica circuits (All the circuits besides PLL) should be constructed symmetrically as Q-path (Quadrature phase path) or I-path (In phase path).

The only disadvantage of this paper is the added mixer compared with other architecture. The affection it brought is as we mentioned in the second full-band architecture [5]. Although this, the paper still provides the best UWB full-band frequency synthesizer solution. No doubt the paper is chosen to publish in the IC's highest sanctuary, International Solid-State Conference 2008.

Well, the CMOS frequency synthesizers covering as much UWB bands as fewer circuit components attract more and more attentions. It is placed huge emphasis on low-chip-area, lower-power, and higher-integration applications. The trend is ongoing all the time.

1.3 Motivation

As mentioned above, some published frequency synthesizers for UWB applications have been developed and surveyed. These frequency synthesizers require huge amount of chip area to satisfy the UWB specification. They not only use a lot of passive elements but also waste extra circuit components. Using a high efficiency frequency planning architecture would thoroughly solve these difficult positions. The architecture of the frequency synthesizer for UWB full-band applications would try to realize in TSMC 0.13μm process under 1.2-V supply voltage. The constructing circuit components would consist of the phase-lock-loop with a quadrature two-stage ring oscillator without inductors to save space. The system simulation and the design reliability of phase-lock-loop would be considered carefully.

The frequency synthesizer is fulfilled to IEEE 802.15 TG3a specification, which specifies a frequency switching time less than 9.47ns as fast hopping. It basically must cover the 14 bands from 3.1~10.6 GHz, and have quadrature phase outputs.

1.4 Thesis Organization

Chapter 2 describes the detailed specification of IEEE 802.15 Task Group 3a, design consideration of the UWB frequency synthesizer, and the proposed a 3.1~10.6 GHz UWB full-band frequency synthesizer is introduced. In Chapter 3, the circuit components of the phase-lock-loop are considered: phase and frequency detector, charge pump, and two-stage quadrature ring oscillator. The system simulation of a phase-lock-loop is also brought up. The chapter 4 shows the implementation of the circuits in phase-lock-loop. The design consideration of each component would be illustrated and theoretic analyzed. It would be made together with simulation results. Finally, the conclusion and future work are presented in chapter 5.

Chapter 2

A 3.1~10.6 GHz CMOS Frequency Synthesizer

To get a thorough understanding of the UWB system, the physical layer proposal for IEEE 802.25.3a is introduced and analyzed. The system design consideration, the theoretical analysis, as well as architecture of the proposed frequency synthesizer are discussed and presented in chapter 2.

2.1 Multi-Band OFDM Physical Layer Proposal for IEEE 802.15 Task Group 3a

The IEEE 802.15 TG3a [8] specifies the unlicensed 3.1~10.6 GHz UWB band for short-range and high data-rate communications. The specified frequency width 7.5 GHz spectrum is divided into 5 groups and 14 bands with spacing 528MHz as shown below in figure 2.1.

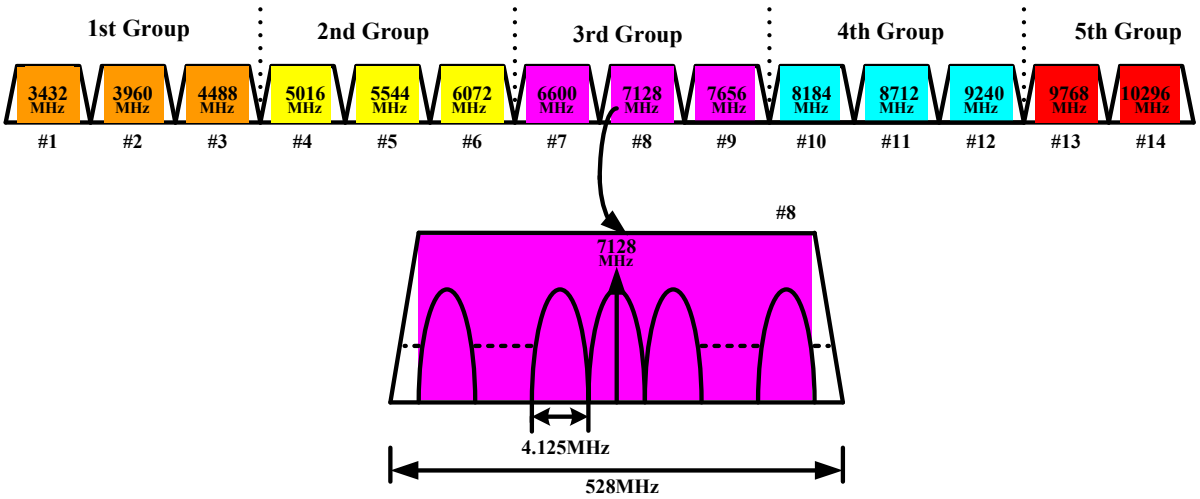


Figure 2.1 Frequency planning of MB-OFDM UWB systems

The band frequencies are given as follow: [9]

$$\text{Band central frequency} = 2904 + 528 \times N_b(MHz) \qquad N_b = 1.....14 \tag{2-1}$$

$$= 528 \times N_b'(\text{MHz}) \qquad N_b' = 6.5.....19.5 \tag{2-2}$$

where N_b represents band numbers, and N_b' represents the numbers of spacing frequency. Band #1~ Band #3 are used for Mode 1 application (mandatory mode), while Mode 1 and Band #6~ Band #9 are as Mode 2 application (optional mode). The remaining channels are reserved for future used. The UWB system provides a wireless PAN with data payload communication capabilities of 55, 80, 110, 160, 200, 320, and the fastest 480 Mb/s. It incorporates orthogonal frequency division multiplexing (OFDM) modulation using quadrature phase shift keying (QPSK), a technique that uses multiple carriers to mitigate the effect of multipath path fading. In order to satisfy the QPSK application, the signals in UWB system are different from conventional communication system. Quadrature phase signals must be applied in whole UWB system surely including frequency synthesizer.

The divided bands bandwidth is 528 MHz which is also divided into 128 sub-carriers resulting in a sub-carrier bandwidth is 4.125 MHz as shown in figure 2.1. Among the 128 sub-carriers, 100 tones carry payload data, 12 pilot tones facilitate coherent detection against frequency offset, 10 guard tones relax filter design and the other 6 null tones carry no information at all.

The MB-OFDM system adopts a frequency-hopping scheme to provide frequency diversity and multiple accesses. The performance of such MB-OFDM UWB architecture in multipath is fundamentally limited by the energy capture ability because when the TX/RX switches to demodulating the subsequent sub-band [9], [10], [11], it loses any ability to

capture the multipath dispersed energy from the current sub-band. Thus, in order to improve the energy capture, pulsed multiband UWB systems need slower time-frequency hopping, i.e., longer contiguous symbol transmissions in each sub-band. This has naturally led to OFDM instead of pure pulse modulation in each sub-band due to the former's inherent robustness to multipath.

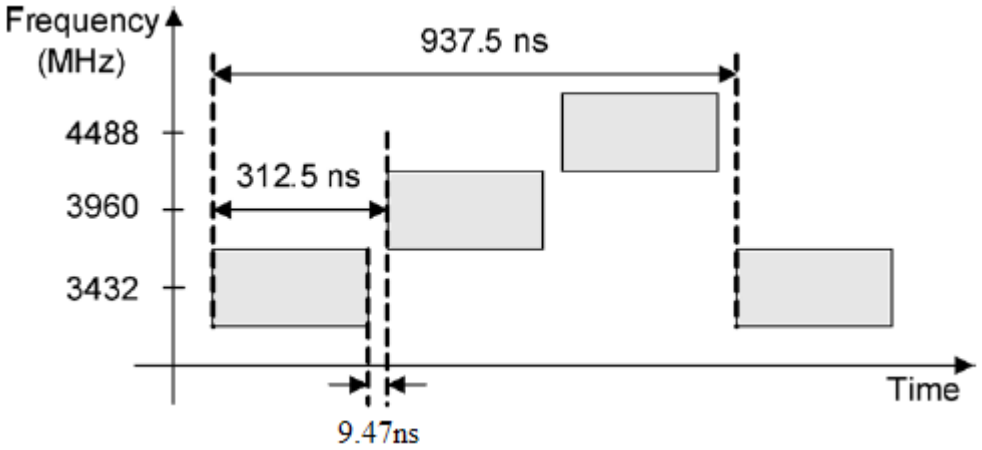


Figure 2.2 Frequency switching for each symbol of a MB-OFDM UWB burst

Multiple piconet coexistence is enabled in multiband UWB systems by introducing channelization via use of suitably designed frequency-hopping sequences over the set of sub-bands as in fig. 2.2 above—in principle, depending on the channel environment and desired data rates, the hop rate can be slow (multiple symbols sent on one sub-band prior to band switching) or fast (only one symbol sent per sub-band). The frequency-hopping sequences are designed to minimize "collision" events when two users in different piconets simultaneously use the same sub-band—such cases lead to erasure of the transmitted symbols. Thus, the number of simultaneously operating piconets that can be supported by this approach depends on the availability of frequency-hopping sequences with one coincidence property. A guard interval of 9.47ns (5/528MHz) is given as TX/RX switching time, which essentially specifies the maximum frequency synthesizer settling time when hopping between

multi-bands.

Therefore, we know the two essential factors for UWB frequency synthesizer different from the conventional synthesizer. That is the fast hopping time for the TX/RX switching time, 9.47ns, and the quadrature phase output signals for QPSK application as TX/RX LO signals.

2.2 Frequency Planning

The architecture of the frequency planning for UWB systems application is quite important. Our frequency planning for MB-OFDM UWB application provides a great improvement of decreasing the chip area and spurious response. This frequency generation scheme makes the third-order unwanted sidebands caused by mixing fall outside the 7.5 GHz spectrum so that the lower spur level is achieved. The third-order frequencies of spurious tones are given as:

$$f_1 = 3 \cdot f_{RF} - f_{LO} \quad \text{and} \quad f_2 = 3 \cdot f_{LO} - f_{RF} \tag{2-3}$$

where all the third-order spurious tones are out of the 7.5 GHz spectrum as fig 2.3 below.

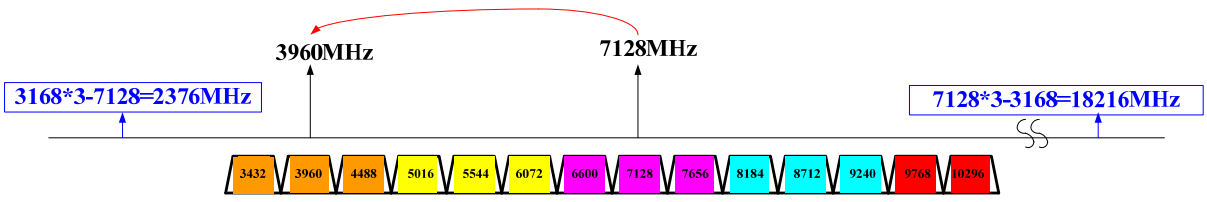


Figure 2.3 Third-order spurious tones are out of 7.5 GHz spectrum for UWB application

As a result of this, the better frequency planning we used, the less circuit components and system disadvantages are revealed. As we mentioned in chapter 1 section 2, the reviews of the UWB frequency synthesizers, all the frequency planning architecture published have the goals to achieve themselves. Some of them want to subtract the number of the too many PLLs to decrease the chip area, some want to reduce the spurious response by subtracting the number of the SSB mixers, and so on ….. Every frequency planning algorithm for UWB frequency synthesizers earns its benefits for their goals, but it also brings the imperfection affecting the other property. Therefore, how to be universally satisfied is a huge challenge to get over. The followings are the frequency planning diagram of the UWB frequency synthesizer.

2.2.1 Frequency Planning Architecture

The frequency planning diagram is to generate the fundamental band at 7128MHz of the 3rd Group. Then we generates the extending frequencies 1584 MHz, 3168 MHz as extending frequency A, and 528 MHz as extending frequency B. The fundamental band can extend to cover 3rd Group by extending frequency B, or cover 1st, 2nd, or 5th Group by using extending frequency B first and then using extending frequency A. It is quite uncomplicated and directly perceived through the senses as shown in fig 2.4 below.

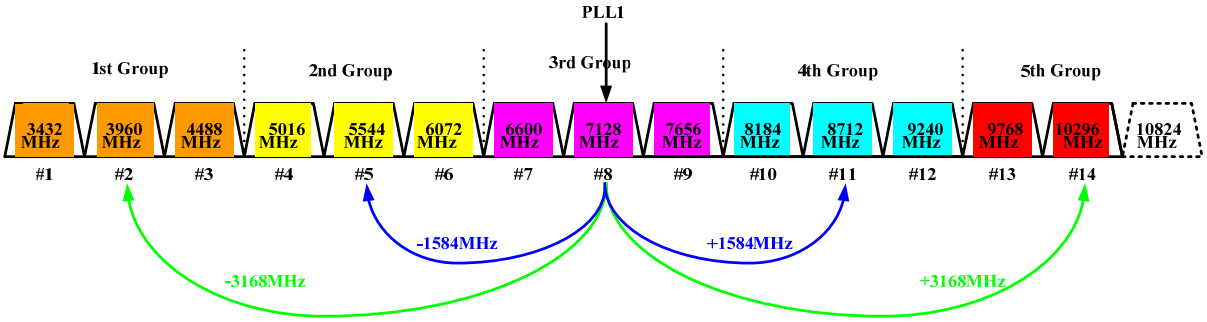


Figure 2.4 The block diagram of proposed frequency planning architecture for UWB applications

For example, if you want to get the frequency band 8184 MHz, you should let the fundamental band 7128MHz subtract the extending frequency B (528 MHz) as band 6600 MHz first. Second, the band 6600 MHz adds the extending frequency A (1584 MHz) to the band 8184 MHz we expected. All the frequency bands can be obtained by the two steps. This is much more simple and convenient to cover full-band spectrum than [5]. The block diagram of the above example frequency algorithm (fig 2.5) is as follow.

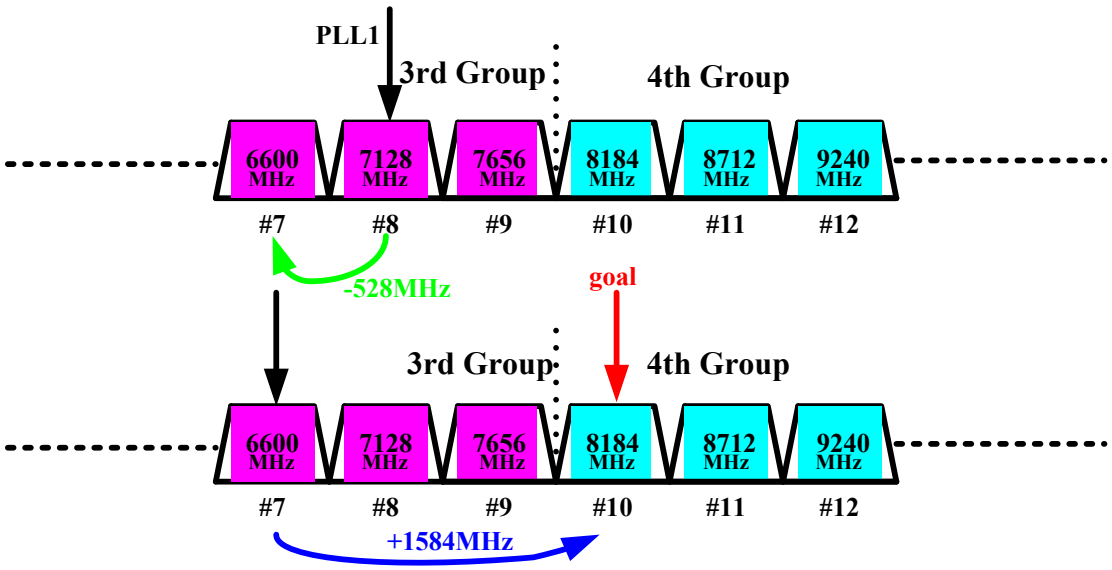


Figure 2.5 The block diagram of the example frequency algorithm

The advantage of this frequency generation scheme would be discussed and compared with other published architectures in the last session.

2.3 System Design Consideration

UWB frequency synthesizer is quite dissimilar to conventional narrow band ones in some aspect: I/Q output phase, data rate, operating bandwidth, co-existence with other standards… and so on. Therefore, the system design consideration should be modified to get the appropriate features of it. Preliminarily, single-ended circuits take the priority for its low power consumption and smaller chip area as compared to differential ones, though it is liable to suffer from higher noise and second-order distortion.

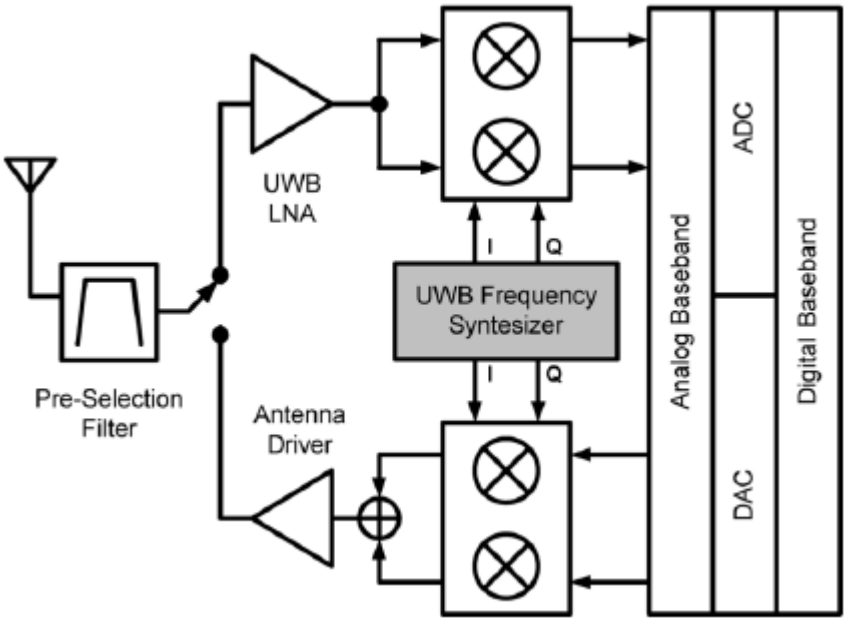


Figure 2.6 Frequency synthesizer in a MB-OFDM UWB transceiver

Fig. 2.6 above [12] illustrates the role of a UWB frequency synthesizer in an MB-OFDM direct conversion transceiver. As in other wireless systems, the frequency synthesizer has the crucial function of generating the local oscillator (LO) signal that drives the down-converter in the receiver path and the up-converter in the transmitter. There are at least two demanding requirements that make a frequency synthesizer for an MB-OFDM UWB radio significantly different from the widely explored synthesizers for narrow-band wireless systems, which are: 1) the range of frequencies to be generated spans several gigahertz and 2) the time to switch between different band frequencies within a band group should be less than 9.47 ns. This requirement prevents the use of a standard PLL-based synthesizer as a solution for this application.

In addition to the frequency switching speed, the synthesizer's output LO signal must comply with other requirements to ensure proper operation of the MB-OFDM UWB radio. The specifications outlined here assume the OFDM parameters and bit error rate (BER) requirements described in [3] for a 480-Mb/s data transmission and an additive white Gaussian noise (AWGN) channel. A quadrature phase-shift keying (QPSK) constellation is considered for the individual sub-carriers. For a packet error rate of 8% with a 1024-byte packet, the target BER when using a coding rate $R = \frac{3}{4}$ is 10^{-5}, which corresponds to an un-coded BER of approximately 10^{-2}. The complete characteristics over the entire frequency bands and analysis are discussed below:

(1) Phase Noise

The phase noise from the LO in an OFDM receiver has two different effects on the received symbols. It introduces a phase rotation of the same magnitude in all of the sub-carriers and creates inter-carrier interference (ICI) [13]. The first undesired effect is eliminated by introducing pilot carriers with a known phase in addition to the

information carriers. On the other hand, phase noise produces ICI in a similar way as adjacent-channel interference in narrow-band systems. Assuming that the data symbols on the different sub-carriers are independent, the ICI may be treated as Gaussian noise. The power spectral density (PSD) of a locked PLL can be modeled by a Lorenzian spectrum described by [13]

$$|\Phi(f)|^2 = \frac{1}{\pi} \cdot \frac{\beta}{f^2 + \beta^2} \tag{2-4}$$

where β is the 3-dB bandwidth of the PSD, which has a normalized total power of 0 dB.

The degradation (D in decibels) in the signal-to-noise ratio (SNR) of the received sub-carriers due to the phase noise of the LO in an OFDM system can be approximated as [14]

$$D \cong \frac{11}{6 \cdot \ln 10} \cdot 4\pi \cdot \beta T \cdot \frac{E_S}{N_O} \tag{2-5}$$

where T is the OFDM symbol length in seconds (without the cyclic extension), β defines the Lorenzian spectrum described above, and $\frac{E_S}{N_O}$ is the desired SNR for the received symbols (in a linear scale, not in decibels). For this system, $\frac{1}{T} = 4.125$ MHz and the $\frac{E_S}{N_O}$ for the target coded BER of 10 is 5.89 (7.7 dB). For D=0.1dB and the mentioned parameters, β can be computed with (2-4) and is 7.7 kHz. The corresponding Lorenzian spectrum has a power of -86.5 dBc/Hz @ 1 MHz.

(2) In Phase (I) and Quadrature Phase (Q) Matching

In an OFDM system, the amplitude and phase imbalance between the I and Q channels transform the received time-domain vector into a corrupted vector r_{iq}, which

consists of a scaled version of the original vector r combined with a term proportional to its complex conjugate r^* . This transformation can be written as [15]

$$r_{iq} = \alpha \cdot r + \beta \cdot r^* \tag{2-6}$$

where α and β are complex constants, which depend on the amount of IQ imbalance. This alteration on the received symbols can have a significant impact on the system performance. The effect of a phase mismatch in the quadrature LO signal on the BER versus SNR performance of the receiver was evaluated considering the system characteristics. Simulation results for uncoded data over an AWGN channel showed that the degradation in the sensitivity is 0.6 dB for 5° of mismatch.

(3) Spurious Content

As in other communication systems, the most harmful spurious components of an LO signal are those at an offset equal to multiples of the frequency spacing between adjacent bands (in this case, 528 MHz) since they directly up/down convert the transmission of a peer device on top of the signal of interest, as shown in fig 2.7 below. It was found that, in order to have a negligible degradation in the sensitivity (0.1 dB); the carrier-to-interferer ratio (CIR) at baseband should be at least 24 dB. In other words, to tolerate the presence of other UWB transmissions that arrive with comparable power at the antenna of the receiver, the synthesizer spurs that appear at frequencies corresponding to other bands must have an aggregate power of less than -24 dBc. A summary of the UWB frequency synthesizer specifications is given in Table 2.1.

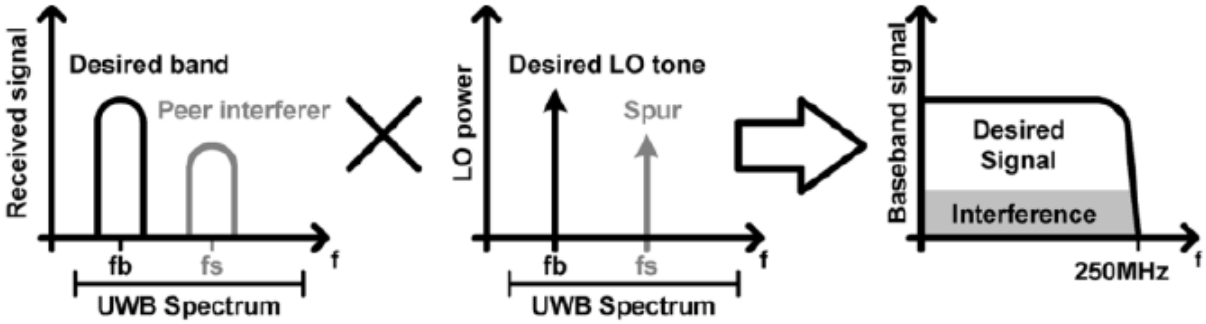


Figure 2.7 Effect of unwanted frequency translation of interferers

Table 2.1 The summary of the UWB frequency synthesizer specification

Band spacing	**528 MHz**
Switching time between adjacent bands	**< 9.47ns**
Phase noise of the LO signal	**< -86.5 dBc/Hz@1 MHz**
Aggregate power of spurs at band frequencies	**< -24 dBc**
Phase I/Q mismatch	< 5°

There are two types of spurs in this synthesizer. One type of spur is caused by the frequency mixing with 528MHz in mixer1. Hence, the spurs in the first group will decide those in other groups. The other type of spur is due to mixer2. Although the third-order unwanted sidebands have been prevented by the frequency generation scheme in fig 2.3, fig 2.4, first-order spurious tones must be taken into consideration when the groups are up/down-converted by mixer2. The first-order spurious tones would be generated at the opposite side of the target band, and it would be placed in the 7.5 GHz spectrum of UWB application. Suppressing the first-order spurs and letting it less than -24 dBc should pay close attention to carefully.

2.4 UWB Frequency Synthesizer Architecture and Operational Principle

The block diagram of the proposed frequency synthesizer is shown in fig 2.8, which consists of two I/Q output PLLs, two SSB mixers, a multiplexer, and a combined output buffer. It generates the fundamental band (7128 MHz) by the ring oscillator of the first PLL and the input reference frequency is 66 MHz produced by a crystal oscillator with low phase noise distortion. In order to cover the frequency spectrum of Group 3rd in UWB application, the spacing frequency 528 MHz is generated by the cascaded dividers (included a quadrature divider-by-3). The frequency spectrum of Group 3rd (included 6600 MHz, 7128 MHz, and 7656 MHz) would come into existence by the first SSB mixer1. The output of the Group 3rd would send to the output buffer.

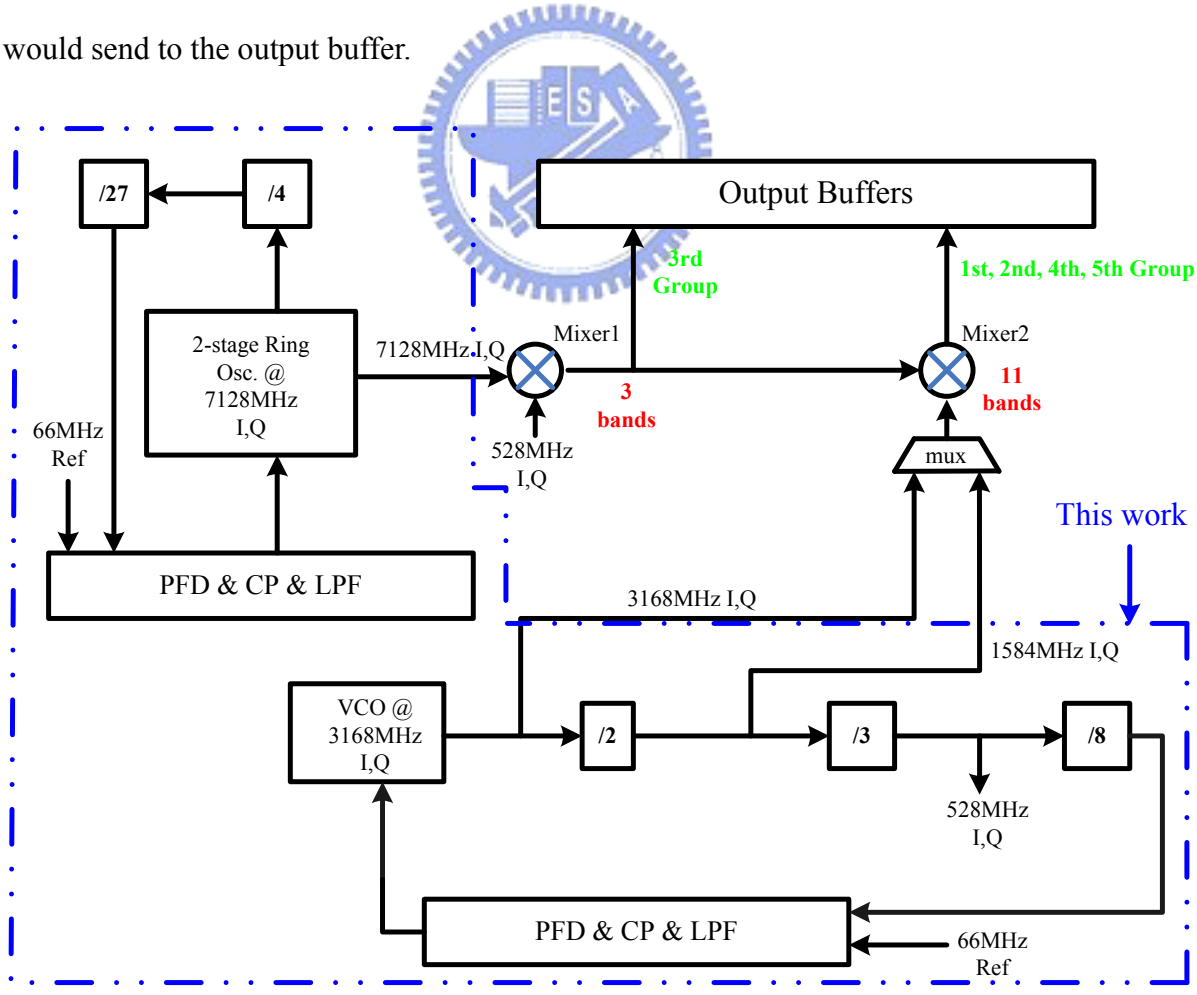


Figure 2.8 The proposed 3.1~10.6 GHz frequency synthesizer for MB-OFDM UWB application

The other frequency spectrum of Group 1st, 2nd, 4th, and 5th are produced at the output of the second SSB mixer2. The extending frequency of 1584 MHz and 3168 MHz are generated by the VCO's output and the connected divider-by-2. Through the LO signal of the 1584MHz or 3168 MHz, the frequency spectrum of the Group 2nd, 4th or Group 1st, 5th would come into existence at the SSB mixer2. The output of SSB mixer2 would also send to the output buffer, and it would be combined with the output of SSB mixer1. The unique output should be constructed for an exact and complete frequency synthesizer. Finally, it would be a single output and full-band frequency synthesizer for MB-OFDM UWB application. The frequency spectrum generation scheme as the block diagram would be shown in fig 2.9 below.

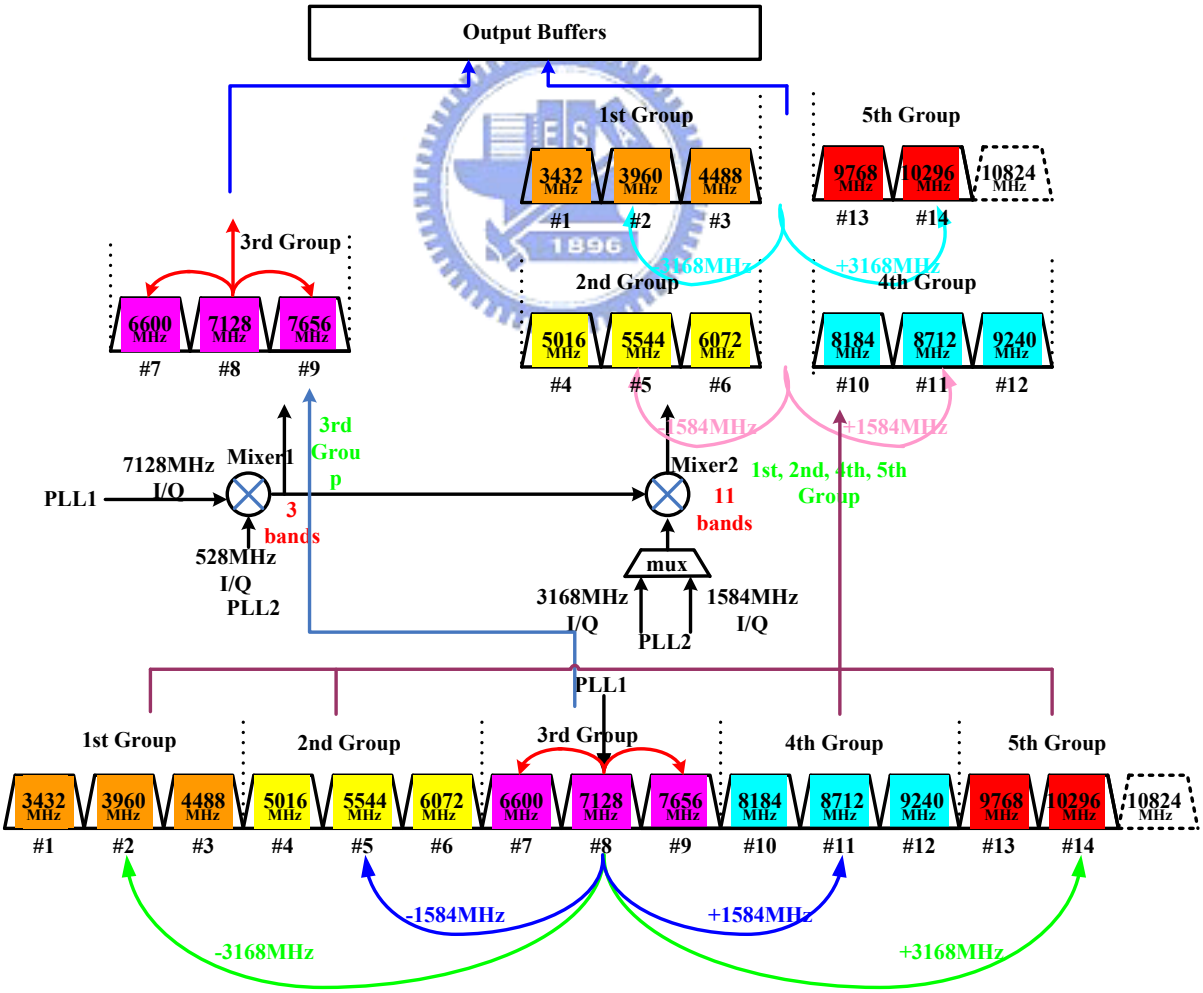


Figure 2.9 The block diagram of the frequency spectrum generation scheme

2.5 Discussion and Comparison

As we mentioned in chapter 2 section 2, the better frequency planning we used, the less circuit components and system disadvantages are revealed. In the followings, the frequency planning architecture for MB-OFDM UWB applications would be compared with previous works at system level. Each frequency planning architecture has its own logical thinking to improve some of the frequency synthesizer's performance. However, in order to reach the goal covering the 7.5 GHz frequency spectrum and satisfying the UWB specifications, there must be some cost. How to let the cost down and achieve the same purpose is the great issue for us to pay efforts on it. Table 2.2 is the comparison of the proposed frequency planning architecture with the illustrated works in chapter 1.

Table 2.2 The summary and comparison of the UWB frequency synthesizer characteristics

	This work	[4] JSSC2006	[5] ISSCC2006	[6] MTT-S	[7] ISSCC2008
Architecture	extending by SSB mixers	extending by SSB mixers	extending by SSB mixers	extending by SSB mixers	extending by SSB mixers
Frequency range (GHz)	3.1~10.6	3~8	3.1~10.6	3.1~10.6	3.1~10.6
Numbers of PLL	2	2	2	1	1
Numbers of SSB mixer	2	2	3	3	3
Numbers of MUX	1	3	2	2	2
Particular and complicated circuits	1.quadrature divider-by-3	1. tri-mode divider 2. divider-by-13 3. very wide bandwidth SSB mixer	1.quadrature divider-by-3	1.poly phase filter*4	none

The frequency planning architecture at system level of this work has superior advantages on low spurious response, uncomplicated system design, and saving much more chip area for UWB application. As compared to [4], the SSB of this work does not need to operate in very wide bandwidth (over 5 GHz frequency spectrum), and dividers in [4] is also a difficulty to realize. The architecture of [5] must waste an extra SSB mixer to realize the whole system. That causes not only chip area consumption but the lower spurious response. [6] is realized for the past UWB frequency planning specification, and the chip area of [6] is huge because of its poly phase filters. The I/Q mismatch problem is another issue for [6] because the poly phase filter cannot operate exactly at wide frequency range. The SSB mixer in PLL also might cause extra problem in locking and spurious consideration in [6]. The [7] uses extra SSB mixer causing the issue as [5], but [7] only need one PLL. Although this work has more one PLL, we use two-stage ring oscillator to save the chip area. Without the passive component inductor, the chip area would even be smaller than [7]. Finally, in all the frequency generation schemes, this work is the most directly perceived through the sense, and the system is the most uncomplicated to realized.

Chapter 3

Phase Lock Loop Theory and System Simulation

Among the circuit component of frequency synthesizer, the phase-lock-loop is the major part of it. Synthesizers used in commercial radio receivers are largely based on phase-lock-loops (PLLs). Transceivers' LO signals are generally produced by it. Because of this, the PLLs play an important role in the radio communications.

Phase-lock-loop (PLL) is a control system that generates a signal that has a fixed relation to the phase of a "reference" signal. A phase-lock-loop circuit responds to both the frequency and the phase of the input signals, automatically raising or lowering the frequency of a controlled oscillator until it is matched to the reference in both frequency and phase. A phase-lock-loop is an example of a control system using negative feedback. It is widely used in radio, telecommunications, computers and other electronic applications. They may generate stable frequencies, recover a signal from a noisy communication channel, or distribute clock timing pulses in digital logic designs such as microprocessors. Since a single integrated circuit can provide a complete phase-lock-loop building block, the technique is widely used in modern electronic devices, with output frequencies from a fraction of a cycle per second up to many gigahertz. The next section is the general consideration of the PLLs.

3.1 Basic Considerations

Phase Noise

A purity of spectrum synthesized output signal is the most important requirement in all

wireless communication systems. Ideally, the output spectrum of a frequency synthesizer should be a pure tone at the desired frequency, as shown in fig 3.1 (a) below. In the time domain, the output can be expressed as:

$$v_{out}(t) = A \cdot \cos(\omega_0 t) \tag{3-1}$$

However, due to random amplitude and phase fluctuations, the actual output becomes:

$$v_{out(t)} = \left[A + \varepsilon(t)\right] \cdot \cos\left[\omega_0 t + \theta(t)\right] \tag{3-2}$$

Where $\varepsilon(t)$ represents amplitude fluctuations and $\theta(t)$ represents phase fluctuations. The actual output spectrum exhibits "skirts" around the desired carrier impulse in the frequency domain, as shown in fig 3.1 (b) below. Because the amplitude fluctuations can be removed or greatly reduced by a limiter, the phase fluctuations, expressed in terms of phase noise, become a bigger and dominant concern in frequency synthesizer design. The phase fluctuations could be attributed to either the external noise at the frequency-tuning input of the oscillator or the noise sources such as thermal, shot, or flicker noise of the devices in the oscillator.

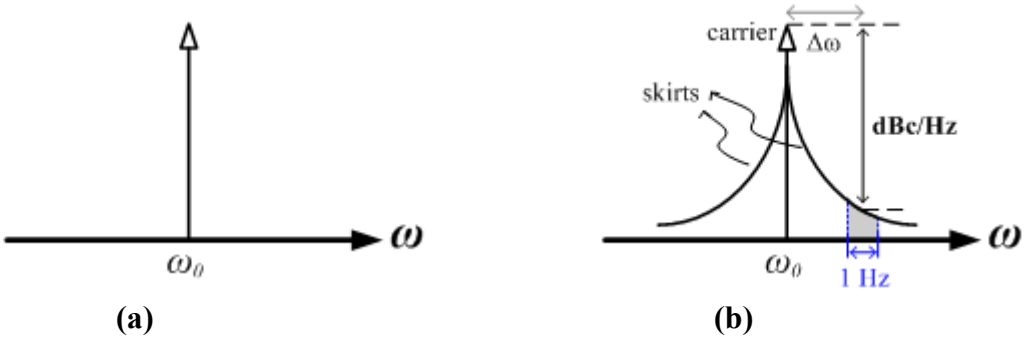


Figure 3.1 The (a) ideal, (b) actual output spectrum of an oscillator

The phase noise limits the quality of the synthesized signal. In order to quantify the phase noise, the total noise power within a unit bandwidth at an offset frequency ($\Delta\omega$) from the carrier frequency (ω_0) is compared with the carrier power. As shown in fig 3.1 (b) above,

this quantity is defined as:

$$L\{\Delta\omega\} = 10 \cdot \log\left[\frac{P_{sideband}(\omega_0 + \Delta\omega, 1Hz)}{P_{carrier}}\right] \qquad \text{(dBc / Hz)} \tag{3-3}$$

Where $P_{sideband}(\omega_0 + \Delta\omega, 1Hz)$ represents the single sideband noise power within a 1Hz bandwidth at an offset frequency ($\Delta\omega$).

Fig 3.2 below illustrates the impact of the oscillator or synthesizer phase noise in both the receive path and transmit path of a transceiver. As depicted in fig 3.2 (a), in the receive path, the weak desired signal is accompanied by a larger interferer in the adjacent channel. Ideally, the received RF signal is down-converted with a pure LO signal into the desired pure IF signal and the down-converted interferer can be easily filtered. However, in fact, there exists a phase noise skirt around the LO signal. After down-conversion, the weak desired signal could be corrupted by the tail of the interferer spectra and even possibly canceled if the phase noise skirt is too large. It degrades the SNR of the desired signal. In the transmit path, the weak nearby signal of interest can be corrupted by the tail of the large-power transmitted signal, as shown in fig 3.2 (b).

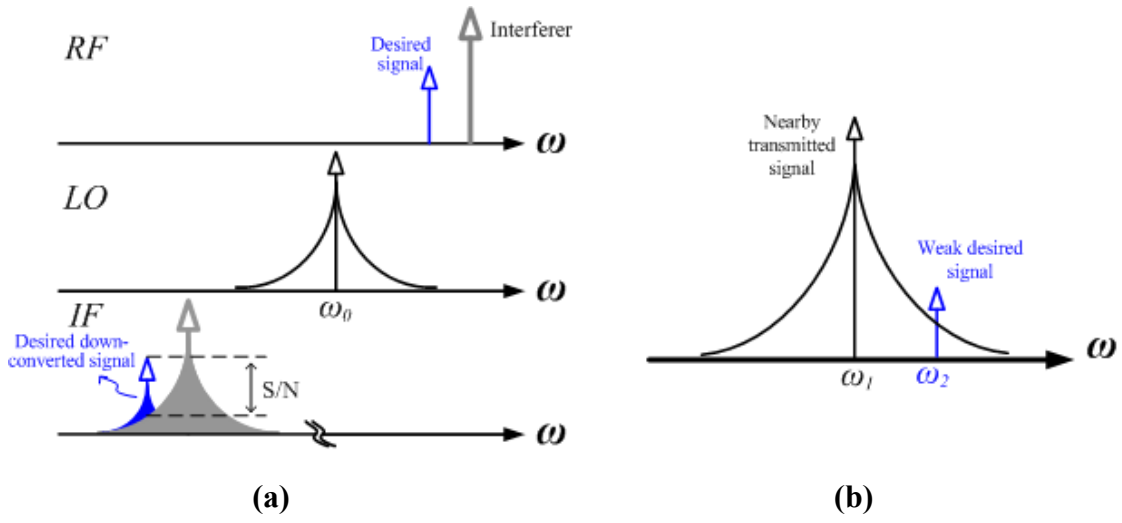


Figure 3.2 The effect of phase noise in (a) the receive path, (b) the transmit path

Therefore, the output spectrum of the LO or synthesizer must be extremely sharp, and a set of stringent phase noise requirements must be achieved so as to satisfy the maximum blocking signal power specified in the wireless communication system.

Settling Time

Transient behavior of the frequency synthesizers is also a critical performance parameter. A change in the division ratio of divider or in the reference frequency would result in a loop transient. Every time a different division ratio or reference frequency is set for channel selection, the synthesizer requires a finite time to lock to the new frequency. The synthesizer needs settling to certain accuracy within the specification of the wireless standard and the overall required time is called “settling time” (also called “locking time”). Also, one thing worth mentioning is that the locking speed requirement of synthesizers is even more stringent for a fast frequency-hopping spread-spectrum system. However, in the UWB specifications, the switching time to the other frequency bands is only 9.47 ns, it is impossible for PLL to lock in such a tiny time. Therefore, changing the frequency bands by settling time of one PLL is not a solution for UWB application. The detailed analysis to model the loop settling behavior will also be discussed in later sections.

Tuning Range

The basic requirement set for a frequency synthesizer by any wireless communication system is that the synthesizer must be able to generate all required frequencies of the system with a sufficient accuracy for channel selection. Therefore, the voltage-controlled oscillator (VCO) and the prescaler must be carefully designed so as to cover the required dynamic frequency range of the synthesizer. However, in our frequency planning architecture, the output frequency of the PLLs should be fixed and unique. This is because of the settling time

of PLL cannot satisfy the UWB specifications (9.47ns).

Spurious Response

Apart from the phase noise, the other key parameter affecting the purity of spectrum synthesized output signal is the relatively high-energy spurious tones (also called spurs), appearing as spikes above the noise skirt, as shown in fig 3.3 (a) below.

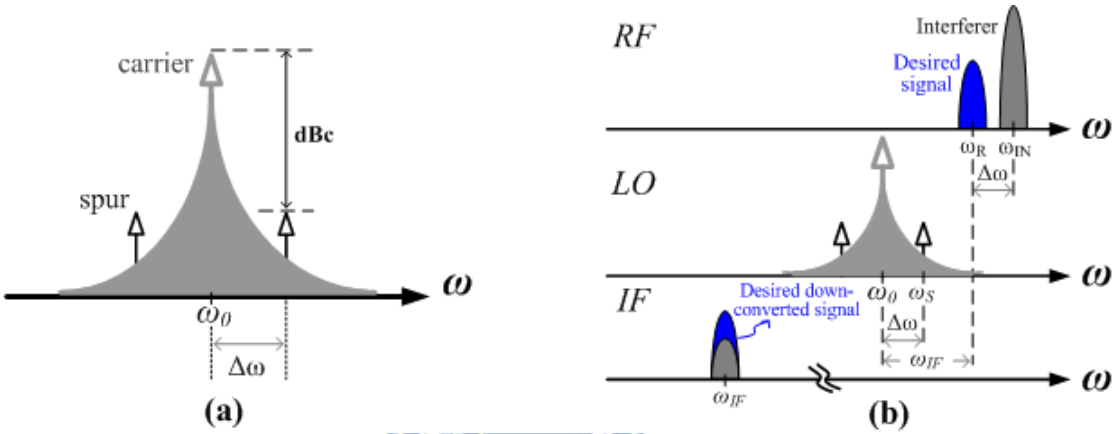


Figure 3.3 The (a) spurs, (b) effect of spurs in receive path

Any systematic disturbance on the tuning input of the oscillator will cause the periodic phase variation and thus modulate the synthesized output. In the frequency domain, it manifests itself as the undesired tones at the upper and lower sideband of the carrier. These tones can be quantified by the difference between the carrier power and the spurious power at certain frequency offset in the dBc unit. As illustrated in fig 3.3 (b), similar to the case of phase noise, if a large interferer is close to the weak desired signal and the LO signal has spurs, then both the desired signal and interferer will be mixed down to the IF. If the spacing between the desired signal and the interferer is equal to that between the LO signal and the spur, the spur in the down-converted interferer falls into the center frequency of the desired down-converted signal, and then also degrades the SNR performance. The most common type

of spur is the reference spur that appears at multiples of the comparison frequency. Due to the non-ideal switching nature of the synthesizer, it may cause reference frequency feed-through, and then the resulting periodic ripples on the tuning input of the oscillator induces the reference spurs at the output, as shown in fig 3.4 below.

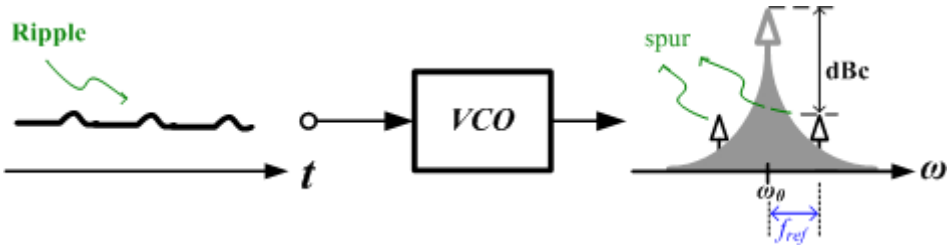


Figure 3.4 The feed-through of the reference frequency

The basic considerations would be analyzed and considered in the later section, and it also be the most important issues in the PLL design specifications. The performance of the frequency synthesizer is compared with them. How to achieve the specifications the frequency synthesizer needed is a tough task.

3.2 Phase-Lock-Loop Architecture

Phase-lock-loop based frequency synthesizer is the most popular in the communications systems. With the ability of high-integration in low-cost CMOS process, the PLL based frequency synthesizer is incomparable and unique. In order to achieve the frequency planning algorithm we designed, we should choose the most satisfying PLL architecture fit in with the UWB specification requirement from numerous PLL types. The integer-N is the most suitable PLL architecture for the demand we need.

3.2.1 Integer-N Architecture

The generic PLL-based frequency synthesizer generates its output by phase- locking the divided output to a reference signal. Due to low cost IC solutions, a charge pump is widely used in PLL-based frequency synthesizers nowadays. As shown in fig 3.5 below, an ideal charge pump combined with an ideal phase-frequency detector (PFD) provides an infinite dc gain with passive loop filters, which results in an unbounded pull-in range and zero static phase error. "Integer-N" means that the division ratio N of the frequency divider is a variable integer. In other words, the synthesized output frequency is integer multiples of the input reference frequency. In general, f_{ref} is fixed and the frequency step or channel spacing is equal to f_{ref}. Various frequencies are achieved by changing the division ratio N. In the locked state, the output frequency is as follows:

$$f_{out} = N \cdot f_{ref} \tag{3-4}$$

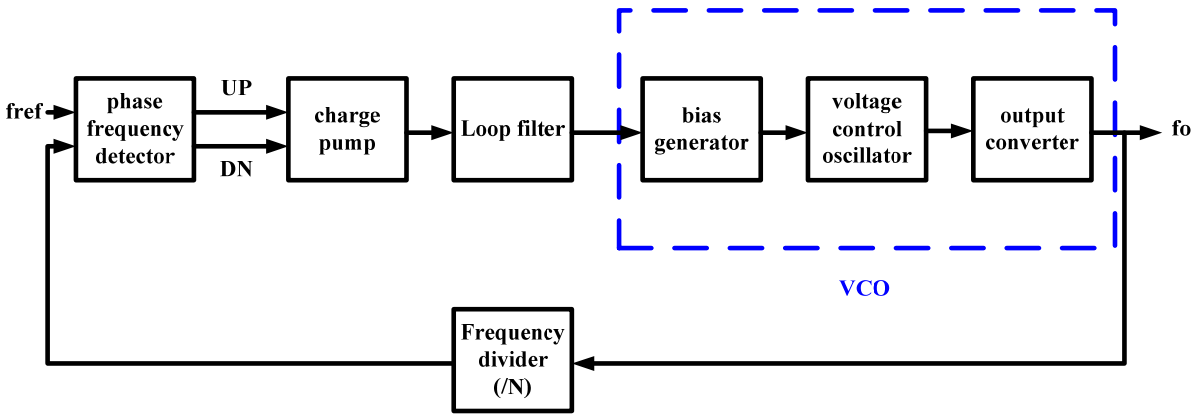
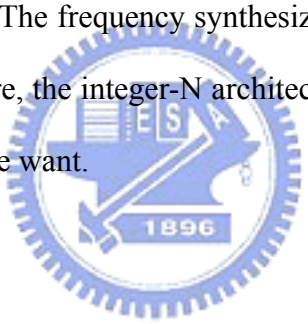


Figure 3.5 A simple charge pump PLL as frequency synthesizer

In the design of integer-N frequency synthesizers, to achieve the well frequency resolution, a low f_{ref} is needed. This low f_{ref} yields a high division ratio as well as a

narrow loop bandwidth. However, a narrow loop bandwidth results in slower settling speed of transients and deteriorates the in-band phase noise. So, the loop performance of the integer-N architecture is intrinsically limited by the standard-specified frequency resolution. Generally, a larger loop bandwidth is desired to achieve a faster dynamic loop response and suppress the VCO close-in phase noise, but otherwise the reference frequency leakage becomes serious. Additionally, as a rule of thumb, the loop bandwidth should be ten times less than f_{ref} for the consideration of the loop stability under linear, continuous-time approximation [16].

Although the trade-off of the reference frequency between the loop bandwidth and the frequency resolution, the frequency resolution issue is not considered in our PLL. The phase-lock-loop in UWB frequency synthesizer would not change its frequency as we mentioned in previous chapter. The frequency synthesizer needs fixed frequencies to generate the frequency scheme. Therefore, the integer-N architecture PLL is more convenient and easy to realize for the requirement we want.



3.2.2 System Specifications

Due to satisfy the specifications for MB-OFDM UWB application, the PLL should conform to the demands of frequency synthesizer architecture. The frequency planning algorithm in chapter 2 needs the fundamental PLL as frequency generation as 7128 MHz. In the followings, the expected specification for the PLL would be presented. The proposed PLL architecture is as follows (fig 3.6). The reference frequency in this work is produced from signal generator outside the chip. Considering the integration for future work, the reference frequency 66 MHz is decided by the crystal oscillator which can popularly and simply generate. Division number can be decided as the output frequency and the reference

frequency appearing. The lock time in proposed architecture is not an issue, so it is chosen as 50μs. Phase noise is -10 dBc/Hz less than the whole architecture we design in chapter 2 as the margin. Considering to save the chip area or convenient to make off chip, the loop filter would be chose as second order structure. It would be discussed in the later section. This work would be realized with TSMC 0.13μm process.

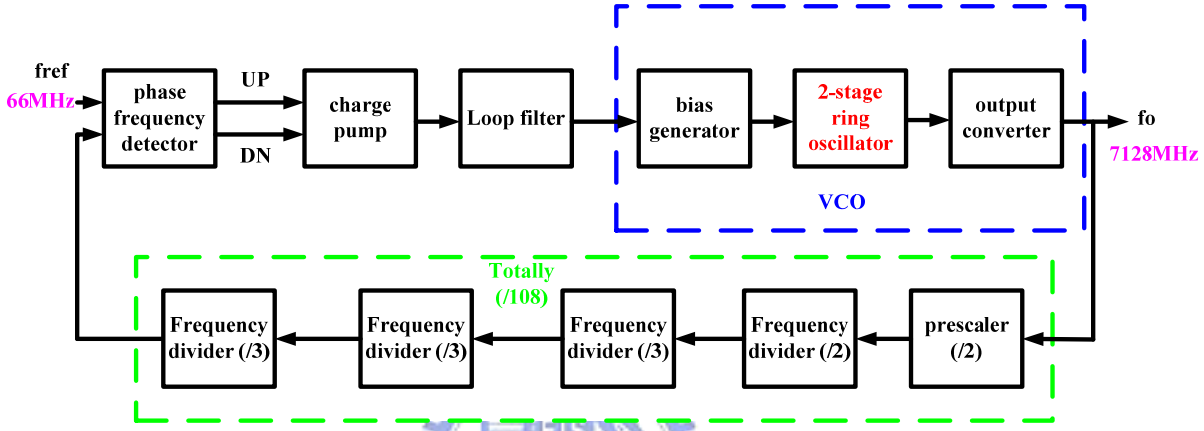


Figure 3.6 The proposed PLL architecture

Table 3.1 is the expected specification for the proposed PLL in order to satisfy the specified UWB frequency synthesizer architecture.

Table 3.1 The specification for proposed PLL

parameter	value
Output frequency f_{out}	7128 MHz
Reference frequency f_{ref}	66 MHz
Loop filter order	2nd
Division number N	108
Lock time t_s	50μs
Supply voltage V_{DD}	1.2 V
Phase noise @ 1MHz	< -96.5 dBc/Hz
Process	TSMC 0.13 μ m

3.2.3 Phase Noise Analysis [17], [18]

From the arrangement in the previous section, we set up the phase noise specification for frequency synthesizer in our application. In this section we would analyze the whole phase noise in PLL further in order to fit in with the specification for the proposed frequency generation scheme. The PLL-based frequency synthesizer suffers from noise introduced at the input or generated by the other components, such as PFD, CP, VCO, loop filter, and frequency divider, etc. It is important to get insight into how these noise sources affect the overall noise performance of synthesized output signal. These noise sources may be classified into two main types to sum up: one is the noise of VCO and the other is the noise from other sources. The effect caused by each of these noise sources can be seen from the closed-loop transfer functions.

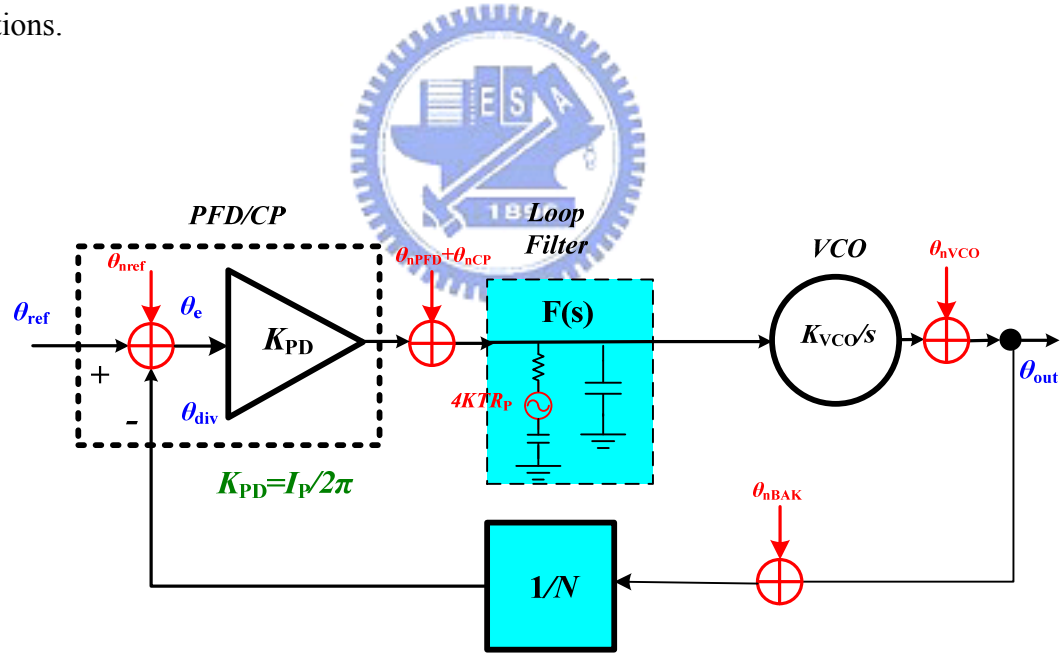


Figure 3.7 Noise sources of type II 3rd PLL linear model

Fig 3.7 illustrates an analytic linear model of the type-II third-order PLL with noise sources added. Based on this linear model, the transfer function from each noise source to the output can be derived so that we can quantify how much each noise source contributes to the output signal. These noise sources can be characterized as follows:

θ_{nPFD}: the noise arises from timing jitter caused by additive noise, predominantly thermal noise within PFD.

θ_{nCP}: the noise comes from thermal and flicker noise of each transistors in each current source. (i.e. $\propto \frac{\overline{I_n^2}}{\Delta f} = 4KT\gamma g_m$)

θ_{nLF}: the mainly equivalent thermal noise of resister R_P inside the loop filter. (i.e. $\propto 4KTR_P$)

θ_{nVCO} and θ_{nref}: the noise sources from VCO and the crystal reference oscillator, respectively.

θ_{nBAK}: the noise sources from the feedback path such as prescaler and dividers respectively.

The transfer functions for these noise sources can be derived as

$$H(s)\big|_{nref} = \frac{\theta_{nout}(s)}{\theta_{nref}(s)} = \frac{2\pi K_{PD}K_{VCO}F(s)}{s + \frac{2\pi K_{PD}K_{VCO}F(s)}{N}} = H(s) \tag{3-5}$$

$$H(s)\big|_{nVCO} = \frac{\theta_{nout}(s)}{\theta_{nVCO}(s)} = \frac{s}{s + \frac{2\pi K_{PD}K_{VCO}F(s)}{N}} = 1 - H(s) \tag{3-6}$$

$$H(s)\big|_{nBAK} = \frac{\theta_{nout}(s)}{\theta_{nBAK}(s)} = \frac{\frac{2\pi}{N}K_{PD}K_{VCO}F(s)}{s + \frac{2\pi K_{PD}K_{VCO}F(s)}{N}} = \frac{1}{N}H(s) \tag{3-7}$$

$$H(s)\big|_{nPFD+nCP} = \frac{\theta_{nout}(s)}{\theta_{nPFD+nCP}(s)} = \frac{2\pi K_{VCO}F(s)}{s + \frac{2\pi K_{PD}K_{VCO}F(s)}{N}} = \frac{1}{K_{PD}}H(s) \tag{3-8}$$

$$H(s)\big|_{nLF} = \frac{\theta_{nout}(s)}{\theta_{nLF}(s)} = \frac{2\pi K_{VCO}}{s + \frac{2\pi K_{PD} K_{VCO} F(s)}{N}} = \frac{1}{K_{PD} F(s)} H(s)$$

(3-9)

We have already deliberated the transfer function for every noise sources above. The overall output phase noise $\theta_{nout}(s)$ transfer function from each noise source can be expressed as

$$\theta_{nout}(s) = (\theta_{nref} + \theta_{neg}) \left[\frac{2\pi K_{PD} K_{VCO} F(s)}{s + \frac{2\pi K_{PD} K_{VCO} F(s)}{N}} \right] + \theta_{nVCO} \left[\frac{s}{s + \frac{2\pi K_{PD} K_{VCO} F(s)}{N}} \right],$$

Where $\theta_{neq} = (\theta_{nPFD+nCP} + \frac{\theta_{nLF}}{F(s)} + K_{PD}\theta_{nBAK}) \Big/ K_{PD}$

(3-10)

The first term of $H(s)\big|_{nout}$ is a low pass term and the second is a high pass term. At low frequencies (i.e. *F(s)* has infinite DC gain, $s \to 0$), $\theta_{nout}(s) = (\theta_{nref} + \theta_{neg})N$, which implies that the noise contribution mainly comes from the reference oscillator, the frequency divider of feedback path, phase frequency detector, and charge pump. At high frequency (i.e. $F(s) \approx 1$, $s \to \infty$), $\theta_{nout}(s) \approx \theta_{nVCO}$, which reveals that the main noise contribution comes from the VCO phase noise.

Finally, the total quantity $\Phi(s)_O$ of output phase noise θ_{nout} contributed by each noise source can be expressed as:

$$\begin{aligned}\Phi(s)_O &= \Phi(s)_{O,ref} + \Phi(s)_{O,PFD+CP} + \Phi(s)_{O,LF} + \Phi(s)_{O,VCO} + \Phi(s)_{O,BAK} \\ &= \left| H(s) \right|^2 \Phi(s)_{ref} + \left| \frac{1}{K_{PD}} H(s) \right|^2 \Phi(s)_{PFD+CP} + \left| \frac{1}{K_{PD} F(s)} H(s) \right|^2 \Phi(s)_{LF} \\ &+ \left| 1 - H(s) \right|^2 \Phi(s)_{VCO} + \left| \frac{1}{N} H(s) \right|^2 \Phi(s)_{BAK}\end{aligned}$$

(3-11)

Where the $\Phi(s)_{O,ref}$, $\Phi(s)_{O,PFD+CP}$, $\Phi(s)_{O,LF}$, $\Phi(s)_{O,VCO}$, and $\Phi(s)_{O,BAK}$ mean the quantity of phase noise in output by each noise source respectively. The $\Phi(s)_*$ means the

corresponding noise sources frequency power spectrum. We could quantize and analyze every noise sources, and compute it with Matlab (in the next section) to get the contributions of each noise source. By means of it, the best loop bandwidth could be designed to gain the best performance of phase noise.

3.3 PLL System Simulation

The phase lock loop (PLL) system includes reference signal generator, phase frequency detector (PFD), charge pump (CP), loop filter (LF), voltage control oscillator (VCO), and divider. Each circuit block has its own system specification for the PLL system to integrate. The purpose for the system simulation is to establish the loop to understand signal behavior in the transient state and the stable state. It could also have the idea about the influence caused by each circuit block. Furthermore, the specifications for every circuit block would be decided by the process of the system simulation. This should be a great ministration to design the integrated circuits. The auxiliary software for system in this section is Simulink of Matlab.

3.3.1 Design Consideration

The PLL system considerations are as fig 3.8 below:

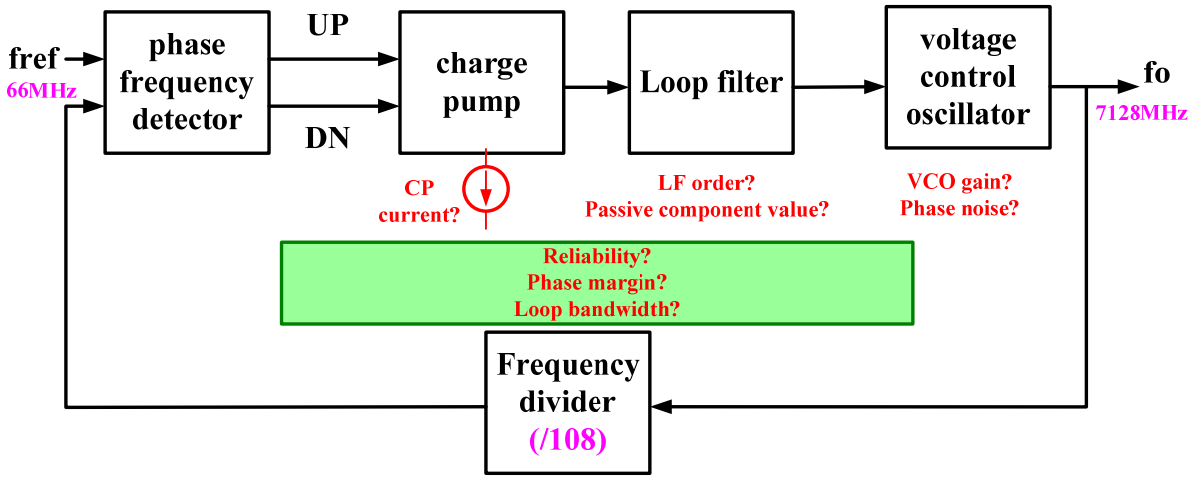


Figure 3.8 System considerations for each block of PLL

The input frequency (reference frequency) is 66 MHz, and the output frequency is 7128 MHz. The division of the divider is 108. They are determined in the previous section. Besides them, all the other situation we should know for each blocks are the charge (discharge) currents in the charge pump, the LF order decision, the passive component value in LF, the VCO gain, and the phase noise model for VCO. There is also a very important property for the whole PLL system, the reliability consideration. It includes the phase margin and loop bandwidth analysis. The system simulation can also check the PFD working state by the Simulink, however it is easy to simulate the PFD circuit behavior in circuit level. The PFD would not model in system level.

The PLL system design would be start at the rough design of VCO circuit block. It could be done because we already have the output frequency quantity. The VCO gain so called K_{VCO} could be decided roughly. The second step is to establish the phase noise model of the VCO. It could design how much charge pump current we should choose for the requirement and waste least power consumption. The next procedure is to design the bandwidth of the whole PLL. Because the settling time of the PLL is not the most important characteristic for our synthesizer architecture, the loop bandwidth of PLL could be chose one of tenth of input

frequency. The passive component of loop filter would be design when we set up the reliability issue as phase margin 60°. All the important specifications could be decided to simulation the transistor level like this.

3.3.2 System Simulation

The system simulation procedure mainly divides into four parts: 1. the design of the K_{VCO}, 2. the decision of the charge pump current, 3. the design of the loop bandwidth, and 4. the design of loop filter. In this section, we would set up the system simulation step by step as follows:

- The design of the K_{VCO}

The first step of system simulation for PLL is to set up a modeled VCO for the future used. This VCO does not the final version of the PLL, but it supports us to understand the behavior and the data of VCO. The most important issue of this is the gain of VCO, it is one of the loop gain factor in PLL. This procedure also needs to construct the phase noise model of VCO. Because of the noise sources from other than the reference oscillator and VCO are usually relatively insignificant and hence negligible. In other words, the overall phase noise performance is mostly dominated by the reference oscillator and VCO. However, the reference frequency in this work would be produced by the signal generator outside the chip. VCO noise behavior is the most critical point in the PLL system. From the noise behavior of VCO, we could establish the noise environment to design the other properties.

The details of the design considerations and simulation procedures would be completely discussed in the next chapter. This design of VCO is only the rough simulation in order to

gain the data we need. Therefore, the rough simulation of VCO would not present here instead of the simulated data from transistor level. The most important data we need is the VCO gain K_{VCO}. The VCO gain in this work is 8.8 GHz/Volt, and the phase noise performance is in fig 3.9 below.

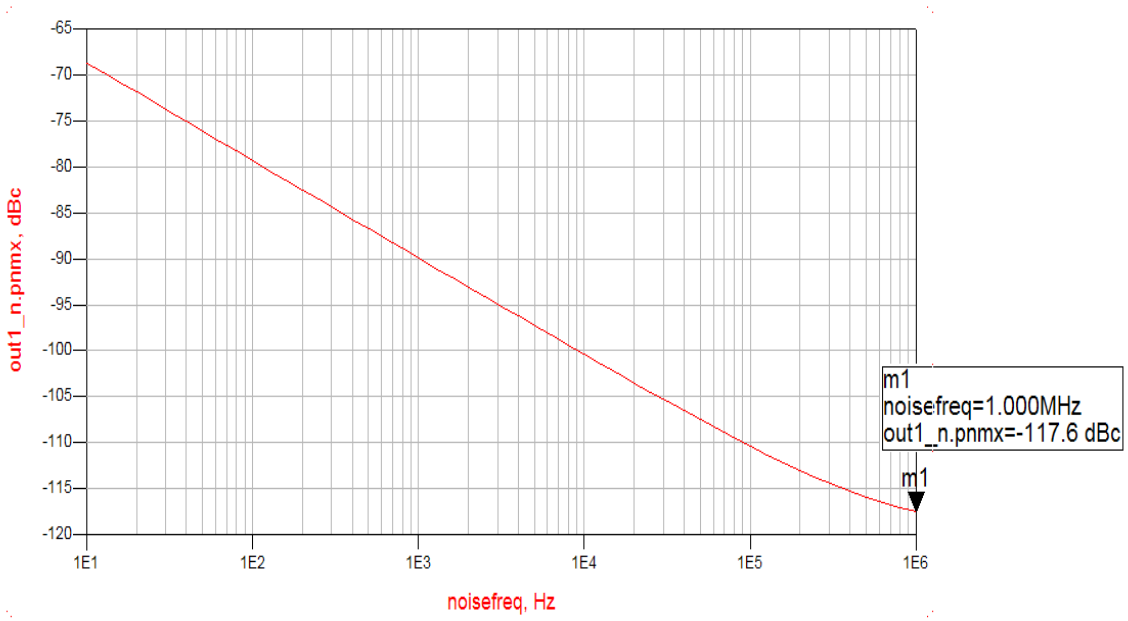


Figure 3.9 Phase noise performance of roughly simulated VCO

The quantity of phase noise could be modeled by an linear line

$$\frac{y-(-68.5)dBc}{x-10^{1}Hz}=\frac{[(-117.6)-(-68.5)]dBc}{(10^{6}-10^{1})Hz}. \tag{3-12}$$

It would replace the real noise behavior in the PLL system simulation in Simulink. That makes the outcome of the system simulation more accurate than tradition method. The tradition method is using analytic equation [19] as:

$$L\{\Delta\omega\}=10\log\left[\frac{2FkT}{P_{sig}}\{1+\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\}\left(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right] \tag{3-13}$$

Then substitute the parameter as the TSMC 0.13μm process' model characteristic. However, the equation would not be more correct than using the simulation software tools. The detailed analysis would also be presented in the next chapter.

- The decision of the charge pump current

Charge pump current in the PLL is also an important issue. How to choose a correct value of charge pump current affects the reliability and the noise performance. The more charge pump current PLL uses, the more noise would be suppressed. However, it would cause the reliability problem and the increasing power consumption. The better way is to let the charge pump current slightly over the current that just make the phase noise of PLL matching the specification and cost the least power consumption. In order to achieve the goal, we would construct the phase noise simulation environment for the PLL.

The phase noise similar model of VCO is mentioned above, and the phase noise caused by divider and reference is tiny. The noise of charge pump and loop filter would be concerned. Fig 3.10 below is the equalized structure of the charge pump and the loop filter. The loop filter is 2^{nd} order structure as we mentioned in the previous section. Due to the negative VCO gain, the UP and DOWN signals of the charge pump are reverse to each other from typical signals.

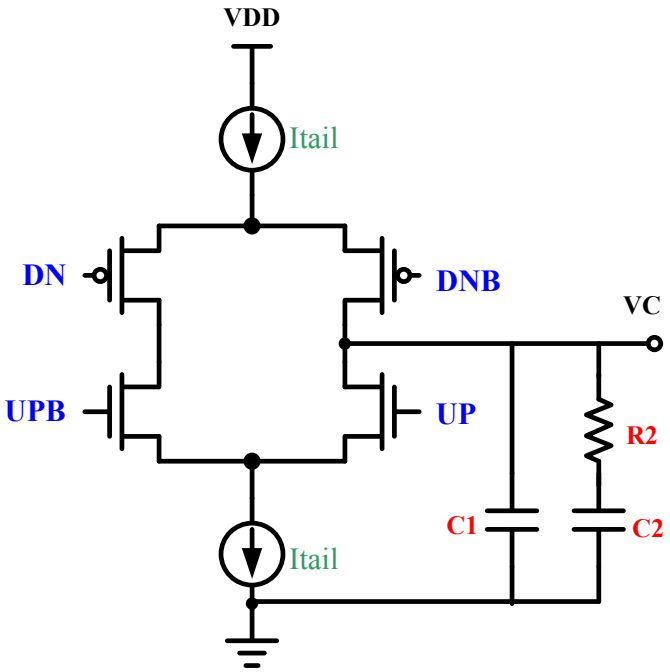


Figure 3.10 The equalized structure of charge pump and loop filter

We can know that the main noise sources of charge pump come from the up/down tail current source from fig 3.10. The current sources are always constructed of NMOS and PMOS. As the result, the two transistors would become the main noise source. Referring to National Semiconductor, we could get the noise mentioned as:

$$\frac{\overline{i^2}}{\Delta f} = 4KTgm + \frac{KF_n \cdot gm_n^2}{W_n L_n C_{OX} \cdot f^{AF_n}} + \frac{KF_p \cdot gm_p^2}{W_p L_p C_{OX} \cdot f^{AF_p}} \tag{3-14}$$

Where the $4KTgm$ is the noise of channel resistance, and the $\frac{KF_n \cdot gm_n^2}{W_n L_n C_{OX} \cdot f^{AF_n}} + \frac{KF_p \cdot gm_p^2}{W_p L_p C_{OX} \cdot f^{AF_p}}$ is the flicker noise of NOMS and PMOS respectively.

The noise source of loop filter mainly comes from the hot noise of resistor as:

$$\frac{\overline{i^2}}{\Delta f} = \frac{4KT}{R_2} \tag{3-15}$$

Finally, we can consider the noise of charge pump and loop filter together with current mode as:

$$\frac{\overline{i^2}}{\Delta f} = 4KTgm + \frac{KF_n \cdot gm_n^2}{W_n L_n C_{OX} \cdot f^{AF_n}} + \frac{KF_p \cdot gm_p^2}{W_p L_p C_{OX} \cdot f^{AF_p}} + \frac{4KT}{R_2}$$

(3-16)

From equation 3-12, and 3-16, we can understand the phase noise of VCO, charge pump, and the loop filter. And we analyze the transfer function of every noise source. The influence quantity at the output of PLL could be gained by multiplying the noise quantity and its transfer function. The whole data could be put into the PLL noise simulation model by Matlab to set up a noise simulation environment to get the specification we need. Fig 3.11 shows the output phase noise with different charge pump current.

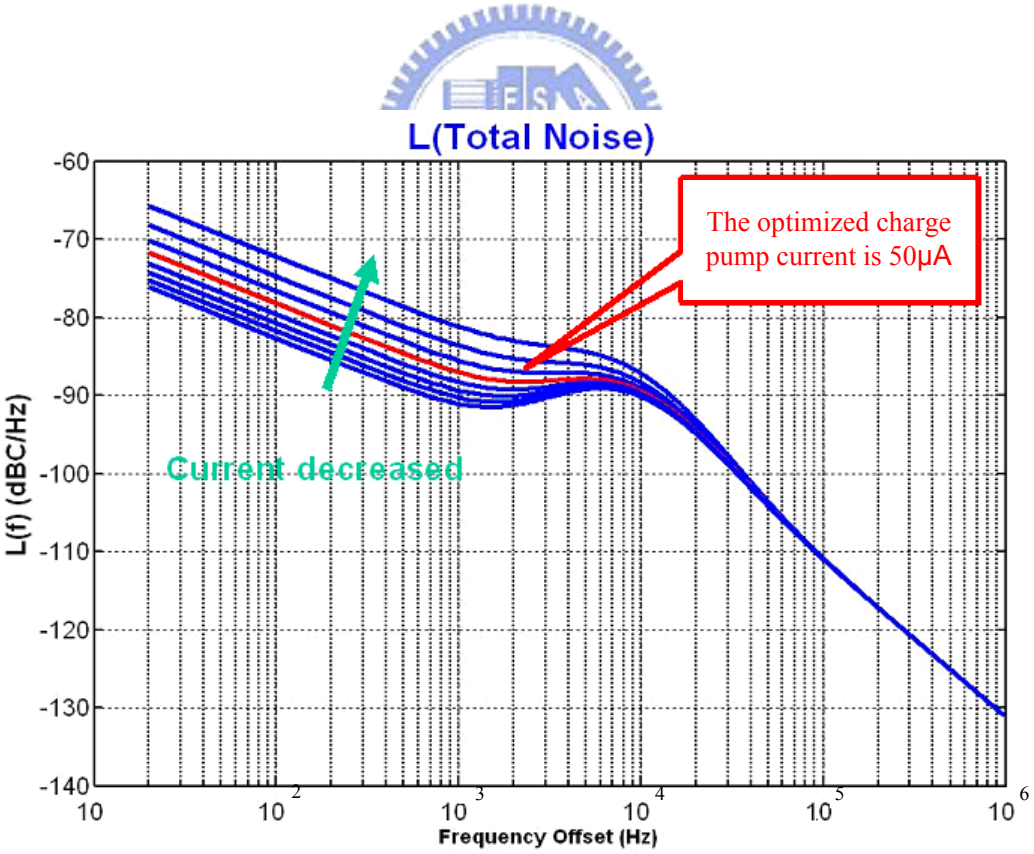


Figure 3.11 The variation of output phase noise with different charge pump current

The arrow tip means the trend of decreasing the charge pump current. We could find out

that the bigger charge pump current is, the lower output phase noise is. The final decision is to choose the current that satisfy the PLL system specification and not to cost too much power consumption. 50μA is the best choice for this consideration as charge pump current.

- The decision of the loop bandwidth

The loop bandwidth affects the performance of settling time and output phase noise. It also has huge influence in reliability issue. There is trade-off between settling time and the ripple on the VCO control line. The lower loop bandwidth is; the greater suppression would be the high frequency components produced by the phase frequency detector but the longer settling time. Comparatively, the lower loop bandwidth is, the shorter settling time of PLL is. How to choose exact value for loop bandwidth is a great challenge. Fortunately, the settling issue is not the concerned problem in our UWB frequency synthesizer architecture. Because even using the fastest settling time PLL in the world cannot satisfy the specification of settling time for UWB frequency synthesizer, 9.47ns. In order to match the switching problem, it is the only way to undertake the frequency generation scheme so far. The methods in operation are illustrated in the chapter 1.

Therefore, the only issue we need to concern is to improve the output phase noise performance. In general, the loop bandwidth is at least 10 times less than reference frequency by experience. Although the lower bandwidth brings the advantage of good suppression at VCO control line, too small bandwidth causes the huge value of the passive component. For future integration, a reasonable bandwidth let the clean VCO input and acceptable value of capacitance. We choose the loop bandwidth as 3 MHz let the passive component might be integrated on chip.

■ The design of the loop filter

As we mentioned above about the loop bandwidth, it affects not only the settling time and output phase noise but the reliability. The choice of the loop bandwidth causes the variation of the phase margin. The higher loop bandwidth is, the lower phase margin of PLL is. The phase margin issue would directly decide the value of passive component in loop filter. By the equation of the loop gain of PLL below [20], we could figure that out.

$$L(s) = \frac{K_{PD} \cdot F(s) \cdot K_{VCO}}{N \cdot s} = \frac{I_P}{2\pi} \cdot \frac{K_{VCO} \cdot k}{N \cdot s^2} \cdot \frac{1 + s\tau_Z}{1 + s\tau_P} \qquad (3\text{-}17)$$

Where τ_Z is the time constant of zero, and τ_P is the time constant of pole. $\frac{I_P}{2\pi}$ equals the gain of phase frequency detector and charge pump. The k is the equivalent transfer gain of the lop filter.

By the analysis of the previous section, we would use the second order loop filter for our frequency synthesizer. Fig 3.12 below is the circuit architecture of the loop filter.

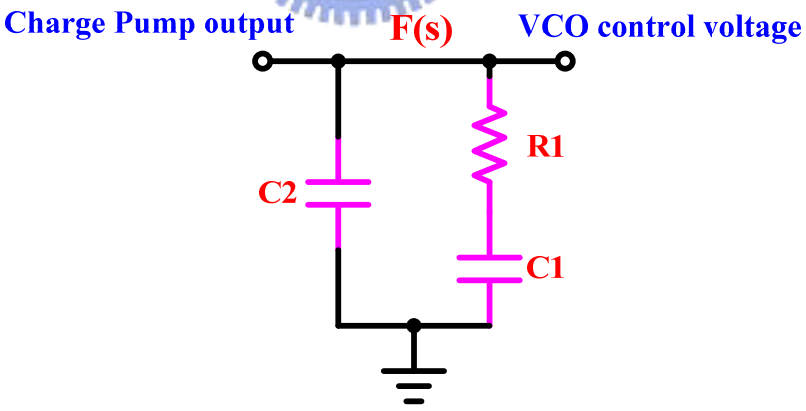


Figure 3.12 The circuit architecture of loop filter.

The loop filter would produce two poles and one zero. The first pole is at DC, the other pole and the zero would place at the right side and left side of the loop gain frequency 3 MHz respectively. The loop gain should be in the middle between the zero and the second pole. The

open-loop Bode plot is shown in Fig 3.13 below.

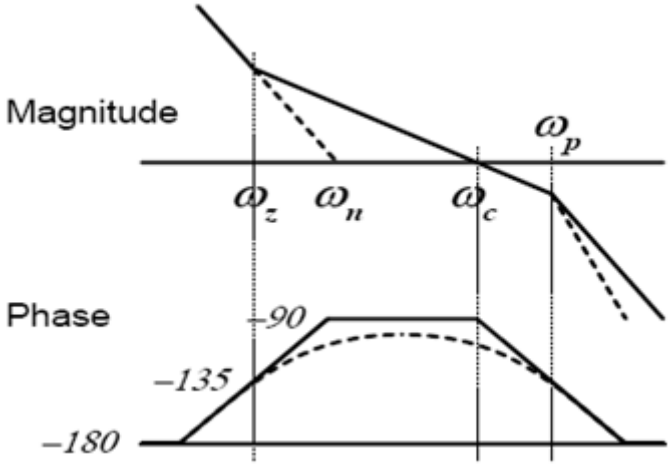


Figure 3.13 The open loop Bode plot of PLL.

In order to attain the phase margin 60°, we choose the zero frequency as 0.75 MHz and the second pole frequency with 12 MHz by the experienced rule, $b = \frac{\omega_P}{\omega_Z} = 16$ as 60° phase margin. The transfer function of the loop filter is as:

$$F(s) = \frac{k}{s} \cdot \frac{1 + s\tau_Z}{1 + s\tau_P} = \frac{k}{s} \cdot \frac{1 + s\tau_Z}{1 + s\tau_Z / b}$$

where $\tau_Z = R_1 C_1$, $\tau_P = R_1 \left[\frac{C_1 C_2}{C_1 + C_2} \right]$, $k = \left[\frac{b-1}{b} \right] \cdot \frac{1}{C_1}$, $b = \frac{\tau_Z}{\tau_P} = 1 + \frac{C_1}{C_2}$

(3-18)

The open loop gain $L(s) = \frac{K_{PD} F(s) K_{VCO}}{N \cdot s} = \frac{I_P K_{VCO} k}{2\pi \cdot N \cdot s^2} \cdot \frac{1 + s\tau_Z}{1 + s\tau_P}$

$$L(s)\Big|_{s=j\omega} = -\frac{I_P K_{VCO} k}{2\pi \cdot N \cdot \omega^2} \cdot \frac{1 + j\omega\tau_Z}{1 + j\omega\tau_P}$$

(3-19)

Then the phase response is $\varphi(\omega) = \tan^{-1}(\omega \cdot \tau_Z) - \tan^{-1}(\omega \cdot \tau_P)$

(3-20)

The loop bandwidth ω_c is at the maximum phase of the phase response as:

$$\frac{d\varphi}{d\omega} = \frac{\tau_Z}{1+(\omega\cdot\tau_Z)^2} - \frac{\tau_P}{1+(\omega\cdot\tau_P)^2} = 0 \Rightarrow \omega_c = \frac{1}{\sqrt{\tau_Z\cdot\tau_P}}$$

(3-21)

and the maximum phase is $\varphi_{\max} = \tan^{-1}\left[\frac{\tau_Z - \tau_P}{2\sqrt{\tau_Z\tau_P}}\right] = \tan^{-1}\left(\frac{b-1}{2\sqrt{b}}\right)$.

(3-22)

Let the $\tau_P = \frac{1}{\omega_c\sqrt{b}}$, $\tau_Z = \frac{\sqrt{b}}{\omega_c}$, the passive component values of loop filter are:

$$\omega_c = \frac{I_P K_{VCO}}{2\pi\cdot N} R_1 \frac{b-1}{b} = \frac{I_P K_{VCO}}{2\pi\cdot N} R_1 \frac{C_1}{C_1+C_2}$$

(3-23)

$$R_1 = \frac{2\pi\cdot N\cdot\omega_c}{I_P K_{VCO}}\cdot\frac{b}{b-1}$$

(3-24)

$$C_1 = \frac{1}{\omega_Z R_1} \quad \text{and} \quad C_2 = \frac{1}{R_1}\frac{1}{\omega_P - \omega_Z}$$

(3-25)

Finally, we substitution the I_P, K_{VCO}, N, ω_Z, and ω_P as the values we analyzed previously as Table 3.2 below. The passive component of loop filter would be presented. Therefore, the loop filter analysis is finished. The value of R_1 is 30.98 kΩ. C_1 is 6.85 pF. And the C_2 is 0.457 pF. The analysis of loop filter could be done like this, however, there is one useful software produced by the National Semiconductor Corporation. It could analysis the loop filter directly and be more accurately. The result is shown in Fig 3.14 below. Fig 3.15 is the Bode plot of the loop filter designed by it.

Table 3.2 The parameters for analyzing the loop filter

parameter	value
Charge pump current I_P	**50 μA**
VCO gain K_{VCO}	**-8.8 GHz/Volt**
Division number N	**108**
Loop bandwidth ω_c	**3 MHz**
Phase margin PM	**60°**
Zero frequency ω_Z	**0.75 MHz**
2nd pole frequency ω_P	**12 MHz**
Frequency coefficient b	**16**

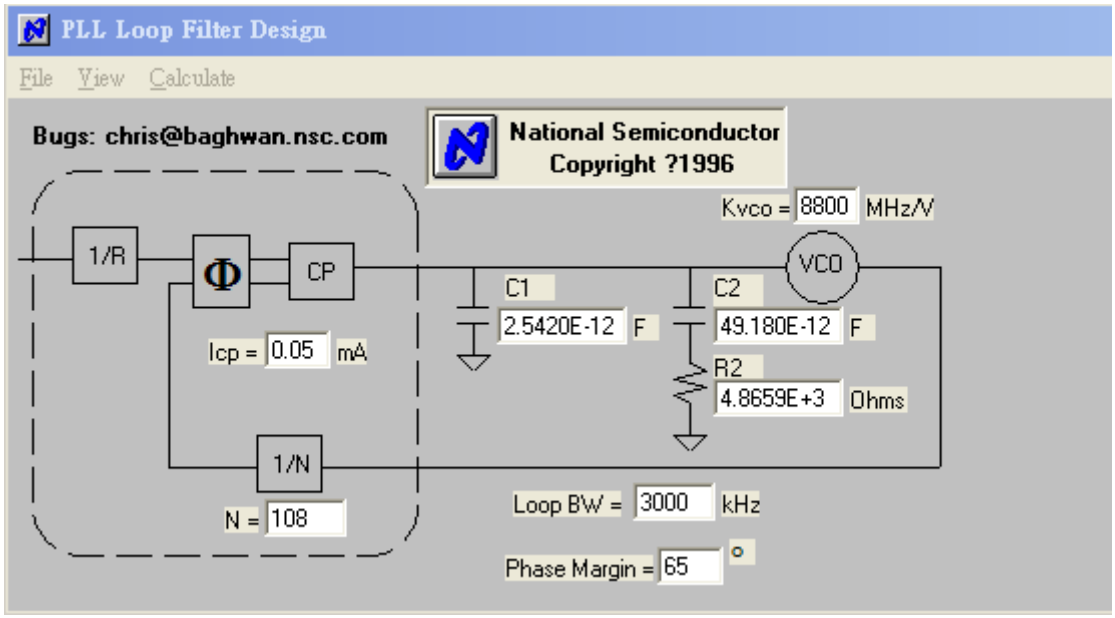


Figure 3.14 PLL loop filter design by the software

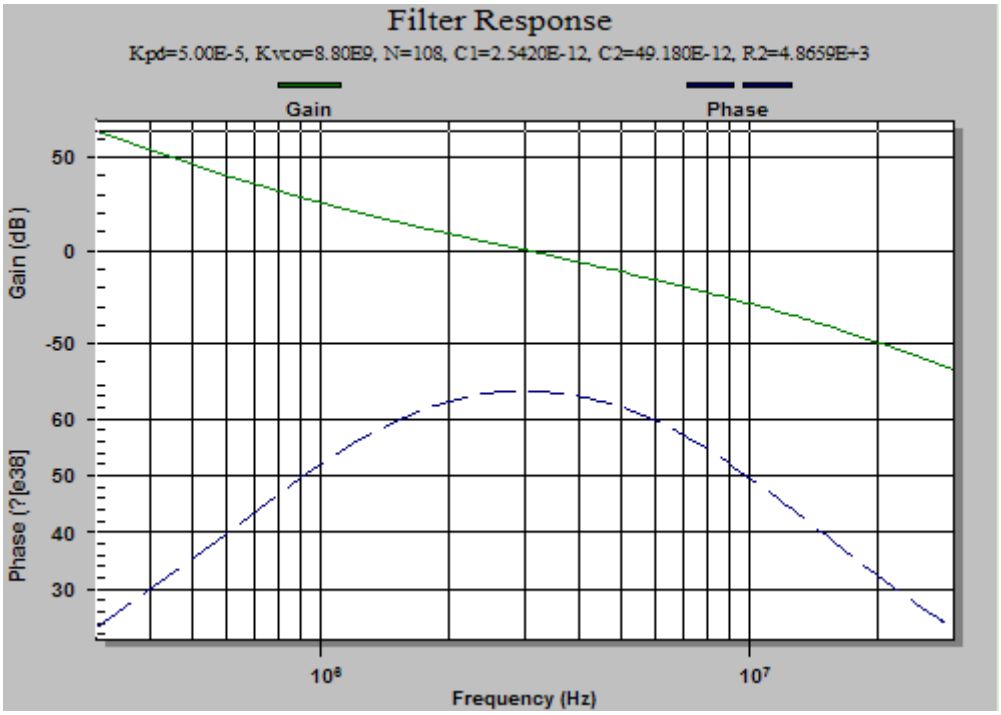


Figure 3.15 The Bode plot of the PLL designed by the software

From the software, NS filter design, the value of R_1 is 4.87 kΩ. C_1 is 49.18 pF, and the C_2 is 2.54 pF. We set the phase margin as 65° to gain some margin. The first choice of the loop filter we decided is the second combination of the passive component for the low pass filter. The final parameters of the PLL in this work are summarized in Table 3.3 below.

Table 3.3 The final parameters of the PLL in this work

Final PLL parameters in this work		
VCO gain	K_{VCO}	8.8 GHz/V
Open loop gain bandwidth	ω_c	3 MHz
Phase margin	PM	60º
Zero frequency	ω_Z	0.75 MHz
Pole frequency	ω_P	12 MHz
Passive elements	R_1	4.87 KΩ
	C_1	49.18 pF
	C_2	2.54 pF

3.3.3 Switching Time and Reliability of PLL

There are still two important verifications for the system simulation of the PLL. It is the switching time (settling time or locking time) and reliability issue in the PLL transient state and frequency response. Although the switching time is not the critical issue for our UWB frequency synthesizer architecture (the settling time in the PLL), we also need to prove and verify it. The settling time under 9.47ns of the PLL is impossible and using only one PLL to achieve the UWB frequency synthesizer is to fish in the air.

We set up the transient state behavior for the each component of the PLL with the Matlab tool, Simulink. That constructs the PLL block circuit with similar mathematical behavior model. Because of the tremendous amount of gate counts in a frequency synthesizer (especially in the frequency divider), closed-loop simulation at the gate-level will take a lot of times. Hence, some prior architecture simulations must be done with Simulink in order to achieve a well-defined closed-loop behavior (system level). A behavior model for the complete PLL is implemented in Simulink as shown in fig 3.16 below.

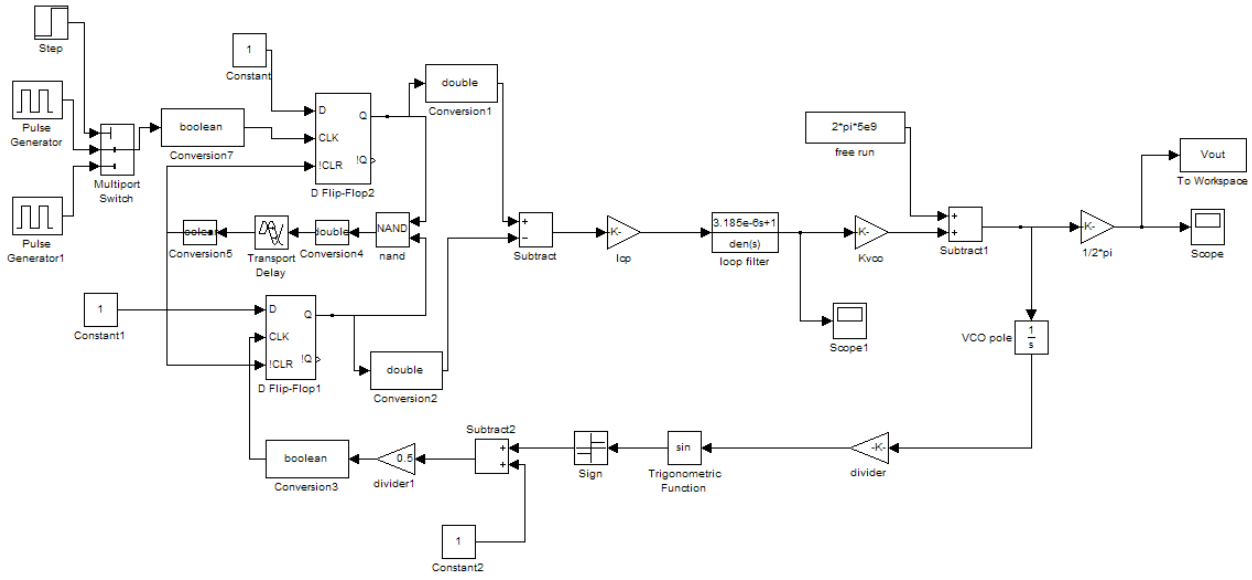


Figure 3.16 The PLL behavior model by Simulink

The transient simulation of the behavior model is shown in fig 3.17 below. It is the switching time from initial state to the stable state of 7128 MHz output. The settling time within 1 KHz accuracy is 41.5 μs. It exceeds the specification for the UWB frequency synthesizer very much. Therefore, using special architecture instead of single PLL is indeed a strong demand for the system to fit in with the switching time less than 9.47ns.

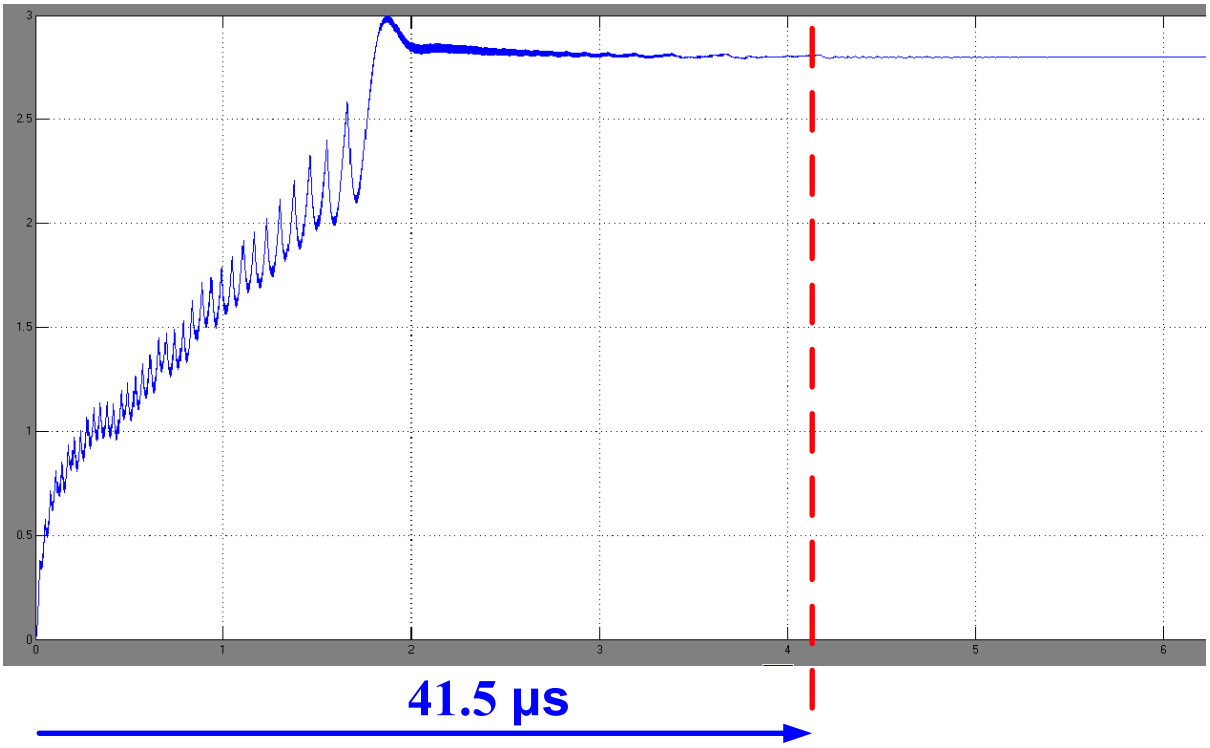


Figure 3.17 The locking time of the PLL from initial state to the output wanted frequency

The sensitivity of the PLL system is quite important. We set the phase margin as 60º, but the loop filter design is modeled as 65º. Reliability would affect directly the stable state of the PLL transient behavior. An unstable PLL system would never output a stable frequency spectrum because the reliability is not concerned enough. We use Matlab to verify the reliability of the PLL whose passive component of filter is design by the National Semiconductor's software. As shown in fig 3.18 below, it could satisfy the specification of 60 degrees.

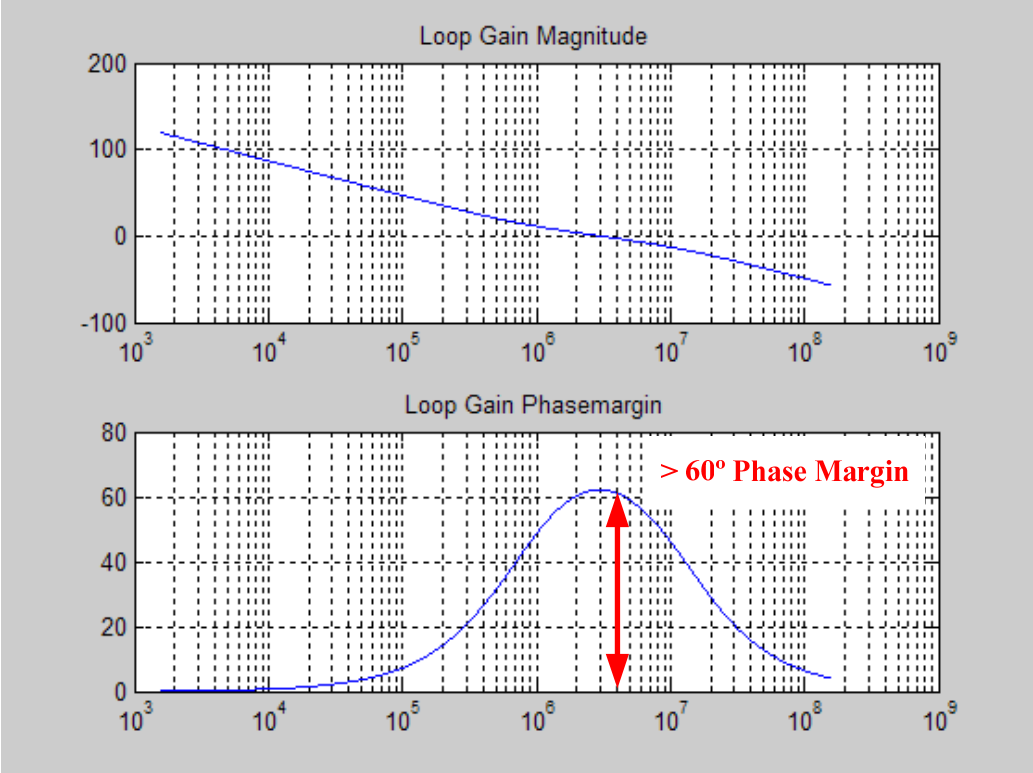
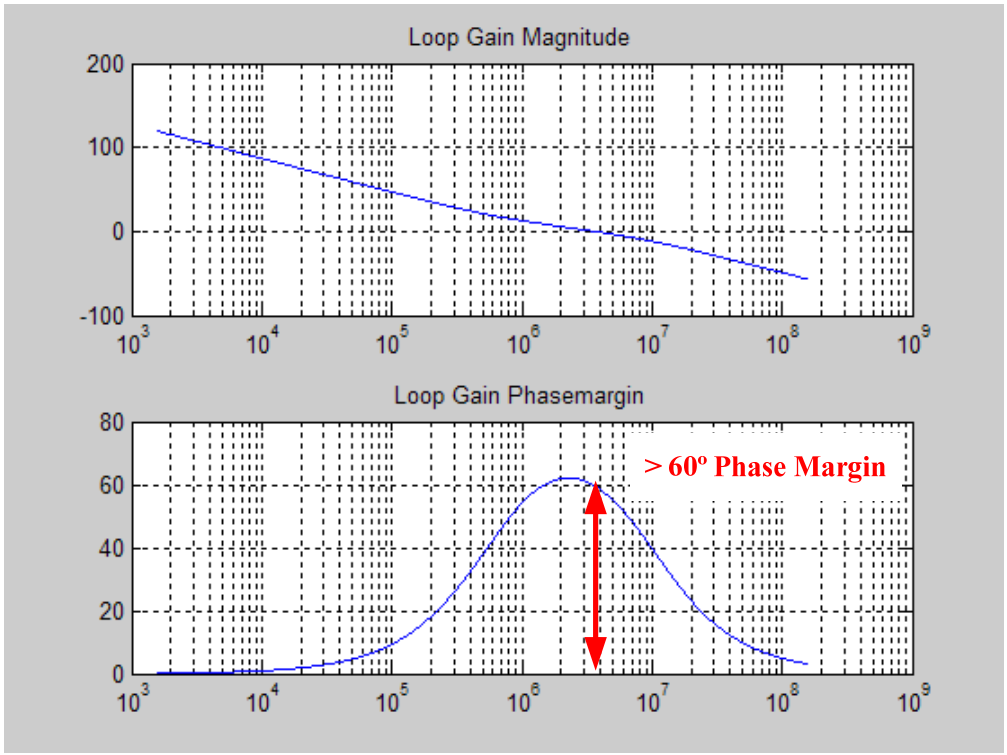
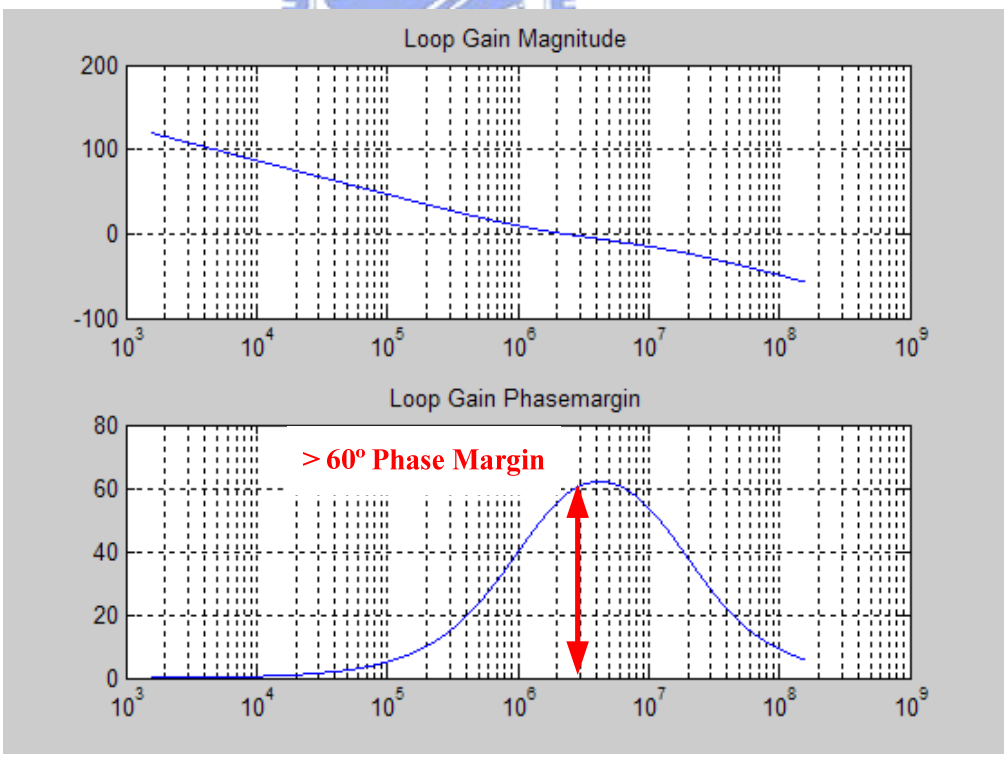


Figure 3.18 The Bode Plot of the open loop transfer function

The variation of the passive components especially the resistor would cause the unstable state because of the process variation. The worst case is the resistor varying ±30% value and might cause the phase margin decreasing. We use Matlab to model the phenomenon of that and verify that they all satisfy the specification of the 60 degrees. As shown in fig 3.19 (a), (b), it could conform to the specification we instituted. Therefore, we could make sure that the PLL system would be stable even under the process variation.



(a)



(b)

Figure 3.19 The Bode Plot of the open loop transfer function with (a) +30% (b) -30% variations

Chapter 4
Quadrature Oscillator based PLL

We have introduced the system level of PLL-based Frequency Synthesizer in Chapter 2. In this chapter, we will demonstrate the design of individual building blocks. A PLL structure is the core of our frequency synthesizer design, which involves the designer's analog and digital expertise. Also, it has many design constraints, some of which have been briefly stated earlier. In this chapter, we will utilize a full-custom design flow for the PLL design. The behavior simulation run by Matlab Simulink has implied the specification and direction for the system design in Chapter 3. However, the circuit level design is based on the deep submicron CMOS 0.13-μm technology. In this thesis, our focus is on the integer-N architecture.

Fig 4.1 below shows the architecture of integer-N frequency synthesizer in this thesis. It has five building blocks, including voltage-controlled oscillator (VCO), prescaler (divide by 2) and dividers (one divide by 2, three divide by 3), phase-frequency detector (PFD), charge pump (CP) and loop filter (LF). The following sections will discuss the design consideration and implementation of individual building blocks in PLL. Finally, the implementation of a complete frequency synthesizer with our proposed two-stage ring oscillator is achieved. With the help of ADS (Advanced Design System) and SPICE simulation, the results are provided in the later sections.

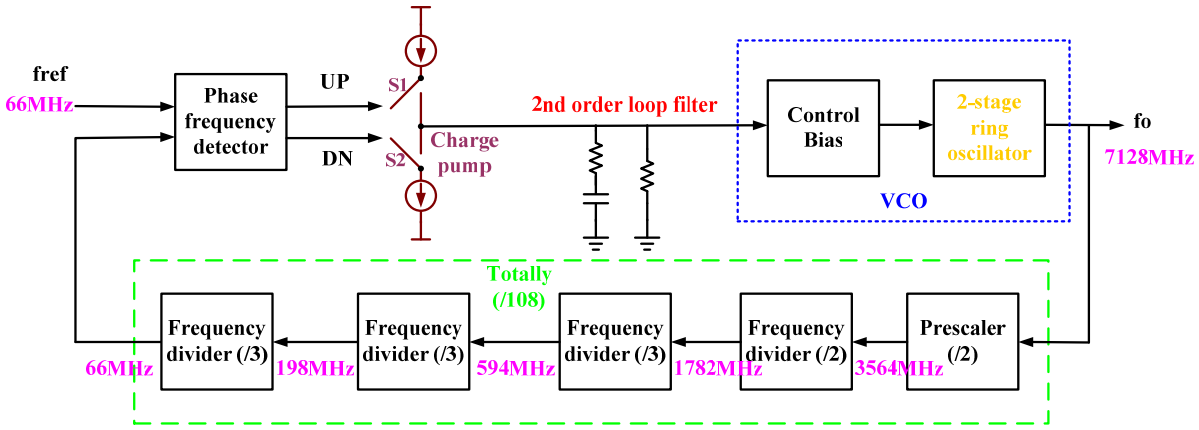


Figure 4.1 The architecture of the integer-N PLL in this work

4.1 Quadrature Voltage-Controlled Oscillator

Quadrature phases of every LO signal are required in UWB systems, which utilize a large bandwidth from 3.1 to 10.6 GHz. Therefore, how to provide the LO signals with quadrature phases as correct down/up conversion for receiver/transmitter are essential and critical. A LO signal with poor phase noise performance results in unwanted frequency translation of nearby interferers, degrading the receiving signal quality seriously. It is interesting to note that unlike narrowband RF systems, UWB applications exhibit susceptibility to phase noise primarily in the form of the corruption of the signal constellation. And the effect of the reciprocal mixing is much less, pronounced because it is determined by the phase noise at an offset of several hundred megahertz. Hence, what is influenced occupies a small portion of the channel.

The proposed two-stage ring oscillator is designed to provide one of the required LO signal for the UWB frequency synthesizer with moderate phase noise performance and power consumption. And it supports the output signal for the basic phase lock loop to generate the

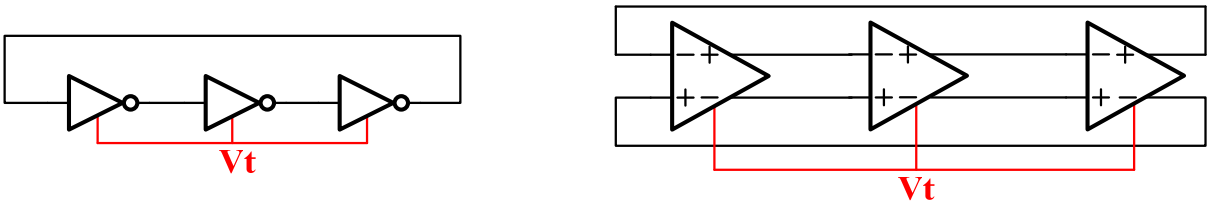
stable LO signal source.

4.1.1 Operational Principle [21]

In general, it has better phase noise performance by using LC tank voltage control oscillator in single chip integrated circuits. However, it must to employ passive component, spiral inductors which would consume a lot of chip area. It is also difficult to model the behavior of passive inductors exactly by simulation tools, so the taped out measurement results may have huge differences between simulations and the actual performance.

Nowadays, the ring oscillators have acceptable performance in phase noise behavior, and the spiral inductors would not be the necessary in the ring oscillator architecture. It could successfully save the space in the chip area and have wider frequency tuning range. Moreover, it is highly integrated in mixed signal ICs. Because of these advantages, it is popularly used in the early microprocessor clock generator of low frequency spectrum. By the chip process goes progress, the ring oscillator start to be utilized in constant angular velocity phase lock loop of the high frequency clock generation, giga-bit microprocessor, and DVD/CD-ROM, etc……..

The architecture of ring oscillator is like fig 4.2 below. The inverters in ring oscillators could be (a) single-ended or (b) differential output. It becomes the ring structure by connecting the output of the last stage to the input of the first stage in multi-inverters. In integrated circuits, the differential pair is much more used because of its differential signal output.



(a) (b)

Figure 4.2 The architecture of the (a) single ended (b) differential output ring oscillators.

By Barkhousen Criterion, the oscillator is a positive feedback that the closed loop gain equals 1 and the phase shift of the loop is 2nπ, (n could be any integer). If we consider an odd number of the stages inverter based ring oscillator, every stage provides basic 180° phase shift. And the phase shift caused by the output load R and the inner/outer parasitic capacitor C also should be thought over to achieve the left phase shift. For example, the 3-stage inverter basically provide phase shift as $3\times180°=540°$. We want to obtain the 2nπ=720° most nearest 540°, so each stage should supply extra phase shift, $(720°-540°)/3=60°$. The RC delay time is shown as t_d, and the delay of n stages is $Nt_d=\frac{T}{2}$ (T is the cycle time of the loop). Therefore, the oscillation frequency is $1/2Nt_d$.

If we use the even number of the stages ring oscillator as the fig 4.3 below, the differential output of the last stage would be cross back to the input of the first stage. It forms a eight-stage inverter chain equaled 2n, and the inverter loop basically provides the phase shift as $180°\times8=8\pi$. In order to obtain the positive feedback to the phase shift 2nπ, the left phase shift would share the 2π degrees to the eight inverter stages. That means the delay time of each stage is t_d, and the $2Nt_d=T$. Therefore the oscillation frequency is:

$$f_{osc}=\frac{1}{2Nt_d}. \tag{4-1}$$

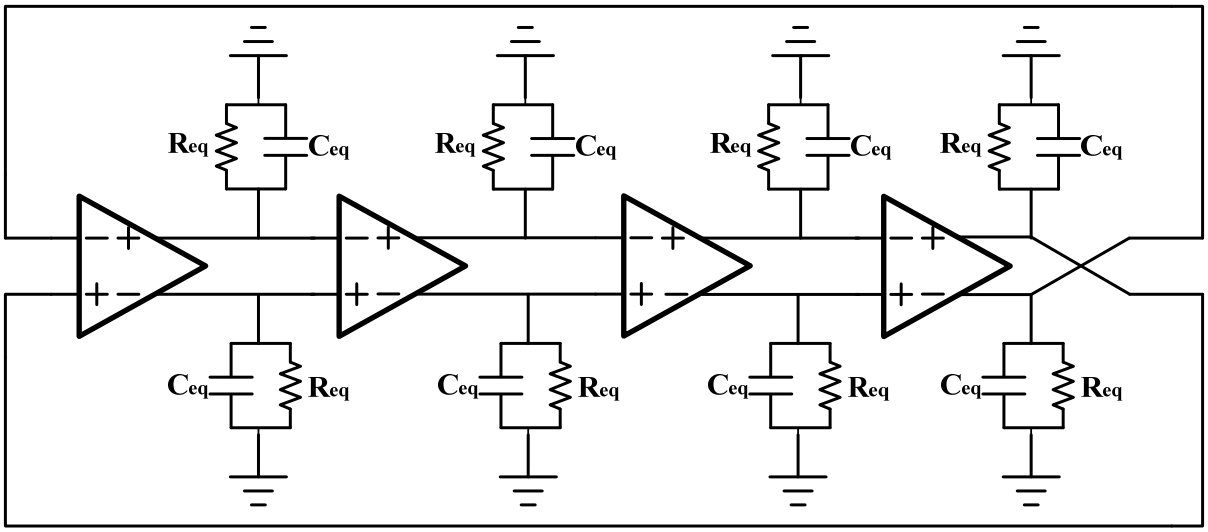


Figure 4.3 The architecture of the even number stages ring oscillator with RC equivalent delay.

The inverter gain and the phase shift of each inverter stage would be considered in the next step. We simply assume by first order approximate that each inverter stage contains a dominant pole formed by the load R and parasitic C. The transfer function of each inverter stage would be:

$$H(s) = -\frac{A_o}{\left(1+\frac{s}{\omega_o}\right)}. \tag{4-2}$$

The whole loop transfer function of the 3-stage inverter chain ring oscillator would be:

$$H(s) = -\frac{A_o^3}{\left(1+\frac{s}{\omega_o}\right)^3} \tag{4-3}$$

The 3-stage inverter should support 180° for the loop to attain the 2nπ=720°, so each stage should provide the phase shift, 60°. In Bode plot, the equation of the frequency response in phase is as:

$$\tan^{-1}\frac{\omega_{osc}}{\omega_o} = 60° \tag{4-4}$$

Therefore, the $\omega_{osc} = \sqrt{3}\omega_o$, and ω_{osc} substitute into the equation 4-2. The loop gain should be greater than 1, so the smallest gain of each inverter stage would be $A_o \geq 2$.

By the same analysis, each inverter stage of the 4-stage differential ring oscillator would share the phase shift 45° (from 360° divide by 8), and the smallest gain of them would be $A_o \geq \sqrt{2}$.

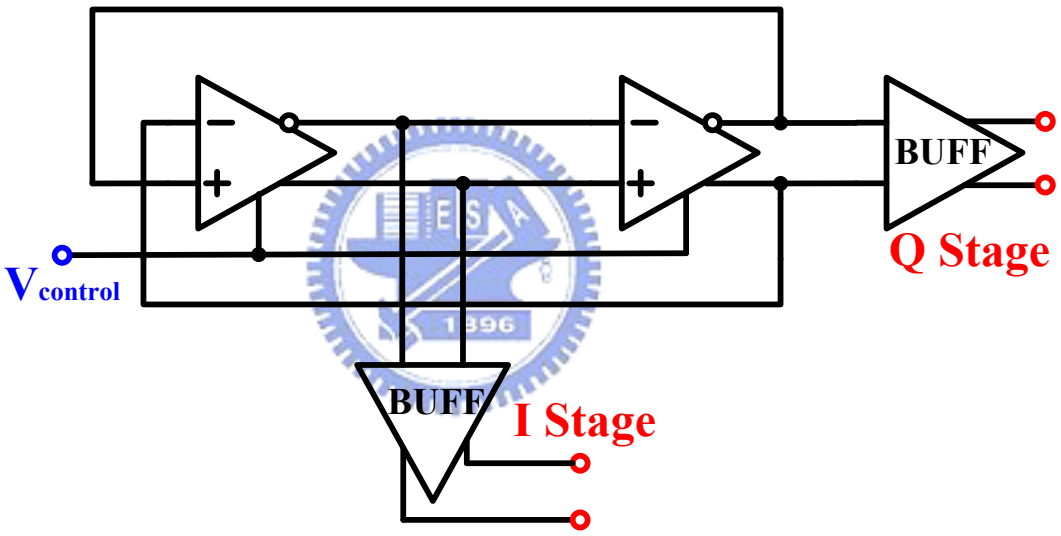


Figure 4.4 The conceptual block diagram of the proposed two-stage ring oscillator.

Equation (4-1) shows that the increase of the oscillators speed can be realized by two ways: through the reduction of the delay time in the cell or by decreasing the number of cells in the ring oscillator. To decrease the delay time is limited by the process congenital conditions. That cannot improve the oscillation speed too much. The reduction of the number of cells is very attractive not only for the operation speed increment but for the power consumption reduction and the saving in area for its implementation. However, as *N* diminishes it is more difficult to satisfy the Barkhausen's oscillation criteria that would be

discussed later. That is why we choose the two-stage ring oscillator, a challenge and a opportunity.

The conceptual block diagram of the proposed two-stage ring oscillator is shown in fig 4.4 above. It contains two differential inverter stages and the same control voltage. The output signal has in phase (I channel) and Quadrature phase (Q channel), two differential orthogonal frequency sources. The differential output of the Q stage would be cross back to the input of the I stage. It forms a four-stage inverter chain equaled 2n, and the inverter loop basically provides the phase shift as $180° \times 4 = 4\pi$. In order to obtain the positive feedback to the phase shift 2nπ, the left phase shift would share the 2π degrees to the four inverter stages. That means the delay time of each stage is t_d, and the $2Nt_d = T$. Therefore the oscillation frequency is $1/2Nt_d$. The whole loop transfer function of the 4-stage inverter chain ring oscillator would be:

$$H(s) = -\frac{A_o^4}{\left(1 + \frac{s}{\omega_o}\right)^4} \tag{4-5}$$

As the analysis of the other stages ring oscillator, each stage of the two-stage ring oscillator should provide the phase shift, 90°. As a result of the impossibility of achieving 90° phase shift by unit RC stage, the traditional ring oscillator should have three inverter stages at least. In order to attain the goal of two-stage ring oscillator, some circuit improvement would be presented in the next section.

The advantages of the two-stage ring oscillator are as follows:

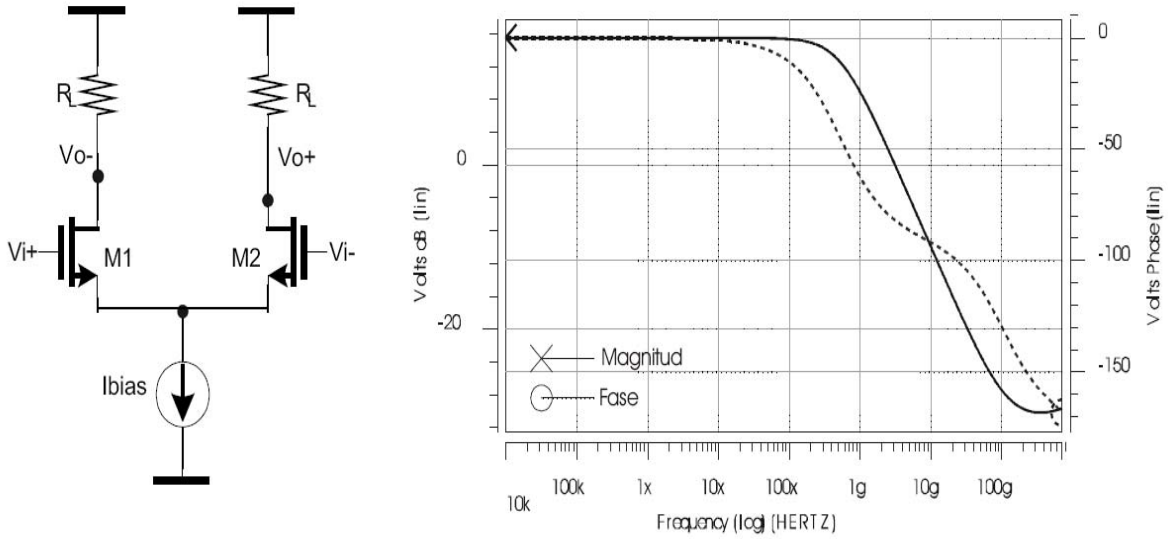
1. It consumes less power dissipation (almost $1/2$ power consumption of the four-stage ring oscillator).
2. It could oscillate at higher frequency (almost twice the oscillation frequency of the four-stage ring oscillator).

3. It occupies less chip area (almost $\frac{1}{2}$ chip area of the four-stage ones).

4. two-stage ring oscillator generates the quadrature phase sine-wave signal with the minimum components.

4.1.2 Design Consideration [21], [25], [26], [27], [28]

For a two-stage ring oscillator, the demands for high speed, low power consumption and quadrature outputs, dictate oscillators of single two stages. However, a simple differential structure in the delay cell fails satisfying the oscillation conditions, just as it is observed in fig 4.5 below. In this figure it is possible to identify a dominant pole around 500MHz created by the time constant in an output node of the cell and a zero at very high frequency (100GHz), above which the magnitude of the gain ends up being flat. The zero comes from the gate-drain capacitance of the transistor M1 in the differential pair and it causes that the absolute phase shifts from 90º to 180º. If this cell was used in a two-stage ring oscillator, the system would not oscillate because the gain is under 0dB at the frequency in which the absolute phase changes 90º, causing the insufficient gain problem.

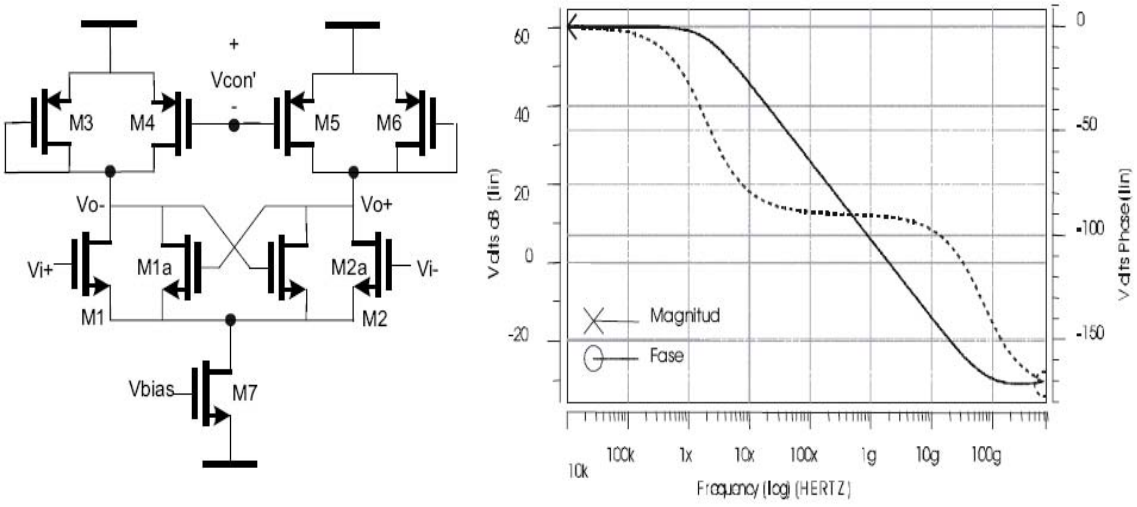


(a) (b)

Figure 4.5 The differential delay cell: (a) circuit diagram, (b) frequency response.

It is possible to generate the oscillation if one adds a mechanism that can provide a bigger change in the phase of the delay cell. An approach is to increase the dc gain and the shift phase of the cell simultaneously using differential amplifiers in parallel [22]. Nevertheless, even when the speed is increased the power consumption stays high, due to the use of four delay cells. In the delay cell of the proposed VCO shown in fig 4.6 below, extra circuitry is not required, the wanted characteristics are obtained by means of positive partial feedback [23] generated by M1a and M2a. The transistors M3 and M4 or M5 and M6, form a voltage controlled symmetrical load [24] that substitutes the resistor *R* of the fig 4.5 such that the delay time of the cell can be modified when the control voltage is changed (Vcon') along with the VCO oscillation frequency. The use of this load type allows diminishing the sensibility to variations in common mode and the noise of phase of the circuit [24]. As shows fig 4.6, the partial positive feedback increases the gain of the cell, at the same time that it provides the necessary delay (the pole moves to the left) and the Barkhousen criteria are

simultaneously satisfied. That means when you design a differential inverter stage, you should verify that gain is above 0dB at the frequency in which the absolute phase changes 90º.



(a) (b)

Figure 4.6 The differential delay cell with partial positive feedback: (a) circuit diagram, (b) frequency response.

The transfer function of the proposed delay cell can be written in the following way:

$$H(s) = A_o \frac{\left(\frac{s}{\omega_z} - 1\right)}{\left(\frac{s}{\omega_p} + 1\right)} \tag{4-6}$$

where A_o is the low frequency gain, ω_p the frequency of the pole and ω_z the frequency of the zero.

Therefore, the differential delay cell of the ring oscillator should satisfy the following conditions:

1. When the phase shift changes absolutely 90º in frequency response, the gain should be greater than 0dB.
2. Changes in one input phase must let the both two output phase change.
3. It needs the ability of high common mode rejection ratio (CMRR). The input of the delay cell will relate to the CMRR value. The higher transconductance of the input, the more assurance it will oscillate and the higher frequency. But that will consume more power.
4. Use the cross couple pair as latch to generate the positive feedback and let the output voltage difference larger.
5. The stronger the coupling of the latch, the more assurance it would oscillate. But the stronger the coupling of the latch, the lower oscillation frequency it would be.

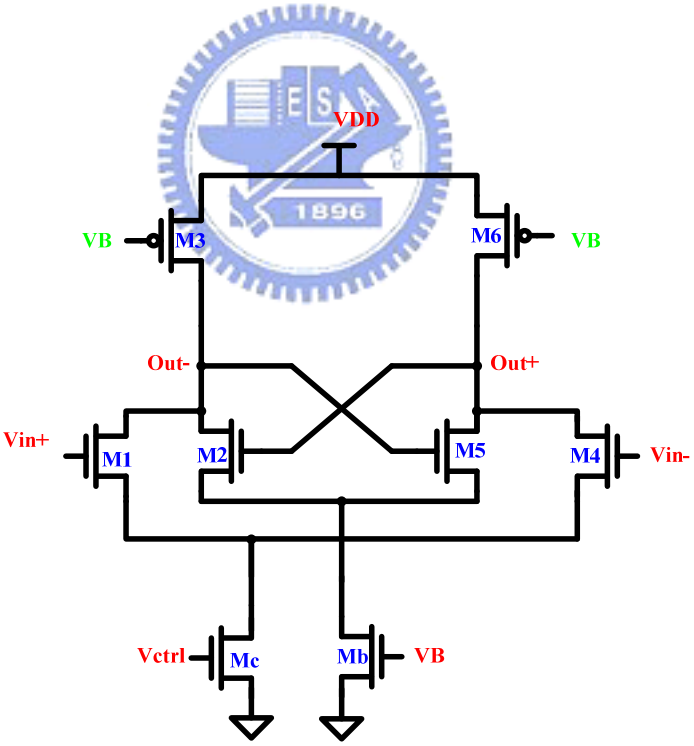


Figure 4.7 The first version of the designed differential delay cell.

The first version of the designed differential cell is shown in fig 4.7 above. It contains a differential amplifier, M1, M3, M4, M6, and Mc. And the M2 and M5 form a cross couple

pair as a latch to provide the negative resistor cancelling the positive resistor. That could obtain the 90º phase shift. Due to the differential pair is completely symmetric, the Mc and Mb would be virtual ground. In order to analyze the circuit conveniently, we would assay it with half circuit as the following fig 4.8.

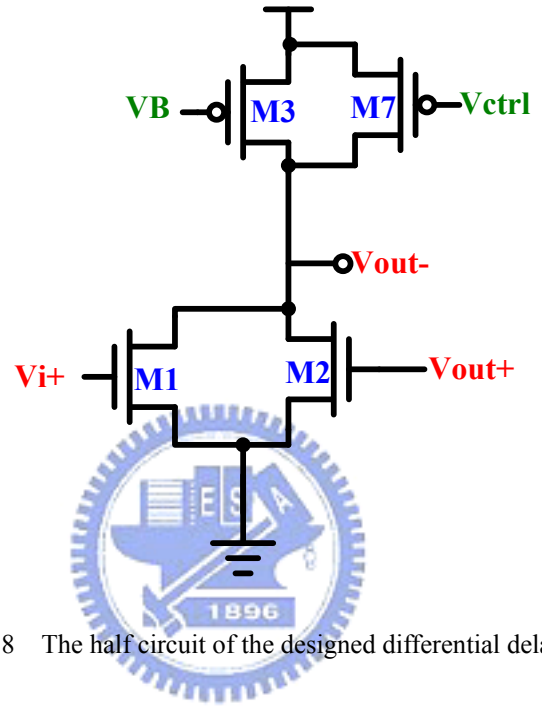
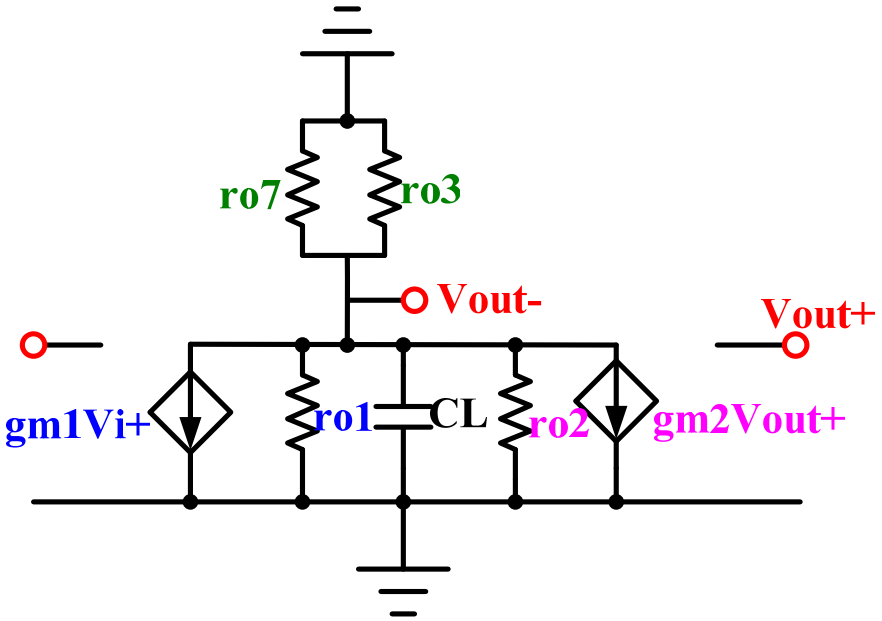
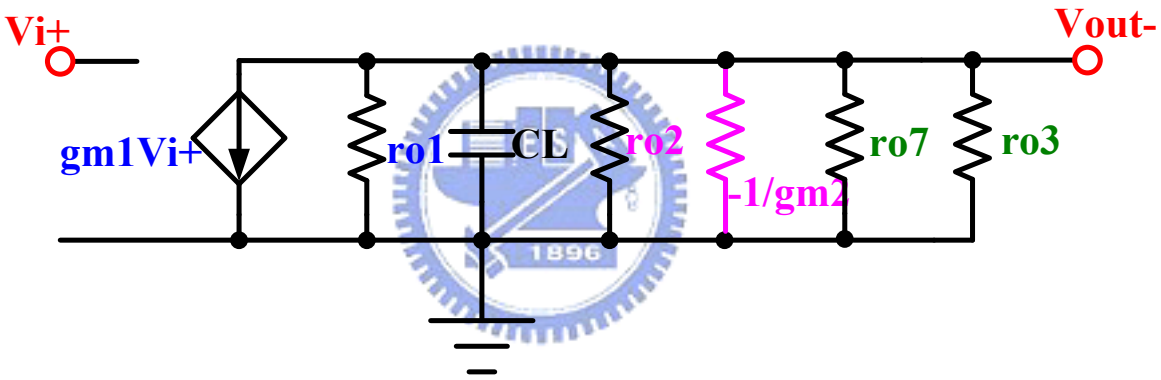


Figure 4.8 The half circuit of the designed differential delay cell.

And the corresponding small signal equivalent model of the differential delay cell half circuit is shown in fig 4.9 (a) below. The fig 4.9 (b) is the rearrangement of the small signal equivalent model.



(a)



(b)

Figure 4.9 The small signal equivalent model of (a) the half circuit (b) with rearrangement.

From the fig 4.9 (b), we could know the V_i to V_o transfer function:

$$\frac{V_{out-}}{V_{i+}} = -g_{m1} \times \left[\left(r_{o1} // r_{o2} // r_{o3} // r_{o7} \right) // \left(-\frac{1}{g_{m2}} \right) // \frac{1}{sC_L} \right]$$

$$= -\frac{g_{m1}}{\left(-g_{m2} + \frac{1}{R_L} \right) + sC_{total}}$$

(4-7)

Where the $R_L = r_{o1} // r_{o2} // r_{o3} // r_{o7}$, the C_{total} is the equivalent capacitance seen from V_{out-}.

In order to satisfy the Barkhausen's criteria, the phase shift of each delay cell must achieve 90 degree and the gain must be greater than 1. When $g_{m2} = \frac{1}{R_L}$, the real part of the transfer function would counteract and it become pure capacitance. That could let the phase shift come to 90º. When the $g_{m2} = \frac{1}{R_L}$, the absolute value of the transfer function would be:

$$\left|\frac{V_{out-}}{V_{i+}}\right| = \frac{g_{m1}}{\sqrt{\left(-g_{m2} + \frac{1}{R_L}\right)^2 + (\omega_{osc} C_L)^2}} = 1 \tag{4-8}$$

Therefore the oscillation frequency is:

$$\omega_{osc} = \frac{g_{m1}}{C_L} \tag{4-9}$$

We could vary the output oscillation frequency by changing the gate voltage of the MOS M1. That would change the g_{m1} to vary the oscillation frequency.

4.1.3 Circuit Realization

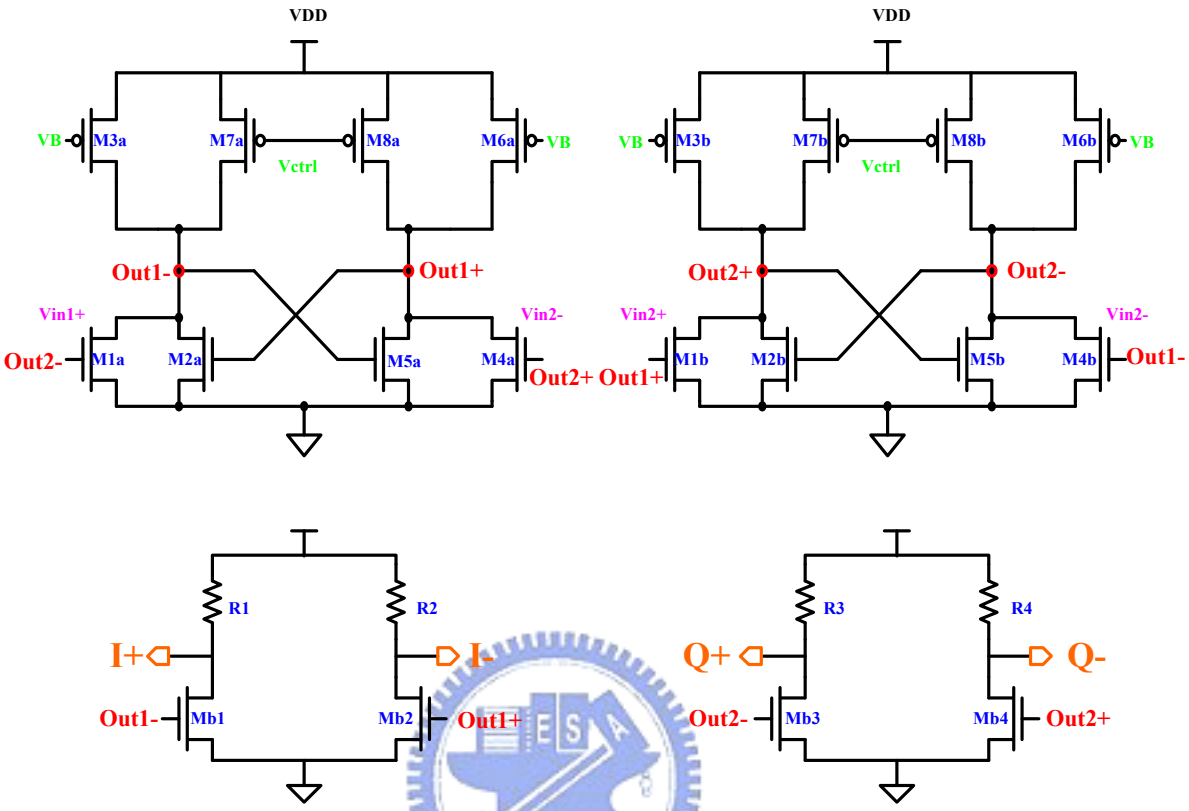


Figure 4.10 The circuit diagram of the proposed two-stage ring oscillator and the oscillator buffers

Fig 4.10 is the final version of the differential delay cell of the proposed two-stage ring oscillator and the buffers of the oscillator. The M1, M3, M4, and M6 also form a differential amplifier; the M2 and M5 is the regeneration latch as the positive feedback either. The current source is taken for the high output amplitude. We add another PMOS load as control transistor by changing the gate voltage to vary the oscillation frequency. The operational principle is the same as the discussion in the previous section we presented and it could make the better performance. The ring oscillator buffer is designed as common source amplifiers composing of transistors Mb1~Mb4 and resistors R1~R4 [37].

We first design the differential delay cell satisfying the requirement in previous section. The most important condition is that when the phase shift changes absolutely 90º in frequency response, the gain should be greater than 0dB. The result of the proposed differential delay cell is shown in fig 4.11 below.

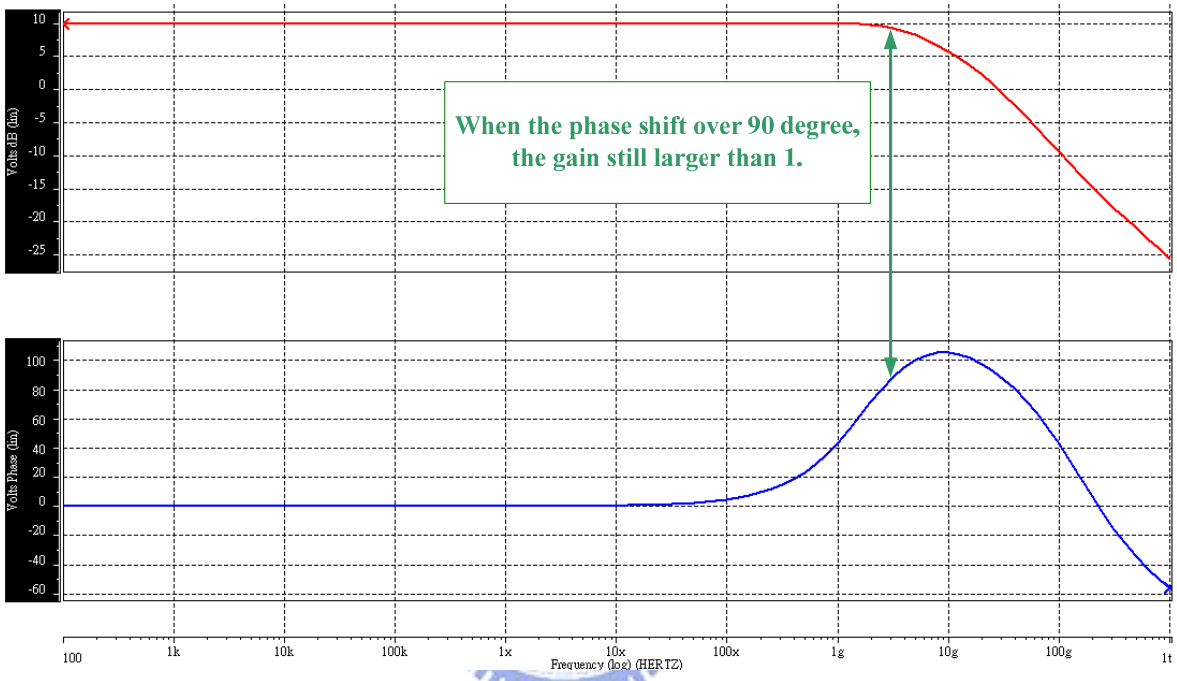


Figure 4.11 The frequency response of the proposed differential delay cell

The second step is to verify if the changes in one input phase must let the both two output phase change. We would easily find out that even if there is only one disturbance in one input of the differential delay cell, both the outputs of the differential delay cell which satisfy the first demand and has the regeneration latch would fit the second requirement. The stronger the positive feedback is, the faster response happened in the differential outputs. Fig 4.12 below is the input and output signals of the proposed differential delay cell. We only input a sine wave signal to the V_{i+}, and the V_{i-} is a common mode voltage. Both the differential outputs would have the differential signals.

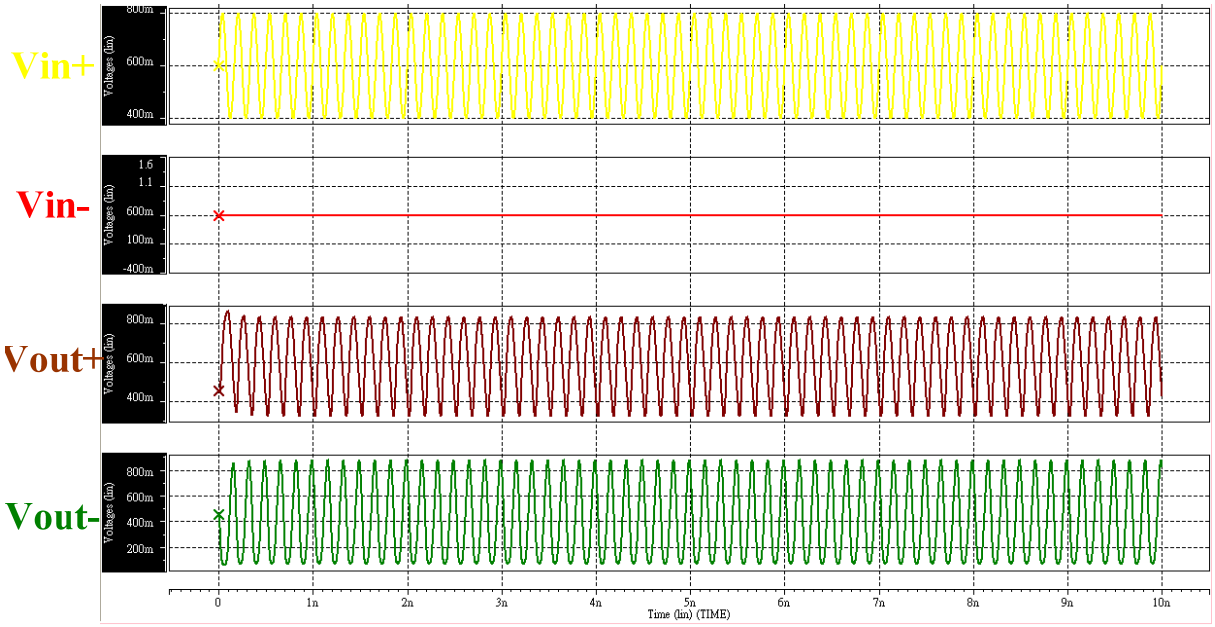


Figure 4.12 The input and output signals in differential delay cell with only one input signal.

The verification of the differential delay cell would make sure that the ring oscillator would oscillate or not. The other conditions of the differential delay cell would let the ring oscillator has better performance. We could design it as a reference.

The ring oscillator we need to operate in phase lock loop should output the signal for the architecture of the UWB frequency synthesizer. The output frequency of this PLL is 7128 MHz. That means the central frequency of the voltage control ring oscillator should be 7128 MHz. The intervals between the central frequency and the upper and lower operation frequency set up at least 1 GHz bandwidth. And let the central frequency in linear range of the VCO gain.

The MOS device size of the cross couple pair, regeneration latch would affect the oscillation frequency. The smaller device size of the latch is, the weaker locking ability to the differential output frequency is. That would let the differential output signals change their voltage states easier and faster, and the oscillation frequency goes higher. However, if the regeneration coupling ability is not powerful enough, the phase variation in single input

cannot transfer to the phase response in differential outputs. We estimate that the output loading of the ring oscillator buffers would be smaller than 100fF, so we put a 100fF capacitance in the output of each stage of the differential delay cell. That contains the wire loading and the loading of PADs.

The transient situation in output of the ring oscillator at 7128 MHz is shown in Fig 4.13 below. The common mode voltage is 0.6979 V, and the amplitude of the output signal is 0.4459 V.

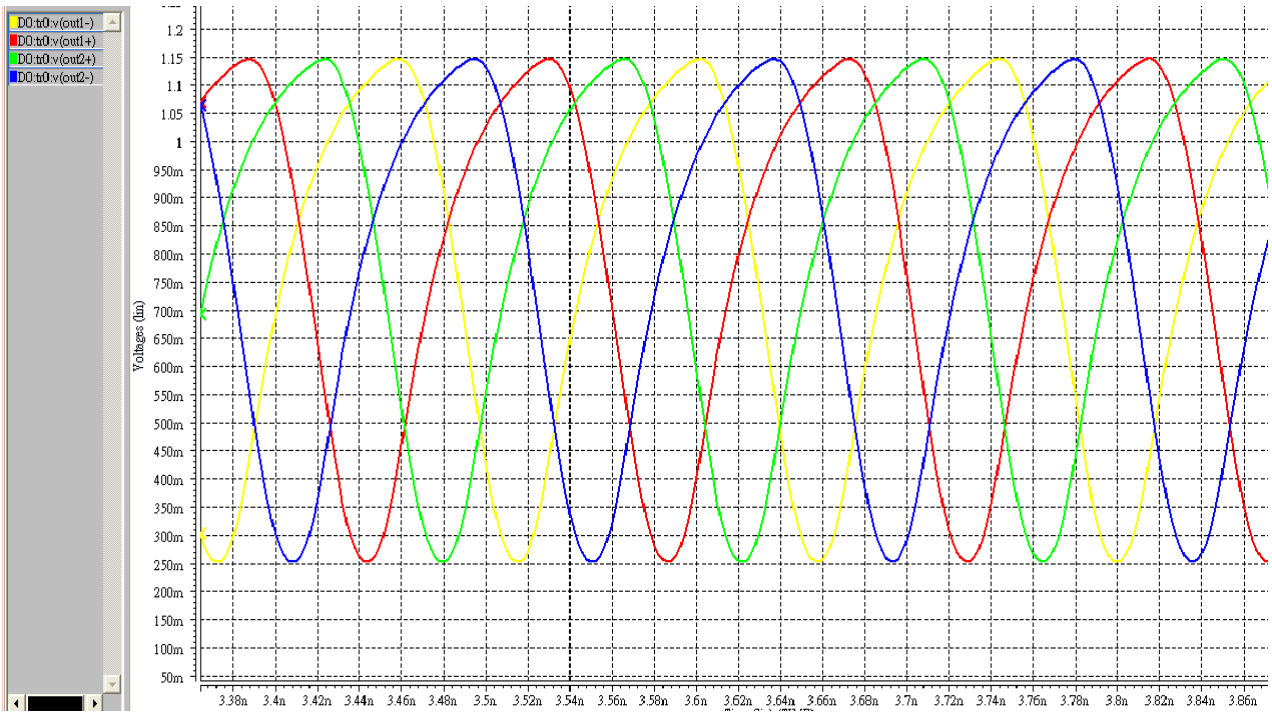
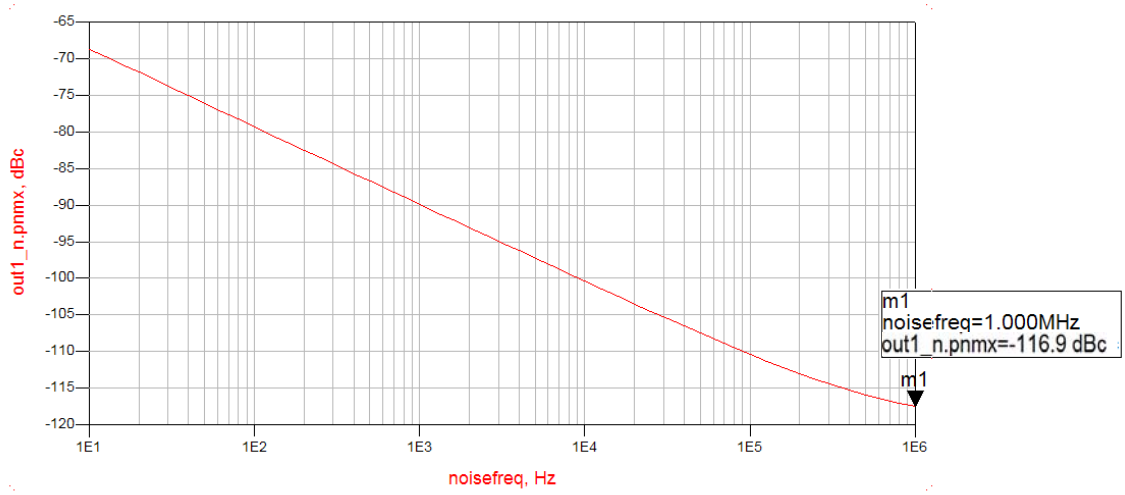


Figure 4.13 The transient results of the ring oscillator at 7128 MHz

Simulation results as shown in fig 4.14 are the phase noise of the two-stage voltage controlled ring oscillator at 7128 MHz. The VCO with loop filter phase noise is -116.9dBc/Hz at 1MHz frequency offset. It is adequately satisfying the specification of the UWB application, -96.5 dBc/Hz at 1 MHz frequency offset.



rin Figure 4.14 The phase noise of the two-stage g oscillator

Fig 4.15 below shows the output frequency tuning range, which is from 5.8 GHz to 8.8 GHz. For the designed frequency band, the average gain of VCO is about -4.43 GHz/V. The current consumption of the two-stage voltage control oscillator is 10.35mA, thus its power consumption is 12.42mW. And the current consumption of the two output buffers is 8.49mA, and the power consumption is 10.19mW.

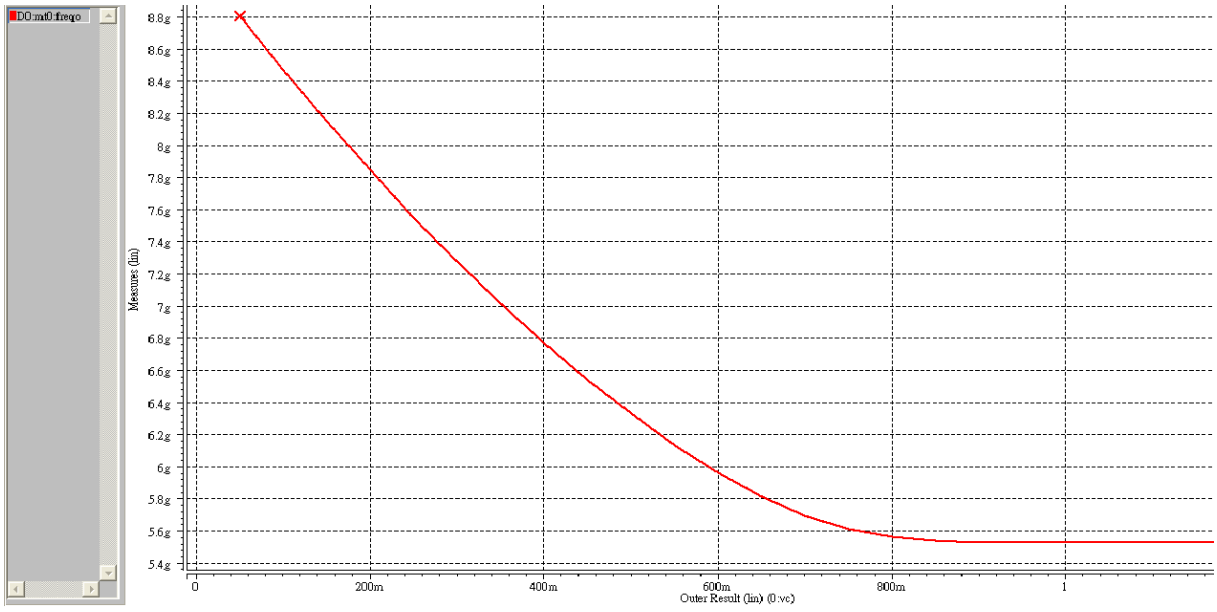


Figure 4.15 The tuning range of the two-stage ring oscillator

The output power spectrum of the two-stage voltage controlled ring oscillator is shown in fig 4.16 below.

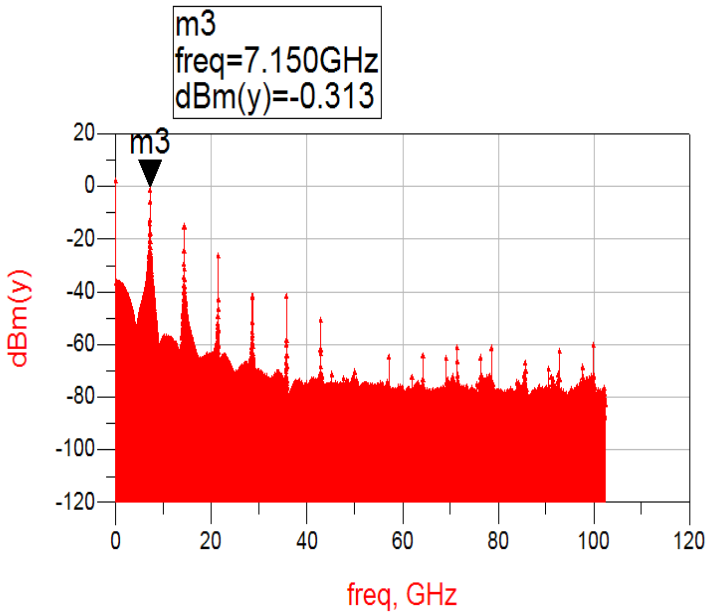


Figure 4.16 The output spectrum of the two-stage ring oscillator

Finally, the verification of the process variation would be considered. The sensitivity of the two-stage ring oscillator under FF and SS corners is depicted in fig 4.17. Both of the FF and SS corner could oscillate and they also cover the 7128 MHz.

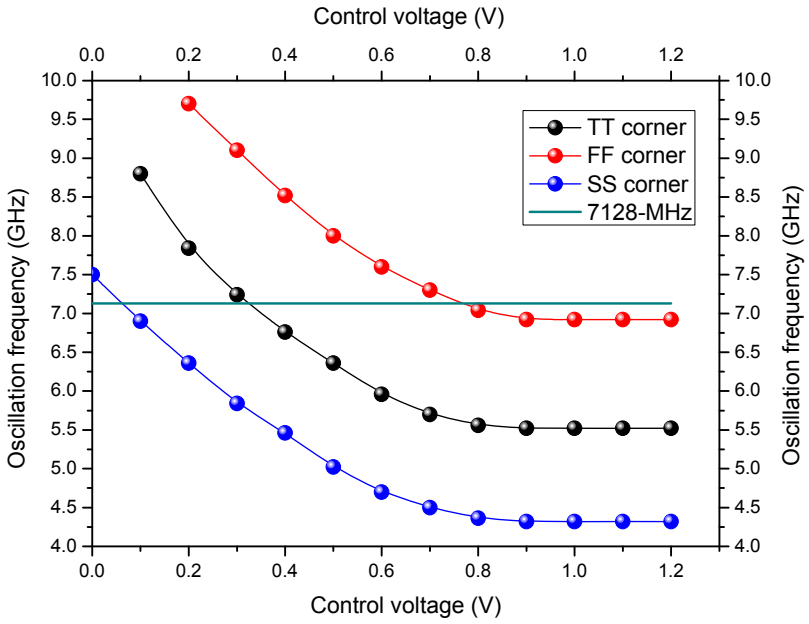


Figure 4.17 The tuning range of the two-stage ring oscillator at 7128 MHz under TT, FF and SS corner

The summary and comparison of the proposed two-stage voltage control ring oscillator is shown in Table 4.1 below.

Table 4.1 The summary and comparison of the proposed oscillator

	This work	[25] *ISCAS2004*	[37] *ISCAS 2005*	[38] *CICC2007*
Architecture	**Ring**	**Ring**	**Ring**	**Ring**
Output phase	**quadrature**	**quadrature**	**quadrature**	**quadrature**
Tuning range (GHz)	**5.8~8.8**	**0.2~2.1**	**8.4~10.1**	**1.05~1.45**
Supply Voltage	**1.2 V**	**3.3 V**	**1.8 V**	**1.2 V**
DC Power (mW)	**12.42**	**7.01**	**100**	**8.58**
Phase noise (dBc/Hz)	**-117.6@1MHz**	**-90@0.1MHz**	**-99.9@1MHz**	**-88@1MHz**
K_{VCO} (GHz/V)	**-4.43**	**1**	**1.13**	**0.38**
Output power (dBm)	**-0.313**	**none**	**none**	**none**
Technology	**TSMC 0.13µm CMOS**	**0.35µm CMOS-AMS**	**TSMC 0.18 µm CMOS**	**TSMC 0.13µm CMOS**

4.2 Prescaler and Dividers

In this work, the programmable integer-N frequency divider is based on a simple divider chain. The division number of the PLL is 108 which are formed by two divide by 2 and three divider by 3. The divider chain is connected between the output of the ring oscillator and one of the phase frequency detector's input. The design issues of the prescaler and the dividers are presented as follws:

4.2.1 Operational Principle

The prescaler and the dividers in this work are used the conventional structures which are widely utilized in nowadays IC design. The divided_by_2 circuits are based on a D flip-flop architecture shown in fig 4.18 below, which is superior at its wide input frequency range and can operate down to a very low frequency [29]. The divided_by_2 frequency dividers employ two D-latches in a master-slave configuration with negative feedback. One of the latches is positive clock cycle triggered, the other is negative one. In high speed master-slave dividers, it is common practice to design the slave as the "dual" of the master so that they could be both driven by a single clock. However, duality requires one of the latches to incorporate PMOS devices in the single path, hence lowering the maximum speed. To avoid the problem, the divider could be driven by two complementary clocks and the skew on each single path must be minimized [30].

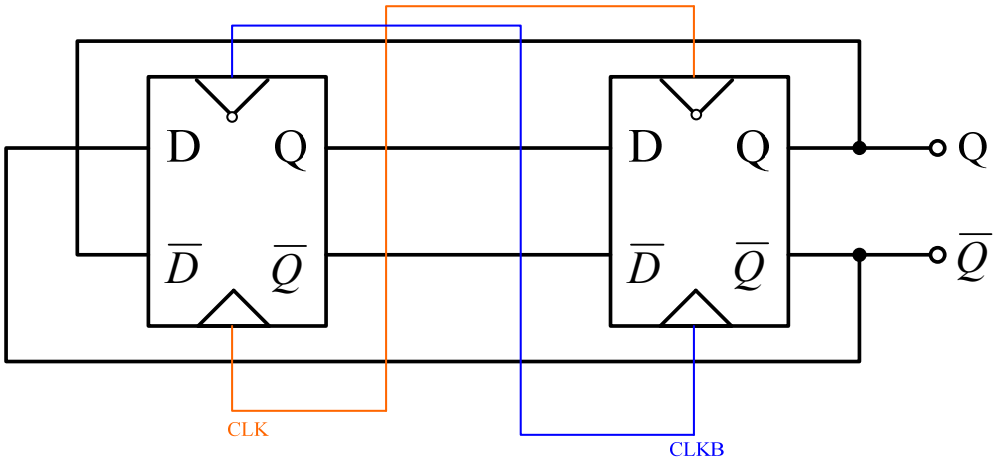


Figure 4.18 The architecture of the D flip-flop based divide_by_2 frequency divider

The divide_by_3 frequency dividers are also based on two D flip-flops but the addition of an AND gate between the two D flip-flops. That could let the latches lock the clock cycle later half a period to achieve the goal of divide_by_3. Besides this, the other operational principles are the same as the divide_by_2 frequency dividers. The architecture of the divide_by_3 circuit is show in fig 4.19 below.

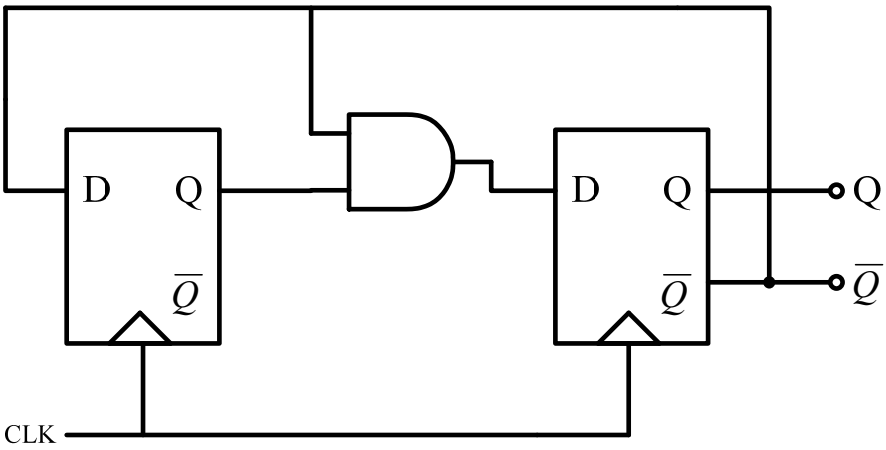


Figure 4.19 The architecture of the D flip-flop based divide_by_3 frequency divider

4.2.1 Design Consideration [32], [39]

The divider is designed to self-oscillate, that is if the input amplitude is set to zero, the output will still oscillate at some frequency. This is a desirable characteristic that the divider operates correctly with low input amplitude at its input frequency near 2 times the self-oscillating frequency. Furthermore, the required minimum amplitude for input signal increases as its frequency deviates from self-oscillating frequency which limits its operating range of the divider. For the input signal given at some frequency without sufficient amplitude, it would cause the divider malfunction. Therefore, output signal frequency would not be the half of the input signal frequency. While the minimum tolerable input amplitude is associated with the input MOS size of the divider [31], the large size of it results the smaller input required amplitude, nonetheless, this also results in a extra loading capacitance of proceeding stage degrading the speed of self-oscillating frequency.

Due to the output frequency of the 2-stage ring oscillator is at a high frequency, 7128 MHz, the prescaler and the divide_by_2 divider would choose the dynamic current mode architecture that would increase the speed of the frequency division. The output of the oscillator is as the clock cycle of the D flip-flop in fig 4.18, therefore, the first cycle of the oscillator would change the output of the positive cycle triggered latch to import to the negative cycle trigger latch. And it must wait until the second cycle of the oscillator come, the output of the negative cycle triggered latch would change. Thus it could be seen that the oscillator changes two clock cycles, and the divide_by_2 changes only one. Therefore it achieves the ability of divide_by_2. The dynamic D flip-flop among the divide_by_2 frequency divider is as fig 4.20 below. The V_B is the bias voltage of the latches.

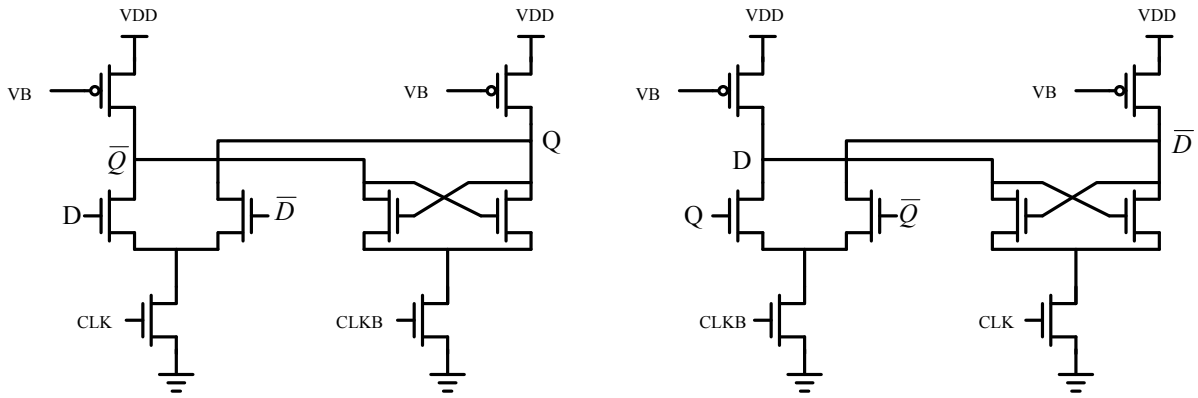


Figure 4.20 The circuit diagram of the dynamic D flip-flop for the divide_by_2 frequency dividers

Using the left positive cycle triggered latch as the example, when the clock cycle is positive, the differential pair would preliminarily separate the outputs, Q and $\overline{Q}$ according to the height of the D and $\overline{D}$. While the negative clock cycle comes, the separated outputs, Q and $\overline{Q}$ would be apart from each other further by the positive feedback cross couple pair. The operating principle of negative clock triggered latch is almost the same as the positive one, but the difference between the positive or negative clock cycles.

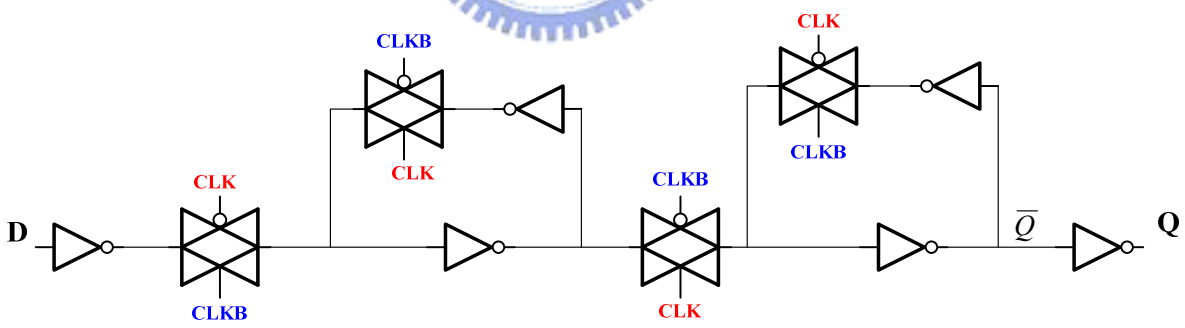


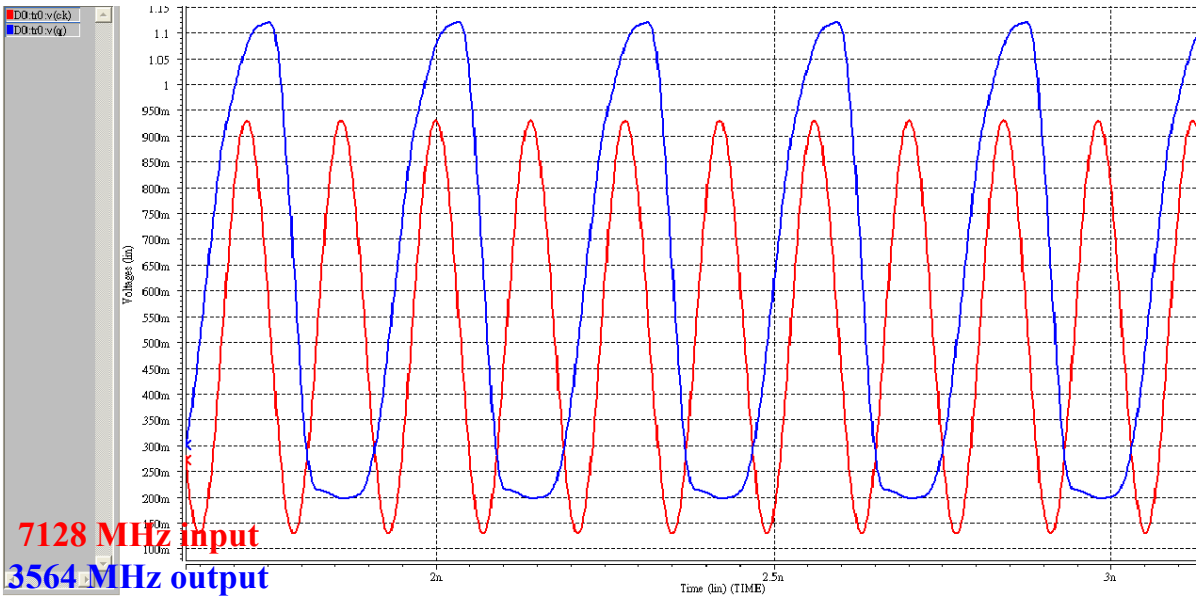
Figure 4.21 The static D flip-flop for the divide_by_3 frequency dividers

Owing to the output signal of the ring oscillator cross the two divide_by_2 frequency dividers would be lower frequency ($7128 \div 2 \div 2 = 1782$ MHz), the structure of the dynamic current mode latch would cost too much power consumption. The static logic D flip-flop based dividers could be adopted to save the power consumption. Fig 4.21 shown above is the

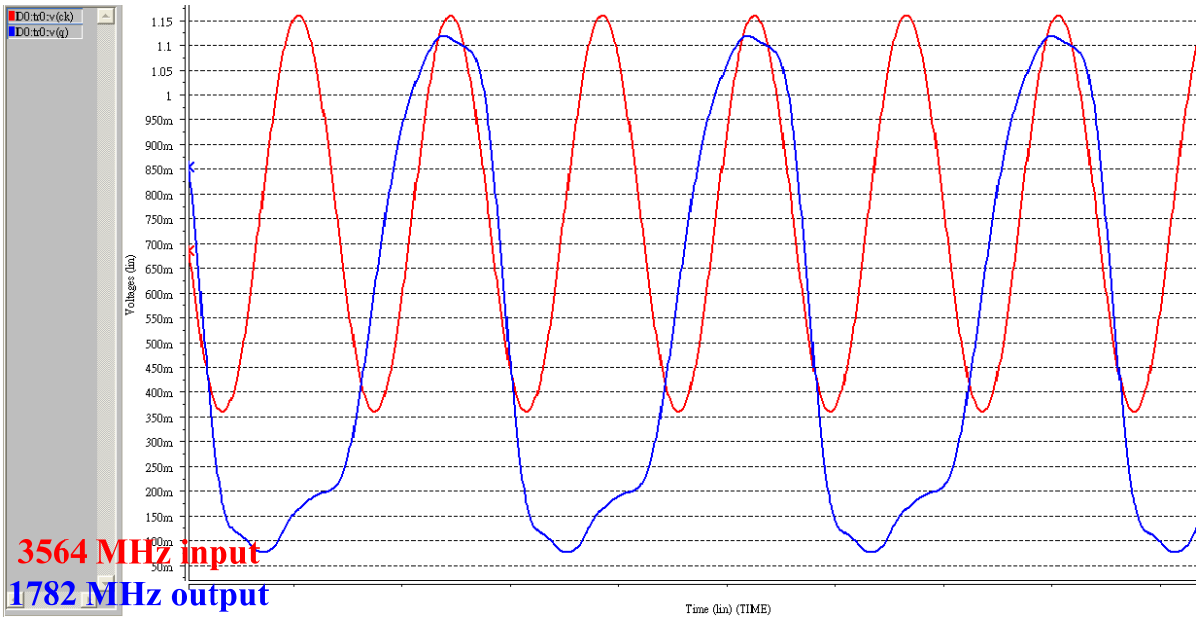
architecture of the D flip-flop for the divide_by_3 frequency dividers. It is made from transmission gates and inverters that the ratio of the PMOS and NMOS equals 2. The AND gate in fig 4.19 is used the conventional complementary structure. The followings is the simulation results of the prescaler and dividers.

4.2.3 Circuit Realization

Fig 4.22 (a) shows the simulation results of the prescaler with input frequency, 7128 MHz, and fig 4.22 (b) is the simulation result the next divide_by_2 frequency divider with 3564 MHz input signal. In the waveforms, the functions of the dividers work correctly. The average current consumption of the prescaler is 2.17 mA, thus the power consumption is 2.61 mW. The next divide_by_2 divider cost current 0.96 mA, and the power consumption is 1.15 mW. The minimum input amplitude of the both dividers could be smaller than 10 mV at the objective input frequency, 7128 MHz and 3564 MHz, and they could function correctly between the range that input frequency add or subtract 1 GHz under input amplitude 100mV.



(a)

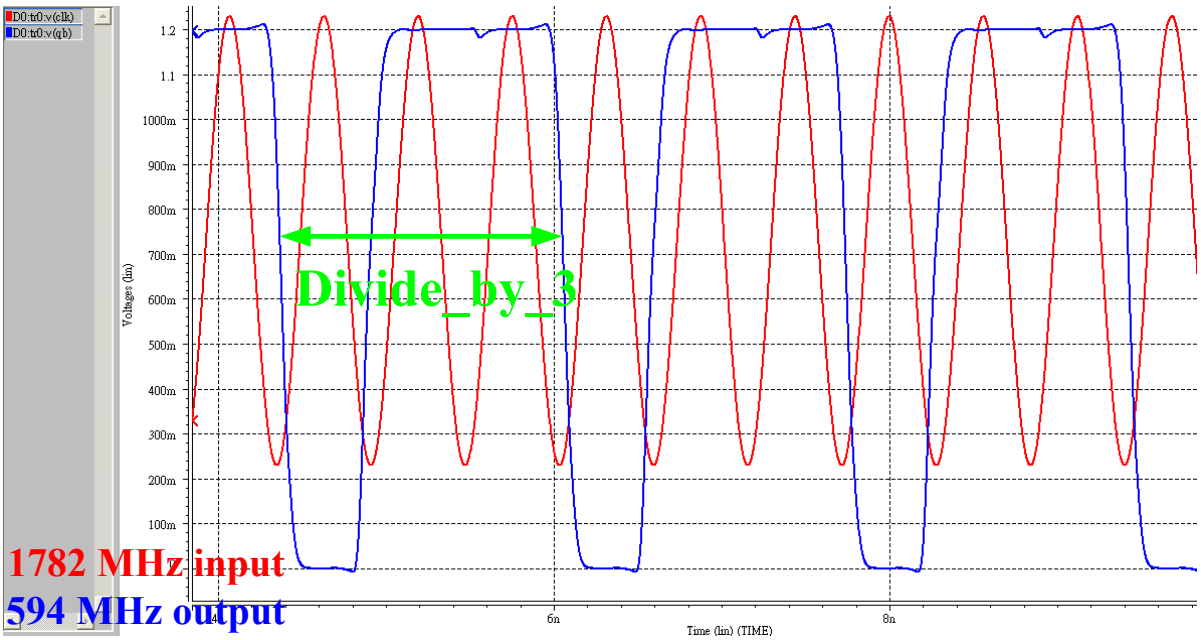


(b)

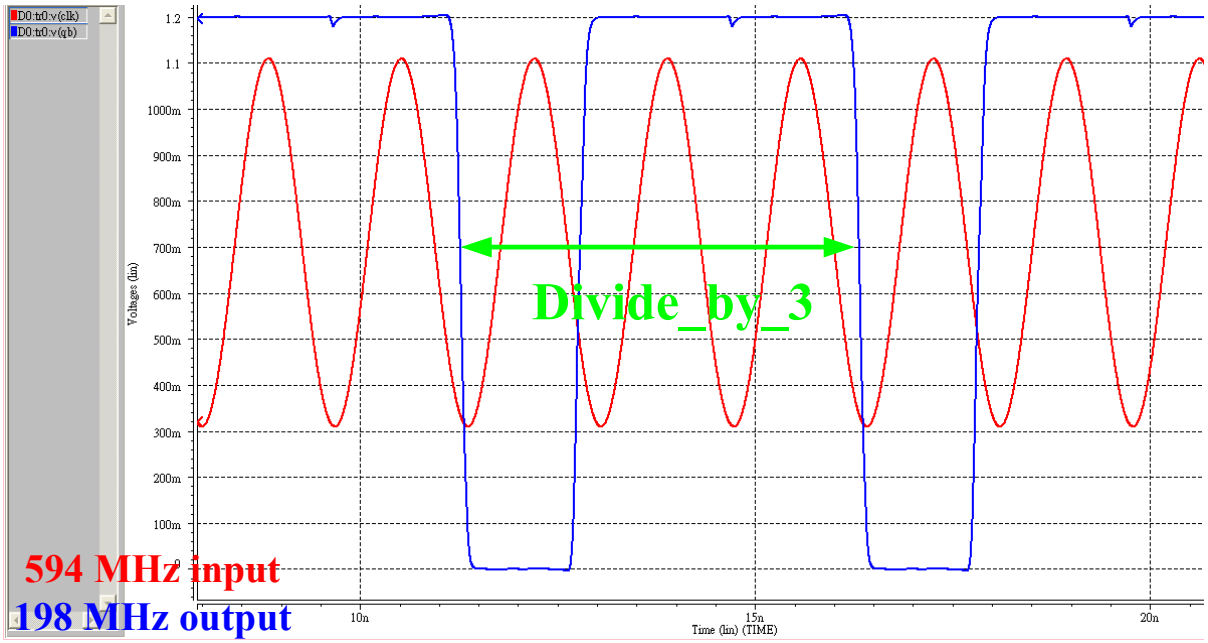
Figure 4.22 The simulated waveforms of (a) prescaler, and (b) divide_by_2 frequency divider

Fig 4.23 (a) shows the simulation results of the first divide_by_3 frequency divider connected after the divide_by_2 frequency divider with input frequency, 1782 MHz, and fig 4.22 (b) is the simulated waveform of the second divide_by_3 frequency divider with 594 MHz input signal. Finally, the last divide_by_3 frequency divider is connected between the

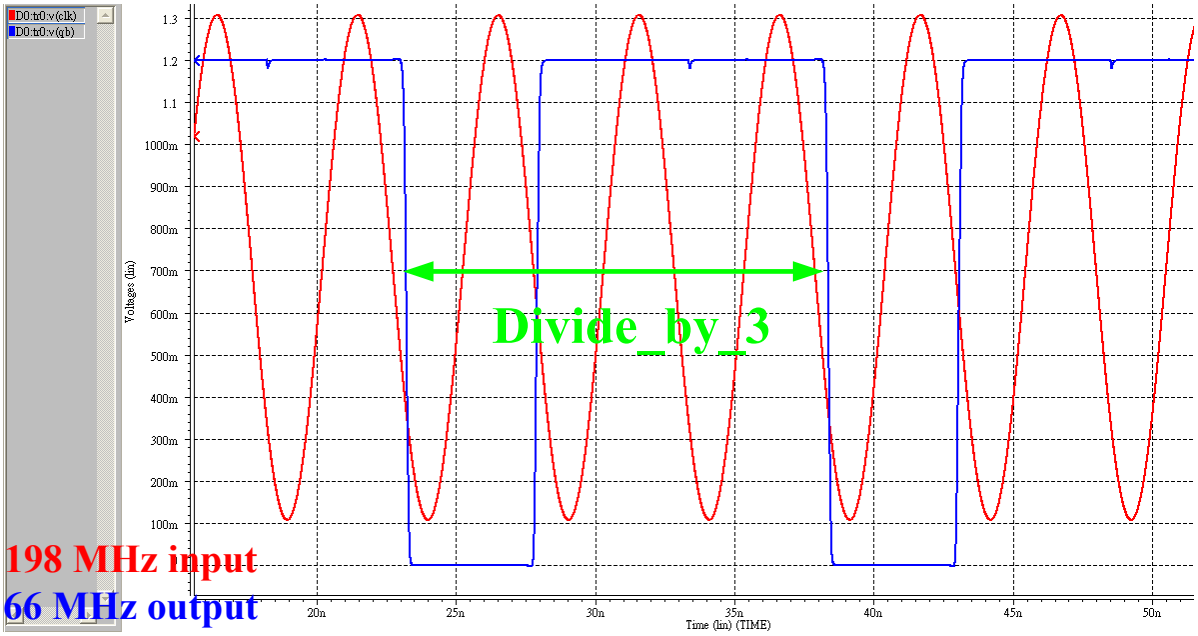
second divide_by_3 and PFD with input frequency, 198MHz. In the waveforms, the functions of the dividers work correctly. The average current consumption of the 1st divider is 0.54 mA, thus the power consumption is 0.64 mW. The 2nd divide_by_3 divider cost current 0.15 mA, and the power consumption is 0.18 mW. The current consumption of the last divide_by_3 divider is 0.049 mA, and the power consumption is 0.059 mW. The minimum input amplitude of all the divide_by_3 frequency dividers could be smaller than 30 mV at the objective input frequency, 1782 MHz, 594 MHz, and 198 MHz. They could function correctly between the range that input frequency add or subtract 30% themselves under input amplitude 300mV.



(a)



(b)



(c)

Figure 4.23 The simulated waveforms of (a) the first, (b) the second, and (c) the last divide_by_3 frequency dividers

Finally, we connect the two-stage voltage control ring oscillator and the divide_by_108 frequency divider. The total current consumption of the oscillator and dividers are 22.75 mA,

thus the power consumption of them are 27.30 mW. The simulated waveforms function correctly in the fig 4.24 below.

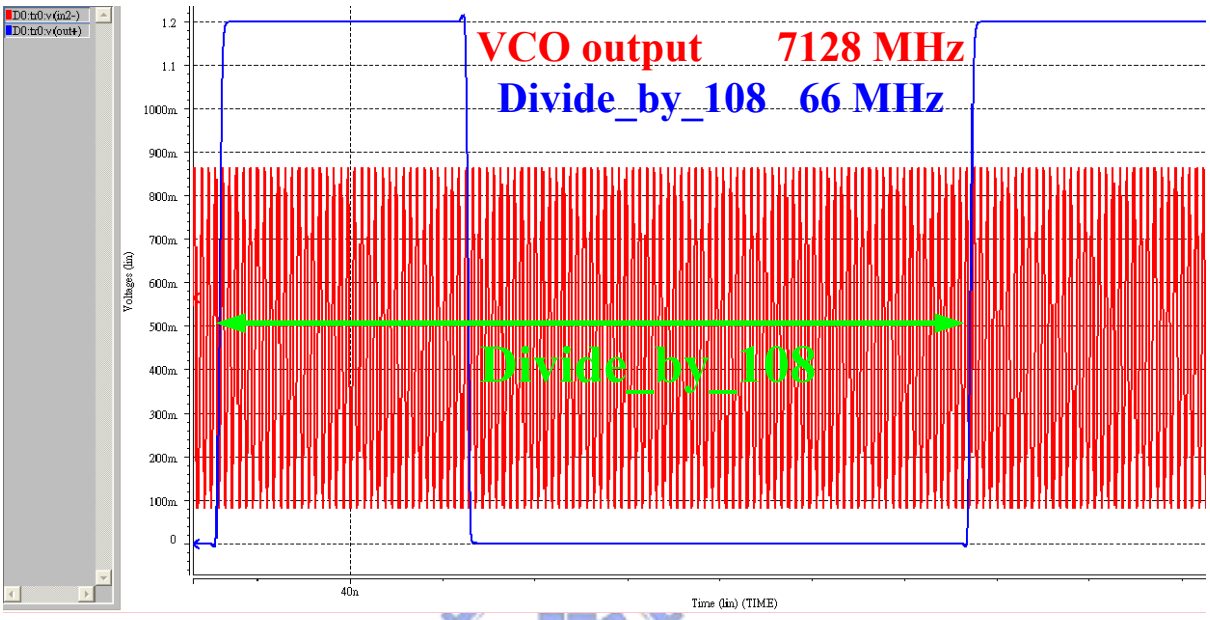


Figure 4.24 The simulated waveforms of the ring oscillator and the divide_by_108

4.3 Phase and Frequency Detector

The phase and frequency detector (PFD) could detect the difference of the phase and frequency between the input reference frequency and the divided frequency. It mainly detects the phase differences for the charge pump to revise the output frequency of the oscillator, so it could also be called phase detector, PD. The followings are the operational principle of the conventional phase and frequency detector we utilized.

4.3.1 Operational Principle

Nowadays, the common phase detectors can be categorized to three types: the analog multiplier-type, the XOR-type, the sequential-type. However, the analog multiplier-type phase detector exhibits the nonlinear dependence of the output voltage on the phase difference and the instability, resulting from the inverted gain polarity beyond the phase difference range, ± π/2. Concerning the XOR-type phase detector, the instability issue still exists except for the nonlinear dependence.

Unlike the multiplier-type and XOR-type, which are only phase-sensitive, the phase-frequency detector (PFD) is a sequential phase detector triggered by else the rise or fall edge of the reference signal and the divided signal. As the result, the PFD has the capability of operating as a frequency discriminator for large frequency errors or as a coherent phase detector once inside the pull-in range of the PLL, allowing a fast frequency acquisition and a full linear phase difference range, ± 2π shown in fig 4.25 below.

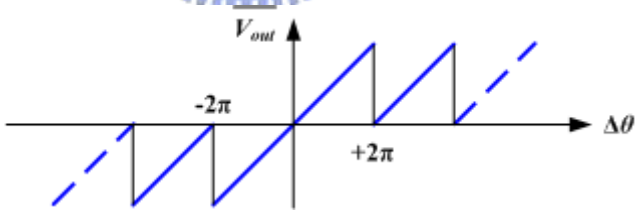


Figure 4.25 The characteristic of the phase and frequency detector

As illustrated in fig 4.26 below, the operation of a typical PFD is as follows. If initially UP = DN = 0, then a rising transition on reference frequency leads to UP = 1, DN remains *0*. The circuit remains in this state until the divided frequency goes high, upon which UP returns to zero simultaneously. The behavior is similar for the divided signal input. Thus, the average dc value of (UP-DN) is an indication of the frequency or phase difference between reference signal and divided signal.

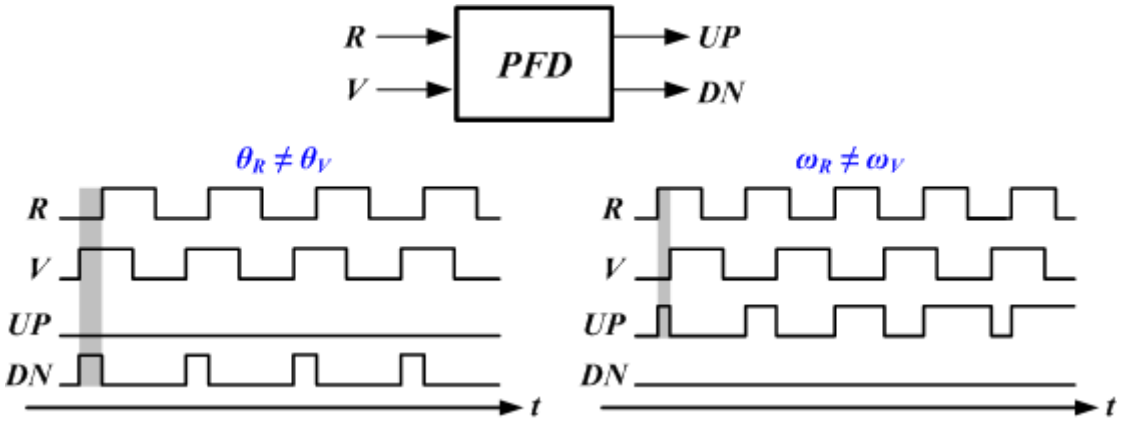


Figure 4.26 The conceptual operation of phase and frequency detector

To achieve a PFD with the above behavior, at least, three logical states are required: UP = DN = 0 (state 0); UP = 1, DN = 0 (state I); UP = 0, DN = 1 (state II). Fig 4.27 below shows a state diagram summarizing the operations. If the PFD is in the state 0, then a transition on reference signal takes it to state I. During state I, any more rising edge on reference signal would not changes the state at all. The PFD will remain in this state until a transition occurs on divided signal, upon which the PFD returns to state 0 immediately. The switching sequence between state 0 and state II is similar. Such a PFD is called "tri-state phase-frequency detector".

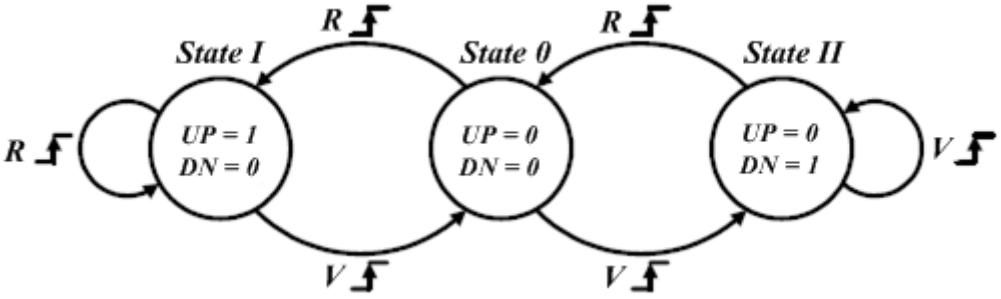


Figure 4.27 The state diagram of the tri-state phase and frequency detector

4.3.2 Design Consideration

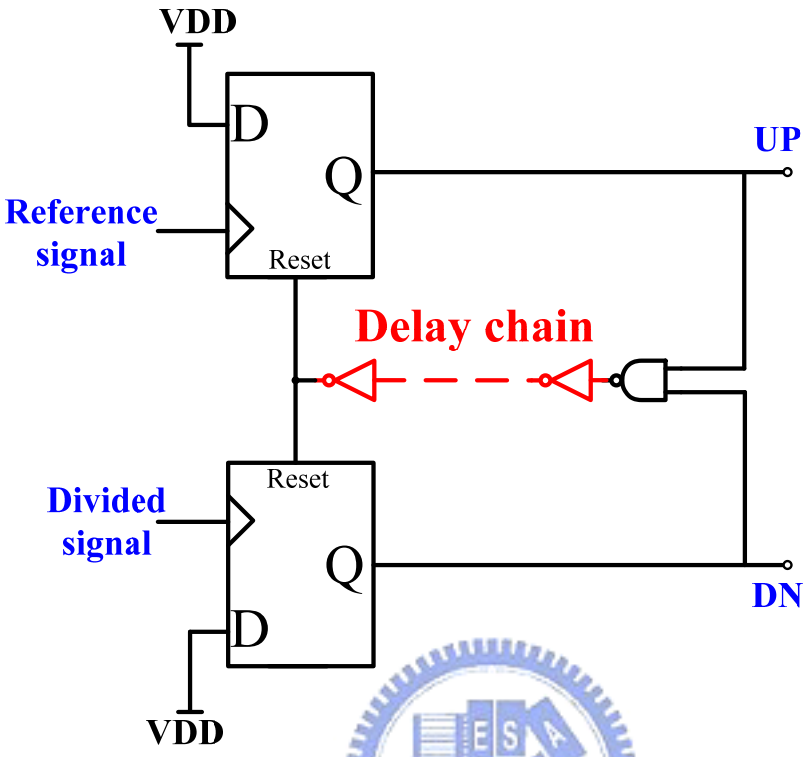


Figure 4.28 The structure of the tri-state phase and frequency detector

Fig 4.28 upon is the structure of the tri-state phase and frequency detector. It includes two edge-triggered, resettable D-type flip-flops (DFFs), a delay chain, and an NAND gate. Note that the use of the edge-triggered DFFs is to avoid the dependence of the output upon the duty cycle of the inputs.

The D inputs of the flip-flops are tied to logic one (VDD). Reference signal and divided signal act as the clock inputs of the two DFFs, respectively. A positive transition in the input of the reference signal sets the output UP “high”. Similarly, a positive transition in the input of the divided signal sets the output DN “high”. When both UP and DN are simultaneously “high”, a reset pulse generated by the NAND gate and inverter chain as “AND” resets both flip-flops, which brings UP and DN to low and then terminates the reset pulse. In order to eliminate the dead-zone, a delay chain has been introduced in the reset path, so that minimum

width pulses are always present in the outputs UP and DN when the inputs are in phase. That would increase the response time for charge pump to minimize the influence of the reference spurs.

The circuit architecture of the D-type flip-flops in the proposed phase and frequency detector is shown in fig 4.29 below. It is a true single phase circuit (TSPC) structure that could increase the linearity, decrease the switching time, and has simple circuit structure.

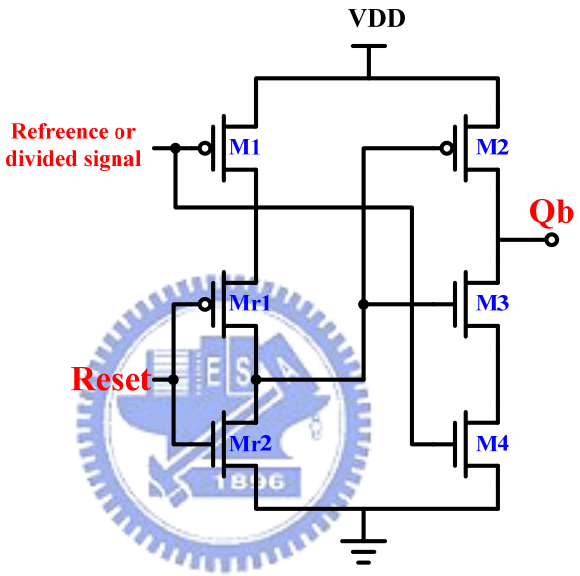
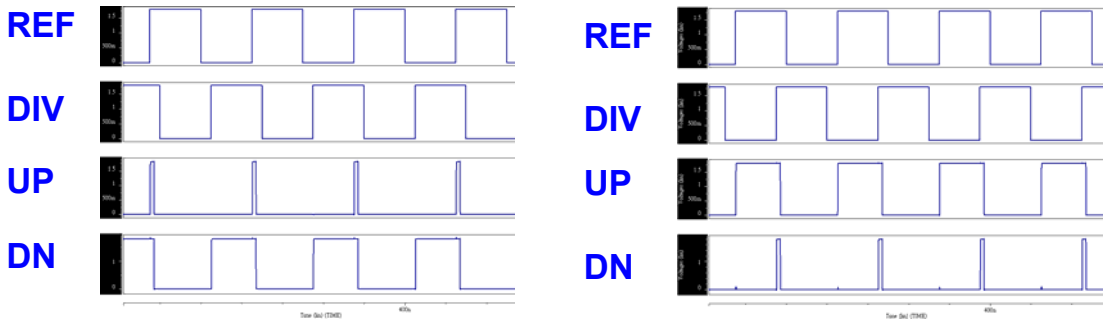


Figure 4.29 The structure of the TSPC D-type flip-flop in phase and frequency detector

4.3.3 Design Consideration

Fig 4.30 shown below is the simulation results of the phase and frequency detector. Fig 4.30 (a) is the simulated waveform of the divided frequency leading to the reference frequency, thus the PFD would generates the discharging signal for the charge pump to lower the control voltage of the oscillator. That would let the oscillation frequency decrease and then reduce the divided frequency. On the other hand, fig 4.30 (b) is the simulated waveform of the divided frequency lagging reference frequency. The PFD would generate the discharging

signal for the charge pump to raise the control voltage of the oscillator. That would let the oscillation frequency increase proceed to heighten the divided frequency. The average power consumption of the proposed phase and frequency detector is about 0.2 mW. The phase characteristic (linear range) at 100 MHz is $\pm 2\pi$, and at 500 MHz is $\pm 1.65\pi$. These are presented in Table 4.2 shown below.



(a) (b)

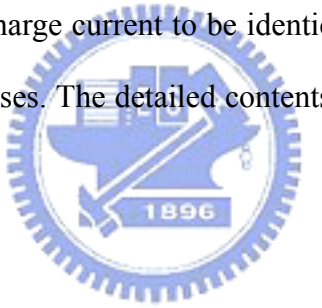
Figure 4.30 The simulated waveform of phase and frequency detector at (a) divided frequency leading to reference frequency, and (b) divided frequency lagging reference frequency

Table 4.2 The summary and comparison of the PFD for the important characteristics

		[33]	[34]	This Work
Maximum Frequency		1.53 GHz	1.7 GHz	500 MHz
Power		~1.4 mW	~4.5 mW	0.2 mW (ave)
Phase Characteristic (Linear range)	@0.1GHz	none	± 2π	± 2π
	@0.5GHz	± 1.8π	none	± 1.65π
	@ 1 GHz	none	± 1.3π	none
Technology		CMOS 0.25 μm	CMOS 0.18 μm	CMOS 0.13 μm

4.4 Charge Pump

The ability of the charge pump is to charge or discharge the energy of the loop filter. When the phase and frequency detector gives the charge signal (UP), the charge pump would charge the loop filter in order to raise the control voltage of the oscillator. That would increase the oscillation frequency of VCO. On the other hand, it would discharge it to lower the control voltage. The main design key is to increase the matching between the charge and discharge current. This is because the difference between charge and discharge current would generate some residue current during the compared cycle period of PFD. The residue current would cause the variation of control voltage periodically. That makes the output of the frequency synthesizer generating the reference spur seriously. The other design key is to ensure the stability of the charge and discharge current to be identical, so there would not have the over charging or over discharging cases. The detailed contents of charge would be presented in the following.



4.4.1 Operational Principle

A PFD couldn't alone provide the exact voltage (or current) signal proportional to the phase difference at its inputs. A charge pump serves to convert the difference of the two output signal UP and DN of the PFD into the corresponding error current either sourced to or sunk from the loop filter, depending on the state of the switches S_U and S_D controlled by UP and DN, respectively. No current flows through the loop filter if both switches are off and the output node represents an infinite-impedance towards the loop filter.

A charge pump (CP) with a PFD and a capacity C_P as the loop filter is shown in fig 4.31, which illustrates the corresponding time-domain response. One should note that the system is

nonlinear and discrete time in the strict sense. To overcome this quandary, it could be approximated by a continuous-time model only when the loop bandwidth is much less than the reference frequency [35]. Therefore, the characteristic of the PFD and charge pump can be together approximated linearly as:

$$\overline{I_e} = I_P \cdot \frac{\Delta\theta}{2\pi} \tag{4-10}$$

where $\overline{I_e}$ is the average error current over a cycle, $\Delta\theta$ represents the phase error between the PFD inputs and $I_P = I_1 = I_2$ is the current value of the two current sources in the charge pump.

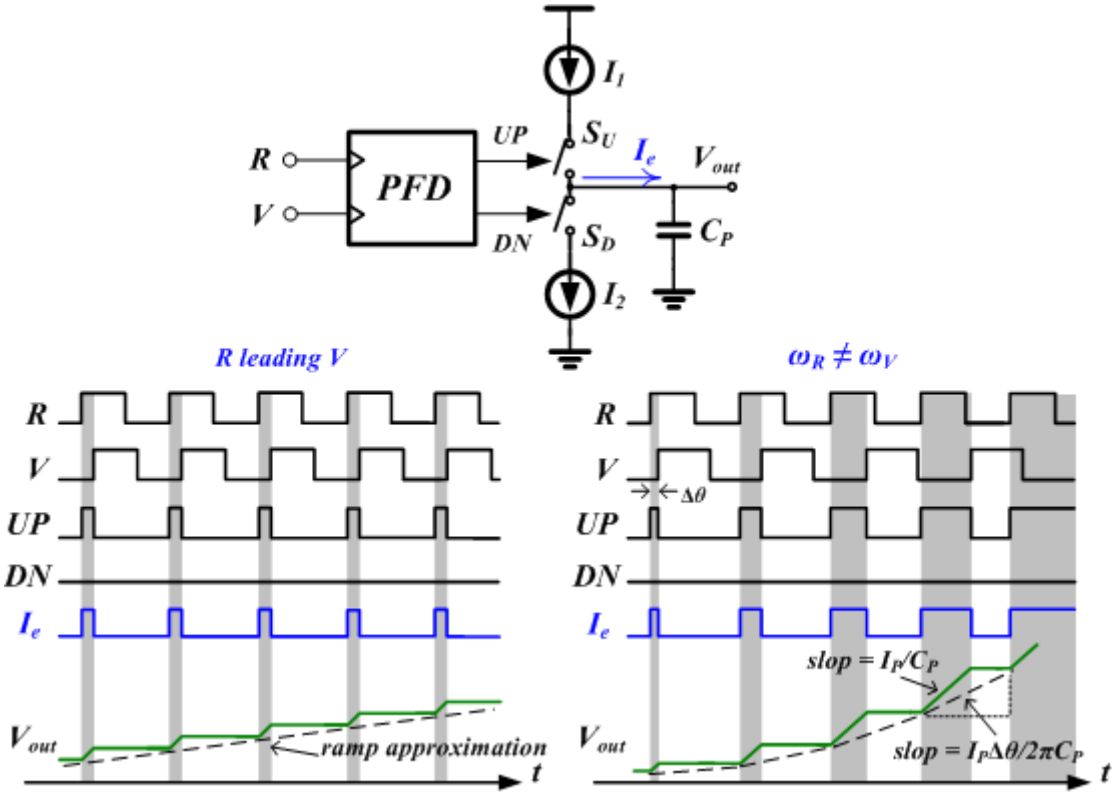


Figure 4.31 The block diagram of the PFD and charge pump with the timing diagrams.

4.4.2 Design Consideration [36]

Because of the effect of the channel length modulation, the charge current I_{up} and discharge current I_{down} of the conventional current-steering charge pump circuit could not match in whole range of the oscillator control voltage. Even if the PMOS and NMOS of the output stage in charge pump are sizing as the rate of their mobility ratio and the same over-drive voltage, they still cannot fit in with the total control voltage range. At every reference clock edges, the I_{up} and I_{down} would both turn on for a very short time to cancel the dead zone effect of the PFD. If the I_{up} and I_{down} are not equal at this moment, the mismatch current will increase the spur level of the oscillator output spectrum.

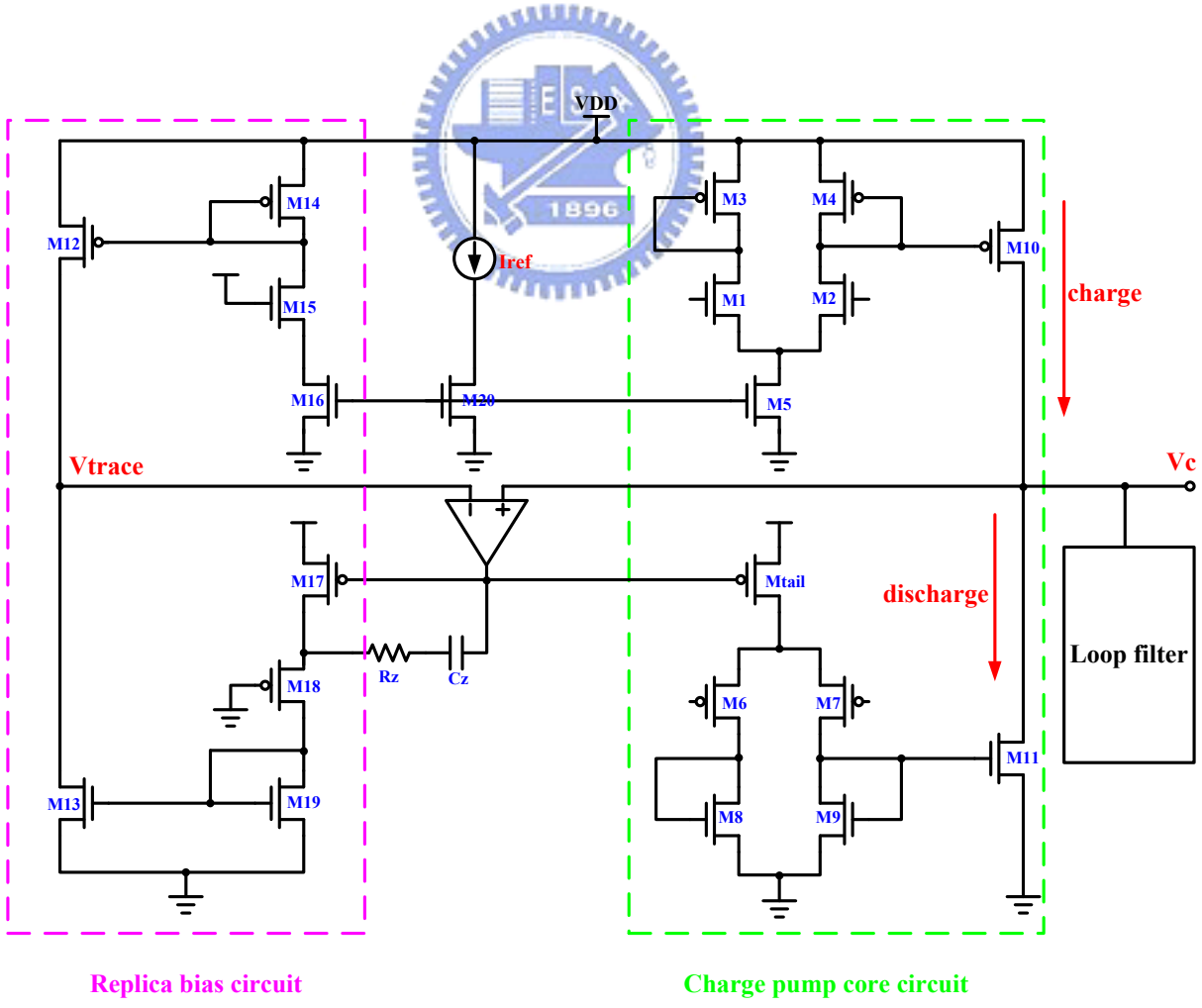
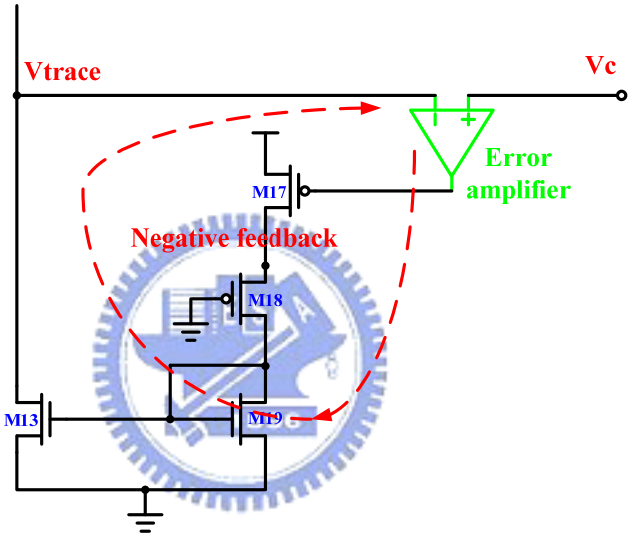
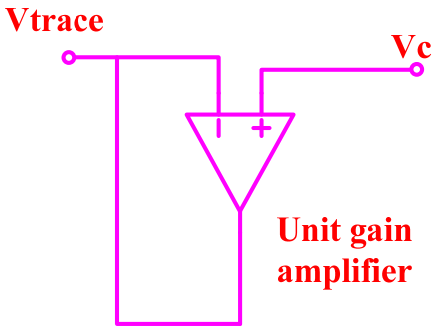


Figure 4.32 The current-match charge pump architecture used in this work

Fig 4.32 upon shows the current-match charge pump circuit which has a function could let the I_{up} and I_{down} tally with each other. The right part of fig 4.32 is the charge pump core circuit, and the left part is the replica bias circuit. This replica circuit is used to give the transistors M12 and M13 the same bias as M10 and M11. The replica bias circuit has a feedback loop which could tune the I_{up} fit in with the I_{down} automatically while the output of the charge pump is varying.



(a)



(b)

Figure 4.33 (a) The feedback loop of the charge pump, and (b) the equivalent circuit of the loop

Fig 4.33 (a) above shows the half circuit of Fig 4.32. The error amplifier and the other transistors form a negative feedback loop and we could view the error amplifier as the first stage. M17 is the amplifier of the second stage, and M18 in the triode region series connects with M19 in diode connection. The third stage is a common-source amplifier M13 with the output load $r_{o12} // r_{o13}$. The negative feedback would be equivalent to a unit gain buffer as fig 4.33 (b) upon. This would be a voltage follower buffer that the V_{trace} would trace the V_c voltage. The gain of the feedback loop would be analyzed as follows.

The gain of the error amplifier is A_{err} (negative value), and then the gain of the second stage, CS amplifier, is shown below:

$$A_2 = -g_{m17} \cdot \left(R_{18} + \frac{1}{g_{m19}} \right) \cdot \frac{\frac{1}{g_{m19}}}{R_{18} + \frac{1}{g_{m19}}} = \frac{g_{m17}}{g_{m19}} \tag{4-11}$$

Where R_{18} and $\frac{1}{g_{m19}}$ are the equivalent resistance of M18 in triode region and M19 in diode connection respectively.

The third stage of the loop is also a CS amplifier whose gain is as follow:

$$A_3 = -g_{m13} \cdot (r_{o12} // r_{o13}) \tag{4-12}$$

Then, the overall gain of the negative feedback loop is as:

$$A_o = A_{err} \cdot A_2 \cdot A_3 = A_{err} \cdot \frac{g_{m17} \cdot g_{m13}}{g_{m19}} \cdot (r_{o12} // r_{o13}) \tag{4-13}$$

The difference between V_c and V_{trace} is:

$$V_{err} = (V_c - V_{trace}) = \frac{1}{1 + A_o} \cdot \left(V_c - \frac{V_{DD}}{2} \right) \tag{4-14}$$

And the channel length modulation effect coefficient is λ, the maximum $\left(V_c - \frac{V_{DD}}{2}\right)$ is $\left(V_c - \frac{V_{DD}}{2}\right)_{\max}$. According to the square law of the MOS $I_D = \frac{1}{2}K\frac{W}{L}\cdot V_{OV}^2 \cdot (1+\lambda V_{DS})$, we could calculate the maximum mismatch of the charge and discharge current:

$$I_{diff} = \lambda \times V_{err} \times (I_{up} - I_{down}) = \frac{\lambda \cdot \left(V_c - \frac{V_{DD}}{2}\right)_{\max}}{1+A_o} \cdot (I_{up} - I_{down}) \quad (4\text{-}15)$$

The higher loop gain of the negative feedback is, the smaller current mismatch ratio is.

4.4.3 Circuit Realization [36]

There is a serious problem might happen in current-match charge pump which is shown in fig 4.32. The output of the error amplifier is a high impedance node that when supply voltage grows like a ramp of time and takes long time to reach V_{DD}, the V_c might be pulled up to approach V_{DD}. And the V_c would be out of the input range of the error amplifier, the error amplifier turns off. Therefore, the discharge part of the charge pump would disable and I_{down} becomes zero. PLL would fail to have correct function, and the output frequency would always keep low.

The proposed current-match charge pump is shown in fig 4.34 below. The added transistors M21 and M22 would give the discharge part of the charge pump a constant bias. It could suppress the V_c going to near V_{DD}, and the charge pump would never fail to function in low frequency.

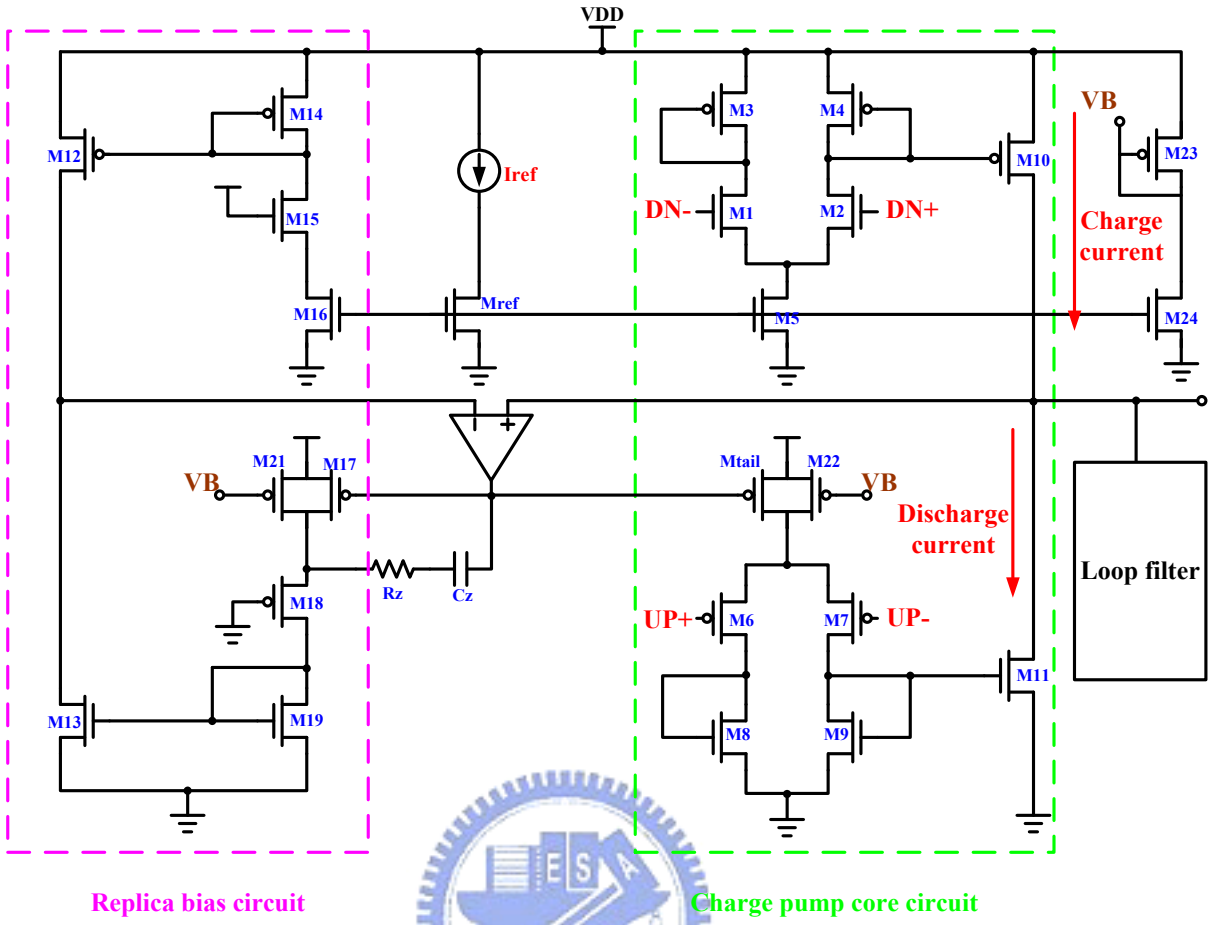
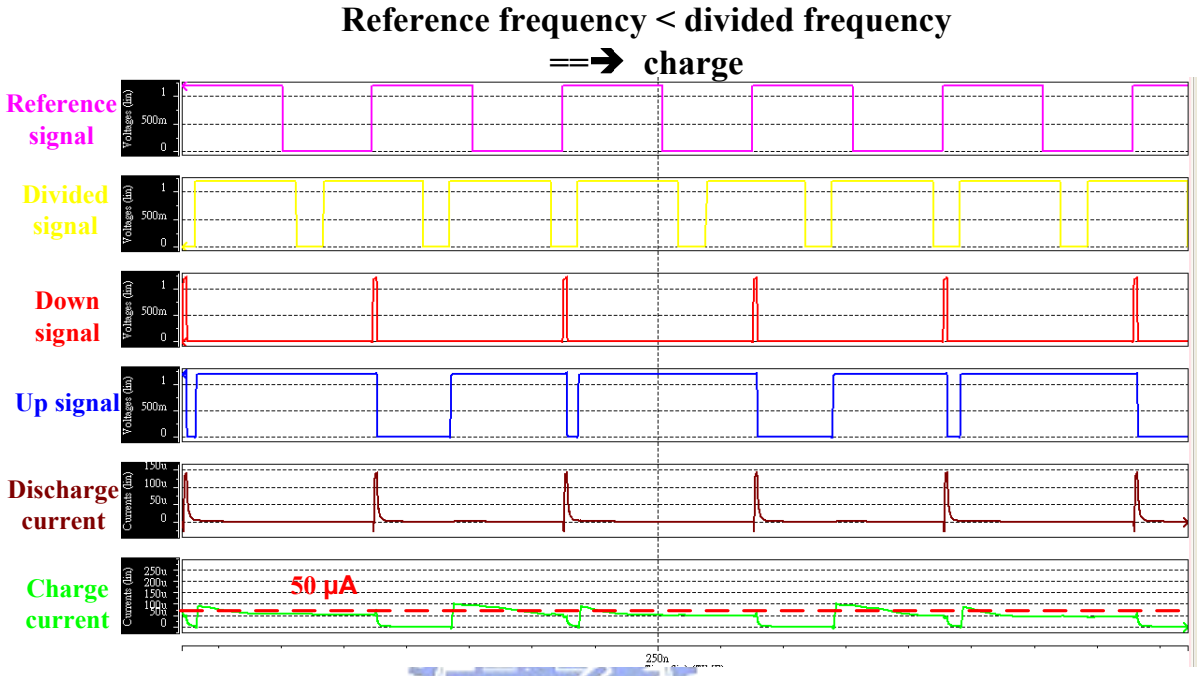


Figure 4.34 The proposed current-match charge pump with solved start-up problem

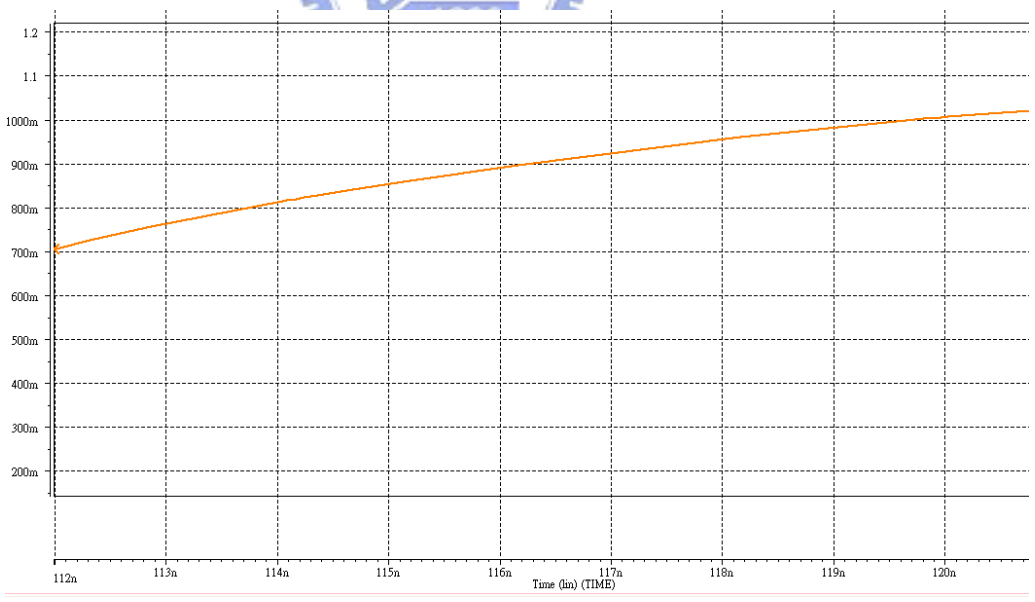
Because the gain of proposed two-stage voltage control oscillator is negative, the UP/DN signals are connected to the inputs reversely. To increase the output frequency of the oscillator, the control voltage V_c should sink to zero. And the output frequency would be decreased that if the V_{DD} is charging the control line of the oscillator.

The simulated results of the charge pump combined with the phase and frequency detector is shown as follows. In fig 4.35 (a) and (b), the control line of the oscillator is charge toward V_{DD} in case of the divided signal leading to reference signal and the charging current is around 50 μA. On the other hand, the control voltage of the oscillator is sinking toward 0V in case of the divided signal lagging to reference signal which is shown in fig 4.36 (a) and (b), and the discharging current is also around 50 μA in the simulated waveforms. The average

current consumption of the charge pump is 0.72 mA, and the power consumption is 0.87 mW in the simulated results.

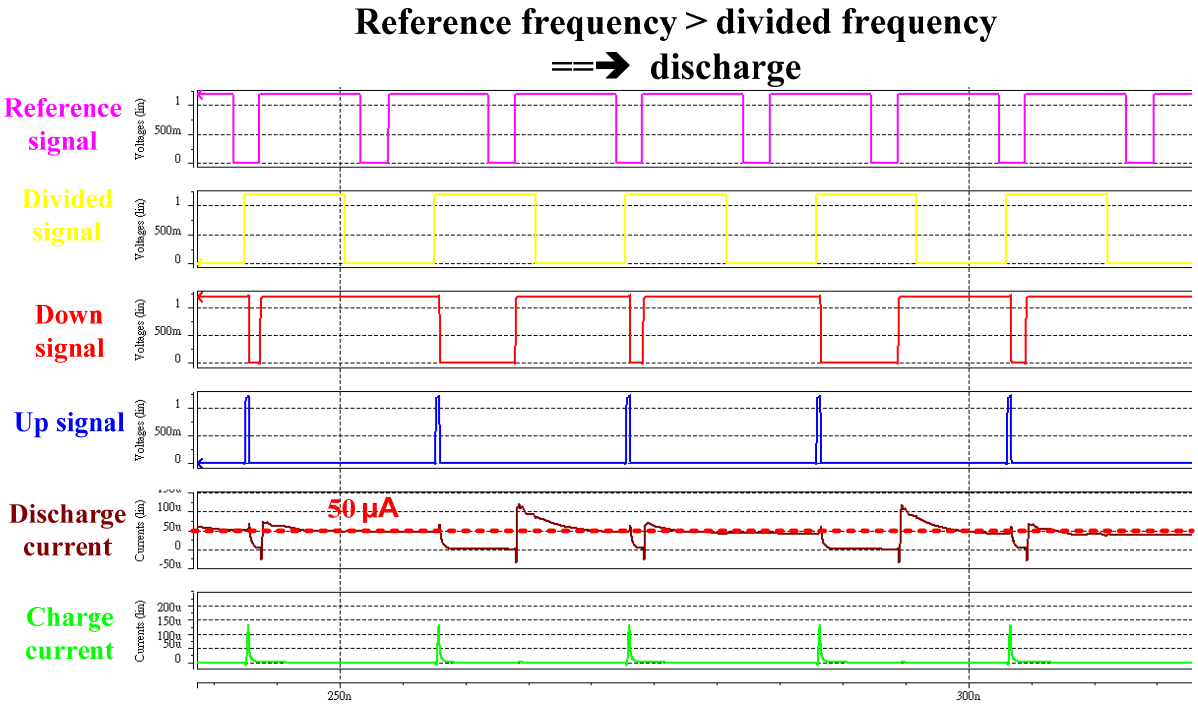


(a)

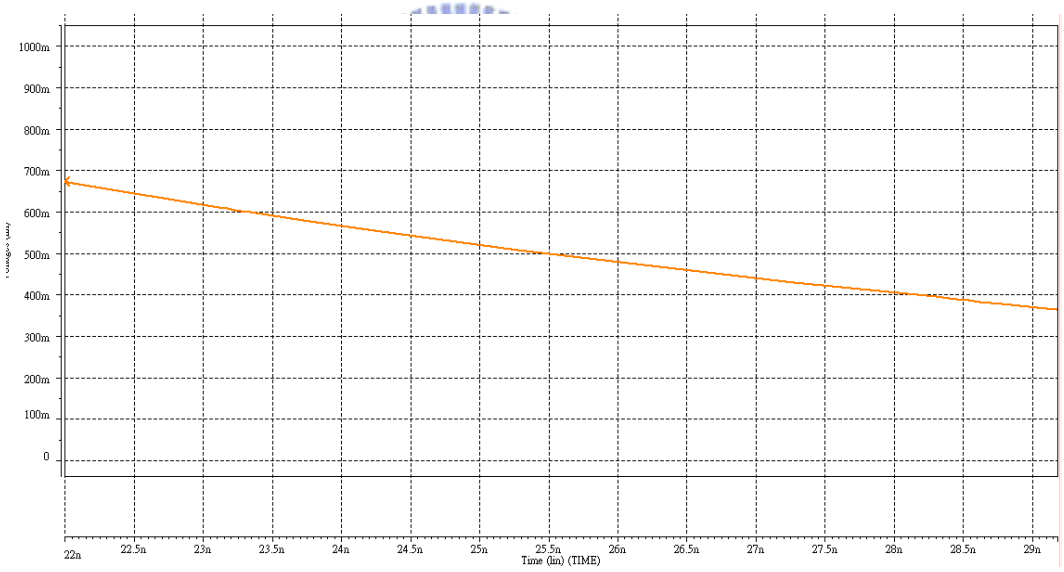


(b)

Figure 4.35 (a) The simulation results of the proposed PFD and charge pump, and (b) the control line of the oscillator in charging case



(a)



(b)

Figure 4.36 (a) The simulation results of the proposed PFD and charge pump, and (b) the control line of the oscillator in discharging case

The mismatching ratio of the charging and discharging current under the control voltage range is shown in fig 4.37. As the result, the mismatching of the charge pump would less than 4% under the oscillator control voltage 0.1~1.1V.

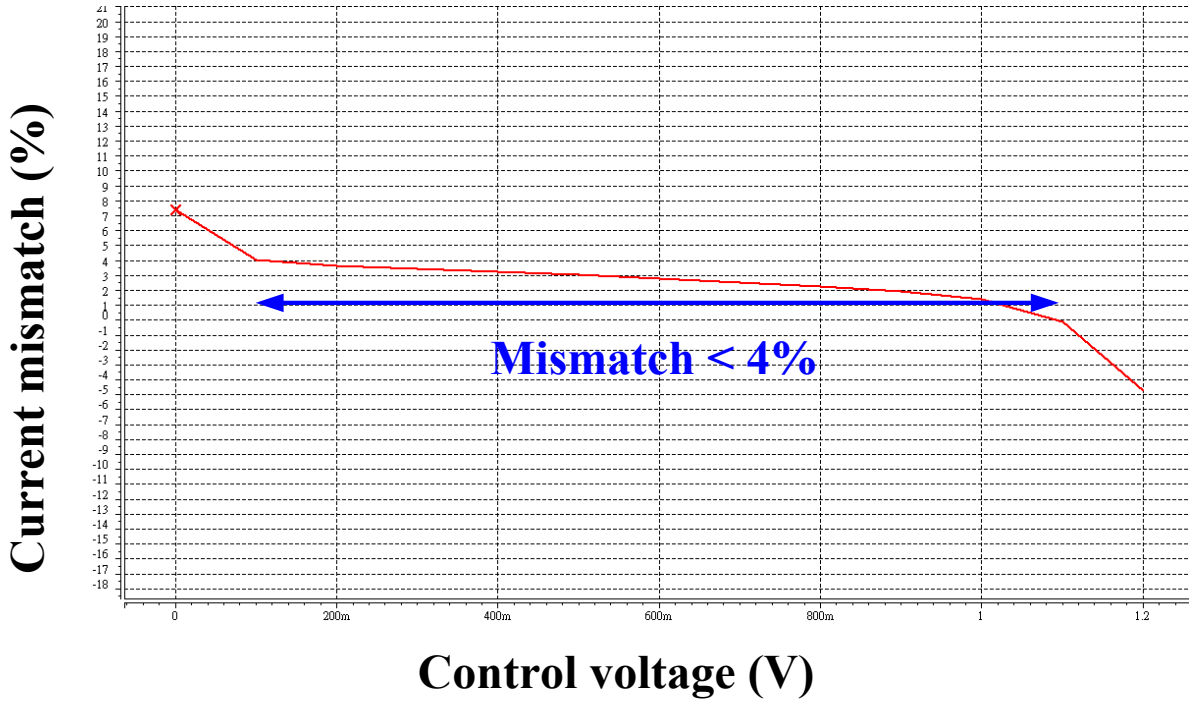


Figure 4.37 The mismatching ratio of the charge pump between charging and discharging currents

The summary and the comparison of the proposed charge pump is shown in the Table 4.3 below.

Table 4.3 The summary and comparison of the CP for the important characteristics

	This Work	[41]	[42]
Maximum frequency	Up to 1 GHz	Up to 0.5 GHz	Up to 1 GHz
Ref Current	50 uA	10 uA	10 uA
Power	0.87 mW	60 uW	~28 uW
Supply Voltage	1.2 V	1 V	1 V
Technology	CMOS 0.13µm	CMOS 0.18µm	CMOS 0.18µm

4.5 Loop Filter

The last part of the PLL component is the loop filter in this work. As we discussed in chapter 3, the specifications for loop filter design has changed, and the clearly design would be presented step by step in the followings. The structure of the loop filter is shown in fig 3.12 in chapter 3 above.

4.5.1 Design Consideration

The loop filter in this work is a second-order passive filter that consists of two capacitors and one resistor. The resulting PLL is then a type-II third-order loop. The capacitors and resistor of the loop filter should be properly chosen to perform the required filtering function and maintain the stability of the loop without introducing too much noise. The component values in the filter are calculated, which follows the design flow:

(1) The average VCO gain in this work is about -4.43 MHz/V.

K_{VCO} = -4.43 MHz/V.

(2) The input reference clock is 66 MHz.

f_{ref} = 66 MHz

(3) The loop bandwidth is chosen to be 3 MHz

K = 3 MHz

(4) A 60° phase margin is chosen. It corresponds to a coefficient γ of 4. In other words, the zero ω_Z is placed a factor 4 times below K, and the pole ω_P is placed a factor 4 times above K, to obtain a phase margin of approximately 60°.

(5) An equivalent charge pump current is 0.05 mA.

I_{CP} = 0.05 mA

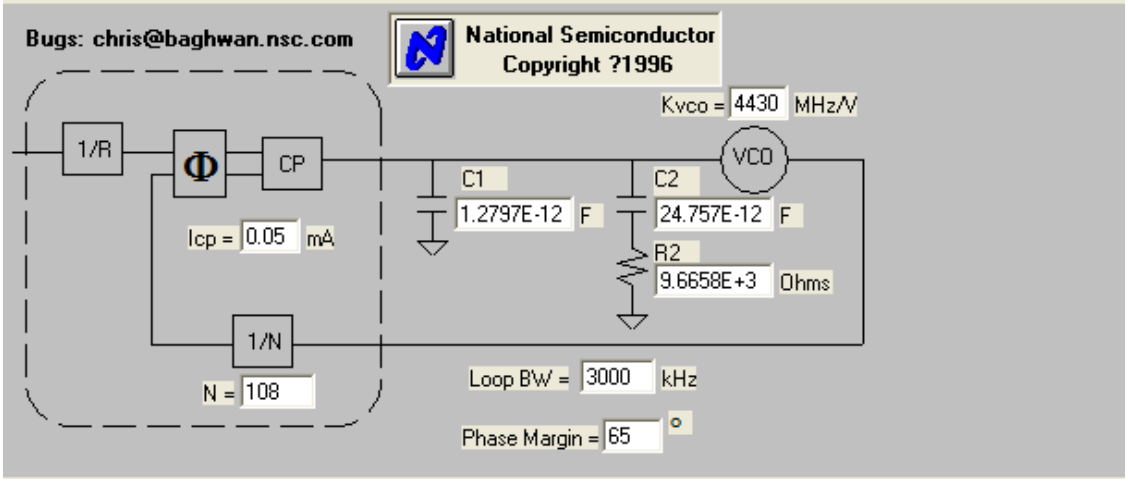
(6) In the design of the loop filter, the loop filter design software we mentioned in chapter 3 from National Semiconductor called “PLL Loop Filter Design “. As shown in fig 4.38 (a), the passive components of the loop filter are calculated as follows:

$$R_1 = 9.666k\Omega \qquad C_1 = 24.757\,pF \qquad C_2 = 1.280\,pF$$

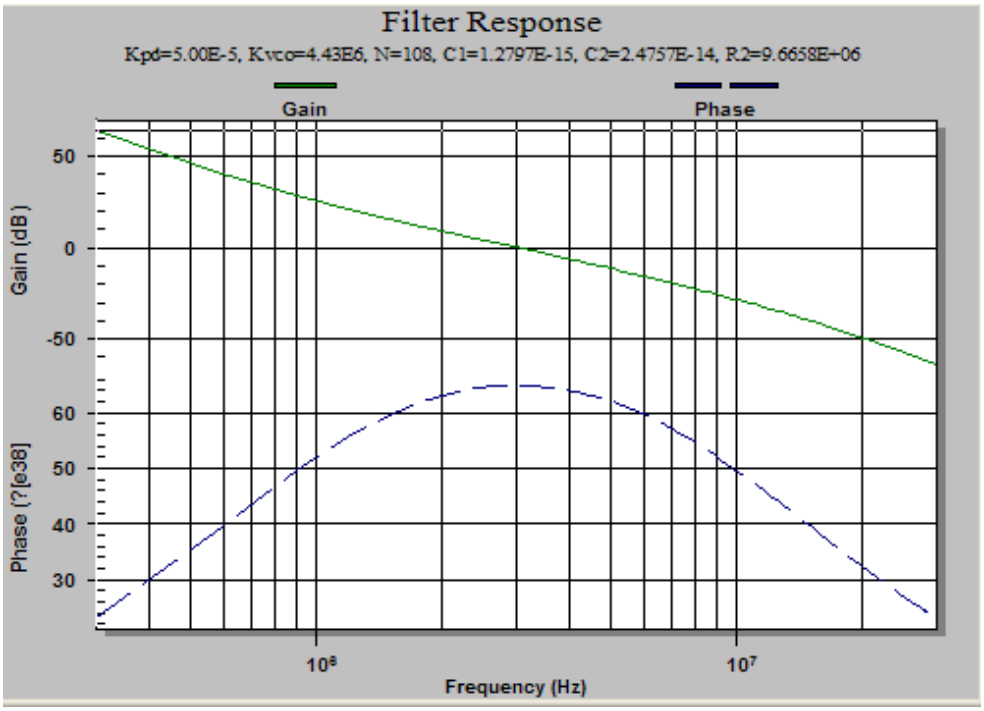
The summary of the loop filter parameters are listed in Table 4.4. And the stability of the PLL is shown in 4.38 (b) below.

Table 4.4 The parameters for the loop filter

parameter	value
Charge pump current I_P	**50 μA**
R_1	**9.666 kΩ**
C_1	**24.757 pF**
C_2	**1.280 pF**
VCO gain K_{VCO}	**-4.43 GHz/Volt**
Division number N	**108**
Loop bandwidth ω_c	**3 MHz**
Phase margin PM	**60°**
Zero frequency ω_Z	**0.75 MHz**
2nd pole frequency ω_P	**12 MHz**
Frequency coefficient b	**16**



(a)



(b)

Figure 4.38 The (a) loop filter design, and (b) Bode plot of the proposed PLL by the software

Then, it is the verification of the sensitivity of the PLL. Reliability would affect directly the stable state of the PLL transient behavior. We use Matlab to verify the reliability of the PLL whose passive component of filter is design by the National Semiconductor's software. As shown in fig 4.39 below, it could satisfy the specification of 60 degrees.

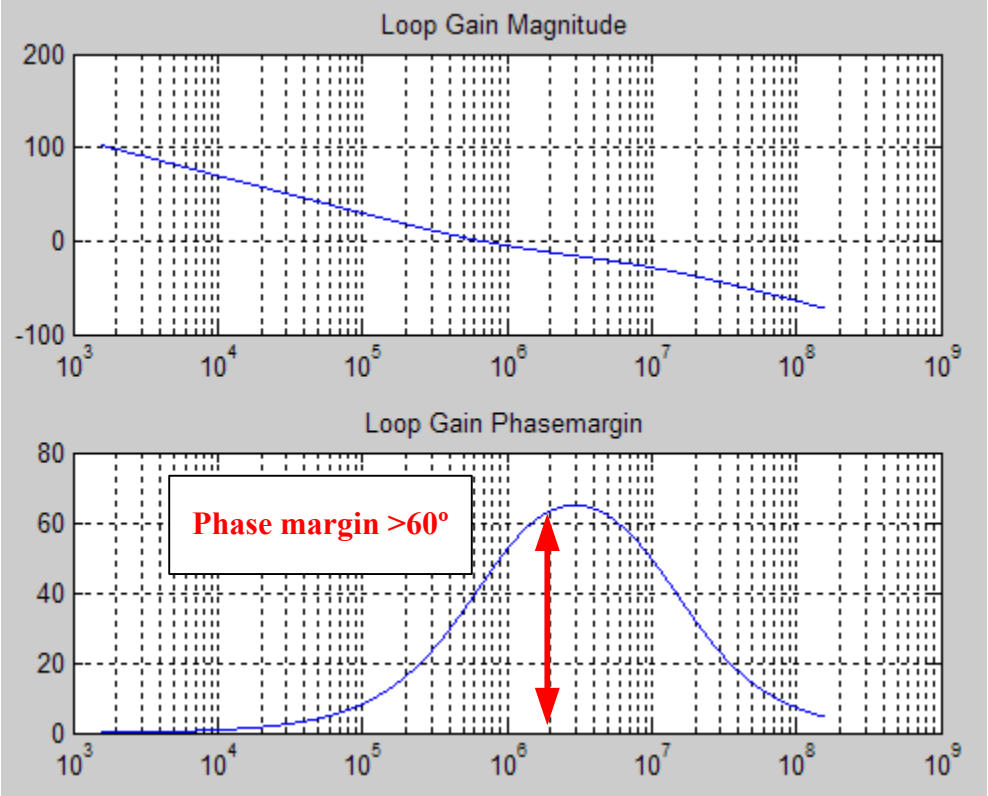
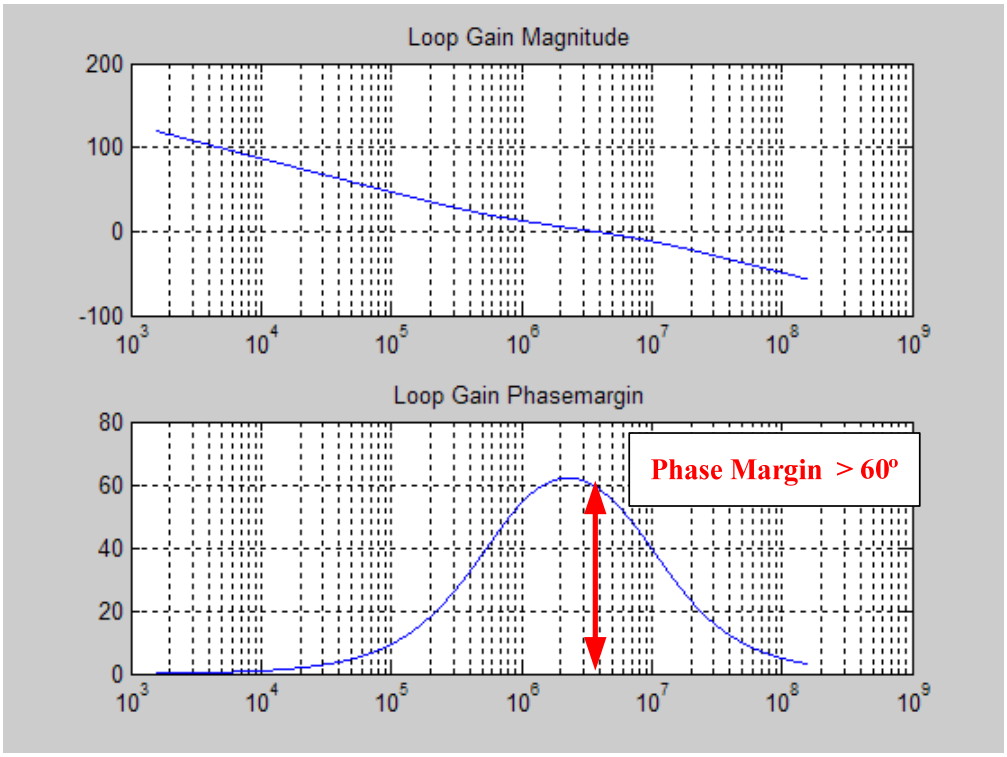
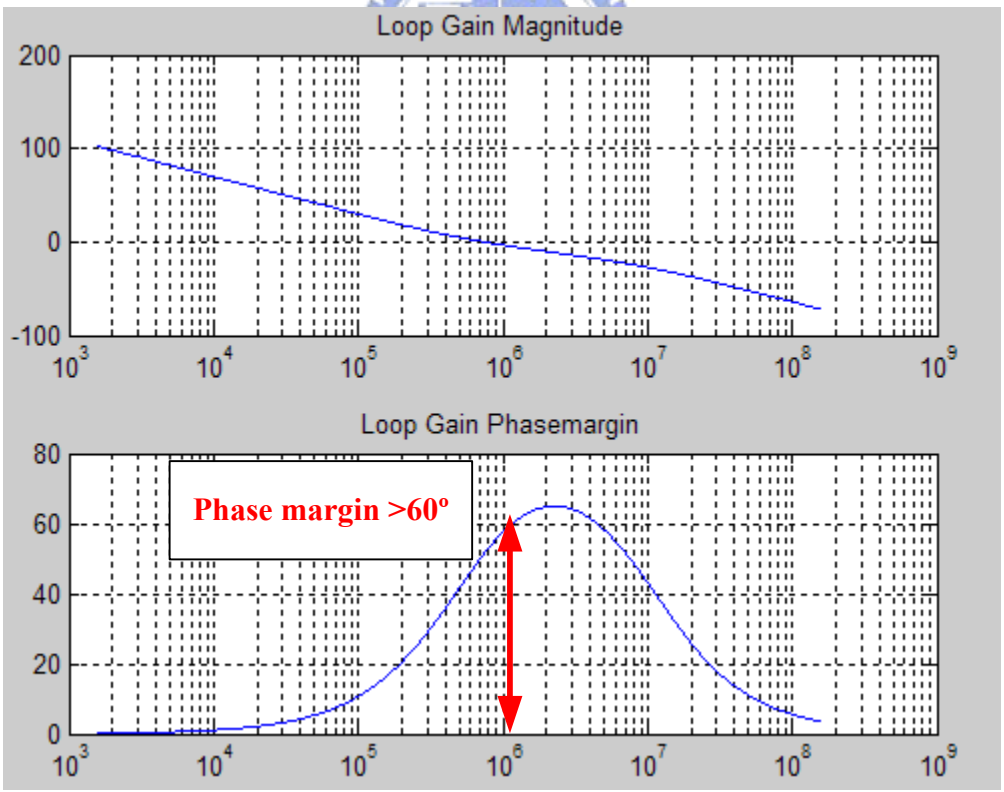


Figure 4.39 The Bode Plot of the open loop transfer function simulated by Matlab

The variation of the passive components of the resistor would also be considered. The worst case is the resistor varying ±30% value. We would use Matlab to model the phenomenon of that and verify them. As shown in fig 4.40 (a), (b), all the simulated results of the waveforms are correct and the phase margin is over the 60°.



(a)



(b)

Figure 4.40 The Bode Plot of the open loop transfer function with (a) +30% (b) -30% variations simulated by Matlab

4.6 Summary of the 7128-MHz PLL

With all discussion of the architecture and simulation of each block above, the complete frequency synthesizer can thus be implemented by combining all of them. In this work, a third-order PLL is achieved to provide a 7128 MHz frequency signal for the frequency synthesizer as the fundamental frequency spectrum. We complete the whole closed-loop simulation in TSMC 0.13-μm CMOS process model. The locking time (settling time) of the 7128-MHz phase lock loop is 25.4μs. Fig 4.41 below shows that the output phase error between quadrature phase. The worst phase error is around 0.3°. The in band spur of the PLL is less than -53dBc which is smaller than the required specification of -24dBc. The fft simulation of the proposed closed loop PLL is shown in fig 4.42.

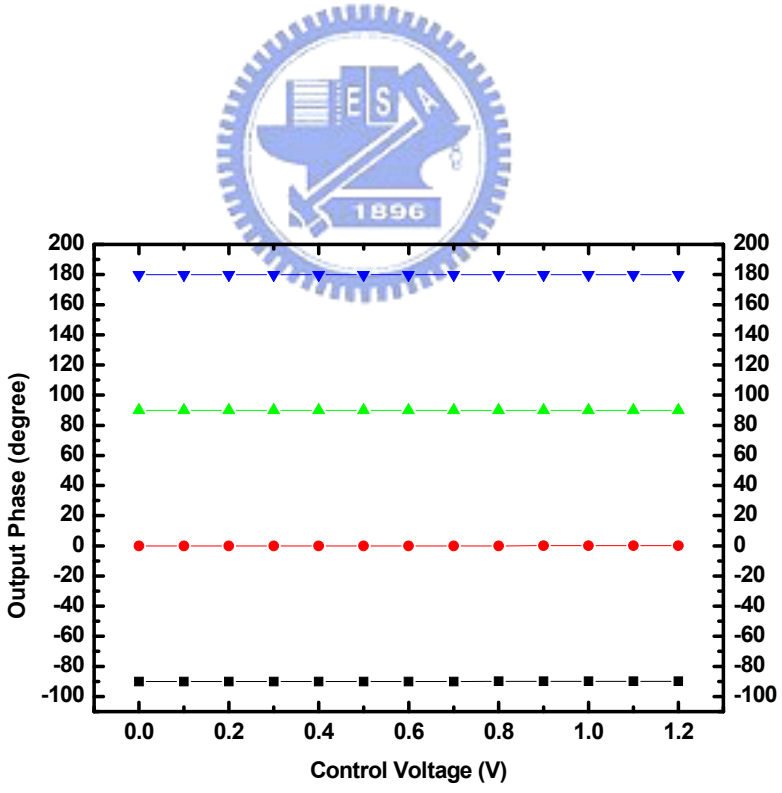


Figure 4.41 The phase relation between quadrature phase of oscillator

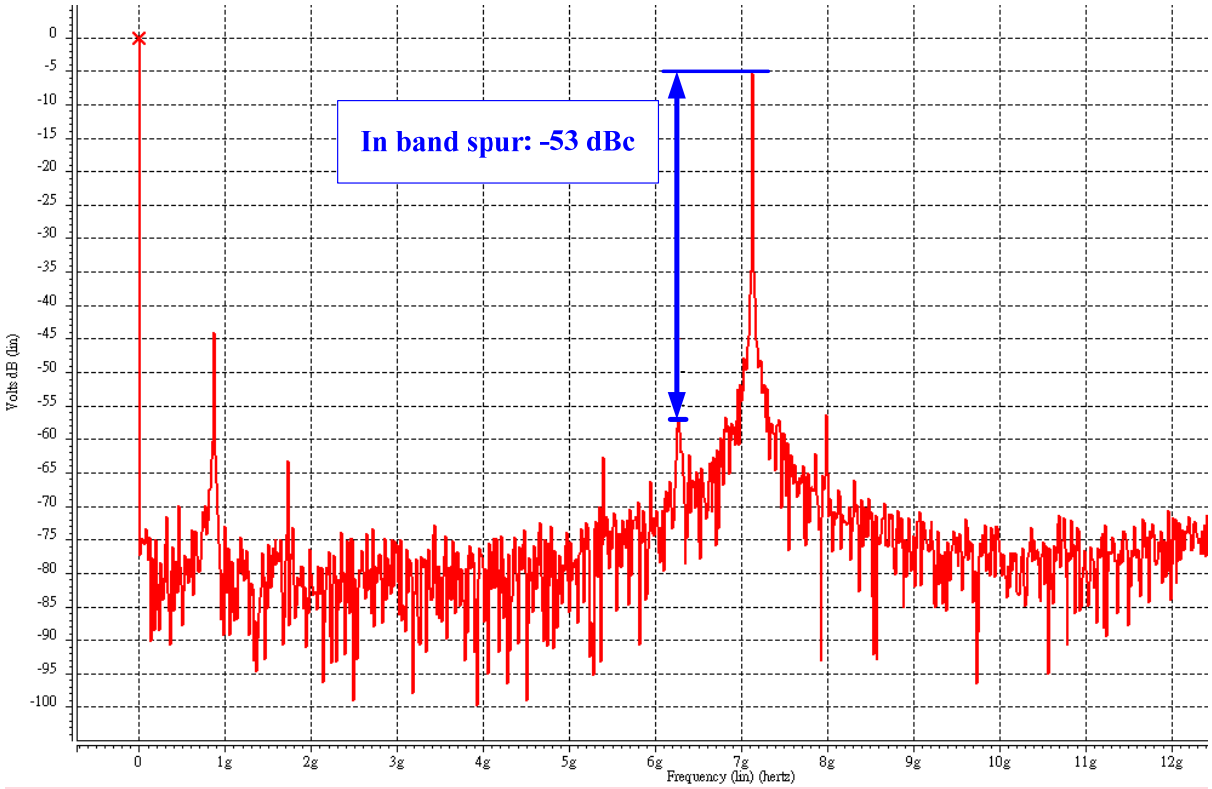


Figure 4.42 The fft simulation of the closed loop PLL

Table 4.5 below summaries the performance of the 7128-MHz phase lock loop.

Table 4.5 The summary of the 7128-MHz PLL

Parameter		Specification	Simulation result
Output frequency (MHz)		7128	7128
Reference frequency (MHz)		66	66
Spur rejection (dBc)		-24	-53
Division number		108	108
Settling time (μs)		none	25.4
Total dc power (mW)		none	~29
Process		TSMC 0.13 μm	TSMC 0.13 μm
Two-stage ring oscillator	Tuning range (GHz)	none	5.8~8.8
	Phase noise (dBc/Hz)	< - 96.5 @1MHz	< -117.6 @1MHz
	Phase error (°)	< 5	0.3
	DC power (mW)	none	12.42
VCO buffers	DC power (mW)	none	10.19
Dividers	DC power (mW)	none	4.65
Phase and frequency detector	Linear range @ 0.1GHz	none	± 1.8π
	DC power (mW)	none	0.2
Current-match charge pump	Mismatching ratio	none	< 4%
	Maximum frequency (GHz)	none	1
	DC power (mW)	none	0.87
Loop filter	order	2nd	2nd
	Phase margin (°)	> 60	> 60

4.7 Summary of the 3168-MHz PLL

As the system simulation and circuit design flow we set up in the previous chapter and section, the second PLL which outputs 3168-MHz in the proposed frequency generation scheme could be designed simply. Some of the dividers, the phase and frequency detector and charge pump use the same circuits as the 7128-MHz PLL. The summary of the proposed 3168-MHz PLL is listed in the Table 4.6 below. Table 4.7 is the summary and the comparisons of the proposed two PLLs.

Table 4.6 The summary of the 3168-MHz PLL

Parameter		Simulation result
Output frequency (MHz)		3168
Reference frequency (MHz)		66
Spur rejection (dBc)		-55
Division number		48
Settling time (μs)		32.2
Total dc power (mW)		~15.5
Process		TSMC 0.13 μm
Two-stage ring oscillator	Tuning range (GHz)	2.6~3.8
	Phase noise (dBc/Hz)	-105.2@1MHz
	Phase error (°)	0.25
	DC power (mW)	3.30
VCO buffers	DC power (mW)	8.49
Dividers	DC power (mW)	1.88
Phase and frequency detector	Linear range @ 0.1GHz	± 1.8π
	DC power (mW)	0.2
Current-match charge pump	Mismatching ratio	< 4%
	Maximum frequency (GHz)	1
	DC power (mW)	0.87
Loop filter	order	2nd
	Phase margin (°)	> 60

Table 4.7 The summary and comparisons of the proposed two PLLs

	This work		[43]	[44]	[45]	[46]	[47]
	7128-MHz	3168-MHz	*MTT2007*	*ICMMT2008*	*ISCAS2008*	*JSSC2004*	*CICC2008*
VCO architecture	Ring	Ring	LC tank	LC tank	LC tank	Ring	Ring
Output phase	quadrature	quadrature	quadrature	differential	differential	Three	quadrature
Central frequency	7.3GHz	3.2GHz	3.96GHz	5GHz	2.4GHz	2.4GHz	2.4GHz
Supply Voltage(V)	1.2	1.2	1.2	1.8	1.8	3.3	1.2
DC Power (mW)	29	15.5	39	83.3	22	49.5	65
Settling time (μ s)	25.4	32.2	none	0.6	none	none	none
Phase noise (-dBc/Hz)	117@1MHz	105@1MHz	115@1MHz	104@1MHz	81@0.1MHz	97@1MHz	100@1MHz
Technology	0.13 μ m CMOS	0.13 μ m CMOS	0.13 μ m CMOS	0.18 μ m CMOS	0.18 μ m CMOS	0.35 μ m CMOS	0.13 μ m CMOS

Chapter 5
Conclusion and Future Work

5.1 Conclusions

A 1.2-V phase lock loop with two-stage voltage control oscillator and current-match charge pump for full-band UWB frequency synthesizer has been designed in a TSMC 0.13-μm CMOS technology. The new frequency spectrum generation scheme is also proposed for the least usage of the SSB mixers to improve the performance of the spur level. In addition, a two-stage voltage control ring oscillator with quadrature phase output has been designed to implement a small chip area and high integration oscillator. The architecture of the proposed frequency synthesizer is the most directly perceived through the sense, and the system is the most uncomplicated to realized. There are not any inductors in our phase lock loop and it is the least number of the SSB mixers, so the chip area of the proposed frequency spectrum generation scheme would be reduced hugely.

The improved current-match charge pump is also proposed in this work. This new current-match charge pump solves the start-up problem, and it still has good performance in current matching.

Finally, a clear design flow of phase lock loop is presented in this work. By using the Matlab and Simulink, the simulation in system level could decrease the designing time of the whole phase lock loop circuits. The more accurate simulation in system level, the less modification takes in transistor level.

5.2 Future work

The proposed architecture for UWB frequency synthesizer has three blocks unfinished. And it could be fabricated with the simulated system and complete structures. It also could be integrated with the UWB receiver done by Yi-Kai Lo to verify the capability of the frequency synthesizer for UWB applications.

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