

國立交通大學

電子工程學系 電子研究所碩士班

碩士論文

銅製程中考量耦合電容與電鍍之無意義金屬擺放
用以改善平整度

Coupling Capacitance and ECP-Aware Dummy Metal Fill
for Layout Uniformity in Cu Process

研究生：柯宇倫

指導教授：陳宏明

中華民國九十六年十二月

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摘要

晶片在新一代製程中，隨著特徵尺寸的縮小，在製造困難度及可靠度上相對遇到的困難也越來越多。這種情況下，使得必須要有更良好的晶片表面平整度才能改善晶片的性能和參數良率。普遍用來降低晶片表面地形變化的方法是在佈局上較空曠的區域中填入一些無意義的金屬，然而，這些填入的金屬會增加導線之間的電容因而造成延遲和耦合/串擾等雜訊問題。

在這篇論文中，我們提出了一個演算法特別去考慮到一些佈局上會影響電鍍表面的參數來做無意義金屬的填入，同時我們使用一個貪婪演算法來放置這些金屬，使得額外增加的耦合電容能達到最小。在實驗結果方面，我們與傳統上以佈局密度為主的演算法做比較，我們的方法在電鍍後厚度差和等效密度差上都能有顯著的改善，這表示對晶片表面的地形平整度能有明顯的改善。而且，我們放置無意義金屬的方法也能有效降低額外增加的耦合電容。

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Abstract

With feature sizes on chips shrinking at new process node, the difficulty in manufacturability and reliability of chips is increasing. It has necessitated better planarization of chip surface topography to improve both functional and parametric yield. The common solution to minimize topography variation is to insert dummy metals in empty spaces in the layout. However, these dummy metals will increase the capacitances between wires and then invoke delay and coupling/crosstalk noise problems.

In this thesis, we propose an algorithm to consider especially the key layout parameters that affect the post-ECP (electroplating) topography and we use a greedy method to place the dummy metals with minimal additional coupling capacitances. Compared with a traditional density-based algorithm, the experimental result shows that our method has significant improvement on both post-ECP thickness variation and effective density variation which means the significant improvement in planarization of chip surface topography. Furthermore, our placing method of dummy metals can reduce the additional coupling capacitances efficiently.

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柯宇倫

民國九十六年十二月 於新竹

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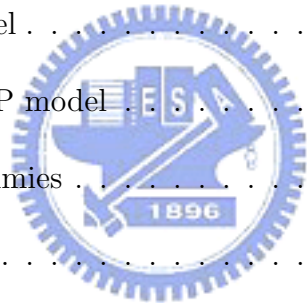
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Contents

1	Introduction	1
2	Preliminaries	3
2.1	ECP topography model	3
2.2	2D low-pass filter CMP model	7
2.3	Different types of dummies	8
2.4	Problem formulation	9
3	Proposed algorithm	12
3.1	Greedy heuristics for layout density and perimeter assignment	13
3.2	Dummy fill placement with minimal coupling capacitances	16
4	Experimental result	19
5	Conclusion	22
	Bibliography	22



List of Figures

2.1	A typical topography after ECP process [7]	4
2.2	An arbitrary layout in window with size $D \times D$	5
2.3	Three typical ECP topography cases [7]	5
2.4	Case selection of ECP topography	7
2.5	The weighting filter function used to transfer local pattern density to effective density.	8
2.6	Possible dummy shapes: (a) square, (b) rectangular, (c) parallel line, and (d) orthogonal dummy [4].	9
2.7	Total capacitance increments with different types of metal dummy [4].	9
2.8	Profile after ECP and CMP [10].	10
3.1	The flow chart of dummy fill insertion algorithm.	12
3.2	(a) empty rectangles within tile (b) fill-able regions	13
3.3	Capacitance increment : (a) dummy at track 0 (b) dummy at other track	17

List of Tables

4.1	The experimental results of proposed algorithm	19
4.2	The comparison of dummies placing methods	20



Chapter 1

Introduction

Continued aggressive scaling down of VLSI feature size has necessitated better planarization of chip surface topography to improve both functional and parametric yield. Non-planar chip surface can eat into the depth of focus (DOF) budget and also produce resistance and capacitance variations which can adversely impact chip timing. The commonly approach to improve the planarity of chip surface is to insert electrically inactive features (also known as metal fills or dummies) in the empty spaces in the layout to reduce the variations in key layout characteristics.

In the past, the primary objective of metal filling mostly focus on even layout density [2] [12]. This can be attributed to the fact that most metal filling solutions were originally developed to obtain better planarization after inter-layer dielectric (ILD) chemical mechanical polishing (CMP) in Al metallization process. Previous work by Ouma [8] shows that the ILD thickness is primarily a function of the underlying density. Hence, it sufficed to have a metal filling algorithm that sought to reduce the density differences between the different regions of the layout to attain smaller final thickness range. However, in Cu metallization process, there are various layout characteristics (besides density) which will affect planarity of chip surface and should be considered in metal fill algorithm.

Electroplating (ECP) and CMP are two key steps in the Cu fabrication process. The variations in the post-ECP topography are propagated through the CMP steps, thereby affecting the final surface topography. In our approach, we apply the ECP model of [7] to get the post-ECP thickness from layout characteristics and evaluate the effective density to indicate the final planarity of chip surface after CMP process.

As we insert dummies to improve the chip planarity, the interconnection capacitances will increase and then invoke delay and coupling/crosstalk noise problems. Therefore, another objective is to decide the positions of dummies in the empty spaces with minimal coupling capacitances. The computation of coupling capacitance increment refers to the capacitance model for intra-layer dummies in [4] [1] [3].

In this thesis, we begin with the descriptions of ECP and CMP models and briefly explain how the two processes affect the chip surface in Chapter 2. In Chapter 3, we proposed an algorithm to improve the planarity and reduce the capacitive increment due to dummy insertion. We show the experimental results of the algorithm in Chapter 4, and conclude in Chapter 5.

Chapter 2

Preliminaries

In this chapter, we introduce two important models that are applied in our algorithm. The first one is the electroplating (ECP) topography model, which is developed based on the additive nature of the physics of the ECP process [7], and it can predict the post-ECP topography by the strong dependency of post-ECP thickness and layout characteristic. The second one is the 2D low-pass filter CMP model, which is used to determine the effective density of each panel by weighting the influence of nearby panel density.

2.1 ECP topography model

During the copper(Cu) Damascene process, trenches and holes are first etched in the oxide material. An ECP process is applied to deposit the copper onto the whole wafer filling up the trenches. It is followed by a CMP process in which excess overflowing copper is removed from the oxide surface leaving copper in the intended trenches and holes. And the interconnect wires and vias are formed.

Figure 2.1 shows an example of a typical topography after ECP. Post-ECP topography can be described by two parameters: step-height and array-height. The

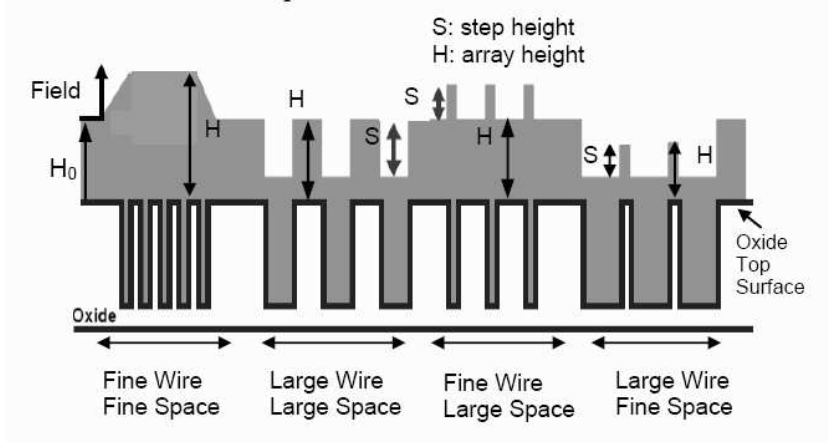


Figure 2.1: A typical topography after ECP process [7]

array height H is defined as the thickness of Cu above the oxide after deposition; the step height S is defined as the difference of Cu height between the Cu above the oxide and the Cu above the trench in the oxide. We can observe that the Cu thickness after ECP process strongly depends on wires attributes of the region.

Before we further discuss the ECP topography model, we should give the definitions of several layout parameters first. They are the perimeter sum L , the feature density ρ , shrunk density ρ_s , expanded density ρ_e . For an arbitrary layout in window with size $D \times D$ shown in Figure 2.2,

$$L = 2(L1 + L2 + L3 + L4 + L5 + L6 + L7 + L8) + L9 + L10 + 2L11 + L12$$

ρ = the area of all the layout objects (or feature trenches)

divided by the total area of the design

ρ_s = the feature density after shrinking all the

layout features by an amount of δ_s

ρ_e = the feature density after expanding all the

layout features by an amount of δ_e

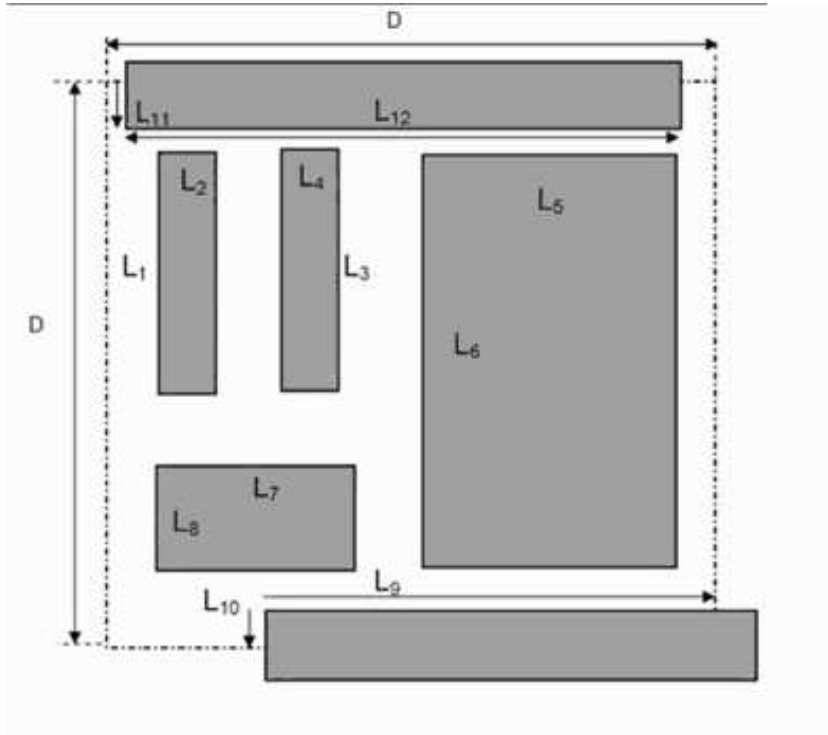


Figure 2.2: An arbitrary layout in window with size $D \times D$

There are primarily three different topographies that result after an ECP process. For simplicity of the presentation, Figure 2.3 shows these three topographies for a single wire only. However, the following discussions are applicable to multi-wires as well.

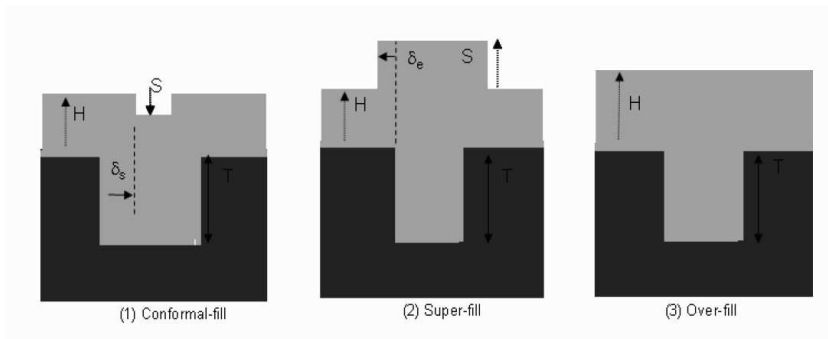


Figure 2.3: Three typical ECP topography cases [7]

In this model, the topography is formulated as the functions of layout variables

for each case:

Case 1 (conformal-fill):

$$H = H_0 \frac{1 - \rho}{1 - \rho_s} \quad (2.1)$$

$$S = H_0 \frac{1 - \rho}{(1 - \rho_s)\rho_s} + T \frac{\rho}{\rho_s} - H_0 \frac{T_e L}{D^2 \rho_s} - \frac{H_0}{\rho_s} \quad (2.2)$$

Case 2 (super-fill):

$$H = H_0 \quad (2.3)$$

$$S = T \frac{\rho}{\rho_e} - H_0 \frac{T_e L}{D^2 \rho_e} \quad (2.4)$$

Case 3 (over-fill):

$$H = H_0 + H_0 \frac{T_e L}{D^2} - T \rho \quad (2.5)$$

$$S = 0 \quad (2.6)$$

where H_0 is the field copper thickness, T is the feature trench depth.

Because of the evolution process of topography described in [2], the case selection must follow the flow chart shown in Figure 2.4.

As this model is developed, we can get post-ECP topography by evaluating the step height and array height. We can reduce post-ECP height difference in dummy insertion algorithm to lower the influence on sequential CMP process, which will be discussed in Chapter 3.

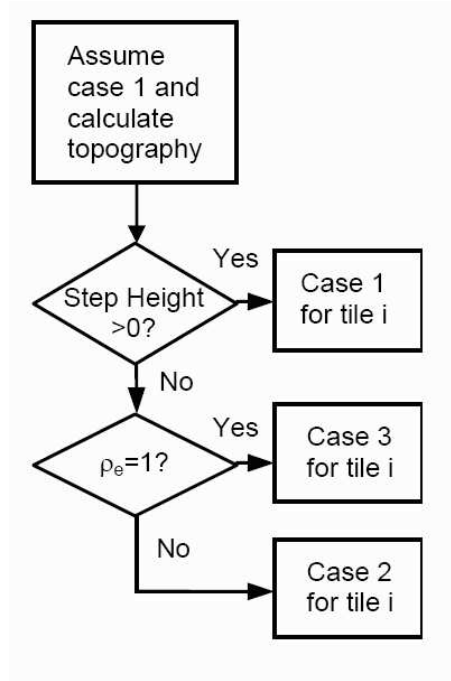


Figure 2.4: Case selection of ECP topography

2.2 2D low-pass filter CMP model

After Cu deposited onto the wafer, excess overflowing Cu is removed from the oxide surface in CMP process. A detailed CMP process models, which take process parameters such as slurry contents, down pressure, pad material and pad speed into consideration, are usually complicated. However, an abstract-level model may be simple since the CMP process that is designed to polish uneven surfaces is analogous to a low-pass "filter". A 2-D low-pass-filter CMP model is found to be both efficient and easy to calibrate [9][13].

As we know, for more uniform ECP profiles, there is a dependence between the final thickness and the density [6]. The thickness in such cases is inversely proportional to the effective density, which is a function of the local density. After the layout is discretized to rectangle panels, the effective density at the center of

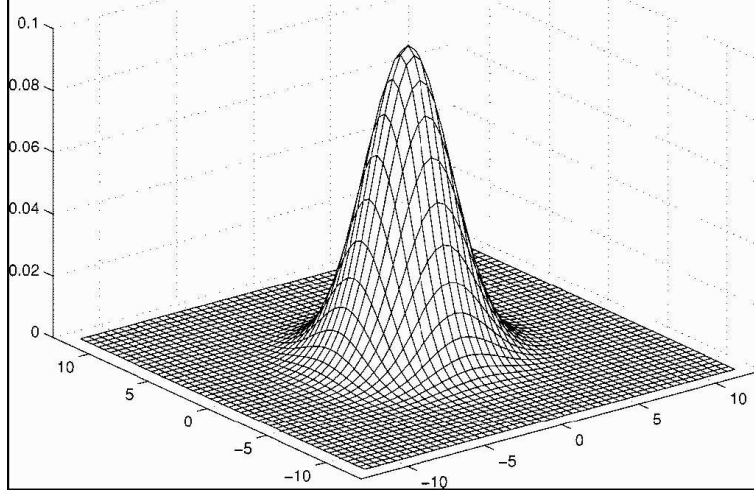


Figure 2.5: The weighting filter function used to transfer local pattern density to effective density.

panel (i,j) is a 2-D convolution of the local pattern density with the filter function.

The effective density $\rho_{eff(i,j)}$ can be calculated using [11]:

$$\rho_{eff(i,j)} = \text{IFFT}[\text{FFT}[\rho(i,j)] * \text{FFT}[f(i,j)]] \quad (2.7)$$

where $\rho(i,j)$ is local pattern density, and $f(i,j)$ is the weighting filter function shown in Figure 2.5.

2.3 Different types of dummies

For the dummy metal fill problem, there are floating dummies and grounded dummies. Before we talk about our algorithm, we have to mention that the type we use is floating dummies while some of prior works choose grounded stripe metals as their dummies. Grounded dummies are not desirable due to both their higher impact on capacitance and also routing difficulties in current technology nodes, although they are more stable and easy to extract.

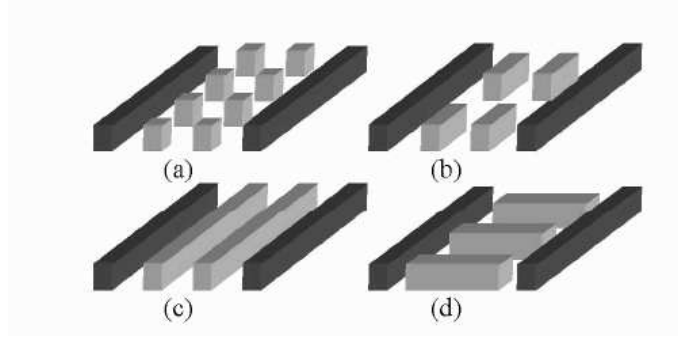


Figure 2.6: Possible dummy shapes: (a) square, (b) rectangular, (c) parallel line, and (d) orthogonal dummy [4].

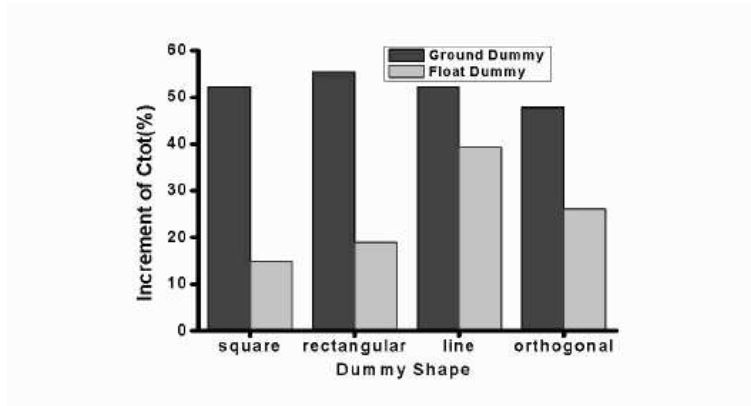


Figure 2.7: Total capacitance increments with different types of metal dummy [4].

In addition, different shapes of dummies will cause different capacitance increment. Figure 2.6 present the four possible types of dummy shapes. Figure 2.7 shows the square, floating dummy has least capacitance increment and consequently was used for insertion in our approach [5][4].

2.4 Problem formulation

Most prior model-based solutions use an ILD thickness model to guide the metal filling process. The ILD thickness model states the dielectric thickness at a location

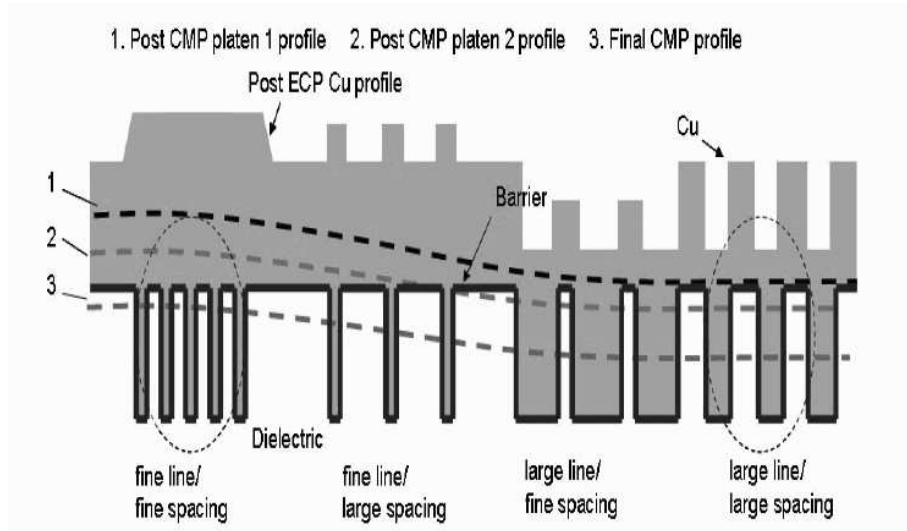


Figure 2.8: Profile after ECP and CMP [10].

is proportional to the convolution of the metal density and a suitable weighting function which considers the deformation of the polishing pad during CMP. All of these model-based solutions focus primarily on metal density and does not consider the impact of ECP. However, there are experiments show that different regions with the same density have different final thickness values after Cu ECP and CMP [10]. Therefore, it can be concluded that it is not sufficient to consider only density during metal filling for copper processes.

Figure 2.8 shows that the variations in the ECP topography are propagated through the CMP steps, thereby affecting the final surface topography. For this reason, one of our objectives is to reduce the post-ECP thickness range (i.e. height difference between highest and lowest point) by changing layout characteristics with dummies.

As long as the post-ECP topography is smooth, there is dependence between the final thickness and the effective density. Our another objective is inserting dummies

to reduce effective density range, at the same time, without increasing post-ECP thickness range.

Although metal filling is an effective method to improve chip planarity, it draws some drawbacks. The more dummies we inserted, the more capacitances would be induced. These additional capacitances will result delay or crosstalk problems. Accordingly, another consideration is to reduce the additional capacitances by put the dummies we inserted into suitable place between empty spaces of layout.



Chapter 3

Proposed algorithm

In this chapter, we present an algorithm to solve the dummy filling problem. The algorithm is performed with the procedures shown in Figure 3.1. We will show the details in how to reduce variations of chip surface and, meanwhile, minimize the dummy-induced coupling capacitance in the following subsections.

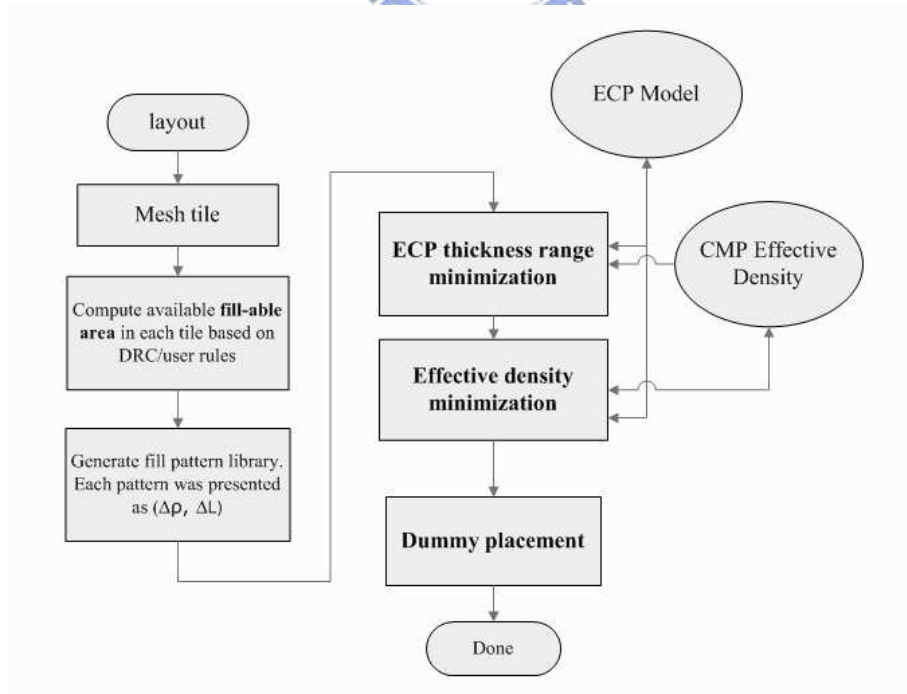


Figure 3.1: The flow chart of dummy fill insertion algorithm.

3.1 Greedy heuristics for layout density and perimeter assignment

The key layout parameters that are considered in this step are density and perimeter since ECP thickness profile primarily depends on both parameters and the effective density depends only on density. The manipulation of adjusting these parameters between tiles can improve chip surface planarity.

We start with meshing the layout of design into non-overlapping tiles, and then slicing the layout to get empty spaces for dummy insertion. Figure 3.2(a) shows the rectangular empty spaces and Figure 3.2(b) shows the fill-able region that is safe for dummy filling.

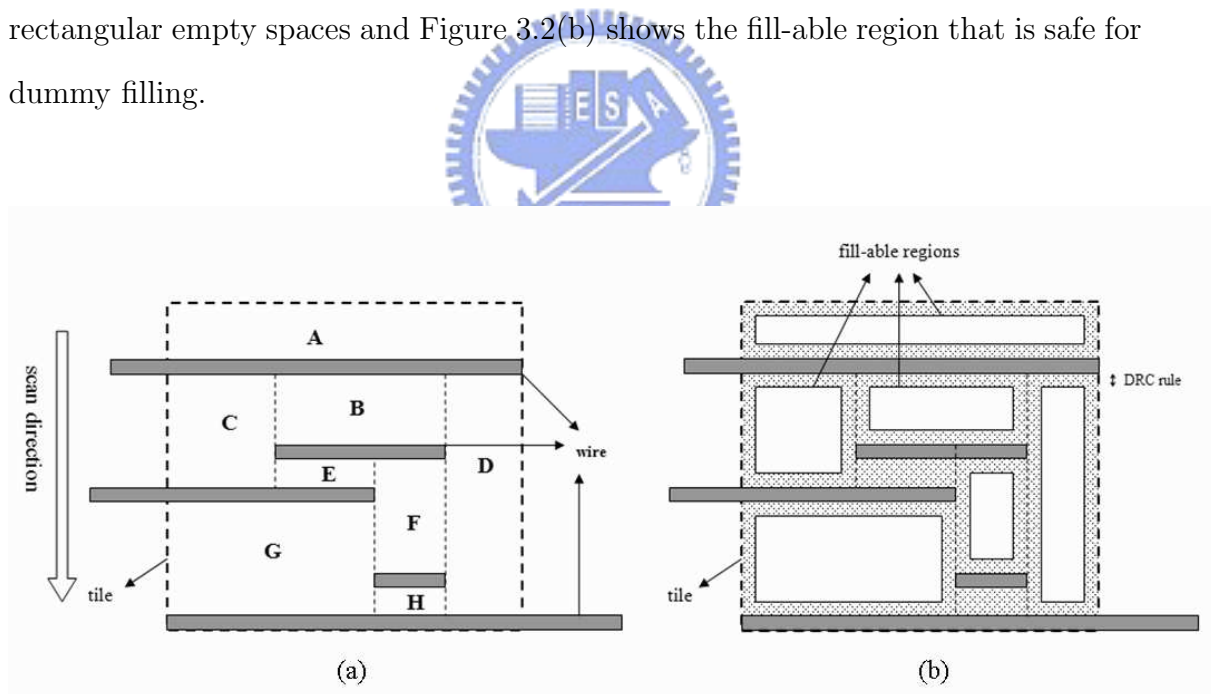


Figure 3.2: (a) empty rectangles within tile (b) fill-able regions

Parameter assignment has two main steps. In the first step, our objective is to reduce the post-ECP height difference. And we minimize the effective density range without increasing post-ECP height difference in the second step. Throughout both steps, we change layout parameters of each tile by appending a combination of den-

sity and perimeter, which is chosen from the established fill pattern library. As long as the parameters are assigned, we apply the ECP and CMP model to check that the topography is convergent or not. Following processes are the greedy heuristics for parameters assignment:

Greedy Heuristics for Density and Perimeter Assignment :

1. Layout Preparation :
 - (a) Mesh the layout into non-overlapping tiles. Denote the i th tile as T_i .
 - (b) Determine the fill-able areas in each tile based on DRC rules. The fill-able density of the tile T_i is denoted as d_i^F .
 - (c) Generate a fill pattern library which includes many (density, perimeter) combinations that can be assigned to tiles. The set of combinations is denoted as CS .
2. Reduce ECP Thickness Range :
 - (a) **Intra-tiles ECP thickness range minimization**
 - (b) **Inter-tiles ECP thickness range minimization**
3. Minimize Effective Density Range :
 - (a) **Restricted effective density range minimization**

The detail of the minimization algorithms will be provided below. After the heuristics are performed, we get the target density and perimeter of each tile that can make the chip more smooth. With these parameters, we know how many and how large dummies should be inserted in each tile. However, the positions of the dummies are not really decided. Following section we will have the discussions about this part.

Intra-tiles ECP thickness range minimization algorithm

For each tile T_i

Determine ECP case by ECP model.

If T_i is not over-fill case

For each $c = (d_k^c, L_k^c) \in CS$ and $d_k^c < d_i^F$.

Let d_k^c and L_k^c add to the tile's parameters temporarily.

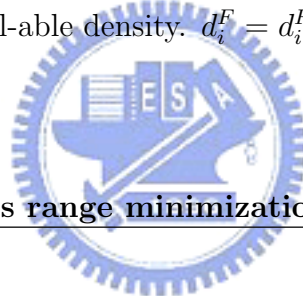
If the tile is over-fill case.

Break

Else

Restore the tile's parameter .

Update the fill-able density. $d_i^F = d_i^F - d_k^c$.



Inter-tiles ECP thickness range minimization algorithm

1. Determine the ECP thickness H_i of all tiles and denote maximum as H_{max} .
2. Compute priority of each tile as a function of $H_{max} - H_i$. And sort the tiles according to the priority function.
3. **For** all tiles in sequence

$$H_{diff} = \infty$$

For each $c = (d_k^c, L_k^c) \in CS$ and $d_k^c < d_i^F$.

Let d_k^c and L_k^c add to the tile's parameters temporarily.

Compute H_i by ECP model.

If $H_{max} - H_i < H_{diff}$

$$c_{opt} = c$$

$$H_{diff} = H_{max} - H_i$$

Break

Else

Restore the tile's original parameters.

Assign c_{opt} to the tile and update the fill-able density. $d_i^F = d_i^F - d_k^{c_{opt}}$.

Restricted effective density range minimization algorithm

1. Determine the effective density ρ_i of all tiles and denote maximum as ρ_{max} .
2. Unlocked each tile T_i and compute its priority as a function of $\rho_{max} - \rho_i$. And sort the tiles according to the priority function.
3. **For** all tiles in sequence

$$\rho_{diff} = \rho_{max} - \rho_{min}$$

For each $c = (d_k^c, L_k^c) \in CS$ and $d_k^c < d_i^F$.

Let d_k^c and L_k^c add to the tile's parameters temporarily.

Compute H_i and ρ_i of each tile by ECP and CMP model.

If $\rho_{max} - \rho_{min} < \rho_{diff}$, and ECP thickness range does not increase

If for each neighbor tile in CMP radius, its $\rho \leq \rho_{max}$

$$c_{opt} = c$$

$$\rho_{diff} = \rho_{max} - \rho_i$$

Break

Else

Restore the tile's original parameters.

Assign c_{opt} to the tile and update the fill-able density. $d_i^F = d_i^F - d_k^{c_{opt}}$.

3.2 Dummy fill placement with minimal coupling capacitances

Dummy fill insertion is an effective and widely-used method to improve chip planarity. However, these dummy metals will increase coupling capacitances and bring some problems. Placing the dummies to suitable positions in the empty spaces may reduce the capacitive increments. The coupling capacitance introduced by dummies can be evaluated by the closed-form equation [3] as shown below:

$$C = C_0 \frac{l}{d^\alpha}$$

where C_0 is the coupling parameter, α is an experimentally estimated constant, l is the coupling length, and d is the distance between two segments. C_0 and α are technology related constants, $\alpha \in (1, 2)$ for the current technology.

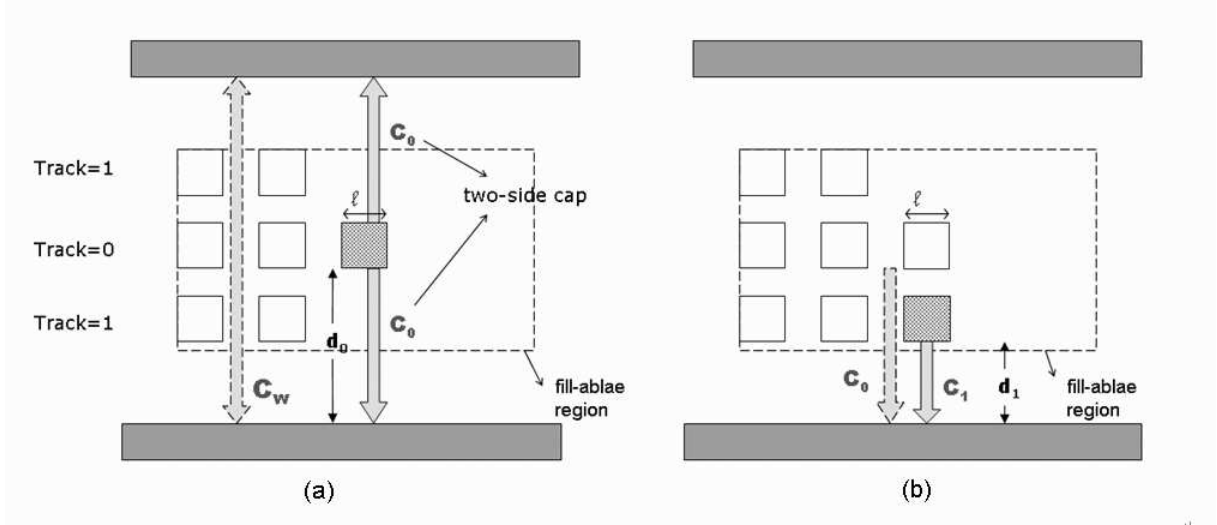


Figure 3.3: Capacitance increment : (a) dummy at track 0 (b) dummy at other track

As shown in Figure 3.3, when we select a dummy at track 0, the dummy will introduce new coupling capacitances for both side. When we select a dummy at other tracks, it will introduce new coupling capacitances on one side and block some old coupling capacitance. Assume the dummies at higher tracks can be inserted only if dummies at lower track are inserted, then, the increase of the coupling capacitance for the dummy at track i can be formulated as following:

$$\text{Additional cap cost} = \begin{cases} (\frac{1}{C_i} + \frac{1}{C_i})^{-1} - C_w \cdot l & \text{if } i=0, \\ \frac{1}{2}[(\frac{1}{C_i} + \frac{1}{C_i})^{-1} - (\frac{1}{C_{i-1}} + \frac{1}{C_{i-1}})^{-1}] & \text{otherwise.} \end{cases} \quad (3.1)$$

where l is dummy width, C_w is cap per unit before inserting any dummies, and C_i is the cap between the dummy at track i and its neighbored wire.

In the previous parameter assignment step, we get target density ρ and perimeter L of each tile. Since we choose square dummies to be inserted, we can easily compute the dummies numbers N and their width w of each tile from its target density and target perimeter. Following equations are the relations of these parameters:

$$L_{fill} = N \cdot 4w \quad (3.2)$$

$$\rho_{fill} = N \cdot \frac{w^2}{TileWidth^2} \quad (3.3)$$

After we get dummies amount N , dummy width w , and the cap cost of each possible position, the minimization of capacitances within a tile is just choosing lowest-cost positions until N dummies are inserted. Notice that the selection of possible dummy position should keep the order from lower tracks to higher tracks.



Chapter 4

Experimental result

Here, we present the experimental result for two chips to validate the proposed algorithm. The first one (D1) is $3.4 \times 3.4 \text{mm}^2$ for $0.13 \mu\text{m}$ 1P8M process and the second one (D2) is $3.9 \times 3.9 \text{mm}^2$ for 90nm 1P9M process. For both designs, we choose an $1 \times 1 \text{mm}^2$ dissection and mesh it into 20×20 tiles to perform the algorithm.

In Table 4.1, the ρ_{eff} range of original chip means the peak-to-peak value of effective density between tiles. We first compute local density from layout patterns, and then get the effective density by the low-pass filter CMP model. The layout patterns before dummy filling are only composed of routing wires. When the dummies are inserted, the density of dummies will be counted in.

Table 4.1: The experimental results of proposed algorithm

Original chip				After our approach		
Test case	Avg. ρ_{eff}	ρ_{eff} range	Post-ECP thickness range	Avg. ρ_{eff}	ρ_{eff} range	Post-ECP thickness range
D1	0.156	0.2368	454.085	0.259	0.1177	34.99
D2	0.174	0.2901	398.882	0.265	0.1222	34.88
					45.9%	8.2%

As we mentioned before, The effective density is the key indicator of final thickness only if the ECP topography is more smooth. Therefore, the changes of post-ECP thickness range is important and is also shown in the table. We can observe that the post-ECP thickness range becomes 8.2% of original chip and effective density range becomes 45.9% after the proposed algorithm. It means that the ECP topography is really smooth, and therefore we can say the final thickness range is reduced to about 45.9% of original thickness range after our algorithm.

After the numbers of fills are assigned to tiles, the methods of placing fills will affect coupling capacitances. Traditional dummy fill insertion are based on even effective density. Thus, for each tile, the fills are distributed to fill-able regions by their area to get even density on tile scale. We compare our method with density driven method in Table 4.2. The additional capacitance is the increment of the capacitances from the same layer after the dummy fills insertion is applied.

Table 4.2: The comparison of dummies placing methods

	Additional capacitance		
Test case	density driven method	our method	improvement
D1	4528	1804	60.2%
D2	3877	1299	66.5%

In the density driven method, each tile T_i has many non-overlapping fill-able regions R_{ij} , where $\sum R_{ij} = F_i$ (total fill-able area). For each R_{ij} , the dummies number is equal to $\{\text{target dummies numbers} \times R_{ij}/F_i\}$ [10]. Therefore, the dummies are evenly distributed in a tile. And then dummies are put into R_{ij} from center track to edge track to reduce additional capacitance. As Table 4.2 shown, our approach

has less additional capacitances than the density-driven method, thereby having less coupling/crosstalk noise problems.



Chapter 5

Conclusion

In this thesis, a metal filling algorithm that is based on the physical models of the copper damascene process was presented. Key predictors of final thickness range that can be efficiently computed were identified and used to drive metal filling. Experimental results indicate that the proposed method can significantly reduce the post-ECP thickness range and effective density range after metal filling. Also, we take the capacitances into consideration, for which will definitely increase after metal filling and cause unwanted effect. The proposed method can significantly reduce the additional coupling capacitances when compared to the density-driven approach.

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