國立交通大學

電子工程學系 電子研究所碩士班

碩 士 論 文

應用於 WiMAX 與 WiFi 傳送端並具備補償 I/Q 未匹配與 LO 饋出之直接升頻混波器

Direct Up-Conversion Mixer with Matching Compensation Eliminating I/Q Imbalance and LO Feedthrough in WiMAX and WiFi Transmitter

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碩 士 論 文

A Thesis

Submitted to Department of Electronics Engineering & Institute of Electronics

College of Electrical Engineering and Computer Science

National Chiao Tung University

In Partial Fulfillment of the Requirements

For the Degree of

Master

In

Electronic Engineering

May 2008

Hsinchu, Taiwan, Republic of China

中 華 民 國 九十七 年 五 月

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摘要

本篇論文提出具備匹配補償之升頻混波器電路，可搭配回授電路與演算法可達到自動校正。利用向量的補償方法來使 I/Q 訊號達到正交，且找出引發混波器輸出端的本地振盪器訊號的主要原因，利用小電流源補償，使本地震盪器在輸出端的訊號大小達到一個最小值。所有用來匹配補償的小電流源需要三十組的控制訊號，因此我們使用序列訊號轉平行訊號的轉換器來輸入我們的控制訊號。經由模擬驗證後可達到 0.67%的 EVM。

此混波器電路利用台灣積體電路(TSMC)製程下線，整個架構包含 I/Q 混波器、本地振盪器的四相位產生器、本地震盪器的 I/Q 緩衝器、I/Q 混波器和序列訊號轉平行訊號的轉換器。電路的下線面積為 1.65X1.25 mm^2，功率消耗為 50.4mW。

由於序列訊號轉平行訊號的轉換器電路部分發生了箝制效應，致使控制訊號無法正確輸入且匹配補償電路無法正確工作，因此我們最後只能量測 I/Q 混波器未匹配補償的特性。量測結果顯示在 2.4GHz~2.7GHz，I/Q 混波器具有大於

-11.15dB 的增益、5dBm 的 1-dB 功率增益壓縮點、大於 15dB 的無用邊帶抑制與最大 15dB 的 LO 饋出抑制。由於無法經由電路本身最匹配補償，經由人為手動補償後，可達到 38.5dB 的無用邊帶抑制。

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ABSTRACT

This thesis proposes an up-conversion I/Q mixer with matching compensation eliminating I/Q imbalance and LO feedthrough. By additional power detection feedback loop and compensation algorithm, auto-compensation can be achieved. The compensation for I/Q balance is achieved by using vectors compensation. The main factor resulting in LO feedthrough is identified and compensated by small current sources. All the small current sources used for matching compensation are controlled with thirty control signals. The thirty control signals is fed by 3-wire. From post-simulation results, the EVM with 0.67% can be achieved.

The circuit in this work is realized in TSMC 0.18um CMOS technology and composed of I/Q mixer, polyphase filter, LO I/Q buffers, and 3-wire. The total area of this chip is 1.65x1.25 mm^2 and the power consumption is 50.4mW.

From measurement results, the 3-wire is failed due to latch-up. The control signals for matching compensation can't be fed the circuit. So, the matching compensation can't work successfully. The performance of the I/Q mixer without any

matching compensation is measured with LO frequency form 2.4GHz to 2.7GHz. The I/Q mixer is measured with conversion gain of better than -11.15dB, the 1-dB compression point of 5dBm, the unwanted sideband suppression of better than 15dB, and the maximum LO feedthrough suppression of 15dB. Since the matching compensation can't be achieved by compensation circuit in the chip, the unwanted sideband suppression can be lowered as 38.5dB after manual compensation with tuning the magnitude and phase of baseband I/Q signals.

誌謝

得以順利完成此篇論文，首要感謝的是我的指導教授，郭建男教授，這近三年來的悉心指導，使我體悟到許多人生的大道理。此外，感謝參與工研院計畫的陳巍仁教授、溫文燊博士、工研院楊子毅組長，給予我相當多的建議與指導，在此獻上最深的敬意。

感謝昶綜、鈞琳、明清、鴻源等學長們的不吝指導，在許多方面給予我非常大的幫助；感謝一起研究、一同奮鬥、互相勉勵的俊興、燕霖，以及易耕、煥昇、俊豪、建忠、子超、信宇等學弟們，由於有了你們，實驗室就像一個溫馨的大家庭，非常感謝大家這兩年多來的照顧。另外還要感謝國家晶片中心在晶片製作上所提供的協助。

最後，要特別感謝我的家人給我的栽培與鼓勵，以及女友佩詩的陪伴與打氣，使我能順利的度過碩士生涯。還有很多其他要感謝的人，在此一併謝過。

余宗男

九十七年 五月

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CHAPTER 1

Introduction

1.1 Motivation

The standard of IEEE 802.16 family, popularly known as WiMAX, provides wireless transmissions of high data rates over metropolitan areas. The transmitted signal format may include complicated modulation such as 64-QAM. To ensure correct data receiving, the measure of error vector magnitude (EVM) quantifies the error of transmitted signals and defines the performance of digital radio transmitters. It is therefore critical to minimize the EVM.

Many non-ideal circuit effects contribute to EVM degradation in RF end, including LO phase noise, carrier feedthrough, I/Q imbalance, and nonlinearity. The normal figure of transmitter circuitry achieves the level from -20dB to -25dB. In the latest released WiMAX mobile standard [1], however, it defines a severe EVM level of -30dB, much higher than that as required by other standards such as WLAN. Recently, there are some circuit calibration solutions for this issue [2] [3].

In this thesis, an open-loop compensation mechanism for I/Q imbalance and LO feedthrough in the I/Q modulator is described to meet the specifications. Combined with simple power detection in the analog circuitry and decision making in the digital circuitry, auto-calibration can be realized in the transmitter circuit

1.2 Thesis Organization

In Chapter 2, the factors degrading EVM are identified and introduced how they influence EVM. And EVM specification of WiMAX is also defined.

In Chapter 3, the I/Q modulator with compensating I/Q imbalance match and LO feedthrough is designed. Also the compensation algorithm is proposed to cooperate with the I/Q modulator.

In Chapter 4, the circuit implement and measurement results are presented.

In the last Chapter, the work is summarized and concluded.

CHAPTER 2

EVM in Direct-Conversion Transmitter Consideration

2.1 Direct-Conversion Transmitter

The direct-conversion transmitter combines the signals of I and Q channels and converts baseband signals to radio-frequency. First the baseband codes are translated to analog signals by D/A converters and low-pass filters to suppress out-band spurious noise. Then the signals of I and Q channels are up-converted to RF and combined together by I/Q modulator. Almost over 90% of transmitter gain is in the RF block from the I/Q modulator to the PA. An RF band-pass filter is inserted between the driver amplifier and the PA to suppress the out-of-band interference.

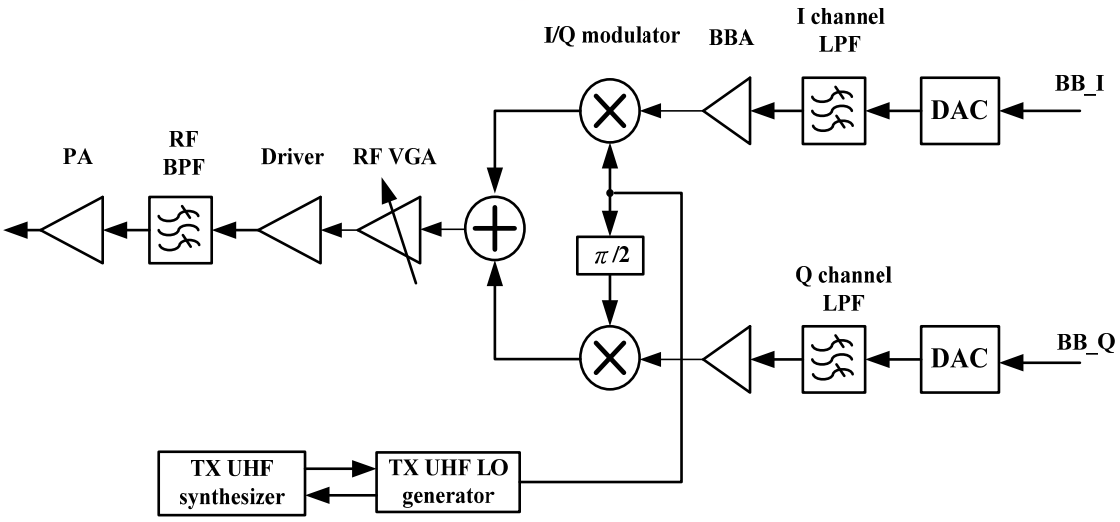

Fig 2.1 Block diagram of direct-conversion transmitter

The signal level in the transmitter is normally much higher than that in a receiver, and thus the noise figure is not as critical in the transmitter as in the receiver. The important parameters for a transmitter are the output power, especially the maximum output power, and the fidelity of the transmission waveform measured by modulation accuracy, EVM. In addition to these parameters of the desired transmission signal, the unwanted emissions, such as adjacent channel power and in-band and out-band noise/spurs emissions, are usually well defined in the mobile transmitter specifications.

This Chapter focuses on EVM analysis of direct-conversion transmitter. The sources that degrading EVM are discussed below.

2.2 Sources of Degrading EVM in General Consideration

EVM may be degraded by Intersymbol or Interchip Interference (ISI or ICI), Close-in phase noise of synthesized LO, LO feedthrough, I/Q Imbalance, and Nonlinearity. These sources are induced by the circuit blocks in direct-conversion transmitter and indicated in Fig. 2.2. We can identify how they affect EVM by [1]-[3] and define the system requirements to meet the specification.

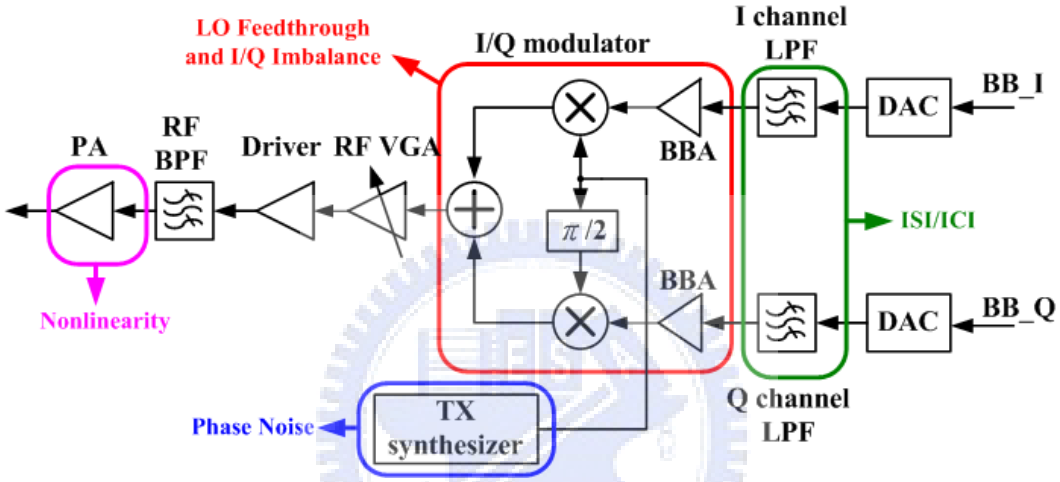

Fig 2.2 Factors degrading EVM in direct-conversion transmitter.

2.2.1 Intersymbol or Interchip Interference (ISI or ICI)

Intersymbol interference (ISI) is a form of distortion of a signal in which one symbol interferes with subsequent symbols. This is an unwanted phenomenon as the previous symbols have similar effect as noise, thus making the communication less reliable. ISI is usually caused by multipath propagation and the inherent non-linear frequency response of a channel. Ways to fight against intersymbol interference include adaptive equalization and error correcting codes.

The ISI or ICI of symbols or chips may have been created at beginning to generate a transmission signal. To obtain high spectral efficiency of the transmission

signal, the originally rectangular symbol or chip waveform is reshaped, and it is also called pulse shaping. The shaped symbol (or chip) waveform a_{TX_ideal} can be expressed as

$$a_{TX\_ideal} = h_{PS} * a_{rect}(t). \tag{2-1}$$

In the wireless systems, a complementary filter with an impulse response h_{PS_C} is normally used in the corresponding receiver side to equalize the phase and magnitude distortion and thus to eliminate or to minimize the ISI or ICI caused by the pulse shaping in the transmitter.

The filters in the transmitter path other than the pulse-shaping filter may cause the degradation of the modulation accuracy degradation especially when the pass-band of the filter, such as a channel filter, is close to the bandwidth of the transmission signal. Assuming the impulse response of the filter is $h_{fltr}(t)$, the shaped symbol or chip waveform a_{TX_ideal} after passing through the filter turns into

$$a_{TX}(t) = h_{fltr}(t) * a_{TX\_ideal}(t). \tag{2-2}$$

The corresponding EVM_{ISI} can be expressed by the impulse response function as [4]

$$EVM_{ISI} = \sqrt{\frac{\sum_{k=-\infty, k\neq 0}^{k=\infty} \left|h_{fltr}(t_0 + kT_s)\right|^2}{\left|h_{fltr}(t_0)\right|^2}}. \tag{2-3}$$

The terms in the numerator in the square root of (2-3) right side are ISIs or ICIs to the symbol or chip at t_0, and they are contributed from adjacent and other symbols or chips. Each term in the square root of (2-3) can be also obtained by means of the following formula:

$$\Delta I_{ISI}(\pm k) = \frac{\left|h_{fltr}(t_0 \pm kT_s)\right|}{\left|h_{fltr}(t_0)\right|} = \frac{\int_{t_0-\delta t}^{t_0+\delta t} \left|h_{fltr}(t \pm kT_s)\right| dt}{\int_{t_0-\delta t}^{t_0+\delta t} \left|h_{fltr}(t)\right| dt} \quad , \tag{2-4}$$

where k is equal to 1,2,3,⋯, and 2 δ t is the duration of sampling pulse. The equation (2-3) could be written as

$$EVM_{ISI} = \sqrt{\sum_{-\infty}^{\infty} \Delta I^2{}_{ICI}(k)} \, . \tag{2-5}$$

2.2.2 Close-in Phase Noise of Synthesized LO

Another main contribution to the degradation of the modulation accuracy is the close-in phase noise of the synthesizer applied as local oscillator of the up-converter in the transmitter. Assuming the vector error caused by the synthesizer phase noise $\emptyset_n(t)$ can be expressed as

$$\vec{a}'(t) = \vec{a}(t) + \vec{e}(t) = \vec{a}(t)\exp(j\phi_n(t)) \, . \tag{2-6}$$

The magnitude of the vector error then can be expressed as

$$\left|\vec{e}(t)\right|^2 = \left|\vec{a}'(t) - \vec{a}(t)\right|^2 \cong \phi_n{}^2, \tag{2-7}$$

where $|a(t)|$ is normalize to 1. The statistical average of $\emptyset_n{}^2(t)$ is the autocorrelation function of the phase noise. The autocorrelation function and the power spectrum density $S_n(f)$ have the following relationship

$$\lim_{n\to\infty} \frac{1}{nTs} \int_{-Ts/2}^{Ts/2} E\left\{\phi_n{}^2(t)\right\} dt = \int_{-\infty}^{\infty} S_n(f) df = P_{Nphase} \tag{2-8}$$

Hence the EVM_{Nphase} resulting from the phase noise of the synthesizers could be written as

$$EVM_{Nphase} = \sqrt{P_{Nphase}} \ . \tag{2-9}$$

Usually the phase noise within the loop bandwidth of synthesizers used in the mobile transmitters is in the range of -60 to -80 dBc/Hz. In the case of the synthesizer loop bandwidth being reasonable wide, P_{Nphase} could be approximated as

$$P_{Nphase} \cong 2 \cdot 10^{N_{phase}/10} \cdot BW_{synth\_loop} \ , \tag{2-10}$$

Where N_{phase} is the average phase noise, in dBc/Hz, within the synthesizer loop bandwidth, and BW_{synth_loop} is the bandwidth of the synthesizer loop filter in Hz. The EVM_{Nphase} in (2-4) could be modified as

$$EVM_{Nphase} = \sqrt{P_{Nphase}} \cong \sqrt{2 \cdot 10^{N_{phase}/10} BW_{synth\_loop}} \tag{2-11}$$

The equation if (2.11) could help us to define the specification of phase noise and loop bandwidth in the system.

2.2.3 LO Feedthrough

The DC offset in the baseband I and Q channels will cause LO feedthrough, and it will degrade the modulation accuracy of the transmission signal. Assuming the dc offset in the baseband I and Q channels are ΔI_{dc} and ΔQ_{dc}. The baseband signal $a'_I(t)$ and $a'_Q(t)$, in the I and Q channels are respectively represented by

$$a'_I(t) = \cos\phi(t) + \Delta I_{dc} \tag{2-12}$$

$$a'_Q(t) = \sin\phi(t) + \Delta Q_{dc} \ . \tag{2-13}$$

At the output of the modulator, the I and Q quadrature signals turn into a signal with an RF carrier, and it can be expressed as

$$\begin{aligned} RF_{out}(t) &= a'_I(t)\cos\omega_c t - a'_Q(t)\sin\omega_c t \\ &\cong A(t)\cos\left[\omega_c t + \phi(t)\right] + \Delta_{dc}\cos(\omega_c t + \Delta\theta) \end{aligned} \ , \tag{2-14}$$

where ω_c is the LO angle frequency and A(t), $\varphi(t)$, Δ_{dc}, and $\Delta\theta$ are obtained as

$$A(t) = \sqrt{\cos^2 \phi(t) + \sin^2 \phi(t)} \tag{2-15}$$

$$\phi(t) = \tan^{-1}\left(\frac{\sin \phi(t)}{\cos \phi(t)}\right) \tag{2-16}$$

$$\Delta_{dc} = \sqrt{\Delta I_{dc}{}^2 + \Delta Q_{dc}{}^2} \tag{2-17}$$

$$\Delta\theta = \tan^{-1}\left(\frac{\Delta Q_{dc}}{\Delta I_{dc}}\right) \tag{2-18}$$

The modulated signal is shown in Fig. 2.3 and also LO feedthrough induced error vector are indicated. How LO feedthrough affecting signal constellation could clearly be found out that it also contributes an error vector.

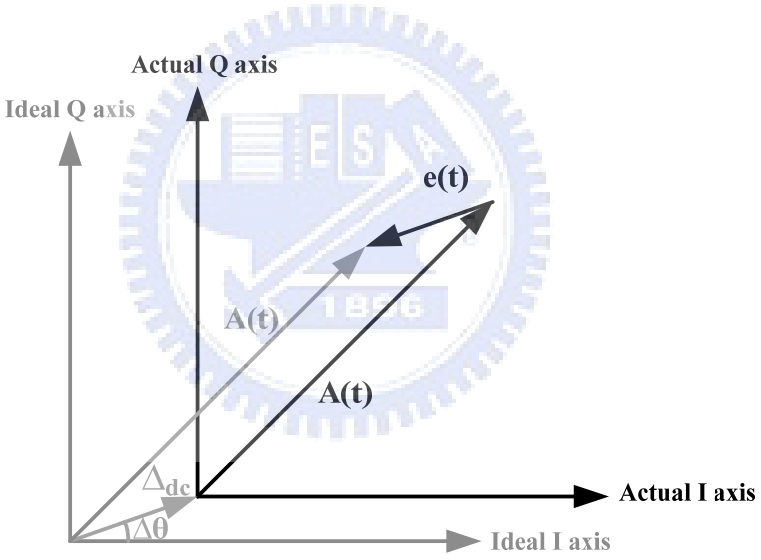

Fig. 2.3 LO feedthrough induced error vector

Since I/Q axis of I/Q constellation is moved by the LO feedthrough term of (2-14), from Fig2.3, the <e(t)> is with the same magnitude of Δ_{dc} and reverse direction of $\Delta\theta$. LO feedthrough suppression (LOFTS) in dB could be defined as

$$LOFTS = 10\log\frac{P_{LOFT}}{P_{TX}} = 20\log\frac{V_{LOFT}}{V_{TX}} = 20\log\frac{\Delta_{dc}}{\left|\overline{A(t)}\right|} \tag{2-19}$$

, where V_{LOFT} is Δ_{dc} and V_{TX} is A(t). And then EVM_{LOFT} which is contributed by LO feedthrough could simply be written as

$$EVM_{LOFT} = \frac{\left|\overline{e(t)}\right|}{\left|\overline{A(t)}\right|} = \frac{\Delta_{dc}}{\left|\overline{A(t)}\right|} = \frac{V_{LOFT}}{V_{TX}} = 10^{\frac{LOFTS}{20}} \quad . \tag{2-20}$$

So, the equation (2.20) could help us to define system specification of EVM which is degraded by LO feedthrough.

2.2.4 I/Q Imbalance

For single sideband modulation the amplitude and phase mismatches between I and Q generate unwanted sideband signal. By using ε and σ to represent amplitude and phase mismatches between quadrature LO signals, respectively. At the output of the modulator, the I and Q quadrature signals turn into a signal with an RF carrier, and it can be expressed as

$$\begin{aligned} RF_{out} \cong & \frac{\sqrt{1+2(1+\varepsilon)\cos\sigma+(1+\varepsilon)^2}}{2}\cos\left[\omega_c t+\phi(t)+\delta\right] \\ & + \frac{\sqrt{1-2(1+\varepsilon)\cos\sigma+(1+\varepsilon)^2}}{2}\cos\left[\omega_c t-\phi(t)+\gamma\right] \end{aligned} \tag{2-21}$$

, where δ and γ are

$$\delta = \tan^{-1}\frac{(1+\varepsilon)\sin\sigma}{1+(1+\varepsilon)\cos\sigma} \tag{2-22}$$

$$\gamma = \tan^{-1}\frac{-(1-\varepsilon)\sin\sigma}{1-(1+\varepsilon)\cos\sigma}. \tag{2-23}$$

The upper side of (2-21) is the desired signal and the lower side of (2-22) is the unwanted sideband signal. Hence the sideband suppression (SBS) in dB could be calculated as

$$SBS = 10\log\frac{1-2(1+\varepsilon)\cos\sigma+(1+\varepsilon)^2}{1+2(1+\varepsilon)\cos\sigma+(1+\varepsilon)^2} \tag{2-24}$$

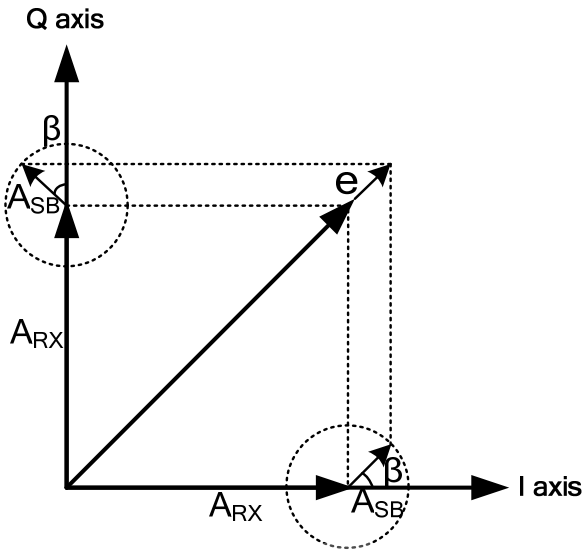

Fig 2.4 Unwanted sideband signal induced error vector

After received by the receiver, the transmitter output is converted to baseband I and Q channels as

$$\begin{aligned} BB_I &= \frac{\sqrt{1+2(1+\varepsilon)\cos\sigma+(1+\varepsilon)^2}}{2}\cos\phi(t) \\ &\quad + \frac{\sqrt{1-2(1+\varepsilon)\cos\sigma+(1+\varepsilon)^2}}{2}\cos(\phi(t)+\beta) \\ &= A_{RX}\cos\phi(t) + A_{SB}\cos(\phi(t)+\beta) \end{aligned} \tag{2-25}$$

$$\begin{aligned} BB_Q &= \frac{\sqrt{1+2(1+\varepsilon)\cos\sigma+(1+\varepsilon)^2}}{2}\sin\phi(t) \\ &\quad + \frac{\sqrt{1-2(1+\varepsilon)\cos\sigma+(1+\varepsilon)^2}}{2}\sin(\phi(t)+\beta) \\ &= A_{RX}\sin\phi(t) + A_{SB}\sin(\phi(t)+\beta) \end{aligned} \tag{2-26}$$

, where β is (γ-δ). The received signal constellation could be affected by the unwanted sideband signals as Fig.2.4 shown. When β is equal to zero, EVM_{SB} which is contributed by unwanted sideband is on the worst degradation and could be written as

$$EVM_{SB} = \frac{|\bar{e}|}{\sqrt{2}A_{RX}} = \frac{A_{SB}}{A_{RX}} = 10^{\frac{SBS}{20}} \quad (2\text{-}27)$$

So, the equation (2-27) could help us to define system specification of EVM which is degraded by I/Q imbalance.

2.2.5 Nonlinearity Influence

Transmitter usually operates well below its 1-dB compression point (P_{-1dB}). Thus, among the nonlinear effects, the third-order intermodulation of two nearby interferers is the major EVM contributor. The input third order intermodulation interception point is

$$IIP3 = \frac{P_{\inf o} - P_{IM3}}{2} + P_{\inf i}, \quad (2\text{-}28)$$

where P_{info} and P_{infi} are out-band signal power in the output and input, and P_{IM3} are in-band interference power of the 3rd intermodulation product. Hence the interference power could be written as

$$P_{IM3} = P_{\inf o} + 2P_{\inf i} - 2IIP3 = 3P_{\inf o} - 2OIP3, \quad (2\text{-}29)$$

where OIP3 is the output 3rd intercept point.

The EVM caused by 3rd intermodulation is just the square root ratio of the P_{IM3} to the desired RF signal power (P_{RFO}), as following

$$EVM_{IM3} \approx \frac{A_{IM3}}{A_{RFO}} = 10^{\frac{P_{IM3} - P_{RFO}}{20}} \approx 10^{\frac{3P_{\inf o} - 2OIP3 - P_{RFO}}{20}}. \quad (2\text{-}30)$$

And it could be used to define the system specification.

Since the nonlinearity in the transmitter is dominated by power amplifier (PA), the distortion of PA contains the amplitude distortion (AM-AM) and phase distortion (AM-PM). And the equation (2-30) just describes the intermodulation influence.

Furthermore the EVM degraded by PA is defined clearly in [4].

2.2.6 Total EVM

If all factors contributing to the degradation of the modulation accuracy are uncorrelated, the overall EVM if the transmission signal can be expressed as

$$\begin{aligned} EVM_{total} &= \sqrt{\sum_{k} EVM_k^2} \\ &= \sqrt{EVM^2{}_{ISI} + EVM^2{}_{Nphase} + EVM^2{}_{CFT} + EVM^2{}_{SB} + EVM^2{}_{IM3}} \end{aligned} \tag{2-31}$$

2.3 EVM in WiFi and WiMAX

EVM requirements for 802.11 are specified at -25 dB, which is required to achieve a 10% packet error rate. For 802.16, EVM is held to -31 dB, which is based on a 1% packet error rate. This lower error rate helps contribute to WiMAX longer range. The difference between 802.16 and 802.11 is indicated in TABLE I.

TABLE I Difference between 802.11 and 802.16

	WLAN (802.11)	WiMAX (802.16)
Bandwidth	Fixed; 20 MHz/52 Subcarriers	Variable; 1 to 28MHz/256 Subcarriers
Guard Interval	Fixed at 1/4 * Symbol Time	Variable; Ranges from 1/32 to 1/4 * Symbol Time
Spectral Efficiency	2.7 Mbits/s/Hz	3.1 to 3.8 Mbits/s/Hz
EVM Requirements	-25 dB	-30 dB
Receive Noise Figure	10 dB Maximum	7 dB Maximum
Duplexing	TDD	TDD, FDD, HFDD
Spectrum	Unlicensed	Licensed & Unlicensed
Transmit Dynamic Range	Tx Power Fixed	50-dB Range

A proper specification of sources degraded EVM are defined in Table I from [5] [6]. Since the EVM specification of 802.16 is stricter than 802.11, the RF transmitter of WiMAX could meet the requirement of WiFi by shifting carrier frequency.

From Fig. 2.2, the I/Q modulator includes two factors of degrading EVM, such as LO feedthrough and I/Q imbalance. So, in this work, I/Q modulator with eliminating LO feedthrough and I/Q imbalance are designed.

TABLE II EVM contribution from each source

Source	EVM (%)	EVM (dB)
ISI/ICI	0.5	-46
LO Phase Noise	2.37	-32.5
Carrier Feedthrough	0.56	-45
I/Q imbalance	1.58	-36
Nonlinearity	1	-40
Total	3.11	-30.13

2.4 Summary

The factors degrading EVM has been identified. We can realize how they degrading EVM by some circuit characteristics, such as ISI or ICI rising after passing channel filters, phase noise of synthesizer, unwanted sideband suppression, LO feedthrough suppression, and the input third order intermodulation interception point.

The specification about EVM in WiMAX is -30dB. From the circuit characteristics mentioned before, a proper specification for the factors degrading EVM and the required circuit characteristics is defined.

CHAPTER 3

Circuit Design for Direct Up-Conversion Mixer with Matching Compensation Eliminating I/Q Imbalance and LO Feedthrough in WiMAX and WiFi Transmitter

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The auto-compensation techniques for I/Q imbalance can be separated into two kinds of feedback loops of power detection loop [7] and dummy path for extracting error messages [8]. The power detection loop needs more iteration for achieving an optimal condition and less additional hardware. The loop with dummy path for extracting error messages can get error messages with less iteration but needs more hardware.

However, the two feedback loops need an open loop circuit to tune the I/Q magnitude imbalance and phase imbalance. In this work, I/Q modulator with an open loop compensation circuit to tune the I/Q imbalance and LO feedthrough is presented. Since LO buffers are originally needed, we design the LO buffers with magnitude and phase tuning without another hardware. An auto-compensation algorithm is developed for power detection loop with advantage of needing less additional hardware. By applying the algorithm for co-simulated with the I/Q modulator, the specification of EVM in Table II can be achieved.

The proposed I/Q modulator in this thesis is shown in Fig. 3.1. The I/Q mixer is based on conventional double balanced Gilbert Cell mixer with LO feedthrough

adjustments. Before LO I/Q signals is fed the I/Q mixer, LO buffers are placed to tune the magnitude and phase of LO I/Q signals. The two stages of polyphase filter are placed before I/Q buffer to generate quadrature LO signals for measurement consideration.

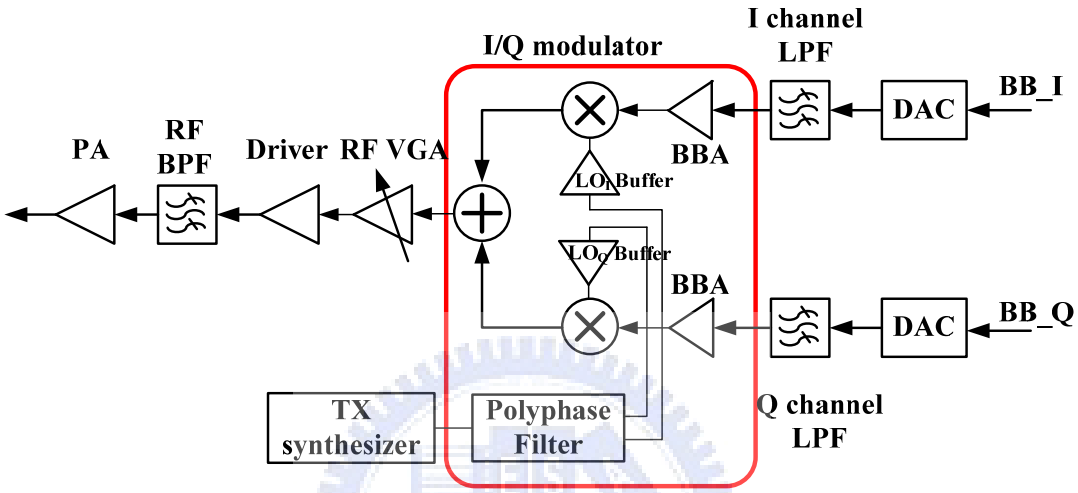

Fig. 3.1 Proposed I/Q modulator

3.1 LO Feedthrough in Up-Conversion Mixer Consideration

The main advantage of double balanced Gilbert Cell mixer shown in Fig. 3.2 is LO cancellation. However, LO feedthrough accompanies imperfect LO cancellation. The LO feedthrough due to dc current offset induced by the transconductance stages (M_{t+} and M_{t-}) device mismatch, switching stage device mismatch, and differential LO signals imbalance, are identified in this thesis. A compensation method is developed to suppress the LO feedthrough.

3.1.1 Factors of Inducing LO Feedthrough

First, we need to identify whether the switching stage (M_{S1}-M_{S4}) or the transconductance stages (M_{t+} and M_{t-}) device mismatch of a double balanced Gilbert Cell mixer causes a larger LO feedthrough. The switching stage (M_{S1}-M_{S4}) device mismatch induces the DC current mismatch of M_{S1} and M_{S3} or M_{S2} and M_{S4}. This DC current mismatch causes imperfect LO cancellation. However, it has less impact to LO feedthrough since the double balanced mixer uses differential topology and can suppress it. The DC current offset between the transconductance stages, M_{t+}, and M_{t-}, is induced by the transconductance stages (M_{t+}, M_{t-}) device mismatch. If the DC current of M_{t+} is larger than M_{t-}, it should further degrade the current matching of M_{S1} and M_{S3}, or M_{S2} and M_{S4}. This effect can't just be suppressed by differential topology. Here, the Monte-Carlo simulations of LO feedthrough use Table III which is supported in TSMC 0.18um technical documents for device mismatch reference. As Fig. 3.3 and Fig. 3.4, the switching stage (M_{S1}-M_{S4}) device mismatch induces small LO feedthrough and the two transconductance stages (M_{t+}, M_{t-}) device mismatch induces larger one. So, the main factor degrading LO feedthrough is the transconductance stages (M_{t+}, M_{t-}) device mismatch. So, the DC current offset of the

Table III TSMC 0.18um technical documents for device mismatch reference

	1.8V NMOS	1.8V PMOS	3.3V NMOS	3.3V PMOS
σVth0 (mV)	3.635*geo_fac	4.432* geo_fac	6.227* geo_fac	4.525* geo_fac
σXL / L (%)	0.458* geo_fac	0.396* geo_fac	0.365* geo_fac	0.247* geo_fac
σXW / W (%)	0.373* geo_fac	0.326* geo_fac	0.298* geo_fac	0.201* geo_fac
σTox / Tox (%)	0.101* geo_fac	0.0873* geo_fac	0.0804* geo_fac	0.0543* geo_fac
Where geo_fac=1/sqrt(N*Leff*Weff) (1/um)				

two transconductance stages needs to be compensated.

Besides DC current offset, there is another factor degrading LO feedthrough, the differential LO signals imbalance. The differential LO signals imbalance can be viewed as a common mode signal existing in differential LO signals. Since the source couple pair is with high common mode rejection ratio, the LO cancellation could be almost perfect. However, the differential LO signals imbalance could still enlarge LO feedthrough when the M_{S1}-M_{S4} or the two transconductance stages (M_{t+}, M_{t-}) are with device mismatch. If the DC current offset of the two transconductance stages can be compensated, the differential LO signals imbalance can be ignored.

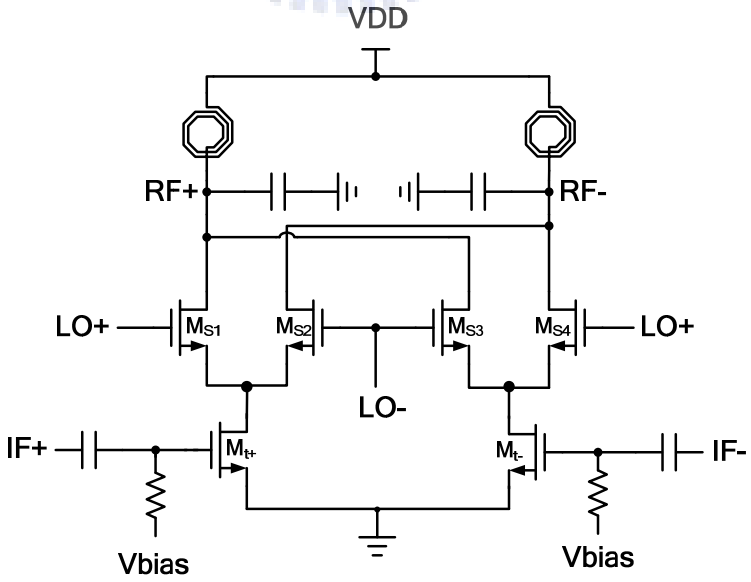

Fig. 3.2 Double balanced Gilbert Cell mixer

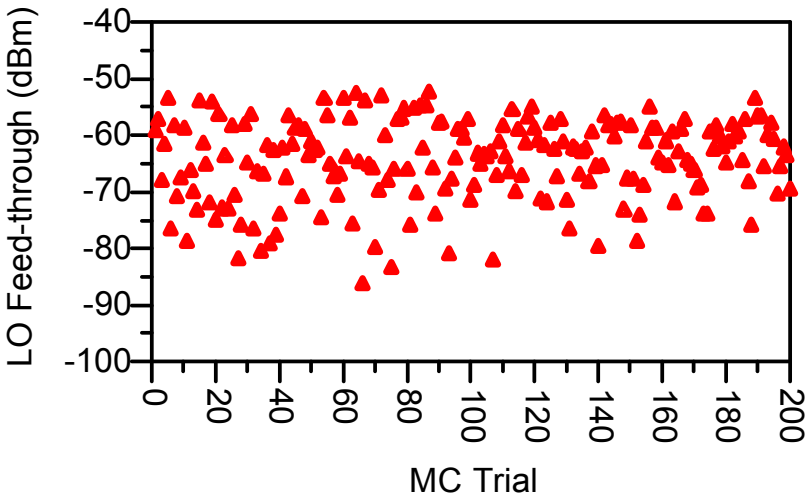

Fig. 3.3 Monte-Carlo analysis of LO feedthrough due to switching stage device mismatch

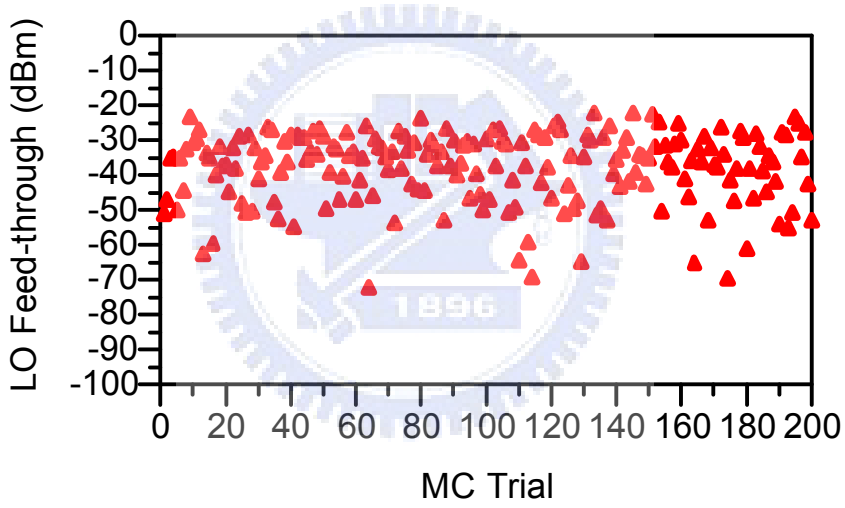

Fig. 3.4 Monte-Carlo analysis of LO feedthrough due to switching stage and transconductance stage device mismatch

3.1.2 I/Q Mixer Design for LO Feedthrough Suppression

Gilbert cell is used for I/Q mixer topology with resonant loads of LC tanks and current summation for combining I-channel and Q-channel signals as shown in Fig.3.7. The I/Q mixer is designed with IIP3 of 10dBm and conversion gain of -7dB at LO power of 6dBm. The total power consumption of I/Q mixer is 13.8mW.

The DC current offset resulting from device mismatch of the two transconductance stages needs to be suppressed to lower LO feedthrough. A compensating circuit with IDACs has applied to compensate DC current offset of the two transconductance stages in the I/Q mixer, as shown in Fig.3.7. The two switches of M_{IS+} and M_{IS-} or M_{QS+} and M_{QS-} decide which transconductance stage of M_{It+} and M_{It-} or M_{Qt+} and M_{Qt-} has less current and needs to be compensated. Since the IDACs have quantization error, the compensation of DC current offset is imperfect. The optimal resolution of the IDACs needs to be identified and ensures the quantization error of it doesn't degrade LO feedthrough too much.

The I/Q mixer is designed with output signal of 0dBm, since it has good linearity. From Table II, LO feedthrough needs 45dB suppression relating to desired signal. Since the desired signal power of the I/Q mixer in this work is 0dBm, the LO feedthrough needs to be designed below -45dBm. By using the standard deviation of device mismatch in Table III for Monte-Carlo analysis, the maximum allowed DC current offset between the two transconductance stages can be identified. From the result shown in Fig.3.5, the DC current offset between the two transconductance stages needs to be set below 5uA to obtain LO feedthrough of -45dBm. On the other hand, the quantization error and the resolution of the IDAC have a maximum value of 5uA and 10uA. Besides, the maximum DC current offset of the two transconductance stages can be obtained by Monte-Carlo analysis of the two transconductance stages device mismatch. As the result of Fig.3.6 shown, the maximum DC current offset is 80uA. Two 4-bit IDACs are used to provide the compensation current with 0~150uA to cover the maximum DC current offset and each bit resolution is 10uA in the I/Q mixer.

However, in practice the routing difference of double balanced mixer induces

imperfect LO cancellation, and LO feedthrough is generated. An inverse phase of LO feedthrough can be induced by using IDACs and then compensate it.

Since the DC current offset is with the order of 10^{-6} ampere, it's hardly to sense the current difference between the two transconductance stages. In this work, a compensation algorithm is used to directly detect the power of LO feedthrough and find the optimal compensation current with minimum power of LO feedthrough. This algorithm is discussed in session 3.4.1.

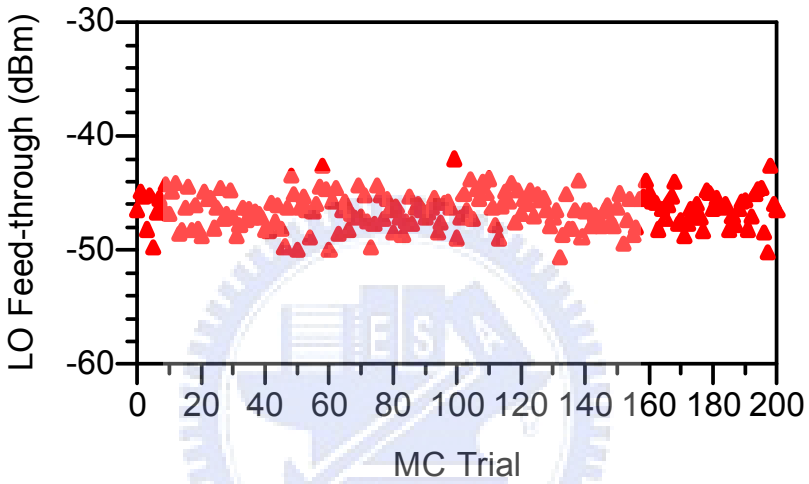

Fig. 3.5 Monte-Carlo analysis of LO feedthrough due to switching stage device mismatch with the DC current offset of the two transconductance stages 5uA

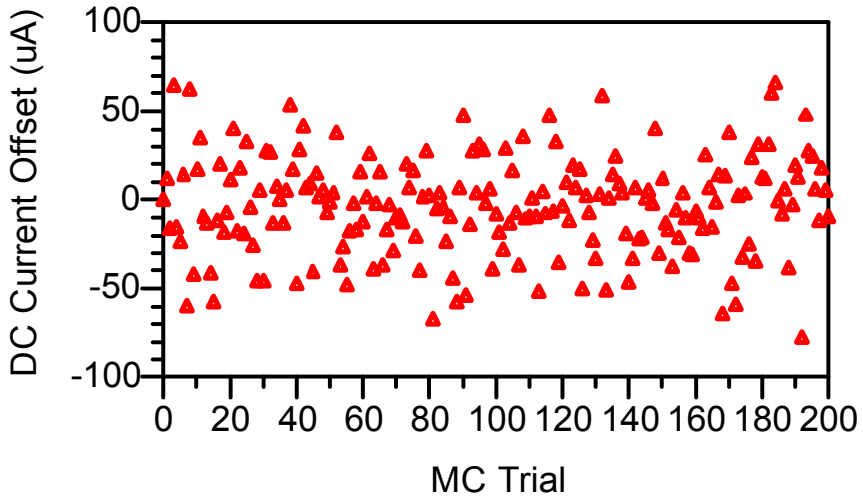

Fig. 3.6 DC current offset of the two transconductance stages device mismatch by Monte-Carlo analysis

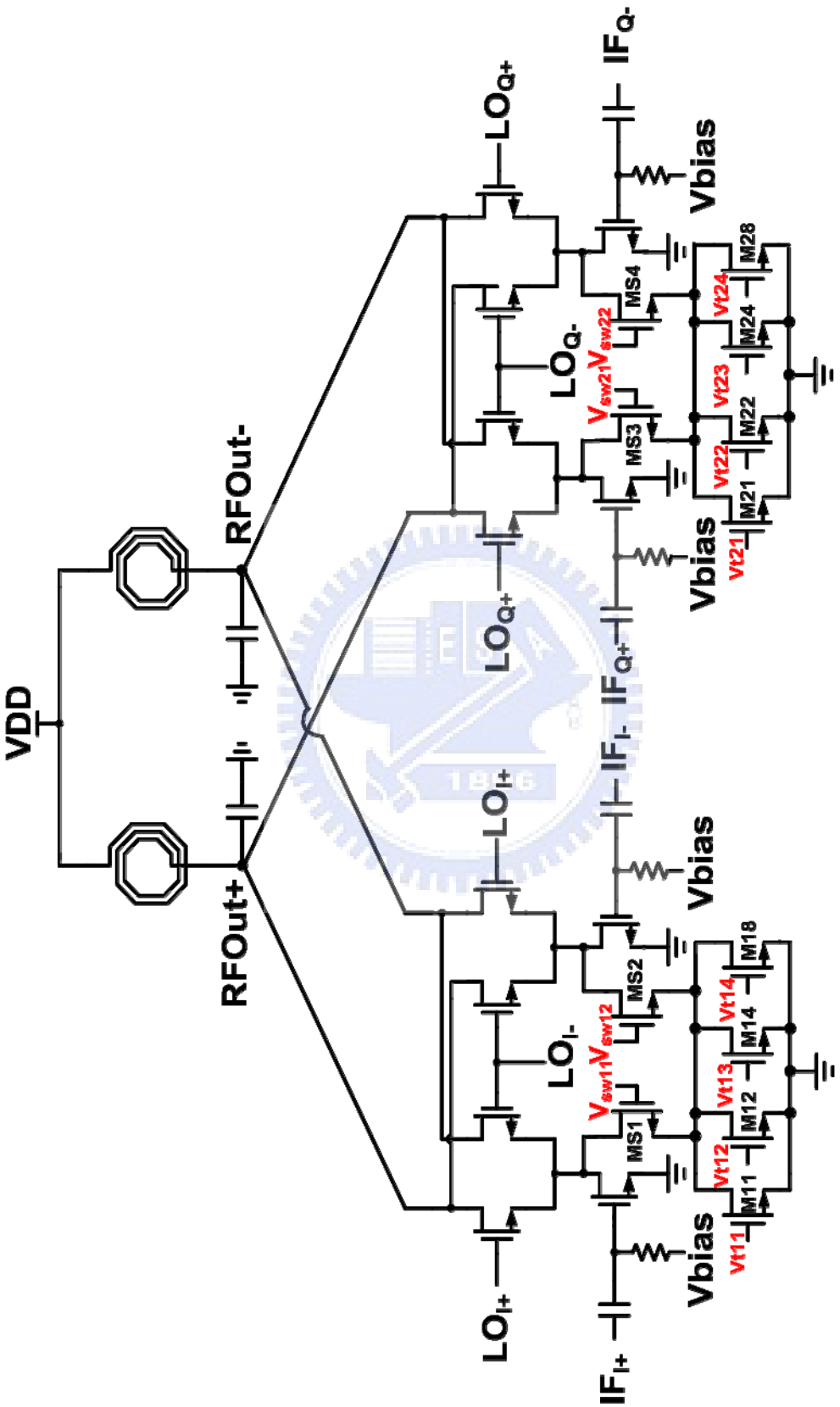

Fig. 3.7 Proposed I/Q mixer

3.2 I/Q Imbalance Compensation Circuit Design for Up-Conversion I/Q Mixer

3.2.1 I/Q Imbalance Equivalent Model

In homodyne system, the up-converter is composed of I/Q mixer, I/Q LO, and summation circuit. Both imbalance I/Q baseband signals and imbalance I/Q LO signals bring magnitude and phase mismatches to the I/Q modulator. The mismatch model of I/Q modulator is shown as Fig.3.8. After some calculations, all the non-ideal effects due to both baseband and LO signals can be all refer to LO only, as indicated in Fig.3.8. So by adjusting the magnitude of LO Q-path and phase of LO I-path, we can compensate I/Q imbalance.

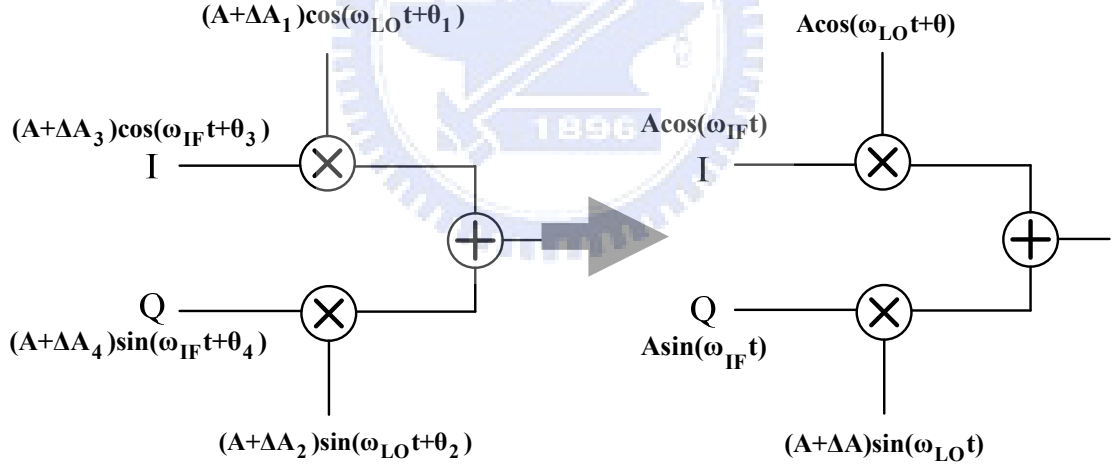

Fig. 3.8 I/Q imbalance equivalent model

3.2.2 I/Q Imbalance Compensation Mechanism

I/Q mismatch could be compensated by adding some vector on I or Q path. A simple I/Q constellation of QPSK is shown in Fig.3.9(a). In this work, both the magnitude and phase mismatch will be manipulated using magnitude compensation.

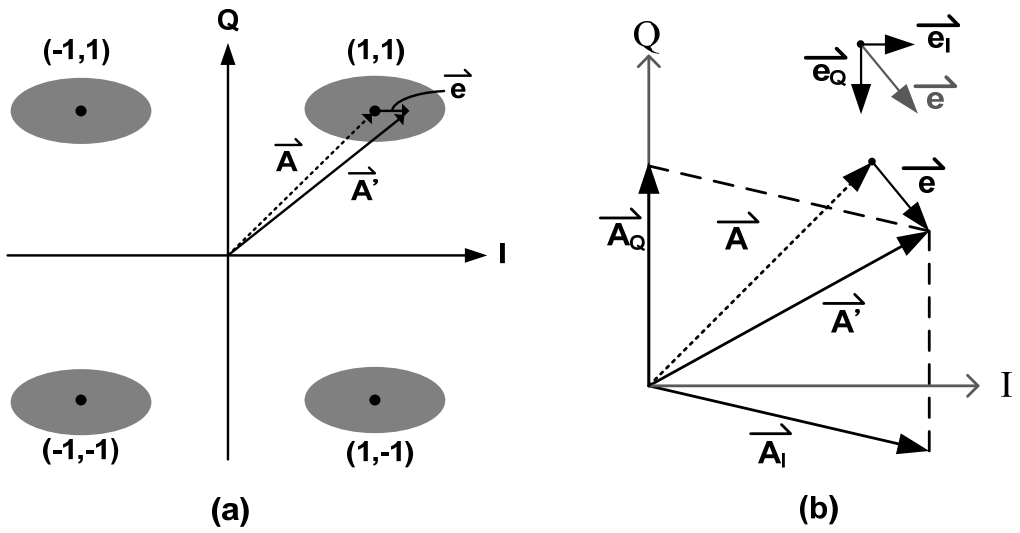

Fig. 3.9 (a) The constellation of QPSK and the error vector. (b) The error vector analysis in I/Q plane

For example, from Fig.3.9(b) the I-channel signal accrue with non-quadrature phase error relating to Q-channel. This phase error is mainly generated by $\langle e_Q \rangle$ and could be taken away by tacking on some Q-channel signal which is with equal magnitude of $\langle e_Q \rangle$ and in reverse direction of $\langle e_Q \rangle$. An error vector $\langle e_I \rangle$ can be referred to I-axis and it can be thought as I channel signal induces magnitude error onto Q channel. If this mismatch needs to be removed, we can increase Q-channel magnitude by $\|\langle e_I \rangle\|$. Applying this mechanism, all magnitude and phase imbalance could be removed.

I/Q imbalance compensation method is separated into three steps in this work. In Fig.3.10(a), first, the original I/Q constellation shows mismatch is appeared and the Q-path signal is set to be phase reference. Second, there is non-quadrature phase error in the I-path, so the I-path signal is added by some ratio of the Q-path signal to compensate its phase and this phase error can be removed as shown in Fig.3.10(b). During phase compensation, magnitude mismatch arises, so the final step is to adjust the Q-path magnitude equal to the I-path, shown in Fig.3.10(c). Through these three steps I/Q imbalance could be removed.

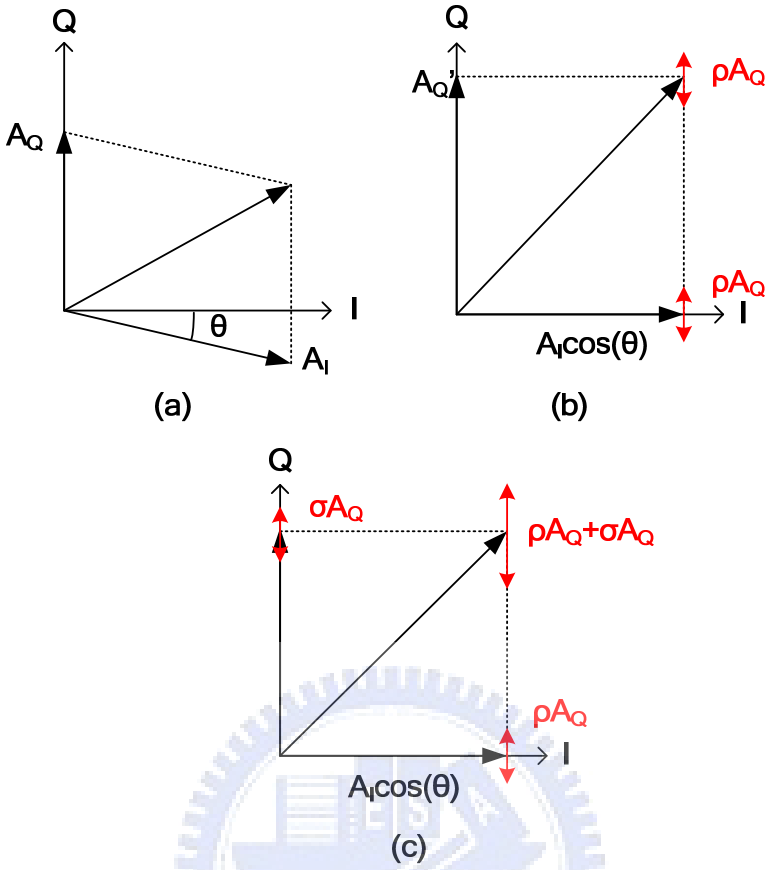

Fig. 3.10 I/Q compensation steps of (a) with original I/Q constellation point,(b) with compensating phase error of I-channel, and (3) with compensating magnitude error of Q-channel.

Since digital control is used, the resolution of each control bit needs to be defined. If each control has resolution of Δε, the compensation method has compensation error of Δε/2. From Fig.3.10(c), if magnitude and phase adjustments have compensating resolution of σA_Q and ρA_I, the compensation error from resolution of digital control is $(\rho A_I+\sigma A_Q)/2$. The specification of EVM contributed by I/Q imbalance is set to be 1.58% in Table II. From EVM fundamental equation calculations, we can get:

$$\frac{A_Q(\sigma+\rho)/2}{\sqrt{2}A_I\cos\theta} \le 1.58\% \qquad (3\text{-}1)$$

If the maximum phase error θ is supposed to 15°, the Eq.(3-1) above could be simplified as

$$\frac{A_Q(\sigma+\rho)}{A_I} \approx (\sigma+\rho) \le 4.32\% \tag{3-2}$$

The σ and ρ are designed as 2% and 0.7% respectively for over-designed. EVM from σ and ρ chosen in this work can be 0.95% by Eq.(3-3). From Eq.(2-27), the unwanted sideband suppression can be calculated as -40.4dB relating to desired signal.

$$EVM = \frac{A_Q(\sigma+\rho)/2}{\sqrt{2}A_I \cos\theta} \tag{3-3}$$

3.2.3 LO I/Q Buffer Design

Since the I-path of LO needs to be added by the ratio of ρ to Q-path to achieve I/Q phase imbalance compensation for I-buffer, the current mode operation is used as shown in Fig.3.11. The voltages of LO_I and LO_Q are translated to currents by transconductance stages and then summed at the output node. The load of Z_L is put in the output node to translate the current to voltage again. From foregoing analysis, the G_{m2} needs to be with the resolution of ρG_{m1}. The magnitude compensation for Q-buffer also uses this scheme as shown in Fig.3.12. The ΔG_{m3} needs to be with the resolution of σG_{m3}.

The LO I/Q buffers in Fig. 3.13 is designed to achieve the schemes discussed above. In I-buffer three source couple pairs act two different characteristics in I- or Q-buffer in Fig. 3.13. The two source couple pairs of M_{i1} and M_{i4} or M_{i2} and M_{i3} are with different bias current by IDACs of i_{d1} to generate Δg_m between M_{i1} and M_{i3} or M_{i2} and M_{i4} as the same as G_{m2} in Fig. 3.11. The other one of M_{i5} and M_{i6} is offered constant g_m as the same as G_{m1} in Fig. 3.11. In Q-buffer the source couple pair of M_{q5}

and M_{q6} is with linear g_m to IDACs of i_{d2} as the same as G_{m3} in Fig. 3.12. The I-path of LO in Fig.3.13 is without any effect since the two source couple pairs of M_{q1} and M_{q4} or M_{q2} and M_{q3} are with identical bias current.

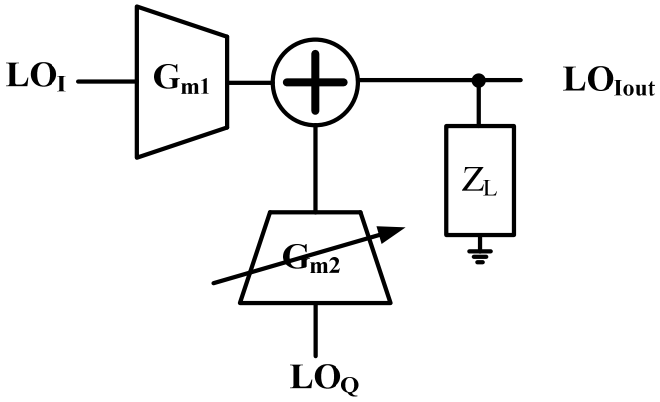

Fig. 3.11 Current mode operation of I-buffer

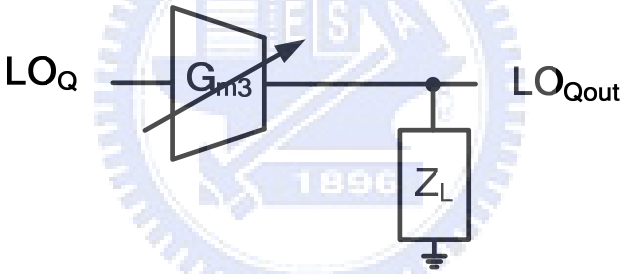

Fig. 3.12 Current mode operation of Q-buffer

The I/Q imbalance due to loading effect produced by I/Q buffers can be ignored since they are identical. In I-buffer, Q-path signal is combined with I signal to tune the phase of I-path. Complementary IDACs of $\pm i_{d1}$ drive the two source couple pairs to get small g_m variation of Q signal in I buffer. Hence we can get I_{out} from Eq.(3-4).

$$I_{out} = \left[A_Q \cdot 2\left(g_{mi1} - g_{mi3}\right) + A_I \cdot 2g_{mi5} \right] \cdot R_L \qquad (3\text{-}4)$$

, where g_{mi1} and g_{mi3} are g_m of Mi1 and Mi3, respectively. The two 4-bit control signals are designed to control this complementary and bidirectional IDACs. The

resolution of the IDACs needs to be set to make g_{mi1} and g_{mi3} as Eq.(3-5) shown

$$(g_{mi1} - g_{mi3}) / g_{mi5} = \rho A_Q / A_I \approx 2\% \tag{3-5}$$

However, the resolution of IDACs roughly make the phase vary with 1˚ from Eq.(3-6)

$$\sin^{-1}(2\%) \approx 1.1^\circ \tag{3-6}$$

Q buffer are implemented by exchanging the input signals of I buffer, as shown in Fig. 3.13. Since the I-path of Q buffer is without DC current variation and g_{mq1} and g_{mq3} are always the same, the I-path contributing to Q_{out} is equal to zero. And the source couple pair of M_{q5} and M_{q6} is used to achieve variable magnitude function of the Q-path signal by changing the IDAC of i_{d2}. The resolution of the IDAC controls g_m variation with

$$\Delta g_{m5} / g_{mq5} = 2\sigma A_Q / A_Q(0) = 0.7\% \tag{3-7}$$

Since the IDAC needs to be bidirectional to increase or decrease the Δg_{m5}, the 10-bit control signal is designed to control this bidirectional IDACs.

The g_m of M_{i1}~M_{i4} in response to I_{D1} is shown in Fig.3.14. There are three biasing regions to choose. In the high slope region the Δg_m is large with high sensitivity to I_D. The power consumption can be saved for M_{i1}~M_{i4} but not the case for M_{i5}~M_{i6}. With the larger Δg_m the $g_{mi,q5}$ and $g_{mi,q6}$ should also be larger in response. This leads to even larger power consumption. Meanwhile, the i_{d1} needs to be small enough to obtain the desired linear variation. The low slope region is also undesired with the high biasing current but insufficient compensation capability. Consequently, the medium slope region is a preferred choice.

As the design result, the linear g_m variation along with i_{d1} varying from

-0.32~0.32 mA is achieved by a source couple pair with tail current of 1.4mA, as shown in Fig.3.15. Fig.3.16 shows the linear response of Δg_m of (g_{mi1}-g_{mi3}) or (g_{mi2}-g_{mi4}) to i_{d1}. Two 4-bit IDACs are used for both directional tuning, such that each direction has 15 tuning steps. For the dynamic range of 0.32mA the current increases by 21uA for each step. The resolution of the IDACs is set as 21uA. The Δg_m versus control bits are with slope of 0.28mS/bit. With Δg_m decided, the $g_{mi5,6}$ is set as 14 mS from Eq.(3.8) and Fig. 3.17.

$$gm_{i5,6} = \Delta g_m / 2\% = 14mS \tag{3-8}$$

The value of I_{D1} has been designed accurate as above. Then the parasitic effects in high frequency operation should be considered. In respect of this, the value of I_{D2} needs to be fine tuned without changing I_{D1} and i_{d1}. Fig.3.18 and Fig.3.19 shows the simulation results for high frequency operation. The optimal I_{D2} setting is found at 1.8mA, fulfilling the requirement of Eq.(3-7).

Fig.3.19 shows the linear g_m variation with I_{D2} as I_{D2} being around 1.8mA. Hence the I_{D2} can be used for magnitude tuning in Q buffer. From Eq.(3-2-5) each I_{D2} tuning step for magnitude tuning is set as 0.7%. With this setting simulation result shows the g_{mq5} variation to I_{D2} as 2.022mS/mA. Consequently, the i_{d2} in Q buffer is set as 20uA. The final I/Q buffer simulation results are shown in Fig.3.20 and Fig.3.21, for the phase tuning of I-buffer and the magnitude tuning of Q-buffer, respectively. Each step of phase tuning and magnitude tuning are 1° and the ratio of 0.07. In later section the LO I/Q buffer are combined with the I/Q mixer and the compensation algorithm are used to implement the I/Q imbalance compensation.

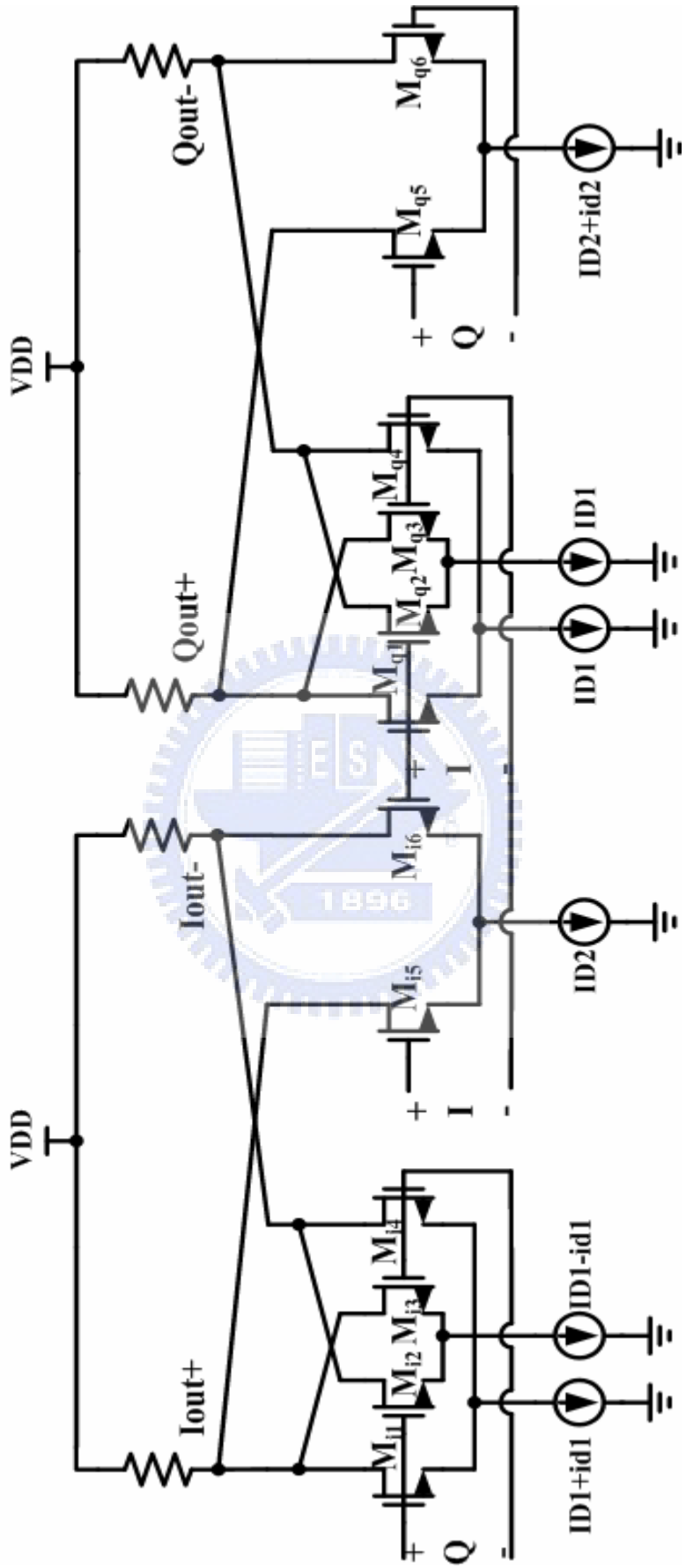

Fig. 3.13 I/Q buffer schematic

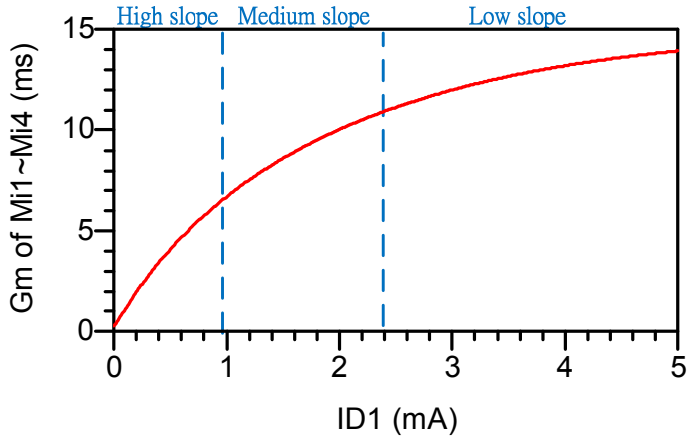

Fig. 3.14 The g_m of M_{i1}~M_{i4} in response to I_{D1}

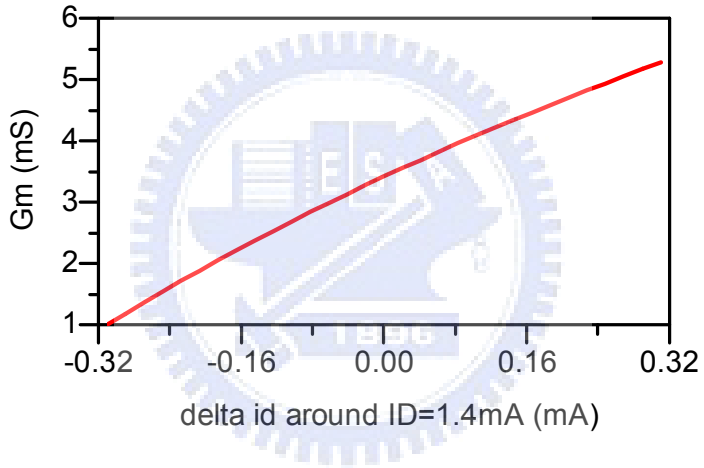

Fig. 3.15 Linear gm variation of M_{i1}~M_{i4} along with i_{d1}

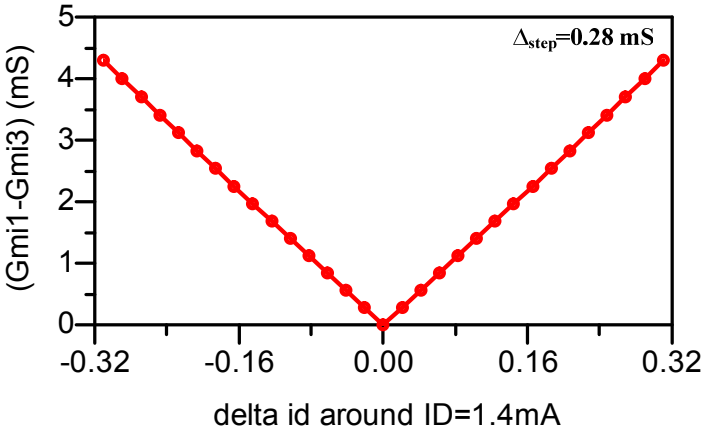

Fig. 3.16 The linear response of Δg_m of (g_{mi1}-g_{mi3}) or (g_{mi2}-g_{mi4}) to i_{d1}

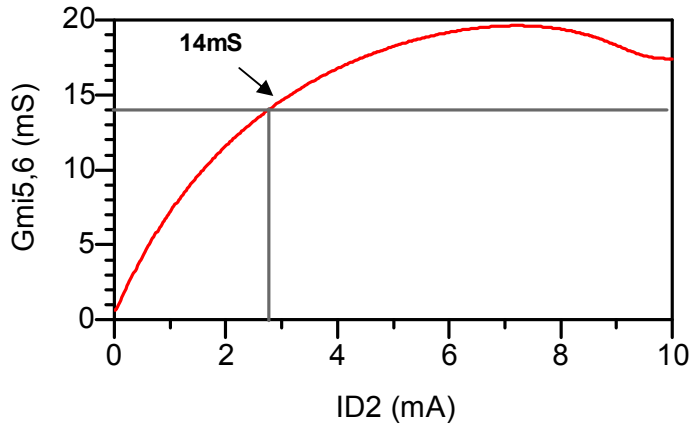

Fig. 3.17 The g_m of M_{i5}~M_{i6} and M_{q5}~M_{q6} in response to I_{D2}

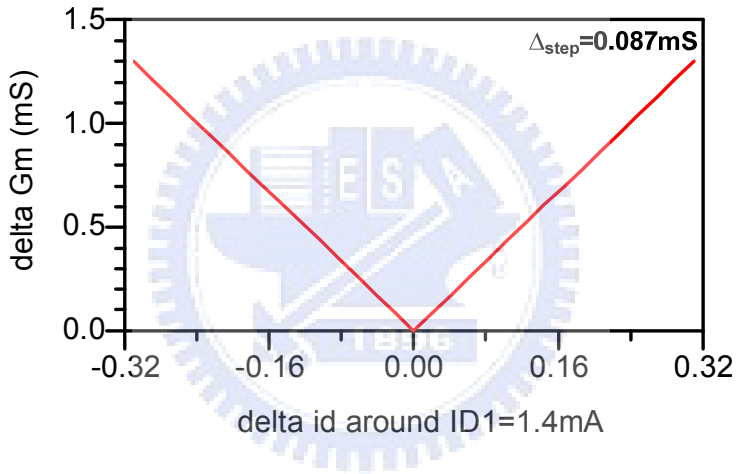

Fig. 3.18 Frequency response to the relation of Δg_m of (g_{mi1}-g_{mi3}) or (g_{mi2}-g_{mi4}) to i_{d1}

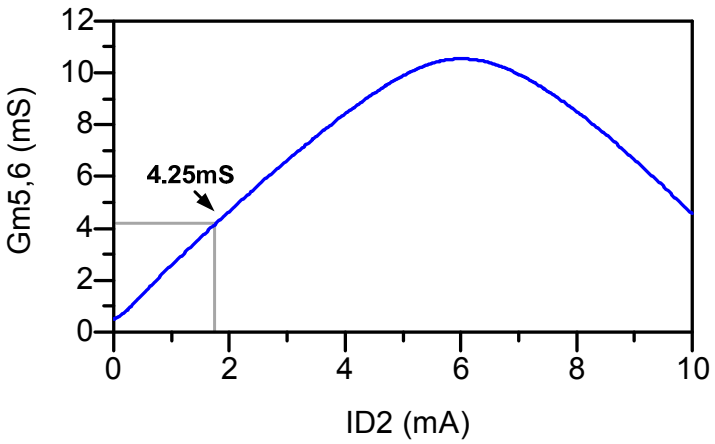

Fig. 3.19 Frequency response to the g_m of M_{i5}~M_{i6} and M_{q5}~M_{q6} in response to I_{D2}

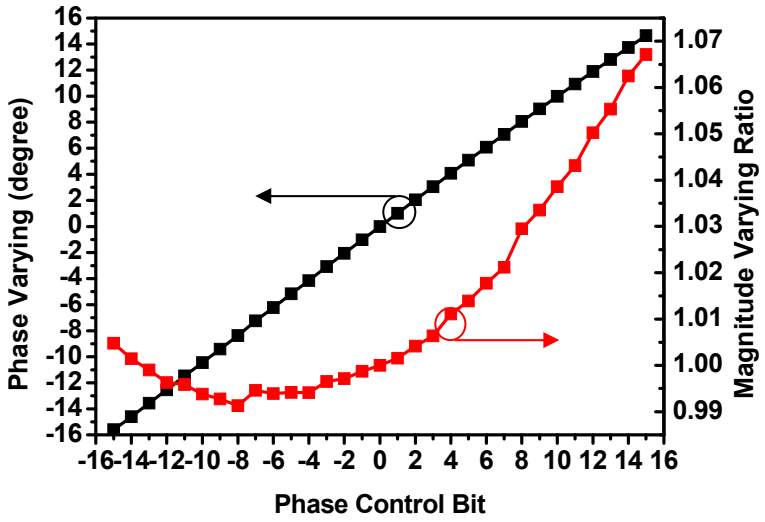

Fig. 3.20 The phase and magnitude of I-buffer varying with control bits

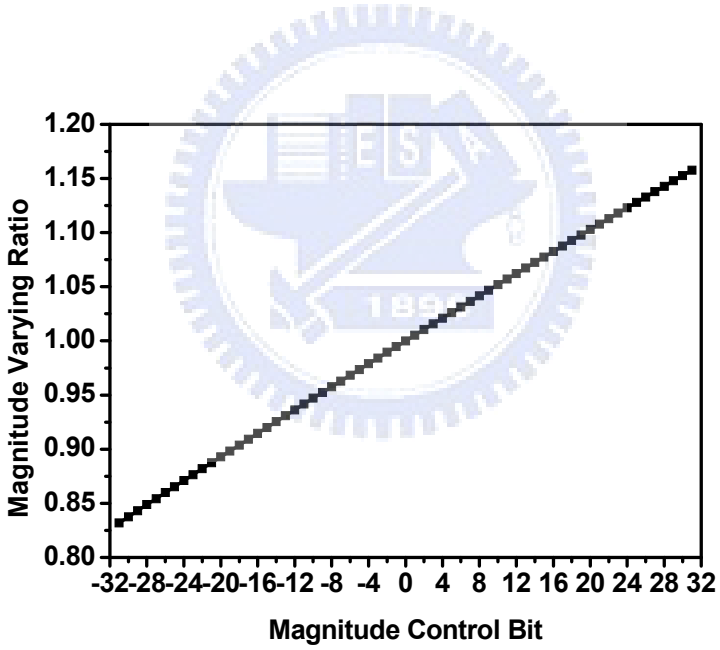

Fig. 3.21 The magnitude of Q-buffer varying with control bits

3.3 Algorithm for I/Q Imbalance and LO Feedthrough Compensation

The compensation algorithm is with the order of LO feedthrough, I/Q phase imbalance, and I/Q magnitude imbalance. Since the I/Q phase imbalance causes magnitude of I-path varying simultaneously. It needs to put the I/Q phase imbalance compensation before I/Q magnitude imbalance compensation.

3.3.1 Algorithm for LO Feedthrough Compensation

In LO feedthrough compensation mode, an extra closed loop needs to be designed with pre-amplifier, power detector, sample-and-hold circuit, and comparator. Baseband signals are not to be fed the I/Q mixer. So LO signals at output node can directly be detected by PD. First, the initial LO feedthrough is detected by PD and sampled and held by S/H. Second, the IDAC of the I/Q mixer is changed with one bit of LSB (less significant bit), and LO feedthrough is detected by PD. Since the previous state of PD output is held in S/H, the comparator can be used for deciding which one is larger. With this method, the direct aspect of decreasing the bits of IDACs or increasing the bits of IDACs can be identified, and also which sides of M_{It+} and M_{It-} or M_{Qt+} and M_{Qt-} in Fig.3.7 needs to be compensated. The completed algorithm is indicated in Fig.3.22. The algorithm would stop when the comparator switches the polarity. This means it has found the optimal compensating current for minimizing LO feedthrough in previous state and in the current state LO feedthrough is enlarged by undesired compensation current. So, this algorithm could find the minimum values of LO feedthrough under the condition of no baseband signals.

Since the routing difference results in LO feedthrough as mentioning in session

3.1.2, the post-simulation uses this algorithm to get a minimum LO feedthrough. First, the Q-mixer is compensated with the bit number of IDACs from initial 0 to 10 as Fig.3.23 shown. Second, the I-mixer is compensated with bit number of IDACs from initial 0 to 10 as Fig.3.24 shown. After compensation, a -60dBm power of LO feedthrough can be obtained.

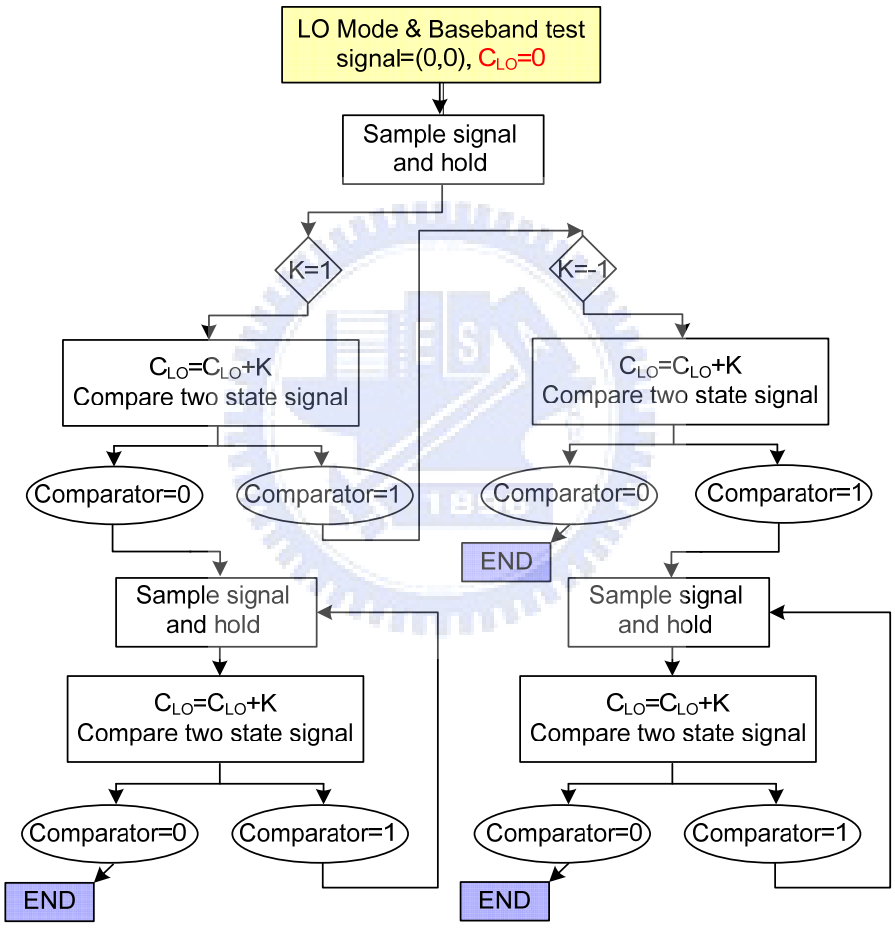

Fig. 3.22 Algorithm for LO feedthrough compensation

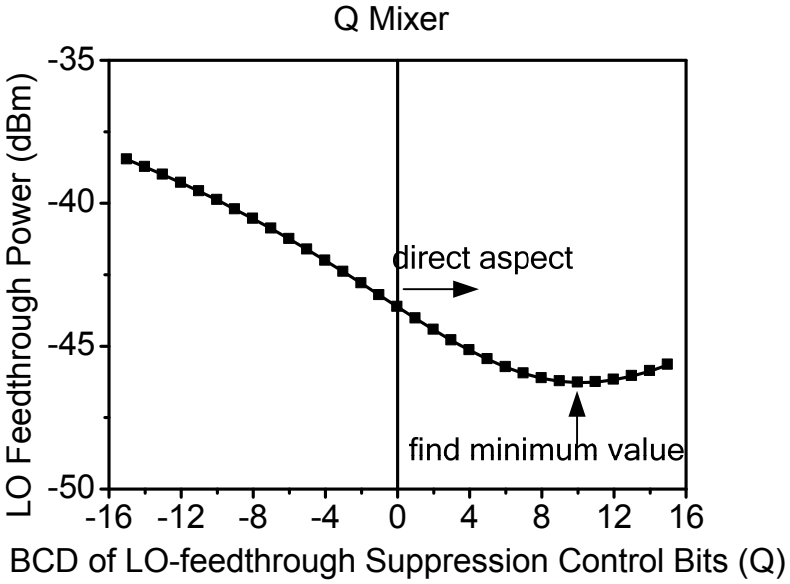

Fig. 3.23 The post simulation result of Q-mixer by using LO feedthrough compensation algorithm

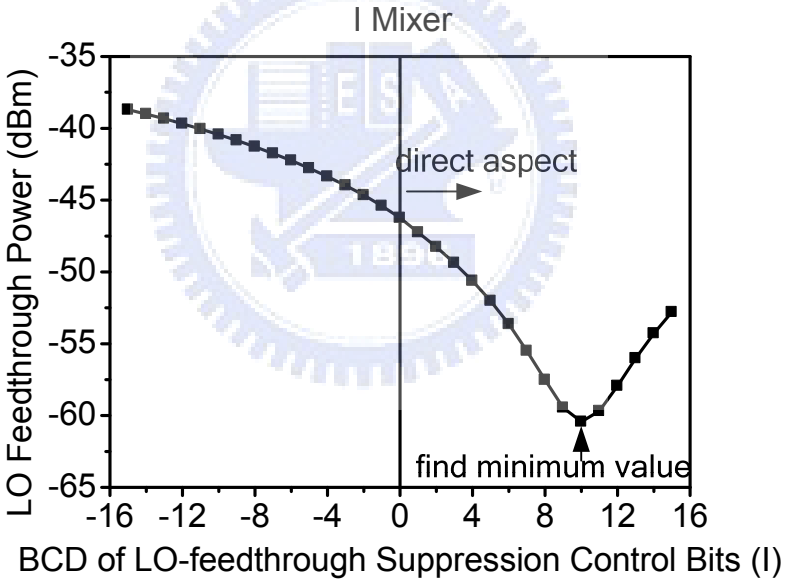

Fig. 3.24 The post simulation result of I-mixer by using LO feedthrough compensation algorithm

3.3.2 Algorithm for I/Q Phase Imbalance Compensation

The phase imbalance generally is hardly to be directly sensed since the signal is up to Giga hertz and I/Q signal has been combined at the output of I/Q mixer. If an

extra path is created to help sense the phase difference, the path might contribute gain imbalance or phase imbalance simultaneously. In this work two sets of baseband test signals are used without extra hardware in RF block to avoid another imbalance contribution. By feeding baseband signals of I-path and Q-path with two in-phase signals and two reverse-phase signals, the error message would appear in the form of magnitude as indicated in Eq.(3-9) and Eq.(3-10).

$$\begin{aligned} RF_{IQ=(A,A)} &= \cos\omega_{IF}t\cdot\cos(\omega_{LO}t+\theta)+\cos\omega_{IF}t\cdot\sin\omega_{LO}t \\ &= 1/\sqrt{2}\cdot\sqrt{1-\sin\theta}\cdot\cos\left[(\omega_{LO}-\omega_{IF})t+\tan^{-1}(1-\sin\theta)/\cos\theta\right] \\ &\quad +1/\sqrt{2}\cdot\sqrt{1-\sin\theta}\cdot\cos\left[(\omega_{LO}+\omega_{IF})t+\tan^{-1}(1-\sin\theta)/\cos\theta\right] \end{aligned} \tag{3-9}$$

$$\begin{aligned} RF_{IQ=(A,-A)} &= \cos\omega_{IF}t\cdot\cos(\omega_{LO}t+\theta)-\cos\omega_{IF}t\cdot\sin\omega_{LO}t \\ &= 1/\sqrt{2}\cdot\sqrt{1+\sin\theta}\cdot\cos\left[(\omega_{LO}-\omega_{IF})t-\tan^{-1}(1+\sin\theta)/\cos\theta\right] \\ &\quad +1/\sqrt{2}\cdot\sqrt{1+\sin\theta}\cdot\cos\left[(\omega_{LO}+\omega_{IF})t-\tan^{-1}(1+\sin\theta)/\cos\theta\right] \end{aligned} \tag{3-10}$$

The phase error appears as (1-sinθ) and (–(1+sinθ)) and affect their magnitude. S/H and comparator could be used for detecting the two different output signals and distinguishing which one is larger. First, the output power is detected by PD and held by S/H with in-phase baseband signals of (A, A). Second, the output power is detected by PD with reverse-phase baseband signals of (A, -A). Since the previous state of PD output is held in S/H, the comparator can be used for deciding which one is larger. If the case of in-phase baseband signals of (A, A) is with larger/ smaller power, the phase of I-path needs to be increased/ decreased by IDACs of LO I-buffer. When compensating the phase in the direct aspect, the power difference between these two vectors would be decreased. Repeat these steps until the comparator switches the polarity. This means it has found the optimal compensating current for minimizing phase imbalance in previous state and phase imbalance is enlarged by undesired

compensating current in the current state. However, another advantage of the method by using the test vectors is the information of phase error could indirectly be calculated by (3-11) and (3-12) when circuit measurement. The completed algorithm is shown in Fig.3.25.

$$P_{(A,A)} \mid dBm - P_{(A,-A)} \mid dBm = \Delta P = 10\log(\frac{1-\sin\theta}{1+\sin\theta}) \tag{3-11}$$

$$\theta = \sin^{-1}\frac{1-10^{\frac{\Delta P}{10}}}{1+10^{\frac{\Delta P}{10}}} \tag{3-12}$$

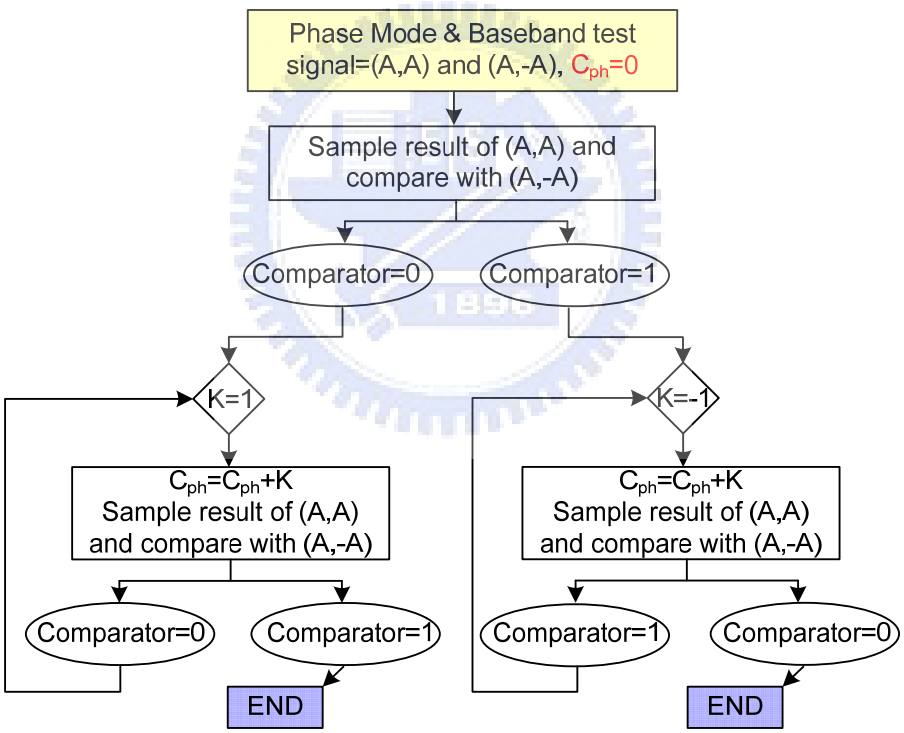

Fig. 3.25 Algorithm for I/Q phase imbalance compensation

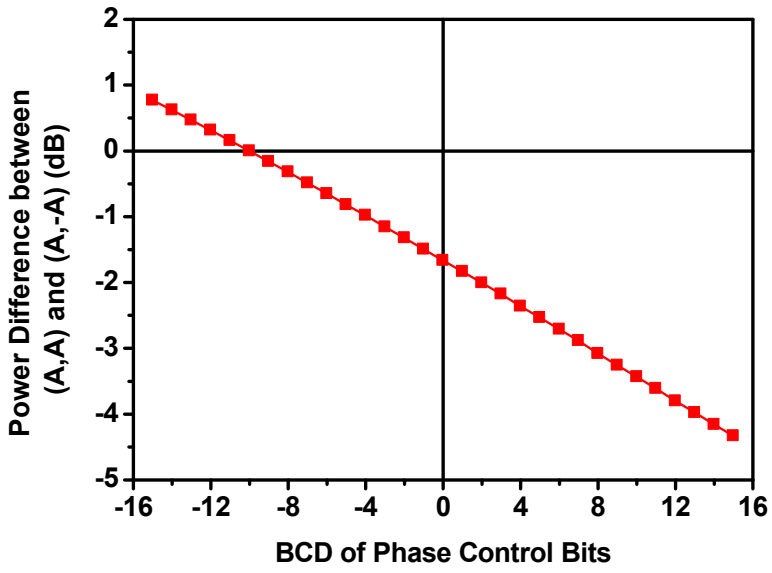

Fig. 3.26 The post simulation result of I/Q mixer by using I/Q phase imbalance compensation algorithm

The post-simulation result is shown in Fig.3.26. The initial power different due to phase imbalance is -1.7dB and the case of in-phase baseband signals of (A, A) is with smaller power. So, the bit number of the IDAC of LO I-buffer is decreased. With bit number of -10, the minimum phase difference can be obtained. From Eq.(3-12), the initial phase error can be obtained as 11°. Since each bit of phase compensation can adjust the phase with 1°, the compensating phase of the post-simulation is 10°. So, the Eq.(3-12) is pretty correct.

3.3.3 Algorithm for I/Q Gain Imbalance Compensation

In gain imbalance calibration, baseband test signals are needed. Since I/Q gain imbalance is wanted to detect, the baseband signals of I/Q path could be respectively fed with another path shutting down. Since I-path is used for magnitude reference, S/H and comparator can be used for distinguishing which path of I or Q is with larger

magnitude. First, the magnitude of I-path is detected by PD and sampled and held by S/H. Second, the magnitude of Q-path is detected by PD. Since the previous state of PD output is held in S/H, the comparator can be used for deciding which one is larger. Third, if the magnitude of Q-path is smaller or larger, the bit number of IDACs of LO Q-buffer is increased or decreased to get larger or smaller magnitude. Then, repeat these steps until the comparator switching the polarity. This means it has found the optimal compensating current for minimizing magnitude difference in previous state and in the current state magnitude difference is enlarged by undesired compensating current. The completed algorithm is shown in Fig.3.27.

The post-simulation result is shown in Fig.3.28. The initial magnitude different is 1dB and the Q-path is with smaller magnitude. So, the bit number of IDACs of LO Q-buffer is increased. With bit number of 11, the minimum magnitude difference can be obtained.

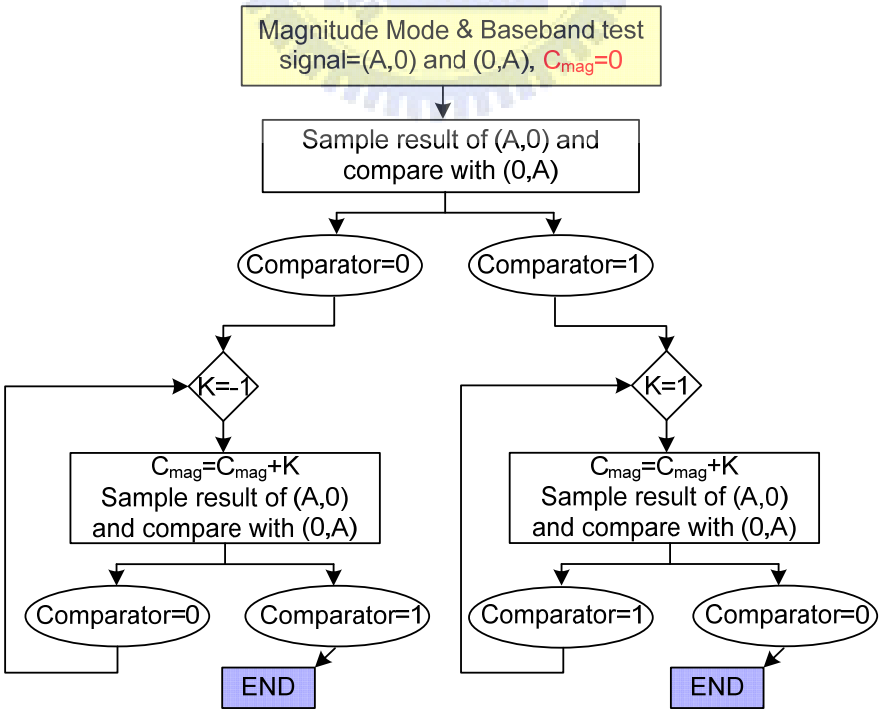

Fig. 3.27 Algorithm for I/Q gain imbalance compensation

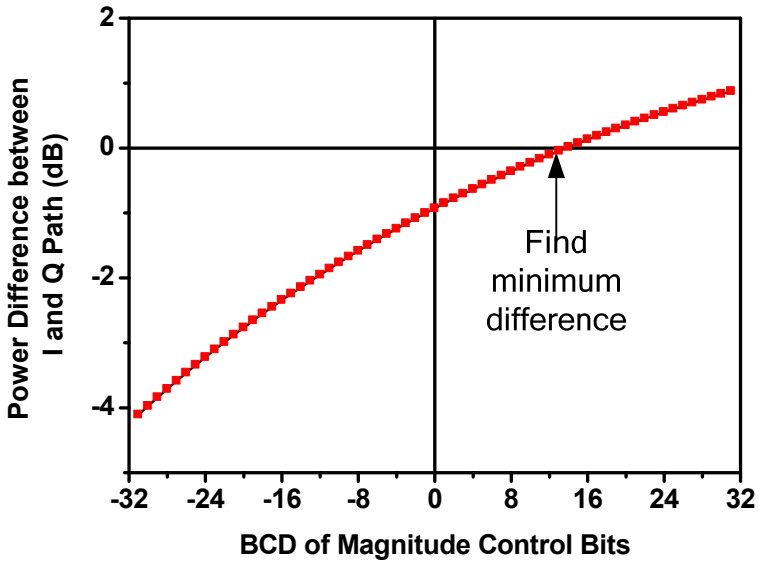

Fig. 3.28 The post simulation result of I/Q mixer by using I/Q magnitude imbalance compensation algorithm

3.3.4 Post Simulation Result with Compensation Algorithm

Due to routing difference and mismatch, the LO feedthrough can be suppressed as 32.61dB and the unwanted sideband can be suppressed as 20dB relating to signal power as Figure.3.29 shown.

After finishing the compensation algorithm above, the LO feedthrough can be suppressed as 59dB and the unwanted sideband can be suppressed as 43.54dB relating to signal power as Figure.3.30 shown. The EVM could be calculated as 0.67% by Eq. (2-31).

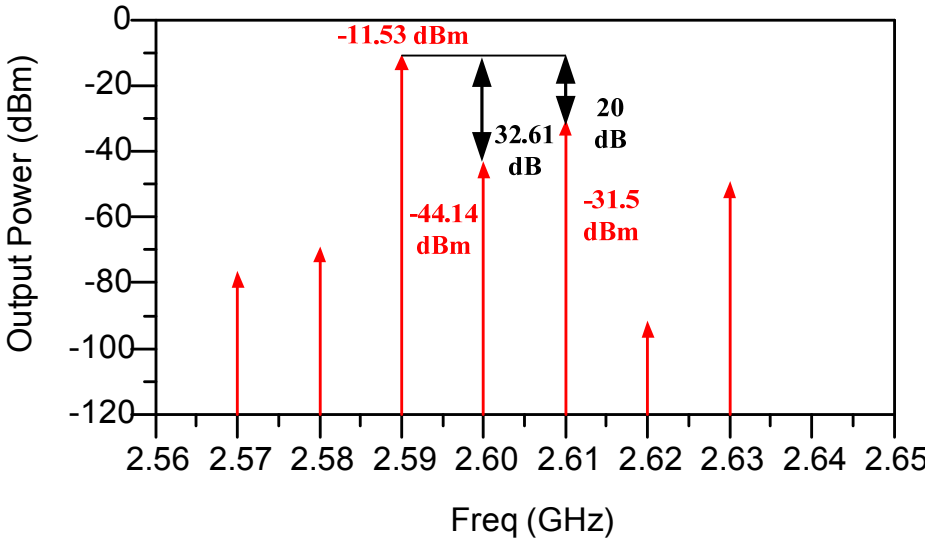

Fig. 3.29 The simulated spectrum by post simulation without compensating

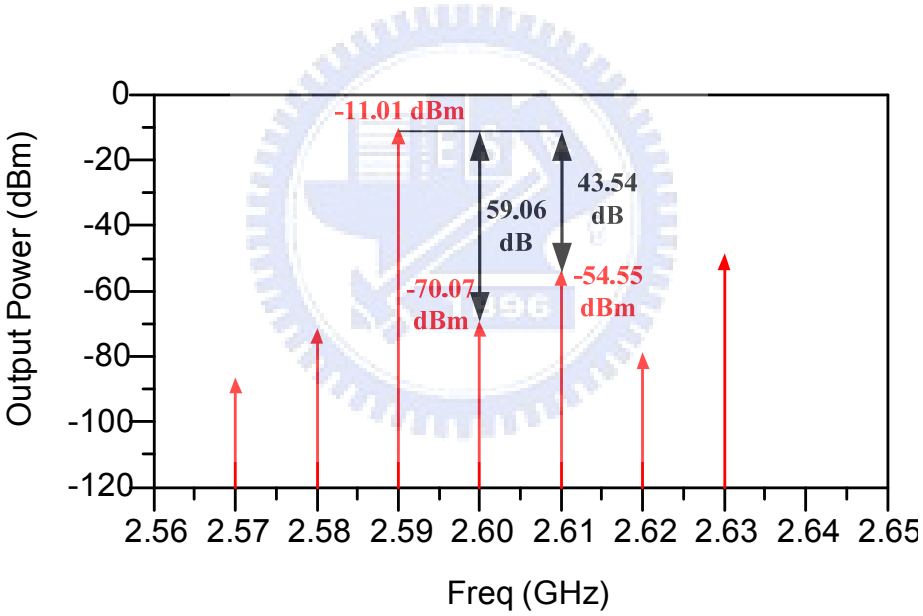

Fig. 3.30 The simulated spectrum by post simulation after compensating

3.4 Summary

Since double balanced mixers are with perfect LO cancellation, some factors of device mismatch, DC current offset, and imbalance LO can degrade LO cancellation and induce LO feedthrough. The main factor is the DC current offset due to the transconductance stages device mismatch and the DC offset from baseband signals. By using two sets of IDACs in the I/Q mixer, the DC current offset can be compensated. The LO feedthrough can be suppressed below -45dB relating to desired signal power after compensation.

A simple I/Q imbalance model has been translated in Fig.3.8. We can adjust the phase of LO I-path and the magnitude of LO Q-path to achieve I/Q matching. Since the digital control is used, the resolution of tuning phase and magnitude for I-buffer and Q-buffer needs to be proper defined. In this work, after choosing proper resolutions, the sideband signals can be suppressed below -40dB relating desired signal power.

The direct up-conversion I/Q mixer, LO buffers, and the two IDACs in the I/Q mixer form an open loop for compensation. An algorithm is needed to achieve a feedback loop by additional pre-amplifier, power detector, sample-and-hold, and comparator for auto-compensation. The algorithm is developed in this work without feedback loop implement, and is verified by co-work with post simulation.

The performance summary is shown in Table IV.

TABLE IV Performance summary of simulation results

	Performance
Technology	TSMC CMOS 0.18um
DC Supply Voltage	1.8 V
LO power	4 dBm
Voltage Conversion Gain	-7 dB
P_{-1dB}	-6 dBm
IIP3	10 dBm
Error Magnitude Tunable Region	0.8～1.2 (per Step 0.07)
Error Phase Tunable Region	-15°~15°(per Step 1°)
Sideband Suppression	>40dBc
LO Feedthrough Suppression	>50dBc
Power Consumption (mW)	33.7mW+ 10.3mW(RF Buffer)

CHAPTER 4 Circuit Implement and Measurement

4.1 Circuit Implement

The I/Q up-conversion mixer is fabricated with TSMC 0.18um technology. The die micrograph of the I/Q up-conversion mixer is shown in Fig 4.1. This circuit contains a polyphase filter, I/Q mixer, LO buffers, and 3-wire for feeding control signals. Besides, the ESD I/O pads are placed before the 3-wire inputs which are VDD, GND, Din, CLK, Clear, and Enable.

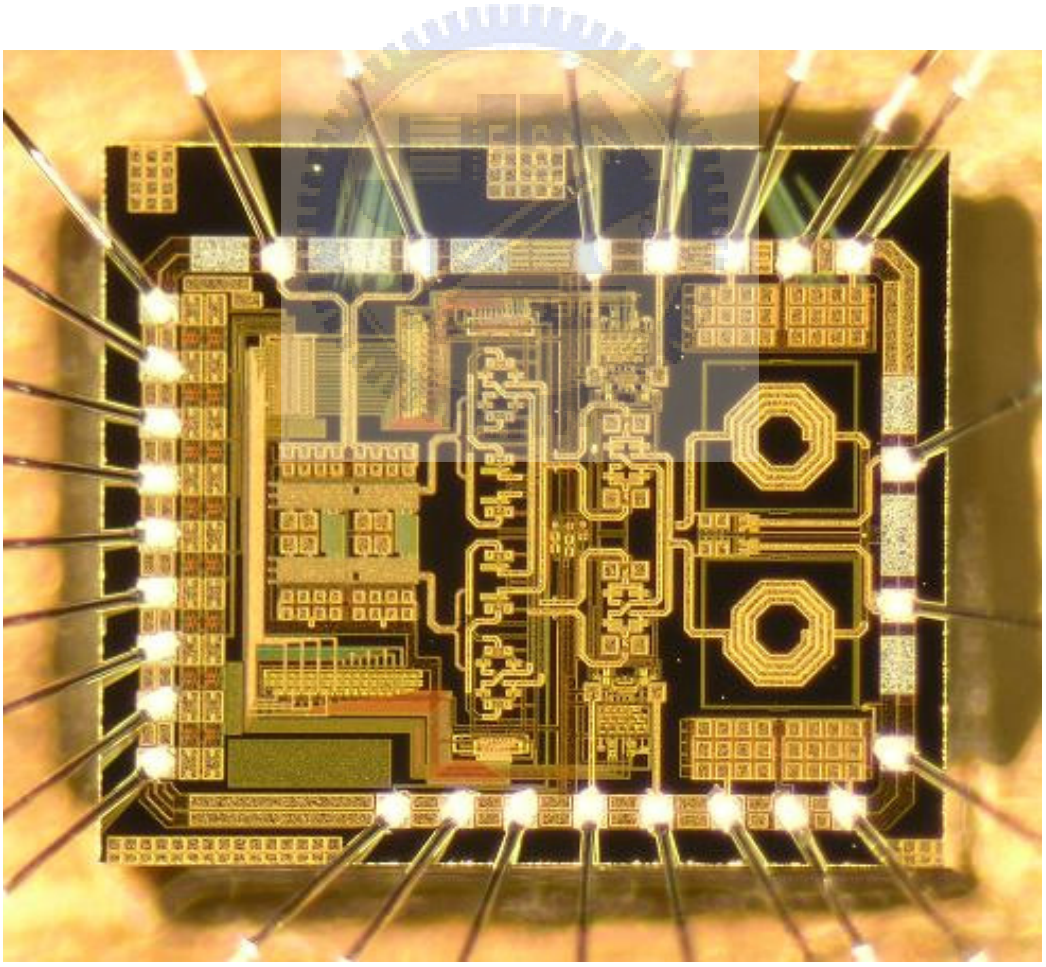

Fig 4.1 Die micrograph

4.2 Circuit Measurement

The measurement setup is shown in Fig. 4.2. All the pads in the chip are connected to PCB by bond-wire. The input signals of 3-wire is fed by Labview and the printer port (parallel port) in PC. Since differential topology is used in this circuit, the signals of LO and IF need on-board baluns to be translated into differential signals. The RF outputs also need an on-board balun to be translated into single-end signals. Finally, the spectrum analyzer is used to measure the power of wanted signal, LO feedthrough, and unwanted sideband.

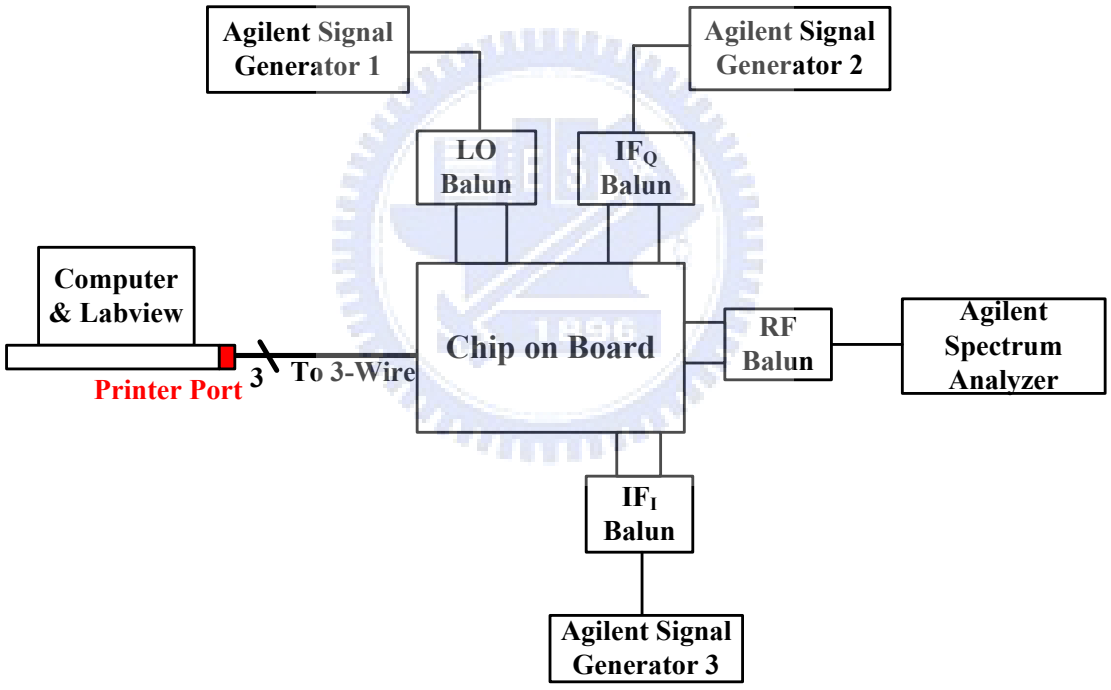

Fig. 4.2 Measurement setup.

For the sake of placing few vias or contacts between the two metal layers or the diffusion and the metal 1 layer as Fig.4.3 shown, the resistance between them becomes too large, so that the 3-wire circuit is latched-up. When VDD of the 3-wire is fed with 1.8V, large DC current of 43mA occurs and the function of the 3-wire fails.

Hence the control signals can't be fed the I/Q up-conversion mixer. However, the performance of I/Q mixer without any compensation could just be measured.

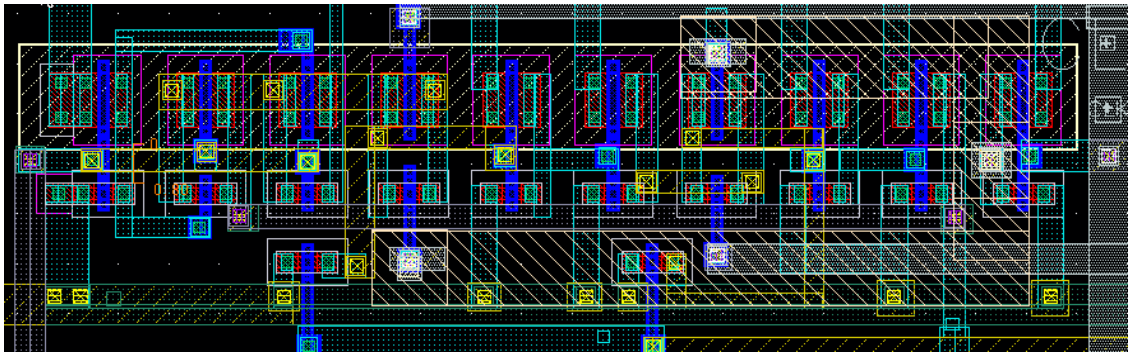

Fig. 4.3 Layout view of D-type flip flop cell

The measurement results of the conversion gain, unwanted sideband suppression, LO feedthrough suppression varying with input power level and LO frequency 2.4GHz to 2.7GHz are shown in Fig.4.4, Fig.4.5, and Fig.4.6. The P_{-1dB} can be identified from Fig.4.4, and is 5dBm. The conversion gain measured degrades much than the simulation results. After the on-board baluns characteristics have been measured by 4-port measurement and saved as touchstone file, they can be put together with circuit simulation. From simulation results, the conversion gain degraded by on-board baluns could be identified. In Fig. 4.7, the result of the circuit simulation with measured on-board baluns degrades the conversion gain with 15.5dB than the one with ideal baluns. We modify the measured conversion gain with adding the on-board baluns loss of 15.5dB and get Fig. 4.8 at 2.6GHz. After all, the conversion gain is higher than -11.15dB with LO frequency from 2.4GHz to 2.7GHz. The conversion gain versus LO Frequency is shown in Fig. 4.9. The resonant frequency of mixer output LC tank is shifted relating to original design with resonant frequency of 2.5GHz.

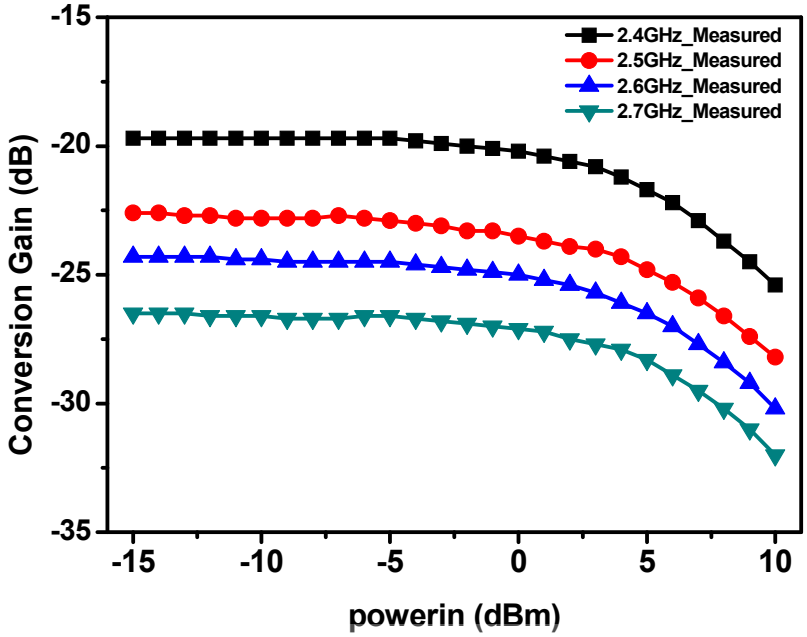

Fig. 4.4 Conversion gain varying with input power level and LO frequency

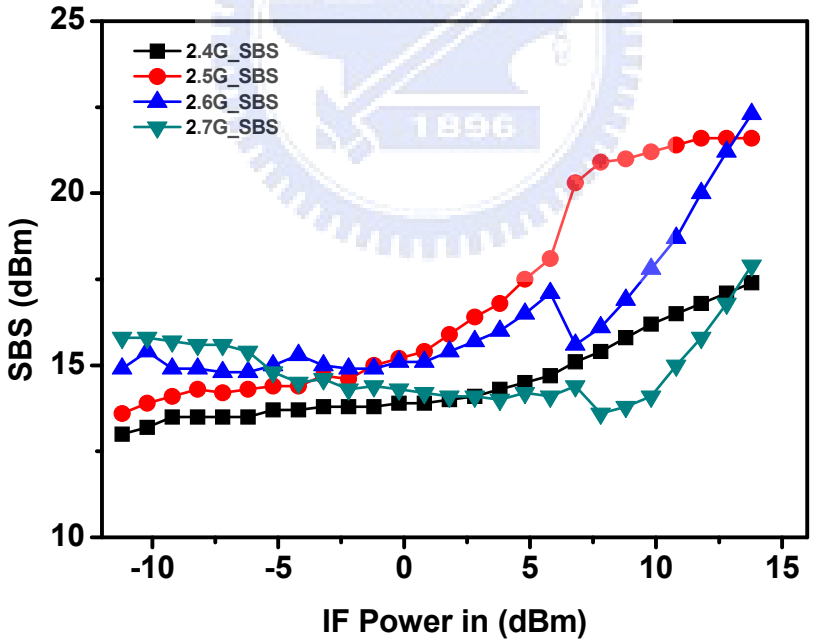

Fig. 4.5 Sideband suppression varying with input power level and LO frequency

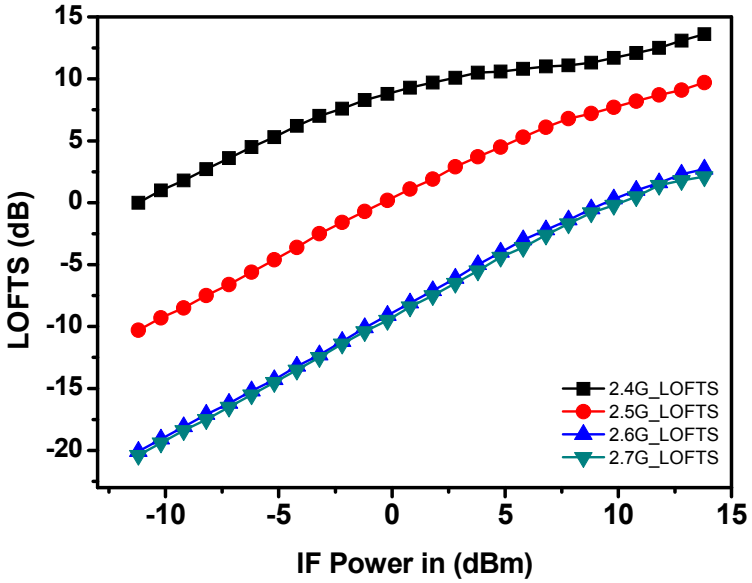

Fig. 4.6 LO feedthrough suppression varying with input power level and LO frequency

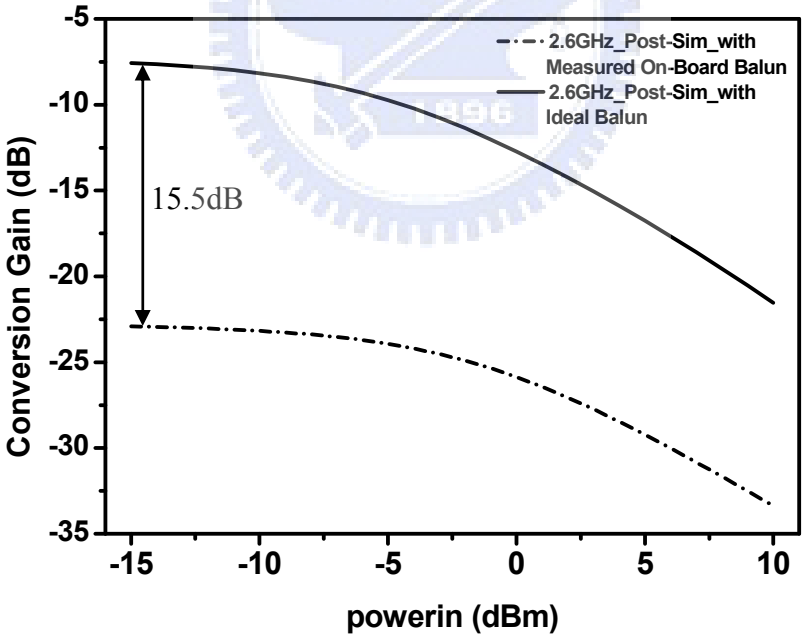

Fig. 4.7 On-board baluns loss check by simulation

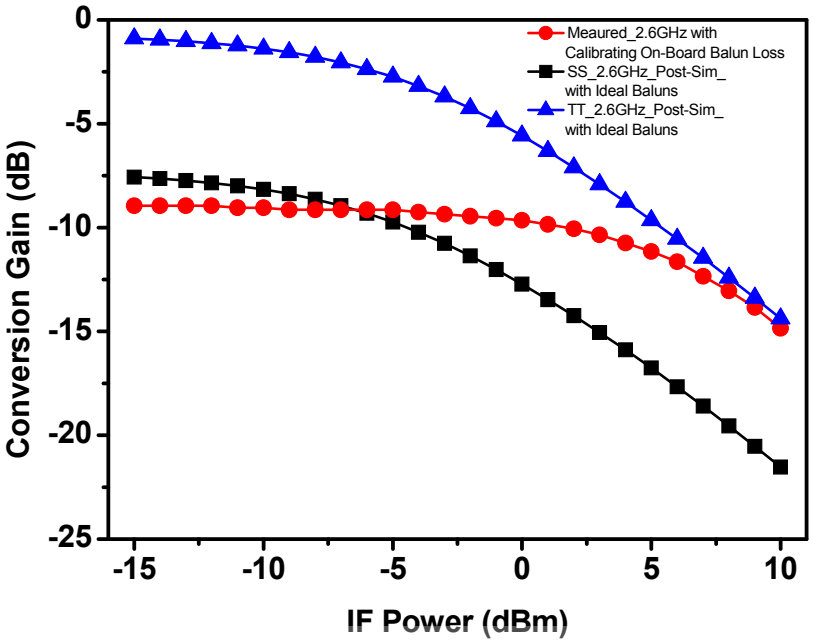

Fig. 4.8 Conversion gain varying with input power level and LO frequency after calibrating baluns loss

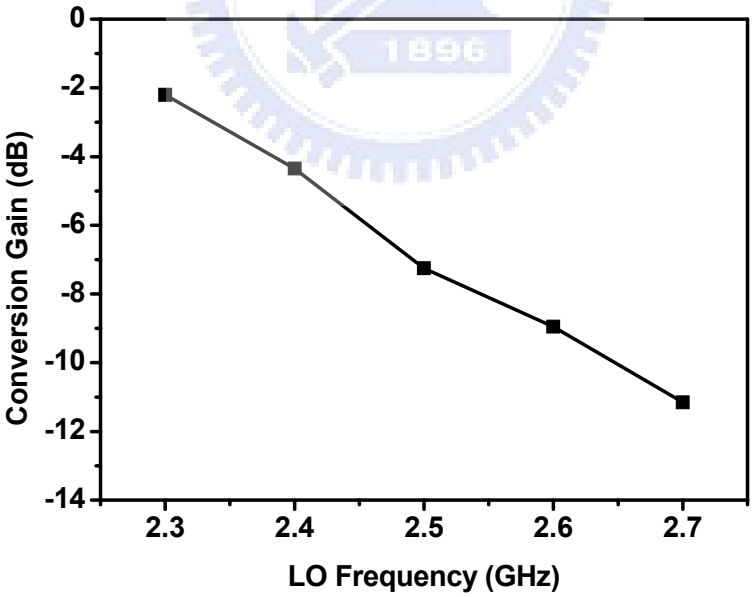

Fig. 4.9 Conversion gain versus LO frequency

The LO I/Q signals is generated by a two-stage polyphase filter, so we can verify the design by tuning the phase and magnitude of LO signals. An equivalent model can be used for verifying our design as Fig.4.10 shown. We can adjust the phase and the magnitude of baseband I/Q signal to verify our design.

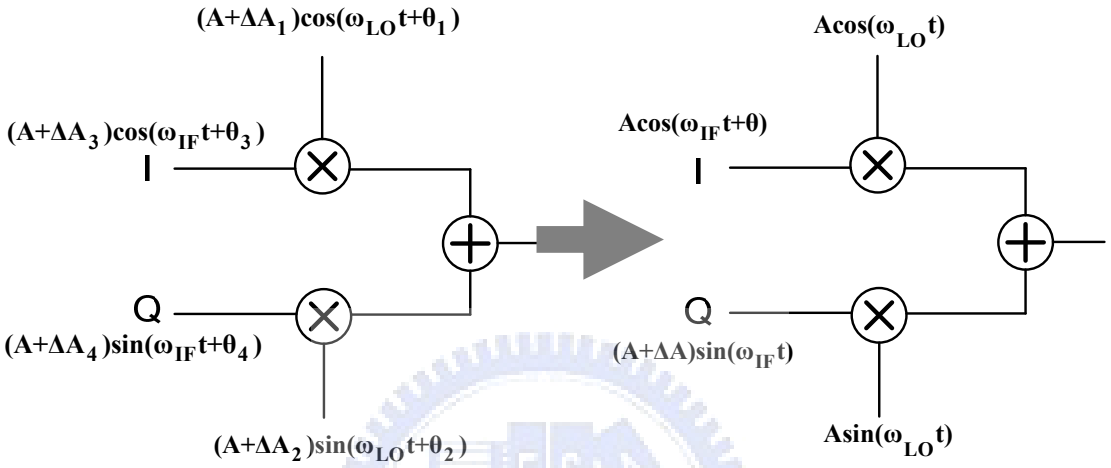

Fig. 4.10 I/Q imbalance equivalent model II

Use another die for measurement. After adjust the phase between the baseband I/Q signals to compensate the phase imbalance, the sideband suppression can achieve 14.3dB and the LO feedthrough suppression can achieve 40dB as Fig.4.11 shown. The magnitude compensation works after the phase compensation. With the algorithm mentioned in session 3.5.3, the spectrum of only I-path or Q-path baseband signals fed is shown in Fig.4.12 and Fig 4.13. The power difference between I-path and Q-path is 3.4dB. After enlarging the power of I-path with 3.4dB, the sideband suppression can achieve 38.5dB as Fig. 4.14. From Eq.(2-31), the EVM is 1.77% and meet the specification. If the 3-wire is on working, we ensure that a pretty good performance could be measured.

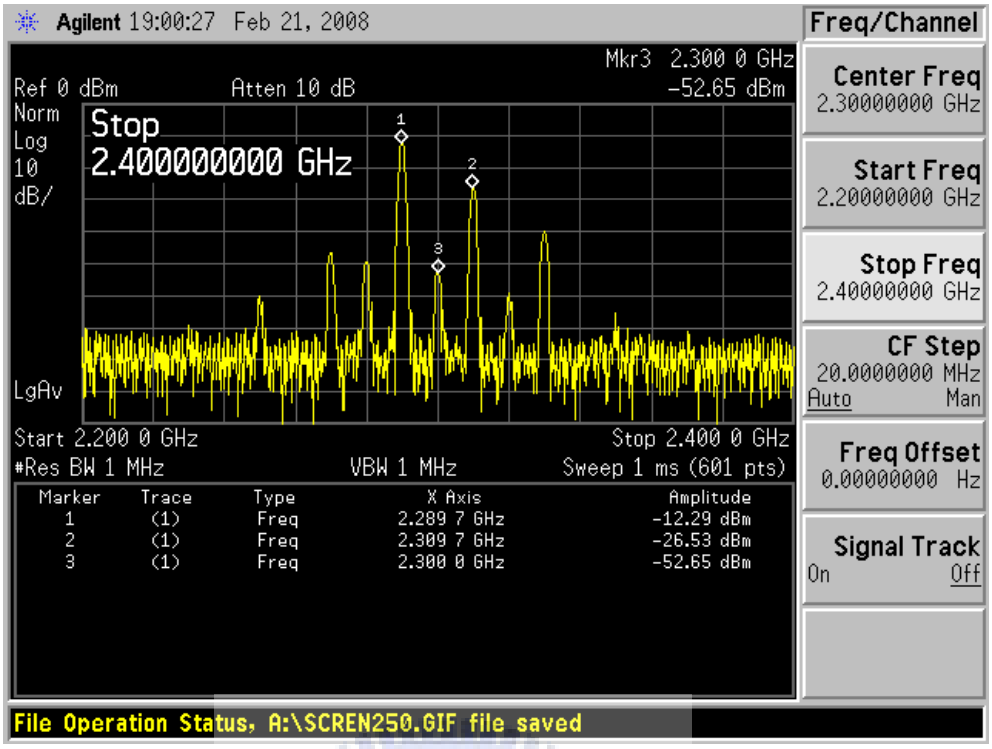

Fig. 4.11 Spectrum measured after phase compensation

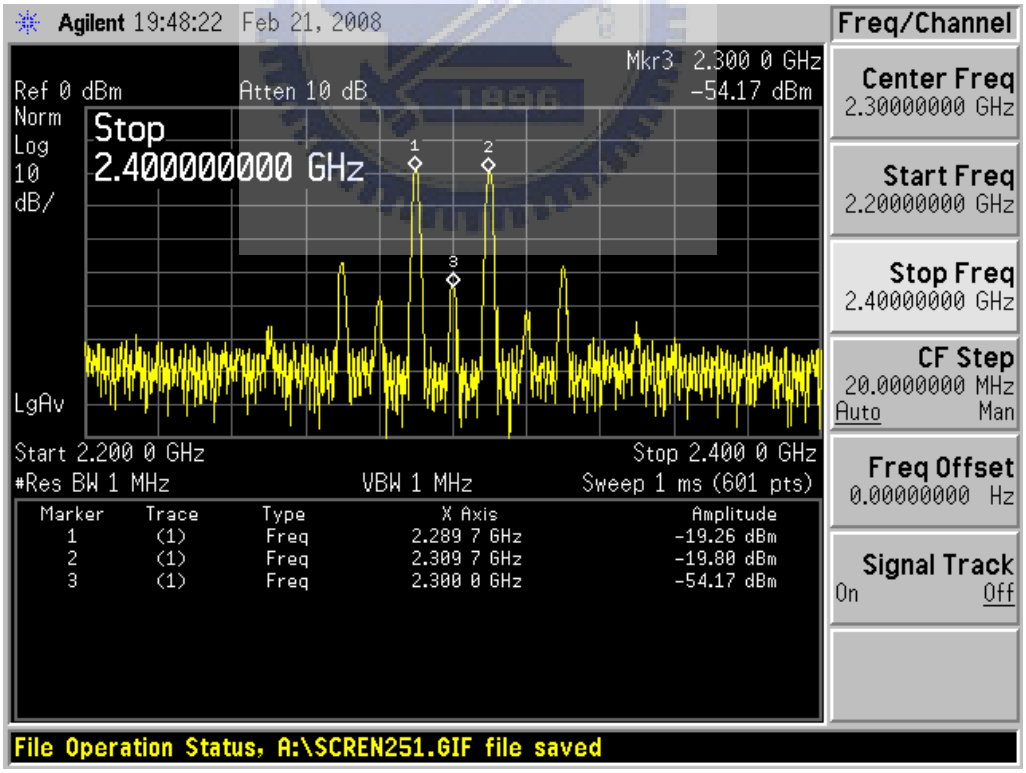

Fig. 4.12 Spectrum measured with baseband signal I-path turning on

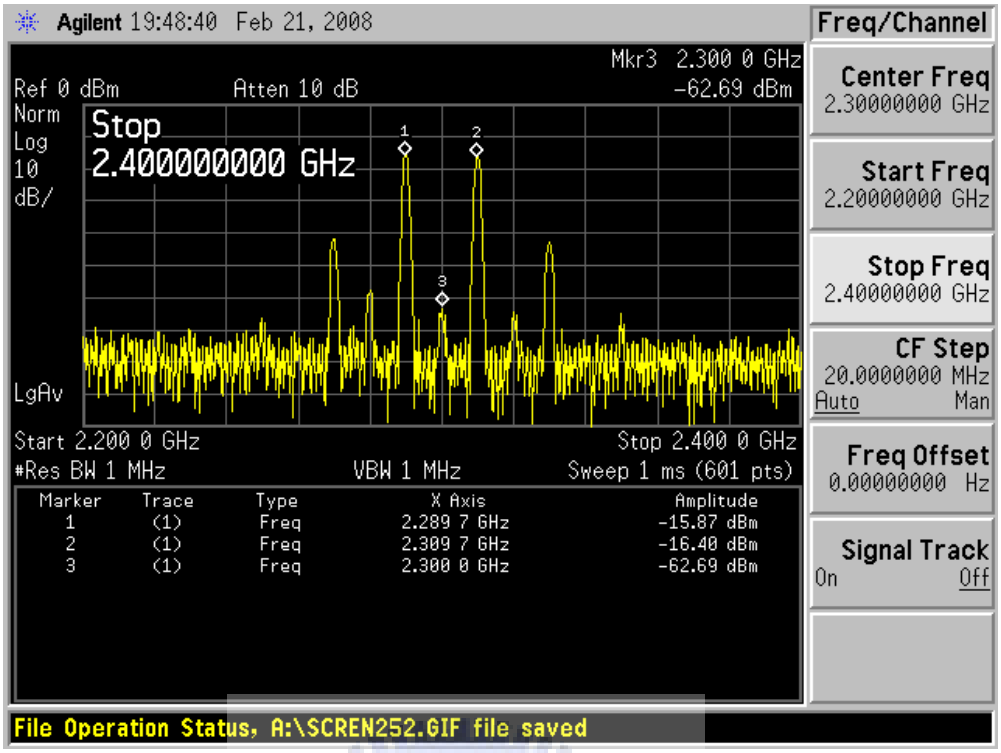

Fig. 4.13 Spectrum measured with baseband signal with Q-path turning on

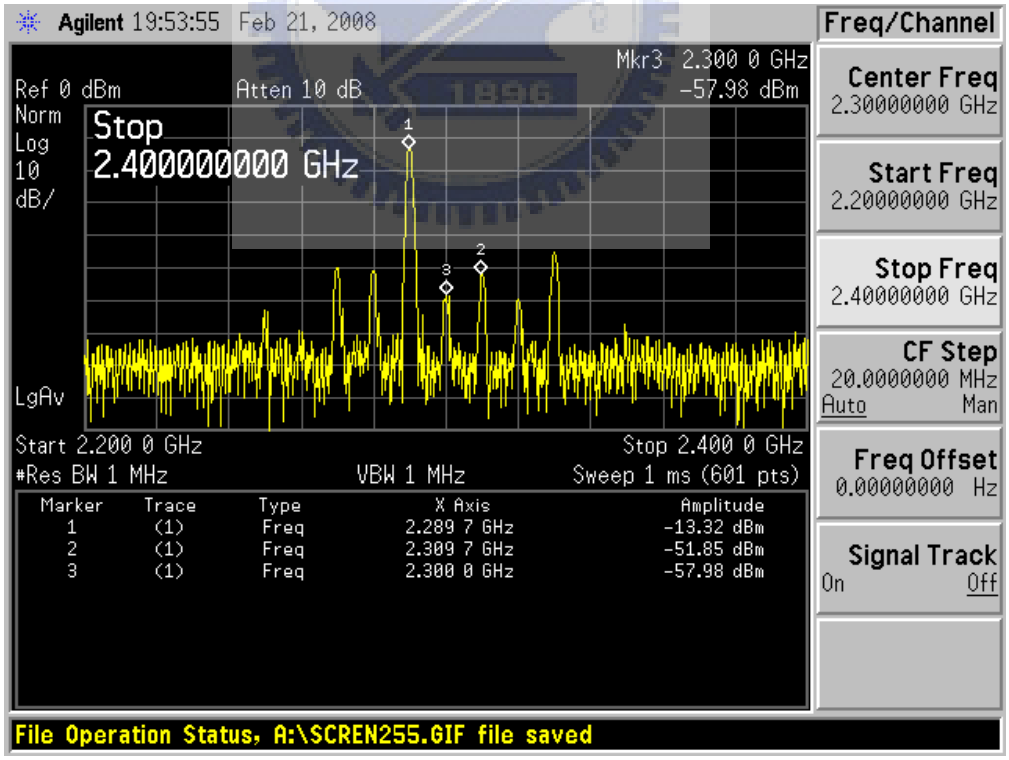

Fig. 4.14 Spectrum after the phase and magnitude compensation

4.3 Summary

The I/Q up-conversion mixer is fabricated with TSMC 0.18um technology composed of a polyphase filter, I/Q mixer, LO buffers, and 3-wire for feeding control signals. The ESD I/O pads are placed before the 3-wire inputs which are VDD, GND, Din, CLK, Clear, and Enable.

The 3-wire circuit is latched-up during measurement. Then the performance of up-conversion I/Q mixer can be measured without any compensation. The conversion gain, P_{-1dB}, sideband suppression, and LO feedthrough suppression are measured as maximum values -11.15dB, 5dBm, 15dB, and 8dB, as Table V shown.

TABLE V Performance summary of simulation results

	2.4GHz	2.5GHz	2.6GHz	2.7GHz
P_{-1dB} (dBm)	5	5	5	5
Conversion Gain (dB)	-4.35	-7.25	-8.95	-11.15
LOFTS (dB) *	8	0	-10	-10
Sideband Suppression (dB)	>15	>15	>15	>15
Power Consumption (mW)	50.4 mW			

* IF power of 0dBm

Use another equivalent model of I/Q imbalance as Fig.4.6 shown. The manual I/Q imbalance compensation can be achieved by adjusting the magnitude and phase of baseband I/Q signals. After manual compensation, the LO feedthrough suppression

and sideband suppression can be achieved as 44.6dB and 38.5dB. After calculation, the equivalent EVM is 1.77%. After manual compensation, the performance measured in this work is compared with other I/Q compensation circuits as Table VI shown.

TABLE VI Performance comparison to other circuits

	This Work	[9]	[7]	[10]	[11]
Sideband Suppression (dB)	38.5	48	-	-	49.6
LO Feedthrough Suppression (dB)	40	30	-	-	45.3
EVM	1.77%	3.19% *	2.24%	3.2%	0.636% *
Power Consumption (mW)	50.4 (Including RF Buffer)	16mA	302 (TX)	324 (TX)	-

*Calculated by Eq. (2-31)

CHAPTER 5 Conclusion and Future Work

5.1 Conclusion

In this work a direct up-conversion I/Q mixer is designed with matching compensation eliminating I/Q imbalance and LO feedthrough for WiMAX and WiFi transmitter. LO buffers are employed in front of I/Q mixer to compensate the I/Q imbalance of this transmitter chain. Two IDACs are employed in the I/Q mixer to compensate the DC current offset and eliminate the LO feedthrough.

Since digital control is used, the resolutions of I/Q imbalance compensation and the compensating IDACs needs to identified to meet the system specification. After choosing proper resolutions, the unwanted sideband signal due to the I/Q imbalance and the LO feedthrough signal can be suppressed at least 40dB and 45dB, respectively.

The direct up-conversion I/Q mixer, LO buffers, and the two IDACs in the I/Q mixer form an open loop for compensation. An algorithm is needed to achieve a feedback loop for auto-compensation. The algorithm is developed in this work, and is verified by co-work with post simulation.

From measurement results, the 3-wire circuit is latched-up. Hence the control signals can't be fed the I/Q up-conversion mixer. The manual I/Q imbalance compensation can achieve by adjusting the magnitude and phase of baseband I/Q signals to get sideband suppression of 38.5dB. This could be used to verify the compensation method we proposed.

5.2 Future Work

The 3-wire needs to be redesigned to avoid the latch-up. Furthermore, we can use cell-based models and synthesis tools to generate automatically the 3-wire.

A feedback loop composed of a power detector, a sample-and-hold circuit, and a comparator needs to be designed for auto-compensation. Since the power of LO feedthrough is tiny for power detector, we need to insert a pre-amplifier in front of the power detector during LO feedthrough compensation. The circuit architecture is shown in Fig.5.1.

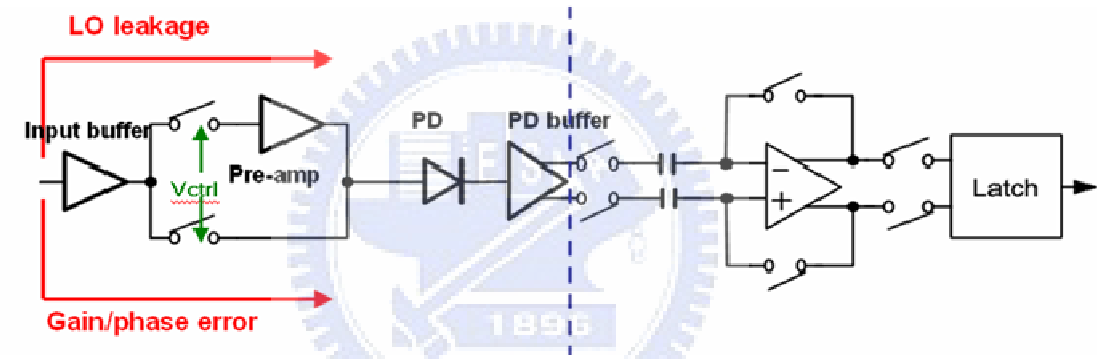

Fig. 5.1 The feedback loop for auto-compensation

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