金氧半場效電晶體導通電流增強之方法與相關可靠性問題之研究

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摘要

在本論文中，我們針對覆蓋氮化矽對於元件特性與可靠性影響作一系列之研究，此外，我們也探索先進的 SOI 元件結構的可行性。主要涵蓋的內容包括有複晶矽鍺閘極元件製作與分析；具有複晶矽鍺閘極與電漿化學氣相沈積氮化矽之 p 型金氧半場效電晶體元件之研製，及其驅動電流及負偏壓不穩定效應探討；利用低壓化學氣相沈積氮化矽覆蓋層之 n 型金氧半場效電晶體之製作與分析；由局部應力造成的能階窄化效應與熱載子測試後之界面缺陷橫向擴散等現象，在本論文中均有詳細之分析。最後，我們也製作應用雜質分離技術之蕭特基 FinFET 元件，與具有省略化學機械研磨和後閘極製作技術之超薄 SOI 元件。

我們的結果驗證使用複晶矽鍺閘極能夠同時減緩閘極空乏與硼穿透等問題，這主要是因為對 p 型半導體而言，雜質在矽鍺中會有較高的活化率，因此可增加驅動電流將近 5.8%。而在負偏壓不穩定效應分析中，具有複晶矽鍺閘極元件則較傳統複晶矽閘極元件有較長之生命期，因此，具有複晶矽鍺閘極之 p 型金氧半場效電晶體將更適用於奈米級元件的製作。

使用電漿化學氣相沈積氮化矽覆蓋層造成元件通道局部壓縮應力，與複晶矽鍺閘極之 p 型金氧半場效電晶體在本論文中被成功製作出來，其驅動電流因為加入具有壓縮應力之氮化矽層而得到明顯提升。事實上，對於通道長度為 0.45 微米元件，分別沈積氮化矽 100 奈米與 300 奈米厚度，驅動電流可提升將近 29%與 36%之多。儘管有此優勢，實驗結果顯示覆蓋氮化矽層也會造成負偏壓不穩定效應的劣化；在電漿化學沈積氮化矽過程中的氫元素，以及氮化矽所造成的通道壓縮應力，都是惡化可靠性之疑兇。因此，嘗試調整與最佳化在氮化矽沈積過程中氫元素的含量，並同時保有元件通道壓縮應力，是改善負偏壓不穩定效應的方法之一。此外，在負偏壓不穩定效應中，臨界電壓的偏移與界面缺陷的增加會隨著測試時間的增加，而表現出飽和現象；這主要是因為隨著測試時間的增加，界面矽氫鍵幾乎已被完全破壞所致。

接下來，此具有電漿輔助化學氣相沈積氮化矽之 p 型金氧半場效電晶體，同時亦作動態負偏壓溫度不穩定效應與交流可靠性分析。結果顯示覆蓋氮化矽之元

件具有較大的臨界電壓與界面缺陷的回復現象，而中性的氫元素是回復過程中的主要角色。然而，實驗結果亦發現，覆蓋氮化矽之元件臨界電壓的偏移，與交流訊號之頻率是息息相關，且本論文同時得到一重要之結論，即具有氮化矽層覆蓋之元件雖然會劣化負偏壓不穩定效應，但是當元件操作頻率增加，此劣化現象將會得到良好的改善。

在本論文中，我們同時也研究低壓化學氣相沈積氮化矽過程本身，以及氮化矽層伸張應力對 n 型金氧半場效電晶體之特性影響。對通道長度為 0.4 微米的元件，在低壓化學氣相沈積氮化矽厚度為 300 奈米時，可造成將近 20%導通電流的增加，且通道伸張應力造成能階窄化現象，隨著通道長度的減小，將造成臨界電壓變小。實驗結果指出，在沈積氮化矽過程中額外的熱預算，會減輕元件反向短通道效應的產生，但是這額外的熱預算，同時也是造成閘極雜質外擴散與閘極氧化層厚度增加的元凶；經由 F-N 穿透電流的計算，閘極氧化層將從對照組的 2.705 奈米，增加至氮化矽沈積 300 奈米時的 2.85 奈米厚度。此外，界面缺陷的密度亦受到氮化矽沈積過程的影響，當增加氮化矽的沈積時間，相對的將有更多的氫元素參與界面缺陷的填補。

其次，氮化矽的沈積與沈積過程本身，兩者對於元件操作與相關可靠性都有重大的影響。事實上，具有低壓化學氣相沈積氮化矽之元件，因為能階窄化與載子遷移率的增加，將會惡化熱載子效應。然而，我們亦需將注意力集中在氮化矽沈積過程本身，因為沈積氮化矽製程使用含氫元素的反應氣體源，大量的氫元素將累積在閘極氧化層，而造成熱載子效應的劣化；另外，熱載子效應本身的局部現象，也是惡化可靠性的因素之一。此外，因為閘極氧化層的變動與能階窄化現象，使得具有氮化矽沈積之元件的熱載子劣化現象，與氮化矽層沈積厚度並不相關。

最後，我們將展示具有白金金屬矽化物與雜質分離技術的蕭特基 FinFET 元件，藉由雜質分離技術可有效改善蕭特基能障，而得到較佳之元件特性，並且不必經由電場引致汲極(FID)結構來降低漏電流，其導通電流甚至可比利用 FID 技術之蕭特基元件多達五倍之多。此外，我們同時成功的製作出一新型，同時可省略化學機械研磨動作，且具有提升矽鍺源/汲極的超薄 SOI p 型金氧半場效電晶體，因為其後閘極的製程方法，使得其有潛力應用於未來結合高介電常數的閘極介電層與金屬閘極中的元件製作。

關鍵字：氮化矽沈積，壓縮應力，負偏壓溫度不穩定效應，動態負偏壓溫度不穩定效應，伸張應力，熱載子效應，蕭特基能障

A Study of Drive Current Enhancement Methods and Related Reliability Issues for MOSFETs

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Abstract

In this thesis, we have investigated the impacts of silicon nitride (SiN) capping layer on drive current and the associated reliability issues. In addition, novel SOI devices were also fabricated and characterized in this study. This study includes the fabrication and characterization of devices with poly-SiGe gate electrode. Attentions were paid on the drive current and NBTI degradation of PMOSFETs with poly-SiGe gate and PE-SiN capping layer. Moreover, NMOSFETs with LP-SiN capping were also fabricated and investigated. Bandgap narrowing effect induced by local strain and lateral diffusion of interface states after hot-carrier stress were addressed. Finally, novel Schottky-barrier (SB) FinFET with impurity segregation and UTB SOI devices with CMP-free and gate-last process were fabricated and characterized.

Devices with poly-SiGe gate electrodes can help alleviate poly-depletion and boron penetration problems due to higher dopant activation in p-type semiconductor. These result in about 5.8% enhancement of saturation current as compared with the poly-Si-gated counterparts. During NBTI stress, devices with poly-SiGe gate even have longer lifetime than those with conventional poly-Si gate.

Next, poly-SiGe-gated PMOSFETs with local compressive strain in the channel induced by a compressive PECVD SiN capping layer were fabricated in this study. The drive current of PMOSFETs is found to be significantly enhanced by the incorporation of the compressive PE-SiN capping layer. Specifically, the drive current enhancement can reach about 29% and 36% for devices with PE-SiN capping thickness of 100 nm and 300 nm, respectively, at a channel length of 0.45 μm. Despite this much-coveted merit, our results also show that the PE-SiN capping may aggravate the NBTI characteristics. The abundant hydrogen species contained in the PE-SiN layer as well as

the strain energy stored in the channel may be the culprits for the worsened reliability. Cares should therefore be exercised to optimize the amount of hydrogen species to ensure that the NBTI effect is kept at bay, while simultaneously maintaining the performance enhancement pertaining to the compressive strain channel. In addition, the saturation phenomena in ΔV_{th} and ΔN_{it} are also observed during NBTI stress. This is believed to be due to the fact that nearly all the interfacial Si-H bonds have been broken.

DNBTI and AC stressing were also performed on PMOSFETs with PE-SiN capping layer. The results show that devices with SiN capping have larger recovery of ΔV_{th} and ΔN_{it} than those without capping. The neutral hydrogen species are mainly responsible for the recovery phenomena of the generated interface states in the SiN-capped devices. However, a strong dependence on the AC stress frequency is also observed for the SiN-capped devices. Our observation reveals an important message that the aggravated NBTI in the SiN-capped devices could be largely alleviated by high frequency operation.

In this study, we have also investigated the effects of LPCVD SiN capping process and the resultant channel strain induced by the SiN-capping layer on the device characteristics. Enhancement ratio up to 20% is achieved for devices with LP-SiN capping thickness of 300 nm at a channel length of 0.4 μm. The bandgap narrowing effect due to the channel strain may result in further lowering in V_{th} as the channel length is shortened. Our results indicate that the thermal budget associated with the deposition of the SiN capping layer could alleviate the reverse short-channel effect seen in the uncapped devices. However, it is also the main culprit for the gate dopant out-diffusion and gate oxide thickness variation. The gate oxide thickness extracted by F-N tunneling current would increase from 2.705nm for the control sample to 2.85nm for the 300nm-SiN-capped sample. In addition, interface state density is also affected by SiN capping procedure. More hydrogen species are expected to participate in interface state passivation as the duration of the LP-SiN deposition increases.

Next, both the deposited LP-SiN layer and/or the deposition process itself have significant impacts on the device operation and the associated reliability characteristics. In fact, the accompanying bandgap narrowing and the increase in carrier mobility tend to worsen the hot-electron reliability in the LP-SiN-capped devices. Nevertheless, attentions should also be paid to the SiN deposition process itself. Owing to the use of hydrogen-containing precursors, abundant hydrogen species is incorporated in the oxide that may also contribute to the hot-electron degradation. The edge effect of hot carrier stress is also a factor to cause reliability degradation in SiN-removal devices. In addition, the hot carrier degradation of devices with SiN capping is independent of SiN thickness due to gate oxide thickness variation and bandgap narrowing induced by channel strain.

Finally, we have successfully demonstrated Schottky barrier (SB) FinFETs formed

by Pt salicide and impurity segregation. By adjusting SB height through impurity segregation, excellent device performance is achieved without resorting to field-induced drain (FID) structure to reduce the leakage current. The driving current can even be five times larger than that of the SB device with FID. Moreover, we have also proposed and successfully demonstrated a new CMP-free process for fabricating UTB SOI PMOS transistors with SiGe raised source/drain and replacement gate schemes. Satisfactory device characteristics have been achieved. With its inherent gate-last feature, the new scheme lends itself handily to the advanced nano CMOS featuring high-k gate dielectric and metal electrode.

Keyword: SiN capping, compressive strain, negative bias temperature instability (NBTI), DNBTI, tensile strain, hot-electron effect, Schottky barrier (SB)

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