Chapter 1

Introduction

1.1 General Background

1.1-1 Poly-SiGe Gates

Since ULSI devices are being scaled down into the nanometer regime, the "dual-gate" process has replaced the conventional "single-gate" process for complementary metal-oxide-semiconductor (CMOS) fabrication in order to keep the short-channel effects at bay. Nevertheless, boron penetration through the gate oxide from the p^+-doped gate of PMOSFETs has emerged as a new but major concern in the dual-gate process. In addition, gate-depletion effect due to insufficient dopant activation at the gate/dielectric interface becomes more prominent as gate oxide thickness is scaled down, resulting in the degradation of the drive current [1,2]. To alleviate the above-mentioned problems, poly-SiGe has been proposed as a promising alternate gate material to replace the conventional poly-Si gate [3]. First of all, the dopant activation in poly-SiGe is better than in poly-Si for p-type gate material. Besides, the p-type poly-SiGe film has lower resistivity, reduced gate-depletion effect, and suppressed boron penetration, thanks to the higher dopant activation ratio comparing with poly-Si film. The improved boron activation is presumably caused by the local strain compensation due to the difference in atomic radii between Si and B atoms [4].

Another important feature of p^+-poly-SiGe is that the p-type work-function decreases with increasing Ge mole fraction [5-10]. For a specified threshold voltage (V_{th}), the channel doping is reduced to compensate for the change in work-function as the p^+-poly-SiGe replaces p^+-poly-Si as the gate electrode. As a result, the channel mobility could increase due to reduced Coulomb scattering. The subthreshold swing

could also be reduced due to decrease in the depletion layer capacitance, leading to an improved I_{on}/I_{off} ratio. The dopant activation temperature could also be reduced owing to the lower melting point of poly-SiGe film, and this is conducive to reducing the process thermal budget. The poly-SiGe alloy films also have good compatibility with standard CMOS processing.

1.1-2 Strained Channel Techniques

Geometric scaling of CMOS transistors has not only led to an increase in circuit integration density but also a corresponding enhancement in the transistor performance. However, as the gate length scales to nanometer regime, some limitations such as off-state leakage current and power density have mad geometric scaling an increasingly challenging task. To continue historical performance improvement, the industry needs a new scaling vector. In this regard, channel strain engineering to improve electron and hole mobility has been actively pursued [11,12]. Strain improves MOSFET drive current by altering the band structure of the channel and can therefore enhance performance even at aggressively scaled channel lengths [13-18].

MOSFETs with bi-axial tensile channel stress by growing a Si channel layer on a relaxed SiGe substrate has been demonstrated [19,20]. Drive current of both NMOSFET and PMOSFET was enhanced by the bi-axial tensile stress when more than 20% of Ge is incorporated in the relaxed SiGe layer. It is noted that the thickness of the top strained-Si layer must be thinner than a critical thickness that depends on the Ge content of the underlying relaxed SiGe layer to avoid the generation of high amount of dislocations. However, the yield issue associated with high threading dislocation density (typically > 10^4 cm^{-2}) of the virtual SiGe substrates represents a major obstacle for practical applications. In addition, other concerns such as high Ge up-diffusion, fast

diffusion of n-type dopants, and high wafer cost further blight the situation.

In contrast, uni-axial channel strain is free from the aforementioned concerns. Uni-axial strain can be engineered by modifying contact-etch-stop-layer (CESL) deposition [21,22], shallow trench isolation (STI) [23,24], source/drain (S/D) material [25], silicidation [26], packing process [27], and so on. Furthermore, the behaviors of carrier mobility under uni-axial strain depend on the strength of the strain and the orientation [28]. Electron and hole mobilities respond to the complex three-dimensional mechanical stress in different, even opposite ways. Depending on the CESL deposition conditions, the SiN layer can generate either tensile or compressive stress [21]. The channel tensile and compressive stress can be applied on NMOS and PMOS devices, respectively, to enhance performance [28].

The carrier mobility is given by $\mu = \frac{q\tau}{m^*}$, where $1/\tau$ is the scattering rate and m^* is the conductivity effective mass. Strain enhances the mobility by reducing the conductivity effective mass and/or the scattering rate. Both effective mass and scattering rate change are important for mobility enhancement in electrons [29]. However, only effective mass change due to band warping and repopulation [30] plays a significant role in holes. For electron transports in bulk Si, the conduction band is comprised of six degenerate valleys (Δ6) of the same energy. Strain removes the degeneracy between the four in-plane valleys (Δ4) and the two out-of-plane valleys (Δ2) by splitting them in energy. The energy difference (ΔE) between Δ2 and Δ4 sub-bands determines the total population of the bands. The enhancement caused by the splitting of conduction band can suppress inter-valley phonon scattering [31]. The lower energy of the Δ2 valleys indicates that they are preferentially occupied by electrons. The electron mobility partly improves by reducing in-plane and increasing out-of-plane effective mass due to the

favorable mass of the Δ2 valleys, which result in more electrons with an in-plane transverse effective mass and out-of-plane longitudinal mass.

For holes, the valence-band structure of Si is more complex than the conduction-band. This complex band structure is as well as valence-band warping under strain resulting in a much larger mobility enhancement of hole than that of electron. These two factors also explain why strained-channel PMOSFET is a key focus in advanced logic technologies. Holes occupy the top two (the heavy- and light-hole) bands for unstrained Si. With the application of strain, the hole effective mass becomes highly anisotropic due to band warping, and the energy levels become mixtures of the pure heavy, light, and split-off bands. Thus, the light and heavy hole bands lose their meaning, and holes increasingly occupy the top band at higher strain due to the energy splitting. To quantify the mobility enhancement of holes, changes of the scattering and effective mass depend on the altered valence band caused by the strain. From full-band Monte Carlo simulation [32], uni-axial compressive strained PMOSFETs may have lighter in-plane effective mass thus improve hole mobility. But, for bi-axial tensile stress, the effective mass is heavier than that in the un-strained case. Thus the hole mobility enhancement is only possible through the reduction of inter-valley scattering [33]. This effect becomes significant only when the strain level is high enough (e.g., Ge > 20 %). Reducing the intra-band acoustic scattering by altering the light- and heavy-hole band density-of-states is negligible for uni-axial strain in Si, even at several hundreds of mega-pascal.

Hole mobility at high vertical field with uni-axial compressive and biaxial tensile stresses would have different behaviors. Splitting of light- to heavy-hole band caused by uni-axial and biaxial stresses has no significant difference without considering surface quantization confinement. However, the splitting of light- and heavy-hole bands caused

by bi-axial tensile stress would be nullified at high electric field due to surface confinement [34]. In contrast, hole mobility enhancement under uni-axial compressive strain is not nullified by surface confinement, which represents a major advantage for MOSFETs operating at high electric fields. The splitting of the surface confinement depends on the relative magnitude of the stress-altered out-of-plane masses of the light and heavy holes. Recent reports [35] showed an interesting result that the out-of-plane effective mass of light hole is heavier than that of the heavy hole for uni-axial stress, and causes the light to heavy hole band splitting to increase. On the contrary, for bi-axial stress the previously-reported out-of-plane effective mass of light hole is lighter than that of the heavy hole, leading to a reduced band splitting. This is why the bi-axial stress degrades hole mobility enhancement at high vertical electric fields.

For NMOSFETs, it has been reported that the threshold voltage shift caused by bi-axial tensile stress is larger than the case with uni-axial tensile strain [36]. For PMOSFETs, larger shift of light-hole band edge under bi-axial tensile strain leads to larger shift in V_{th}, compared with the case with uni-axial compressive strain [35].

1.1-3 Negative Bias Temperature Instability (NBTI)

Bias temperature instability (BTI) is a degradation phenomenon occurring mainly in MOSFETs, known since the late 1960s [37,38]. As the oxide thickness is shrunk to nanometer, hot carrier effects become less important due to the reduced operation voltage [39, 40]. Negative-bias-temperature instability (NBTI) refers to the generation of positive oxide charge and interface traps under negative gate bias at elevated temperatures. It was first reported by Miura and Matukura [41], and further characterized by researchers at Bell Laboratories [42,43], Fairchild Semiconductor [44], and RCA Laboratories [45]. Despite many research efforts, detailed NBTI degradation

mechanism has not yet been fully understood.

Recently, NBTI has been identified as one of the major reliability concerns for deep sub-micron PMOSFETs [46]. A large number of interface states and positive fixed charges were generated during negative-bias-temperature stressing (NBTS), resulting in a negative shift in threshold voltage showing a power-law dependence on stress time with exponent value of 0.2 ~ 0.3. The shift in threshold voltage and degradation in transconductance have been suggested to be due to the interfacial electrochemical reactions related to the holes from the channel inversion layer. A generalized reaction-diffusion model for interfacial charge formation based on the trivalent silicon and its hydrogen compounds was proposed [47], and schematically expressed as [48-50]

$$(Si/SiO_2 \text{ interface defect}) + \text{hole} \leftrightarrow (\text{oxide positive charge}) + (\text{interface trap}) + X_{interface} \qquad (1\text{-}1)$$

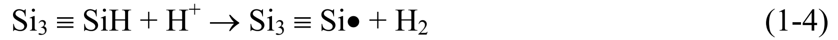
$$X_{interface} \leftrightarrow X_{bulk} \qquad (1\text{-}2)$$

where X represents a mobile species which diffuses away from the interface. It is noted that the initial Si/SiO_2 interface defect in Eq. (1-1) is comprised of a hydrogen passivating Si dangling bond and that X is hydrogen (atom or proton) or some water-related species [48,51,52]. The interface trap is then supposed to be a silicon dangling bond denoted as Si• which results when H is removed from Si–H. A detailed critical analysis of the proposed reactions has been given in [47,49].

The neutral interstitial hydrogen atom or atomic hydrogen would be generated by high electric fields to dissociate the silicon-hydrogen bond [53]:

$$Si_3 \equiv SiH \rightarrow Si_3 \equiv Si\bullet + H^0 \qquad (1\text{-}3)$$

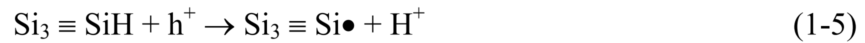
Recently, the positively charged hydrogen or proton (H^+) is considered the only stable charge state of hydrogen at the interface, and reacts directly with SiH to form an interface trap [54]:



$$Si_3 \equiv SiH + H^+ \rightarrow Si_3 \equiv Si\bullet + H_2 \quad (1\text{-}4)$$

The mobile positive H^+ migrates towards the negatively charged dipole region in the SiH molecule due to the polarized SiH. Then, the H^+ atom reacts with the H^- to form H_2, leaving behind a positively charges Si dangling bond.

The interaction of SiH with "hot holes" or holes near or at the Si/SiO_2 interface [47] is given by:



$$Si_3 \equiv SiH + h^+ \rightarrow Si_3 \equiv Si\bullet + H^+ \quad (1\text{-}5)$$

The fixed charge (Q_f) is a by-product of trivalent Si defect near the SiO_2/Si interface oxide and also contributes to the shift of threshold voltage.

$$O_3 \equiv SiH + h^+ \rightarrow O_3 \equiv Si^+ + H^0 \quad (1\text{-}6)$$

The generation of fixed oxide charges is independent of oxide thickness, while the interface trap generation is inversely proportional to oxide thickness [47]. This suggests that NBTI is worse for thinner oxide, but this phenomenon is not always observed and highly dependent on the process conditions.

As proved by Jeppson and Svensson [55], the behavior of the interface trap generation suggests the generation process is diffusion controlled. N_{it} buildup equals the total number of released H species. Hole-assisted reaction breaks interfacial SiH bonds, resulting in N_{it} generation:

$$\Delta N_{it} = S_N (D_x t)^n \quad (1\text{-}7)$$

where D_x is the diffusion coefficient of X in the oxide, time exponent value depends on the type of H species trapped and released in the oxide bulk [56].

1.1-4 Dynamic NBTI

Under actual operations of digital circuits, the applied bias to the gate of PMOSFETs in a CMOS inverter is switched between "high" and "low" voltages.

During “low” phase of PMOSFETs bias, the electric passivation or recovery effect may effectively reduce the interface traps generated during the “high” phase. Dynamic NBTI (DNBTI) may result in a less severe shift in device parameters over the long term compared with the static result [57-59], and greatly prolongs the lifetime of PMOSFETs while the conventional static NBTI measurement underestimates the PMOSFET lifetime. In this aspect, DNBTI stress measurements are much closer to the situation of practical circuit operation.

A physical model is proposed for DNBTI that involves the interaction between hydrogen and silicon dangling bonds [60]. ΔV_{th} is attributed to the creation of interface traps and the released hydrogen species subsequent diffuse towards the gate electrode in the stress process. Then, released hydrogen species re-passivate Si dangling bonds in the recovery process [60]. Some reports found that ΔNit remains constant but ΔVth decreases [61]. This implies that re-passivation of interface states is a negligible part of the recovery process, and that hole de-trapping dominates this process.

1.1-5 Hot-Carrier Effect

One of the serious reliability problems posed by continued shrinking of MOSFETs into the submicron regime is the hot-carrier effect [62,63]. If device dimensions are reduced and the supply voltage remains constant, the lateral electric field in the channel increases. This would cause the inversion layer charge to be accelerated, and leads to a number of harmful devices phenomena. The most important hot carrier effect is the damage inflicted to the gate oxide and/or the Si/SiO_2 interface. This causes a time dependent degradation of various MOSFET characteristics, for example, threshold voltage, linear region transconductance, subthreshold slope, and saturation current.

While the time-dependent degradation of MOSFET device parameters is the result

of hot-carrier effects, another important one involves the substrate current (I_{sub}) generated by such hot carriers. The conventional metric for impact ionization in a MOSFET is the I_{sub}. For MOSFETs, if electrons in the channel acquire more than about 1.5 eV of energy, impact ionization can result upon their collision with the lattice. Electron-hole pairs are generated from such collisions, with the total number being exponentially dependent on the reciprocal of the electric field. The electrons produced in this manner are either attracted to the drain or injected into the oxide if they have sufficient energy. The generated holes, on the other hand, enter the substrate and constitute a parasitic I_{sub}. I_{sub} can also be used to indirectly monitor hot-carrier effects. Hence, the bias conditions that have traditionally been used for performing hot carrier reliability studies are the biases that correspond to maximum I_{sub}.

Hot electron injection is generally considered as the key factor responsible for the hot carrier degradation [64]. One of the simplest microscopic degradation models is based on the assumption that damage arises from the creation of interface states [65]. If $V_{GS} < V_{DS}$ in MOSFETs, hot electrons bombard the Si/SiO_2 interface against a field that tries to repel them. However, if the electrons possess sufficient energy to overcome the barrier of the Si/SiO_2 interface and the repelling field, they can break chemical bonds at the interface. Most likely the bonds that are broken are Si-H bonds. The strength of Si-H bonds is about 0.3 eV. Hence, the barrier energy that would have to be overcome to break the bond would be the sum of the Si/SiO_2 energy barrier (~3.2 eV) plus this bond strength and the retarding potential difference between the current path and the interface. The resultant trivalent Si atom at the Si/SiO_2 interface becomes an electron trap. Such broken bonds accumulate with time, and their filling with electrons would account for the buildup of negative charge at the Si/SiO_2 interface under hot-carrier stress.

The location of the damage region due to hot-carrier stress is found to be adjacent

to the drain of the device. The lifetime of devices is impacted by the spatial non-uniformity of this damage. The extent of the damaged region is a function of device geometry, of the duration and conditions of stress, and of spatial distribution of oxide and interfacial defects. However, it has also been reported that the length of damaged region is independent of channel length [66]. Thus, the damaged region becomes a larger fraction of the channel length as the devices shrink. This causes the percent degradation in drive current to increase more rapidly as L_{eff} is made smaller for the same stressing time and the same value of I_{sub}.

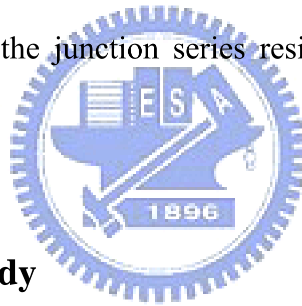
1.1-6 Nano-Scale Silicon-on-Insulator (SOI) CMOS

As the feature size of CMOSFETs is scaled to nano-scale, the challenges to overcome the short-channel-effect (SCE) and dopant fluctuation in ULSI fabrication become more and more difficult to surmount with the conventional structures [67]. Therefore, some new materials and structures are employed for building novel nano-scale transistors. In light of this, some advanced structures, such as FinFET [68-71] and ultra-thin body (UTB) SOI [72], have been proposed to relax these constraints.

Hisamoto et al. [68,69] have proposed a new device structure called double-gate MOSFET (or FinFET) with excellent SCE immunity. This is because the double-gate structure allows the effective termination of the drain field lines, preventing the drain potential from reaching the source end of the channel [68]. Together with a process flow and layout compatible with conventional MOSFETs [73-75], it thus represents one of the most promising candidates for nano device fabrication [69,71]. However, insufficient current driving capability caused by the nature of the fin structure with large series resistance seriously impedes its applications to high speed circuits. In this regards, Schottky barrier (SB) source/drain formed by low resistivity silicide [76,77] is attractive

in reducing the unwanted source/drain series resistance with conventional MOSFETs using heavily doped source/drain.

UTB SOI has also been proposed as a potential candidate for future device manufacturing. The ultra-thin silicon body is effective in reducing the off-state current flowing through the body inherent in conventional planar CMOS structures [78]. Nevertheless, the large parasitic source/drain resistance associated with the thin Si film adversely affects device current drive. To alleviate this shortcoming, raised source/drain structure has been proposed. Drive current increase by as much as 50 % have been demonstrated in UTB devices with raised source/drain [79,80]. Selective epitaxial growth of SiGe [81] by chemical vapor deposition (CVD) has been successfully employed for forming the raised source/drain. It has also been shown that SiGe-epitaxy is more effective in reducing the junction series resistance and contact resistance in PMOS devices than Si [82].



1.2 Motivation of this Study

As mentioned in the above section, devices with strained-channel are powerful for nano-scale devices, especially those built with uni-axial strain technique. Uni-axial channel strain can be free from the concerns related to the bi-axial strain arising from the use of SiGe virtual substrates, such as substrate defects, high Ge out-diffusion, fast diffusion of n-type dopants, self-heating, and high wafer cost. It can also be easily engineered by modifying contact-etch-stop-layer deposition, shallow trench isolation, source/drain silicidation, packing process, and so on. Moreover, the behaviors of carrier mobility under uni-axial strain depend on the strength of the strain and the channel orientation. Depending on the CESL deposition conditions, the SiN layer can generate either tensile or compressive stress. The tensile and compressive channel stress can be

applied to NMOS and PMOS devices, respectively, to enhance performance. Low pressure (LP) and plasma-enhanced (PE) CVD were used to deposit tensile and compressive SiN layer for NMOSFET and PMOSFET, respectively. Thanks to the stress effect of SiN layer, drive current can be greatly enhanced in both NMOSFETs and PMOSFETs.

As the knowledge base concerning mobility enhancement in strained-Si has been reasonably well established, attentions should now be paid to the associated reliability issues for practical applications. NBTI and hot-carrier stress are the most critical reliability issues in deep sub-micron CMOSFETs. They are all deeply related to hydrogen species during stress. Unfortunately, the general precursors used for SiN deposition are NH_3 and SiH_4 (or SiH_2Cl_2). It is reasonable that there are a large amount of hydrogen-containing species in the process chamber during SiN deposition. Those may play an important role in device degradation during NBTI and hot-carrier stress. In this study, we investigate NBTI characteristics of PMOSFETs and hot carrier degradation of NMOSFETs, both having local channel strain induced by the SiN-capping layer.

In this work, we also propose, fabricate, and demonstrate two types of SOI devices with advanced structure. One has Schottky barrier source/drain (S/D) structure implemented with a Schottky barrier height engineering process using impurity segregation of boron. In addition, a CMP-free and "gate-last" scheme for fabricating ultra-thin body (UTB) SOI PMOS transistor with SiGe raised source/drain is also proposed and demonstrated.

1.3 Organization of the Thesis

The dissertation is divided into eight chapters.

In Chapter 1, the backgrounds and motivations of the thesis are reviewed.

In Chapter 2, devices with poly-Si and -SiGe gate electrodes were fabricated and characterized. The poly-SiGe gate electrode can help alleviate poly depletion and boron penetration problem, resulting in higher drive current. Moreover, NBTI degradation between poly-Si and -SiGe gate is identical. Due to less boron penetration, poly-SiGe gate devices even have longer lifetime under NBTI stress.

In Chapter 3, the poly-SiGe gated PMOSFETs with local compressive strain in the channel induced by a compressive PE-SiN capping layer were fabricated. The incorporation of the compressive SiN-capping layer is found to significantly enhance the drive current of PMOSFETs. However, the excess hydrogen species contained in the PE-SiN layer as well as the strain energy stored in the channel may be the culprits for the worsened reliability.

In Chapter 4, DNBTI and AC stress of the devices with PE-SiN capping described in Chapter 3 are further studied. Devices with SiN capping have larger recovery of ΔV_{th} and ΔN_{it} than those without capping. An important message is that the aggravated NBTI in the SiN capping devices could be largely alleviated by high frequency operation.

In Chapter 5, we investigate and compare the characteristics of NMOSFETs with and without LP-SiN capping layer. Moreover, we also investigate the effects of LP-SiN deposition process on the device characteristics. The thermal budget associated with the deposition of the SiN capping layer could alleviate the reverse short-channel effect of the uncapped devices. The bandgap narrowing effect due to the channel strain may result in further lowering in V_{th} as the channel length is shortened.

In Chapter 6, hot carrier stress was performed on devices with LP-SiN capping. Both the deposited SiN layer and the deposition process itself have significant impacts on the device operation and the associated reliability characteristics. Nevertheless, the

accompanying bandgap narrowing and the increased carrier mobility tend to worsen the hot-electron reliability. In this aspect, attention should also be paid to the SiN deposition process itself.

In Chapter 7, novel SB FinFET and UTB SOI device were proposed and demonstrated in this chapter. The drive current of the SB device with impurity segregation is five times larger than that of the SB device with conventional field-induced drain (FID) scheme. Moreover, we also have proposed and successfully demonstrated a new CMP-free process for fabricating UTB SOI PMOS transistors with SiGe raised source/drain and replacement gate.

In Chapter 8, we conclude with summaries of the experimental results. Recommendations for future research are also given.

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Chapter 2

Fabrication and Reliability Characterization of Poly-SiGe-Gated Devices

2.1 Introduction

Technical challenges emerge as the critical dimensions of semiconductor devices are scaled down to the deep-submicron regime in pursuit of higher levels of integration and performance. To address the short-channel effects associated with the conventional buried-channel PMOSFETs, the "dual-gate" process has replaced the conventional "single-gate" process for advanced CMOS fabrication [1,2]. For dual-gate process, however, boron penetration through the gate oxide from the p^+-doped gate of PMOSFETs becomes a new but major concern. In addition, gate-depletion effect due to insufficient dopant activation at the gate/dielectric interface becomes more significant as gate oxide thickness becomes thinner, and leads to the degradation of the drive current [3,4]. To alleviate the above-mentioned problems, poly-SiGe has been proposed as a promising alternate gate material to replace the conventional poly-Si gate [5]. Firstly, the dopant activation in poly-SiGe is better than that in poly-Si for p-type gate material. Besides, the p-type poly-SiGe film has lower resistivity, reduced gate-depletion effect, and suppressed boron penetration, thanks to the higher dopant activation ratio as comparing with poly-Si film.

Bias temperature instability (BTI) is a degradation phenomenon occurring mainly in MOSFETs, known since the late 1960s [6,7]. Negative Bias Temperature Instability (NBTI), in which interface traps and positive oxide charges are generated in metal-oxide-silicon (MOS) structures under negative gate bias, in particular at elevated

temperatures. NBTI of pMOSFETs is becoming an increasingly serious issue for the reliability of scaled CMOS devices. In this work, we found that devices with the poly-SiGe gate electrodes can help alleviate poly-depletion and boron penetration problem without degrading the NBTI characteristics.

2.2 Devices Fabrication

The PMOSFETs tested in this study were fabricated on 6-in n-type Si wafers with conventional local oxidation of silicon (LOCOS) isolation. Gate oxide with a thickness of 3 nm was grown in a vertical furnace in O_2 at 800 ˚C. After gate oxide growth, a 150 nm poly-Si and/or poly-SiGe layer were deposited by LPCVD, followed by standard plasma gate-etch process to form the patterned gate. Afterwards, the standard procedures of forming TEOS spacer and S/D junctions were performed, and then a TEOS passivation layer was deposited by a LPCVD system. Contact holes and metallization processes were subsequently performed. Finally, the processing is completed with a forming gas annealing at 400˚C. In this study, the content of germanium of silicon is around 20%, measured by secondary ion mass spectroscopy (SIMS), as shown in Fig. 2.1. Electrical characterizations were measured using an HP4156 system. NBTI stress measurements were performed using a temperature-regulated hot chuck. Setups of measurements are shown in Fig. 2.2. The source, drain, and substrate electrodes were all connected to ground, while the gate bias was applied with -3.2 V, -3.5 V, and -3.8 V, during the measurements. Interface traps were evaluated using charge pumping method with a fixed amplitude of 1.5 V at 1 MHz.

2.3 Results and Discussion

2.3-1 Electrical Characteristics of Poly-SiGe Gate Electrode

Figure 2.3 shows the cumulative probability distribution of sheet resistance for poly-Si and poly-SiGe (Ge: 20%) gates with nominally identical implantation (Boron, 3×10^{15} cm^{-2}, 10 keV) and annealing conditions (900˚C, 30 sec). Thickness of the films is around 150 nm. As can be seen in the figure, the sheet resistance becomes lower as Ge is incorporated, owing to the higher dopant activation [8]. Figure 2.4 compares the C-V characteristics of the devices. This further confirms that poly-SiGe gate could effectively suppress poly-depletion effect, consistent with the sheet resistance data. The shift of flat band voltage in Fig. 2.4 is due to the work function difference of poly-Si and poly-SiGe. Si and Ge have similar electron affinities but Ge has a much smaller bandgap. Therefore, a relatively large energy difference (>0.5 eV) exists between the valence-band edges of Si and Ge. The work function is defined to be the difference between the free electron energy (vacuum level) and Fermi level. Since the Fermi level is close to the valence-band in a p-type semiconductor, the work function of p^+-poly-SiGe can be expected to decrease noticeably with Ge incorporation. The work function difference would shift flat band voltage.

$$V_{fb} = \phi_{ms} - \frac{Q_{ox}}{C_{ox}} \qquad (2\text{-}1)$$

where ϕ_{ms} is the work function difference, C_{ox} is the gate oxide capacitance per unit area, and Q_{ox} is the equivalent oxide charge per unit area at the oxide-silicon interface.

Using the capacitance definitions [9], we obtain

$$\frac{1}{C_{\max}} = \frac{1}{C_{ox}} + \frac{1}{C_{Si}} + \frac{1}{C_p} = \frac{1}{C_{ox}} + \frac{2kT}{qQ_p} + \frac{Q_p}{\varepsilon_{Si} q N_p} \qquad (2\text{-}2)$$

where C_p is the capacitance of the poly depletion region. As gate voltage becomes more positive, C_{Si} ($\propto Q_p$) increases but C_p ($\propto 1/Q_p$) decreases. This results in a local maximum of the low-frequency capacitance at a V_G or Q_p value where the last two

terms of Eq. (2-2) are equal,

$$\frac{1}{C_{\max}} = \frac{1}{C_{ox}} + \sqrt{\frac{8kT}{\varepsilon_{Si} q^2 N_p}} \tag{2-3}$$

where $Q_p = \sqrt{2\varepsilon_{Si} kTN_p}$. The active doping concentration of the poly gate can be easily estimated using Eq. (2-3). From Fig. 2.4, the active concentration of poly-Si and -SiGe are 6.4×10^{18} cm^{-3} and 1.8×10^{19} cm^{-3}, respectively. The results are consistent with sheet resistance results that poly-SiGe has higher dopant activation than poly-Si.

As discussed above, poly-SiGe has the ability to suppress boron penetration and poly depletion effect. These result in improved output characteristics for the device with poly-SiGe gate, as shown in Fig. 2.5. The increase of the saturation current in poly-SiGe gate is due to larger dopant activation and less poly depletion effect. Clearly, the saturation current is enhanced by about 5.8% by adopting poly-SiGe gate electrode. The hole mobility was also extracted by split-CV technique [10] in this work. Mobility is expressed as

$$\mu = \frac{L}{W} g_d \frac{1}{Q_{inv}} = \frac{L}{W} \frac{I_d}{V_d} \frac{1}{Q_{inv}} \tag{2-4}$$

where Q_{inv} is the channel charge per unit density and can be calculated from the integration of C_{inv} (the inversion capacitance). Due to reduced poly depletion, poly-SiGe gated device has a slightly higher Q_{inv}. Figure 2.6 shows the mobility as a function of effective vertical electric field. PMOSFETs using poly-SiGe as gate electrode have a slight lateral shift on hole mobility with nominally identical channel doping profile. Actually, current enhancement in poly-SiGe gated device is due to higher active carrier concentration and thus thinner EOT). However, lowering in channel doping to compensate for the V_{th} shift due to work-function difference in poly-SiGe-gated devices may result in improved low-field mobility.

2.3-2 Negative Bias Temperature Instability Characterization

For the aggressively scaled CMOS technology, ultra-thin gate oxide is essential to maintain high drive current under lower power operation. The integrity and reliability of such thin gate oxides are therefore crucial for ultra-large-scale-integration (ULSI) manufacturing. Recently, NBTI has been identified as the most likely lifetime-limiting reliability concern for deep sub-micron PMOSFETs [11]. It has been observed that a large number of interface states and positive oxide trap charges are generated during NBT stressing, causing a negative threshold voltage shift that shows a power-law dependence on stress time:

$$\Delta V_{th} = A \cdot t^{n} \qquad (2\text{-}5)$$

This phenomenon becomes even more pronounced as the gate oxide is scaled down, and may even become the lifetime-limiting factor for deep sub-micron p-channel devices. The exponential value of the power law equation is around 0.25, which could be explained by the diffusion-controlled electrochemical reactions. A generalized reaction-diffusion (R-D) model for interfacial charge generation based on trivalent silicon and its hydrogen compounds was proposed [12,13] and modeled as

$$Si_3{\equiv}SiH + X \rightarrow Si_3{\equiv}Si\bullet + Y_{interface} \qquad (2\text{-}6)$$

$$Y_{interface} \rightarrow Y_{bulk}^{+} \qquad (2\text{-}7)$$

where $Si_3{\equiv}Si\bullet$ is the interface trap, X is a hole-related species, and Y is a hydrogen species. This reaction causes interface trap generation at the interface, and the released hydrogen diffuses into the gate dielectric, generating positive charge [14]. Actually, NBTI degradation is largely related to the hydrogen species, especially those located at the SiO_2/Si interface.

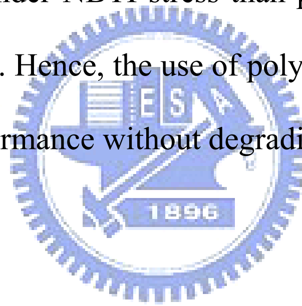
Firstly, the NBTI characteristics of poly-Si and -SiGe gated devices were tested. As shown in Fig. 2.7, threshold voltage shift and interface state generation are slightly

larger in poly-Si than poly-SiGe gated devices. However, the NBTI degradation of poly-Si and -SiGe gated devices is nearly the same. As stated above, the exponent value of power-law dependence in NBTI is an important indicator during NBTI stress. Different types of hydrogen-related species possess different exponent values [15]. Table 2-I shows possible types of hydrogen-related species and their corresponding exponent values. Table 2-II shows the exponent values of the test devices. It is clearly seen that neutral and molecular hydrogen species are the major diffusion species in poly-SiGe and -Si gated devices. It is noted that the exponent values of the poly-SiGe gated devices is slightly smaller than those of the poly-Si gated ones. The smaller exponent value may be due to less boron penetration in the poly-SiGe gated devices. In other words, poly-SiGe gated devices depict less NBTI degradation in the long time stress because of their smaller exponent values.

Figure 2.8 is the charge pumping current (Icp) of the poly-Si and -SiGe gate electrodes in fresh state and after 5000 sec NBTI stress. In fact, Icp between the poly-Si and -SiGe gate electrodes is nearly the same. This indicates that devices with the poly-Si and/or -SiGe gate electrodes have the same interface state generation during NBTI stress. The activation energy (E_A) of poly-Si and -SiGe gates under NBTI stress is shown in Fig. 2.9. It is clearly seen that a slight difference in E_A exists between poly-Si and -SiGe gated devices. E_A as shown in Fig. 2.9 suggests hydrogen species is neutral H_2 [16], which is consistent with the result of exponent value. Figure 2.10 is the ten-year lifetime, extracted by using ΔV_{th} = -30 mV as the lifetime criteria, of poly-Si and -SiGe gated devices. It is clearly seen that poly-SiGe gated device has slightly longer lifetime than poly-Si gated counterpart due to less boron penetration in the poly-SiGe gate.

2.4 Summary

Devices with poly-SiGe gate electrodes can help alleviate poly-depletion and boron penetration problem because of the higher dopant activation in p-type semiconductor. Under the same implant condition and annealing temperature, the active concentration of poly-Si and -SiGe are 6.4×10^{18} cm^{-3} and 1.8×10^{19} cm^{-3}, respectively. These result in about 5.8% enhancement of saturation current by using poly-SiGe gate electrode. During NBTI stress, the neutral and molecular hydrogen species are major diffusion species in both poly-SiGe and -Si gate devices. It is interesting to see that the exponent values of power-law dependence in the poly-SiGe gated devices are slightly smaller than those in the poly-Si gated ones. In addition, the poly-SiGe gated devices have slightly longer lifetime under NBTI stress than poly-Si gated devices due to less boron penetration in the former. Hence, the use of poly-SiGe gate electrode is beneficial for enhancing PMOSFET performance without degrading reliability characteristics.



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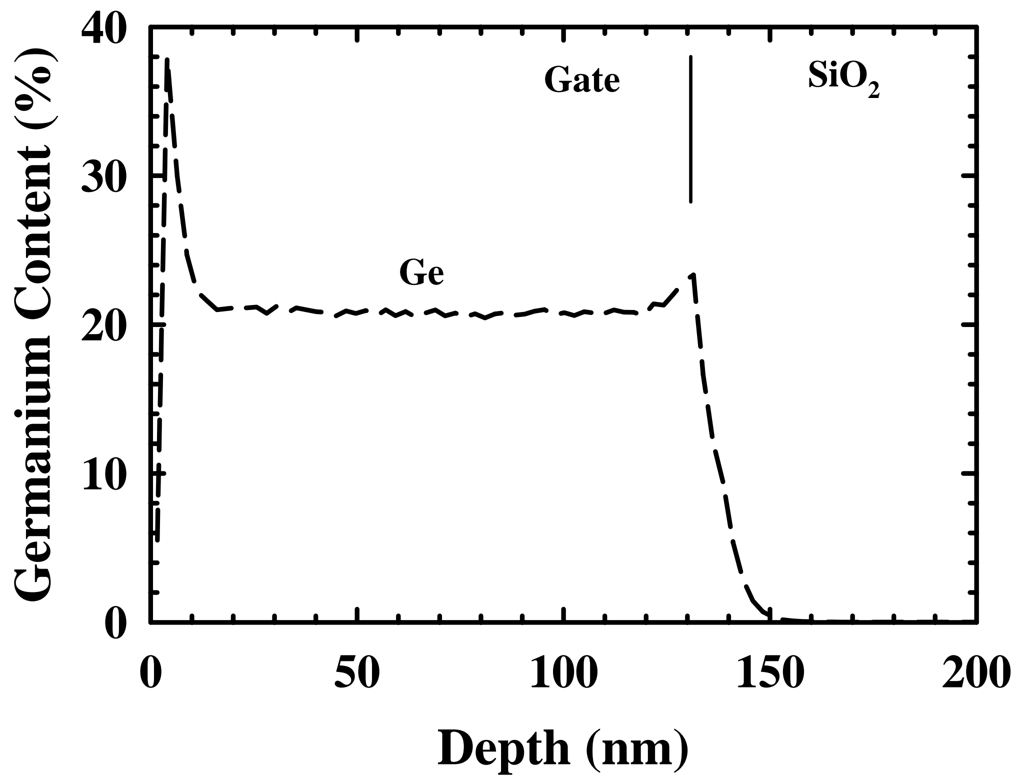

Fig. 2.1 SIMS profile of germanium content in the deposited poly-SiGe material.

Stress: $V_G - V_{th}$ = -3.2V, -3.5V, and -3.8V

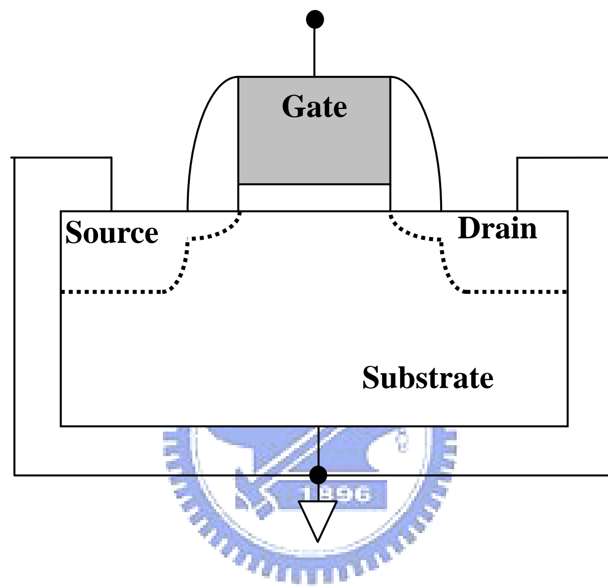

Fig. 2.2 Measurement setup of NBTI stress.

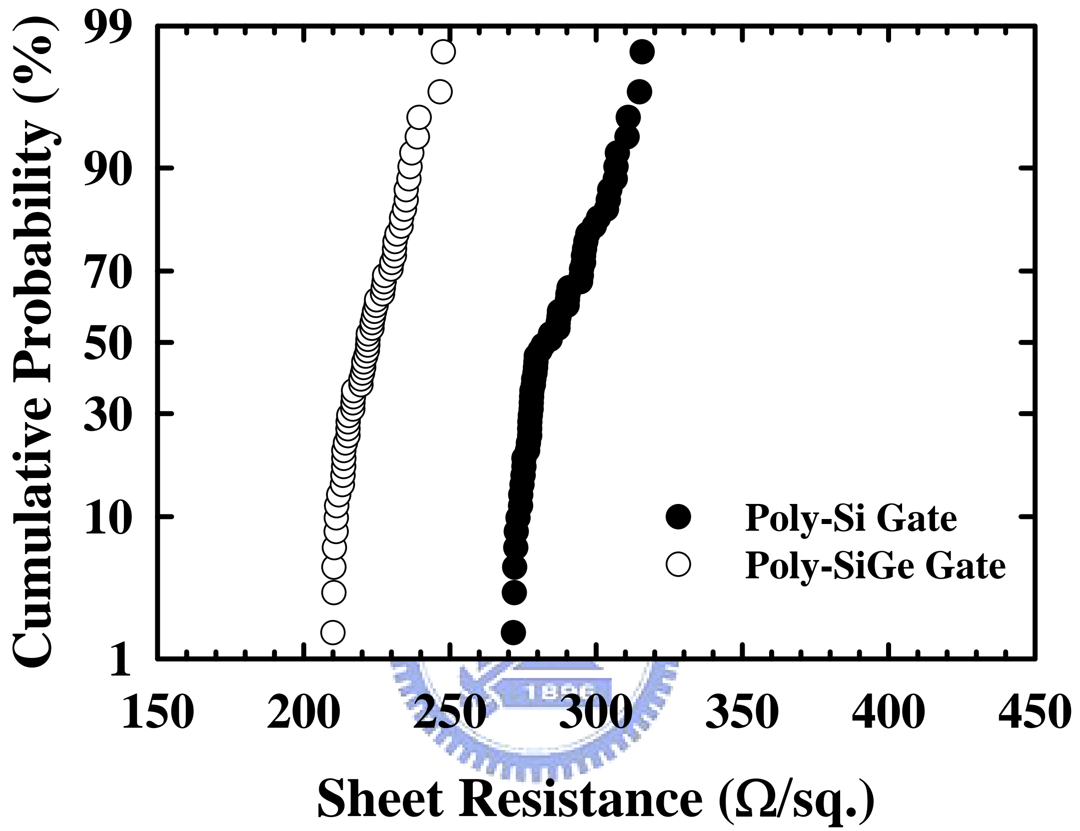

Fig. 2.3 Cumulative probability distribution of sheet resistance in poly-Si and poly-SiGe films. Both with the same implantation (boron, 3×10^{15} cm^{-2}, 10 keV) and annealing temperature (900˚C, 30 sec).

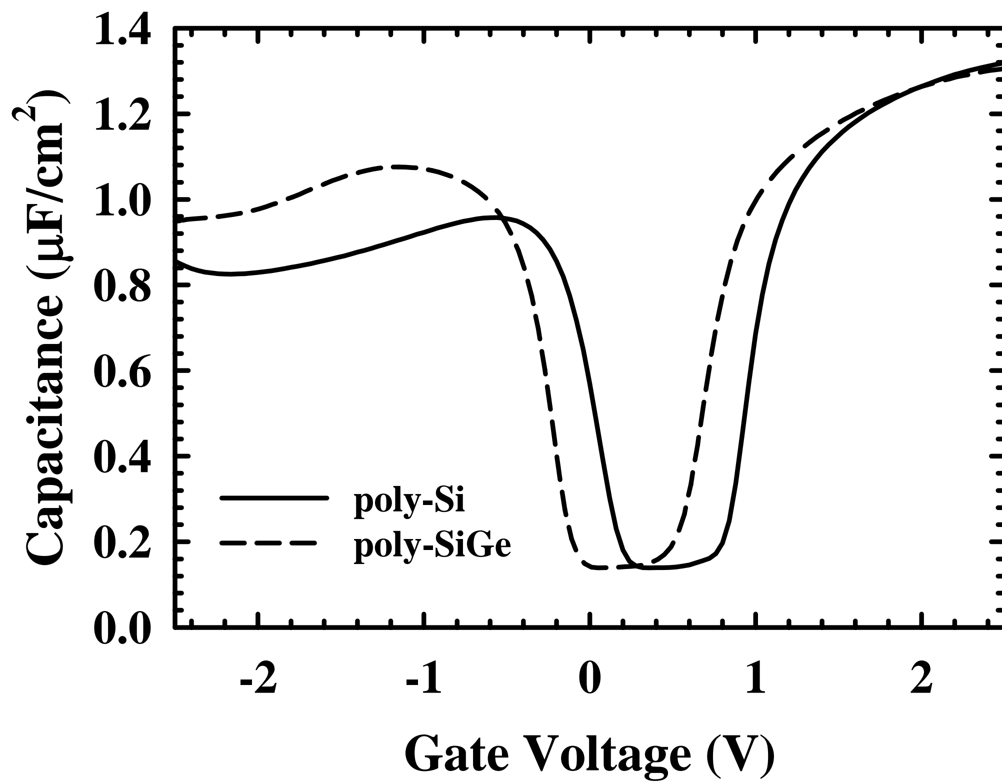

Fig. 2.4 Capacitance-voltage *(C-V)* characteristics of devices with poly-Si and poly-SiGe gates.

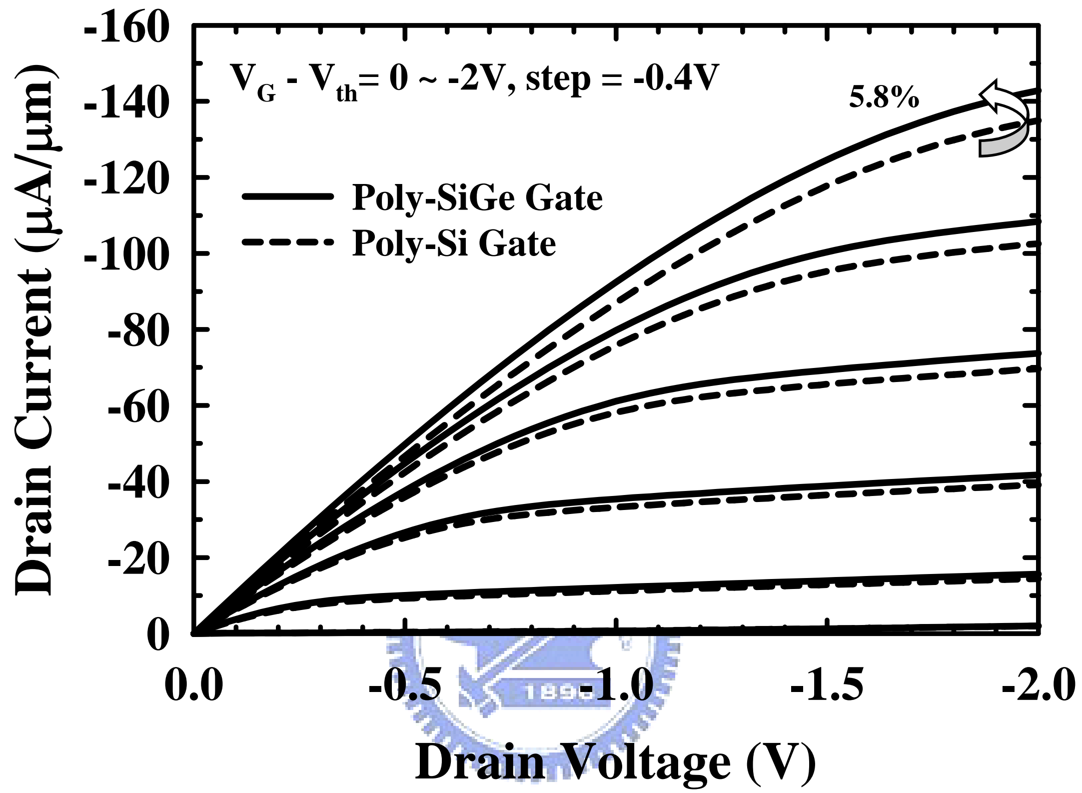

Fig. 2.5 Output characteristics of devices with poly-Si and poly-SiGe gates at L/W= 1μm/10μm.

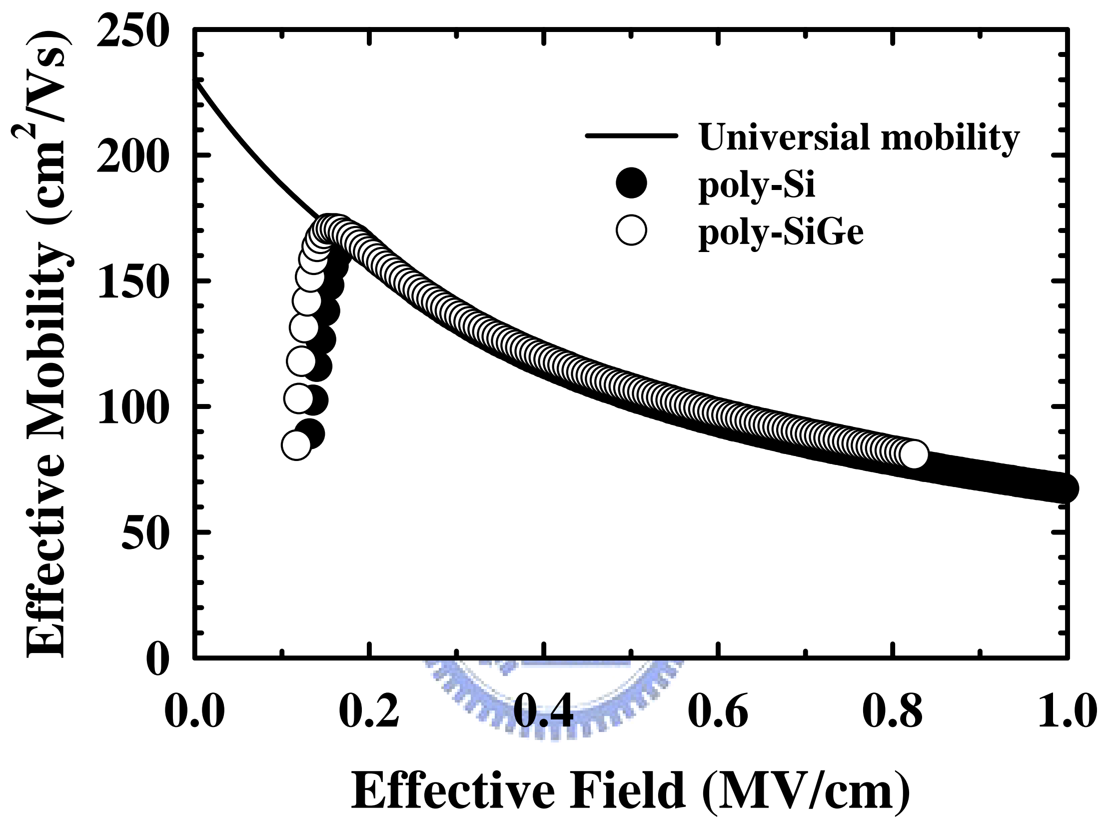

Fig. 2.6 Comparison of effective hole mobility between poly-Si and -SiGe gated devices measured by split-CV method.

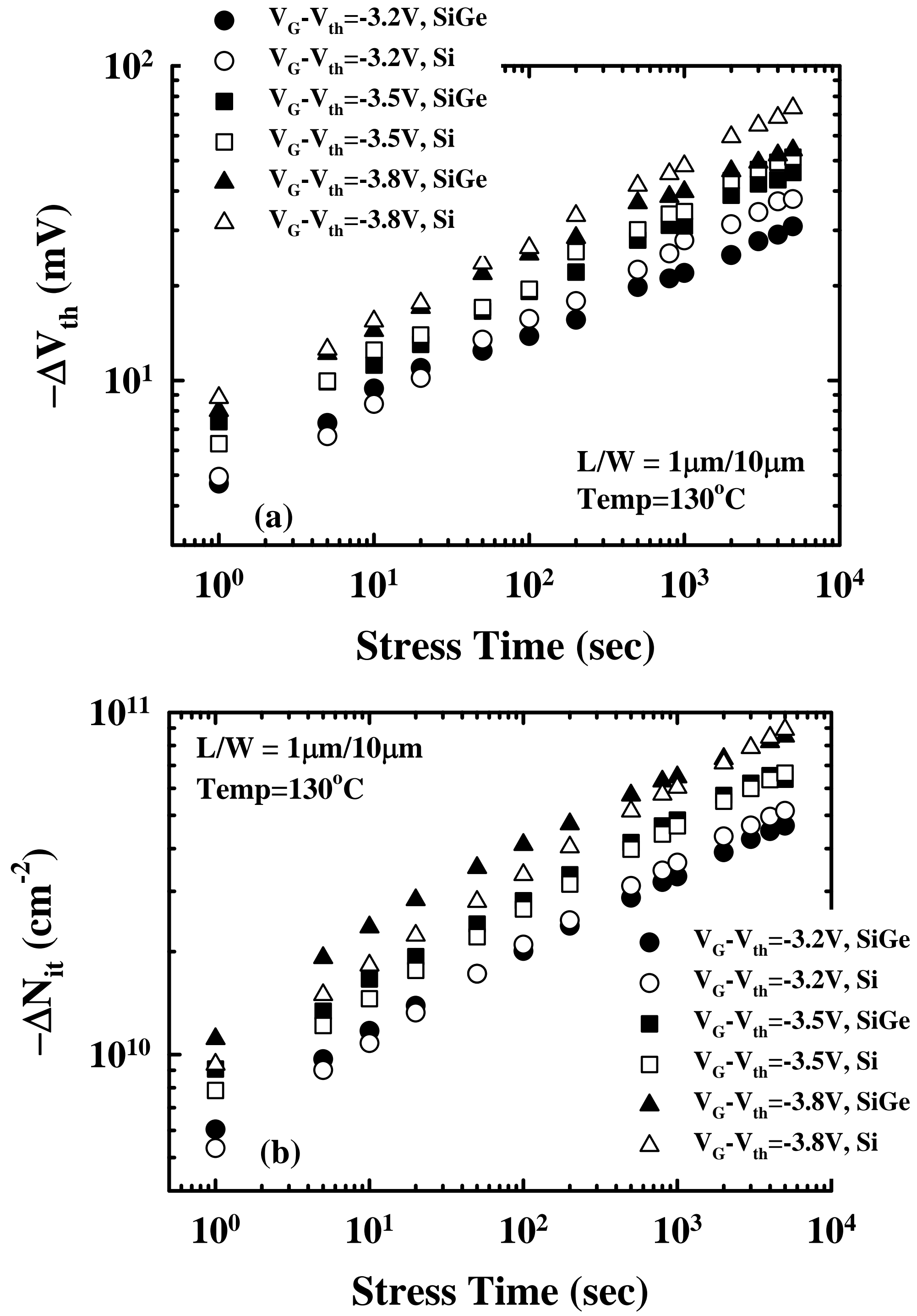

Fig. 2.7 (a) ΔV_{th} and (b) ΔN_{it} versus stress time at three different gate biases performed at 130˚C for poly-Si and -SiGe gated devices.

Table 2-I Fractional time dependence of NBTI for different species.

Species	Exponent value
H^0	0.25
H_2	0.165
H^0, H_2	0.165 ~ 0.25
H^+	0.5
H^0, H_2, H^+	0.165 ~ 0.5

Table 2-II Exponent values of power-law dependence in the poly-Si and -SiGe gated devices under different stress biases and temperatures.

SiGe	70˚C	100˚C	130˚C
$V_G - V_{th} = -3.2V$	0.1868	0.1836	0.1997
$V_G - V_{th} = -3.5V$	0.1788	0.2052	0.2244
$V_G - V_{th} = -3.8V$	0.1774	0.1957	0.2065
Si			
$V_G - V_{th} = -3.2V$	0.2158	0.2368	0.2367
$V_G - V_{th} = -3.5V$	0.2214	0.2252	0.2382
$V_G - V_{th} = -3.8V$	0.2220	0.2439	0.2523

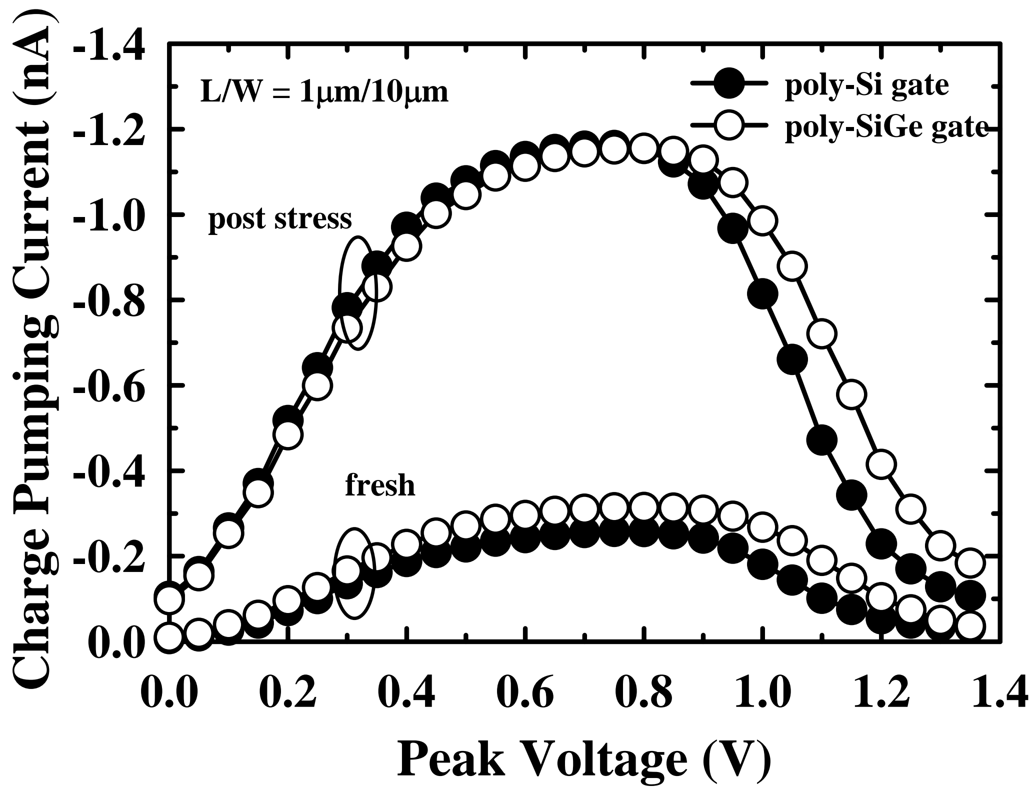

Fig. 2.8 Charge pumping current in fresh state and post 5000sec NBTI stress for devices with poly-Si and -SiGe gate electrodes at L/W = 1 μm/10 μm. NBTI stress was performed at $V_G - V_{th}$ = -3.5 V and 100˚C.

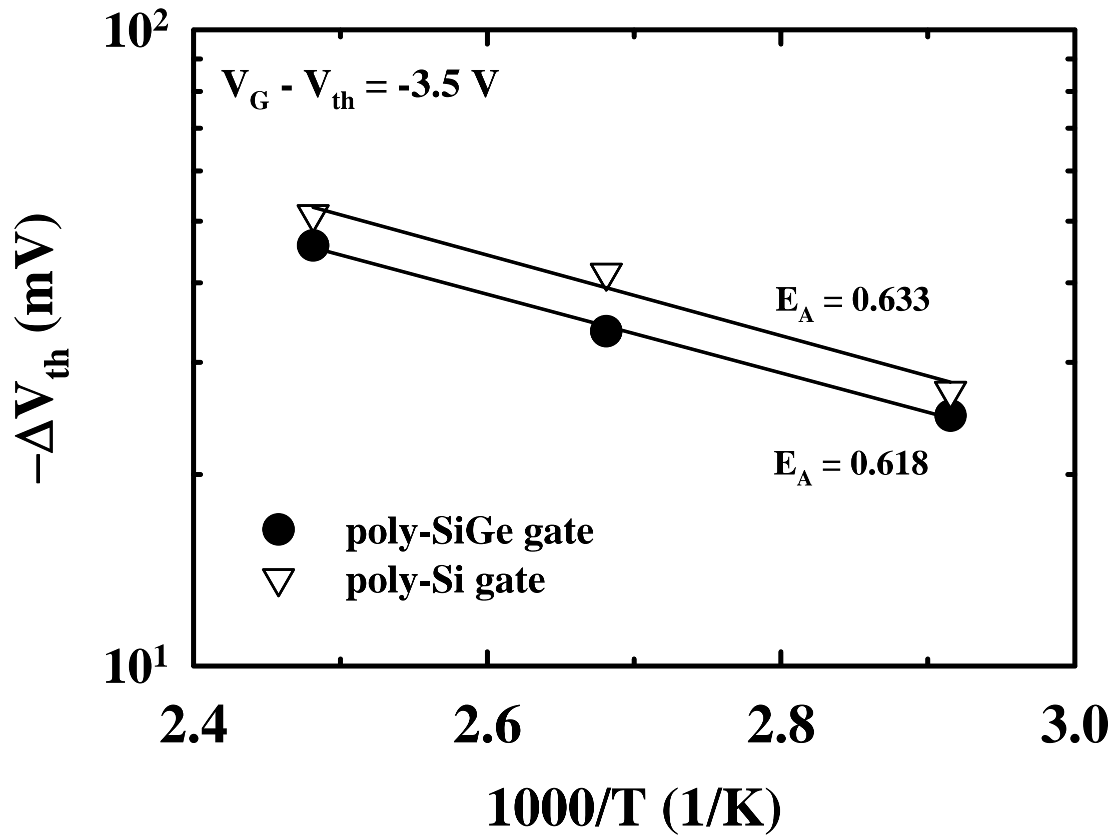

Fig. 2.9 Activation energies of the poly-Si and -SiGe gated devices at $V_G - V_{th}$ = -3.5 V.

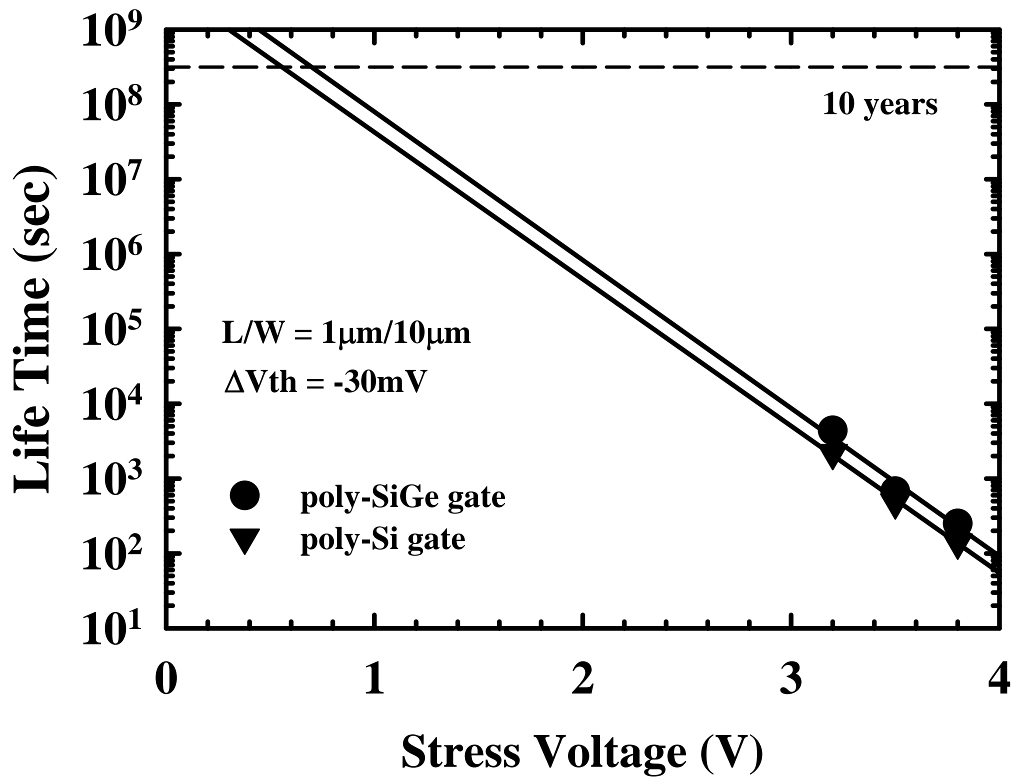

Fig. 2.10 10-year lifetime projection for the poly-Si and -SiGe gated devices. Lifetime was defined as ΔV_{th} = -30 mV.

Chapter 3

Devices Characteristics and Aggravated Negative Bias Temperature Instability in PMOSFETs with Uniaxial Compressive Strain

3.1 Introduction

Aggressively scaled metal-oxide-semiconductor field-effect transistors (MOSFETs) suffer from carrier mobility degradation because of the higher channel doping necessary for keeping the short-channel effects at bay. Recently, mobility enhancement by channel strain engineering has emerged as an effective approach to alleviate the above shortcoming, especially local-strain technology [1-7]. This could be accomplished by either applying a large biaxial tensile strain to the channel region with a SiGe virtual substrate [1,2], or by uniaxially straining the channel with strain boosters [3-7]. The former approach, however, suffers from a number of drawbacks such as Ge up-diffusion and high defect density. In contrast, the latter approach is essentially free of the aforementioned drawbacks, and therefore is more suitable for practical manufacturing. In fact, Intel has adopted this approach by introducing tensile strain to n-channel devices through a low-pressure chemical vapor deposition (LPCVD) SiN capping layer over the gate electrode, while simultaneously introducing compressive strain to p-channel devices through SiGe source/drain (S/D) [5,7]. Another method to introduce compressive strain to the channel of PMOSFETs is by use of a SiN capping layer deposited by plasma-enhanced CVD (PECVD) [3,4]. Though strained channel could enhance the mobility and thus the drive current of the device, potentially it could also

compromise the device's reliability characteristics. This is because the energy stored in the strained channel may be released during normal device operation, resulting in additional defect generation. The device reliability issue is therefore a potential concern when the local strain is introduced, and should therefore be carefully addressed. In the mean time, hydrogen species unintentionally incorporated in the thin film of stress booster may also affect the device characteristics. Negative bias temperature instability (NBTI) is well known as the lifetime-limiting reliability concerns in PMOS devices when the gate oxide thickness is scaled to 3.5 nm and beyond [8]. In this work, we investigate not only drive current enhancement but also the NBTI of PMOSFETs having compressive channel strain.

3.2 Devices Fabrication

The PMOSFETs in this study were fabricated on 6-in. n-type Si wafers with conventional local oxidation of silicon (LOCOS) isolation. Gate oxide with a thickness of 3 nm was grown in a vertical furnace in O_2 at 800˚C. After gate oxide growth, a 150 nm poly-SiGe layer was deposited by LPCVD, followed by a standard plasma gate-etch process to form the patterned gate. Afterwards, the standard procedures of forming TEOS spacer and S/D junctions were performed, followed by the deposition of a PECVD SiN layer (100 nm or 300nm) and a PECVD TEOS passivation layer. Contact holes and metallization processes were subsequently performed. Finally, the processing was completed with a forming gas anneal at 400˚C. Electrical characterizations were measured using an HP4156 system. NBTI stress measurements were performed using a temperature-regulated hot chuck at 125˚C. The measurement setup is shown in Fig. 3.1. Interface traps were evaluated using charge pumping method with a fixed amplitude of 1.5 V at 1 MHz.

3.3 Results and Discussion

3.3-1 Devices Characteristics

Channel strain engineering is slated for mobility enhancement in the 2003 ITRS roadmap with much fanfare. Strains can improve MOSFET's drive current by altering the band structure of the channel and thus enhance the device performance especially for devices with scaled channel lengths. In our study, the stress induced by depositing PE-SiN layer was first examined by probing the blanket samples deposited on Si wafers. The stress was measured to be around –469.8 MPa for 300 nm SiN capping layer. The minus sign indicates that the stress is compressive in nature, and its magnitude is found to increase monotonically with increasing thickness. Figure 3.2 shows the cross-sectional TEM pictures of devices with and without SiN capping. It can be seen that the gate oxide thickness as illustrated in the TEM pictures is indistinguishable between the two splits. Figure 3.3 compares the output characteristics of PMOSFETs with and without SiN capping layer. It can be seen that irrespective of the drain voltage, the drive current always increases when the SiN capping layer is incorporated. Fig. 3.4 shows the percentage increase of the drive current for the SiN-capped devices, compared with the controls, as a function of channel length. When the channel length is scaled to less than 1 μm, the drive current increases sharply owing to the unique feature mentioned above. In general, nearly 29% and 36% in drive current enhancement is observed for the SiN layer thickness of 100 nm and 300 nm, respectively, both with a channel length of 0.45 μm.

The capacitance-voltage (*C*-*V*) characteristics shown in Fig. 3.5 indicate that although the inversion gate oxide thickness is slightly thicker for the control sample, the thickness difference alone cannot account for the observed large drive current enhancement. This confirms that the drive current enhancement is not due to the

variation in gate oxide thickness. The slight shift of the threshold voltage is due to the hydrogen species that will be addressed in more detail later. The transconductance values (Gm) is linearly related to channel mobility. As shown in Fig. 3.6, Gm exhibits similar trend, i.e., it increases by 38% and 54% with the implementation of the channel strain with SiN thickness of 100nm and 300nm, respectively. These findings confirm the effectiveness of compressive SiN capping in enhancing the hole mobility, as reported previously [3,4].

Despite the shift in threshold voltage, the subthreshold characteristics of the devices do not seem to be affected by the SiN capping, as shown in Fig. 3.7. The threshold voltage shift could be due to the bandgap narrowing by the compressive strain [9,10]. As channel length decreases, the threshold voltage difference between the control and strain samples widens, as shown in Fig. 3.8. This is a unique feature of the uniaxial strain that the booster effect becomes more prominent with reducing channel length.

In short, we have confirmed that devices with SiN capping operating at room temperature indeed exhibit enhanced performance, consistent with literature report. When the device is operating at a raised temperature (e.g., 125 ˚C), similar trend is also observed, as shown in Fig. 3.9. For the device with a channel length of 0.45 μm, the drive current enhancement still reaches 25%. The results depicted in Fig. 3.9(b) indicate that the uniaxial strain also shows less effect on the subthreshold slope at higher temperature.

3.3-2 Field Effect Mobility at Low Temperature

In order to understand the reason of mobility gain in PMOSFETs with SiN capping, low temperature measurements were performed. Because of the difficulty in measuring

the capacitance of small area, the field-effect mobility (μ_{FE}) is measured, instead of the effective mobility (μ_{eff}). While the effective mobility is derived from the drain conductance, the filed-effect mobility is determined from the transconductance. The field-effect mobility is given by

$$\mu_{FE} = \frac{LGm}{WC_{ox}V_{DS}} \qquad (3\text{-}1)$$

The discrepancy between μ_{eff} and μ_{FE} is due to the negligence of electric field dependence of the mobility in the derivation of Eq. (3-1). In addition, parasitic S/D resistance will also affect the accuracy of field-effect mobility. Figure 3.10 shows μ_{FE} versus gate voltage in the devices with and without SiN capping. The mobility is dominated by the coulomb scattering and the phonon scattering at low effective field region. The coulomb scattering and the phonon scattering are primarily affected by the substrate concentration and the measure temperature, respectively. Since the substrate doping is nominally identical for those splits of samples, it is reasonable to assume that all samples have nominally identical contribution of Coulomb scattering. In Fig. 3.10 we can see that, irrespective of whether the SiN capping is deposited or not, the low field mobility increases as temperature decreases due to the suppression of phonon scattering. However, in the devices with SiN capping, the phonon scattering is largely suppressed. It is clearly seen that the mobility gain increases with decreasing measurement temperature in Fig. 3.11. Hence, we deduce that the phonon scattering is an important factor on mobility enhancement in devices with SiN capping.

3.3-3 Negative Bias Temperature Instability Characterization

For the aggressively scaled CMOS technologies, ultrathin gate oxide is essential to maintain high drive current under lower power operation. Recently, NBTI has been

identified as the most likely lifetime-limiting reliability concern for deep sub-micron PMOSFETs [11]. It was observed that a large number of interface states and positive oxide trap charges are generated during negative-bias-temperature stressing (NBTS), causing a negative shift of threshold voltage (ΔV_{th}) that shows a power-law dependence on stress time:

$$\Delta V_{th} = A \cdot t^{n} \qquad (3\text{-}2)$$

The exponential value of the power law equation is around 0.25, which could be explained by the diffusion-controlled electrochemical reactions. Based on the $t^{0.25}$-like time evolution, a generalized reaction-diffusion (R-D) model for interfacial charge generation based on the trivalent silicon and its hydrogen compounds was proposed [12,13], and the released hydrogen diffuses into the gate dielectric, generating positive charge [14].

Figures 3.12 and 3.13 show the results of NBTI for the control and two SiN-capped samples performed at three different gate biases at either 25˚C or 125˚C, respectively. It can be seen that more interface states are being generated. In addition, a larger gate bias leads to a larger ΔV_{th}. As can be seen in the figures, under the same stress conditions, a much larger change in ΔV_{th} is observed for devices with SiN capping. For example, at $V_G - V_{th} = -3.9$ V and stress time of 10000 sec, ΔV_{th} between the control sample and devices with SiN capping of 100 nm and 300 nm are 16.9 mV, 73.8 mV, and 85.4 mV at 25˚C, and 56.2 mV, 425.5 mV, and 457.9 mV at 125˚C. The shift curves show a fractional power-law dependence on time, and the values of the exponent are roughly 0.2 and 0.3 for samples without and with SiN-capping layer, respectively. In short, ΔV_{th} increases significantly for devices with SiN capping, especially at higher temperature. It is noted in Figs. 3.13(b) & (c) that the saturation phenomenon in ΔV_{th} is observed for the devices with SiN capping when NBT stress

time is longer than 1000 sec at 125˚C. The increase in interface state density (ΔN_{it}) for different splits of samples shows similar saturation characteristics in Figs. 3.13(b) & (c).

The saturation of ΔV_{th} and ΔN_{it} appear in the devices with SiN capping layer after long time stress. This saturation behavior in ΔV_{th} has previously been investigated by Liu et al. [15]. Recently, Zafar [16] and Huard [17] also observed that ΔV_{th} might eventually saturate after subjecting to a sufficiently long stress time. In this work, saturation in ΔV_{th} for SiN-capped devices is attributed to the fact that nearly all the interfacial Si-H bonds have been broken [16]. The large amount of hydrogen species as well as the channel strain effect is presumably the keys responsible for the phenomenon that will be addressed in more detail later.

The above results clearly indicate that the NBTI is aggravated for devices with SiN-capping. Figure 3.14 shows the Gm degradation ratio as a function of stress time, and Gm_{max} degrades gravely in the devices with SiN-capping at high temperature. Despite the significant enhancement in Gm in fresh devices with SiN capping, the degradation under bias-temperature stressing is also grossly aggravated. As can be seen in the figure, the Gm_{max} degradation at 125 ˚C is near 21 % and 23 % in devices with SiN-capping thickness of 100 nm and 300 nm, respectively, both after 10000 sec stress. Although the capping of a SiN layer can enhance drive current in the fresh device, NBT stress degrades the device performance and almost negates the benefit gained by SiN capping layer.

3.3-4 Hydrogen Content in PE-SiN Layer

As mentioned in the above discussions, the saturation behavior in ΔV_{th} may be due to the fact that nearly all the interfacial Si-H bonds have been broken. The extra hydrogen species come from the SiN layer as a result of using SiH_4 and NH_3 as

precursors during deposition. It is well known that the PE-SiN film contains a substantial amount of hydrogen [18]. Actually, the extra signal pertaining to S-H bonds can easily be detected in the PE-SiN by using Fourier transform infrared spectrometer (FTIR), as shown in Fig. 3.15. The charge pumping current of the fresh device with SiN capping is slightly smaller than that of the control sample, as shown in Fig. 3.16. This is ascribed to the fact that hydrogen can effectively passivate the dangling bonds at the SiO_2/Si interface, and leads to a lower interface state density for the as-fabricated devices with SiN-capping regardless of the channel length scaling, as shown in Fig. 3.17. The diffusivity of hydrogen species is orders of magnitude higher in the oxide than in other materials (e.g., poly-Si and SiN) from the previous study [19], consistent with the larger degradation in longer channel devices with SiN capping. Nevertheless, the extra hydrogen species also acts as the reaction precursors for the aggravated NBTI observed in devices with SiN-capping. This is consistent with the higher exponent value of devices with PE-SiN capping in the above discussions.

The above results clearly indicate that the NBTI is aggravated for devices with SiN-capping. Although the capping of a SiN layer can enhance drive current in the fresh device, NBT stress may also degrade the device performance and almost negates the benefit gained by SiN capping layer. Based on the above inference that the deposited PE-SiN layer contains a large amount of hydrogen species, the Si-H bonding is easier to break, and therefore the voluminous hydrogen species aggravate NBTI. Hydrogen is believed to be the main passivating species for Si dangling bonds, and plays a major role during NBTI stress, where Si-H bonds are de-passivated, and interface traps are formed. It is therefore important to optimize the amount of hydrogen species while retaining its compressive stress during the deposition of SiN layer. This could be accomplished by carefully adjusting the process conditions (e.g., $SiH_4/N_2/NH_3$ gas flow

rate, pressure, RF power, etc.) in PECVD systems [4], or resorting to high-density plasma CVD (HDPCVD) systems [18]. The latter approach has been shown to dramatically reduce the hydrogen content incorporated in the deposited films. This is essential to preserve the drive current enhancement while keeping the NBTI reliability characteristics at bay.

3.4 Summary

Poly-SiGe-gated PMOSFETs with local compressive strain in the channel induced by a compressive SiN-capping layer were fabricated in this study. The incorporation of the compressive SiN-capping layer is found to significantly enhance the drive current of PMOSFETs. Specifically, we observe ~ 29% and 36% drive current enhancement for the devices with SiN capping thickness of 100 nm and 300 nm, respectively, both at a channel length of 0.45 μm. Besides, the phonon scattering is a main factor for current enhancement in devices with SiN capping. Despite this much-coveted merit, our results also show that the SiN capping may aggravate the NBTI characteristics. In addition, Gm is found to be degraded gravely in the strained devices under high temperature stress, and the Gm_{max} gain in the fresh device with compressive strain is completely negated after 10000 sec of NBT stress.

The voluminous hydrogen species contained in the PE-SiN layer as well as the strain energy stored in the channel may be the culprits for the worsened reliability. Even for the devices with SiN-capping, the saturation phenomena in ΔV_{th} and ΔN_{it} are observed. This is believed to be due to the fact that nearly all the interfacial Si-H bonds have been broken. The large amount of hydrogen species as well as the channel strain effect is presumably the keys responsible for the phenomenon. Hydrogen species is believed to play a major role during NBTI stress. Care should therefore be exercised to

optimize the amount of hydrogen species to ensure that the NBTI effect is kept at bay, while simultaneously maintaining the performance enhancement characteristic of the compressive strain channel.

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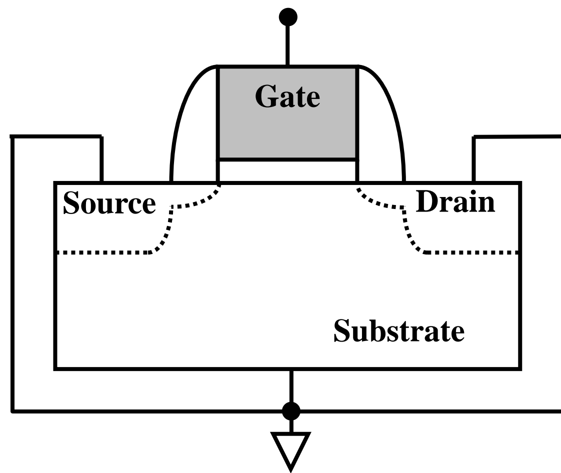
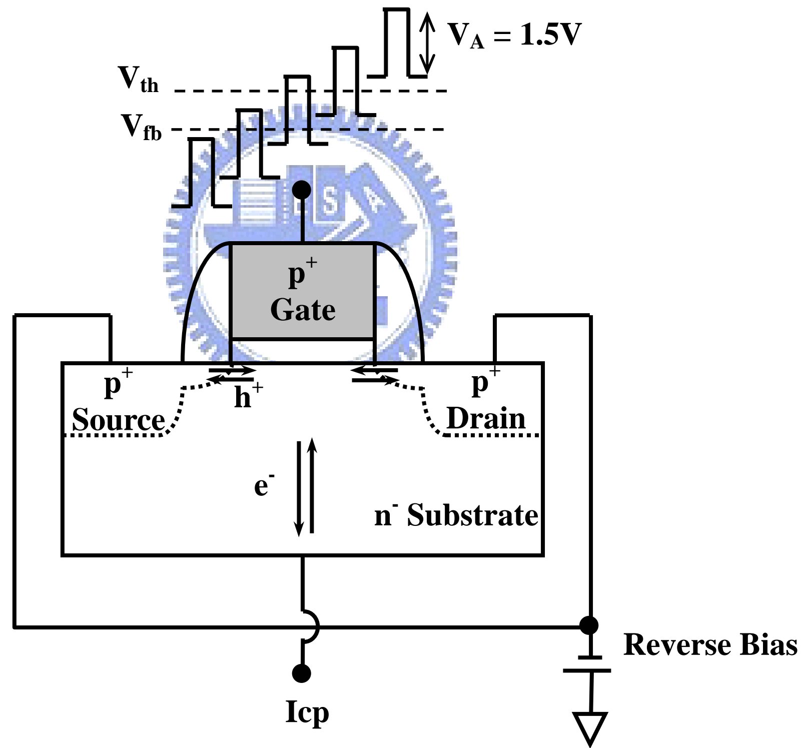
Stress: $V_G - V_{th}$ = -3.5V, -3.9V, and -4.3V



(a)



(b)

Fig. 3.1 (a) Setup of NBTI stress measurement. (b) Setup of charge pumping measurement.

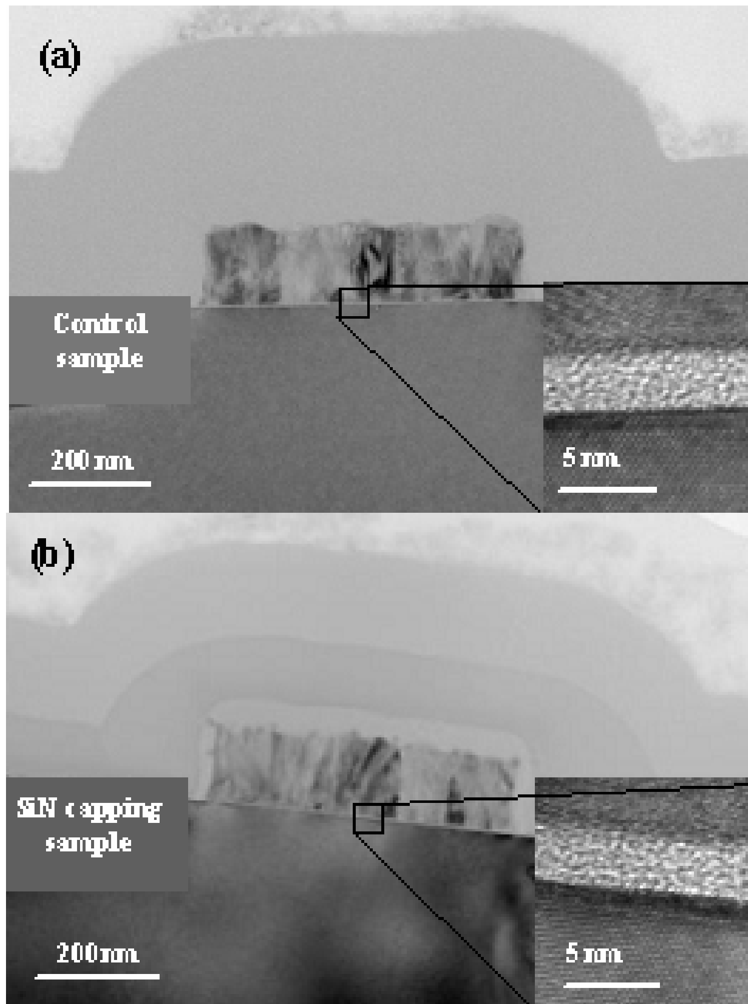


Fig. 3.2 Cross-sectional TEM pictures of devices (a) without and (b) with SiN capping layer. The two samples have nominally identical gate oxide thickness.

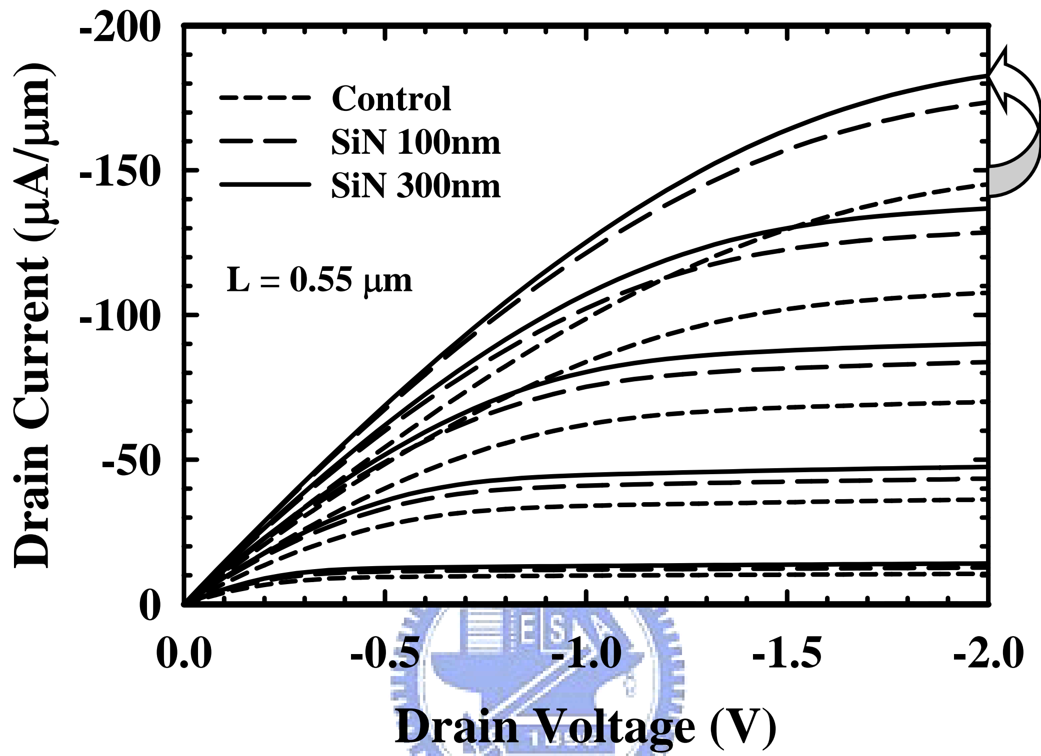


Fig. 3.3 Output Characteristics of PMOSFETs with channel length/channel width = 0.55 μm/10 μm. The drive current clearly increases with SiN-capping.

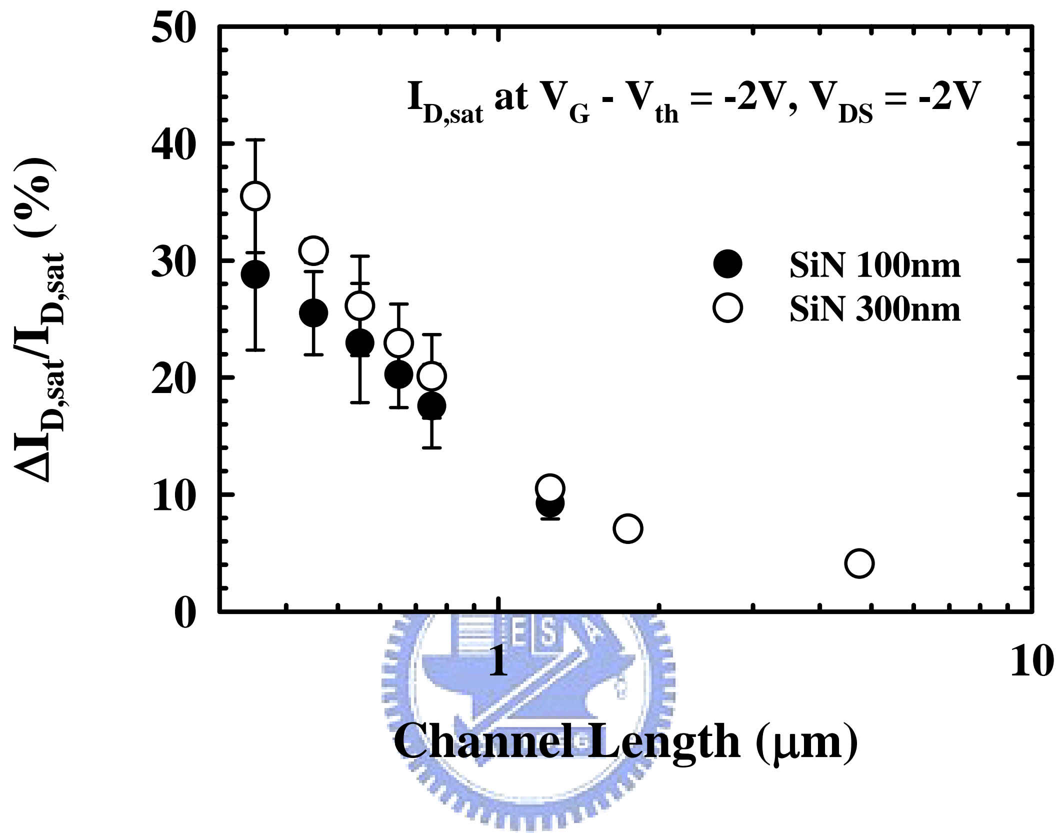


Fig. 3.4 Saturation current increase versus channel length. The saturation current was defined at $V_G - V_{th}$ = -2 V and V_{DS} = -2 V.

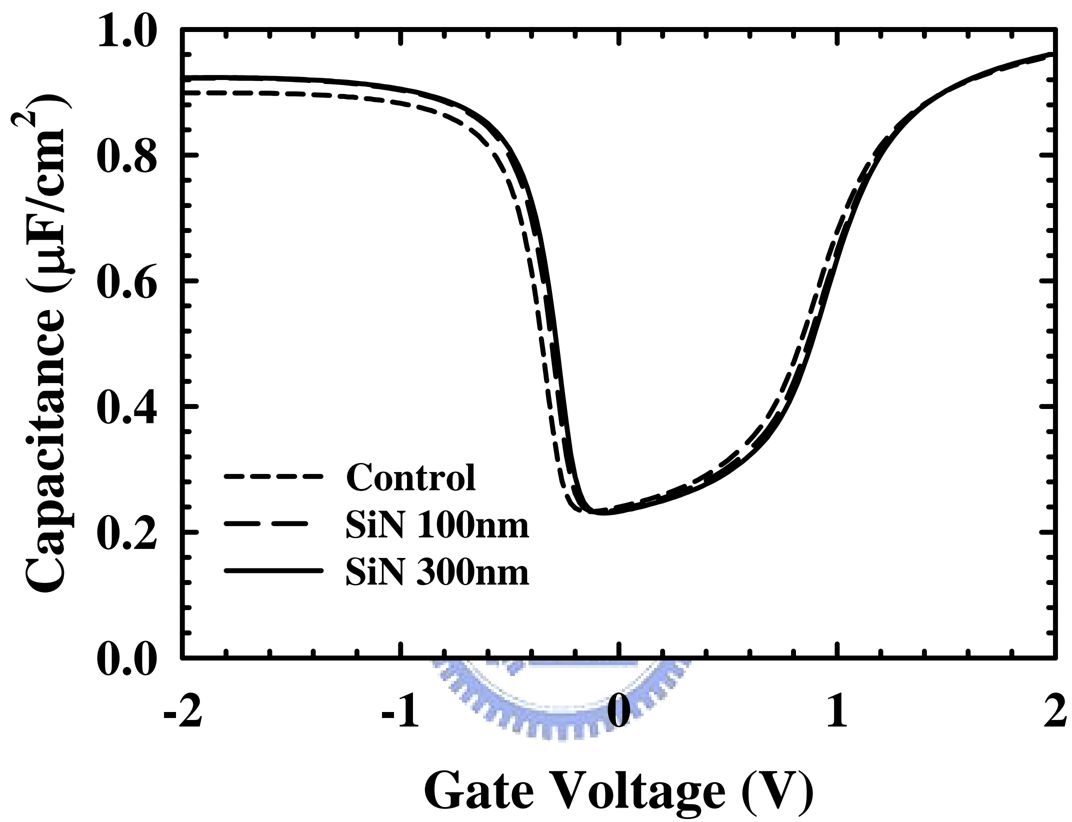


Fig. 3.5 Capacitance-Voltage (*C*-*V*) characteristics of devices with and without SiN-capping.

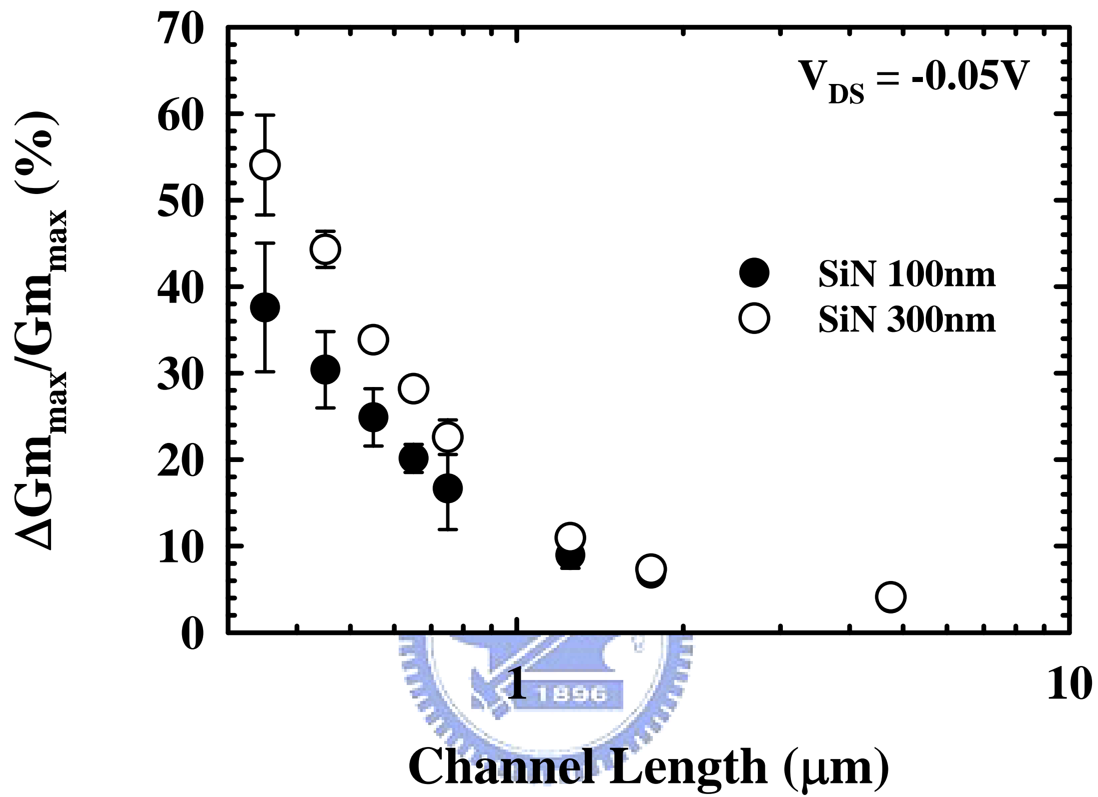


Fig. 3.6 Transconductance gain versus channel length. The transconductance was measured at V_{DS} = -0.05 V.

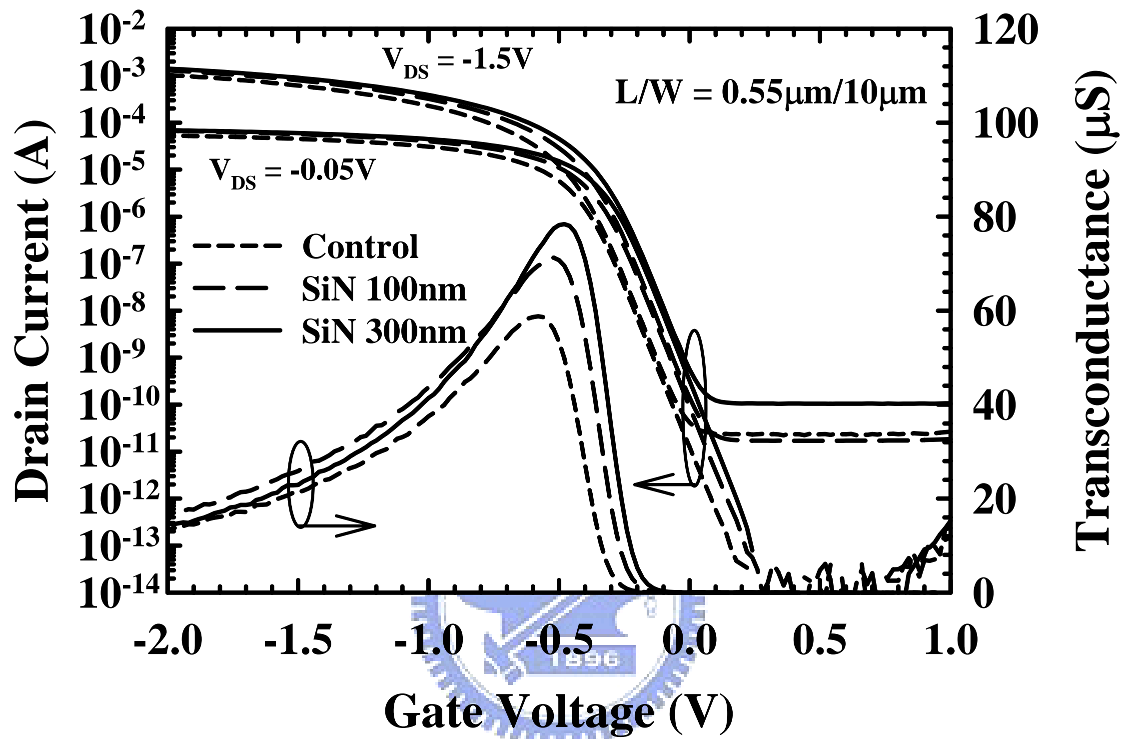


Fig. 3.7 Subthreshold characteristics and transconductance of PMOSFETs with and without SiN-capping. The subthreshold swing is nearly identical among all devices, while the transconductance is obviously larger in devices with SiN-capping.

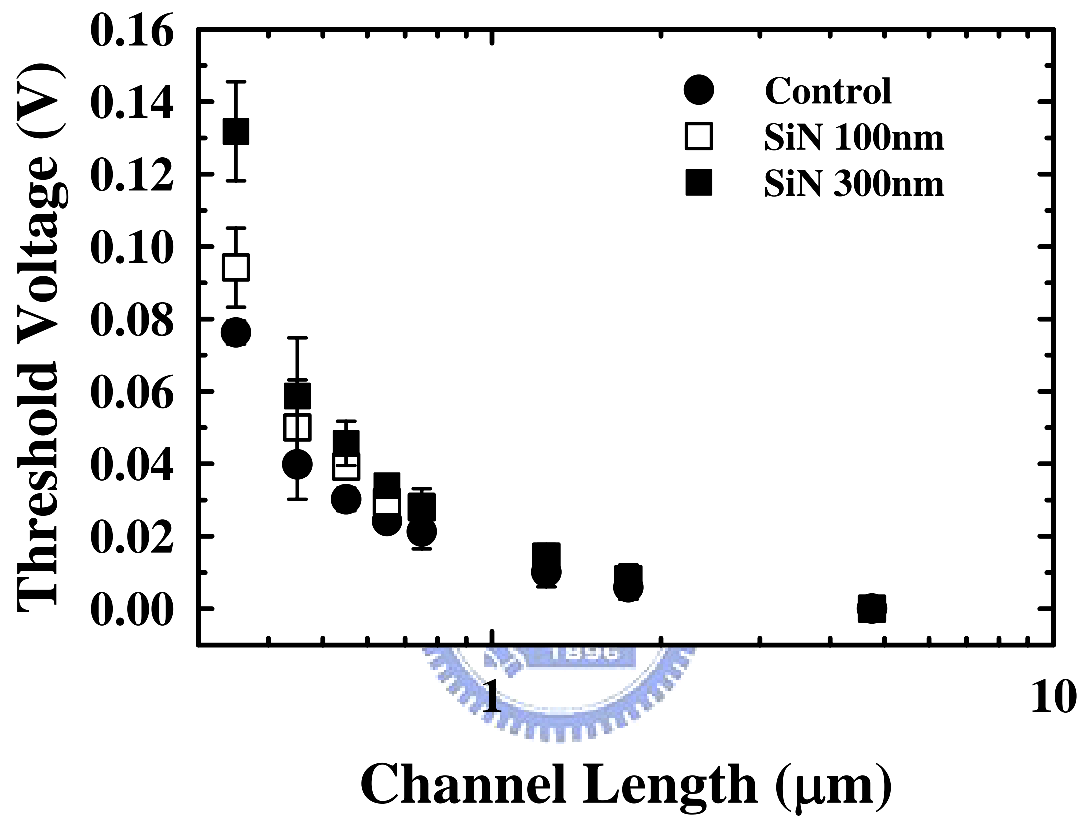


Fig. 3.8 Threshold voltage roll-off between devices with and without SiN-capping normalized to long channel devices, as a function of channel length. Devices with PE-SiN capping depict poorer roll-off characteristics.

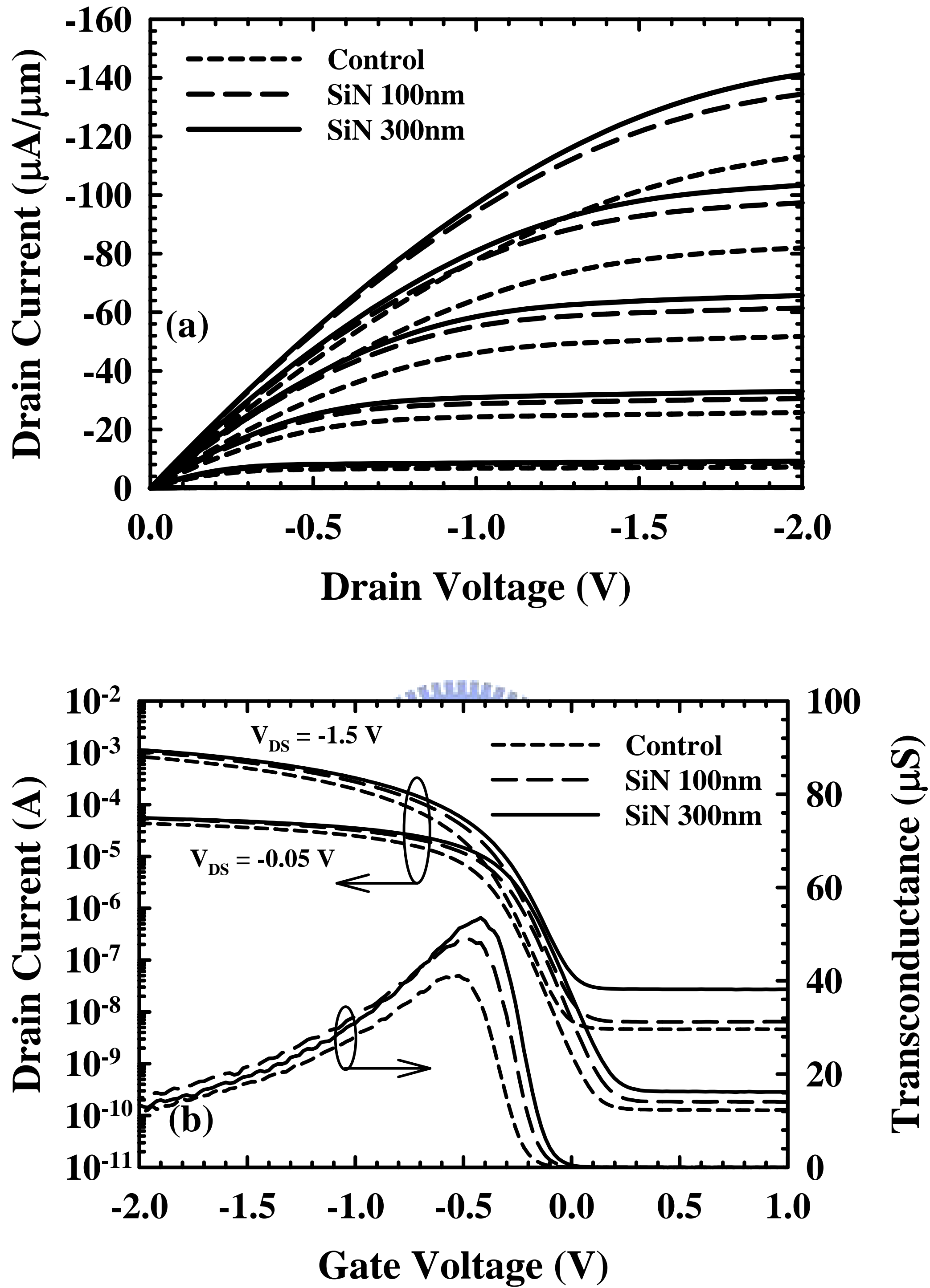
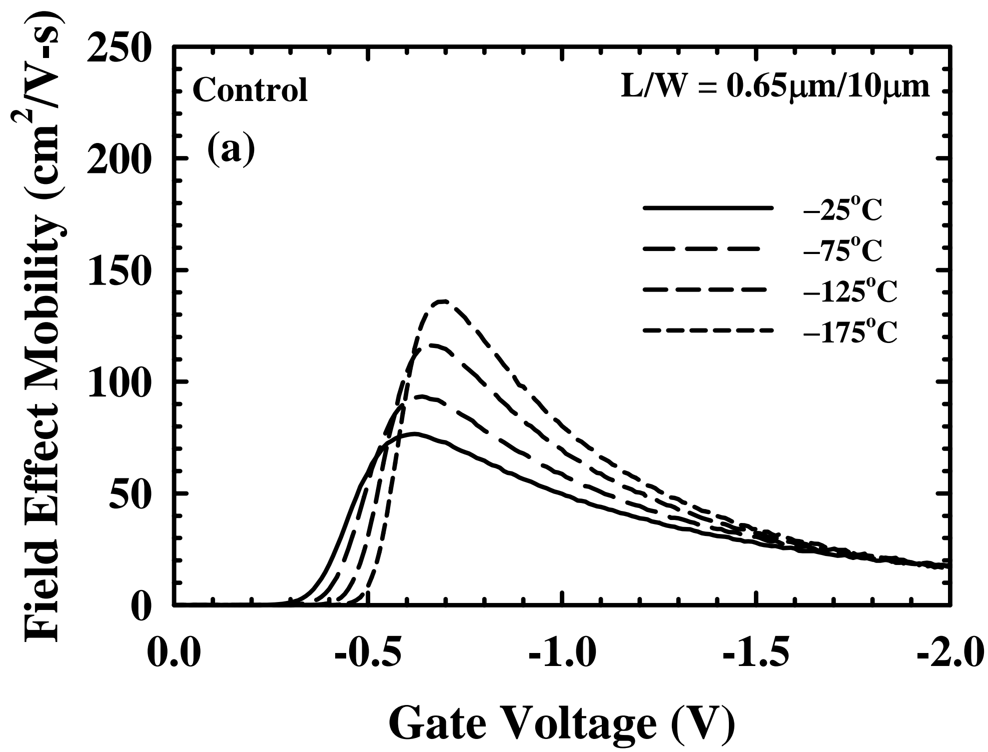


Fig. 3.9 (a) Output Characteristics of PMOSFETs with channel length/channel width = 0.55μm/10μm at 125 ˚C. (b) Subthreshold characteristics and transconductance of PMOSFETs with and without SiN-capping at 125˚C. SiN-capping layer also increases drive current and has less effect on the subthreshold characteristics at high temperature.



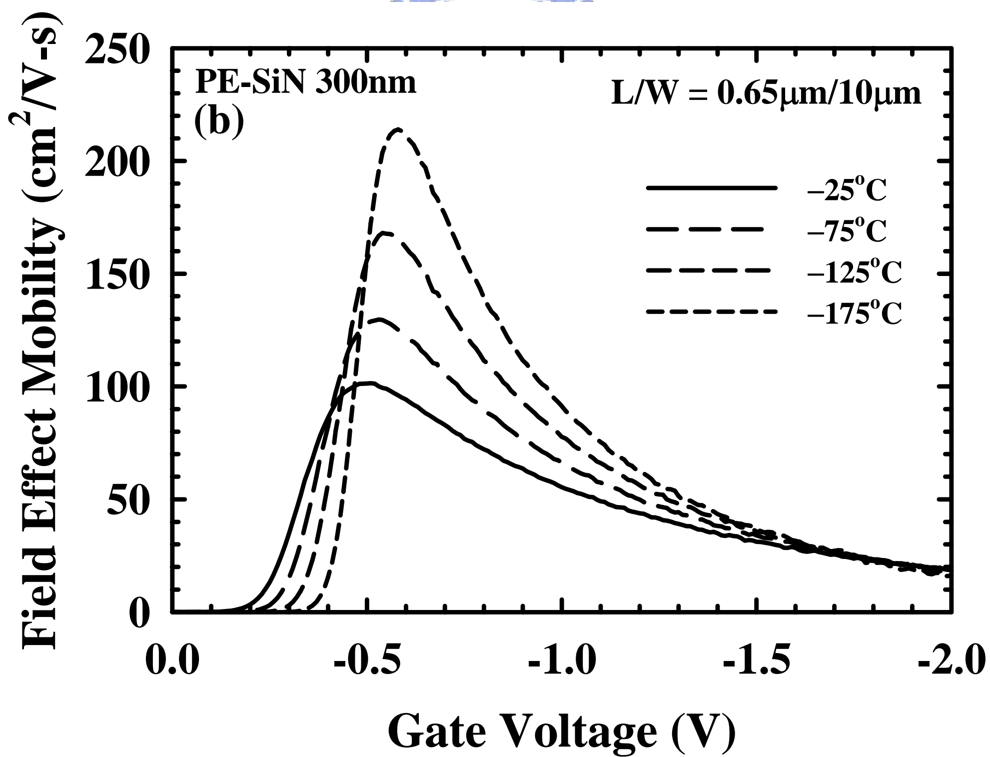


Fig. 3.10 The field-effect mobility versus gate voltage at low temperature. (a) Control samples. (b) Devices with 300nm-SiN capping.

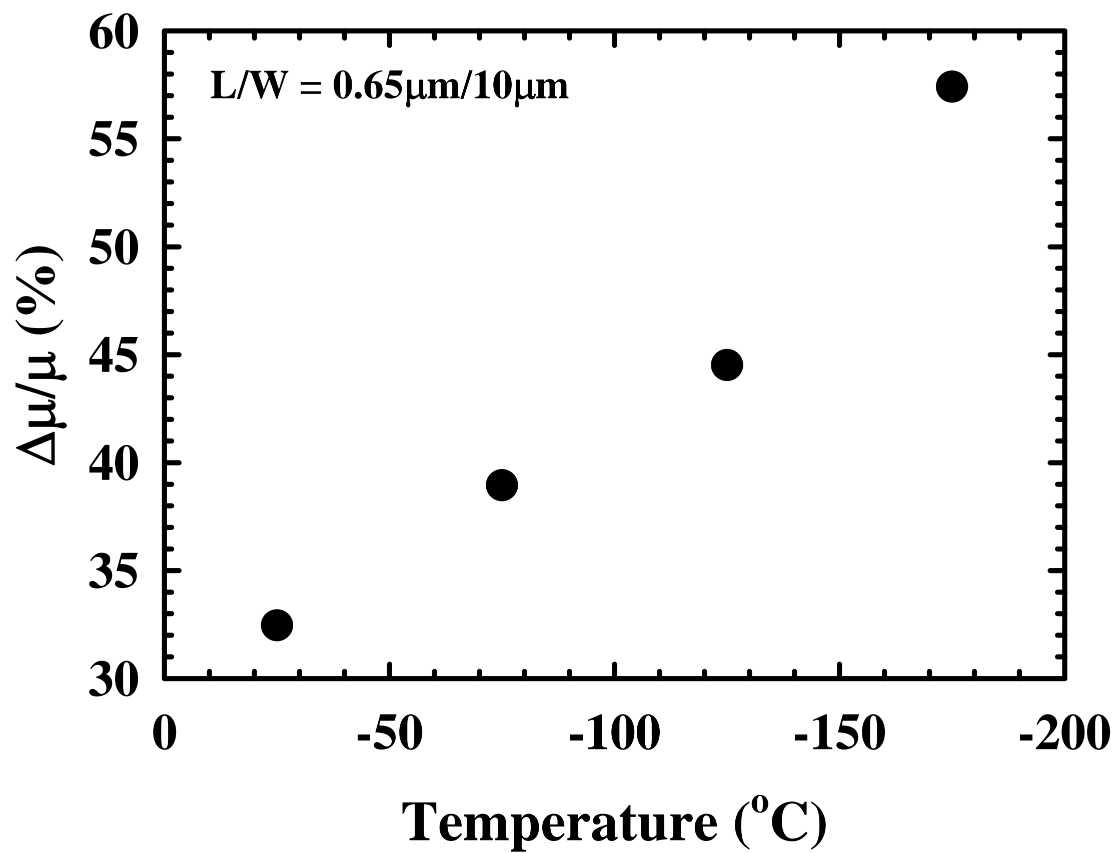


Fig. 3.11 The gain of the field-effect mobility measured at four different temperatures.

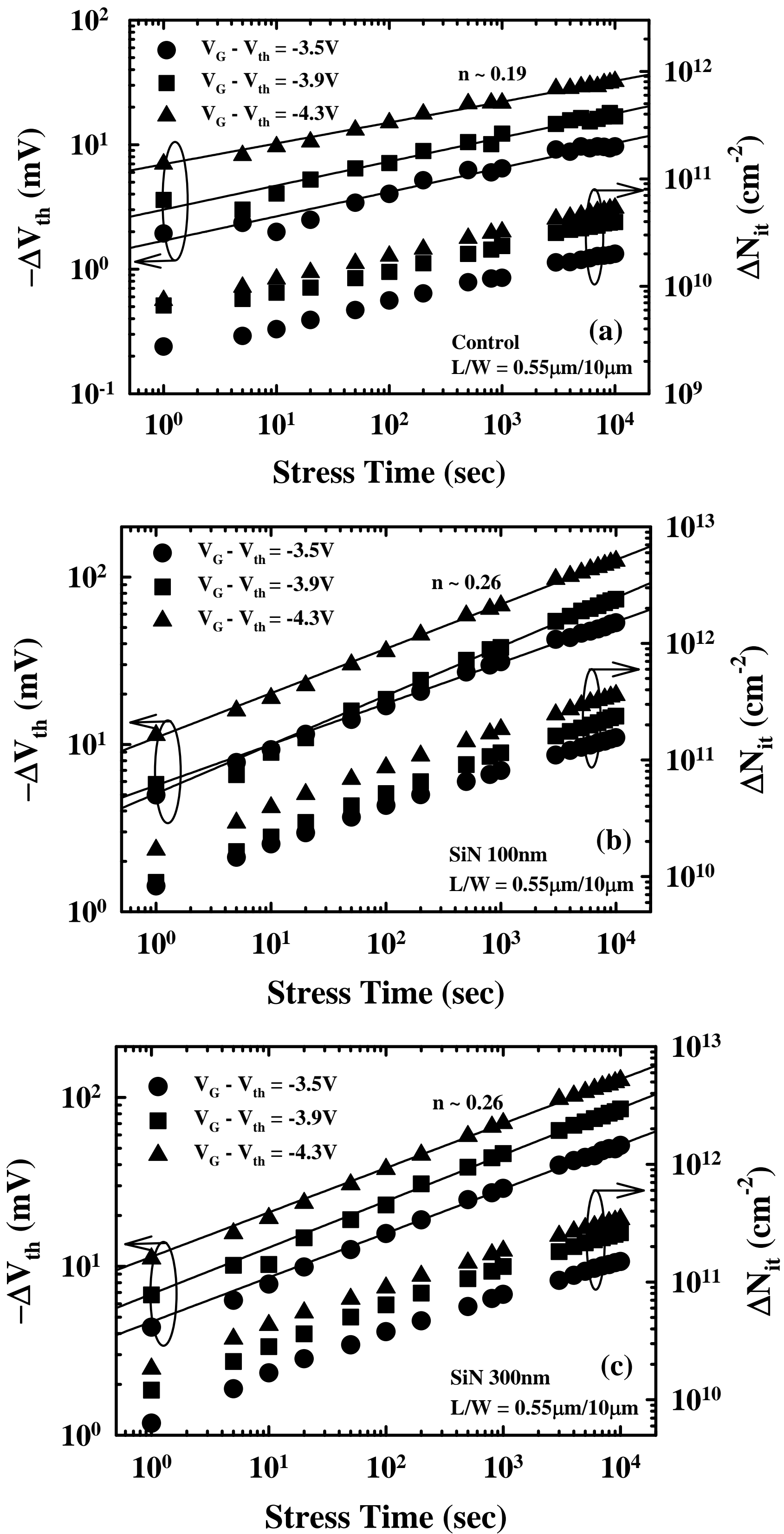


Fig. 3.12 ΔV_{th} and ΔN_{it} versus stress time biased at three different gate voltages at 25°C. (a) Control devices. (b) Devices with 100nm-PE-SiN capping. (c) Devices with 300nm-PE-SiN capping.

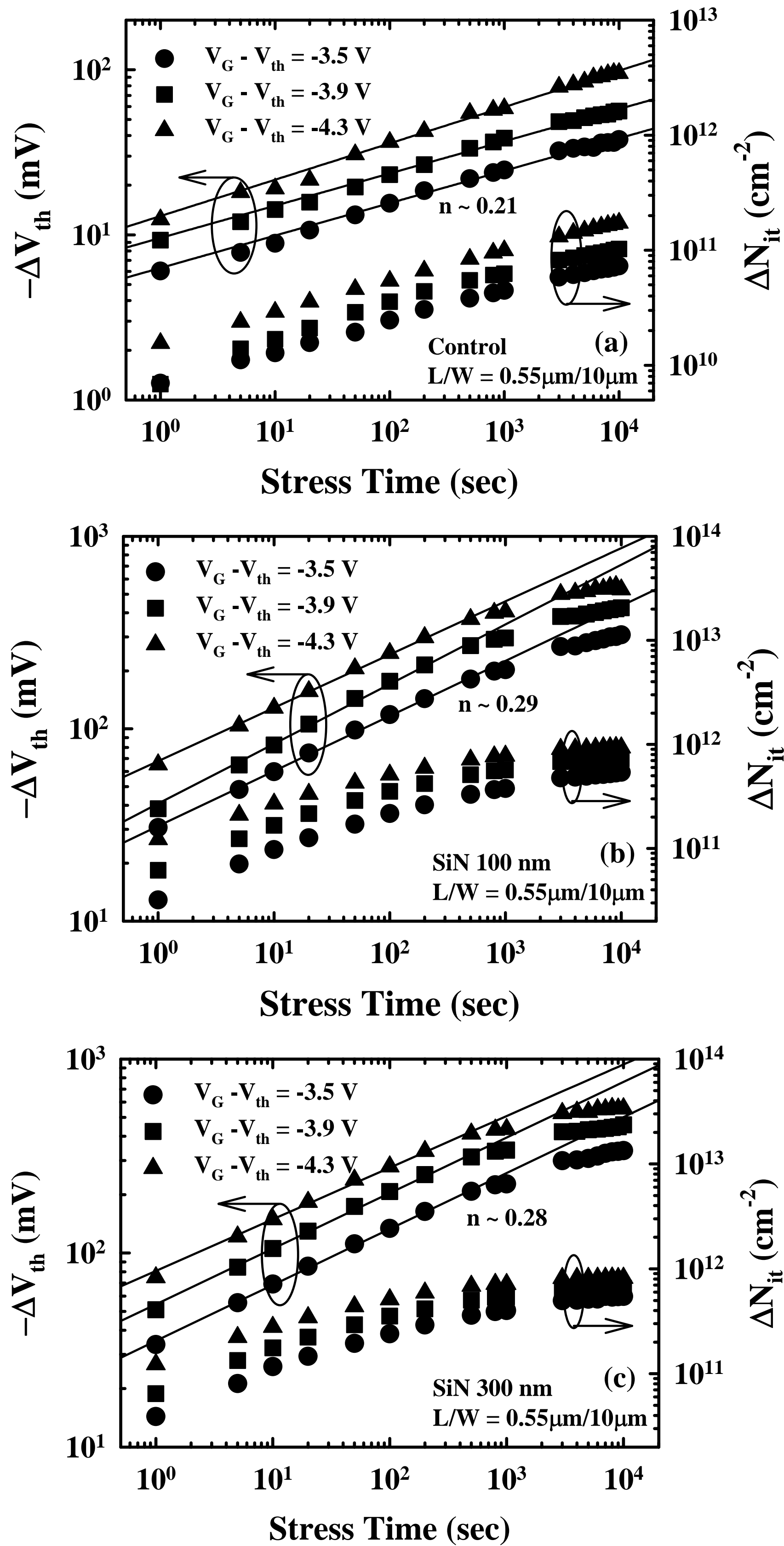


Fig. 3.13 ΔV_{th} and ΔN_{it} versus stress time biased at three different gate voltages at 125˚C. (a) Control devices. (b) Devices with 100nm-PE-SiN. (c) Devices with 300nm-PE-SiN capping.

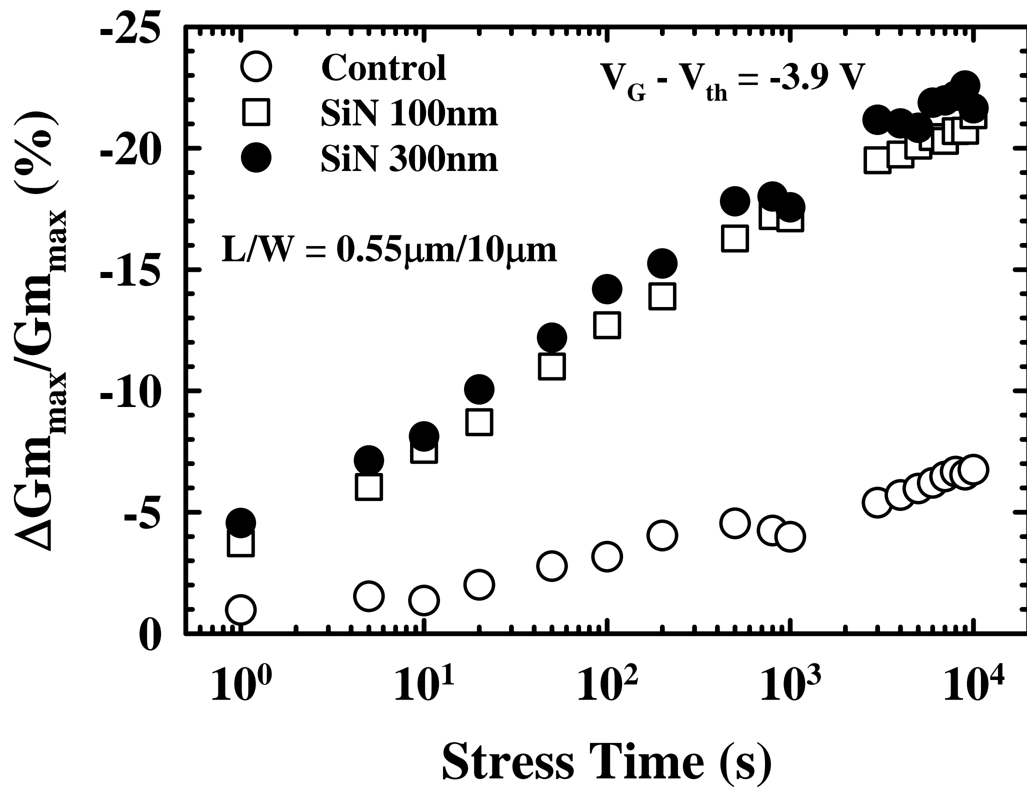
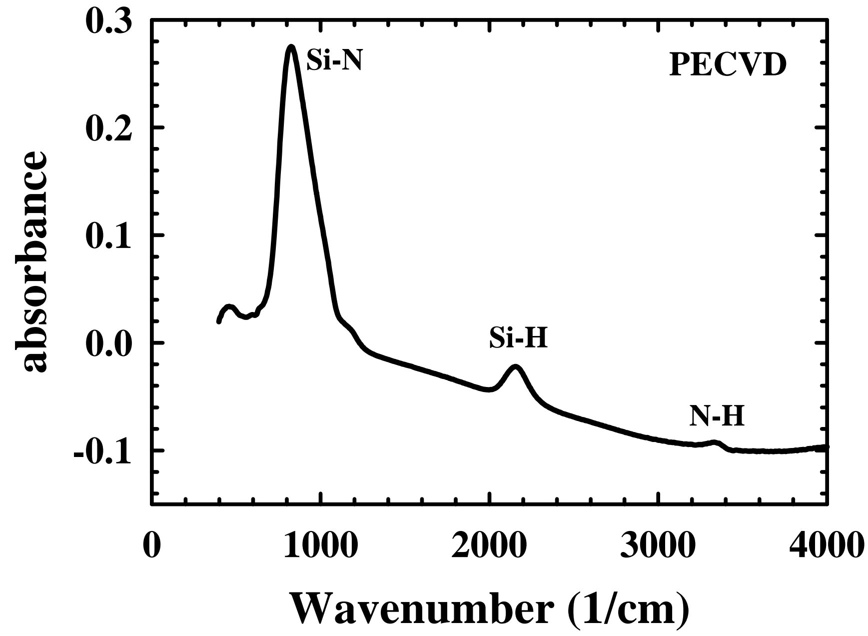


Fig. 3.14 Transconductance degradation versus stress time at 125 ˚C. Transconductance of PMOSFET with PE-SiN layer degrades gravely under NBTI stress.



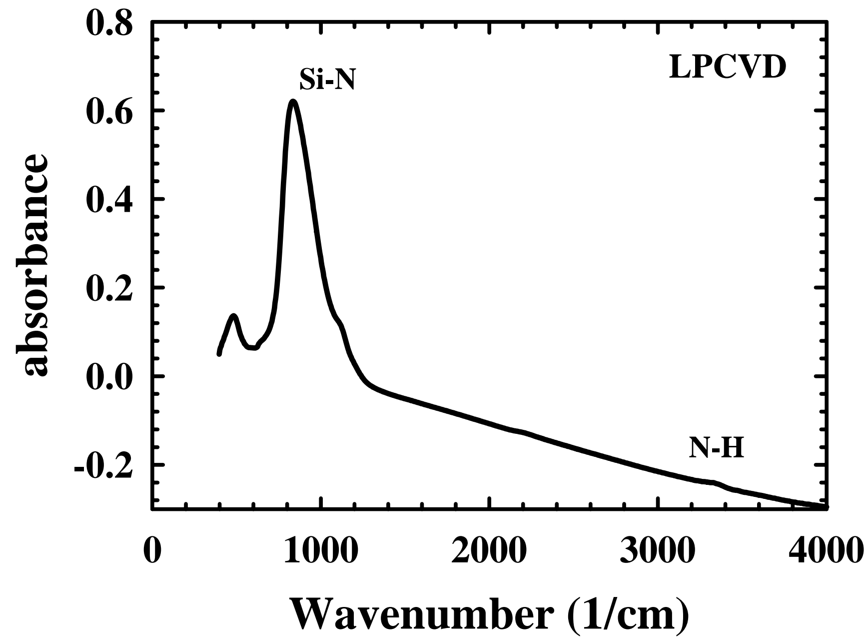
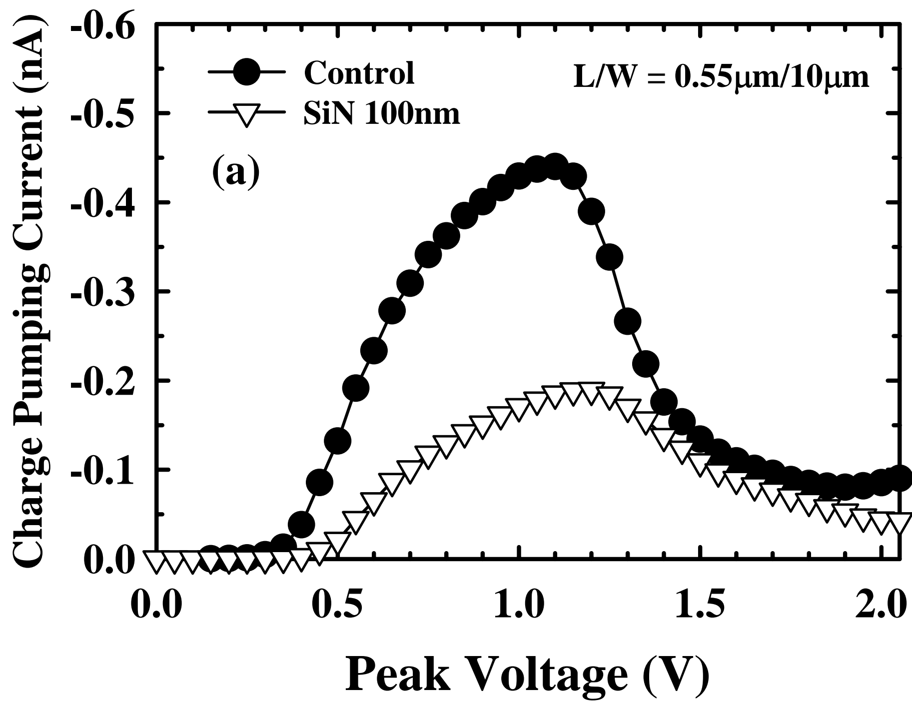


Fig. 3.15 Bonding signals of LP- and PE-SiN layers detected by Fourier transform infrared spectrometer (FTIR). PE-SiN layer depicts the extra signal pertaining to Si-H bonds.



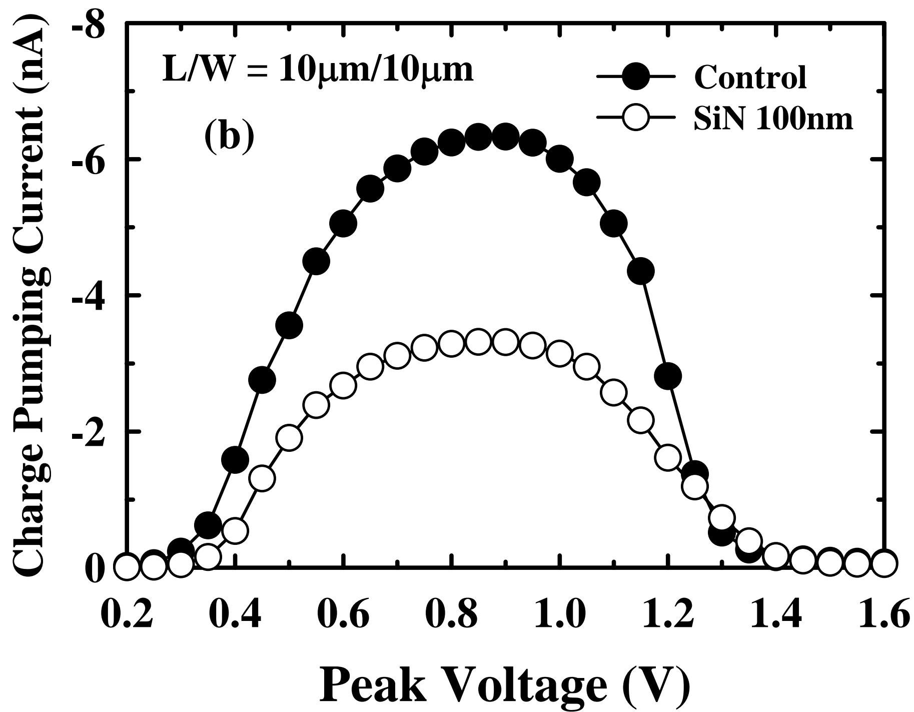
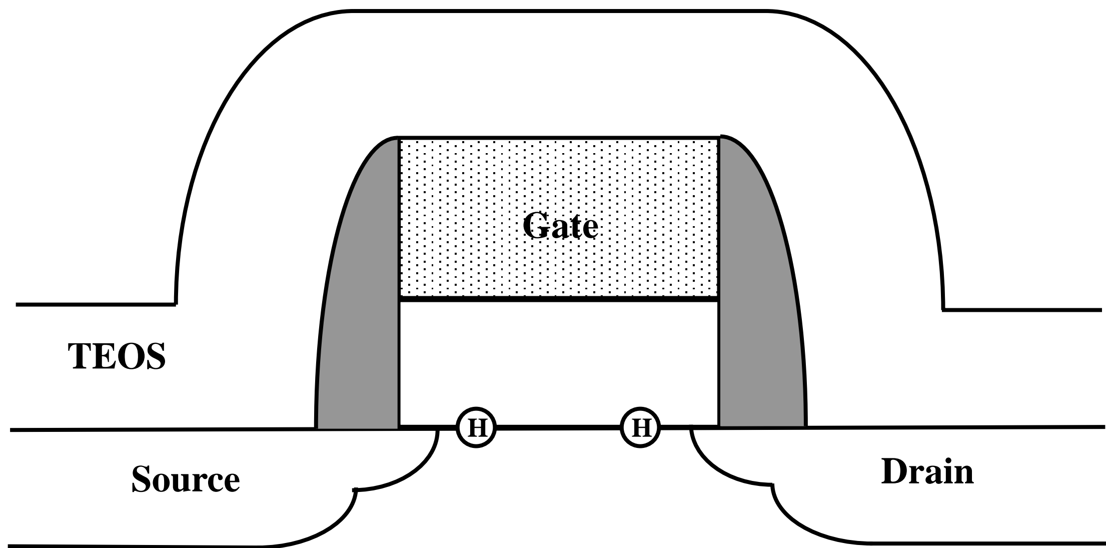
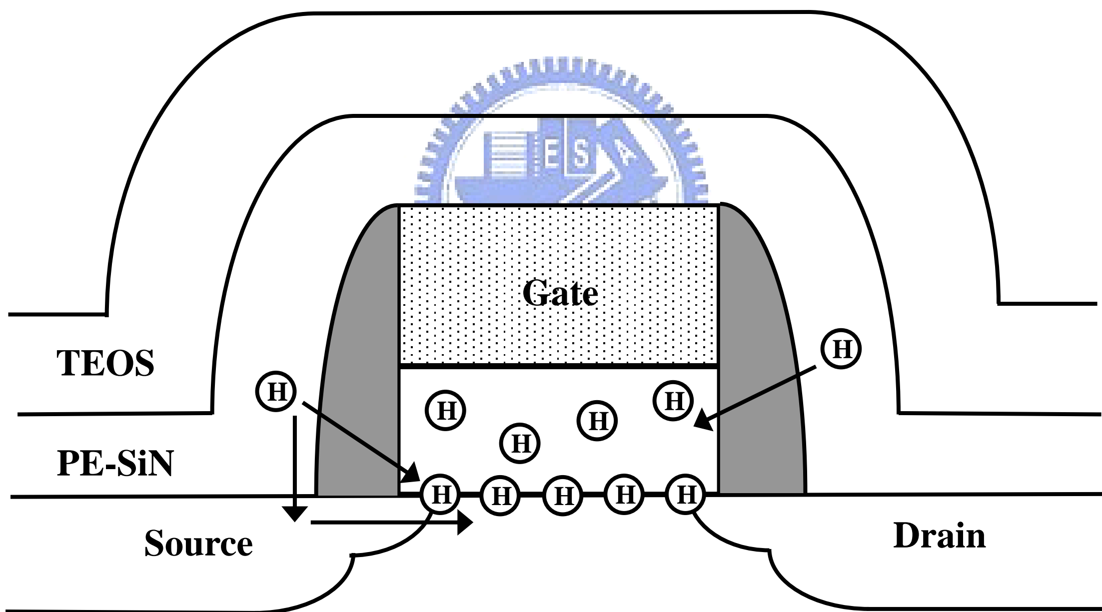


Fig. 3.16 Charge pumping current of fresh devices with and without PE-SiN capping. (a) L = 0.55 μm. (b) L = 10 μm.



(a)



(b)

Fig. 3.17 (a) In control devices, hydrogen species mainly locate at the interface to passivate the interface states. (b) In SiN-capping devices, a large amount of hydrogen species from the SiN layer diffuse to the gate oxide layer and the Si/SiO_2 interface.

Chapter 4

Dynamic and Frequency-Dependent NBTI Characteristics of PMOSFETs with PE-SiN Capping

4.1 Introduction

Recently, mobility enhancement by channel strain engineering has emerged as an effective approach to boost the performance of scaled devices, especially local-strain technology [1-5]. A method to introduce compressive strain to the channel of PMOSFETs is to add a SiN capping layer deposited by plasma-enhanced CVD (PECVD) [1,2]. Though strained channel could enhance the mobility and thus the drive current of the device, potentially it could also compromise the device's reliability characteristics. From the results presented in Chapter 3, hydrogen species unintentionally incorporated in the thin stress-booster film may also adversely affect the device reliability characteristics. The device reliability issue is therefore a potential concern when the local strain is introduced, and should therefore be carefully addressed.

Negative bias temperature instability (NBTI) is well known as the lifetime-limiting reliability concerns in CMOS devices when the gate oxide thickness is scaled to 3.5 nm and below [6]. Conventionally, characterization of NBTI is primarily based on static experimental data. However, for real-life operations of digital circuits, the applied bias to the gate of PMOSFETs in a CMOS inverter is being switched between "high" and "low" voltages incessantly. In line with this, the evaluation of the dynamic NBTI (DNBTI) characteristics seems to be more practical for reliability characterization. In this aspect, it has been reported that the dynamic NBTI (DNBTI) effect greatly prolongs the lifetime of PMOSFETs operating in a practical digital circuit [7]. A physical model

has also been previously proposed for DNBTI involving the interaction of the released hydrogen re-passivating Si dangling bonds during the passivation time [8]. However, reports on DNBTI of devices with SiN capping are lacking. In this work we investigate the issue by performing dynamic and AC stress measurements on PMOSFETs with a compressively strained channel.

4.2 Experimental

The PMOSFETs in this study were fabricated on 6-in n-type Si wafers with conventional local oxidation of silicon (LOCOS) isolation. Gate oxide with a thickness of 3 nm was grown in a vertical furnace in O_2 at 800 ˚C. After gate oxide growth, a 150 nm poly-SiGe layer was deposited by LPCVD, followed by standard plasma gate-etch process to form the patterned gate. Afterwards, standard procedures were applied to form TEOS spacer and S/D junctions. A SiN layer of 100 nm (and/or 300nm) and a TEOS passivation layers were then deposited in turn by a PECVD system. Contact holes and metallization processes were subsequently performed. Finally, the processing is completed with a forming gas anneal at 400˚C. Electrical characterizations were performed using an HP4156 system. Setups of measurements are showed in Fig. 4.1. DNBTI stress measurements were also performed in this study. For DNBTI measurements (Fig. 4.1(b)), alternant "stress" and "passivation" modes, both with a period of 2000 sec, were performed on the devices. The source, drain, and substrate electrodes were all connected to ground during the measurement, while the gate bias was applied with –4 V and 0 V (and/or 1 V) in stress and passivation periods, respectively. Interface traps were evaluated using charge pumping method with a fixed amplitude of 1.5 V at 1 MHz. We have also performed the measurements with applied frequencies ranging from 1 kHz to 1 MHz, and found that the measured charge pumping

current (Icp) showed essentially a linear dependence on the frequency. Based on the results we conclude that interface states are mainly responsible for the Icp.

4.3 Results and Discussion

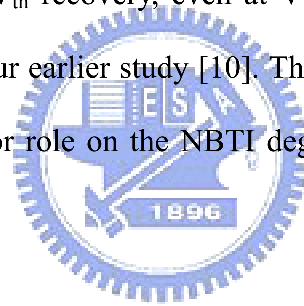
4.3-1 Dynamic NBTI Characteristics

It was shown in Chapter 3 that the deposited PE-SiN film tends to enhance the drive current, and the improvement becomes more significant as the devices become shorter. This is a reasonable trend since the uniaxial strain level increases with decreasing channel length. Specifically, 29 % and 36 % improvements in drive current could be reached for the devices with SiN capping thickness of 100 nm and 300 nm, respectively, both at a channel length of 0.45 μm [6].

Figures 4.2(a) & (b) depict DNBTI results in devices with and without SiN capping, respectively. Under the same stress condition, the device with SiN capping layer also depicts larger ΔV_{th} and ΔN_{it}. It is also noted that ΔN_{it} saturates in the case of the SiN capping devices when the stress time exceeds 2000 sec (i.e., the first stressing period), as shown in Figs. 4.2(b) & (c). During the second and third stressing periods, the peak values remain almost unchanged. According to the analysis performed in previous chapter, this could be explained by the fact that nearly all Si-H bonds have been broken after certain stress time (e.g., 2000 sec). Despite the saturation of ΔN_{it}, ΔV_{th} continues to reach higher peaks during subsequent stressing periods, as shown in Figs. 4.2(b) & (c), indicating the existence of an unaccounted contributor to the NBTI degradation and recovery processes. In addition, it is obviously seen that the peak value of ΔV_{th} increases with stressing period in Fig. 4.2. The fixed charges contribute to ΔV_{th} besides interface state. In devices with SiN capping, the amount of generated fixed-charges are significantly due to the extremely high amount of hydrogen incorporation in the gate

oxide, as shown in Fig. 3.17 (in Chapter 3).

Some of the results are normalized and shown in Fig. 4.3. Threshold voltage is essentially fully recovered for the strained devices, as shown in Fig. 4.3(a). The dependence of recovery in ΔV_{th} on V_P (i.e., the passivation voltage) indicates the contribution by some charged species. We can also see that the amount of V_{th} recovery is higher for passivation voltage (V_P) of 1 V. But the dependence of ΔN_{it} on V_P is negligible, as shown in Fig. 4.3(b). This observation strongly suggests that the neutralization of trapped holes in the oxide [9], in addition to the re-passivation of interface states, occurs in the recovery period for the strained devices. Although ΔN_{it} in the strained devices is independent of V_P, the recovery in ΔN_{it} still represents the most significant contributor to the V_{th} recovery, even at V_P of 1 V. This is consistent with static stress results shown in our earlier study [10]. The results also suggest that neutral hydrogen species plays a major role on the NBTI degradation and recovery processes [11].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4.3-2 Effect of Stress Frequency

We have also investigated the effect of AC stress frequency on these devices. Figure 4.4 shows ΔV_{th} for devices, both with and without SiN capping, that were stressed at four different frequencies, all with 50 % duty cycle. The amplitude of AC signal was $|V_{th}| + 4$ V (from $V_G - V_{th} = -4$ V to $V_G = 0$ V). From Fig. 4.4, it is clearly seen that the interface state creation shows only weak frequency dependence for the control devices. In reference to the analysis in previous reports [9, 12], this observation is reasonable. In contrast, the strained devices depict strong frequency dependence on both ΔV_{th} and ΔN_{it}. Moreover, it is noted that the exponent values of ΔN_{it} is slightly larger than that of ΔV_{th} for both the control and SiN-capping devices. This is consistent

with [13] that not only interface state but also oxide charge are generated in MOSFETs under NBTI stress.

Such frequency dependence is further evidenced in Fig. 4.5, in which the shifts in ΔV_{th} and ΔN_{it} after 5000 sec stress are plotted as a function of stress frequency. It can be seen that both ΔV_{th} and ΔN_{it} are strongly dependent on the stress frequency for the strained devices. Specifically, ΔV_{th} decreases from 214 mV to 94.2 mV for the device with 100nm SiN-capping, and from 242.3 mV to 103.6 mV for the device with 300nm SiN-capping, when the stress frequency increases from 1 kHz to 1 MHz. These observations are explained as follow: the excess hydrogen species coming from the SiN capping layer would diffuse to the oxide/Si interface, as inferred in the above discussion. The breaking of the excess hydrogen-related bonds during stressing would contribute to the generation of interface states and leads to a higher exponent value. Nevertheless, the bond breaking process needs sufficient stress time to trigger, resulting in the significant frequency dependence.

Figure 4.6 compares the device transconductance (Gm), fresh and after subjecting to 5000 sec of DC or AC stress. It is obvious that the differences between the DC and AC stress samples are marginal in the control devices. On the other hand, despite the significant enhancement in Gm in fresh devices with SiN capping, the degradation under DC stress is grossly aggravated. In other words, the benefit of using channel strain is negated under DC NBT stress. Nevertheless, such restriction is greatly relieved under AC stress, especially when the frequency is high.

4.3-3 Effects of Channel Length and PE-SiN Layer Thickness

From the above discussions, we have confirmed the effect of hydrogen species under the NBTI stress. Next, the relationship of channel length and NBTI will be

addressed below. Figure 4.7 shows ΔV_{th} of the stressed samples versus channel length after 500 sec DC stress or AC stress (1 MHz). In the figure, it is clearly seen that the use of PE-SiN capping may result in aggravated NBTI, although the device degradation could be largely reduced at high stress frequency. Moreover, it is seen that the ΔV_{th} slightly increases with decreasing channel length in the SiN-capping devices. In the long-channel devices (i.e., L = 10 μm), although the channel strain induced by the SiN is negligible (referred to Fig. 3.4 in Chapter 3), the NBTI degradation is still larger in the SiN-capped devices than that in the control devices. This again implies that the diffusion of the excess hydrogen species from the PE-SiN is mainly responsible for the aggravated NBTI characteristics. In fact, a larger ΔV_{th} was observed for the devices with gate length shorter than 0.1 micron [14]. This phenomenon is not clear in our case due to the rather longer channel length.

The charge pumping current of the fresh device with SiN capping is slightly smaller than that of the control sample, as shown in Fig. 4.8. This is ascribed to the fact that hydrogen can effectively passivate the dangling bonds at the SiO_2/Si interface, and leads to a lower interface state density for the as-fabricated devices with SiN-capping. Nevertheless, the extra hydrogen species also act as the reaction precursors for the aggravated NBTI observed in devices with SiN-capping. Moreover, note that for samples with 300nm SiN capping, the largest drive current enhancement (see Fig. 3.4 in Chapter 3) and the smallest charge pumping current (Fig. 4.8) are simultaneously realized. These findings mean that a larger channel strain and higher amount of hydrogen species are simultaneously contained in the devices with 300nm SiN capping. As the thickness of SiN layer increases, NBTI stress would aggravate devices performance. Higher SiN strain energy stored in the channel may also play a role on the aggravated degradation process [15], which may weaken Si-N, Si-O, and Si-Si bonds

near the SiO_2/Si interface. However, more efforts are required to fully understand details about this mechanism.

4.4 Summary

PMOSFETs with uniaxial strain in the channel induced by a compressive SiN-capping layer were fabricated in this study. Our results show that the SiN capping may aggravate the NBTI characteristics. Devices with SiN capping show larger recovery of ΔV_{th} and ΔN_{it} than those without capping. The recovery of the generated interface states in the SiN capping device is not sensitive to the passivation voltage during stressing, indicating that neutral hydrogen species are mainly responsible for the phenomena. However, a strong dependence on the AC stress frequency is observed for the devices with SiN capping. Our observation reveals an important message that the aggravated NBTI in the devices with SiN capping could be largely alleviated by high frequency operation, especially for GHz. In addition, ΔV_{th} increases with decreasing channel length in the SiN-capping devices. This implies that diffusion of the excess hydrogen from the PE-SiN is mainly responsible for the aggravated NBTI characteristics. The large amount of hydrogen species contained in the PE-SiN layer is the main culprit responsible for the worsened reliability.

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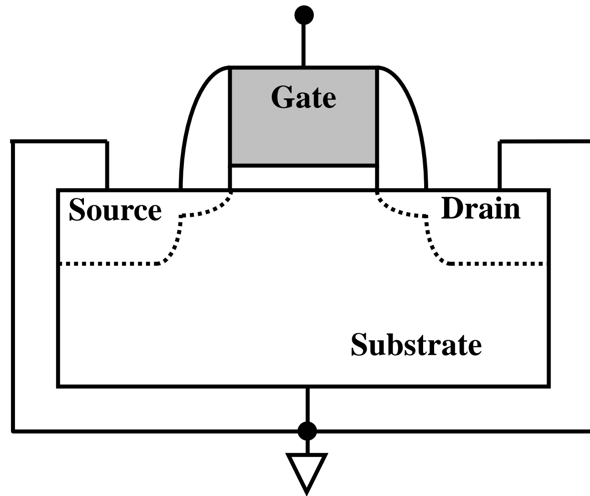
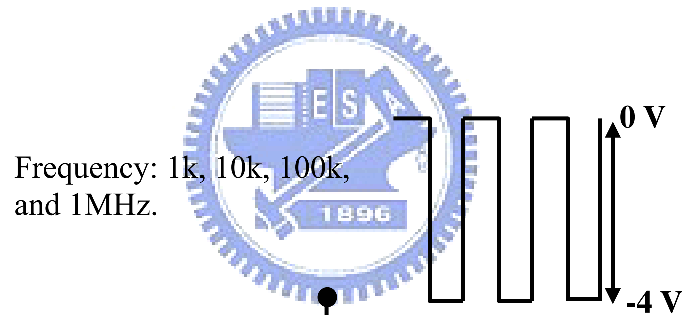
carrier-transport enhanced pMOSFET with performance boosters", in *IEDM Tech. Dig.*, 2005, p.692-695.

Stress: $V_G - V_{th}$ = -4 V (2000 sec)
Relaxation: V_G = 0 (or 1) V (2000 sec)



(a)



(b)

Fig. 4.1 Measurement setups for (a) Dynamic NBTI stress and (b) AC NBTI stress.

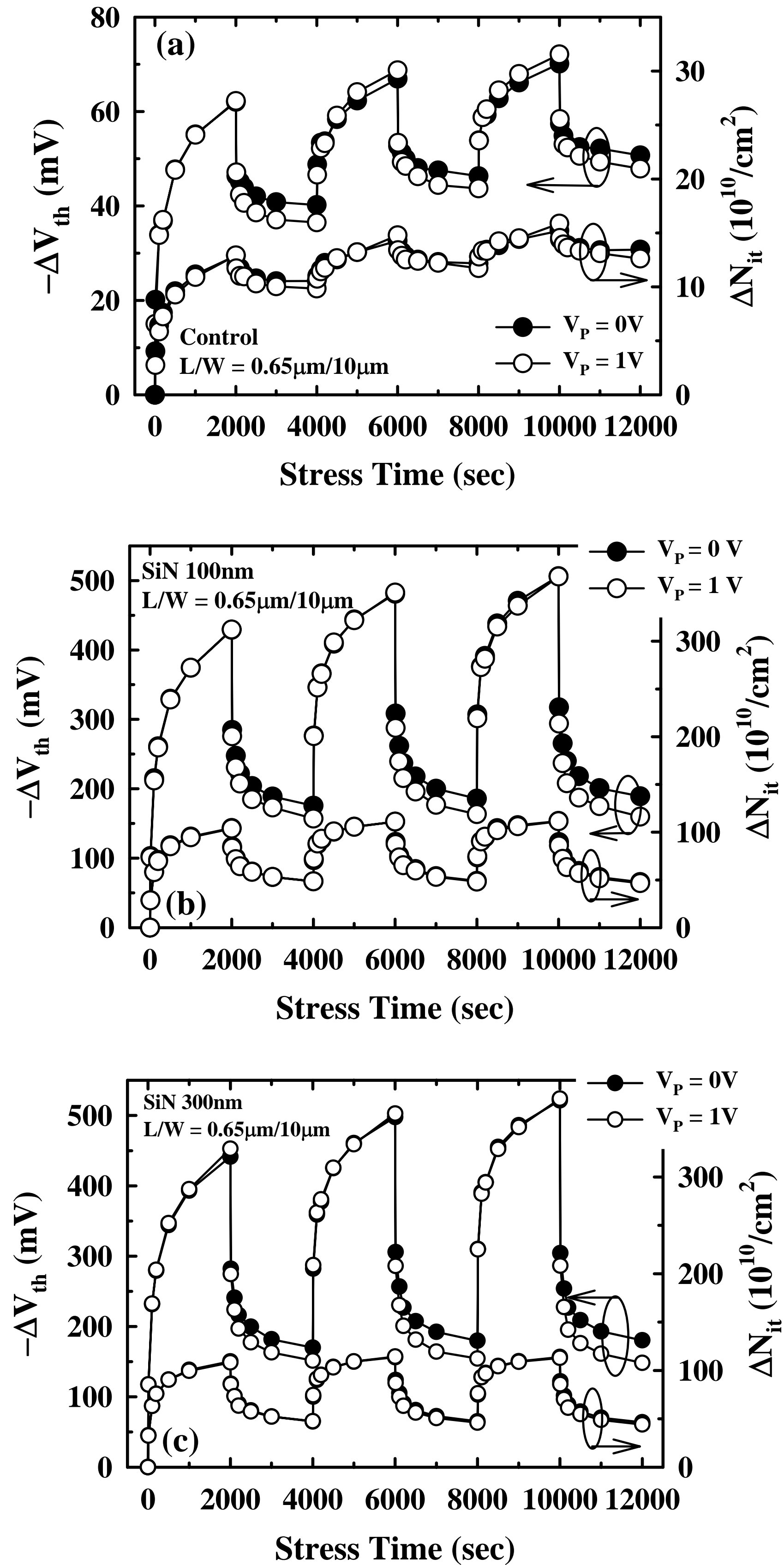
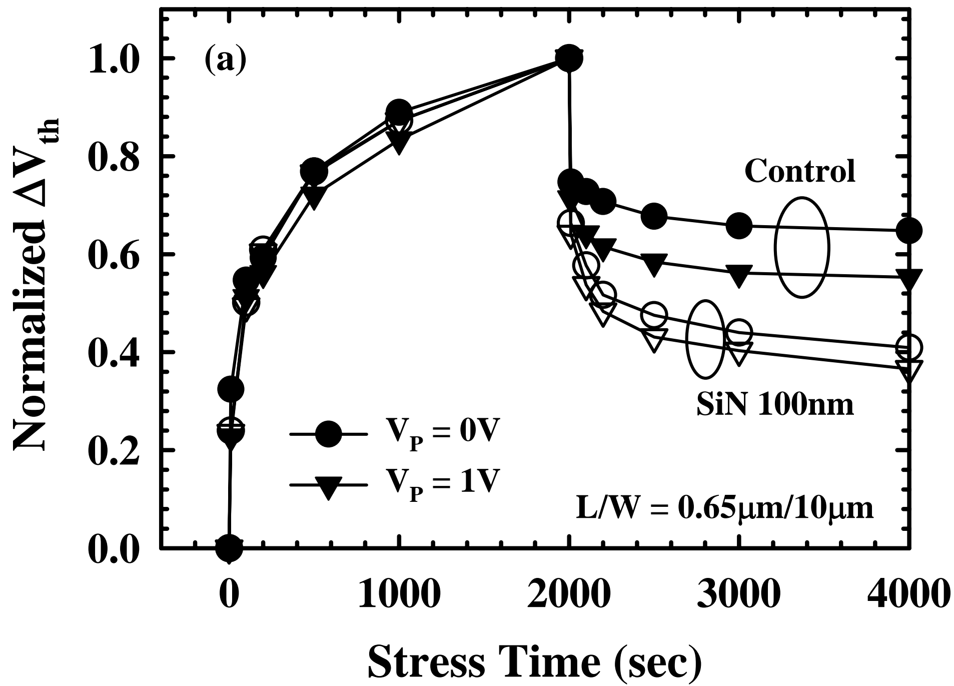


Fig. 4.2 DNBTI characteristics of (a) control samples, (b) samples having 100 nm PE-SiN capping, and (c) samples having 300 nm PE-SiN capping. Stress and passivation voltage are $V_G – V_{th}$ = - 4 V and V_G = 0 V (or 1 V) at 125°C, respectively.



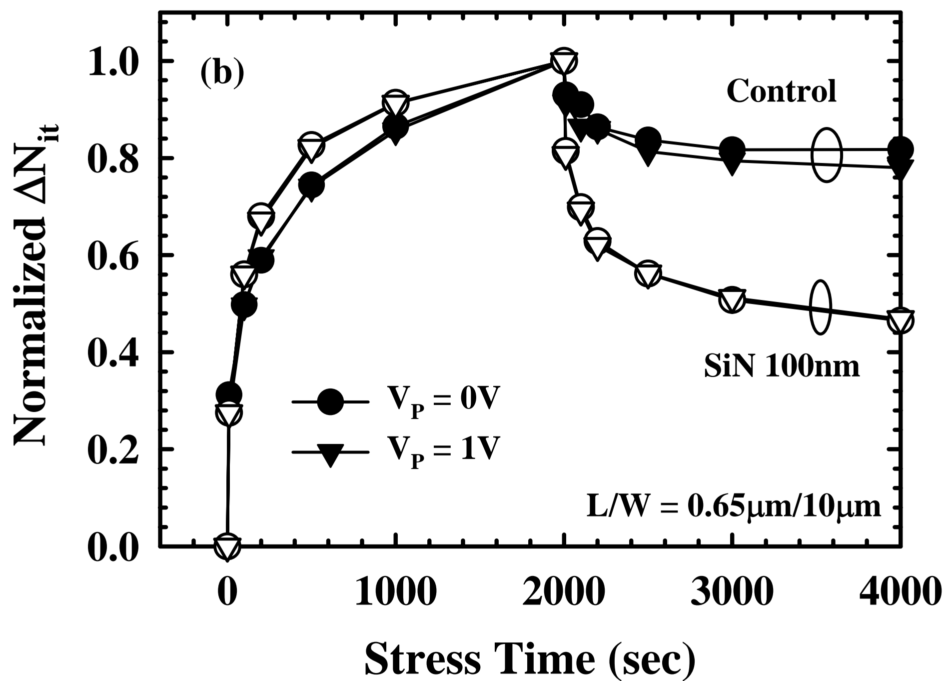


Fig. 4.3 Normalized ΔV_{th} and ΔN_{it} versus stress time. (a) Recovery behavior of ΔV_{th} in the control and SiN capping devices under V_P = 0 and 1 V. (b) Recovery behavior of ΔN_{it} in the control and SiN capping devices under V_P = 0 and 1 V.

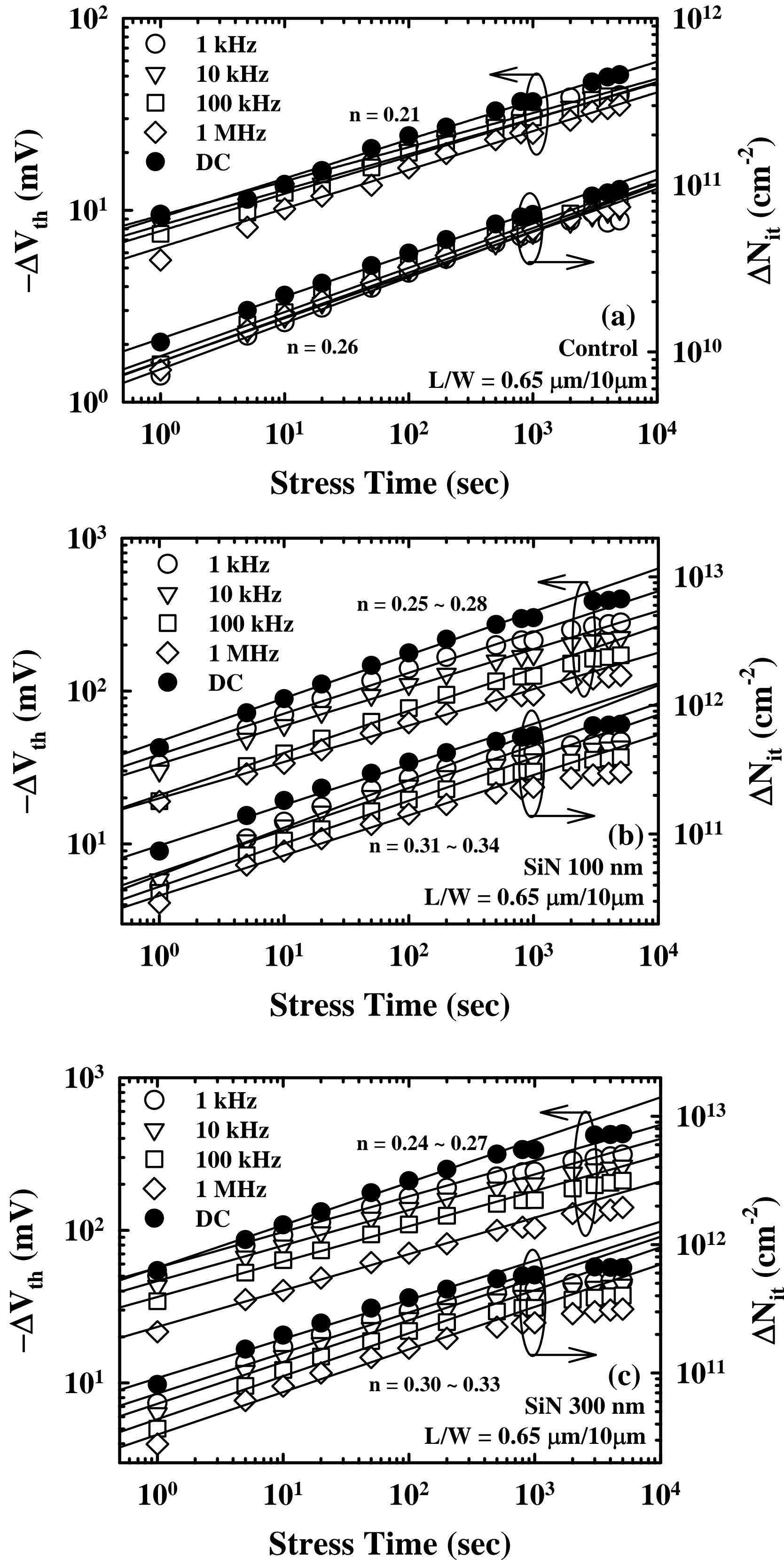


Fig. 4.4 Threshold voltage shift and interface state generation for devices measured at four different AC stress frequencies at 125 ˚C. (a) Control samples, (b) samples having 100 nm PE-SiN capping, and (c) samples having 300 nm PE-SiN capping.

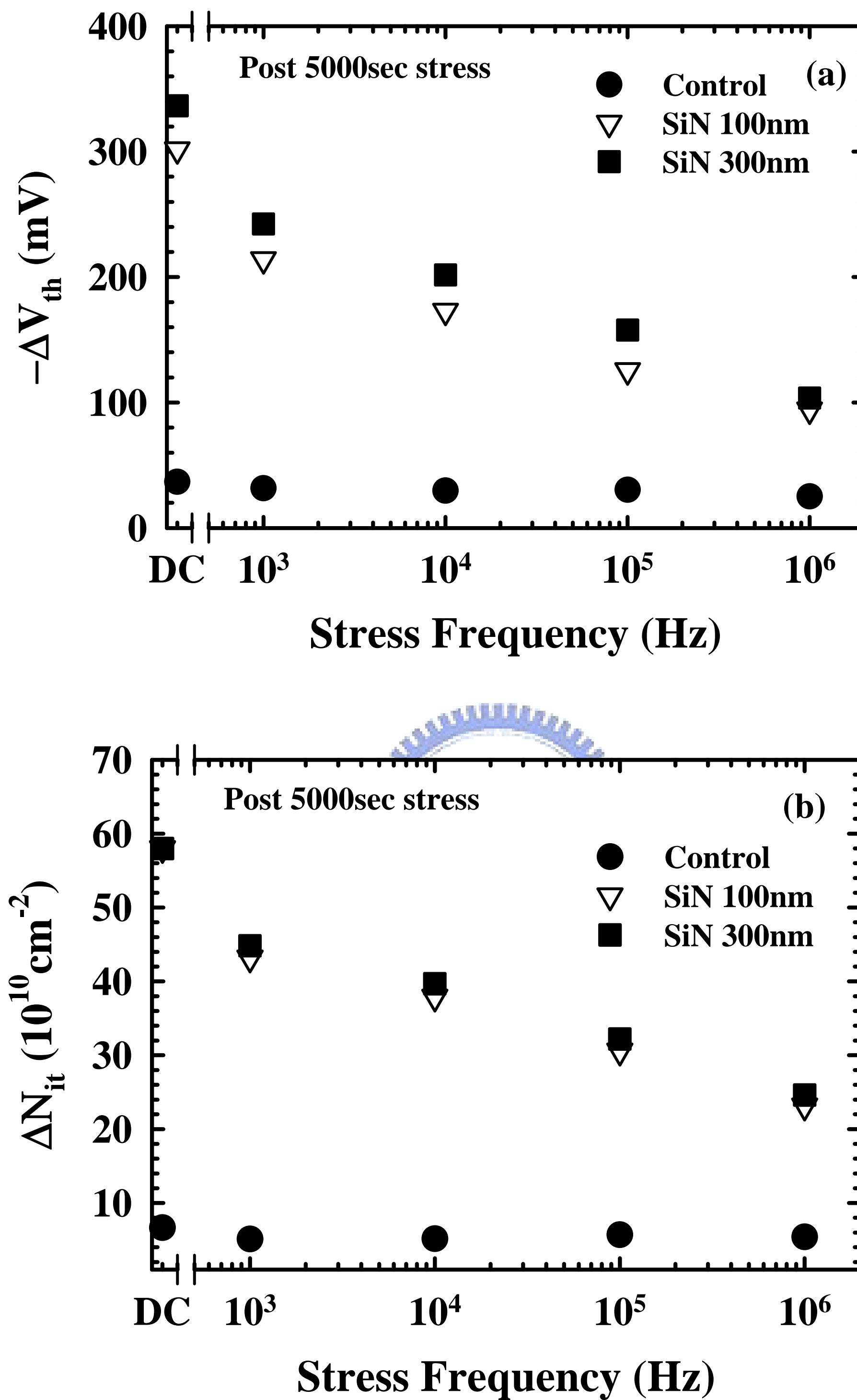


Fig. 4.5 (a) ΔV_{th} and (b) ΔN_{it} versus stress frequency after 5000sec stress. In the device with SiN capping, ΔV_{th} and ΔN_{it} are strongly dependent on frequency. As frequency increases, both ΔV_{th} and ΔN_{it} decrease significantly.

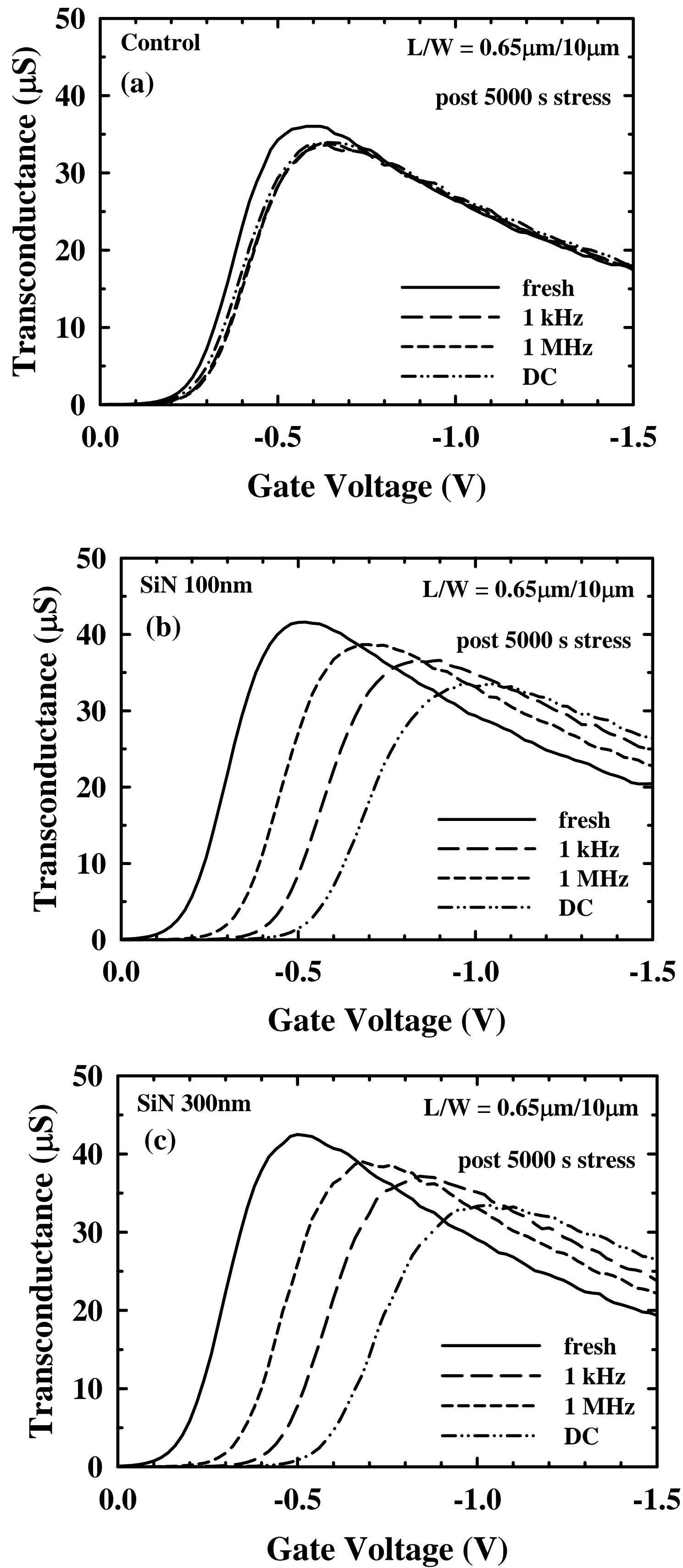


Fig. 4.6 Transconductance in devices with and without SiN-capping, as-fabricated and after 5000 sec DC and AC stress (1 kHz and 1 MHz), all measured at $V_G - V_{th}$ = -4 V and 125˚C.

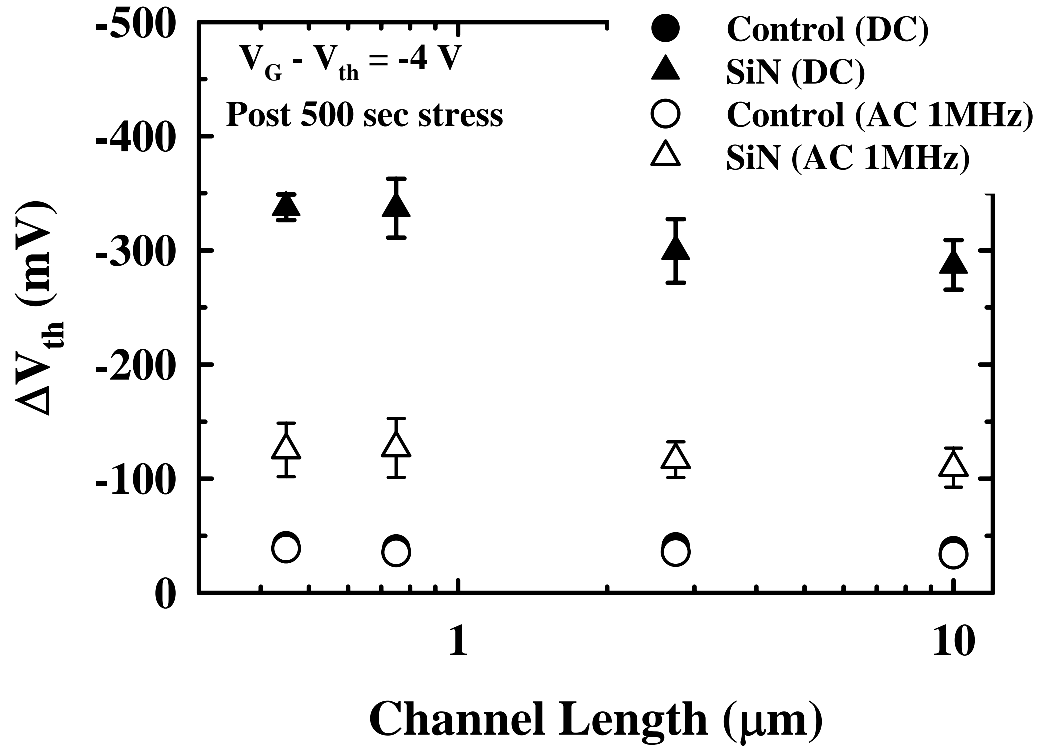


Fig. 4.7 ΔV_{th} vs. channel length after 500 s NBTI stress. Regardless of the channel length, devices with PE-SiN capping have larger ΔV_{th}.

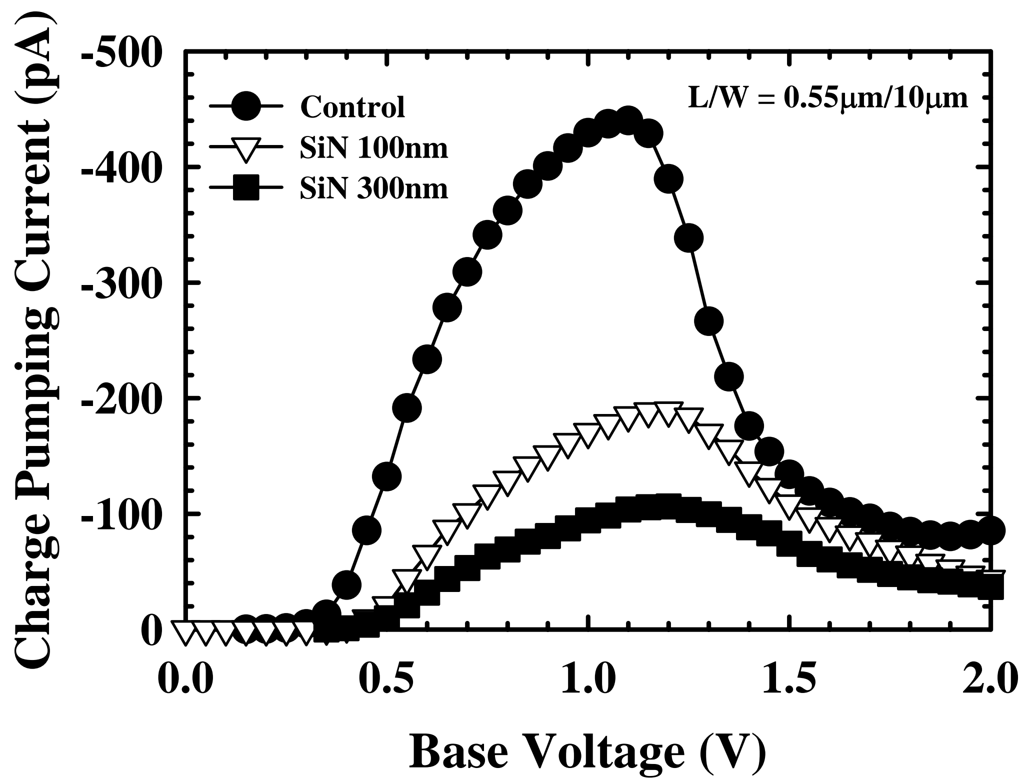


Fig. 4.8 Charge pumping current of fresh devices for the control and devices with SiN capping thickness of 100 nm and 300 nm.

Chapter 5

Fabrication and Characterization of NMOSFETs with LP-SiN Capping Layer

5.1 Introduction

Geometric scaling of silicon complementary metal-oxide semiconductor (CMOS) transistors has enabled not only an exponential increase in circuit integration density (Moore's law), but also a corresponding enhancement in the transistor performance itself. Many methods have been adopted to improve CMOS integrated circuits. Recently, strain engineering in the channel has emerged as one of the most effective remedies to boost the drive current in the scaled devices [1-7]. This could be done by either applying high biaxial tensile strain to the channel region with a SiGe virtual substrate [1-2], or by uniaxially straining the channel with strain boosters [3-7]. The approach of using SiGe virtual substrate, however, suffers from a number of drawbacks such as Ge up-diffusion and high defect density. In contrast, the approach of uniaxially straining the channel is essentially free from the aforementioned drawbacks. For example, a SiN capping layer deposited by the low pressure CVD (LPCVD) over the gate was shown to induce a uniaxial tensile strain in the channel that is beneficial for boosting the drive current in scaled NMOSFETs [4-6]. The above approach is attractive since it can be incorporated seamlessly in state-of-the-art ULSI technology, and has received many attentions in the last few years.

Generally, the tensile SiN layer was deposited by an LPCVD system, and the extra thermal budget of SiN deposition is inevitable. However, few studies have focused on

whether this extra process step has negative impacts on device characteristics or not. This work is aimed at evaluating the effects of channel strain as well as the procedure of SiN deposition on the devices performance. Bandgap narrowing induced by the channel strain and its influences on device characteristics are also addressed.

5.2 Devices Fabrication

The NMOSFETs tested in this study were with 3 nm thermal oxide grown in a vertical furnace in O_2 at 800˚C, and 150 nm poly-Si layer as the gate material. After the gate formation, most samples were capped with a SiN capping layer of 100 nm, 200nm, or 300nm, deposited using an LPCVD system (i.e., SiN splits), while some wafers were deliberately skipped of the SiN capping layer to serve as the controls (i.e., control split). The SiN deposition was performed at 780˚C with SiH_2Cl_2 and NH_3 as the reaction precursors. For some samples having SiN capping, the SiN layer was intentionally removed after the deposition in order to evaluate the impact of deposition process (i.e., SiN-removal split). Topmost passivation layer of all wafers is a 300 nm-thick TEOS, followed by contact holes and metallization processes. Finally, the processing steps were completed with a forming gas anneal at 400˚C. Electrical characterizations were performed using an HP4156 system. The interface traps were evaluated using the charge pumping method with a fixed amplitude of 1.5 V at 1 MHz.

5.3 Results and Discussion

5.3-1 Effects of Channel Strain on Device Performance

Figure 5.1 shows the output characteristics of NMOSFETs for all splits (i.e., control split, different SiN-capped splits, and SiN-removal split) with channel length of 0.5 μm. Drive current enhancement is clearly observed for the devices with SiN capping

layer, and increases as SiN thickness increases. For the SiN-removal split also shown in Fig. 5.1(b), it is seen that the current enhancement becomes negligible, confirming that the origin of the current enhancement indeed arises from the stress of the SiN-capping layer. Subthreshold characteristics of the same devices are shown in Fig. 5.2. The aforementioned impact of SiN on current enhancement also reflects on the results of transconductance. The SiN-removal sample shows slightly higher transconductance than the control counterpart, mainly due to the reduced interface state density that will be addressed in more detail later. Nevertheless, the subthreshold slope of all devices does not seem to be affected by the SiN capping and removal processes, as shown in Fig. 5.2. Figure 5.3 shows the percentage increase of the drive current of the SiN-capped and SiN-removal samples compared with the controls, as a function of channel length. We can see that the drive current enhancement reaches about 12%, 17%, and 20% at a channel length of 0.4 μm with 100 nm, 200 nm, and 300 nm of SiN-capping, respectively. In contrast, the SiN-removal devices in Fig. 5.3(b) show negligible enhancement. These observations demonstrate that the current enhancement is truly due to the uniaxial tensile strain induced by the SiN capping which increases with decreasing channel length [5,6].

The capacitance-voltage *(C-V)* characteristics of the samples are shown in Fig. 5.4. Basically the oxide thickness difference among the three splits is negligible, though slightly higher poly depletion effect is observed in the SiN-capped and SiN-removal samples, presumably related to the high temperature incurred during SiN deposition (i.e., 780˚C). Less solid solubility of poly gate dopants at such a high temperature may be one of the culprits to lower the inversion gate capacitance. However, the origin of this phenomenon remains unclear and more efforts are needed for a full understanding at this stage. The active dopant concentration can be easily extracted by the following

equation [8]:

$$\frac{1}{C_{\max}} = \frac{1}{C_{ox}} + \sqrt{\frac{8kT}{\varepsilon_{Si} q^2 N_p}} \tag{5-1}$$

where N_p is the active dopant concentration at the poly gate. Figure 5.5 shows the values of N_p in all splits. It should be noted that a higher thermal budget will result in the less solid solubility of gate dopants and decreases the inversion gate capacitance. Hence, the SiN capping procedure is not a negligible factor in affecting device characteristics.

5.3-2 Short Channel Effects

Figure 5.6 shows the threshold voltage (V_{th}) roll-off characteristics of the devices from all splits. The results are obtained at V_{DS} = 0.05 V. Among the three SiN-capping splits and the control split, the control split depicts a pronounced reverse-short-channel-effect (RSCE). This is probably due to boron segregation at the implant-damaged regions located close to the edge of the channel [9]. The phenomenon, however, is not observed in the three SiN capping splits. It is noted that RSCE would be suppressed due to boron redistribution as the thermal budget increases [9]. Additional thermal budget introduced by the SiN deposition step well explains the suppression of the RSCE as shown in Fig. 5.6(b). Another interesting trend shown in Fig. 5.6(b) is that the prominent V_{th} roll-off behavior for the SiN-capped samples is relaxed by the removal of the SiN layer. We believe this is related to the bandgap narrowing effect caused by channel stress [10], which could be eliminated when the SiN is removed. In brief, both extra thermal budget and the channel strain associated with the SiN-capping devices would lead to a larger threshold voltage shift.

Next, short-channel effect on the drain-induced barrier lowing (DIBL) is examined.

1896

DIBL is another indicator for evaluating the short-channel effects, and can be empirically characterized in MOSFET with a fixed L by measuring and plotting a set of log I_D versus V_G curves with increasing V_{DS} as the parameter. The results are shown in Fig. 5.7. We can see that basically no obvious difference is observed among all samples. This indicates that the use of SiN-capping would not worse the DIBL control of the devices.

5.3-3 Extracting Oxide Thickness by F-N Current Fitting

As device dimensions are reduced to the deep-submicron regime, an accurate knowledge of gate oxide thickness (T_{ox}), oxide voltage (V_{ox}), and surface voltage drop in poly and substrate becomes increasingly important in device design for predicting circuit performance, reliability projection, and manufacturing control. Several techniques have been adopted to extract gate oxide thickness, for example, ellipsometry is commonly used to monitor oxide thickness during device manufacturing. Cross-sectional transmission electron microscopy (TEM) is another tool to analyze not only gate oxide thickness but also interface uniformity. Actually, electrical measurement can also be used to extract gate oxide thickness. For example, capacitance-voltage (*C-V*) method is widely used to extract oxide thickness since much information can be obtained from *C-V* data. However, the *C-V* technique is prone to error due to non-saturation effect in capacitance even under strong accumulation, and could yield a larger value than the real physical thickness. The discrepancy between the electrical and physical techniques is due to the effects of finite thickness of inversion/accumulation layer (including quantum effect) and polysilicon depletion. Therefore, current-voltage method based on the model of Fowler-Nordheim (F-N) tunneling current is proposed to accurately determine the ultrathin oxide thickness by taking the poly-depletion effect

into consideration. Typical gate current characteristics of ultrathin oxide and the simulated F-N current fitting curves are shown in Fig. 5.8.

Figure 5.9 shows the band diagram of a n^+-poly Si/SiO_2/p-Si NMOSFET under positive bias. For $V_{ox} > \Phi_B$, the well-known F-N theory yields the following expression:

$$J_{FN} = AE_{ox}^2 \exp(-B/E_{ox}) \qquad (5\text{-}2)$$

where E_{ox} is the oxide field and is equal to V_{ox}/T_{ox}.

$$V_{ox} = V_G - V_{fb} - \phi_s - V_p \cong V_G - V_p \qquad (5\text{-}3)$$

where Vp is the voltage drop due to poly-depletion. A and B are the constants given by the following relationships:

$$A = \frac{q^3}{8\pi h}\left(\frac{1}{\Phi_B m^*}\right) \qquad (5\text{-}5)$$

$$B = \frac{8\pi}{3qh}\sqrt{2m^*\Phi_B^3} \qquad (5\text{-}6)$$

where h is the Plank constant, and Φ_B is the barrier height at the cathode interface in eV. The m* is the average effective mass in the bandgap of SiO_2 relative to the free electron mass. Generally, A and B are equal to 9.92×10^{-7} A/V^2 and 2.635×10^8 A/cm, respectively.

The oxide thickness extracted by fitting the F-N current curve is shown in Fig. 5.10, and the oxide thickness is nearly 2.705 nm. It is reasonable that the oxide thickness extracted from F-N current is thinner than that deduced from *C-V* characteristics. Figure 5.11 shows typical *C-V* characteristics of the fabricated samples. Theoretical fitting with and without considering the quantum-mechanical and/or poly-depletion effects are performed to extract the oxide thickness. It can be seen that oxide thickness using quantum-mechanical treatment is nearly the same as that using F-N current fitting method. In fact, F-N current fitting method for extracting oxide thickness has been widely adopted because of the accuracy and convenience as an on-wafer measurement

method [11,12]. However, this method is not suitable for measuring oxide thinner than 2.5 nm because direct tunneling is responsible for the gate leakage.

5.3-4 Bandgap Narrowing

In strained Si NMOSFETs using SiO_2 as the gate dielectric, the barrier height is greater than that of conventional devices. The increase of the Si/SiO_2 barrier height is due to the tensile-strain-induced bandgap narrowing lower of the conduction band [10]. Under a specific gate bias, more inversion charges will be induced due to the bandgap narrowing, as a result the threshold voltage is lowered and results in a shallower channel depletion [10]. By using the theoretical data presented by Thompson [13], the induced strain could be extracted based on the threshold voltage shift, as shown in Fig. 5.12.

According to Fig. 5.9, electron tunneling current should be reduced if bandgap narrowing occurs. Figure 5.13 shows the gate tunneling current for all splits of NMOSFETs. It can be seen that the gate leakage current decreases as the thickness of SiN capping increases, and the SiN-removal split shows the same trend. According to the above discussion, no stress is left on the channel. Hence, the gate oxide thickness is slightly changed during the SiN deposition. Figure 5.14 shows the F-N current fitting of the SiN-removal split. It is noted that the SiN layer deposition would slightly increase the gate oxide thickness. The extracted oxide thicknesses are 2.775 nm, 2.81 nm, and 2.85 nm for SiN deposition process of 100 nm, 200 nm, and 300 nm, respectively. This is consistent with Fig. 5.6(b) that the threshold voltage roll-off worsens as the SiN deposition time increases. Hence, not only less solid solubility of gate dopants but also the gate oxide thickness increases with increasing thickness of SiN layer.

Barrier height of SiO_2/Si can easily be extracted from F-N tunneling current, as shown in Eq. (5-2). Recalling Eq. (5-5) & (5-6), both A and B are functions of barrier

height. Figure 5.15 shows the F-N plot of the devices with SiN capping. The intercept of the linear F-N plot gives A, while the slope yields B. Using the value of B, the electron tunneling barrier height can be easily extracted. The extracted barrier height of devices with SiN capping thickness of 300nm is 3.1 eV. On the other hand, 3.21 eV is obtained for the control samples. This result is inconsistent with bandgap narrowing which SiN-capped devices should have larger barrier height. The shorter F-N current region to extract barrier height is the main cause. Devices with thicker gate oxide (e.g., 4 nm) are more suitable for extracting bandgap narrowing by F-N current fitting.

5.3-5 Impacts of SiN Capping on Interface State Density

It is well known that hydrogen species can effectively passivate dangling bonds at the Si/SiO_2 interface. In this work SiN deposition was performed by an LPCVD system with SiH_2Cl_2 and NH_3 as the reaction precursors. Therefore, the reaction chamber would be filled with hydrogen species during the deposition process. Figure 5.16 shows the charge pumping current (Icp) of all splits. It is consistent with the above discussions that Icp of the SiN-removal splits is slightly less than that of the control device, as shown in Fig. 5.16(a). This also explains the observation shown in Fig. 5.2 that Gm in the SiN-removal split is slightly larger than that in the control counterpart. From Fig. 5.16(b), channel strain may actually induce a larger amount of interface states at the Si/SiO_2 interface as compared with that of the control devices. Additional interface states generation due to the channel strain could be the origin of higher Icp in the strained devices, as shown in the figure. Nevertheless, it is interesting to note that Icp decreases with increasing SiN-capping thickness. This could be explained by the fact that more hydrogen species may participate in interface state passivation process as the time of the SiN deposition increases. These results suggest that the benefits of interface

state passivation increase with SiN capping thickness, as long as the induced strain level is not too high to degrade the interface properties. In brief, the hydrogen species contained in the SiN films and the induced strain may both affect the interface state density.

5.4 Summary

In this work we investigate the effects of LPCVD SiN capping process and the resultant channel strain induced by the SiN-capping layer on the device characteristics. The channel strain induced by the SiN capping layer over the gate greatly boosts the drive current of short-channel devices. Enhancement ratio as high as 20 % is achieved for the devices with SiN-capping thickness of 300 nm at a channel length of 0.4 μm. The results indicate that the thermal budget associated with the deposition of the SiN capping layer could alleviate the reverse short-channel effect of the uncapped devices. The bandgap narrowing effect due to the channel strain may result in further lowering in V_{th} as the channel length is shortened.

The extra thermal budget of SiN capping is beneficial for easing the RSCE, albeit it is also the main culprit for the less solid solubility of gate dopants and gate oxide thickness variation. The gate oxide thickness extracted by F-N tunneling current would increase from 2.705 nm for the control sample to 2.85 nm for the SiN-capping sample with 300 nm in thickness. In addition, interface state density is also affected by SiN capping procedure. More hydrogen species are expected to participate in interface state passivation as the time of the SiN deposition increases.

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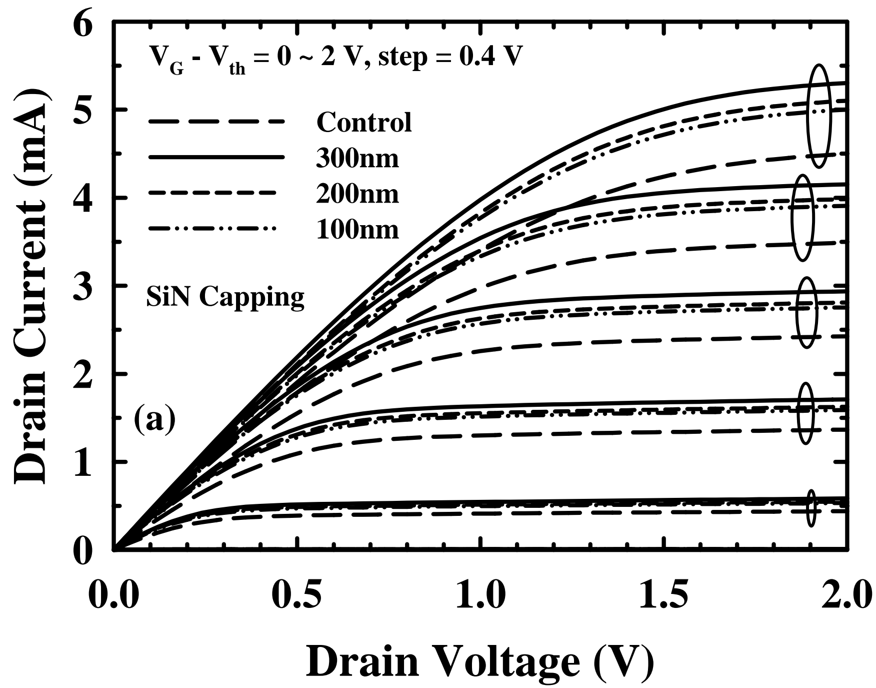


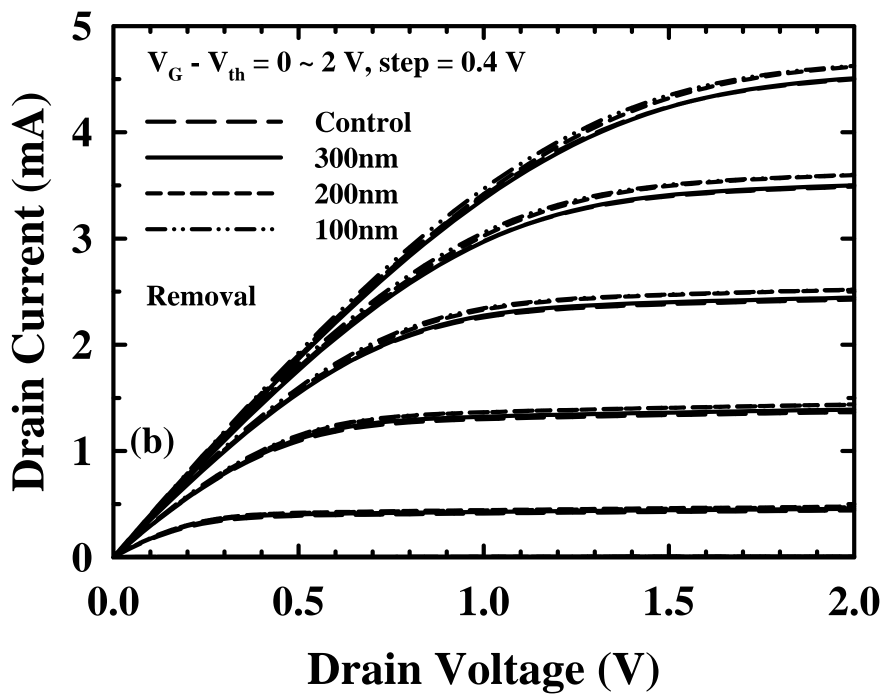


Fig. 5.1 Output Characteristics of different splits of NMOSFETs. Channel length/width = 0.5μm /10μm. (a) Control and different SiN-capping. (b) Control and SiN-removal devices.

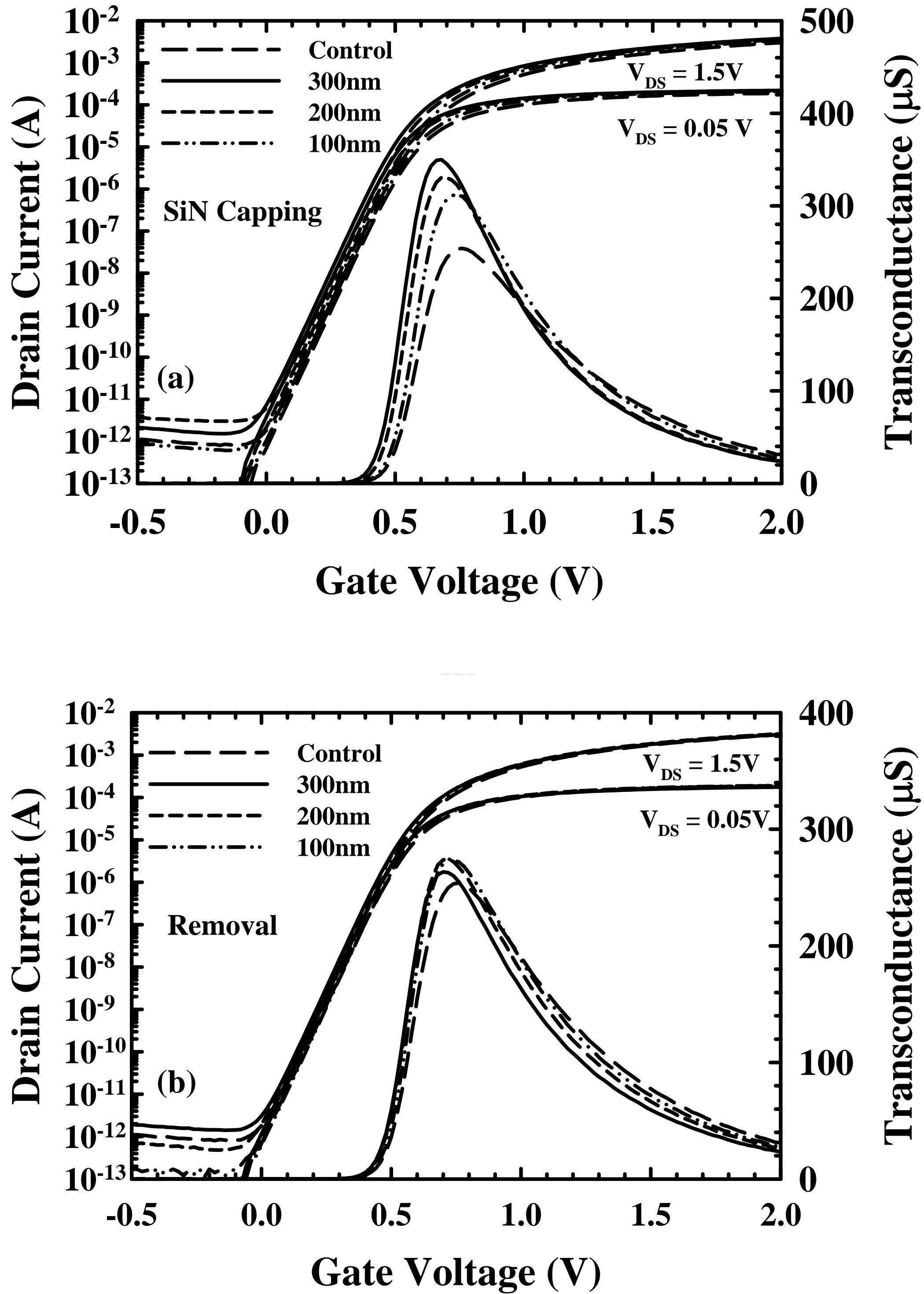


Fig. 5.2 NMOSFET Subthreshold characteristics and transconductance of different splits of samples. Channel length/width = 0.5μm /10μm. (a) Control and three different SiN capping devices. (b) Control and SiN-removal devices.

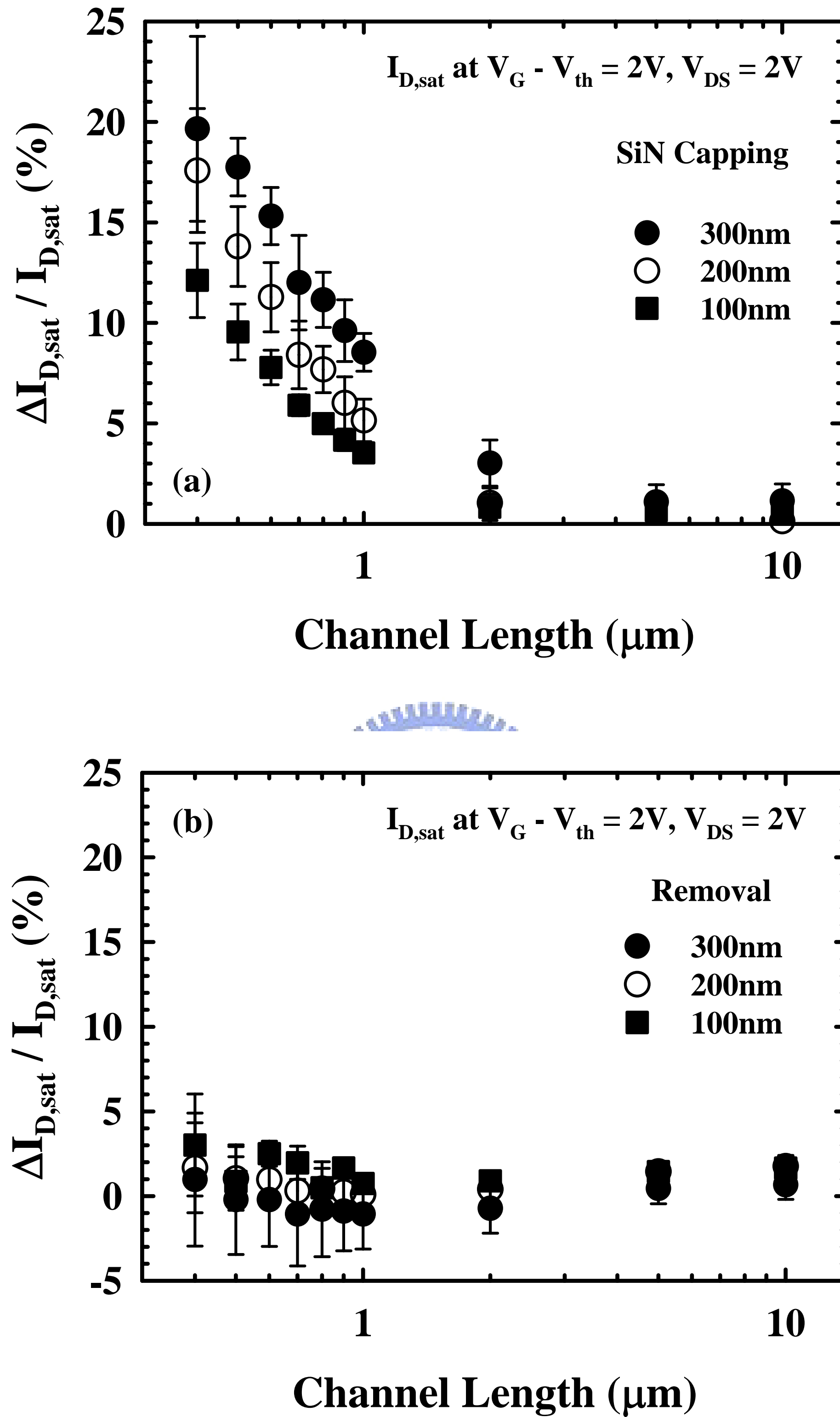
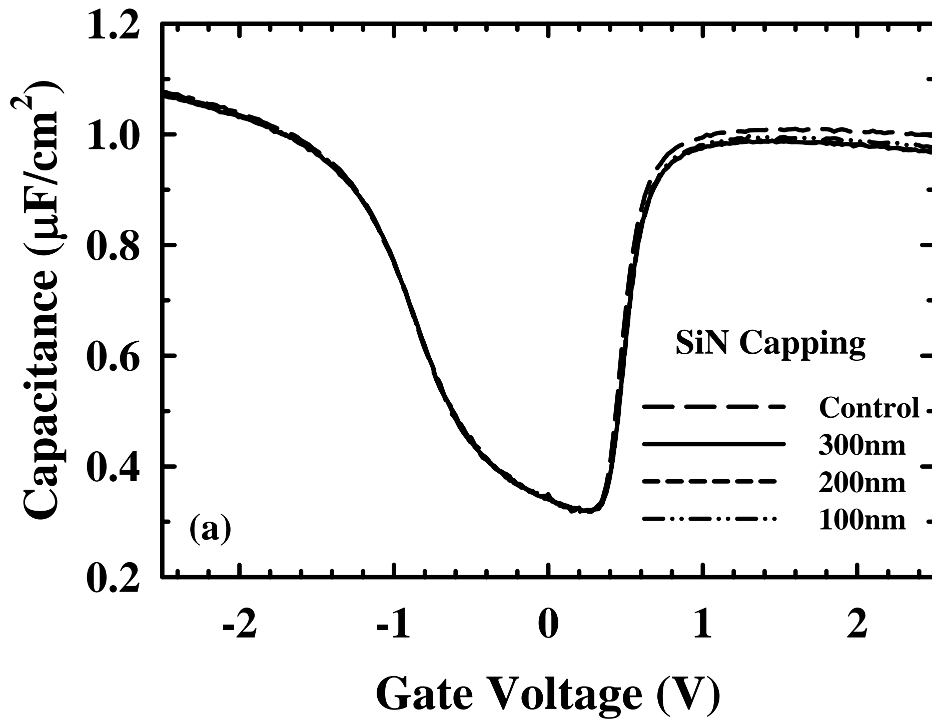


Fig. 5.3 Saturation current increase versus channel length. The saturation current is measured at $V_G – V_{th}$ = -2 V and V_{DS} = -2 V. (a) Control and three SiN capping devices. (b) Control and SiN-removal devices.



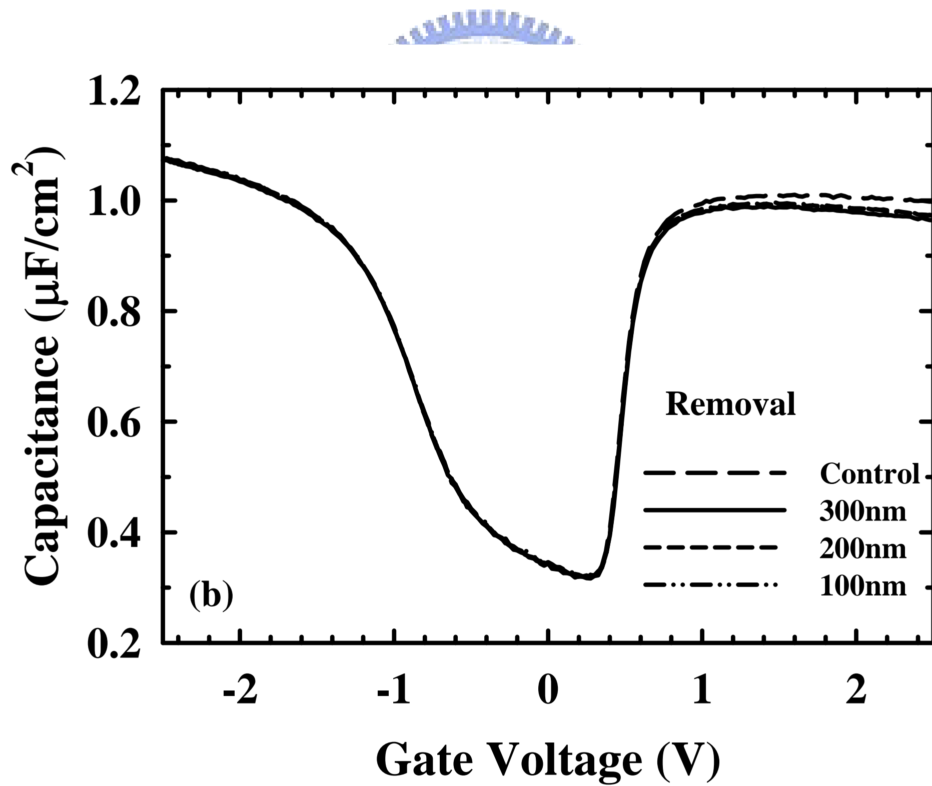


Fig. 5.4 Capacitance-Voltage (*C-V*) characteristics for different splits of samples. (a) Control and three different SiN-capping devices. (b) Control and SiN-removal devices.

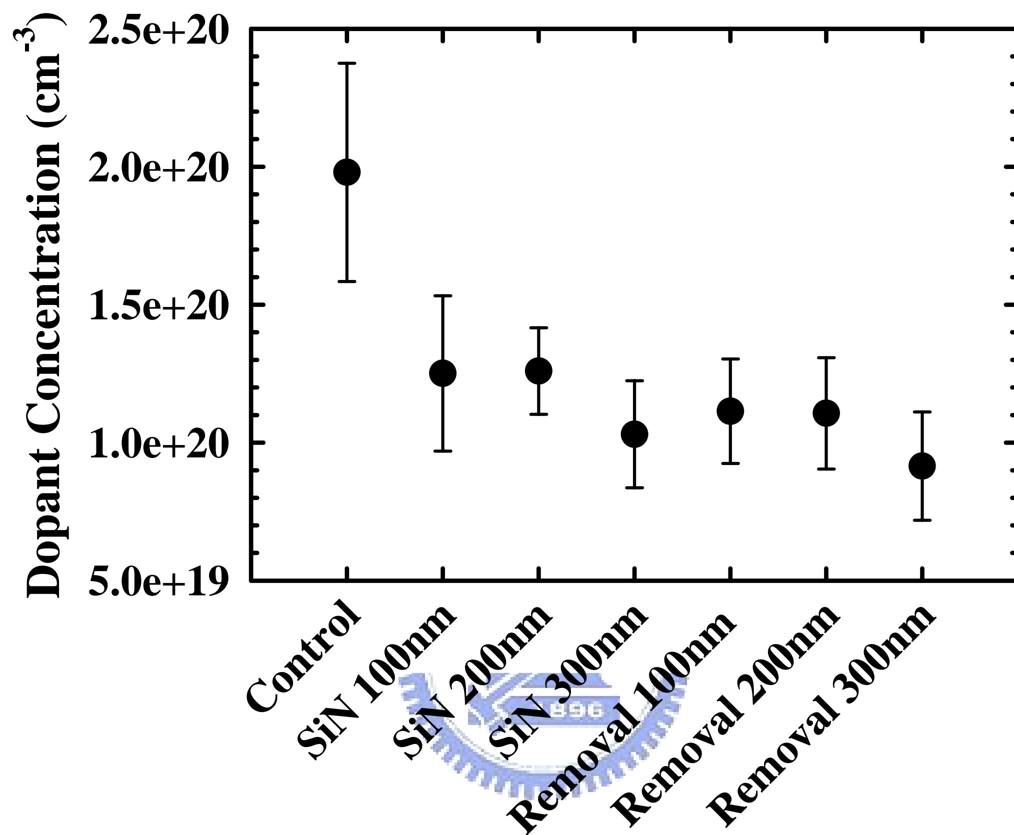


Fig. 5.5 The active dopant concentration of poly gate extracted from the C-V characteristics of different splits of samples.

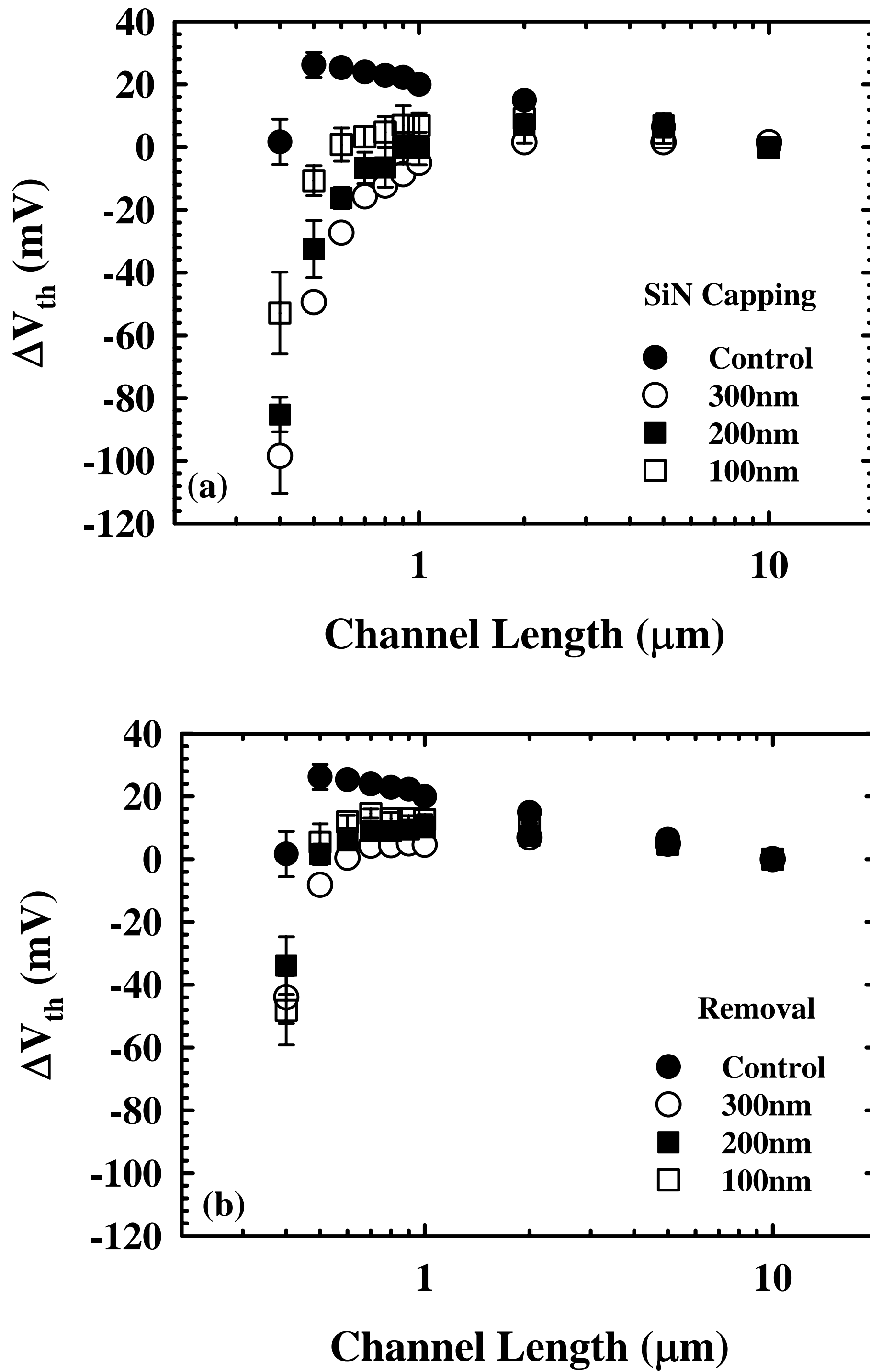


Fig. 5.6 Threshold voltage roll-off as a function of channel length for different splits of samples. (a) Control and three different SiN capping devices. (b) Control and SiN-removal devices.

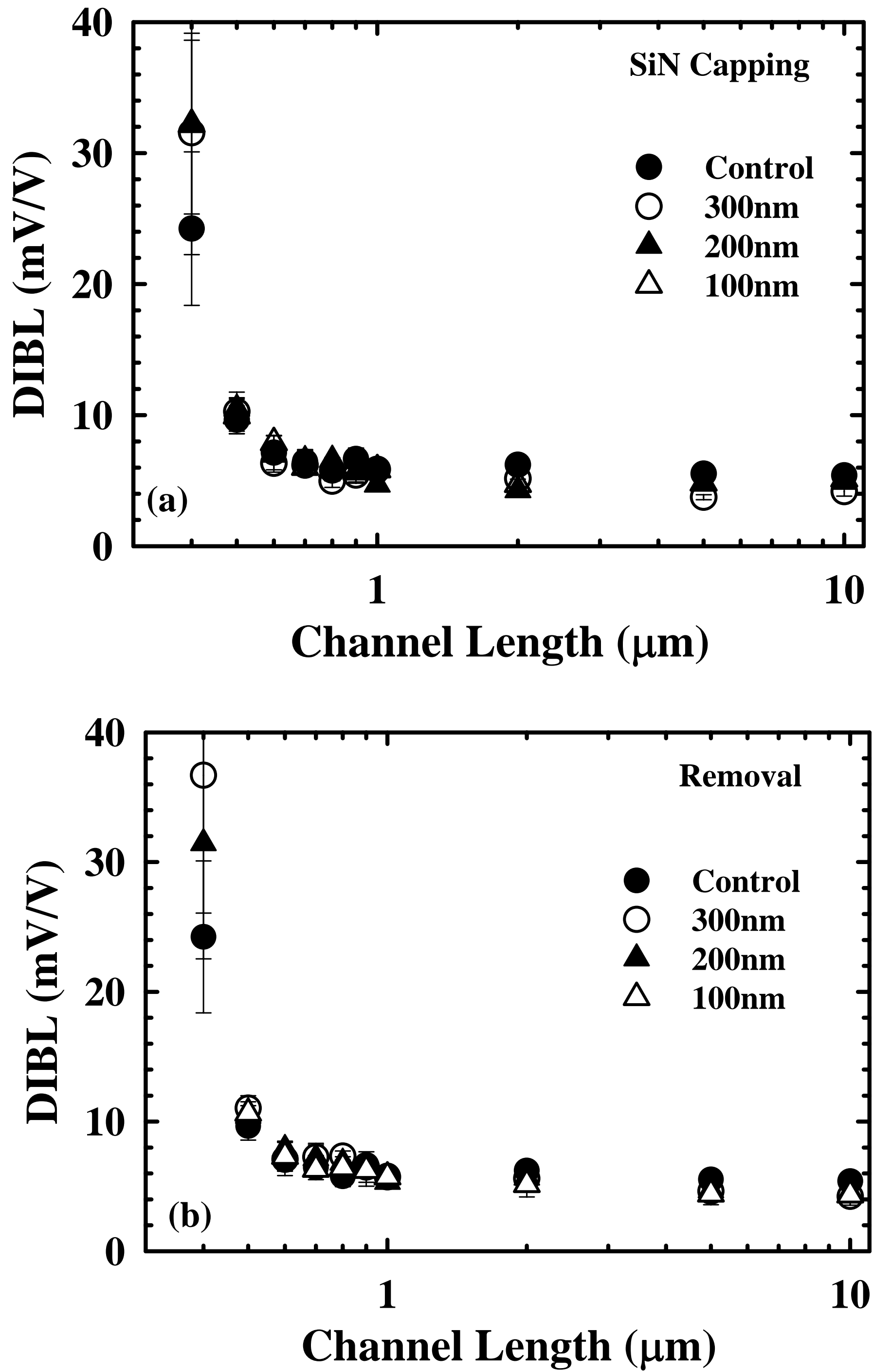


Fig. 5.7 Drain induced barrier lowing (DIBL) characteristics as a function of channel length. DIBL was evaluated by measuring the drain current change as V_{DS} is increased at a fixed gate voltage below threshold voltage. (a) Control and three different SiN capping devices. (b) Control and SiN-removal devices.

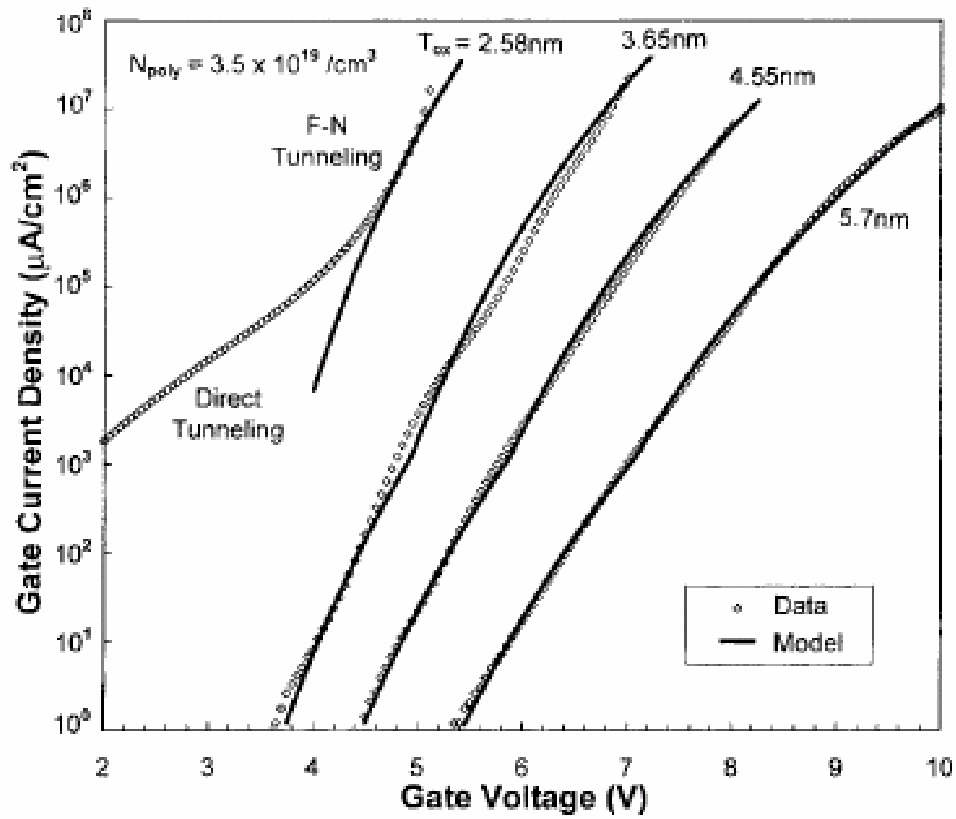


Fig. 5.8 Current density versus voltage characteristics of NMOSFETs. (*Kai Chen, Chenming Hu, Peng Fang, and A. Gupta, "Experimental confirmation of an accurate CMOS gate delay model for gate oxide and voltage scaling", IEEE ED Letter, vol.18, 1997, pp.275-277.*)

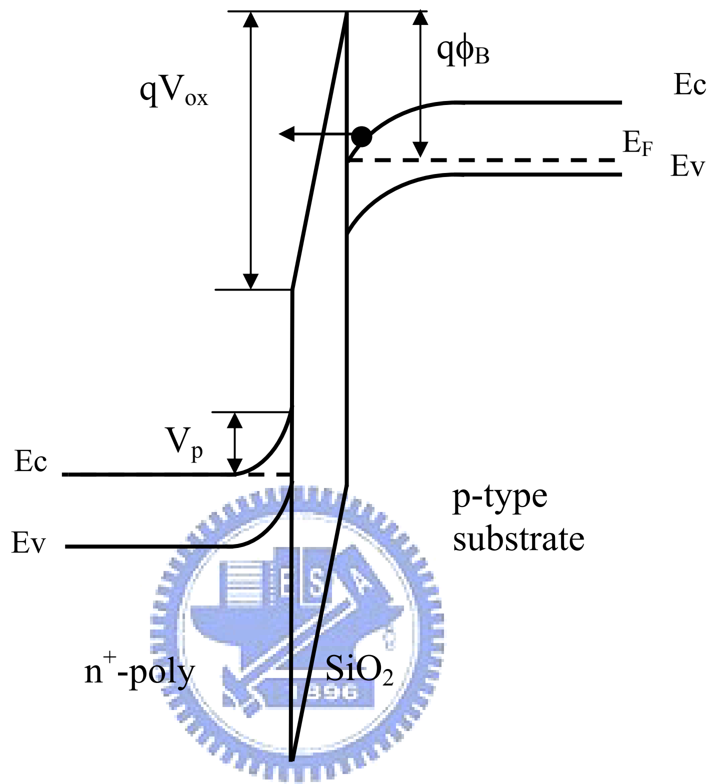


Fig. 5.9 Energy band diagram for conventional NMOS on a p-type substrate under Fowler-Nordheim tunneling.

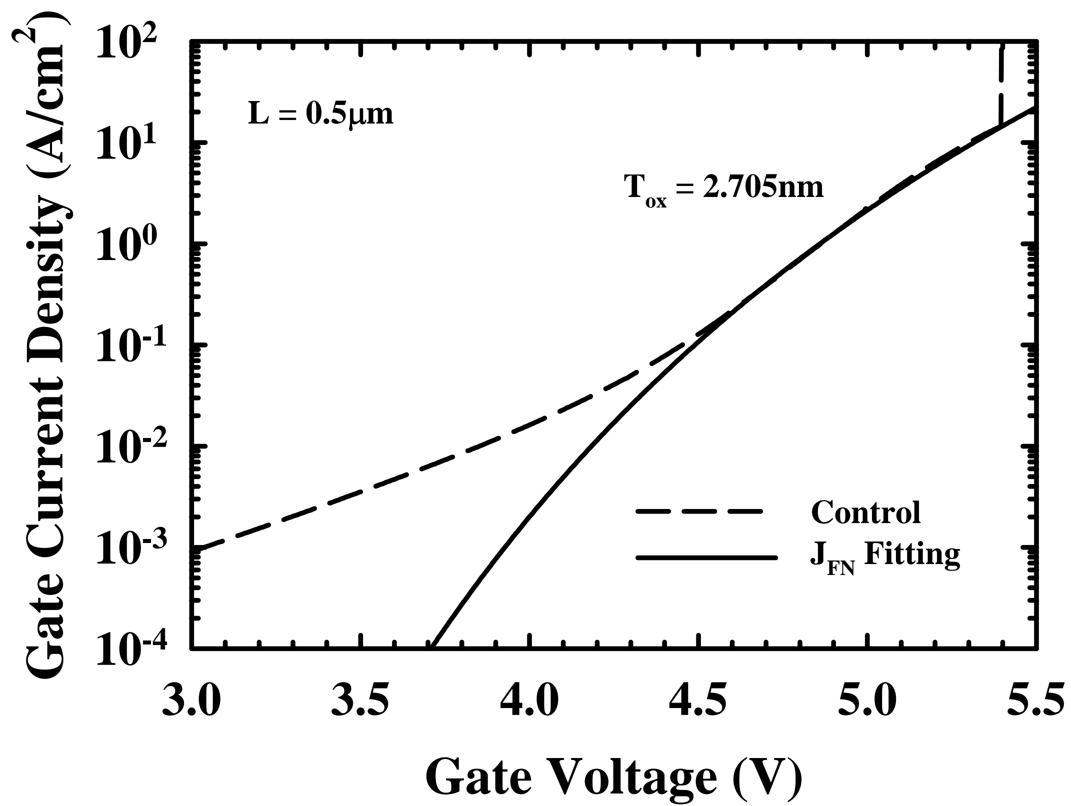


Fig. 5.10 Gate oxide thickness extracted by Fowler-Nordheim tunneling current in a control sample.

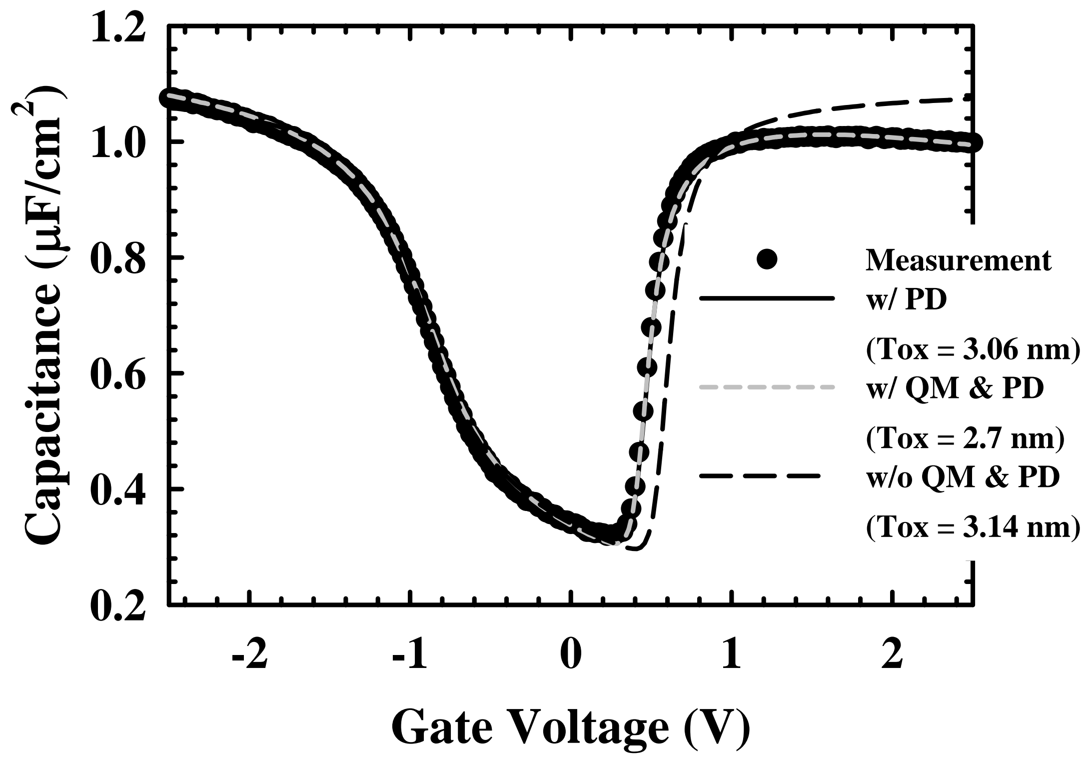


Fig. 5.11 Typical C-V characteristics of the test samples. Thickness is theoretically extracted by taking or not taking the poly depletion (PD) and/or quantum mechanism (QM) into account.

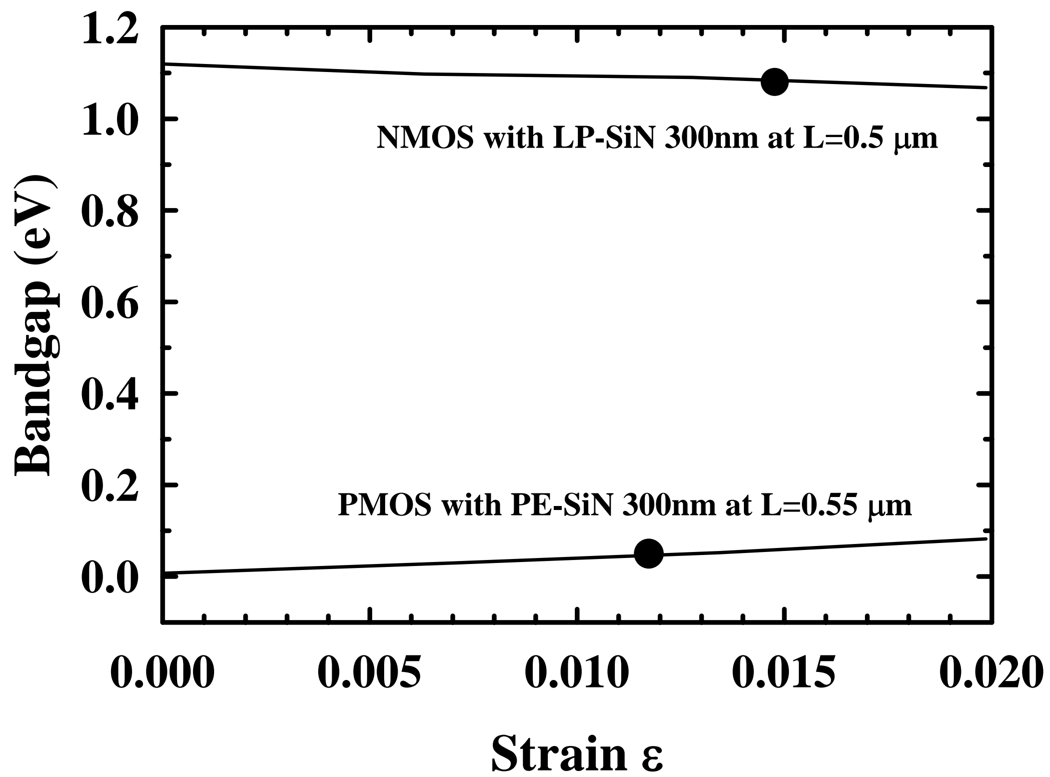


Fig. 5.12 The relationship between bandgap narrowing and strain from Thompson's simulation. (S. E. Thompson et al., in *IEDM Tech. Dig.*, pp.221-224, 2004)

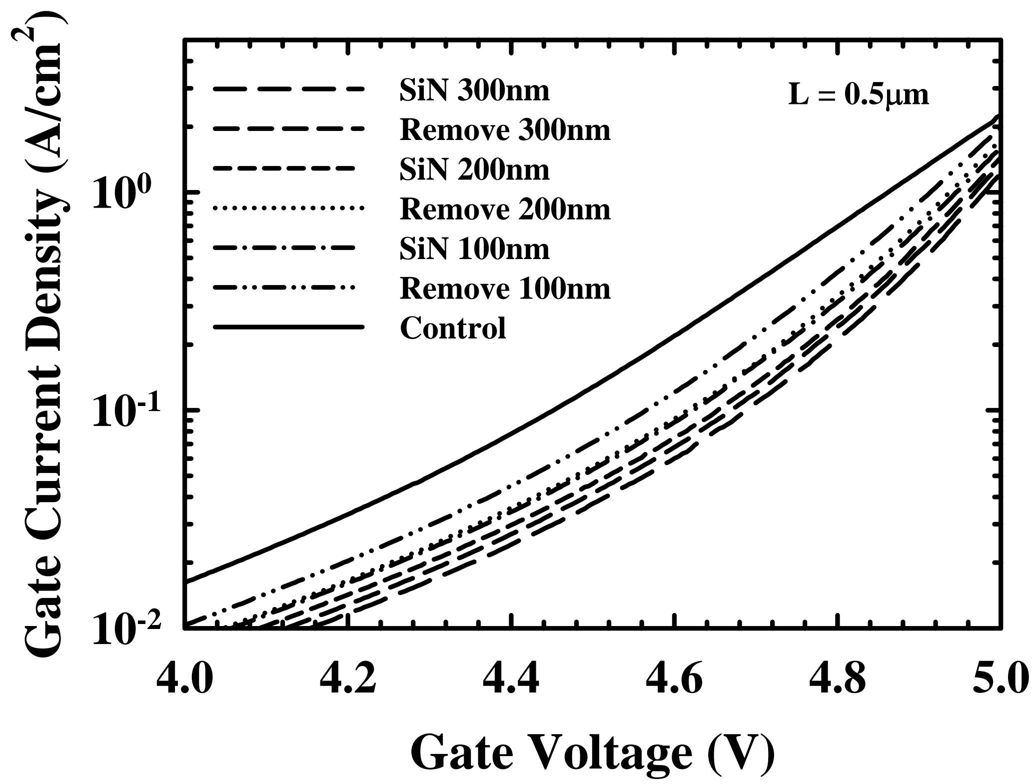


Fig. 5.13 Gate current density versus gate voltage of all splits at channel length of 0.5μm.

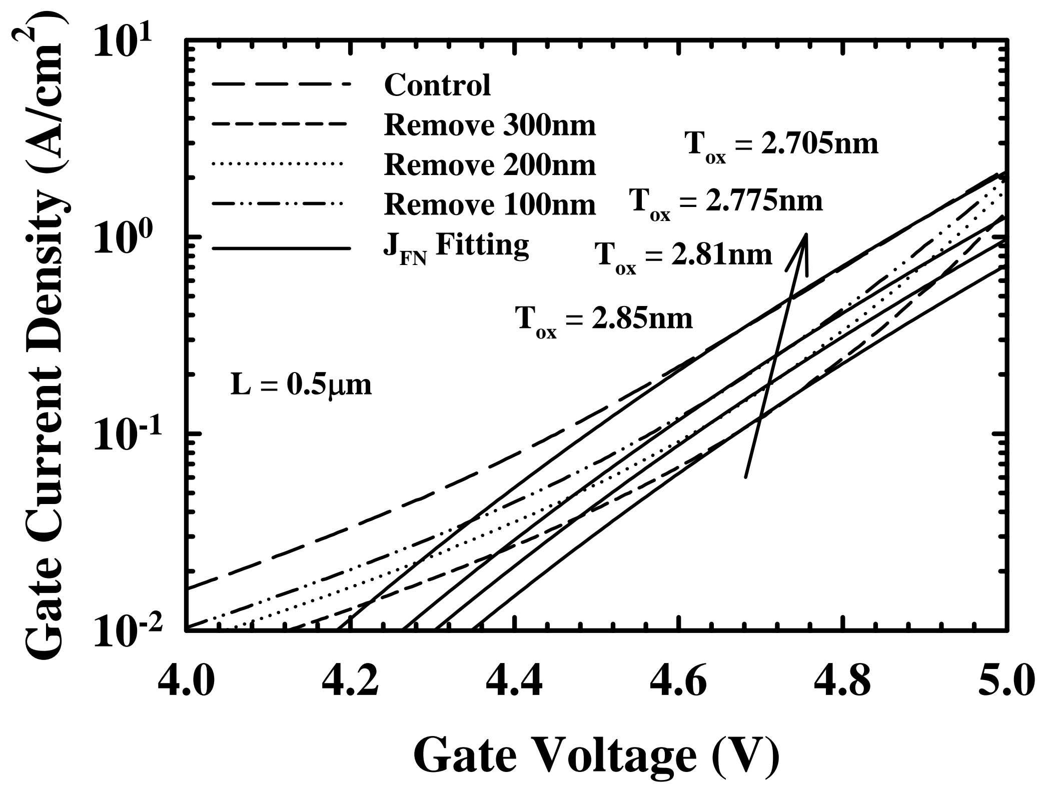


Fig. 5.14 Gate oxide thickness extracted by Fowler-Nordheim tunneling current in SiN-removal samples.

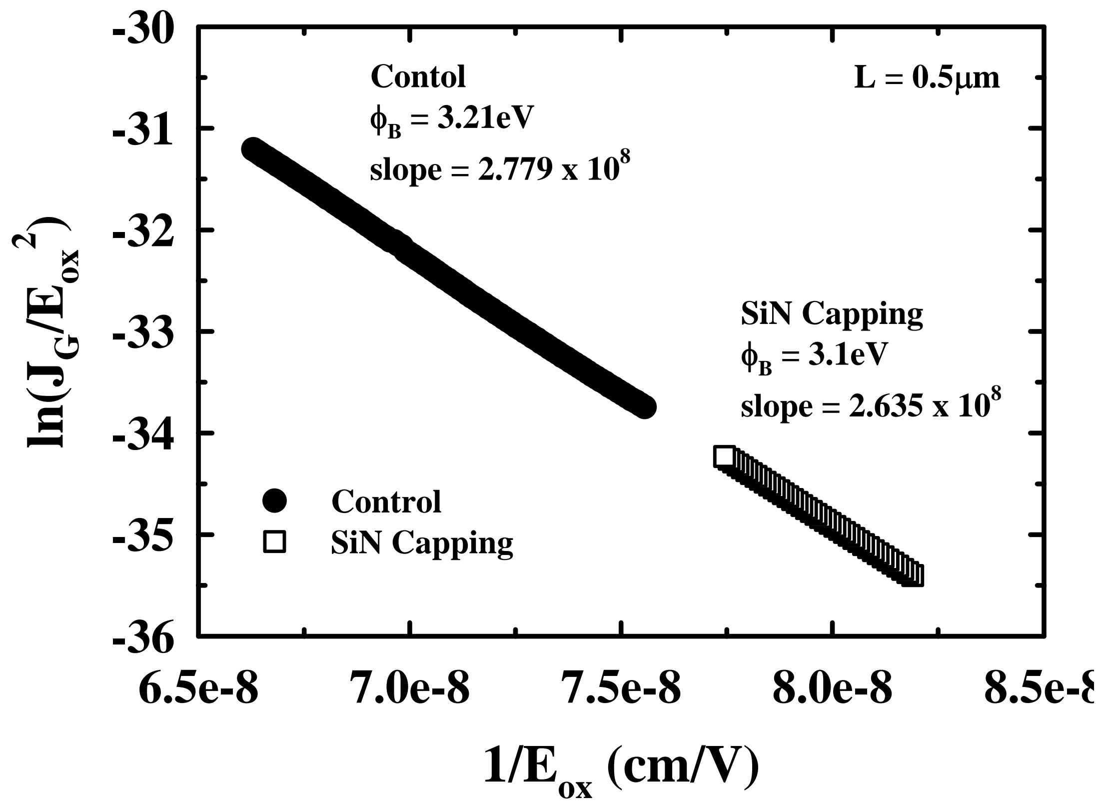
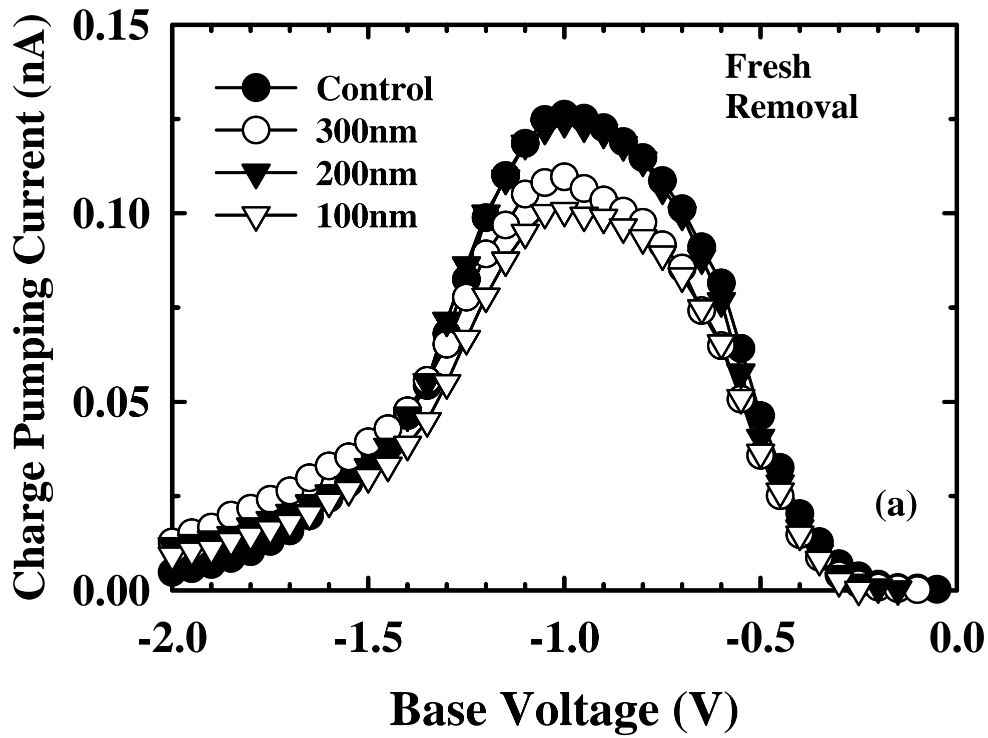


Fig. 5.15 The electron tunneling barrier height measured by the Fowler-Nordheim tunneling plot.



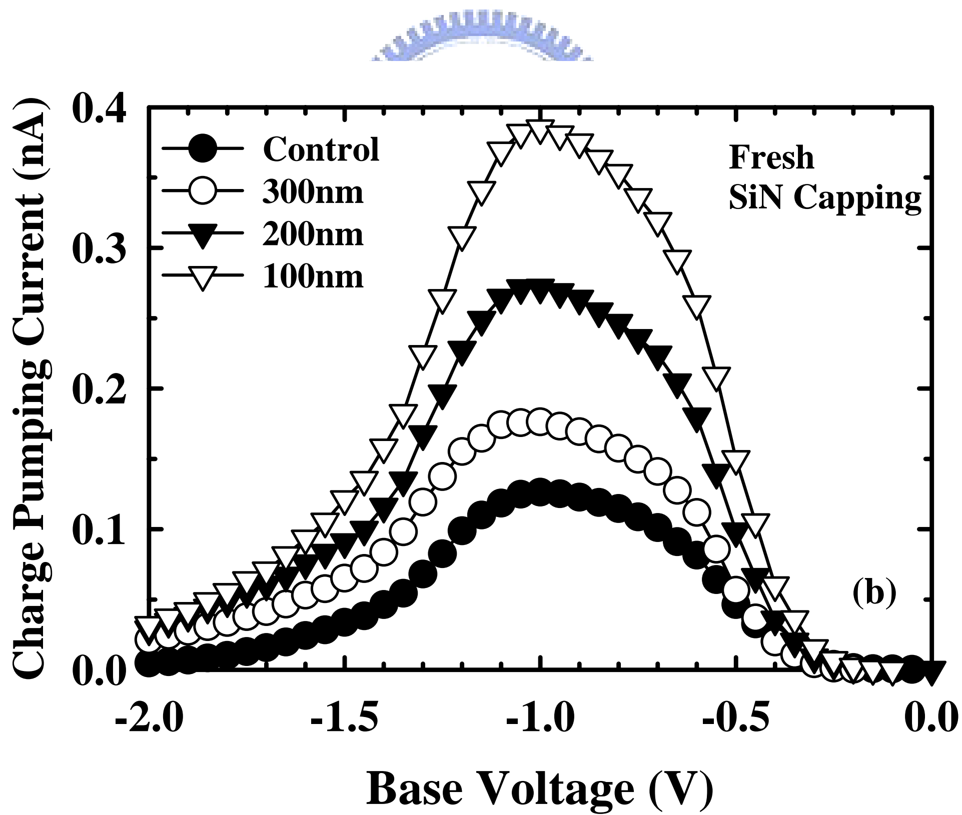


Fig. 5.16 The charge pumping current of all splits. (a) Control and SiN-removal devices. (b) Control and three different SiN-capping devices.

Chapter 6

Impacts of LP-SiN-Capping Layer on Hot Carrier Degradations in NMOSFETs

6.1 Introduction

Strain channel engineering has emerged as one of the most attractive method to the scaling of metal-oxide-semiconductor field-effect transistors (MOSFETs), and it may be the only effective method for dramatically improving the performance of complementary metal-oxide-semiconductor (CMOS) transistors using silicon-based materials. Strain engineering improves MOSFET drive currents by fundamentally altering the band structure of the channel and can therefore enhance performance even at aggressively scaled channel lengths [1-4]. Especially on un-axial strain case, capping a tensile-strain silicon-nitride (SiN) layer on NMOSFETs as contact-etch-stop-layer (CESL) has been shown to enhance drive current by improving channel mobility [5-7], and can be easily implemented using modern process procedures.

Now that the knowledge base concerning mobility enhancement in strained-Si has been reasonably well established, it is time to turn the focus on such issues as integration and reliability. Device degradation induced by hot electrons represents one of the most critical reliability issues in deep sub-micron NMOSFETs [8,9]. The physical mechanisms and characteristics of hot electron degradation have been extensively examined [10,11]. The degradations in terms of threshold voltage shift (ΔV_{th}), drain current degradation (ΔI_{DS}), and transconductance degradation (ΔG_m), were studied using the accelerated stress test. However, very few works have investigated the impact of SiN capping layer and the associated deposition process on the hot carrier reliability of

the strained devices. In this work, we investigate detailed hot carrier degradation characteristics of NMOS devices having local channel strain induced by the SiN-capping layer.

6.2 Experimental

The NMOSFETs used in this study were with 3 nm thermal oxide grown in a vertical furnace in O_2 at 800˚C, and 150 nm poly-Si layer as the gate material. After the gate formation, most wafers were capped with the SiN capping layer of 100 nm, 200nm, or 300nm in thickness, deposited using an LPCVD system (i.e., SiN splits), while some wafers were deliberately skipped of the SiN capping layer to serve as the controls (i.e., control split). The SiN deposition was performed at 780˚C with SiH_2Cl_2 and NH_3 as the reaction precursors. For some wafers that received the SiN capping layer deposition, the SiN layer was removed later in order to evaluate the impact of SiN deposition itself on the device characteristics (i.e., SiN-removal split). Wafers were then combined to receive the deposition of a 300 nm-thick TEOS passivation layer, followed by contact holes and metallization processes. Finally, the processing steps were completed with a forming gas anneal at 400˚C. Electrical characterizations were performed using an HP4156 system. The interface traps were evaluated using the charge pumping method with a fixed amplitude of 1.5 V at 1 MHz.

The lateral diffusion of interface state after hot carrier stress for all splits was also discussed in this work. The method developed in [12] and the measurement setup is shown in Fig. 6.1. The experimental procedures of the method are described below.

(1) Measure the Icp-V_h curve on a virgin MOSFET from the drain junction (with the source junction floating), and from it establish the V_h versus $V_{th}(x)$ relationship [13] near the junction of interest.

(2) Record the Icp-V_h curve after hot-carrier injection.

(3) The hot-carrier-induced interface state distribution, $N_{it}(x)$, is obtained from the difference of the Icp-V_h curve before and after hot carrier stress.

6.3 Results and Discussion

6.3-1 The Substrate Current and Impact Ionization Rate

A hot carrier with sufficient energy can produce more charge carriers through impact ionization. Impact ionization occurs when highly-energetic charge carriers excite an electron to the conduction band (or hole to the valence band) to create an electron-hole pair. The band diagram showing such process is illustrated in Fig. 6.2. The electron-hole pair generation rate is given by [14]

$$G = \alpha_n n \upsilon_n + \alpha_p p \upsilon_p \tag{6-1}$$

where α_n is the electron ionization rate defined as the number of electron-hole pairs generated by an electron per unit distance, α_p is the analogous hole ionization rate, n is the electron concentration, p is the hole concentration, and υ_n and υ_p are the electron and hole saturation velocities, respectively. A simplified, local-field-based empirical expression [15] for the ionization rate is

$$\alpha = A \exp\left(-b/E\right) \tag{6-2}$$

where A and b are experimentally-determined constants and E is the electric field. Eq. (6-2) shows that the carrier ionization rate is exponentially dependent on the electric field. Since a very high longitudinal electric field exists near the drain of a short-channel MOSFET, many electron-hole pairs are created. This provokes a cascading phenomenon in which generated carriers produce even more electron-hole pairs through secondary impact ionization, intensifying the effect. For strained Si, we would expect

that the higher carrier saturation velocities that arise from increased channel mobility would enhance the electron-hole generation rate according to Eq. (6-1).

The conventional metric for impact ionization in a MOSFET is the substrate current (I_{sub}). For NMOS devices, holes generated by impact ionization are collected by the substrate, giving rise to a measurable I_{sub}, as depicted in Fig. 6.1. (Electrons are either collected by the drain or injected into the gate dielectric.) I_{sub} can cause circuit problems, as it leads to noise and CMOS latchup, but it can also be used to indirectly monitor hot-carrier effects. For this reason, the bias conditions that have traditionally been used for performing hot carrier reliability studies are the biases that correspond to maximum I_{sub}. However, the metric for the hot-carrier degradation rate is I_{sub} normalized by the drain current (I_{sub} /I_D), called impact ionization rate.

The I_{sub} of the fabricated devices with various channel lengths are shown and compared in Fig. 6.3. It is clearly seen that with reducing channel length, the substrate current is much larger in the SiN-capped device, as compared with the other two splits (for example, more than 0.1 mA increase at the channel length of 0.5 μm). However, the difference in substrate current among different splits becomes negligible for the long-channel case (e.g., L = 5 μm). This result indicates that the channel strain plays an important role in affecting the generation of channel hot electrons and the associated impact ionization process. This could be related to the bandgap narrowing effect induced by the channel strain as well as the increased mobility, both tend to enhance the impact ionization rate [16,17], and may potentially worsen the hot-electron degradation in the strained devices. In Fig. 6.3(a), it is also interesting to note that the substrate current in the SiN-removal samples is slightly larger than the control counterparts when the channel length is short. This might be due to the additional thermal budget (e.g., 780 ˚C) by the SiN deposition process that tends to reduce the implant damage located close

to the source/drain region, as mentioned in Chapter 5, and thus reduces carrier scattering effect. In addition, it is clearly seen that I_{sub} increases as the thickness of SiN capping layer increases in Fig. 6.3(b), due probably to the mobility increase as the SiN capping thickness increases.

However, the impact ionization ratio (I_{sub} /I_D) is nearly the same no matter how thick the SiN capping layer is, as shown in Fig. 6.4. This result is different from the result of I_{sub}. We have found in previous chapter that a longer SiN deposition time would result in a slightly thicker gate oxide. Moreover, dramatic bandgap narrowing effect occurs due to the channel strain, as indicated in Chapter 5. These factors would reduce the I_{sub} /I_D in the thicker SiN capping layer. Hence, devices with a thicker SiN capping no longer have a larger I_{sub} /I_D. However, the I_{sub} /I_D of the SiN-removal samples is also larger than the control one. It is clearly seen that devices with thinner gate oxide thickness have larger value of I_{sub} /I_D (the difference between device x & y is about 0.4 nm) in Fig. 6.4(b) under the same drain voltage. Since the electric field in Eq. (6-2) is affected by the gate oxide thickness, it is expected that strained devices with thinner gate oxide would have aggravated hot carrier effect.

6.3-2 Hot Carrier Stress

Typical results of hot-electron stressing for the three splits of samples are shown in Fig. 6.5. Channel length and width of the test devices are 0.5 μm and 10 μm, respectively. The devices were stressed at V_{DS} = 4.5 V and V_{GS} at maximum substrate current. The I_D-V_G characteristics at V_{DS} = 0.05 V were measured before and after the stress to examine the degradation caused by the hot electrons. As can be seen in Fig. 6.5, the degradation is the worst in the SiN-capped sample among the three splits. The aggravation is alleviated with SiN removal, though the resultant degradation is still

worse than the control sample.

Figure 6.6 shows the shift of threshold voltage (ΔV_{th}), increased interface state density (ΔN_{it}), and degraded peak transconductance (ΔG_m) as a function of the stress time. As mentioned above, the device with channel strain depicts aggravated degradation in terms of larger shifts in these parameters. As mentioned above, the bandgap narrowing effect and the increased carrier mobility in the strained channel devices [16,17] are postulated to be the two primarily culprits for the aggravated hot carrier degradation in the SiN-capped samples. These two factors may increase the impact ionization rate in the device, which is evidenced in Fig. 6.3, and lead to higher degradation.

In Figs. 6.5 and 6.6, it is noted that the device with SiN-removal also depicts much severe degradation than the control device, even though the channel strain has been eliminated by the SiN removal. This phenomenon clearly indicates that the SiN deposition process itself may result in the enhanced damage effect in the short-channel devices. According to previous reports [18,19], interface states could be generated due to the breaking of Si-H bonds by hot electrons, and the generated interface states would greatly degrade the device performance. Figure 6.7 shows the charge pumping current of fresh devices. As mentioned previously in Chapter 5, SiN-removal sample depicts the smallest charge pumping current (Icp) among all splits of samples. This is ascribed to the use of H-containing precursors (e.g., SiH_2Cl_2 and NH_3) in the SiN deposition step, and the incorporated hydrogen species tends to passivate the interface states. As a result, lower charge pumping current is obtained for the SiN-removal sample. Note that such reduction in interface states comparing with the control sample is not observed for the strained devices. Additional interface states generation due to the channel strain could be the origin for higher Icp in the strained devices.

Although the additional H species incorporated in the SiN-removal device could reduce the interface state density in fresh devices, the extra Si-H bonds would also be responsible for the worsened hot-carrier degradation shown in Figs. 6.5 and 6.6. Figure 6.8 shows the difference in Icp before and after 5000 sec hot carrier stress among the three splits of samples. It is seen that more interface states than those in the control sample are actually generated in the SiN-removal devices, implying that the extra hydrogen species from SiN layer are an important contributor for the aggravated degradation. Figure 6.9 illustrates the 10-year reliability projections for the three splits. Lifetime was defined as 30 mV of ΔV_{th}. Devices with SiN capping were observed to endure lower V_{DS} as compared with the control and SiN-removal samples. Due to hydrogen species, the SiN-removal devices have worse lifetime than the control ones.

The relationship between hot carrier degradation and the thickness of SiN capping was addressed below. Figure 6.10 shows the ΔV_{th} and ΔN_{it} of the devices with three different SiN thicknesses at V_{DS} = 4.5 V and V_{GS} at maximum substrate current. Similar to the result shown in Fig. 6.4(a), difference among the three splits of SiN capping is slight. In our case, the hot carrier degradation is independent of the SiN capping thickness due to gate oxide variation and bandgap narrowing. Based on the above results we conclude that both the deposited SiN layer and the deposition process itself have significant impacts on the device operation and the associated reliability characteristics. For threshold voltage control, not only the bandgap narrowing effect induced by the channel strain but also the thermal treatment associated with the SiN deposition need to be taken into account. This work shows that hot-electron degradation is negatively affected when the SiN is deposited over the gate, even if the SiN is removed later and the channel strain is relieved. The existence of extra Si-H bonds at the oxide/Si interface due to the deposition of SiN is presumably the main cause for this

observation. Optimization of the deposition is thus necessary for improving the immunity of the strained devices to the hot-carrier effect. For example, using deuterium-containing precursors or deuterium annealing process [20] could be helpful in this regard.

6.3-3 Lateral Distribution of Interface State

The measurement presented in section 6.2 was used to extract lateral distribution of interface state. Firstly, Fig. 6.11(a) shows the normalized charge pumping current measured under single junction configuration for three splits (control, SiN capping, and SiN-removal). It should be noted that the local V_{th} and V_{fb} across the MOSFET are not uniform due to the lateral doping variation, as illustrated in Fig. 6.11(b). In order to detect the interface states, the pulse of measurement must undergo the cycles of accumulation-inversion-accumulation. Therefore, there should be no Icp if high-voltage level (V_h) is lower than the minimum V_{th} under the gate. Only when V_h starts to exceed local V_{th} under the gate will the Icp begin to grow. Before V_h reaches the maximum local V_{th} in the channel, only interface states residing near the drain side will contribute to Icp, as the needed electrons cannot yet flow to the drain side from the source. The dopant profile of drain junction can be observed when V_h is less than 0.5V, as depicted in Fig. 6.11. It can be seen that all splits have nearly the same junction profile on the drain side.

If we assume that interface state density is spatially uniform along the channel, which can be written as

$$I_{cp,\max} = qfN_{it}WL \tag{6-3}$$

where f is the gate pulse frequency, W the channel width, and L the channel length. In Fig. 6.12, the corresponding Icp(V_h) comes from the interface state distributed between

the gate edge and the position in the channel where its local V_{th} is equal to V_h, that is

$$I_{cp}(V_h) = qfN_{it}Wx \tag{6-4}$$

where x represents the distance from the gate edge to the position where $V_{th}(x) = V_h$. Comparing Eq. (6-3) and (6-4), we can derive

$$x = \frac{LI_{cp}(V_h)}{I_{cp,\max}} \tag{6-5}$$

Figure 6.13 shows the local V_{th} versus distance x of the control and samples with SiN deposition of 300 nm. Basically, the lateral doping profile is nearly the same as that shown in Fig. 6.11, except for the difference of local V_{th}. Bandgap narrowing induced by strain-channel mentioned in Chapter 5 is mainly responsible for the variation of V_{th}. Moreover, the local V_{th} decreases sharply as x is smaller than 0.07 μm. we can speculate that the drain junction is located near x = 0.07 μm.

After hot carrier stress, the incremental charge pumping current, ΔIcp, at a certain V_h is proportional to the number of generated interface traps from the gate edge to the point x, that is

$$\Delta I_{cp} = qfW\int_0^x N_{it}(x)dx \tag{6-6}$$

Therefore, the Nit(x) generated by the hot carrier stress can be expressed as follows:

$$N_{it}(x) = \frac{d\Delta I_{cp}}{dx}\frac{1}{qfW} = \frac{d\Delta I_{cp}}{dV_h}\frac{dV_h}{dx}\frac{1}{qfW} \tag{6-7}$$

The derived lateral profiles of the interface states extracted by Eq. (6-7) are shown in Fig. 6.14 after 100 sec of hot carrier stress. Actually, we can directly derive the damage region and amount of interface state generated by hot carrier stress from Fig. 6.14. One can see that the damage region is confined within the drain edge to 0.1μm into the channel in all splits. It is reasonable that the hot carrier stress belongs to edge

effect stress. It is obviously seen that interface state generation sharply increases in SiN capping samples nearby the drain region, and induces the variation of local V_{th}. The lateral profile of Icp is related to the local V_{th} near source and/or drain region. The result is consistent with Fig. 6.8 that the device with SiN capping has a larger Icp at V_{base} = -2V. According to the above discussions, the aggravated hot carrier stress of the SiN-removal devices is due to the hydrogen species. In fact, hydrogen species would pile up at the source/drain edge during the SiN deposition. This explains why the SiN-removal devices have larger interface state generation than control devices.

6.4 Summary

Both the deposited SiN layer and the deposition process itself have significant impacts on the device operation and the associated reliability characteristics. This work shows that hot-electron degradation is negatively affected when the SiN is deposited over the gate, even if the SiN is removed and the channel strain released later in the process. Nevertheless, the accompanying bandgap narrowing and the increased carrier mobility tend to worsen the hot-electron reliability. In this aspect, attentions should also be paid to the SiN deposition process itself. Owing to the use of hydrogen-containing precursors, abundant hydrogen species is incorporated in the oxide that may also contribute to the hot-electron degradation. The edge effect of hot carrier stress is also a factor to cause reliability degradation in SiN-removal devices. Optimization of both SiN deposition process and the film properties are thus essential to the implementation of the uniaxial strain in NMOS devices. In addition, the hot carrier degradation of devices with SiN capping is independent of SiN thickness due to gate oxide thickness variation and bandgap narrowing.

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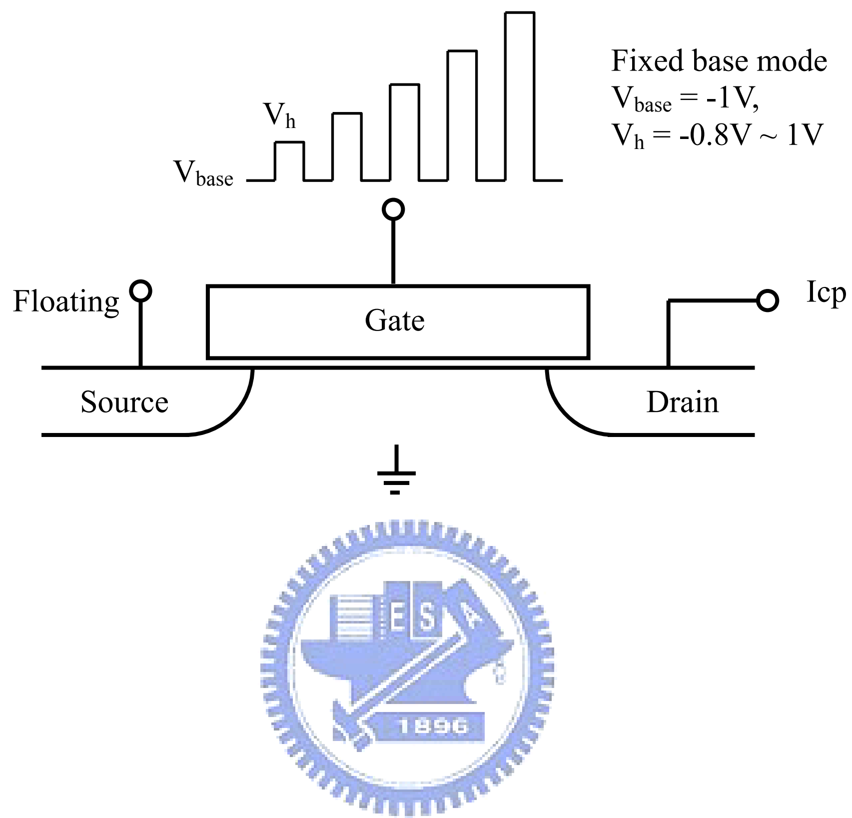


Fig. 6.1 The measurement setup of single junction charge pumping measurement.

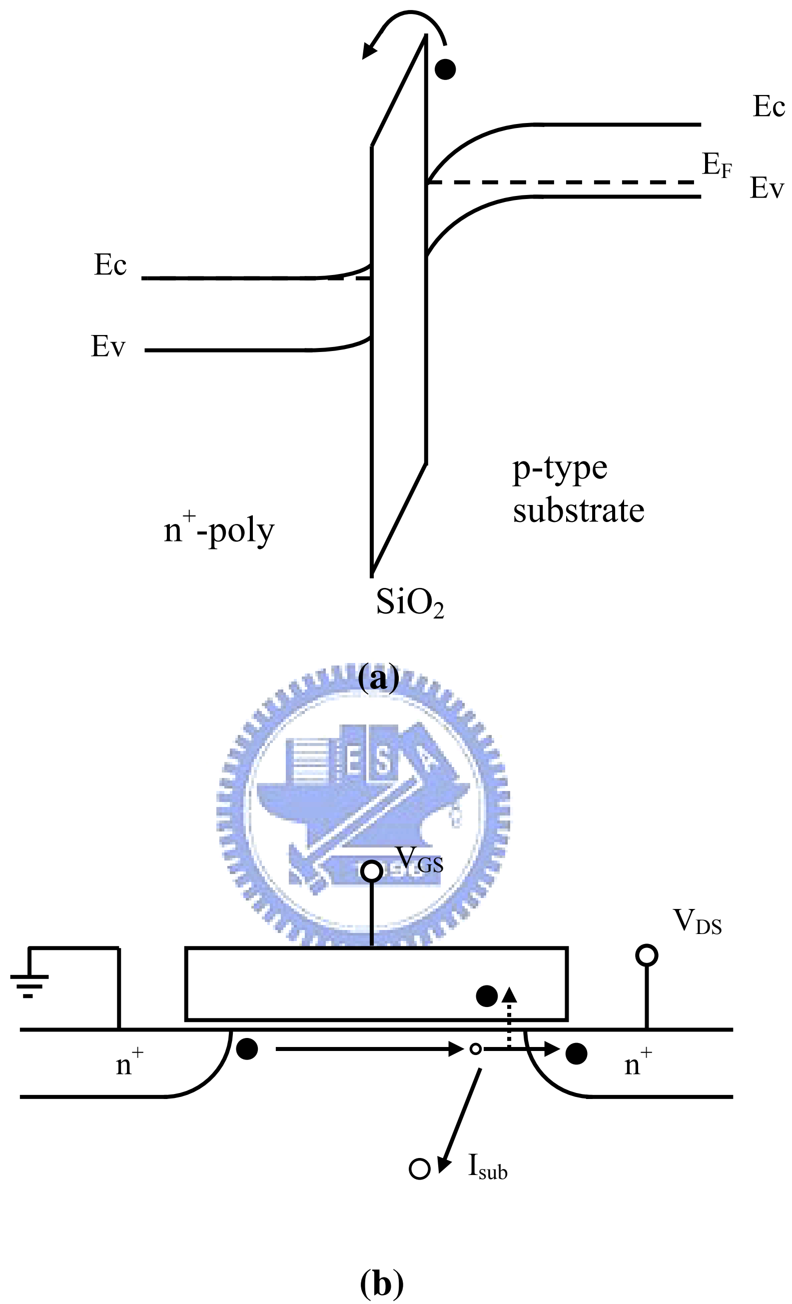
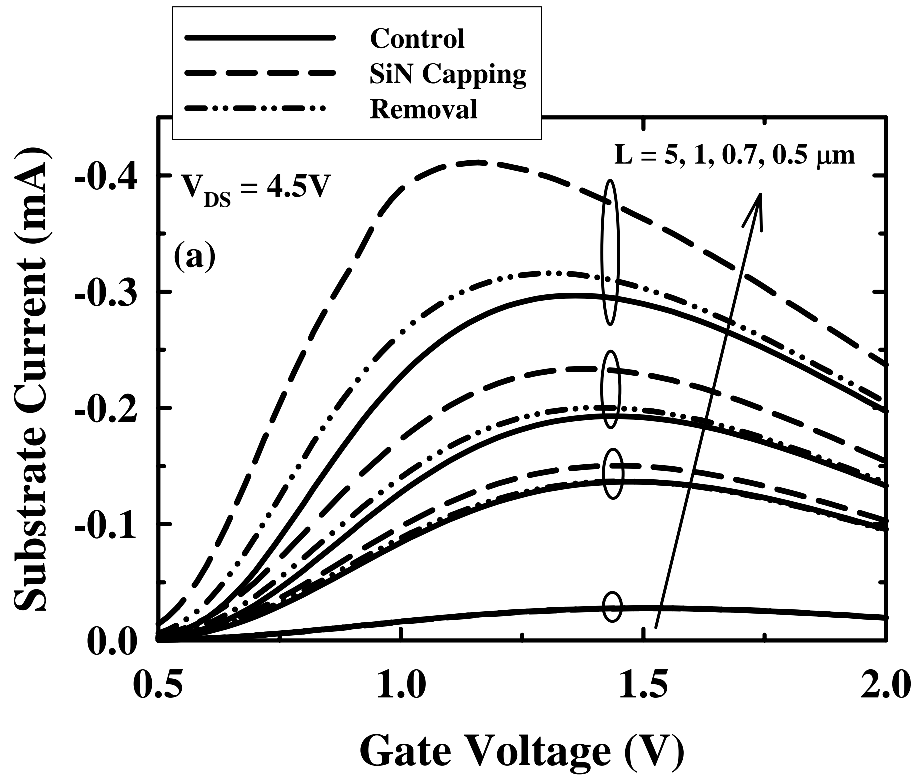


Fig. 6.2 (a) Energy band diagram for conventional NMOS on a p-type substrate. (b) Illustration showing impact ionization occurring close to the drain in an n-channel MOSFET.



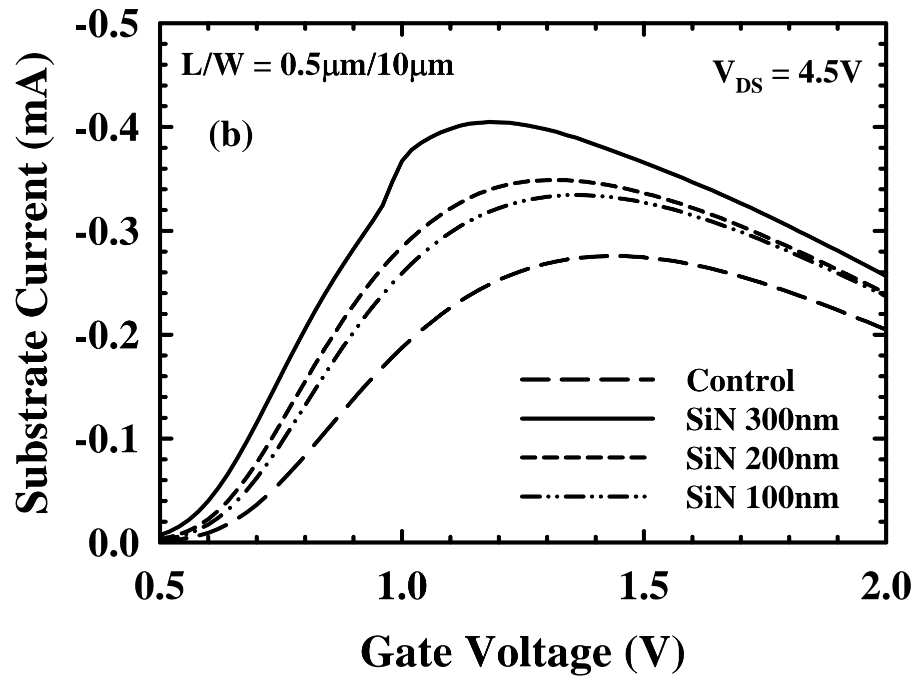


Fig. 6.3 (a) Substrate current versus gate voltage with channel lengths of 0.5 μm, 0.7 μm, 1 μm, and 5 μm. (b) Substrate current versus gate voltage in devices with three different SiN capping thicknesses.

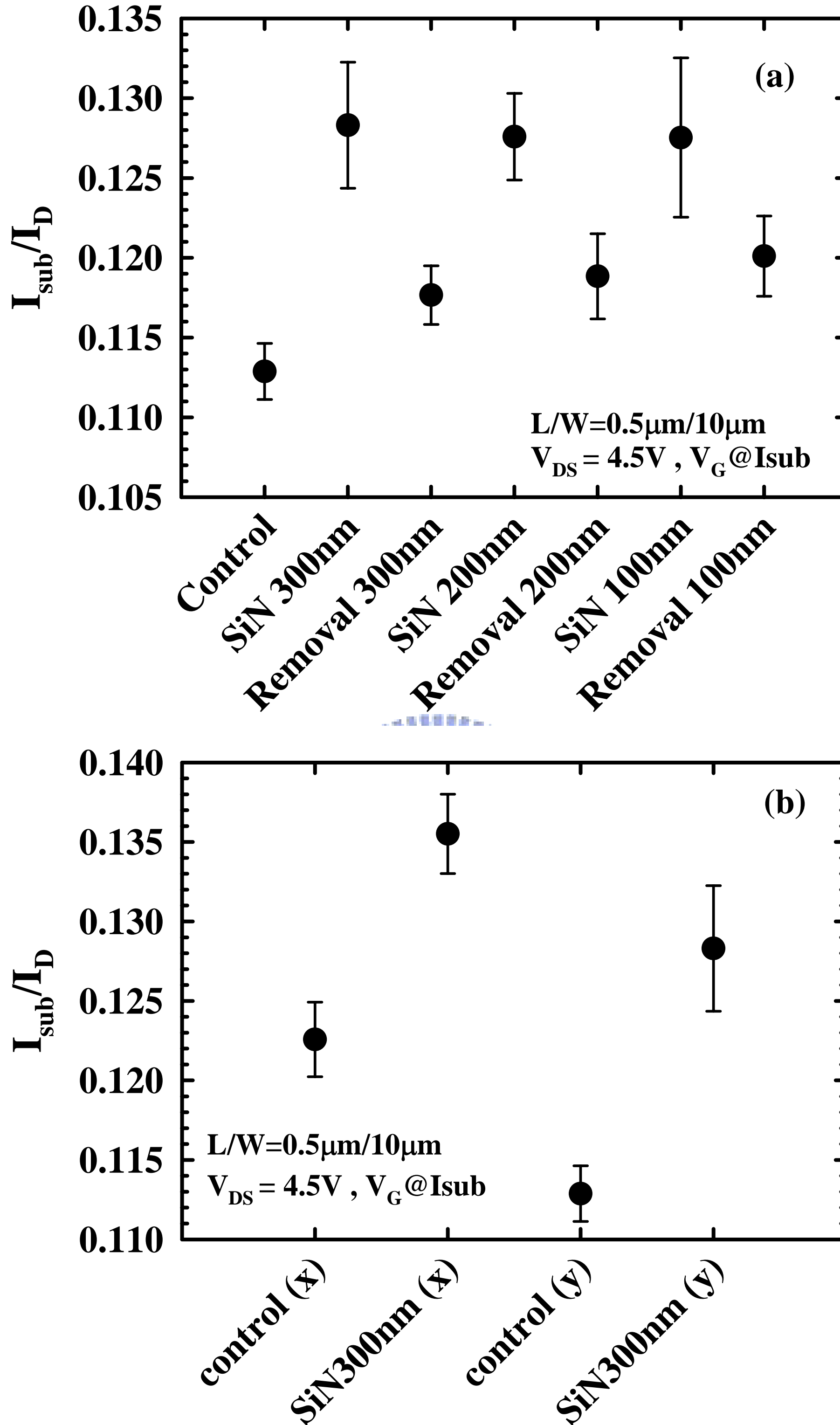


Fig. 6.4 (a) The impact ionization rate (I_{sub}/I_D) in all splits. (b) The I_{sub}/I_D under different gate oxide thickness. The gate oxide thickness between x and y is about 0.4 nm.

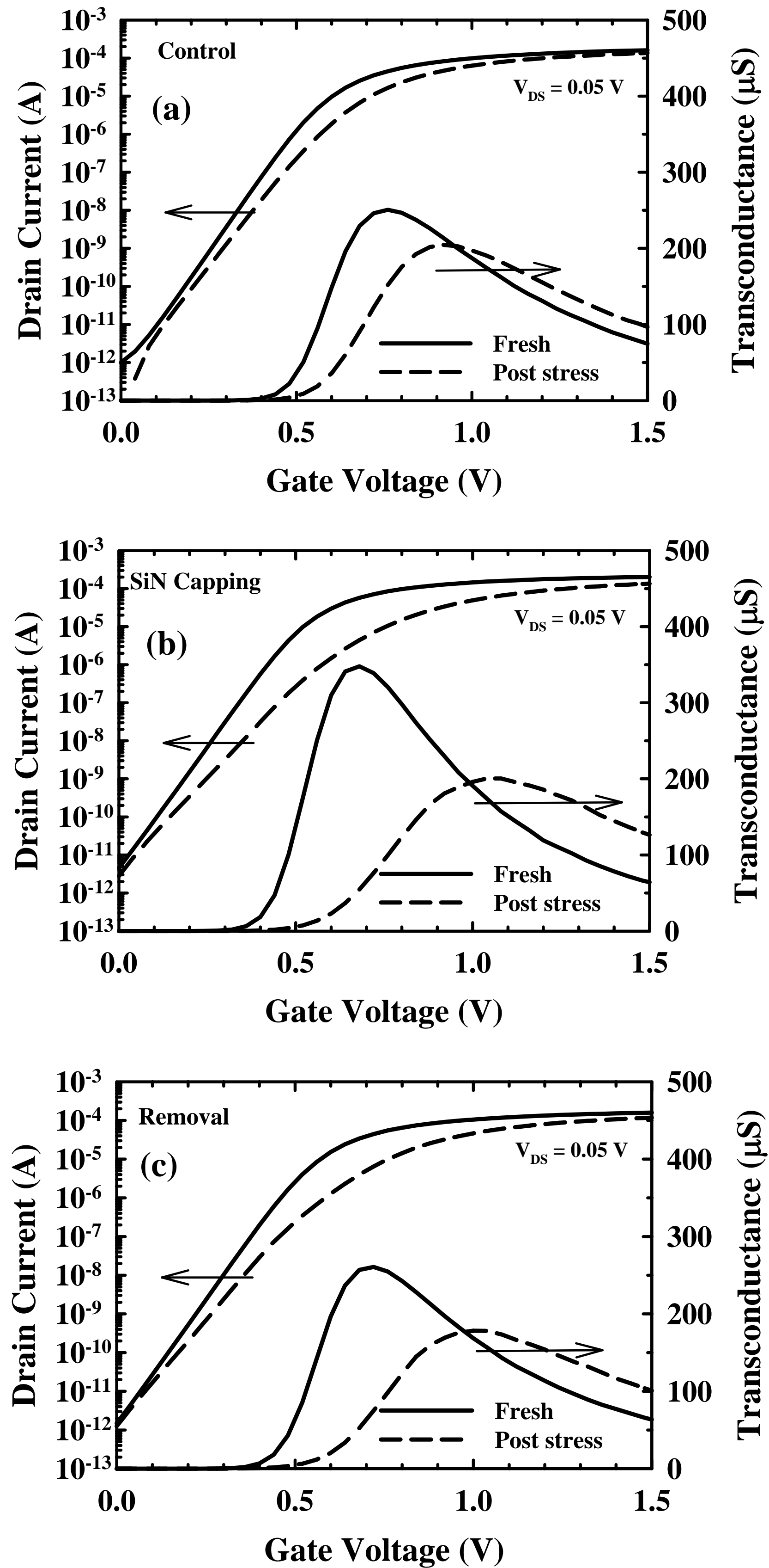


Fig. 6.5 Subthreshold characteristics and transconductance of devices before and after 5000 sec hot-electron stressing. Channel length/width = 0.5μm/10μm. (a) Control sample. (b) SiN-capped sample. (c) SiN-removal sample.

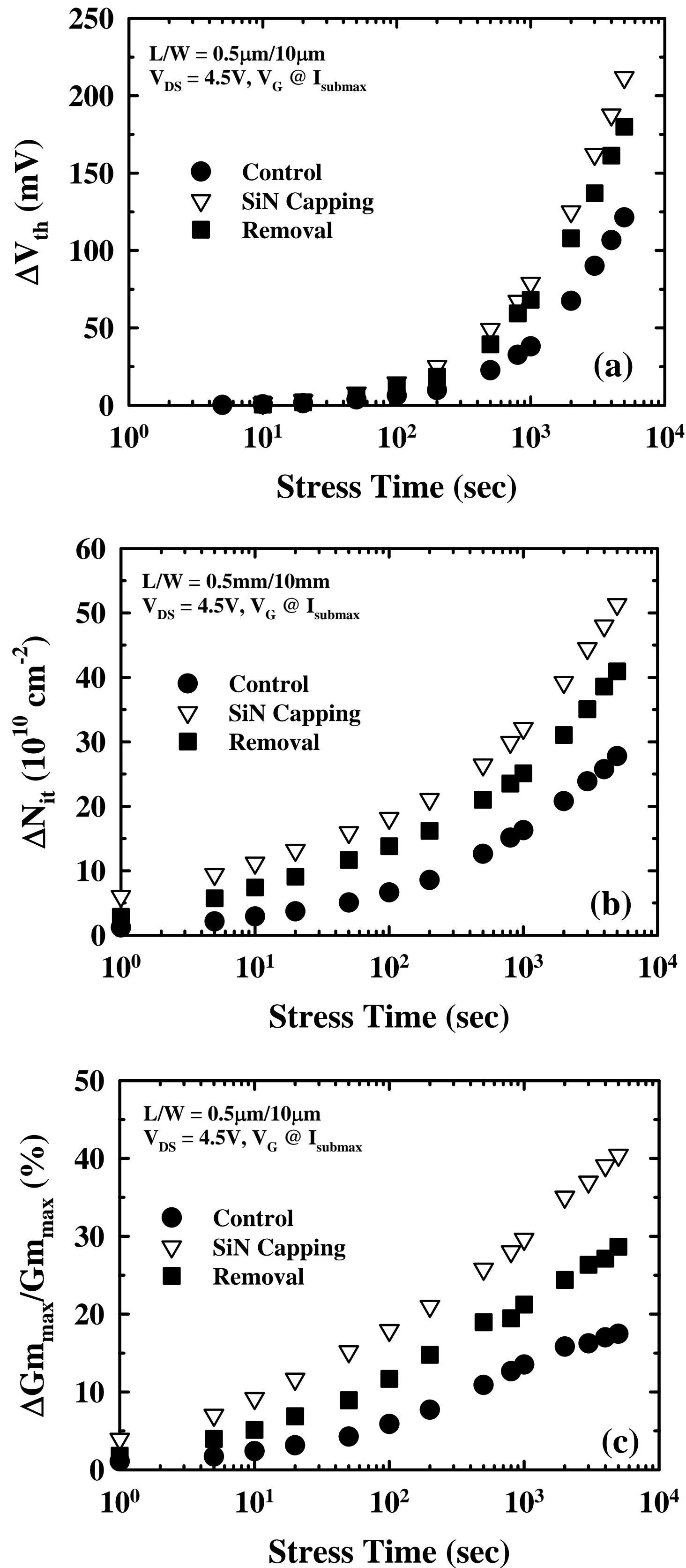


Fig. 6.6 Results of hot-electron stressing at V_{DS} = 4.5 V and maximum substrate current performed on all three splits of devices with channel length/width = 0.5μm/10μm. (a) Threshold voltage shift; (b) interface state generation; (c) transconductance degradation.

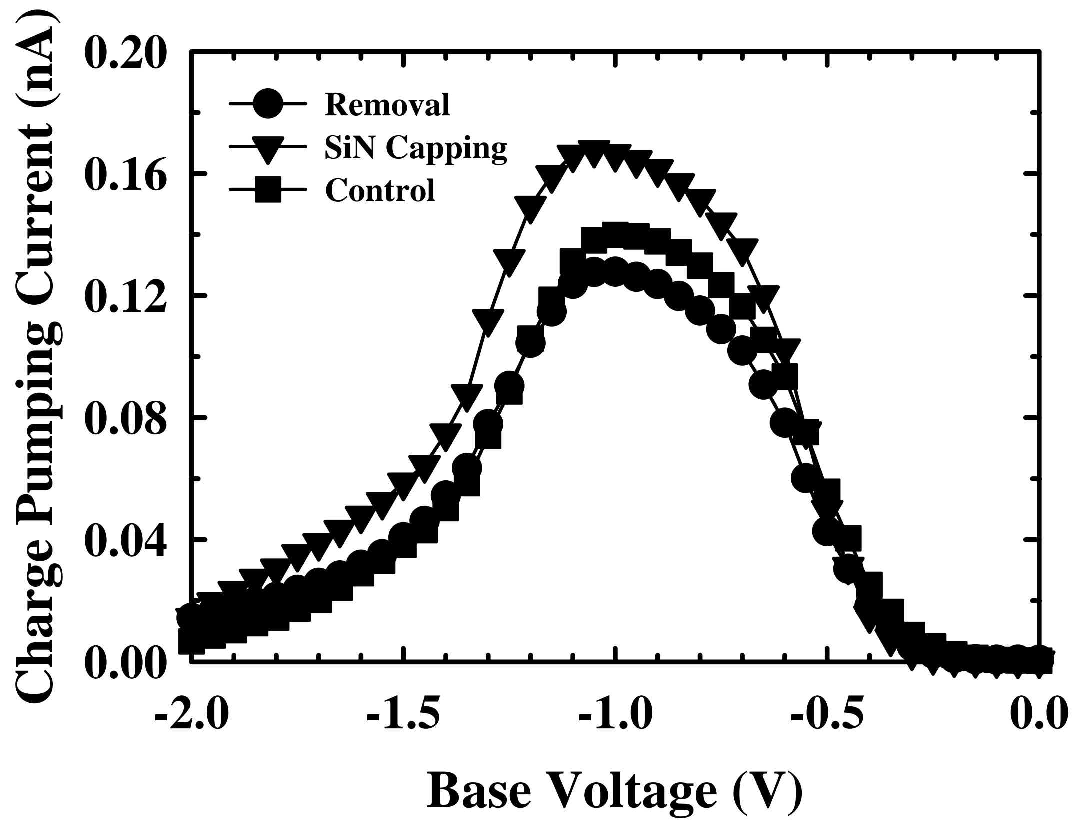


Fig. 6.7 Charge pumping current for the three splits of fresh devices with channel length/width = 0.5μm/10μm. The measurement was performed under fixed amplitude of 1.5 V and frequency of 1 MHz.

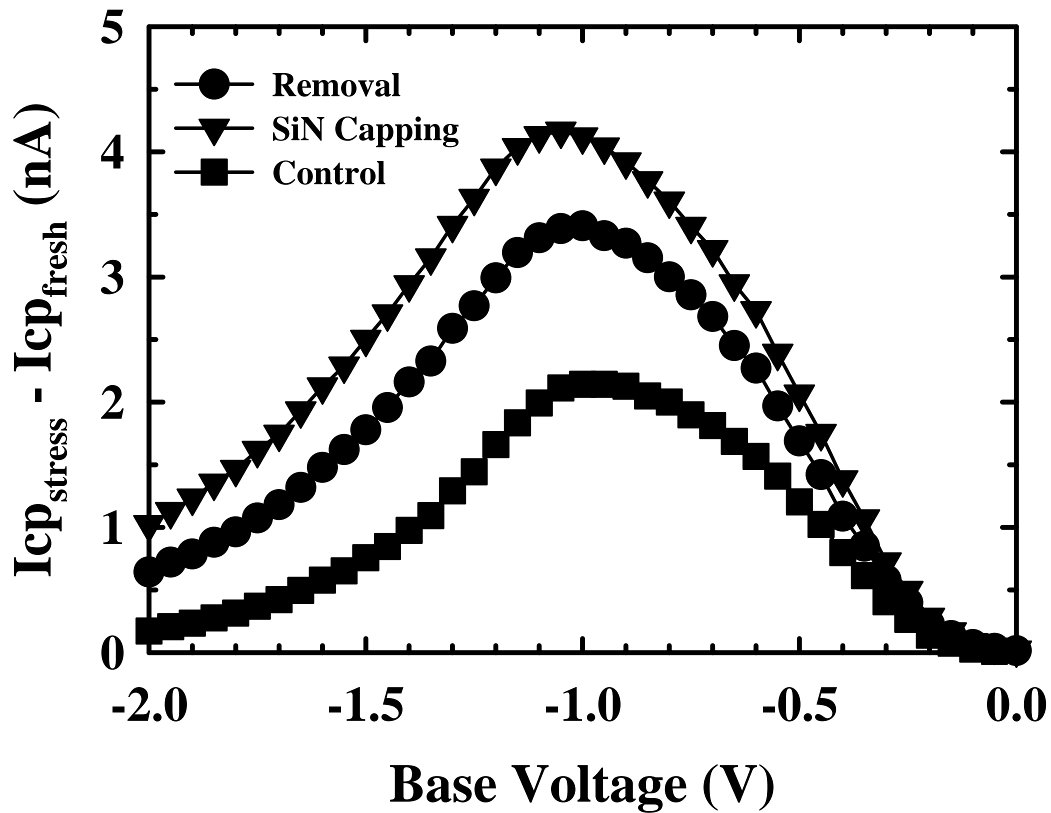


Fig. 6.8 The increase in charge pumping current after hot carrier stress ($V_G@_{Isub,max}$ and V_{DS} = 4.5 V) for the three splits of devices with channel length/width = 0.5μm/10μm.

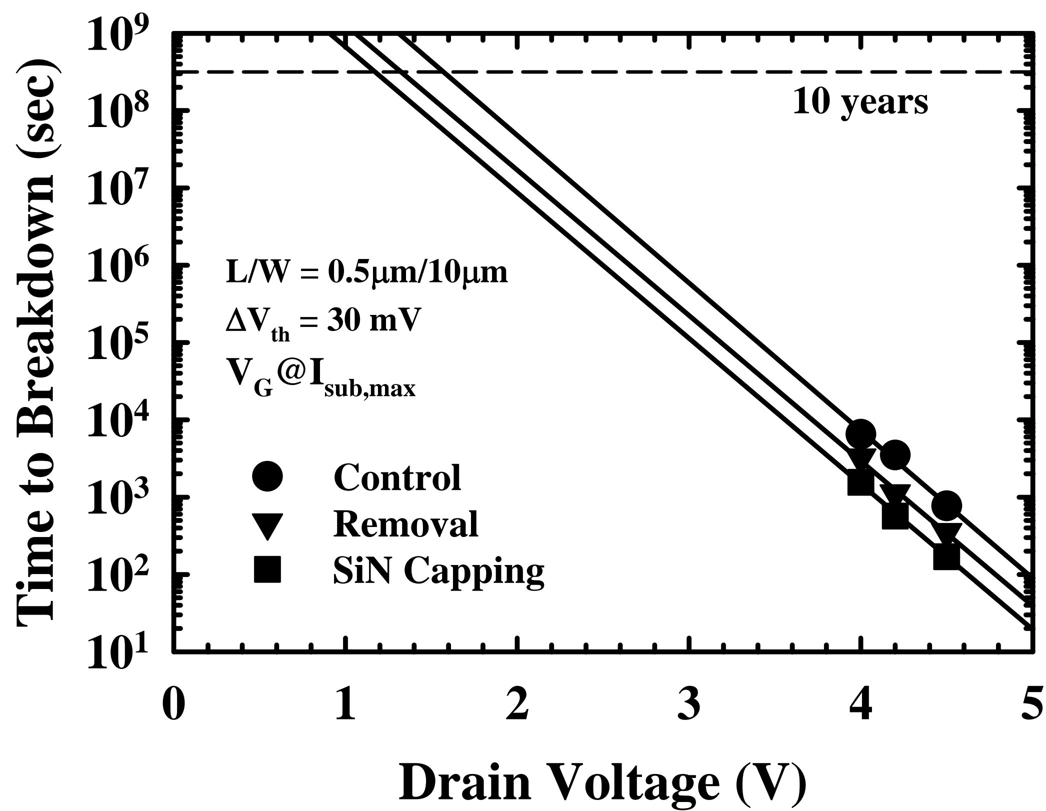
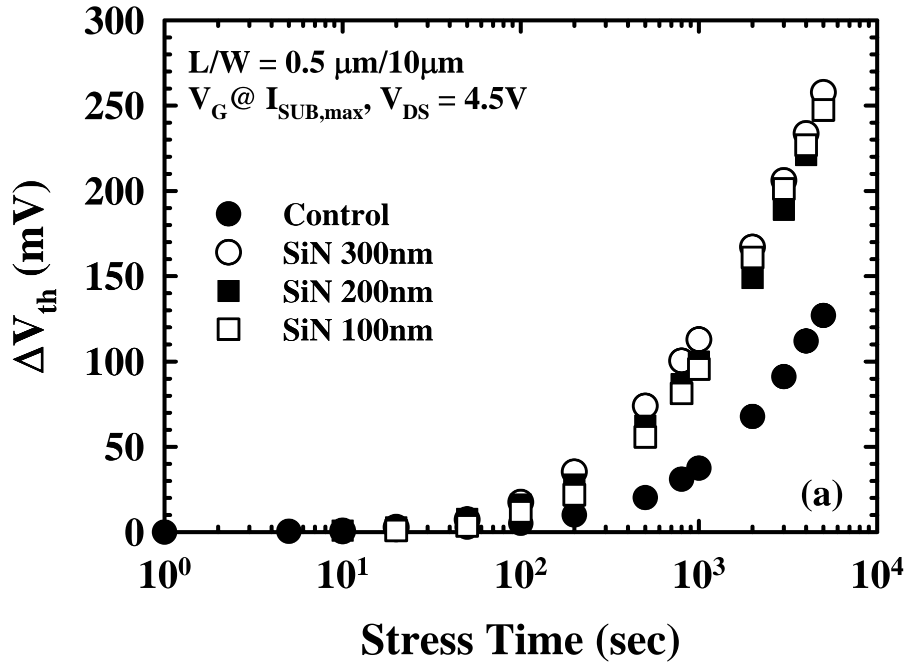


Fig. 6.9 10-year lifetime projection for the control, SiN-removal, and SiN capping samples.



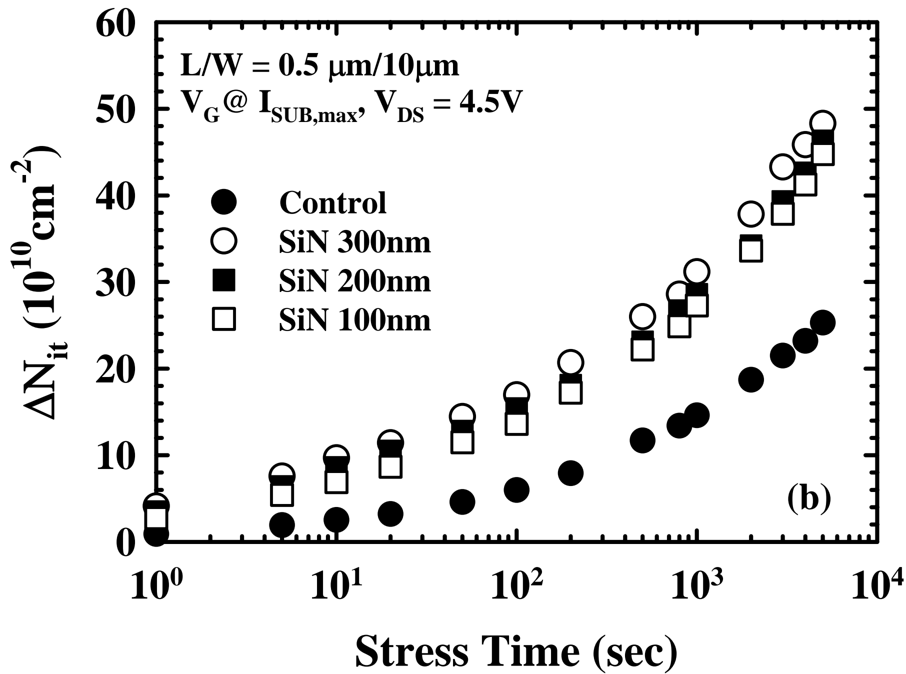
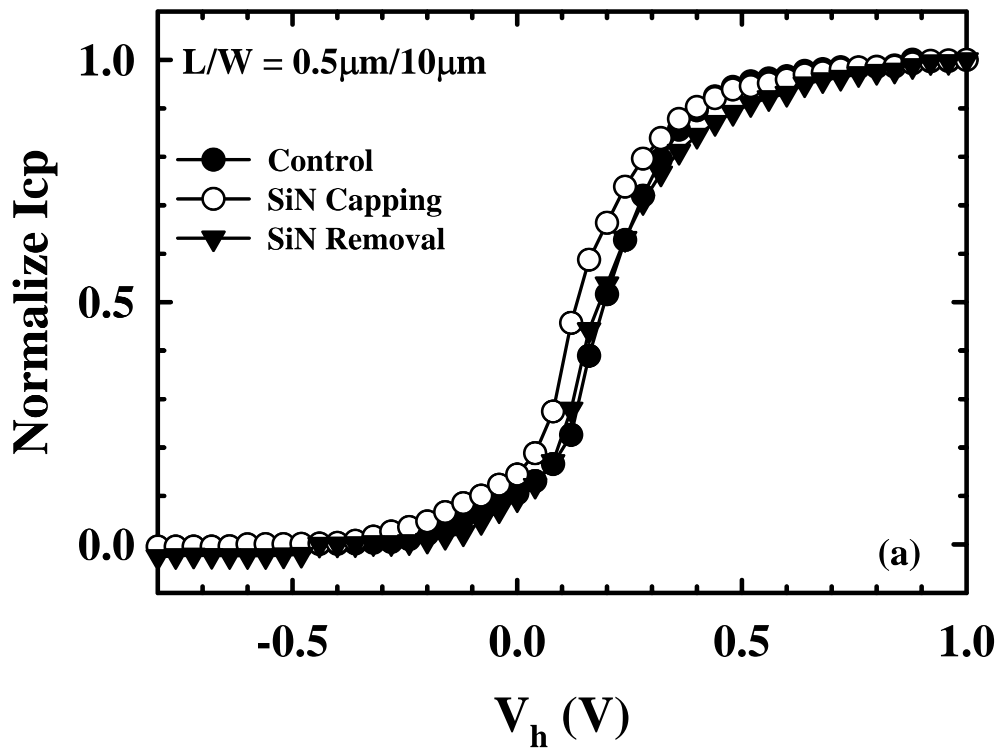
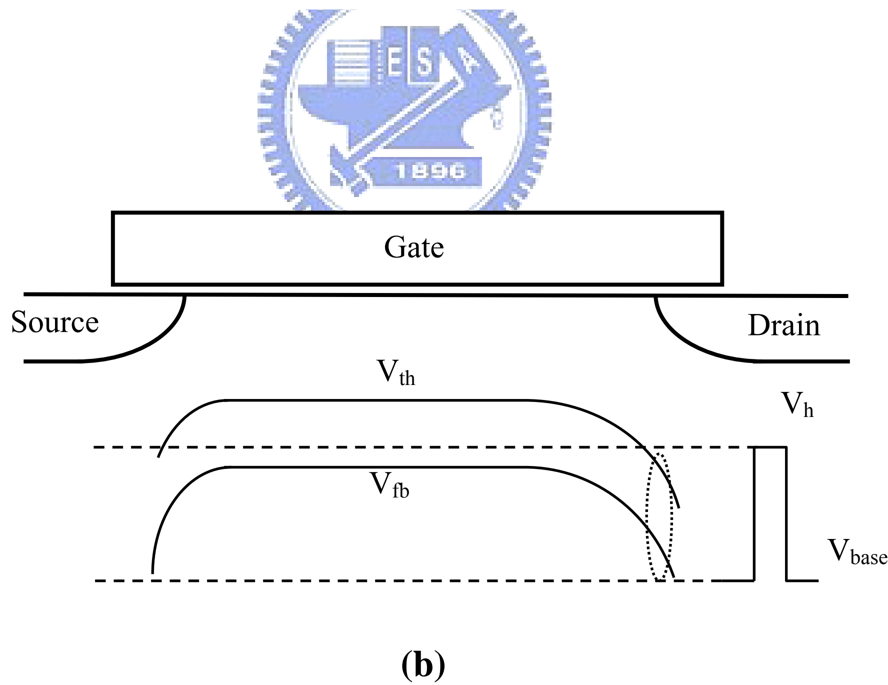


Fig. 6.10 Results of hot-electron stressing at V_{DS} = 4.5 V and maximum substrate current performed on all three splits of devices with channel length/width = 0.5μm/10μm among SiN capping thickness of 100 nm, 200 nm, and 300 nm. (a) Threshold voltage shift; (b) interface state generation.





(b)

Fig. 6.11 (a) The normalized single-junction charge pumping current of the three splits of test samples. The lateral dopant profile of all splits is nearly the same. (b) Illustration of nonunifrom distribution of local threshold voltage and flat-band voltage across the device caused by variation of lateral doping concentration.

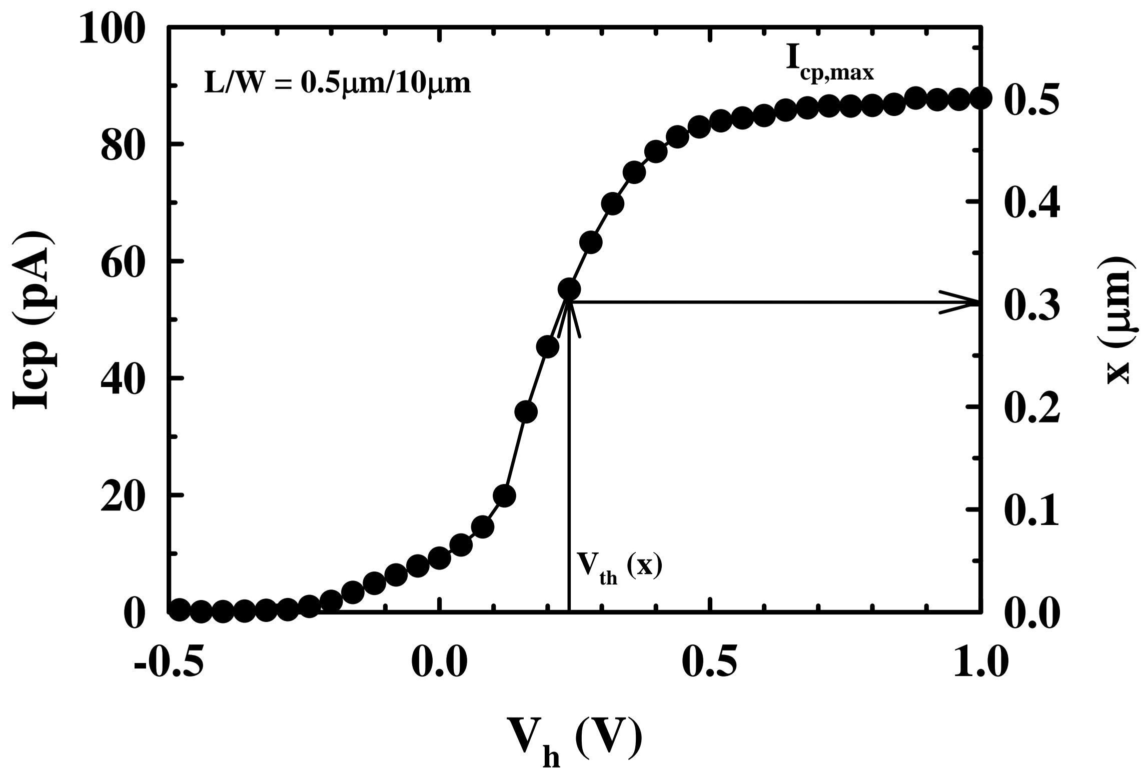


Fig. 6.12 Deriving the relationship between local threshold voltage and lateral distance x from the single junction charge pumping data of the control device.

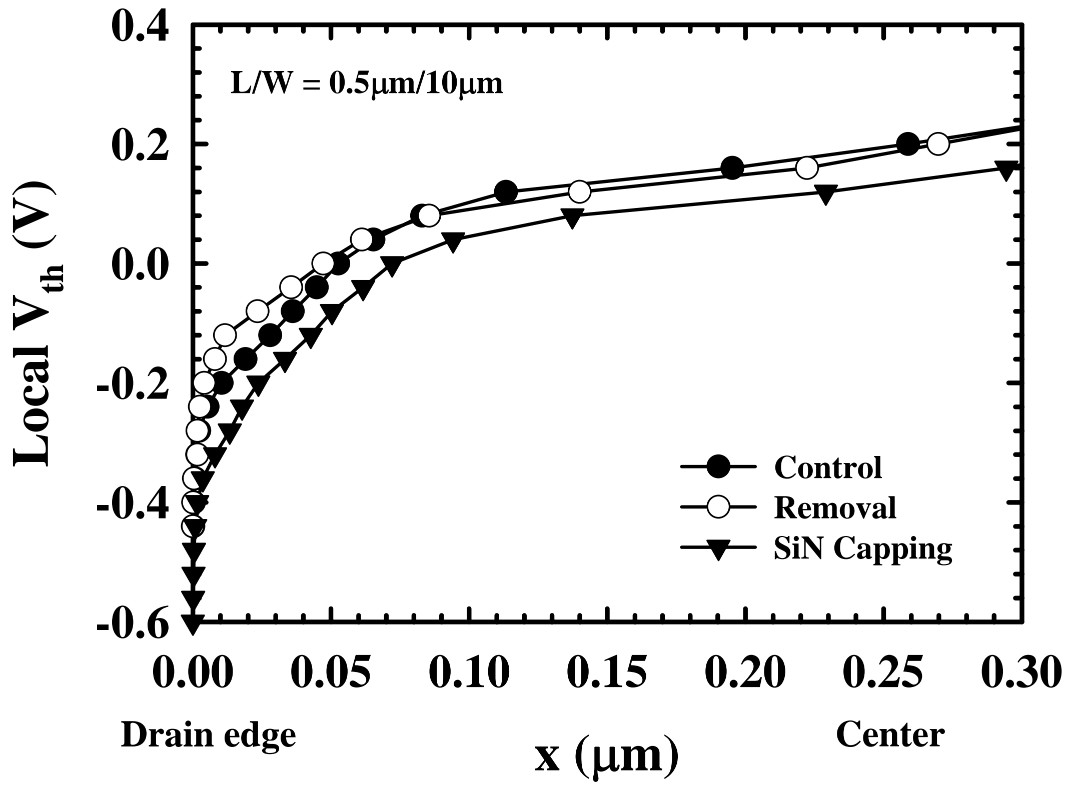


Fig. 6.13 The derived lateral profile of local threshold voltage near the graded drain junction.

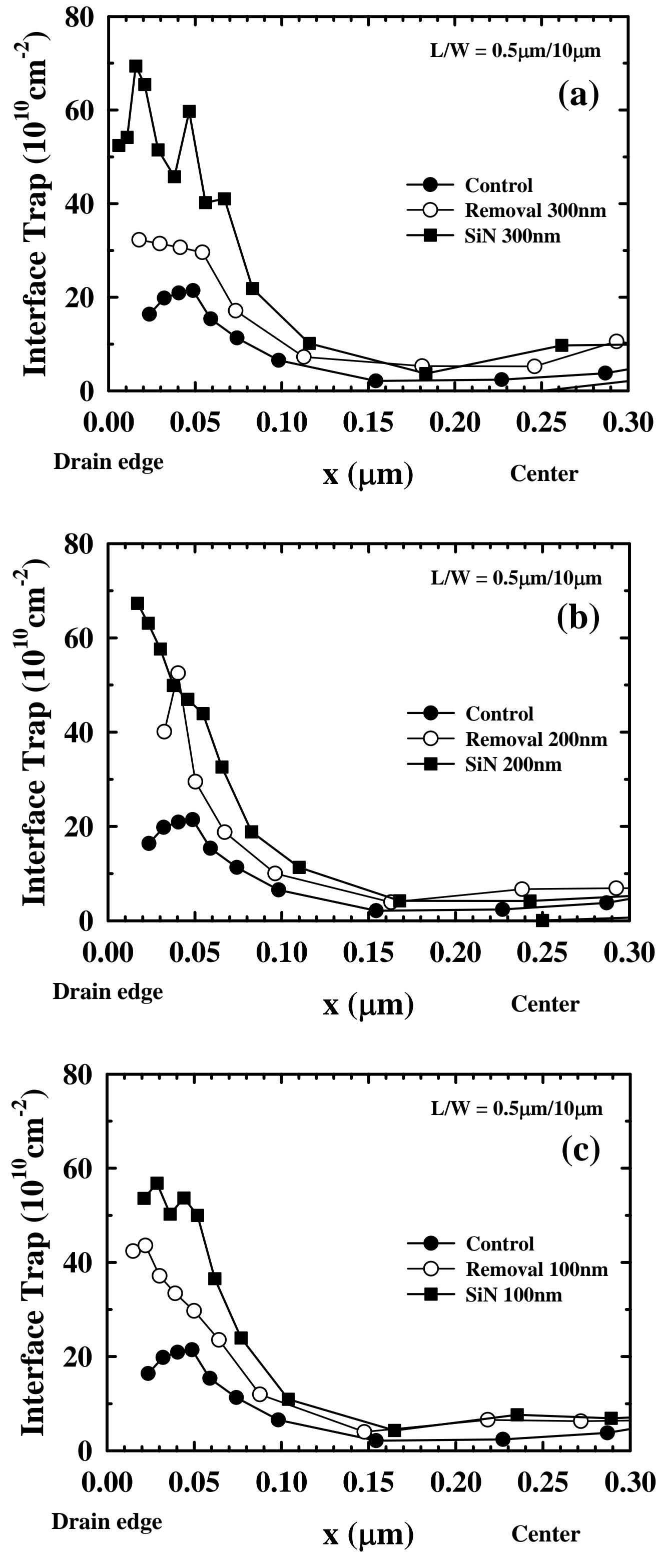


Fig. 6.14 Lateral profile of interface state generation under three different SiN capping thickness. (a) 300 nm. (b) 200 nm. (c) 100 nm.

Chapter 7

Fabrication and Characteristics of Nano-Scale Devices on SOI Substrates

7.1 Introduction

Continuous device scaling since the invention of IC resulted in dramatic improvements in both device density and performance. However, as IC technologies enter the deep nano-scale regime, how to keep short channel effects at bay is extremely important. Conventional strategies for scaling the planar CMOS structure include the use of ultra-thin gate dielectric, heavy channel doping, and ultra shallow junction. However, all these methods face severe challenges and are not easy to implement in the nano-technology era. MOSFETs with ultra-thin-body (UTB) [1] and/or double-gate [2] schemes are more scalable than conventional bulk-Si structures.

Among these advanced structures, quasi-planar FinFET built on SOI wafers receives a lot of attention recently. FinFET belongs to the family of double-gate (or tri-gate) SOI transistors, in which the channel potential and carrier conduction are more effectively controlled by the gate configuration. FinFET offers superior scalability pertaining to the double-gate structures. Together with a process flow and layout compatible with conventional MOSFETs [3-5], FinFET represents a very attractive and useful approach in nano device fabrication. On the other hand, SB FinFET using metallic silicide in lieu of heavily doped semiconductor as the source/drain material [6] has also been proposed for future nano-scale device applications [7]. It received much attention with their superiority

in suppressing the short channel effects. However, conventional SB devices suffer from low driving current due to large Schottky barrier height at the source region. Several metal silicide materials were investigated to alleviate this problem, i.e., $ErSi_2$ for NMOSFET and PtSi for PMOSFET [8], though the improvement is still limited.

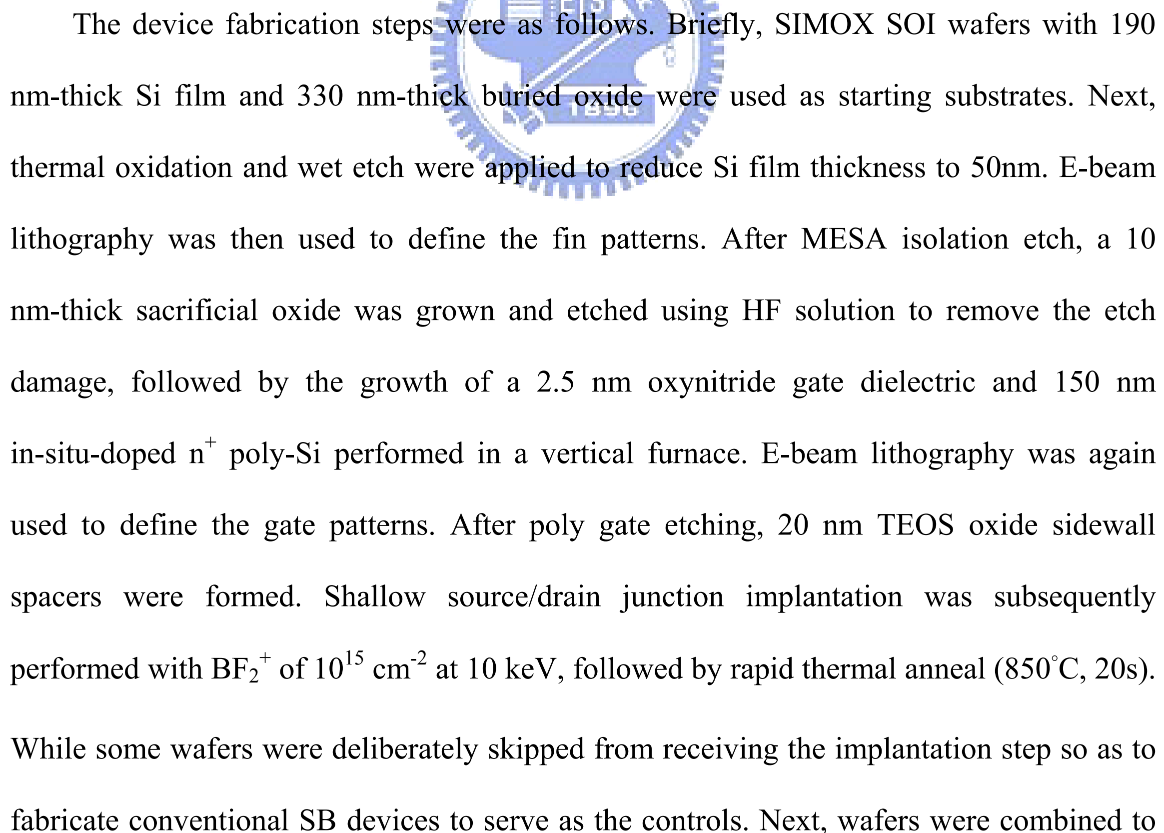
Ultra thin body (UTB) SOI has also been proposed as a potential candidate for future device manufacturing. The ultra-thin silicon body is effective in reducing the off-state current flowing through the body inherent in conventional planer CMOS structures [9]. Nevertheless, the large parasitic source/drain resistances associated with the thin Si film adversely affect device current drive. To alleviate this shortcoming, raised source/drain structure has been proposed. Drive current increase by as much as 50 % have been demonstrated in UTB devices with raised source/drain [10, 11]. Selective epitaxial growth of Si [10] and SiGe [12] by chemical vapor deposition (CVD) has been successfully employed for forming the raised source/drain. It has also been shown that SiGe-epitaxy is more effective in reducing the junction series resistance and contact resistance in PMOS devices than Si [13]. The smaller bandgap of SiGe is conducive to the reduction of Schottky barrier height at the metal-semiconductor interface [14]. In addition, the dopant activation temperature is much lower with SiGe epitaxy, which is crucial for future implementation of high-*k* gate dielectric and metal gate electrodes [15]. Also should be noted that all the above-mentioned prior works belong to the standard “gate-first” scheme. This means that the post S/D-implant annealing may hinder the integration of high-*k* gate dielectric and metal gate, which are essential for future nano CMOS manufacturing.

In this thesis, we propose and demonstrate an approach for Schottky barrier height engineering with PtSi process using impurity segregation of boron. In this approach, BF_2^+ was implanted and activated to form a shallow junction before the silicidation. Afterwards,

the shallow junction was consumed by silicidation. Due to impurity redistribution, boron was piled up at silicide/Si interface, and the piled up profile was steeper with a high peak concentration than the original junction profile. The Schottky barrier height between the silicide source/drain and Si can be adjusted by the impurity segregation, and the drive current could be enhanced. In addition, another novel "gate-last" scheme for fabricating ultra-thin body (UTB) SOI PMOS transistor with SiGe raised source/drain is also proposed and demonstrated in this thesis. This scheme is suitable for the integration of high-*k*/metal gate modules, thus representing a promising method for nano CMOS fabrication.

7.2 Device Fabrication

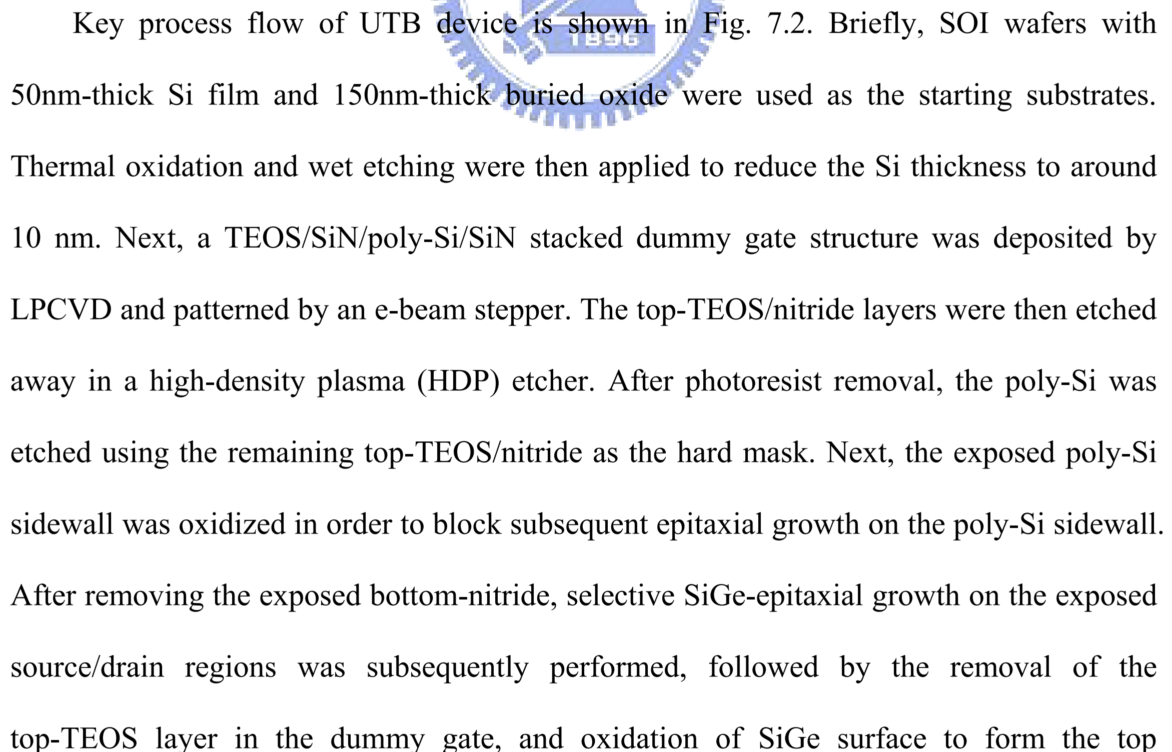
7.2-1 FinFET Device



The device fabrication steps were as follows. Briefly, SIMOX SOI wafers with 190 nm-thick Si film and 330 nm-thick buried oxide were used as starting substrates. Next, thermal oxidation and wet etch were applied to reduce Si film thickness to 50nm. E-beam lithography was then used to define the fin patterns. After MESA isolation etch, a 10 nm-thick sacrificial oxide was grown and etched using HF solution to remove the etch damage, followed by the growth of a 2.5 nm oxynitride gate dielectric and 150 nm in-situ-doped n^+ poly-Si performed in a vertical furnace. E-beam lithography was again used to define the gate patterns. After poly gate etching, 20 nm TEOS oxide sidewall spacers were formed. Shallow source/drain junction implantation was subsequently performed with BF_2^+ of 10^{15} cm^{-2} at 10 keV, followed by rapid thermal anneal (850°C, 20s). While some wafers were deliberately skipped from receiving the implantation step so as to fabricate conventional SB devices to serve as the controls. Next, wafers were combined to

receive 50 nm Pt deposition on the wafer surface and annealed in a furnace at 450°C for PtSi formation. Un-reacted Pt was then removed in a diluted aqua regia solution. Finally, a 25nm-thick PE-TEOS passivation layer was deposited, followed by the formation of contact holes and aluminum pads. The key process flow is described in Fig. 7.1(a). It should be noted that BF_2^+ was implanted and activated to form shallow junctions before silicidation. In our scheme, the silicidation was carefully controlled to almost completely consume the entire doped silicon region, so that at the junction a large amount of boron species is piled up. As a result, a significant reduction in contact resistance at the Schottky junctions is achieved, and the device drive current is significantly improved. Cross section of the SB FinFET device is shown in Fig. 7.1(b).

7.2-2 Ultra-Thin Body SOI Device



Key process flow of UTB device is shown in Fig. 7.2. Briefly, SOI wafers with 50nm-thick Si film and 150nm-thick buried oxide were used as the starting substrates. Thermal oxidation and wet etching were then applied to reduce the Si thickness to around 10 nm. Next, a TEOS/SiN/poly-Si/SiN stacked dummy gate structure was deposited by LPCVD and patterned by an e-beam stepper. The top-TEOS/nitride layers were then etched away in a high-density plasma (HDP) etcher. After photoresist removal, the poly-Si was etched using the remaining top-TEOS/nitride as the hard mask. Next, the exposed poly-Si sidewall was oxidized in order to block subsequent epitaxial growth on the poly-Si sidewall. After removing the exposed bottom-nitride, selective SiGe-epitaxial growth on the exposed source/drain regions was subsequently performed, followed by the removal of the top-TEOS layer in the dummy gate, and oxidation of SiGe surface to form the top

passivation layer on the raised source/drain. The source/drain regions were implanted with BF_2^+ with a dosage of 5×10^{15} cm^{-2} at an energy of 30 keV. Spike RTA (1050 °C) was employed to activate implanted dopants and reduce the damage. The remaining dummy gate was subsequently removed, and a 6nm sacrificial oxide was grown on the channel surface. After stripping off the sacrificial oxide, a 2.5nm oxynitride gate dielectric and a 150nm in-situ-doped n^+-poly-Si were deposited, followed by gate patterning steps. Finally, contact holes and metal pads were finished.

7.3 Results and Discussion

7.3-1 Schottky Barrier FinFET Device

Figure 7.3 shows the subthreshold characteristics of SB FinFET. The off-state leakage can be effectively suppressed because of the field-induced-drain (FID) feature in the structure [16]. It is worth noting that conventional SB MOSFETs have very low drive current, and show large GIDL-like off-state leakage current inherent in ambipolar characteristics. In our previous work, we employed a sub-gate to form FID to effectively reduce this undesirable leakage and improve device performance [16]. Nonetheless, the FID approach requires additional metal connecting line with large applied voltage for the sub-gate, making it less attractive for ULSI manufacturing.

Table 7-I is the drain-induce-barrier-lowing (DIBL) characteristics of SB FinFETs having different fin widths and channel lengths. It can be seen that DIBL reduces as channel length increases under a fixed fin width, as expected. However, it is interesting to see that DIBL reduces as the fin width becomes narrower. This is because the gate electrode is effectively employed to control the potential and carrier conduction in the

channel region, especially when the fin width is smaller than the channel length. Hence, short-channel-effect would be suppressed in devices with narrower fin width. The subthreshold swing (SS) depicts the same trend, as shown in Table 7-II.

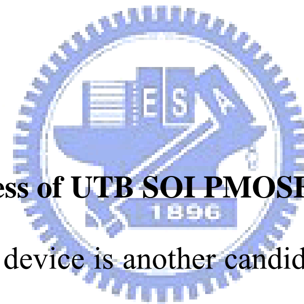
7.3-2 SB FinFET with Impurity Segregation

Although PtSi has low Schottky barrier for holes, the drive current of SB FinFET is still lower than that in the conventional device with heavily implanted S/D junction, as shown in Fig. 7.3. During the device fabrication, gate sidewall spacers are needed to avoid the bridging between the gate and S/D. As a result, a hiatus is created between the source-side Schottky contact and the channel region underneath the gate, further degrading the current drive. Recently, impurity segregation technique was used to fabricate Ni fully silicided gate in an effort to enhance the drive current [17]. Figs. 7.4 and 7.5 show subthreshold and output characteristics, respectively, of a fabricated device with L = 0.14 μm and Si fin width of 0.06 μm. The on-current is 225 μA/μm at V_G = -2.0V, V_D = -1.5V. On/Off current ratio reaches 10^9, and DIBL is 60 mV/V. These characteristics are superior to that of conventional SB devices. The impact of the hiatus between the Schottky contact and the channel region underneath the channel is significantly reduced by impurity segregation at the silicide/Si interface, thus the device performance is improved. Note that the high threshold voltage in our devices is primarily due to the use of n^+ poly-Si gate material used in our study for simplicity, and could be lowered when gate electrodes with suitable gate materials, such as p^+-poly and metal gate, are used.

Figure 7.6 shows the relationship between SS and fin width. SS shows a dependence on fin width, i.e., a smaller fin width depicts a smaller SS. This confirms that FinFET structure is indeed effective in suppressing short channel effects when fin width is smaller

or equal to 0.7 times channel length. When the fin width is about 60 nm, the subthreshold swing of the new SB PMOSFET is 73.5 mV/dec. The overall device performance is superior to that of the conventional SB device because of tri-gate structure and impurity segregation technology.

As shown in Fig. 7.7, the transconductance of the SB device is higher than that of the SB device with field-induced drain (FID) previously proposed by our group [16]. This is consistent with the above results. Figures 7.4 and 7.5 also compare the subthreshold and output characteristics, respectively, of SB devices with impurity segregation and FID. It can be seen that the device with impurity segregation is superior to the device with FID. The driving current of the SB device with impurity segregation is five times that of the SB device with FID.



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7.3-3 A Novel CMP-Free Process of UTB SOI PMOSFET

Besides FinFET, UTB SOI device is another candidate for future nano devices. In this section, we discuss the device characteristics of a novel UTB device fabricated without CMP process. Figure 7.8(a) shows a cross-sectional scanning electron microscope (SEM) picture of a dummy gate with channel length around 40 nm. It can be seen that the sidewall is very steep after the HDP etching. This is helpful for subsequent fabrication steps. Briefly, after poly-Si sidewall oxidation, the sidewall was slightly expanded, as shown in Figure 7.8(b). The sidewall oxide was used to cover the poly sidewalls and prevent the growth of Si during subsequent SEG step. Figure 7.9(a) shows an SEM of the device after dummy gate removal by wet etching techniques. We can see that the bottom of the trench is flat. This is ascribed to the high etch selectivity between poly-Si and SiN, as well as between SiN and Si channel. The high selectivity feature of wet etching ensures that negligible

damage is incurred in the channel. Figure 7.9(b) shows a cross-sectional transmission electron microscope (TEM) picture of the selective SiGe-epi layer on the source/drain region. It can be seen that the structure is essentially defect-free both inside the epi-layer and at the Si/SiGe interface. The quality of the epi layer is important for device performance.

Figure 7.10 depicts threshold voltage (V_{th}) roll-off characteristics for PMOS devices. Note that the high V_{th} is mainly due to the use of n^+-poly gate in our work. V_{th} could be reduced when p^+-poly or metal gate is adopted. In our future work metal gate and high-*k* gate dielectric will be investigated. The short-channel-effect is ascribed to the thick gate oxide. Actually we found that the gate oxide thickness is about 6 nm from the TEM picture (not shown), which is much thicker than we expect. The reason is not known at this stage, and is probably due to some remaining sacrificial oxide that was not fully cleared and left after the removing step. Reducing gate oxide thickness is expected to improve the control over the short-channel effect.

Typical subthreshold and output characteristics of PMOS devices are shown in Figs. 7.11(a) & (b), respectively. The off-state leakage current of the device is presumably related to non-optimized raised source/drain structure and implantation conditions. Though the device fabrication and structure have not been optimized yet, the initial device performance is promising and demonstrates the potential of the proposed approach. In this work, for simplicity, n^+ poly-Si gate and conventional gate dielectric were used. However, it is without doubt that the proposed "gate-last" scheme could be applied for the integration of high-*k* gate dielectric and metal gate.

7.4 Summary

SB SOI-PMOSFET formed by Pt salicide and impurity segregation has been demonstrated. Because of the tri-gate nature in the new structure, the overall performance is much improved over the conventional SB device. By optimizing the SB height through impurity segregation, excellent device performance with low leakage current is achieved without resorting to FID structure. The driving current of the new SB device with impurity segregation is five times larger than that of the SB device with FID. Since the impurity segregation technique is also applicable to arsenic as well as phosphorous dopants, high performance SB CMOS can be realized. Schottky junction with impurity segregation thus appears to be a promising technique for future nano-scale MOSFETs.

We have also proposed and successfully demonstrated a new CMP-free process for fabricating UTB SOI PMOS transistors with SiGe raised source/drain and replacement gate. Satisfactory device characteristics have been achieved. With its inherent "gate-last" feature, the new scheme lends itself handily to high-*k* gate dielectric and metal electrode. By further optimization of the process conditions, the new scheme could be a useful approach for nano-scale CMOS manufacturing.

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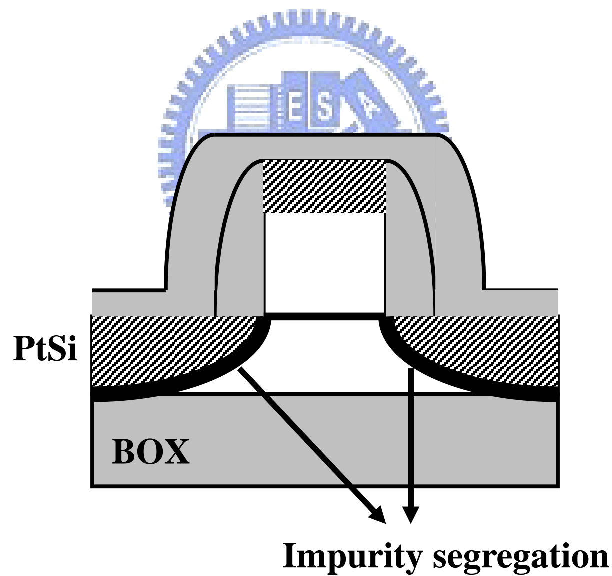
- **Thinning SIMOX SOI wafer to 50 nm by oxidation.**
- **Patterning and etching the Si fin to 60 nm, and growing sacrificial oxide.**
- **Growing and patterning 2.5 nm oxynitride gate dielectric/150 nm poly-gate.**
- **Forming 20 nm LPTEOS spacer.**
- **Implanting BF_2 and RTA-annealing at 850˚C, 20s.**
- **Depositing 50 nm Pt, forming PtSi by 450˚C anneal, and removing unreacted Pt.**
- **Forming passivation oxide, contact holes, and metal pads.**

(a)



(b)

Fig. 7.1 (a) The key process flow of the new SB MOSFET. (b) The cross-sectional view of the new SB SOI PMOSFET with PtSi source/drain. Dopants are segregated at the PtSi/Si interface.

- **Starting with P-type (100) SIMOX SOI.**
- **Depositing SiN (10nm)/poly (80nm)/SiN (10nm)/TEOS (50nm).**
- **Patterning the dummy gate and RIE-etching top TEOS and SiN.**
- **Removing PR, and etching poly with TEOS as hard-mask.**
- **Oxidizing poly sidewall (to grow 10nm oxide).**
- **Etching bottom-SiN, and growing SiGe by selective epitaxy.**
- **Removing TEOS, and oxidizing SiGe surface (to grow 30nm oxide).**
- **Implanting source/drain with BF_2 of 5×15 cm^{-2} at 30 keV.**
- **Removing SiN and poly, and growing 6nm sacrificial oxide.**
- **Removing sacrificial oxide, and depositing 2.5nm oxide/150nm poly gate.**
- **Patterning and RIE-etching the gate.**
- **Depositing passivation layer, and etching contact holes.**
- **Depositing and patterning metal layer.**

Fig. 7.2 Key process flow for the new process of fabricating ultra-thin-body SOI device with raised source/drain.

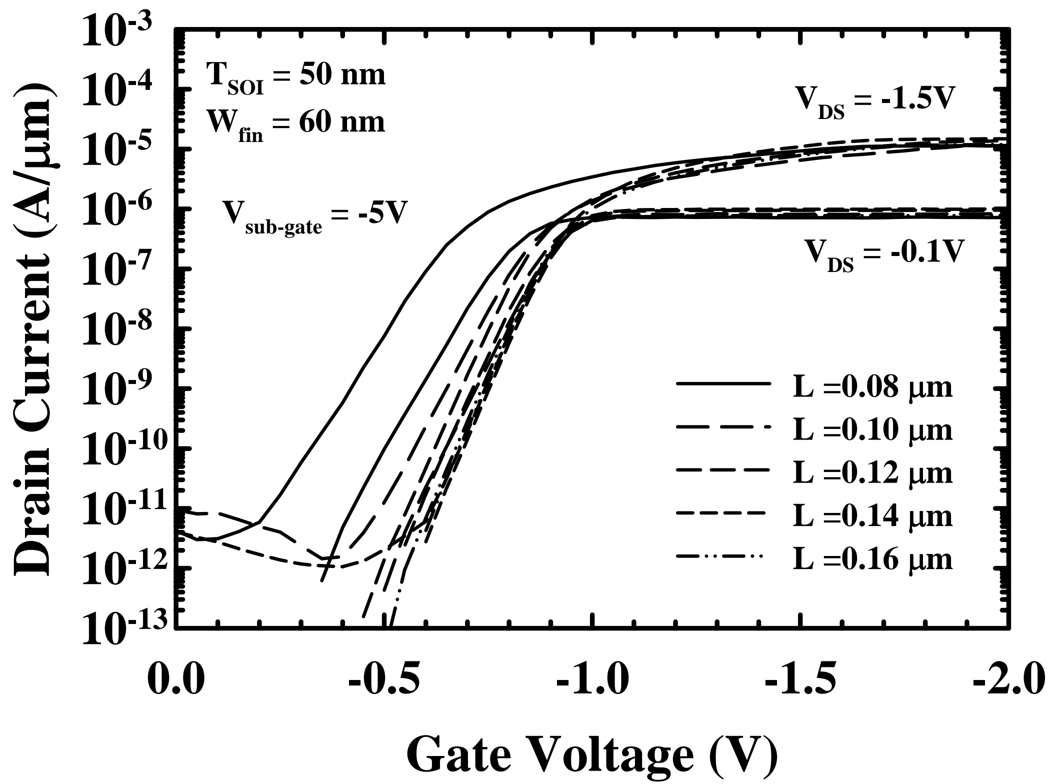


Fig. 7.3 The subthreshold characteristics of schottky barrier (SB) FinFET at a fixed fin width.

Table 7-I Drain-induced-barrier-lowing (DIBL) of SB FinFETs

FW (μm) / L (μm)	0.06	0.08	0.10	0.12	0.14	0.16	0.18	0.20
0.08	112.5							
0.10	44.6	185.3	180.9	472.3				
0.12	21.7	47.2	102.3	149.6	283.3	166.6	281.9	264.6
0.14	9.1	23.6	52.2	76.6	122.3	105.8	141.2	199.5
0.16	6.7	19.2	30.4	44.7	56.5	88.1	87.1	101.4

* Unit in mV/V.

* FW and L are fin width and channel length, respectively.

1896

Table 7-II Subthreshold swing (SS) of SB FinFETs

FW (μm) / L (μm)	0.06	0.08	0.10	0.12	0.14	0.16	0.18	0.20
0.08	75.3							
0.10	66.8	90.4	93.4	94.6				
0.12	63.0	67.1	80.7	77.2	95.6	93.9	104.2	106.5
0.14	61.4	66.3	70.9	73.4	79.3	76.8	85.1	92.1
0.16	61.5	62.0	65.0	69.0	73.9	77.7	76.3	81.7

* Unit in mV/dec.

* FW and L are fin width and channel length, respectively.

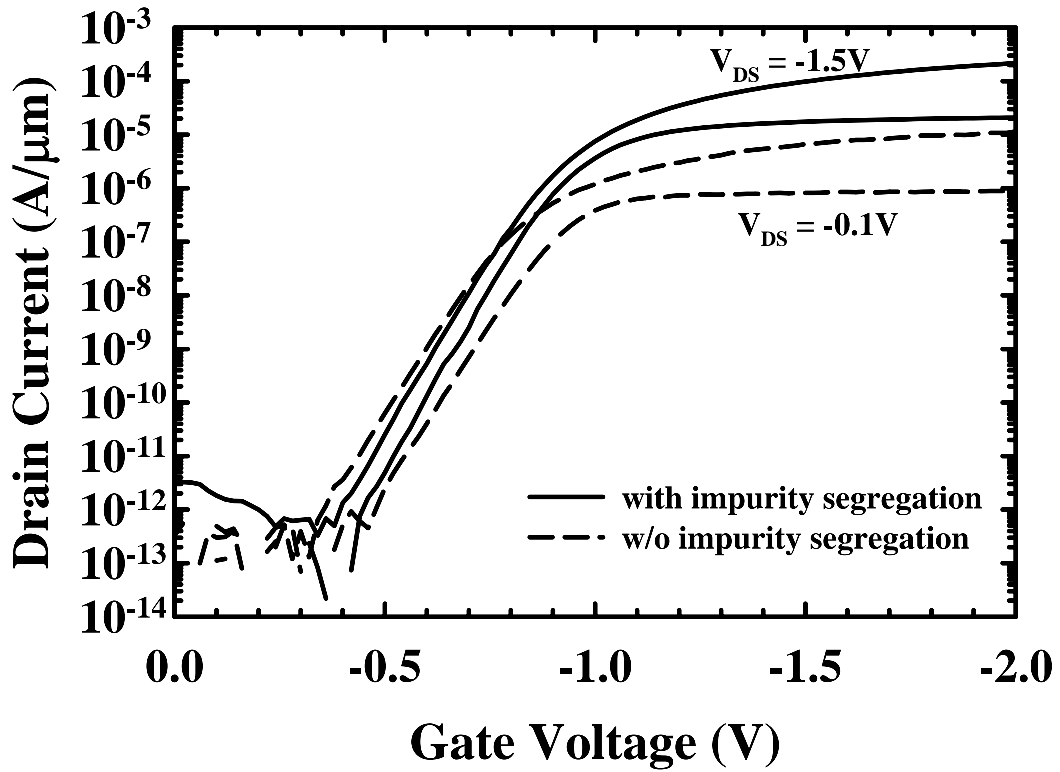


Fig. 7.4 Subthreshold characteristics of SB device with FID and the new SB device with impurity segregation. SB device with impurity segregation is superior to SB device with FID.

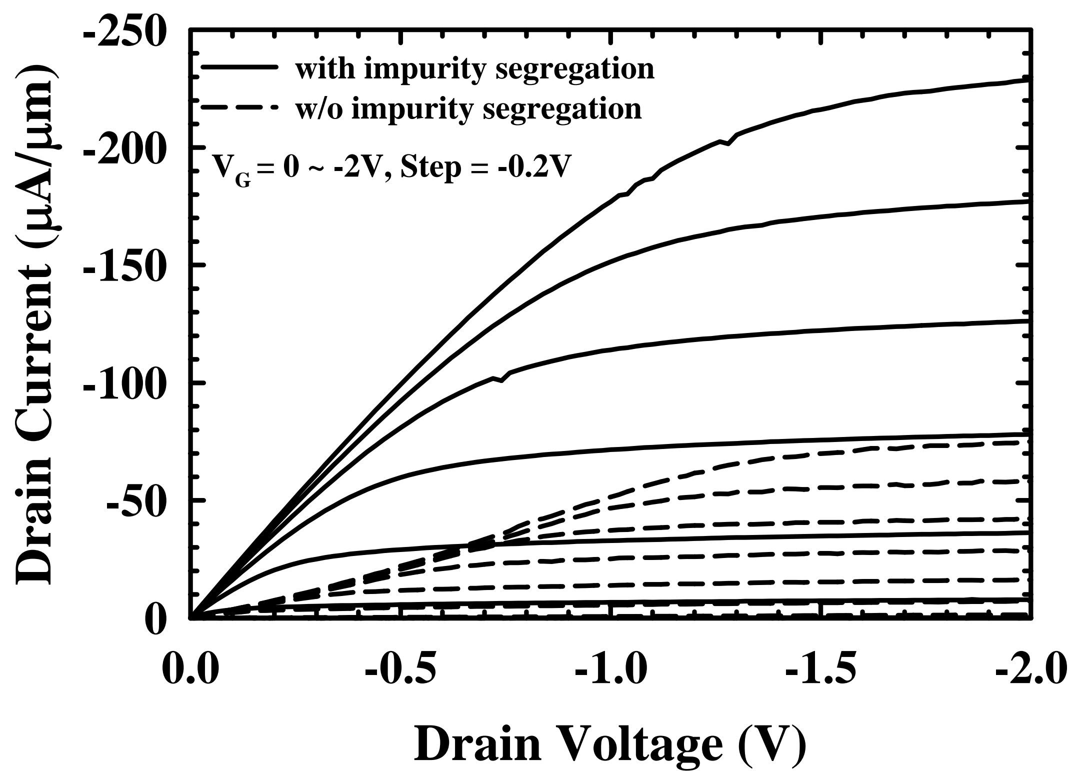


Fig. 7.5 Output characteristics of SB device with FID and the new SB device with impurity segregation. SB device with impurity segregation is superior to SB device with FID.

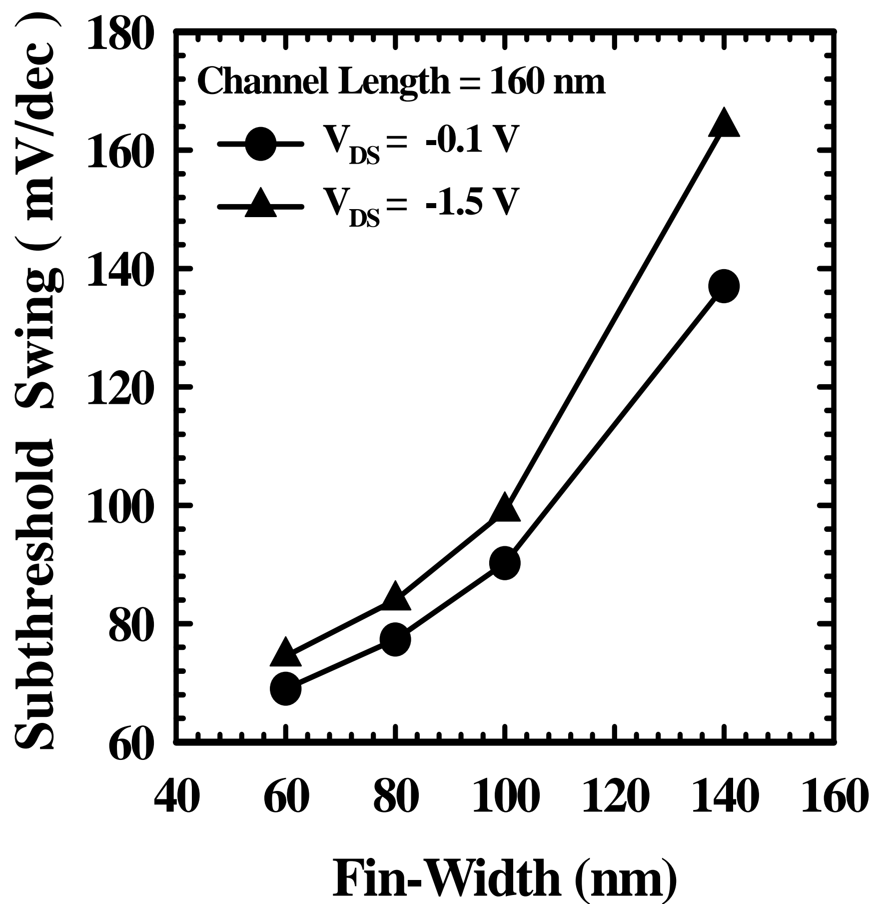


Fig. 7.6 Subthreshold swing of the new SB MOSFET with different fin widths. The subthreshold swing decreases with the smaller fin-width. This confirms that FinFET structure is indeed effective in suppressing short channel effects when fin width is smaller or equal to 0.7 times channel length.

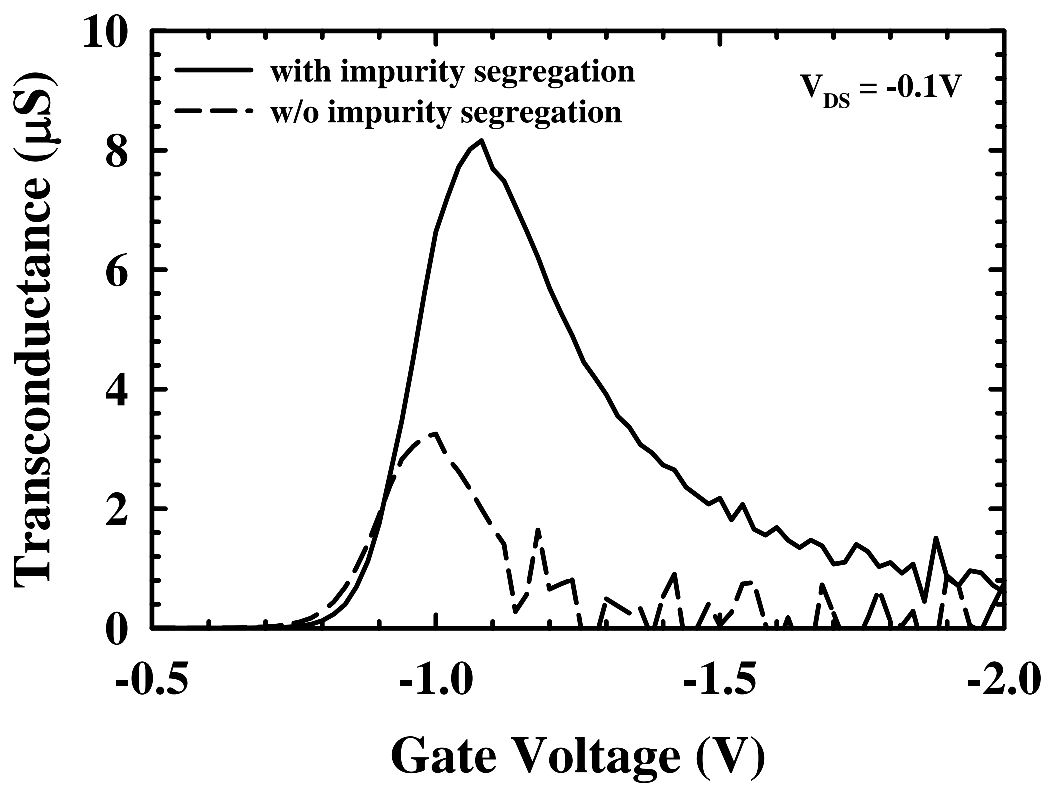
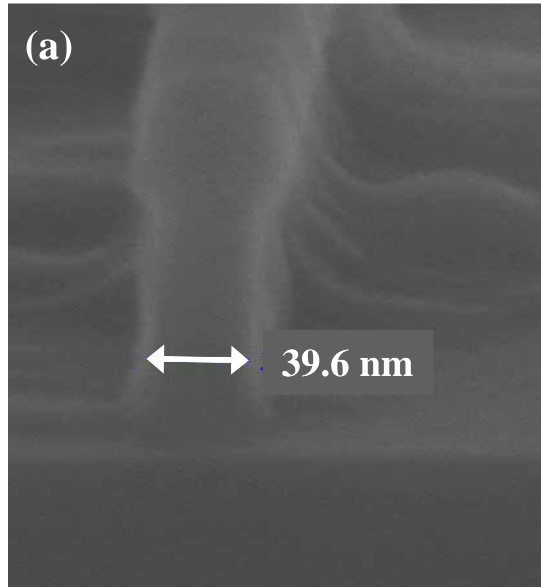


Fig. 7.7 The transconductance curves of the conventional SB PMOSFET and SB with impurity segregation.



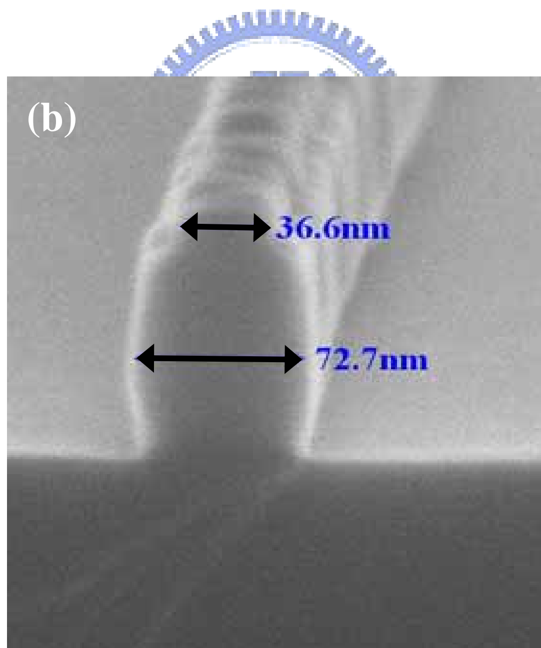


Fig. 7.8 (a) SEM picture of a TEOS/SiN/poly-Si/SiN stacked dummy gate. (b) SEM picture of a dummy gate after poly-Si sidewall oxidaion. The sidewall becomes expanded due to the formation of thermal oxide.

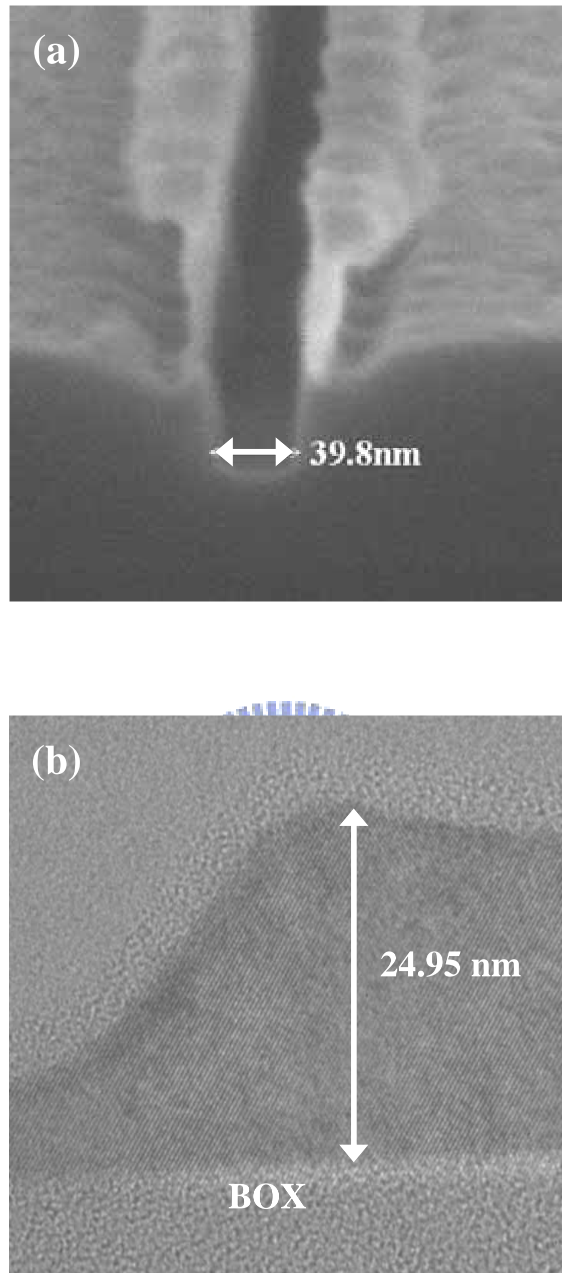


Fig. 7.9 (a) SEM picture after removing dummy gate. The bottom of the dummy gate is very flat and suitable for device fabrication. (b) TEM picture of selective SiGe-epi grown on source/drain region.

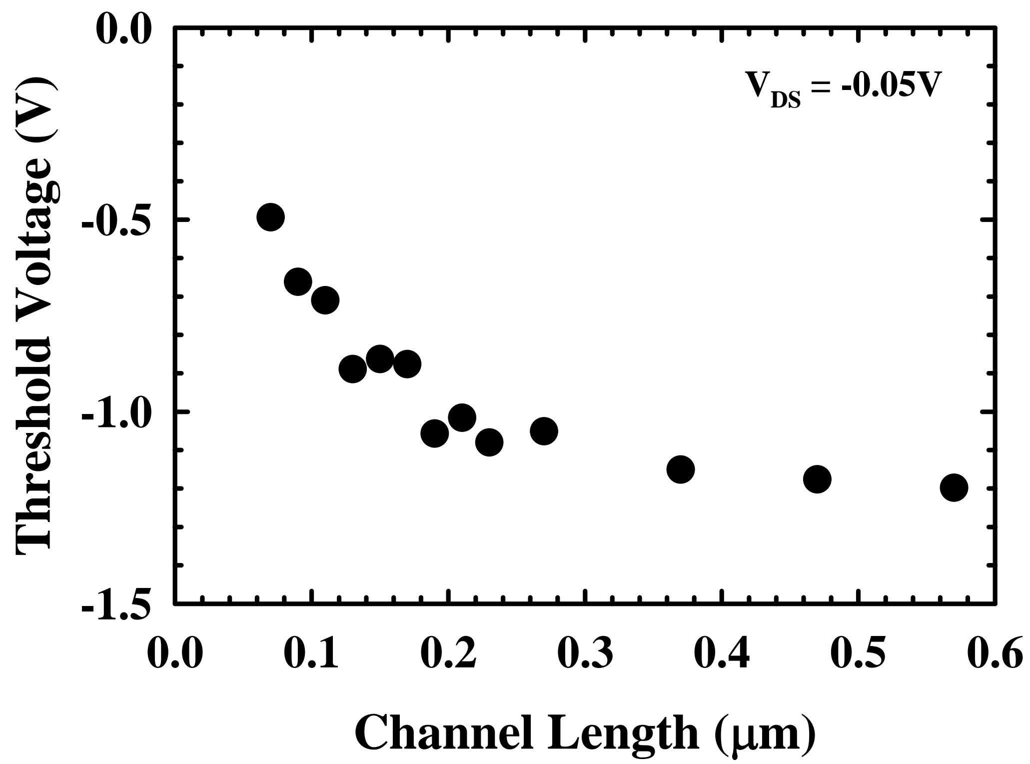
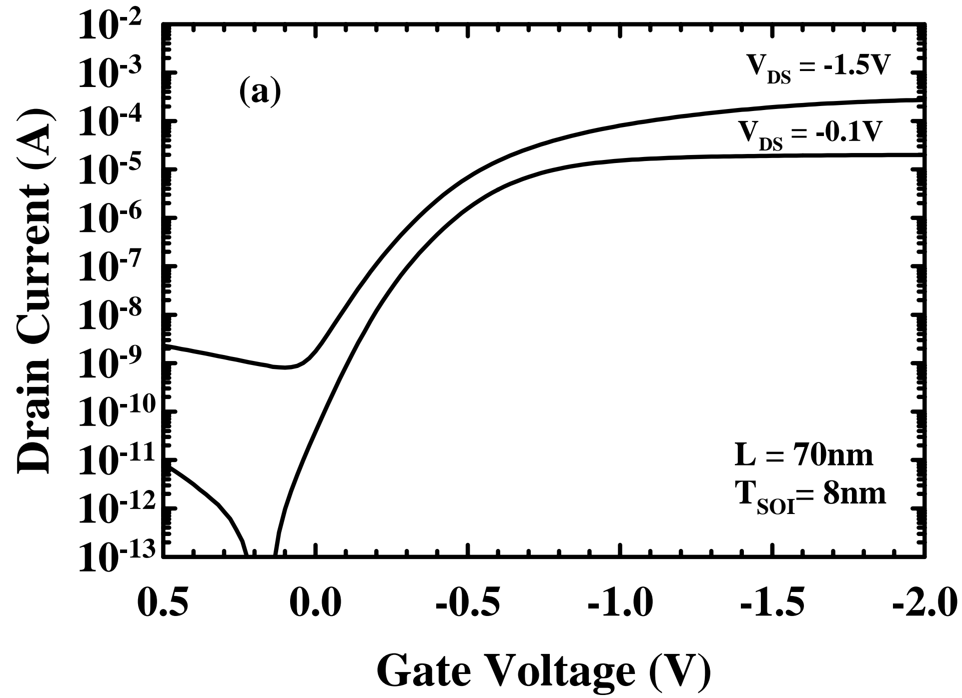


Fig. 7.10 The threshold voltage roll-off of the UTB SOI PMOSFETs.



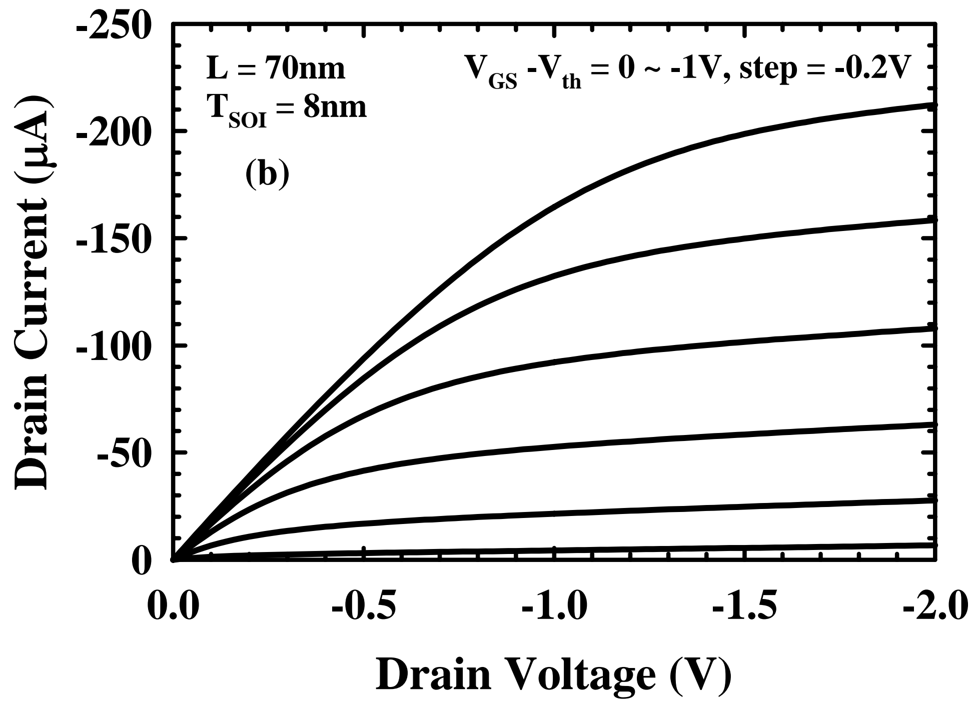


Fig. 7.11 (a) Subthreshold chararcteristics and (b) output chararcteristics of an UTB SOI PMOSFET.

Chapter 8

Conclusions and Suggested Future Works

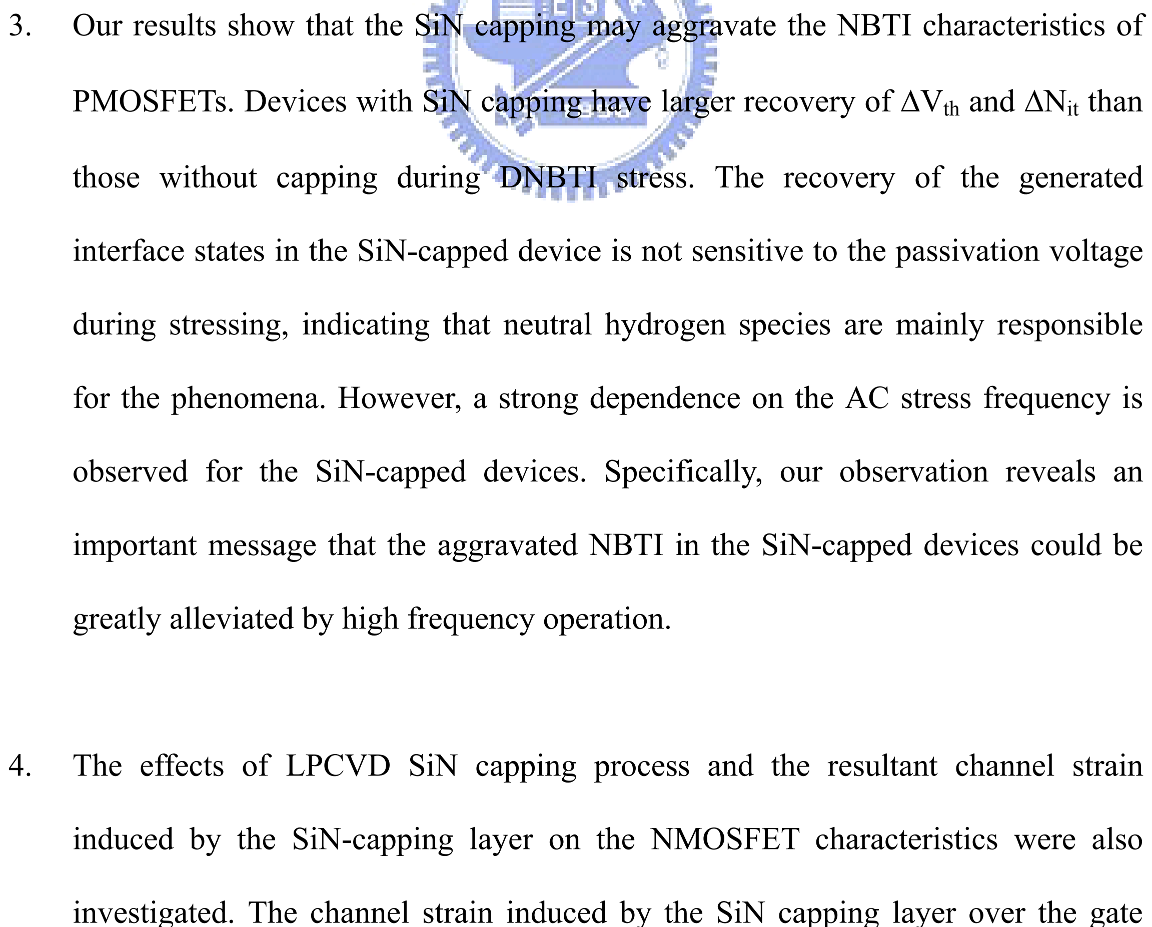
8.1 Conclusions

In this dissertation, we have fabricated and systematically studied devices with SiN capping layer, including investigating the difference and reliability characteristics between devices with poly-Si and –SiGe gates, the current enhancement with SiN capping, the impact of SiN capping on reliability characteristics, and extensive study on AC stress for SiN-capped devices. Finally, we have also employed impurity segregation technique to improve drive current of SB FinFET and proposed a new CMP-free process for fabricating UTB SOI PMOS transistors with SiGe raised source/drain and replacement gate. Several important results were obtained and summarized as follows:

1. Devices with poly-SiGe gate electrodes can help alleviate poly-depletion and boron penetration problem because of higher dopant activation in p-type semiconductor under the same implantation and annealing conditions. Hence, drive current would be greatly enhanced by using poly-SiGe gate electrode. Although the neutral and molecular hydrogen species are major diffusion species in both poly-SiGe and -Si gated devices during NBTI stress, the poly-SiGe gated devices show slightly longer lifetime under NBTI stress over poly-Si gated devices because of less boron penetration. Therefore, PMOSFETs using poly-SiGe gate electrode can be beneficial for device performance without degrading reliability.

2. Poly-SiGe-gated PMOSFETs with local compressive strain in the channel induced by a compressive SiN-capping layer were fabricated. The incorporation of the

compressive SiN-capping layer is found to significantly enhance the drive current of PMOSFETs. Despite this much-coveted merit, our results also show that the SiN capping may aggravate the NBTI characteristics. The voluminous hydrogen species contained in the PE-SiN layer as well as the strain energy stored in the channel may be the culprits for the worsened reliability. Even for the devices with SiN-capping, the saturation phenomena in ΔV_{th} and ΔN_{it} are observed. This is because nearly all the interfacial Si-H bonds have been broken. Hydrogen species is believed to play a major role during NBTI stress. Care should therefore be exercised to optimize the amount of hydrogen species to ensure that the NBTI effect is kept at bay, while simultaneously maintaining the performance enhancement characteristic of the compressive strain channel.



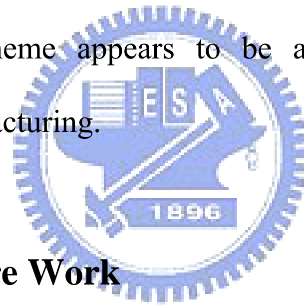
3. Our results show that the SiN capping may aggravate the NBTI characteristics of PMOSFETs. Devices with SiN capping have larger recovery of ΔV_{th} and ΔN_{it} than those without capping during DNBTI stress. The recovery of the generated interface states in the SiN-capped device is not sensitive to the passivation voltage during stressing, indicating that neutral hydrogen species are mainly responsible for the phenomena. However, a strong dependence on the AC stress frequency is observed for the SiN-capped devices. Specifically, our observation reveals an important message that the aggravated NBTI in the SiN-capped devices could be greatly alleviated by high frequency operation.

4. The effects of LPCVD SiN capping process and the resultant channel strain induced by the SiN-capping layer on the NMOSFET characteristics were also investigated. The channel strain induced by the SiN capping layer over the gate

greatly boosts the drive current of short-channel devices. In addition, our results indicate that the thermal budget associated with the deposition of the SiN capping layer could alleviate the reverse short-channel effect (RSCE) encountered in the uncapped devices. The extra thermal budget of SiN capping is beneficial for easing the RSCE, albeit it is also the main culprit for the less solid solubility of gate dopants and gate oxide thickness variation. The bandgap narrowing effect due to the channel strain may result in further lowering in V_{th} as the channel length is shortened. Furthermore, interface state density is also affected by SiN capping process. More hydrogen species are expected to participate in interface state passivation as the time of the SiN deposition increases.

5. Both the deposited SiN layer and the deposition process itself have significant impacts on the device operation and the associated reliability characteristics. This work shows that hot-electron degradation is adversely affected when the SiN is deposited over the gate, even if the SiN is removed later and the channel strain is relieved. Nevertheless, the accompanying bandgap narrowing and the increased carrier mobility tend to worsen the hot-electron reliability. In this aspect, attentions should also be paid to the SiN deposition itself. Owing to the use of hydrogen-containing precursors, abundant hydrogen species are incorporated in the oxide that may also contribute to the hot-electron degradation. The edge effect of hot carrier stress is also a plausible factor that causes degrade reliability in the SiN-removal devices. Optimization of both SiN deposition process and the film properties are thus essential for implementation of the uniaxial strain in NMOS devices.

6. SB FinFET formed by Pt salicide and impurity segregation has been demonstrated in this study. Because of the tri-gate nature inherent in our device structure, the overall performance is much improved over the conventional SB device. By adjusting SB height through impurity segregation, excellent device performance is achieved without resorting to FID approach. Specifically, the drive current of the new SB device is five times larger than that of the conventional SB device with FID. Moreover, we have also proposed and successfully demonstrated a new CMP-free process for fabricating UTB SOI PMOS transistors with SiGe raised source/drain and replacement gate. Satisfactory device characteristics have been achieved. With its inherent "gate-last" feature, the new scheme lends itself handily to high-*k* gate dielectric and metal electrode. By further optimization of the process conditions, the new scheme appears to be a very promising approach for nano-scale CMOS manufacturing.



8.2 Suggestions for Future Work

There are some interesting and important topics that are valuable for the future research regarding devices with SiN capping and SOI devices:

1. In Chapter 2, future work can concentrate on dynamic NBTI and AC stress of poly-SiGe gated devices.

2. In Chapter 3, hydrogen species are believed to be the main passivating species for Si dangling bonds and play a major role during NBTI stress. Therefore, it is important to optimize the amount of hydrogen species while retaining its compressive stress during the deposition of SiN layer. This could be accomplished

by carefully adjusting the process conditions in PECVD systems, or resorting to high-density plasma CVD (HDPCVD). In addition, depositing a thin buffer layer before SiN capping layer to trap hydrogen species can effectively suppress hydrogen into the Si/SiO_2 interface during SiN layer deposition, although the buffer layer must be sufficiently thin so that it will not compromise the beneficial effect of channel strain.

3. In Chapter 4, higher SiN strain energy stored in the channel may also play a role in the aggravated degradation process, which may weaken Si-N, Si-O, and Si-Si bonds near the SiO_2/Si interface. However, more efforts are required to fully understand details about this mechanism. Future research is suggested to simulate the strain effect on bonding destruction and NBTI degradation, and building a current transport model of PMOSFETs with SiN capping.

4. In Chapter 5, the extra thermal budget of SiN capping is the main killer in gate dopant out-diffusion and gate oxide variation. It is suggested to develop a low thermal-budget process for depositing the tensile SiN layer. Moreover, the devices with the thicker gate oxide (i.e., 4 nm) are more suitable for extracting bandgap narrowing by F-N current fitting. Further, simulating the strain effect of drive current and building a current transport model are also suggestions for future work.

5. In Chapter 6, hydrogen species are also a major culprit for the hot-carrier degradation. Optimization of both SiN deposition process and the film properties are thus essential for implementation of the uniaxial strain in MOSFETs. It is also suggested to deposit the SiN layer at low temperature, and/or add a thinner buffer

layer before SiN capping.

6. In Chapter 7, future research is suggested to study other dopants and metal silicide materials in order to improve impurity segregation. Moreover, optimized raised source/drain structure and dopant implant conditions for UTB SOI devices are beneficial to improve device performance.