Chapter 6
Conclusions

6.1 Conclusions

Content-addressable memory (CAM) has a single clock cycle throughput making them faster than other hardware- and software-based search systems. However, the speed of a CAM comes at the cost of increased silicon area and power consumption. As CAM applications grow, the larger CAM size demanding, the further exacerbated power problem. Reducing power consumption, without sacrificing speed or area, is the main thread of recent research topic in large-capacity CAMs. The conventional CAM architecture and applications of CAM were described in Chapter 2 in detail. Besides, several low-power and high-speed CAM design techniques were also introduced in this chapter.

Leakage current is a critical issue in the future, especially in memory applications like DRAM and SRAM due to the fact that the stability of the storage values could be deteriorate by leakage. Due to the thinner oxide in the nano-era, the leakage increased further with the technology advances. However, previous researches only work on search power reduction. Although significant improvement has been made, this also narrows the difference between active power and leakage power, which cause the leakage power being negligible. In view of this, we proposed two novel techniques to reduce the leakage current. The multi-mode data retention power gating technique is introduced in Chapter 3. It has three operation mode to preserve data when needed and reduce the leakage significantly when the data is not needed. In Chapter 5, the super cut-off power gating TCAM cell is proposed. The super cut-off technique is don’t care independent and will not affect the cell stability. In 65nm CMOS technology, it achieves significant leakage saving thus the power overhead incurred by voltage generators and control circuit is negligible.

For IP addressing lookup application, a 256-word x 144-bit energy-efficient ternary CAM array was implemented in Chapter 5. The proposed TCAM scheme is composed of super cut-off power gating technique and multi-mode data retention power gating technique. The simulation results show that the search time of proposed TCAM scheme is 0.23ns and the energy metric is 0.047 fJ/bit/search. The TCAM is operates under 500Mhz at 1.0V supply voltage. The standby power reduction can achieve 70% when 50% don't care is considered. All simulations are based on 65nm Berkeley Predictive Technology Model (BPTM).