Bibliography

[1] M. Meribout, T. Ogura, and M. Nakanishi, "On using the CAM concept for parametric curve extraction," *IEEE Trans Image Process.*, vol. 9, no.12, pp. 2126–2130, Dec. 2000.

[2] M. Nakanishi and T. Ogura, "Real-time CAM-based Hough transform and its performance evaluation," *Machine Vision Appl.*, vol. 12, no. 2, pp. 59–68, Aug. 2000.

[3] E. Komoto, T. Homma, and T. Nakamura, "A high-speed and compactsize JPEG Huffman decoder using CAM," in Symp. *VLSI Circuits Dig. Tech. Papers*, 1993, pp. 37–38.

[4] L.-Y. Liu, J.-F.Wang, R.-J.Wang, and J.-Y. Lee, "CAM-based VLSI architectures for dynamic Huffman coding," *IEEE Trans. Consumer Electron.*, vol. 40, no. 3, pp. 282–289, Aug. 1994.

[5] B. W. Wei, R. Tarver, J.-S. Kim, and K. Ng, "A single chip Lempel-Ziv data compressor," in Proc. *IEEE Int. Symp. Circuits Syst. (ISCAS),* vol. 3, 1993, pp. 1953–1955.

[6] R.-Y. Yang and C.-Y. Lee, "High-throughput data compressor designs using content addressable memory," in Proc. *IEEE Int. Symp. Circuits Syst. (ISCAS),* vol. 4, 1994, pp. 147–150.

[7] C.-Y. Lee and R.-Y. Yang, "High-throughput data compressor designs using content addressable memory," *IEE Proc.—Circuits, Devices and Syst.*, vol. 142, no. 1, pp. 69–73, Feb. 1995.

[8] D. J. Craft, "A fast hardware data compression algorithm and some algorithmic extansions," *IBM J. Res. Devel.*, vol. 42, no. 6, pp. 733–745, Nov. 1998.

[9] S. Panchanathan and M. Goldberg, "A content-addressable memory architecture for image coding using vector quantization," *IEEE Trans. Signal Process.*, vol. 39, no. 9, pp. 2066–2078, Sep. 1991.

[10] T. Kohonen, Content-Addressable Memories, 2nd ed. New York:

Springer-Verlag, 1987.

[11] L. Chisvin and R. J. Duckworth, "Content-addressable and associative memory: alternatives to the ubiquitous RAM," *IEEE Computer*, vol. 22, no. 7, pp. 51–64, Jul. 1989.

[12] K. E. Grosspietsch, "Associative processors and memories: a survey," *IEEE Micro*, vol. 12, no. 3, pp. 12–19, Jun. 1992.

[13] I. N. Robinson, "Pattern-addressable memory," *IEEE Micro*, vol. 12, no. 3, pp. 20–30, Jun. 1992.

[14] S. Stas, "Associative processing with CAMs," *Northcon/93 Conf. Record*, 1993, pp. 161–167.

[15] S. Deering, and R. Hinden, "RFC: 1883 Internet Protocol Version 6 (IPv6) Specification," *Internet Engineering Task Force. (IETF)*, December 1995.

[16] R. Hinden, and S. Deering, "RFC: 3513 Internet Protocol Version 6 (IPv6) Addressing Architecture," *Internet Engineering Task Force. (IETF)*, April 2003.

[17] C.H. Hua, Wei Hwang, and C.K. Chen, "Noise-Tolerant XOR-Based Conditional Keeper for High Fan-in Dynamic Circuits," *IEEE International Symposium on Circuits and Systems*, Kobe, Japan, 2005.

[18] J.R. Yuan, C. Svensson, and P. Larsson, "New Domino Logic Precharged by Clock and Data," *Electronics Letters*, Vol. 29, No. 25, pp. 2188-2189, Dec. 1993.

[19] F. Shafai, K.J. Schultz, G.F.R. Gibson, A.G. Bluschke, D.E. Somppi, "Fully Parallel 30-MHz, 2.5-Mb CAM," *IEEE Journal of Solid-State Circuits*, Vol. 33, No. 11, pp. 1690-1696, Nov. 1998.

[20] P.F. Lin and J.B. Kuo, **"**1-V 128-kb Four-Way Set-Associative CMOS Cache Memory Using Wordline-Oriented Tag-Compare (WLOTC) Structure with the Content Addressable-Memory (CAM) 10-transistor Tag Cell,**"** *IEEE Journal of Solid-State Circuits*, Vol. 36, No. 4, pp.666-675, April 2001.

[21] H. Miyatake and M. Tanaka and Y. Mori, **"**A Design for High-Speed Low-Power CMOS Fully Parallel Content-Addressable Memory Macros**,"** *IEEE Journal of Solid-State Circuits*, Vol. 36, No. 6, pp.956-968, June 2001.

[22] I. Arsovski and A. Sheikholeslami, "A Mismatch-Dependent Power Allocation Technique for Match-Line Sensing in Content-Addressable Memories," *IEEE Journal of Solid-State Circuits*, Vol. 38, No. 11, Nov. 2003.

[23] I. Arsovski, T. Chandler and A. Sheikholeslami, **"**A Ternary Content-Addressable Memory (TCAM) Based on 4T Static Storage and Including a Current-Race Sensing Scheme**,"** *IEEE Journal of Solid-State Circuits,* Vol. 38, No. 1, pp.155-158, Jan. 2003.

[24] A. Roth, D. Foss, R. McKenzie and D. Perry, **"**Advanced Ternary CAM Circuits on 0.13 μm Logic Process Technology**,"** *Proceedings of the IEEE 2004 Custom Integrated Circuits Conference*, pp. 465-468, Oct. 2004.

[25] G. Kasai, Y. Takarabe, K. Furumi and M. Yoneda, **"**200MHz/200MSPS 3.2W at 1.5V Vdd, 9.4Mbits ternary CAM with New Charge Injection Match Detect Circuits and Bank Selection Scheme**,"** *Proceedings of the IEEE 2003 Custom Integrated Circuits Conference*, pp. 387-390, Sept. 2003.

[26] H. Noda, K. Inoue, H.J. Mattausch, T. Koide, K. Arimoto, **"**A Cost-Efficient Dynamic Ternary CAM in 130 nm CMOS Technology with Planar Complementary Capacitors and TSR Architecture**,"** *Symposium on VLSI Circuits Digest of Technical Papers*. pp.83-84, June 2003.

[27] V. Lines, A. Ahmed, P. Ma, S. Ma, R. McKenzie, H.S. Kim and C. Mar, **"**66 MHz 2.3 M Ternary Dynamic Content Addressable Memory**,"** Records of the 2000 *IEEE International Workshop on Memory Technology Design and Testing*, pp.101-105, Aug. 2000.

[28] J.G. Delgado-Frias, A. Yu and J. Nyathi, **"**A Dynamic Content Addressable Memory Using a 4-transistor Cell**,"** *Third International Workshop on Design of Mixed-Mode Integrated Circuits and Applications*, pp.110-113, July 1999.

[29] H. Noda, K. Inoue, M. Kuroiwa, F. Igaue, K. Yamamoto, H.J. Mattausch, T.

Koide, A. Amo, A. Hachisuka, S. Soeda, I. Hayashi, F. Morishita, K. Dosaka, K. Arimoto, K. Fujishima, K. Anami, T. Yoshihara, **"**A Cost-Efficient High-Performance Dynamic TCAM with Pipelined Hierarchical Searching and Shift Redundancy Architecture**,"** *IEEE Journal of Solid-State Circuits*, Vol. 40, No. 1, pp. 245-253, Jan. 2005.

[30] H. Miyatake and M. Tanaka and Y. Mori, **"**A Design for High-Speed Low-Power CMOS Fully Parallel Content-Addressable Memory Macros**,"** IEEE Journal of Solid-State Circuits, Vol. 36, No. 6, pp.956-968, June 2001.

[31] T.-B. Pei and C. Zukowski, "VLSI implementation of routing tables: tries and CAMs," *Proc. IEEE INFOCOM*, vol. 2, 1991, pp. 515–524.

[32] , "Putting routing tables in silicon," *IEEE Network Mag.*, vol. 6, no. 1, pp. 42–50, Jan. 1992.

[33] A. J. McAuley and P. Francis, "Fast routing table lookup using CAMs," *Proc. IEEE INFOCOM,* vol. 3, 1993, pp. 1282–1391.

[34] N.-F. Huang, W.-E. Chen, J.-Y. Luo, and J.-M. Chen, "Design of multi-field IPv6 packet classifiers using ternary CAMs," *Proc. IEEE GLOBECOM*, vol. 3, 2001, pp. 1877–1881.

[35] G. Qin, S. Ata, I. Oka, and C. Fujiwara, "Effective bit selection methods for improving performance of packet classifications on IP routers," *Proc. IEEE GLOBECOM*, vol. 2, 2002, pp. 2350–2354.

[36] H. J. Chao, "Next generation routers," *Proc. IEEE,* vol. 90, no. 9, pp. 1518–1558, Sep. 2002.

[37] D. A. Patterson and J. L. Hennessy, **"**Computer Organization and Design**,"** *Morgan Kaufmann*, 2nd edition.

[38] J. L. Hennessy and D. A. Patterson, **"**Computer Architecture**,"** *Morgan Kaufmann*, 3rd edition.

[39] R. Panigrahy and S. Sharma, "Sorting and searching using ternary CAMs," in *Proc. Symp. High Performance Interconnects*, 2002, pp. 101–106.

[40] , "Sorting and searching using ternary CAMs," *IEEE Micro*, vol. 23, no. 1, pp. 44–53, Jan.–Feb. 2003.

[41] Http://www.commsdesign.com/main/1999/11/9911feat3.htm:Using Content Addressable Memory for Networking Applications

[42] Http://www.eecg.toronto.edu/~pagiamt/: Content-Addressable Memory (CAM) Primer.

[43] N. Mohan and M. Sachdev, **"**Low Power Dual Matchline Ternary Content Addressable Memory**,"** *Proceedings of the 2004 International Symposium on Circuits and Systems (ISCAS '04)*, Vol. 2, pp.633-636, May 2004.

[44] C.A. Zukowski and S.Y. Wang, **"**Use of Selective Precharge for Low-Power on the Match Lines of Content-Addressable Memories**,"** *Proceedings of 1997 International Workshop on Memory Technology, Design and Testing*, pp. 64-68, Aug. 1997.

[45] K. Pagiamtzis and A. Sheikholeslami, **"**Pipelined Match-lines and Hierarchical Search-Lines for Low-Power Content-Addressable Memories**,"** Proceedings of the IEEE 2003 Custom Integrated Circuits Conference, pp. 383-386, Sept. 2003.

[46] N. Mohan and M. Sachdev, **"**A Static Power Reduction Technique for Ternary Content Addressable Memories**,"** *Canadian Conference on Electrical and Computer Engineering*, Vol.2, pp.711-714, May 2004.

[47] M. M. Khellah and M. Elmasry, "Use of charge sharing to reduce energy consumption in wide fan-in gates," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, vol. 2, 1998, pp. 9–12.

[48] I. Arsovski, T. Chandler, and A. Sheikholeslami, "A ternary contentaddressable memory (TCAM) based on 4T static storage and including a current-race sensing scheme," *IEEE J. Solid-State Circuits*, vol. 38, no. 1, pp. 155–158, Jan. 2003.

[49] C. A. Zukowski and S.-Y. Wang, "Use of selective precharge for lowpower content-addressable memories," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, vol. 3, 1997, pp. 1788–1791.

[50] I. Y.-L. Hsiao, D.-H. Wang, and C.-W. Jen, "Power modeling and low-power

design of content addressable memories," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, vol. 4, 2001, pp. 926–929.

[51] A. Efthymiou and J. D. Garside, "An adaptive serial-parallel CAM architecture for low-power cache blocks," in *Proc. IEEE Int. Symp. Low Power Electronics and Design (ISLPED)*, 2002, pp. 136–141.

[52] , "A CAM with mixed serial-parallel comparison for use in low energy caches," *IEEE Trans. VLSI Syst.*, vol. 12, no. 3, pp. 325–329, Mar. 2004.

[53] N. Mohan and M. Sachdev, "Low power dual matchline content addressable memory," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, vol. 2, 2004, pp. 633–636.

[54] K.-H. Cheng, C.-H.Wei, and S.-Y. Jiang, "Static divided word matchline line for low-power content addressable memory design," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, vol. 2, 2004, pp. 629–632.

[55] K. Pagiamtzis and A. Sheikholeslami, "Pipelined match-lines and hierarchical search-lines for low-power content-addressable memories," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, 2003, pp. 383–386.

[56] , "A low-power content-addressable memory (CAM) using pipelined hierarchical search scheme," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1512–1519, Sep. 2004.

[57] J. M. Hyjazie and C. Wang, "An approach for improving the speed of content addressable memories," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, vol. 5, 2003, pp. 177–180.

[58] I. Arsovski and A. Sheikholeslami, "A current-saving match-line sensing scheme for content-addressable memories," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2003, pp. 304–305.

[59] I. Arsovski, A. Sheikholeslami, "A mismatch-dependent power allocation technique for matchline sensing in content-addressable memories," *IEEE J. Solid-State Circuits*, vol. 38, no. 11, pp. 1958–1966, Nov. 2003.

[60] H. Noda, K. Inoue, M.Kuroiwa, A. Amo, A. Hachisuka, H. J. Mattausch, T.

Koide, S. Soeda, K. Dosaka, and K. Arimoto, "A 143 MHz 1.1W4.5 Mb dynamic TCAM with hierarchical searching and shift redundancy architecture," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2004, pp. 208–209.

[61] B. Gamache, Z. Pfeffer, and S. P. Khatri, **"**A fast ternary CAM design for IP networking applications**,"** *Proceedings of The 12th International Conference on Computer Communications and Networks (ICCCN 2003)*, pp. 434-439, Oct. 2003.

[62] S. Choi, K. Sohn, and H.J. Yoo, **"**A 0.7-fJ/bit/search 2.2-ns Search Yime Hybrid-Type TCAM Architecture**,"** *IEEE Journal of Solid-State Circuits*, Vol. 40, No. 1, pp.254-260, Jan. 2005.

[63] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, **"**Leakage Current Mechanism and Leakage Reduction Technique in Deep-Submicrometer CMOS Circuits**,"** *Proceedings of the IEEE*, vol. 91, No. 2, pp. 305-327, Feb. 2003.

[64] Li Ding and P. Mazumder, **"**On Circuit Techniques to Improve Noise Immunity of CMOS Dynamic Logic**,"** *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 12, No. 9, pp. 910-925, Sept. 2004.

[65] Li Ding and P. Mazumder, **"**On Circuit Techniques to Improve Noise Immunity of CMOS Dynamic Logi**c,"** *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 12, No. 9, pp. 910-925, Sept. 2004.

[66] Wei Hwang, R.V. Joshi, and W.H. Henkels, "A 500-MHz, 32-Word x 64-Bit, Eight-Port Self-Resetting CMOS Register File," *IEEE Journal of Solid-State Circuits*, Vol. 34, No. 1, pp. 56-67, Jan. 1999.

[67] Wei Hwang, G.D. Gristede, Pia Sanda, S.Y. Wang, and D.F. Heidel, "Implementation of a Self-Resetting CMOS 64-Bit Parallel Adder with Enhanced Testability," *IEEE Journal of Solid-State Circuits*, Vol. 34, No. 8, pp. 1108-1117, Aug. 1999.

[68] M.H. Anis, M.W. Allam, and M.I. Elmasry, "Energy-Efficient Noise-Tolerant Dynamic Styles for Scaled-Down CMOS and MTCMOS Technologies," *IEEE*

Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 10, No. 2, pp. 71-78, Apr. 2002.

[69] M.W. Allam, M.H. Anis, and M.I. Elmasry, "High-Speed Dynamic Logic Styles for Scaled-Down CMOS and MTCMOS Technologies," *Proceedings of the 2000 International Symposium on Low Power Electronics and Design (ISLPED '00)*, pp. 155-160, 2000.

[70] S.O. Jung; S.M. Yoo; K.W. Kim, and S.M. Kang, **"**Skew-Tolerant High-Speed (STHS) Domino Logic**,"** *The 2001 IEEE International Symposium on Circuits and Systems (ISCAS 2001)*, Vol. 4, pp. 154-157, May 2001.

[71] A. Alvandpour, R. Krishnamurthy, K. Soumyanath, and S. Borkar, "A Conditional Keeper Technique for Sub-0.13um Wide Dynamic Gates," *2001 Symposium on VLSI Circuits Digest of Technical Papers*, pp. 29-30, 2001.

[72] A. Alvandpour, R.K. Krishnamurthy, K. Soumyanath, and S.Y. Borkar, **"**A Sub-130-nm Conditional Keeper Technique,**"** *IEEE Journal of Solid-State Circuits*, Vol. 37, No. 5, pp. 633-638, May 2002.

[73] A. Alvandpour, R. Krishnamurthy, K. Soumyanath, and S. Borkar, **"**A Low-Leakage Dynamic Multi-Ported Register File in 0.13μm CMOS**,"** *2001 International Symposium on Low Power Electronics and Design*, pp. 68-71, Aug. 2001.

[74] C.M. Lee and E.W. Szeto, **"**Zipper CMOS**,"** *IEEE Circuits Devices Magazine*, vol. 2, pp. 10-17, May 1986.

[75] J. Pretorius, A. Shubat, and C. Salama, **"**Charge Redistribution and Noise Margins in Domino CMOS Logic**,"** *IEEE Transactions on Circuits and Systems*, Vol. 33, No. 8, pp. 786-793, Aug 1986.

[76] G.P. D'Souza, "Dynamic Logic Circuit with Reduced Charge Leakage," U.S. Patent 5 483 181, Jan. 1996.

[77] E.B. Schorn, "NMOS Charge-Sharing Prevention Device for Dynamic Logic Circuits," U.S. Patent 5 838 169, Nov. 1998.

[78] Lei Wang and N. R. Shanbhag, **"**Noise-Tolerant Dynamic Circuit Design**,"**

Proceedings of the 1999 IEEE International Symposium on Circuits and Systems (ISCAS '99), Vol. 1, pp. 549-552, May-June 1999.

[79] G. Balamurugan and N.R. Shanbhag, **"**Energy-Efficient Dynamic Circuit Design in the Presence of Crosstalk Noise**,"** *Proceedings of 1999 International Symposium on Low Power Electronics and Design*, pp. 24-29, 1999.

[80] G. Balamurugan and N. R. Shanbhag, **"**A Noise-Tolerant Dynamic Circuit Design Technique**,"** *Proceedings of the IEEE 2000 Custom Integrated Circuits Conference (CICC)*, pp. 425-428, May 2000.

[81] F. Murabayashi, T. Yamauchi, H. Yamada, T. Nishiyama, K. Shimamura, S. Tanaka, T. Hotta, T. Shimizu, and H. Sawamoto, **"**2.5 V CMOS Circuit Techniques for a 200 MHz Superscalar RISC Processor**,"** IEEE Journal of Solid-State Circuits, Vol. 31, No. 7, pp. 972-980, July 1996.

[82] J.J. Covino, **"**Dynamic CMOS Circuits with Noise Immunity**,"** U.S. Patent 5 650 733, July 1997.

[83] D.A. Evans, **"**Noise-Tolerant Dynamic Circuits**,"** U.S. Patent 5 793 228, Aug. 1998.

[84] S. Bobba and I.N. Hajj, **"**Design of Dynamic Circuits with Enhanced Noise Tolerance**,"** *Proceedings of 20th Annual IEEE International ASIC/SOC Conference*, pp. 54-58, Sept. 1999.

[85] C.H. Hua, Wei Hwang, and C.K. Chen, **"**Noise-Tolerant XOR-Based Conditional Keeper for High Fan-in Dynamic Circuits**,"** *presented at IEEE International Symposium on Circuits and Systems*, Kobe, Japan, 2005.

[86] H. Mahmoodi-Meimand and K. Roy, "A leakage-Tolerant High Fan-In Dynamic Circuit Design Style," Proceedings of the 2003 IEEE International SOC Conference, pp. 117-120, Sept. 2003.

[87] A. Solomatnikov, D. Somasekhar, K. Roy, and C. K. Koh, **"**Skewed CMOS: Noise-Immune High-Performance Low-Power Static Circuit Family**,"** Proceedings of 2000 International Conference on Computer Design, pp.

241-246, Sept. 2000.

[88] H. Mahmoodi-Meimand and K. Roy, **"**Diode-Footed Domino: a Leakage-Tolerant High Fan-In Dynamic Circuit Design Style**,"** IEEE Transactions on Circuits and Systems I: Regular Papers, Vol. 51, No. 3, pp. 495-503, March 2004.

[89] J.S. Wang, H.Yu Li, C.C. Chen, and C.W. Yeh, **"**An AND-type Match-line Scheme for Energy-Efficient Content Addressable Memories**,"** *presented at IEEE International Solid-State Circuits Conference*, San Francisco, CA, 2005.

[90] Jinn-Shyan Wang, Chao-Ching Wang, and Chingwei Yeh, "TCAM for IP-Address Lookup Using Tree-style AND-type Match Lines and Segmented Search Lines," *IEEE International Solid-State Circuits Conference*, pp. 166-167, Feb. 2006

[91] Stallings, Williams. 1996. IPv6: The New Internet Protocol [Document on-line]. Available from http://www.ieee.org/ comsoc/stallings.htm; Internet.

[92] Po-Tsang Huang, Shu-Wei Chang, Wen-Yen Liu, and Wei Hwang, "A 256x128 Energy-Efficient TCAM with Novel Low Power Schemes", *IEEE International Symposium on VLSI Design, Automation, and Test*, 2007

[93] J. Zhang, Y. Ye, B. Liu, "A New Mismatch-Dependent Low Power Technique with Shadow Match-Line Voltage-Detecting Scheme for CAMs", *IEEE International Symposium on Low Power Electronics and Design*, pp. 135-138, Oct, 2006

[94] Http://www-device.eecs.berkeley.edu: BSIM 100nm and 70nm predictive technology process files.

[95] International Technology Roadmap for Semiconductors 2001 edition, Semiconductor Industry Association, http://public.itrs.net

[96] C.H. Hus, "Low Power Multi-Port Register File Design for Digital Sognal Processor," Master thesis, National Chiao-Tung University, June 2003.

[97] H. Qin, Y. Cao, D. Markovic, A. Vladimirescu, and J. Rabaey, "SRAM Leakage Suppression by Minimizing Standby Supply Voltage," *Proceedings of 5th International Symposium on Quality Electronic Design*, pp.55-60, 2004.

[98] T. Kawahara, M. Horiguchi, Y. Kawajiri, G. Kitsukawa, T. Kure, and M. Aoki, "Subthreshold Current Reduction for Decoded-Driver by Self-Reverse Biasing," *IEEE Journal of Solid-State Circuits*, Vol. 28, No. 11, pp. 1136-1144, Nov. 1993.

[99] Z. Chen, M. Johnson, L. Wei, and K. Roy, "Estimation of Standby Leakage Power in CMOS Circuits Considering Accurate Modeling of Transistors Stacks," *International Symposium on Low Power Electronics and Design*, pp. 239-244, 1998.

[100] B. H. Calhoun, F. A. Honore, and A. P. Chandrakasan, "A Leakage Reduction Methodology for Distributed MTCMOS," *IEEE Journal of Solid-State Circuits*, vol. 39, issue 5, pp. 818-826, May 2004.

[101] M. Anis, S. Areibi, M. Elmasry, "Design and Optimization of Multithreshold CMOS (MTCMOS) Circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 22, issue 10, pp. 1324-1342, Oct. 2003.

[102] Hulfang Qin, Yu Cao, D. Markovic, A. Vladimirescu, J. Rabaey, "SRAM leakage suppression by minimizing standby supply voltage," *International Symposium on Quality Electronics Design*, pp. 55-60, Mar. 2004

[103] Chung-Hsien Hua, Tung-Shuan Cheng and Wei Hwang, "Distributed Data-Rentention Power Gating Techniques for Column and Row Co-controlled Embedded SRAM", *International Workshop on Memory Technology, Design and Testing*, 2005

[104] International Technology Roadmap for Semiconductors, 1999 update

[105] T. Sakurai, "Perspectives on power-aware electronics," *IEEE International Solid-State Circuits Conference*, 2003. Page(s):26 - 29 vol.1

[106] H. Kawaguchi, K. Nose, T. Sakurai, "A super cut-off CMOS (SCCMOS) scheme for 0.5-V supply voltage with picoampere stand-by current," *IEEE Journal of Solid-State Circuits*, Vol. 35, Issue 10, Oct. 2000 pp. 1498 - 1501

[107] N.M. Madani, B. Tavassoli, A. Behnam, A. Afzali-Kusha, "Study of super

cut-off CMOS technique in presence of the gate leakage current," *The 16th International Conference on Microelectronics*, 6-8 Dec. 2004 Page(s):24 - 27

[108] Kyeong-Sik, H. Kawaguchi, T. Sakurai, "Zigzag super cut-off CMOS (ZSCCMOS) block activation with self-adaptive voltage level controller: an alternative to clock-gating scheme in leakage dominant era," *IEEE International Solid-State Circuits Conference*, 2003 Page(s):400 - 502 vol.1

[109] Kyeong-Sik Min, T. Sakurai, "Zigzag super cut-off CMOS (ZSCCMOS) scheme with self-saturated virtual power lines for subthreshold-leakage -suppressed sub-1-V-VDDLSI's," *Proceedings of the 28th European Solid-State Circuits Conference*, 24-26 Sept. 2002 Page(s):679 - 682

[110] Kyeong-Sik Min; Hun-Dae Choi, H-Y Choi, H. Kawaguchi, T. Sakurai, "Leakage-suppressed clock-gating circuit with Zigzag Super Cut-off CMOS (ZSCCMOS) for leakage-dominant sub-70-nm and sub-1-V-V/sub DD/ LSIs," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 14, Issue 4, April 2006 Page(s):430 - 435

[111] Y. Tsukikawa et al., "An Efficient Back-Bias Generator with Hybrid Pumping Circuit for 1.5-V DRAM's", *IEEE Journal of Solid-State Circuits*, Vol. 29, No. 4, pp. 534-538, April 1994

[112] P. Favrat, P. Deval and M. Declercq, "A High-Effiency CMOS Voltage Doubler", *IEEE Journal of Solid-State Circuits*, Vol. 33, No. 3, pp. 410-416, Mar. 1998.

[113] T.C. Chen and R.B. Sheen, "A Power-Efficient Wide-Range Phase-Lock Loop", *IEEE Journal of Solid-State Circuits*, Vol. 37, No. 1, pp. 51-62, Jan. 2002

Vita

PERSONAL INFORMATION

Birth Date: June. 19, 1982

Birth Place: Tainan, Taiwan, R.O.C.

Address: Department of Electronics Engineering
National Chiao Tung University
1001 Ta-Hsueh Road
Hsin-chu, Taiwan 30010, R.O.C.

E-Mail Address: liu.ee89@nctu.edu.tw

EDUCATION

B.S. [2005] Department of Electronics Engineering, Chiao-Tung University.

M.S. [2007] Institute of Electronics, National Chiao-Tung University.