低功率三態內容可定址式記憶體陣列與電路設計

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摘　　要

本論文利用多模式資料保存電源阻斷技術與超級阻斷電源阻斷技術的低功率技術，提出了一個新穎的高速低功率抗雜訊的三元內容可定址記憶體。利用這兩項低功率技術，記憶體陣列之漏電流將慘遭大幅削減。在搜尋模式下同時應用超級阻斷電源阻斷技術可同時明顯地降低搜尋功率。利用柏克萊預測模型，在65nm 下，一個高速低功率 256 行×144 位元之三態內容可定址式記憶體亦被提出，它可以達到超過 50%的漏電流削減，以及 9%的搜尋功率削減，並達到 0.047 fJ/bit/search 的能源表現以及 0.23ns 之搜尋時間。利用 TSMC 0.13 μm CMOS 技術來實現電路設計與佈局，顯示出所提出的架構對原本的記憶體陣列增加了 19%的面積。

Low Power Ternary Content Addressable Memory Array and Circuit Design

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ABSTRACT

A new high speed, low-power and noise-tolerant ternary content-addressable memories (TCAMs) using multi-mode data retention power gating technique and super cut-off power-gating technique are proposed in this thesis. These two techniques significantly reduce cell leakage current by taking the advantage of input don't care patterns of IPv6 addressing lookup application. Furthermore, search power is also reduced by applying super cut-off power gating technique under search operation. butterfly match-line scheme reduces switching activity also. A 256-word x 144-bit low-power ternary CAM is also proposed. Based on 65nm Berkeley Predictive Technology Model, simulation results shows that 0.23ns search time and 0.047fJ/bit/search energy metric is achieved. Layout is implemented in TSMC 0.13μm CMOS technology, which indicates a 19% area overhead.