Chapter 1
Introduction

1.1 Background

Content-addressable memory (CAM), also called associative memory, is a memory that implements the lookup-table function in a single clock cycle using dedicated comparison circuitry. In past decades, CAM is used in a wide variety of applications requiring high speed search ability. These applications are parametric curve extraction [1], Hough transformation [2], Huffman coding/decoding [3], [4], Lempel–Ziv compression [5]–[8], and image coding [9]. At present, CAM is popular in network routers for packet forwarding, packet classification, asynchronous transfer mode (ATM) switches, and so on.

A CAM cell contains 1-bit storage memory and 1-bit comparison circuit. Based on different forms of storages, it could be divided into two type of CAM cells. The first one is called static CAM cell which is implemented by SRAM, and the other one is called dynamic CAM cell which consists of capacitance. A conventional CAM cell, also called binary CAM (BCAM) cell, has two states: “one” state and “zero” state. Therefore, BCAM cell just needs one storage memory to store data. On the other hand, there exists another kind of CAM cell, called ternary CAM (TCAM) cell. Different from BCAM cell, the TCAM has an extra state, don’t-care, which is suitable to be used in network applications. Because TCAM cell has this extra state, TCAM cell needs an additional storage memory to store data.

According to match-line scheme of CAM, there are two different types of match-line scheme. While stored data is not exactly the same as search data in every bits, the match-line would be discharged to ground. This match-line is called

NOR-type match-line scheme. The other one is AND-type match-line scheme.[1] With AND-type match-line scheme, the match-line would be discharged to ground only when all bits of stored data match with all bits of search data. Generally, NOR-type match-line scheme has shorter search time but consumes more search power. On the contrary, AND-type match-line scheme consumes less search power but needs longer search time to complete each search operation.

1.2 Motivation

Energy-efficient design is essentially important for the future System-on-Chip (SoC) design. CAM compares input search data against a table of stored information, and returns the address of the matching data [10]-[14]. CAMs have a single clock cycle throughput making them faster than other hardware- and software-based search systems. However, the speed of a CAM comes at the cost of increased silicon area and power consumption. As CAM applications grow, the larger CAM size demanding, the further exacerbated power problem. Reducing power consumption, without sacrificing speed or area, is the main thread of recent research topic in large-capacity CAMs.

Internet Protocol Version 6 (IPv6) [15] is the "next generation" protocol designed by the IETF to replace the current version Internet Protocol, IP Version 4 ("IPv4"). IPv6 addresses are 144-bit identifiers for interfaces and sets of interfaces [16]. Each address needs 144 TCAM cells to store data results a long search delay path in network routers for packet forwarding application. As mentioned before, AND-type TCAM has more search power saving but longer search time is the price. Thus, reducing the search time by modifying TCAM architecture becomes the inevitable issue. Furthermore, large amounts of TCAM cells result in large capacitance on search-line which could cause large power consumptions.

With the advance of technology and SoC design, coupling noise, charge sharing and power/ground fluctuation noises are increasing the soft-error rate of dynamic circuits. Since AND-type match-line scheme belongs to dynamic circuits, noise immunity is a serious issue for CAM design. Recently, several techniques have been

[1] Because the principles and operations of AND-type match-line schemes like ones of NAND-type match-line schemes, we call NAND-type match-line scheme as AND-type match-line scheme in this thesis.

developed to improve the noise immunity in dynamic circuits. However, all of them have extra price, like more power consumptions, longer propagation delays, and larger area overheads.

According to above issues, this thesis focuses on the techniques of search time and dynamic power reduction in an energy-efficient TCAM. Moreover, we also care about the noise immunity of match-line schemes. A noise-tolerant butterfly match-line scheme and don't-care based low power technique which can reduce search time and dynamic power would be applied to TCAM design for IPv6 application.

1.3 Organization

The organization of this thesis is as follows. An overview of CAM is introduced in Chapter 2. Here, a conventional CAM architecture including CAM cells and CAM word schemes would be presented. Besides, the application and prior arts of CAM would be described in this chapter as well.

The multi-mode data retention power gating technique is realized in Chapter 3. The proposed multi-mode data retention power gating technique achieves the standby power reduction without cause much area and search time overhead. Although its performance is don't care percentage sensitive, however, it achieves significant standby power reduction even without don't care.

Super cut-off power gating technique is proposed in Chapter 4. Although the use of voltage generators cause much power overhead, simulation result shows that with technology advances, the power saving will outstrip the power overhead. By use the characteristic of addresses of IPv6, almost all don't care cells can be put into super cut-off mode. Furthermore, by applying super cut-off mode during search operation, search power is also reduced. As a result, power consumption can be significantly reduced.

An energy-efficient ternary CAM array is implemented in Chapter 5. In this chapter, multi-mode data retention power gating technique and super cut-off power gating technique is applied, which reduce both standby power and search power. A novel ternary content addressable memory which combines butterfly match-line scheme, don't-care based low power technique [92], XOR-based conditional keeper

[17], pseudo-footless clock, data pre-charge dynamic (PF-CDPD) circuit [18], multi-mode data retention power gating technique and super cut-off power gating technique is proposed. The proposed TCAM array has not only smaller standby power but also consumes less energy per bit per search operation. Moreover, there is only a little area overhead about the proposed TCAM scheme. Finally, the overall investigation results and conclusions will be discussed in Chapter 6.