國 立 交 通 大 學

電子工程學系 電子研究所

博 士 論 文

薄膜電晶體主動式矩陣面板之陣列技術研究

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研 究 生： 陳 紀 文
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推　薦　函

事由：推薦電子研究所博士班研究生陳紀文提出論文，參加國立交通大學博士論文口試。

說明：本校電子研究所博士班研究生陳紀文，業已修畢部訂所需課程學分，通過博士資格考之學科考試，並完成博士論文「薄膜電晶體主動式矩陣面板之陣列技術研究」初稿，且有數篇相關之論文發表或送審，茲列舉如下：

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7. " Temperature Effects of N-channel Poly-Si TFT", *Electrochemical and Solid-State Letters* (submitted)

綜上所陳，陳君已具備國立交通大學電子研究所應有之教育及訓練水準，謹此推薦陳君參加交通大學電子研究所博士論文口試。

此致

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中 華 民 國 九 十 四 年 5 月 18 日

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摘要

本論文首先提出一種具有高導通電流的新穎非晶矽薄膜電晶體元件結構。將Akiyama所提出之遮光結構(light-shield)結構改善，利用多一次重摻雜的非晶矽(n+ a-Si)沉積的引入，將縮於閘極內的非晶矽主動區包圍起來，可以有效阻止金屬與本質非晶矽的接觸，所以光漏電流與暗漏電流皆有明顯改善；此外由於比傳統BCE 結構多了側壁導通區，使得部份載子可以直接透過側壁進出，有效降低汲/源極寄生電阻，使得整體新結構非晶矽元件導通能力上升，比相同製程之傳統BCE結構提升了 50%的導通能力，載子遷移率可達 1.05 cm^2/Vsec，新結構元件可應用於大尺寸電視所需之高導通能力畫素開關元件或是用來驅動有機發光二極體(OLED)。

此外，由於多晶矽薄膜電晶體能夠整合週邊驅動電路進而由於多晶矽元件應用於面板週邊驅動邏輯電路時，需要考量到多晶矽元件可靠度的問題，本論文針對多晶矽元件在AC gate bias stress之後的劣化機制做一深入探討，研究中發現

AC gate bias stress 會造成元件導通電流嚴重的下降，但其起始電壓變化並不大，根據Seto理論，我們計算出元件劣化前後其有效缺陷密度(effective trap density)，由原本的 $1.42\times10^{12}cm^{-2}$增加至 $3.14\times10^{12}cm^{-2}$，並且由其劣化趨勢推論這些缺陷大部分屬於tail states，同時汲/源極寄生電阻的也急劇增加；藉由在較高的源極電壓下操作使元件在saturation region (Vds>Vgs)並且有pinch-off region在汲極附近產生，可以發現導通電流劣化的程度縮小，故可以判定劣化區域是靠近汲/源極，因為在pinch-off region中，載子不再限定於通道表面傳輸而是可以透過bulk方式傳輸，若是AC stress產生的大量tail states位於汲極附近的通道表面，當pinch-off region 在汲極附近產生，載子便可避開這些高電阻區而透過bulk傳輸到汲極，故其導電特性與會隨汲極端電場而有所變化。

本論文也研究探討多晶矽薄膜電晶體元件的溫度效應，首先對 non-LDD 的薄膜電晶體做研究，實驗發現 non-LDD 的元件會隨著溫度下降而導通電流增大，主要原因是因為聲子散射(phonon scattering)的緣故，聲子主要是源由晶格熱震動所產生，聲子會隨著溫度上升而增加，溫度下降而減少，若載子與聲子間的碰撞越多其自由路徑會越短，載子遷移率也會隨之下降。然而在 LDD 元件中，元件導電率與溫度成正比，溫度越高導電率越高，LDD 元件與溫度關係與 non-LDD 元件逕相庭徑，為了釐清兩者之差別，本論文觀察 N+ 與 N- 的片電阻率隨溫度的關係，然而 N-電阻率隨著溫度上升而嚴重下降，N+ 則較不受溫度變化影響，由於 N-中摻雜濃度並非達到使多晶矽導電程度達到簡併態，其自由載子濃度為有效摻雜濃度扣除缺陷態位密度，而隨著溫度下降而參雜活化比率下降，所以 N-阻值上升，故 LDD 電阻特性對於元件溫度效應中扮演一重要角色，為確保在適當溫度範圍內面板能正常工作，這些元件的溫度函數是未來電路或是面板設計上一大考量。

本論文中有探討新型側向結晶方式 Sequential Lateral Solidification (SLS)所製作出的多晶矽元件其電性與可靠度，由材料分析上可發現 SLS 所產出的晶粒尺寸比一般傳統 excimer 雷射來得大，我們可以將 SLS 晶界分為二種：一為主晶界(main-GB)，二為次晶界(sub-GB)，主晶界的特徵在於其晶界走向垂直元件通道方向，並且在多晶矽薄膜結構中為一突起(protrusion)；次晶界則是平行通道方向且較平坦，論文中挑選兩種較明顯對比之電晶體進行分析，GB-TFT 為一含有

主晶界在通道中央，NBG-TFT 中則僅有次晶界存在，由電晶體參數萃取可發現 NGB-TFT 其起始電壓、次臨界擺動、載子遷移率都比 GB-TFT 優良；然而在 hot carrier stress 實驗中則是 GB-TFT 展現較高的可靠度，透過模擬軟體的計算分析可發現由於 GB-TFT 通道中央存在有主晶界的存在，這個高缺陷密度的區域能有效降低汲極端電場，進而降低了 hot carrier effect。

本論文也研究兩種 poly-Si EEPROM 元件結構，一為 floating gate 為儲存電荷單元，另一為 SiN 為電荷儲存層。本論文首先提出新的 doping 方式來改善 floating gate EEPROM 的閘極電壓耦合效果，可以降低記憶寫入電壓，或是擁有較快的寫入速度，而且元件導通電流也被提昇了；此外利用 Oxide/Nitride/Oxide 的堆疊，可以在玻璃上製作 EEPROM 元件而達到與晶圓上 MONOS 的記憶效果，實驗中的穿遂氧化層厚度為 15nm，氮化矽為 15nm，Block oxide 為 25nm，本論文也發現利用 F-N tunneling 寫入抹除的方式，比較不會破壞多晶矽記憶體元件的特性，若是以 Channel hot carrier 方式的話會造成元件開關特性的劣化，起始電壓的飄移，這是由於多晶矽的閘極氧化層為低溫沉積，其品質較晶圓熱氧化層差，而且熱載子效應會因為玻璃絕緣基板的 floating body effect 而更嚴重，會使得多晶矽元件閘極氧化層容易劣化。

本論文最後研究具有低 RC 延遲之連線技術，相似於 IC 的多層導體連線技術發展，Cu 導線與 low-k 材料將是最佳的選擇。本論文先就一種多孔隙的 low-k 材料進行基本特性研究，量測其介電常數並觀察漏電流等等，由於多孔隙材料其孔隙度高，表面積也相對來得大，容易造成水氣吸附在表面並造成的介電特性改變。此外，銅金屬與 low-k 材料的整合會面臨到銅金屬擴散造成 low-k 材料劣化，論文中就水氣造成銅金屬擴散問題作一深入分析，實驗發現水氣會使銅離子更容易在高電場驅策下而進入 low-k 中。而為了避免銅金屬擴散問題，可以引入介電阻障層來隔絕銅金屬與 low-k 直接接觸，研究中探討了 SiCN 絕緣薄膜對阻擋銅擴散的能力的表現，觀察不同氮含量的材料組成對於阻障能力的影響，最後本論文也提出一個 SiCN 阻障層漏電流劣化的物理模型。

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Abstract

A novel technology for manufacturing high-performance hydrogenated amorphous silicon (a-Si:H) TFT is first developed in this thesis. In the bottom gate light-shield a-Si:H TFT structure, the side edge of a-Si:H island is capped with an extra deposition of heavily phosphorous-doped a-Si layer. Such an ingenuity can effectively eliminate the leakage path between the parasitic contacts between source/drain metal and a-Si:H at the edge of a-Si:H island. In addition, our proposed a-Si:H TFT device exhibits superior effective carrier mobility, as high as 1.05 cm^2/Vsec due to the enormous improvement in parasitic resistance. We have evidenced that the leakage current of proposed TFT is lower than the conventional BCE device under bottom-side illumination of 6000 nits. It also exhibits the better ability against the DC current stressing. The impressively high performance provides

the potential of the proposed a-Si:H TFT to apply for AMLCD and AMOLED technology.

Next, the temperature and AC gate pulse stress effects on ELA poly-Si TFT have been demonstrated. We find that the conducting current of non-LDD poly-Si TFT is increasing with the decreasing in the temperatures. The phonon scattering is responsible for the evolution of carrier mobility in poly-Si TFT at temperatures. However, the LDD poly-Si TFT is obviously influenced by the LDD layers extended outside the gate electrode. LDD sheet works as a larger resistor at low temperature than that at high temperature. These results can provide the designers to consider the temperature effects for the poly-Si TFT application in a suitable temperature range.

In addition, the distinct decrease in ON-current of n-channel poly-Si TFT was found during the dynamic voltage stress. In spite of electrical degradation appearing at the ON-current of the poly-Si TFT, both the sub-threshold swing and threshold voltage kept in a good condition. This can be inferred that the tail states were produced in ploy-Si film due to the AC stress. Additionally, the current crowding effect was increased with the increasing of stress time. The parasitic resistances extracted from the I_D-V_D curves of poly-Si TFTs were significantly increased after the 1000 s stressing. The effective trap density of poly-Si TFTs stressed for 1000 s was 3.14×10^{12} cm^{-2}, 2.21 times larger than that of the un-stressed device. The creation of effective trap density in tail-states is responsible for the raise of the parasitic resistance and the degradation in ON-current of TFT. Moreover, the damaged regions whicn contains numerous trap states are evidenced to be mainly located near the source /drain regions.

On study the grain –boundary (GB) effects, the comparison of electrical stability between GB and NGB-TFT has been demonstrated. The NGB-TFT owns superior conducting ability than the GB TFT which contains a 100-nm trap-numerous region at

the middle of the channel. However, the GB-TFT exhibits the better endurance against DC stress than the NGB-TFT. Based on the simulation result, the existence of GB in the middle of channel of poly-Si TFT would reduce the electric field in the drain region significantly. Accordingly, the GB-TFT suffers relatively lighter impact of hot carrier stress and maintains electrical characteristics well during the DC stressing. The NGB-TFT was seriously degraded by the DC stress with the high electric field at the drain side. Nevertheless, the distinct electrical behaviors of the TFTs were demonstrated under the AC gate bias stress. Due to the existence of protrusion in the channel, GB-TFT shows weaker endurance against the AC gate pulse stress than that of NGB TFT. The magnitude of the vertical field at the protrusion is stronger than the other regions in GB TFT. The strong electric field would lead to the state creation and charge trapping at the protrusion and reduce the device's electrical performance.

On the study of non-volatile memory devices fabricated on glass using low temperature poly-Si technology, two structures have been fabricated and characterized. One is floating-gate device and the other consists of the oxide-nitride-oxide stack structure. The maximum temperature of processing is below 650^{o}C for the glass substrate. The floating-gate memory device consists of two active regions of poly-Si layer, one behaves as the control gate and the other is the conducting channel region. The control-gate transistor of the device is proposed to consist of a whole heavily-doped poly-Si sheet. The higher coupled efficiency of gate bias is demonstrated in the proposed structure. Also, the characterizations of MONOS type memory with an oxide-nitride-oxide (ONO) stack structure were studied. In comparison with channel hot carrier injection, the *Fowler-Nordheim* tunneling method is more suitable for the programming of the poly-Si memory device. The memory widow of devices can reach 1.5V under the programming voltage of 20V for 10ms.

The device maintains a wide threshold voltage window of 1.5V after 10^4 program/erase cycles. Moreover, it retains a good retention property without a significant decline of the memory window up to 50 hours at 60^{o}C.

On the study of interconnections with low-RC delay, the porous organosilicate glass (POSG) and a-SiCN have been investigated. The lager leakage current is observed in hot-water dipped POSG sample. The leakage current would be increased and dominated by the ionic conduction as the moisture is contained in the POSG. Additionally, the moisture would enhance the Cu to penetrate into POSG and cause the raise of the leakage current. To avoid the Cu contamination in the interconnections, the electrical properties and stabilities of barrier dielectric a-SiCN films are investigated. The leaky behavior of a-SiCN is evidenced to be Pool-Frenkel conduction in high electric field region. Experimental results indicate that a-SiCN films containing higher nitrogen concentration exhibits better barrier ability. The dielectric breakdown is due to the penetration of Cu. It is observed that the main conduction of post-breakdown a-SiCN at room temperature (298K) is space-charge-limited current (SCLC) due to numerous Cu impurity/traps. Moreover, the characteristics at low temperature can be separated into two distinct stages, Fowler–Nordheim tunneling and space-charge-limited current (SCLC) conduction. We propose a physical model which post-breakdown a-SiCN was composed of two different conduction regions. It can well describe the electrical variation resulted from the Cu traps and temperature.

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歷經了數個寒暑，此論文在盛夏蟬鳴聲中逐漸完成，站在求學歷程的回憶長廊，回頭一望這段眾多人事物交織而成的精彩場景，盡是滿滿的溫暖與感激，是生命的深刻，深覺意長紙短，實在難以用簡短的文句恰如其分的表現出來。在交大博士班的修業期間，首先要特別感謝兩位指導教授 — 曾俊元教授及張鼎張教授，在這兩位教授多年來的教誨與鼓勵下，使我不斷充實成長並得以順利完成論文。曾教授圓融的處事態度及認真為學的精神，讓學生獲益良多，且於我研究上遭遇挫折時適時的給予我啟發與鼓勵，是一個博學而仁慈的長者。張鼎張教授費心指導我論文研究，並於人生規劃上有諸多啟示，而張教授積極處事的態度與研究創意巧思亦讓學生收穫良多。學生能夠師承兩位師長的指導，我感到十分幸運與十二分榮幸。

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陳　紀　文

誌於 風城交大

2005 年 盛夏

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Chapter 1

Introduction

1.1 General Background

Thin film transistor (TFT) is a metal-oxide-silicon field effect transistor (MOSFET) fabricated on an insulator substrate by employing all thin film constituents. Thin film transistors have been widely used as switching devices in flat panel display, such as active-matrix liquid crystal display (AMLCD)[1.1-1.5] and active-matrix organic light emitting diode (AMOLED) display. [1.6-1.10] The thin film transistors can be mainly divided into two types according to the active layers, amorphous and poly-crystalline ones. The amorphous TFT is usually applied in large size flat panel display due to its mature manufacture and low-cost. On the contrary, poly-Si TFT is suitable for the high-resolution medium and small size flat panel display. The high mobility of a-Si TFT is required for high resolution AMLCD since the charging time of pixel is shorter than the low resolution one. However, the numerous trap states existed in a-Si layer seriously strict the transporting of carriers.[1.11-1.13] The application of poly-Si TFT is attractive due to the higher mobility than the a-Si one. The higher mobility and existence of complementary devices lead to integrate functional circuits on the display. Moreover, introduction of the new device, such as EERPOM, can increase the feasibility of circuit design for the flat panel.[1.14-1.15] The improvement of electrical characteristics and understanding of degraded mechanism of TFTs is important for development of display technology.

Additionally, the interconnections with low-RC delay have been received increasing attraction in the ICs and flat panel display applications. To improve the

performance of ICs, the scaling down for integrated circuits is necessary. The shrinkage in critical dimension of active devices would also result in smaller linewidth and spacing between metal interconnections. Moreover, the length of interconnection lines will increase due to the larger chip size, which is the result of getting profitable and excellent IC performances. As a result, a larger part of the total circuit propagation delay (RC delay) is contributed more from the characteristics of the interconnections than that of the scaling of devices. [1.16-1.20]

Similar to the RC delay issues in ICs fields, the lager-area flat panel display such as active matrix liquid crystal displays (AMLCD's) are also currently suffered the RC delay impacts.[1.21-1.22] Large-area high-resolution AMLCD are on their way to becoming an elegant alternative to CRT displays in televisions. However, several fundamental scaling problems are encountered when trying to increase the display size. One of them is associated with the gate metallization for the inverted-geometry thin-film transistors (TFT's) of the active matrix. At present, refractory metals such as tantalum/ molybdenum are used, to ensure stable contacts during TFT fabrication. The gate lines are deposited first onto the glass backplane. They must be thin to ensure good step coverage by the plasma-enhanced chemical-vapor deposited (PECVD) layers. The relatively high refractory metal resistivities result in RC gate delays that restrict the AMLCD size. It is obvious that the gate line pulse suffers distortion as it moves through the line. The distortion increases the rise time and delays the arrival of the gate pulse. The delay can cause the gate and data pulses to arrive at a pixel out of synchronization. As a result, low resistivity metals and low-dielectric are required for high-performance ICs and large-area AMLCD's.

1.1.2. Thin film transistors technology

Amorphous silicon technology is quire attractive due to its low processing temperature and low cost manufacture. The hydrogenated amorphous silicon (a-Si:H) thin film transistors (TFT) have been applied on the flat panel displays and X-ray sensor arrays. There are four structures for a-Si:H TFT's, including staggered, inverted staggered, coplanar and inverted coplanar TFT's, as shown in Fig 1-1. Among these four structures, the inverted staggered one is most popular due to its simple process and acceptable electrical characteristics. Therefore, the inverted-staggered back-channel-etched (BCE) type of a-Si:H TFT has been widely used as a switching element to control the gray level in liquid crystal display(LCD) and to drive organic light-emitting-diode (OLED). With increasing the resolution and size of AMLCD, the charging time of the pixel is decreased with a fixed frame rate. Except to reduce the RC delay of interconnections, the a-Si TFT with high driving capability is required for the large area AMLCD. In addition, a-Si:H TFT with high stability and driving capability is suitable for AMOLED application since OLEDs require a current driving scheme in contrast to LCD, which are voltage driven.

Compared with a-Si TFT technology, the poly-Si TFT technology has some distinct advantages but its manufacture is more complex and high cost. The major advantage of poly-Si TFT is the higher field effective mobility than that of the amorphous silicon (a-Si) based devices. The high carrier mobility and the existence of complementary pairs permit the integration of drive circuits and the smaller area of pixel transistor. The integration of drive circuits could reduce manufacturing costs, and increase the functionality of large-area microelectronics.[1.23-1.24] The smaller area of pixel transistor leads to a larger aperture ratio for a given pixel size, or enables a higher resolution display for a given aperture ratio, resulting in better image quality. Moreover, the poly-Si TFT could be applied to the active matrix organic light emitting

diode (AM-OLED) display due to its high current driving capability. The degree of circuit integration will continue to increase as device characteristics improve further. Additionally, the new functional devices fabricated on the glass can increase the flexibility of circuits for the display. The nonvolatile memories, such as flash memories and electrically erasable PROM's (EEPROM's) fabricated on the wafer, have been widely used for the applications of high-density memories, programmable logics, and microcontrollers. [1.25-1.26] Similarly, the applications of non-volatile memories on the system of flat-panel are attractive. The smart cards consist of memory and RF logic circuits can be fabricated on the low-cost substrate such as plastic and glass ones. In poly-Si TFT devices, however, the status of defect states at grain boundaries plays a crucial role for electrical characteristics, as shown in Fig. 1-2. The stability of poly-Si TFT is one of the important issues for poly-Si technology. Recently, there have been several investigations about the stabilities of poly-Si TFT's. The creation of trap states at poly-Si/gate dielectric interface or the charge trapping in the gate insulator is responsible for the degradation in electrical characteristics of poly-Si TFTs. Since the large area electronics or the flat-panel displays comprised of poly-Si TFTs are used by peoples at the globe, the displays should keep the performances well at temperatures. However, temperature usually influences the characteristics of solid-devices, and relative effects are important for the application of Poly-Si TFT technology. Consequently, it is important to introduce the new functional device into poly-Si technology and understand the fundamental properties of poly-Si TFTs such as electrical stressing degradation, grain boundary effects, and temperature effects.

1.1.2 Interconnections with low-RC delay

The RC delay of interconnections is mainly contributed to the resistivity of metals and capacitors of insulators. In the medium 1990's, the National Technology Roadmap for Semiconductors (NTRS) described the first needs for new conductor and dielectric materials to meet the projected overall IC technology requirements [1. 27]. Similarly, some of research reports have shown that the gate pulse delay is getting serious with the increasing of the size of large area AMLCD. The resistance and capacitance (RC) delay of the gate line retards the turnoff of the transistor at the far end of the gate line. Moreover, the coupling capacitance resulting from pixel electrode and the data and gate line would lead to the cross-talk and signal distortion. To minimize the coupling capacitance, the low-k materials should be introduced into the interconnection of flat panel display. Also, the implantation of low-k in display can achieve a high aperture ratio for improved light transmittance or image quality, as shown in Figs. 1-3(a) and (b). This requires a thick, low dielectric constant (k) material as an inter-level dielectric.

Thereafter, there were many new interconnect materials and structures extensively studied in the industrial and academic committees. For the low-resistivity materials, Cu conductive metal has been recognized to apply to IC technology and flat panel displays due to its low resistivity (1.67 μΩ-cm for bulk materials) and high electromigration resistance. [1.28-1.29] Moreover, the investigation of low-k materials on its physical, chemical and electrical properties is very important for the progress of display technology. There are two principal methods to form low-k films. One is the chemical vapor deposition (CVD), and the other is the Spin-on deposition (SOD). The conventional passivation material was CVD deposited nitride whose dielectric constant is about 6~7. Moreover, CVD method is easily compatible to the standard display processes.

The other technique of forming low-k materials is spin-on deposition (SOD). This

method is using a liquid precursor deposited by spin-coating or spray method. Then, the substrate is subjected to a series of baking. Finally, a furnace curing or UV curing s performed to achieve the network low-k structure. Some SOD low-k materials, additionally, can be patterned by photolithography. The SOD type of low-k materials possesses the features of good gap filling, local planarization and low dielectric constant. In general, most of SOD low-k materials can be divided into two categories. One is organic polymer, and the other one is inorganic silica-based materials.

The interconnections made of Cu and low-k owns lower RC delay to meet the requirements in advance IC and display application. However, one of the reliability issues in Cu/low-k metallization is the dielectric degradation caused by Cu ion penetration. Copper rapidly drifts in silica-based low-dielectric-constant (low-k) materials during bias-temperature stressing (BTS). Moreover, the Cu atom plays as the generation/combination trap center in Si films and seriously influences the performance of Si-based devices. The insertion of barrier dielectrics between Cu wiring and low-k dielectrics is essential for a reliable copper interconnect technology. Silicon nitride (SiN_x) is a good barrier dielectric and efficiently prevents the Cu drift,[3] but its dielectric constant is too large (~7). SiN_x, thereby, needs to be substituted to reduce the effective capacitance for interconnection applications.[4] Studies on barrier dielectrics with lower dielectric constants related to SiN_x, are receiving much attention. Recently, silicon-carbie (SiC) based materials with k<5 are proposed for the barrier dielectric applications.[5-6] But the reliability and degraded mechanism have not been investigated detail.

1.2 Thesis Outline

The dissertation is organized into the following chapters:

In chapter 1, a brief overview of the TFT technology and the interconnections with

low-RC delay is introduced to describe the various applications of them. We describe the trend of TFT technology development and the degradation of low-k caused by Cu penetration. Then, the outline throughout the dissertation is discussed here.

In chapter 2, a new structure of beck-channel etching (BCE) a-Si TFTs was first proposed. This novel device owns superior performance than the conventional one. The ON-current of the new devices is 1.5 times the conventional BCE device. Moreover, the proposed device owns low leakage current either in dark or under bottom-side illumination.

In chapter 3, the temperature and AC stress effects on poly-Si TFT are studied, separately. The electrical characteristics of n-TFT with/without LDD are measured at temperatures. The characterizations of the n-TFTs without LDD under AC gate-bias stressing are investigated to clarify the degradation mechanism.

Chapter 4 contains two parts. For part I, the grain boundary effects of poly-Si TFT were discussed. The electrical properties of TFTs are compared to clear the carrier transport in poly-Si TFT . For part II, the influence of grain boundary in reliability is investigated under DC and AC stress.

In chapter 5, we demonstrated two kinds of the non-volatile memory devices fabricated using low-temperature poly-Si technology. The programming and erasing methods for poly-Si memory devices are also investigated. Moreover, the electrical characteristics and reliabilities of devices

In chapter 6, the intrinsic properties of low-k nano-porous silica and the impact of moisture absorption for interconnect applications are investigated. In addition, the reliability of nano-porous silica with Cu electrode using bias-stressing method is also demonstrated in this chapter.

In chapter 7, the intrinsic properties of barrier dielectric film, a-SiCN, are investigated. The breakdown mechanism of barrier dielectric caused by Cu penetration is depicted.

In chapter 8, we summarize our experimental results and give a brief conclusion. Recommendations of several topics relevant to the thesis are also given for further study.

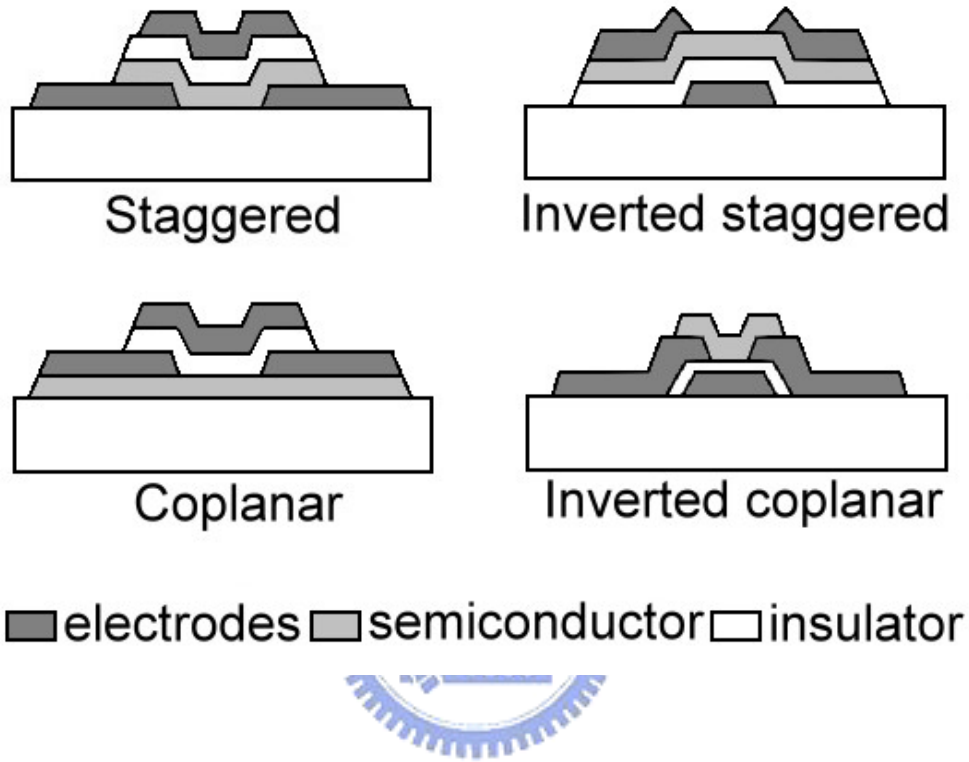

Fig. 1-1 Four structures for a-Si TFTs.

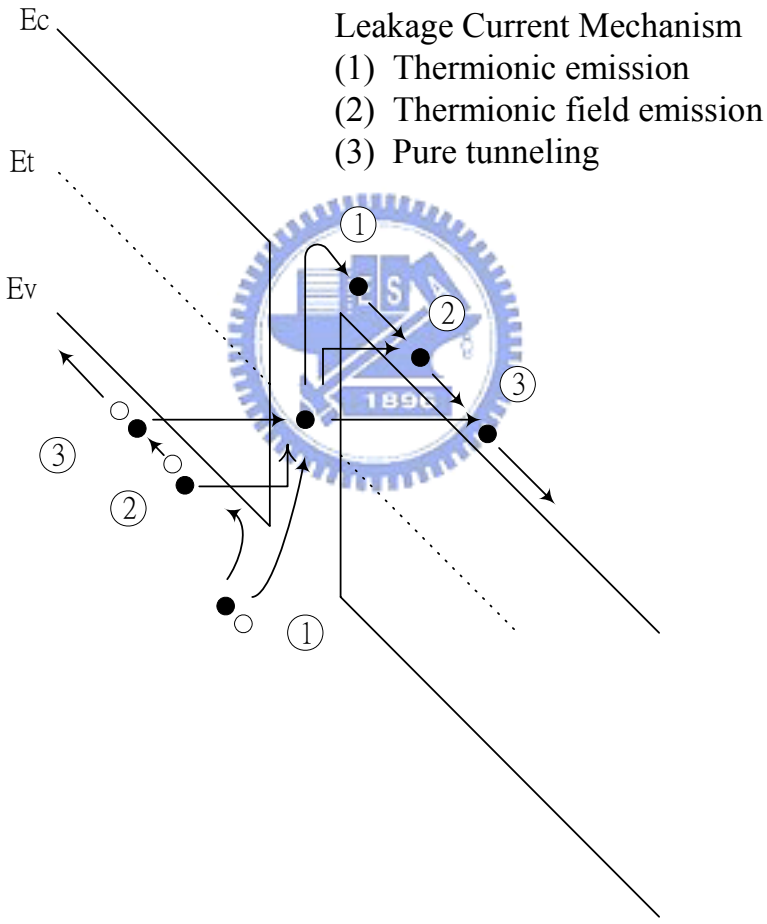

Fig. 1-2 Three possible mechanisms of leakage current in poly-Si TFTs, including thermionic emission, thermionic field emission and pure tunneling.

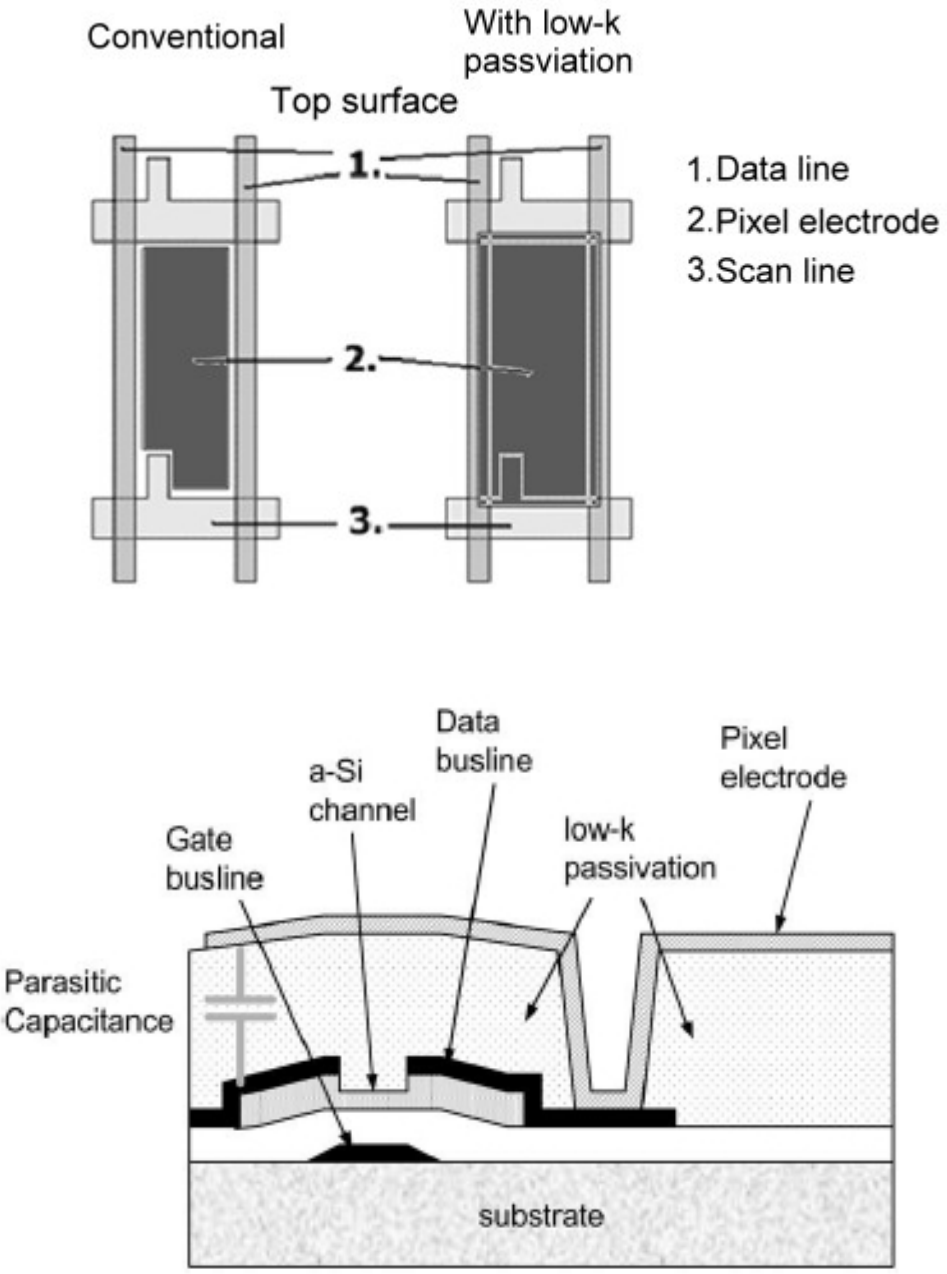

Fig. 1-3 (a) Plan view of the pixel using low-k passivation technology.
(b) Low dielectric constant (k) material as an inter-level dielectric.

Chapter 2

High Performance amorphous Silicon TFT

2.1 Introduction

Amorphous silicon technology is very attractive due to its low processing temperature and low cost manufacture. The hydrogenated amorphous silicon (a-Si:H) thin film transistors (TFT) have been applied on the flat panel displays and X-ray sensor arrays. There are four structures for a-Si:H TFT's, including staggered, inverted staggered, coplanar and inverted coplanar TFT's. Among these four structures, the inverted staggered one is most popular due to its simple process and acceptable electrical characteristics. Therefore, the inverted-staggered back-channel-etched (BCE) type of a-Si:H TFT has been widely used as a switching element to control the gray level in liquid crystal display(LCD) [2.1-2.5] and to drive organic light-emitting-diode (OLED). [2.6-2.12] TFT with a large switch ratio and low off-state leakage current is suitable to control LCDs. In addition, a-Si:H TFT with high stability and driving capability is suitable for AMOLED application since OLEDs require a current driving scheme in contrast to LCDs, which are voltage driven.

The a-Si:H material is a well-known photoconductor and its conductivity increases drastically resulting from the generation of electron-hole pairs under illumination of a visible light.[2.13-2.15] However, LCD panels are usually used in an illumination environment such as under the back-light. Therefore, the leakage current of TFT under back-light illumination in TFT-LCD displays should be reduced to avoid losing the storage charges in the pixel. Akiyama et al. has demonstrated the light-shield

structure for the TFT using in AMLCDs.[2.16] Figure 2-1(a) and 2-1(b) show the conventional and Akiyama's structures, respectively. The major difference between them is that a-Si:H island is completely located inside the coverage of gate metal in Akiyama's structure. The gate metal effectively shields the back-light irradiating to a-Si:H layer, as shown in Fig. 2-1(b). However, the edges of a-Si:H island are direct contact with the source/drain (S/D) electrode, when the TFT fabricated with the deposition of metal deposit on the tri-layer(SiN_x/ a-Si:H/n^+ layer), as shown in Fig. 2-1(b). The metal/a-Si:H contact usually exhibits the Schottky type conduction, being subjected to the leakage.[2.13]

We propose a new and convenient technology to reduce the leakage current originated from the leaky contact between the metal and a-Si:H layer in this study. The turn-on current of the proposed TFT is also increased due to the reduction in parasitic source/drain resistance. Moreover, the proposed TFT exhibits better stability than the conventional BCE TFT under the current stress.

2.2 Experimental Procedure

The fabrication process of the proposed TFT device is described as below. The inverted staggered a-Si:H TFT's were fabricated, but the a-Si:H active island of TFT is located inside the coverage of gate metal electrode. First, metallic Cr was deposited on glass substrates by sputtering and then was patterned to form gate electrodes. It was followed by SiN, undoped a-Si:H and phosphorous-doped a-Si:H (n^+ a-Si:H) layer deposition sequentially on the Cr patterned glass, without breaking the vacuum in a plasma-enhanced chemical vapor deposition (PECVD) chamber. The SiN layer was deposited using a mixture of SiH_4 and NH_3 gases at a substrate temperature of 300^{o}C and the undoped a-Si:H was deposited from a gas mixture of H_2 and SiH_4 at

300 ^{o}C. The film thickness of Cr, SiNx, a-Si:H and n^{+} a-Si:H layers was 150, 200, 150 and 20 nm, respectively. The definition of a-Si:H active region was performed with lithography and etching processes. In our proposed new TFT, the second layer of 20-nm-thick n^{+} a-Si:H film was deposited to clad the active regions. Aluminum film was evaporated to form the source/drain electrodes. Finally, the patterned Al films were used as a mask to etch back the channel to isolate the source and drain electrodes of TFT. In the proposed process, only three masks were required to fabricate TFT and the number of mask is equal to the conventional BCE procedure. Figure 2-1(c) illustrates the new structure of our proposed light-shied TFT device. It should be noted that the proposed TFT described above consists of 20nm n+ layer at the edge and 40nm n+ layer on the top of the active island. We performed the DC stress using Agilent 4156 analyzer on the TFTs to evaluate the stability of TFTs.

2.3Results and Discussions

The solid and dashed lines in Fig2-2 indicate transfer characteristics of light-shield a-Si:H TFTs fabricated with conventional as well as our proposed process, respectively. The leakage current of Akiyama's light-shield TFT is as high as two order the proposed TFT under the simialr negative gate voltages. The S/D metal/intrinsic a-Si:H contact at the edge of a-Si:H island, as shown in Fig. 2-1(b), usually behaves as the Schottky emission.[2.13] On the contrary, the capped n^{+} a-Si layer on the a-Si:H island effectively avoids the direct contact between a-Si:H and S/D metal, as shown in Fig. 2-1(c). The n+ a-Si:H layer can effectively block the hole current when the gate is biased with negative voltages. The leaky path between the metal/intrinsic a-Si:H was thus eliminated and the leakage current was reduced. Under

the same applied gate voltages, the leakage current of Structure C is two orders of magnitude lower compared to the Structure B. In addition, the proposed TFT structure exhibits superior current driving capability, as shown in Fig. 2-3. The turn-on current of the new TFT is about 1.5 times higher than that of Structure A, the conventional inverter-staggered counterpart. Using the proposed structure in this work, the TFT with effective mobility of 1.05 cm^2/Vsec extracted at V_d = 0.1V was obtained. The carrier mobility of conventional inverter-staggered TFT, structure A, fabricated with the same process is 0.72 cm^2/Vsec. Moreover, the threshold voltage of the proposed TFT is 2.3V, extracted at current density of 1 nA with normalized channel width (W)/channel length (L) ratio and lower than the conventional inverter-staggered one (2.8V). To compare the leakage current between the proposed and the conventional BCE TFTs under illumination, the electrical measurements were performed under white-light illumination of 6000 nits underneath, as sketched in the inset of Fig. 2-4. Fig. 2-4 illustrates that the proposed structure has lower leakage current than that of the conventional BCE Structure A device at Vd=10V under the illumination of 6000 nits. Meanwhile, the devices were operated with drain bias of 10V at saturation region (V_D>Vgs-VT) since the photo-induced leakage current would be enhanced by the high drain bias.

The electrical characteristic of the inverter-staggered a-Si:H TFT suffers from the parasitic resistance.[2.17-2.18] The parasitic resistance is dependent on several factors, for instance, the thickness of a-Si:H, sheet resistance of n+ a-Si layer, and source/drain contact quality. For a constant W/L ratio, the effect of parasitic resistance can be clearly observed in the output characteristics of a-Si:H TFTs. The large parasitic resistance would result in the current crowding effect. A comparison of output characteristics (I_D-V_D) for the new TFT and the conventional TFTs under nominal W/L ratio is shown in Fig. 2-5. The current crowding is found in the

conventional inverter-staggered TFT, not observed in the proposed TFT device. The significant difference in device structure is an n^+ a-Si contact formed at the sidewall of a-Si:H island (a-Si:H/n+a-Si) in the proposed TFT, as shown in Fig. 2-1(c). To investigate the difference of electrical characteristics between Structures A and C, the parasitic resistances of TFT devices were extracted. Under the operation of small drain voltages V_D and high gate voltages V_G, it is assumed that the turn-on resistance R_{on} of TFT device consists of the channel resistance R_{ch} and the parasitic source/drain resistance R_p.

$$R_{on} = R_{ch} + R_p \text{, and } R_{ch} = \frac{L}{W\mu C_i (V_G - V_T)}$$

where C_i is the gate nitride capacitance per unit area and W, L, and V_t are the intrinsic device channel width, length, and the threshold voltage, respectively.[2.17] The parasitic resistance R_P of a-Si:H TFT can be extracted through measuring the ON resistance R_{on} from the linear region of TFT output characteristics and through plotting the $R_{on}W$ against the channel length L.[2.17-2.20] Figure 2-6 illustrates the typical gate voltage dependence of the parasitic resistance R_p of Structures A and Structure C, comparatively. The R_p value of the proposed TFT is significantly lower than that of the conventional one. Moreover, the R_p of the conventional inverter-staggered TFT is strongly dependent on the gate voltages. The value of R_p decreases from 6.6 MΩ to 2.2 MΩ, when the gate voltage increases from 6V to 12V. By contrast, the gate-voltage dependence of the R_p of the proposed TFT is weaker and just decreases from 1.2 MΩ to 0.5 MΩ. In the proposed TFT device, the lack of an intrinsic a-Si:H layer between channel and source/drain contacts can reduce such nonlinear effects, as similar to the space charge-limited conduction (SCLC).[2.19-2.20] The SCLC occurred in intrinsic a-Si:H region is influenced seriously by both the drain and gate voltages. Also, the simulation results indicate that

the carriers can be transported form the channel to the n^+ layer at the sidewall of a-Si:H island and are quite different from those having an intrinsic layer between n^+ a-Si layer and the channel.

Figures 2-7 and 2-8 illustrate the distributions of electrons near the drain region in the corresponding structures A and C. The arrow heads labeled in the two figures present the carrier transport directions. In the proposed structure, the electrons can transport though contacts, the side wall and the top contact of drain metal overlap region. By the contrary, the conventional inverted staggered TFT owns one path for transporting, from the bottom accumulation layer of the a-Si:H layer to the top contact of metal. Hence, the lower parasitic resistance of the proposed TFT results in relatively high mobility and low threshold voltage.

Application of a-Si:H TFT on AMOLED is really attractive due to its low cost of a-Si:H TFT processing. TFT is used as a controller to determine the driving current of OLED. However, the stability of a-Si:H TFT is the key concern for the realization of amorphous silicon AMOLED technology. With increasing the operation duration of a-Si:H TFT, the conduction current of a-Si:H TFT is decreased gradually. The interface state creation at a-Si/gate dielectric interface and charges trapped at the gate dielectrics are usually responsible for the degradations of a-Si:H TFT. Figure 2-9 shows the evolution of conducting currents in TFTs during bias temperature stressing (BTS) at 60^oC. The current of 200nA was conducted on two devices with the same W/L ratio. The gate bias of Structure A and C was 11.25V and 9V, respectively. The proposed TFT exhibits the better ability against the DC current stressing. Figure 2-10 shows the I_D-V_G relationship of both TFTs after bias temperature stress. A significant threshold voltage shift of 1.75V was found in the conventional TFT after the stress, while the shift amount of the threshold voltage for the proposed TFT is as low as 0.75V. Since the proposed TFT owns superior driving capability, it could conduct the

same magnitude of current at the lower V_{GS} than the conventional one. Thus, the gate dielectric in the proposed TFT is under lower perpendicular electric field across the gate dielectric, so the amount of trapped charges in the dielectric are decreased. The electrical stability of a-Si: H TFT is therefore improved.

2.4 Conclusions

A novel technology for manufacturing high-performance hydrogenated amorphous silicon (a-Si:H) TFT is developed in this chapter. In the bottom gate light-shield a-Si:H TFT structure, the side edge of a-Si:H island is capped with an extra deposition of heavily phosphorous-doped a-Si layer. Such an ingenuity can effectively eliminate the leakage path between the parasitic contacts between source/drain metal and a-Si:H at the edge of a-Si:H island. In addition, our proposed a-Si:H TFT device exhibits superior effective carrier mobility, as high as 1.05 cm^2/Vsec due to the enormous improvement in parasitic resistance. We have evidenced that the leakage current of proposed TFT is lower than the conventional BCE device under bottom-side illumination of 6000 nits. It also exhibits the better ability against the DC current stressing. The impressively high performance provides the potential of the proposed a-Si:H TFT to apply for AMLCD and AMOLED technology.

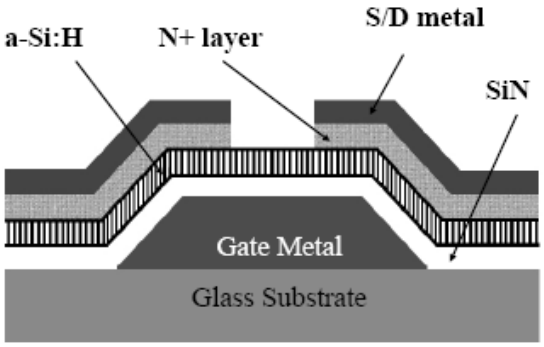

Fig 2-1(a)

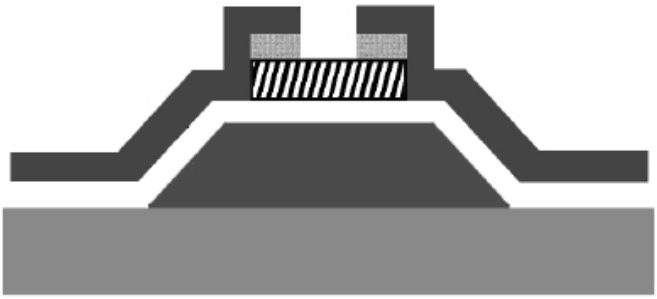

Fig2-1(b)

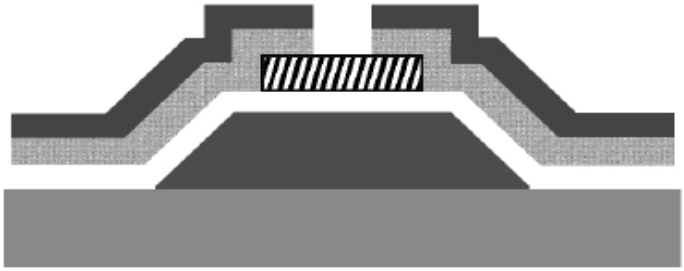

Fig. 2-1(c)

Fig. 2-1 (a) Conventional inverted-staggered a-Si:H TFT (Structure A). (b) Akiyama's light-shield a-Si:H TFT (Structure B) (c) The new structure a-Si:H TFT (Structure C)

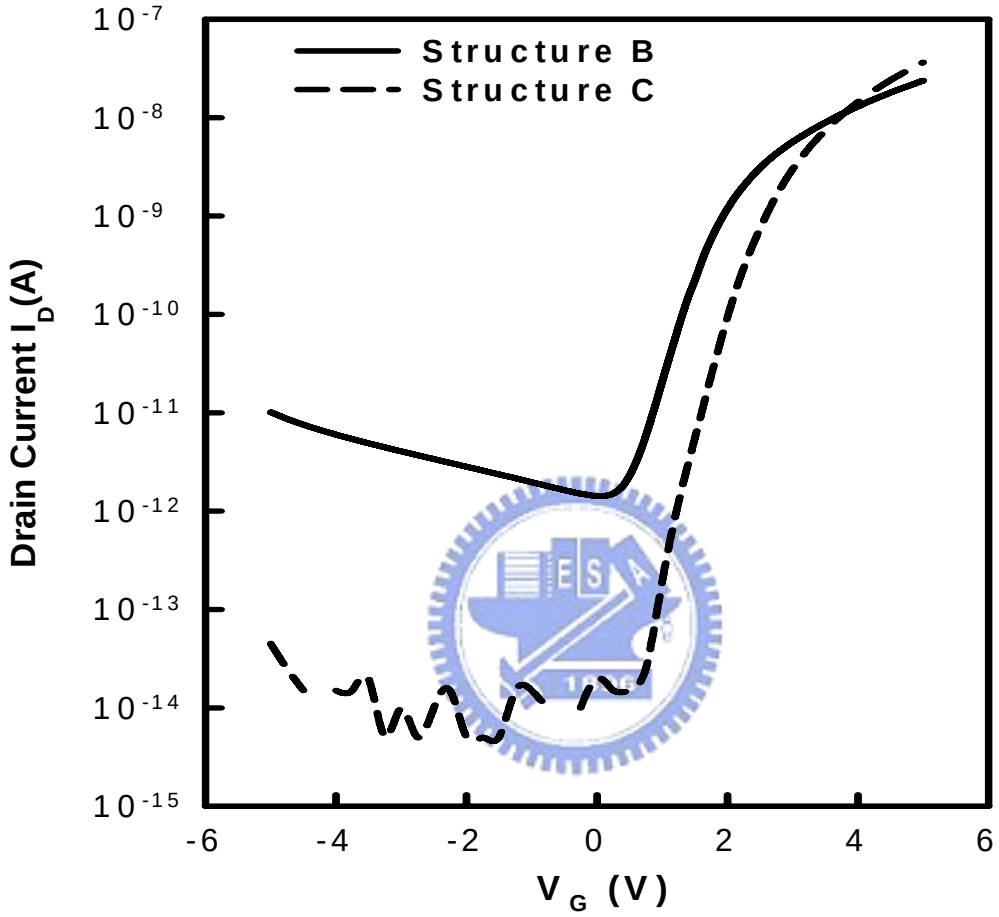

Fig. 2-2 I_D-V_G transfer characteristics of TFTs, Structures B and C with the same W / L ratio at V_D=0.1V. The leakage current of Structure C is effectively suppressed in the proposed TFT structure

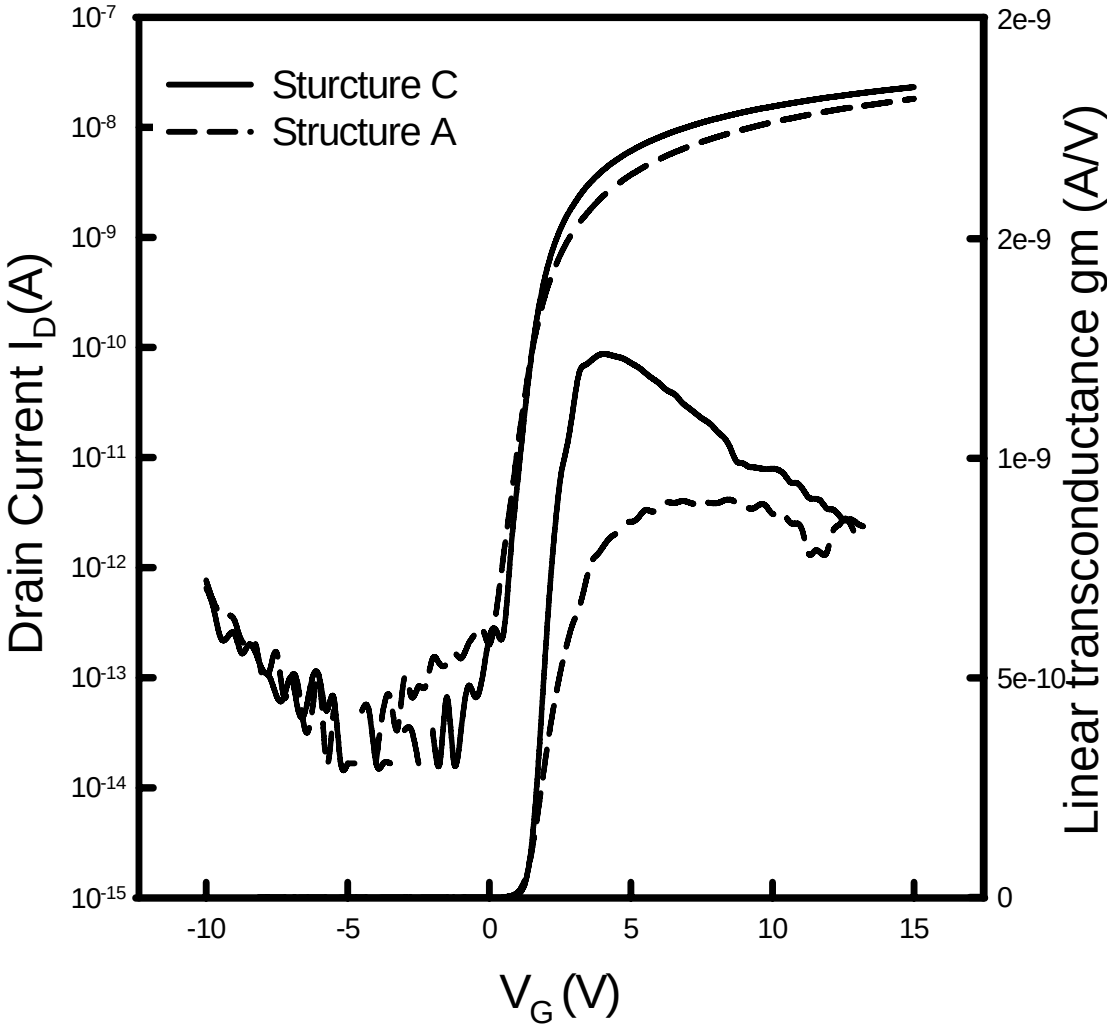

Fig. 2-3 I_D-V_G transfer characteristics and linear transconductances (*gm*) of TFTs, Structure A and C with the same W / L ratio. The superior current driving capability of the proposed TFT is demonstrated.

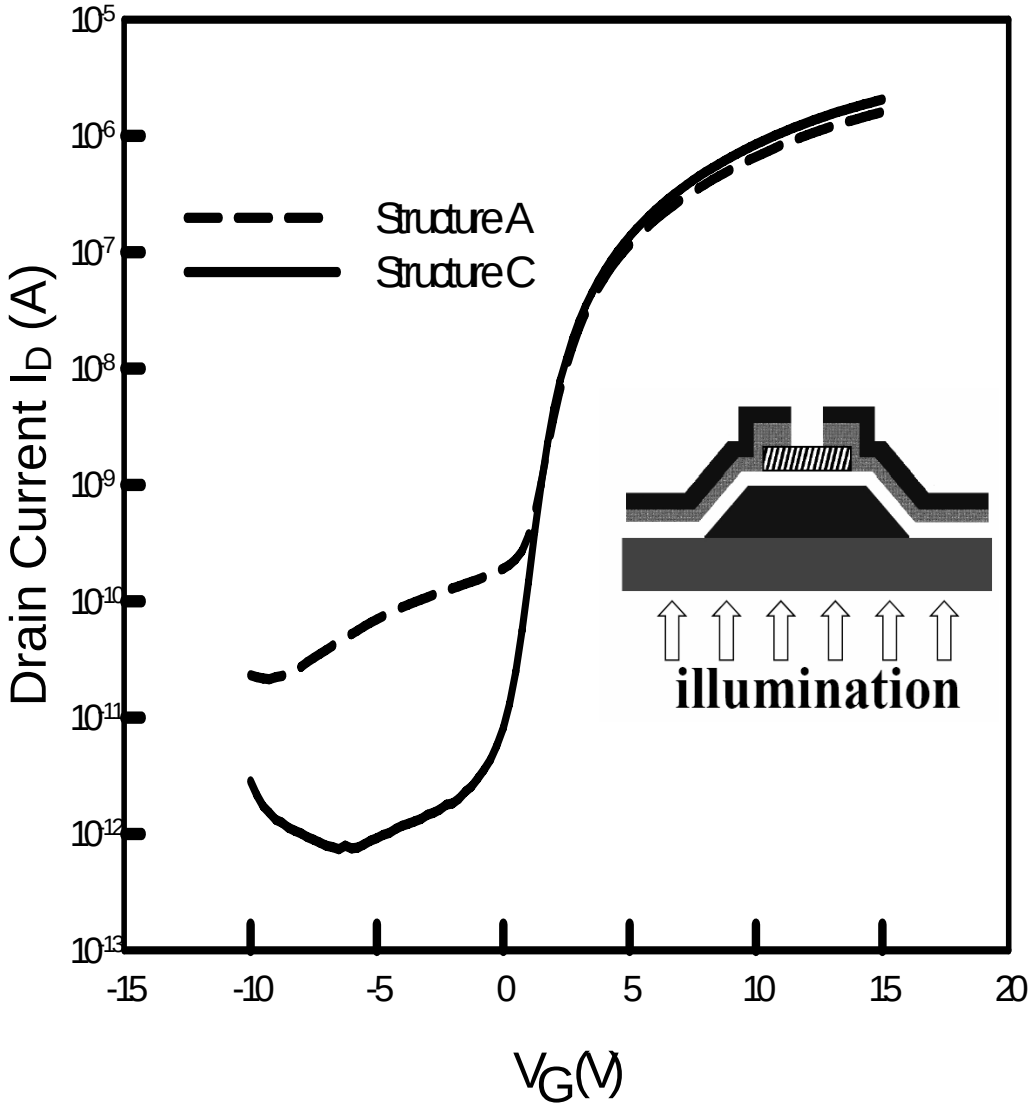

Fig. 2-4 Comparison of I_D-V_G relations of Structures A and C at V_D=10V under the white-light illumination of 6000 nits. The inset sketches the illumination from the bottom-side of the TFTs.

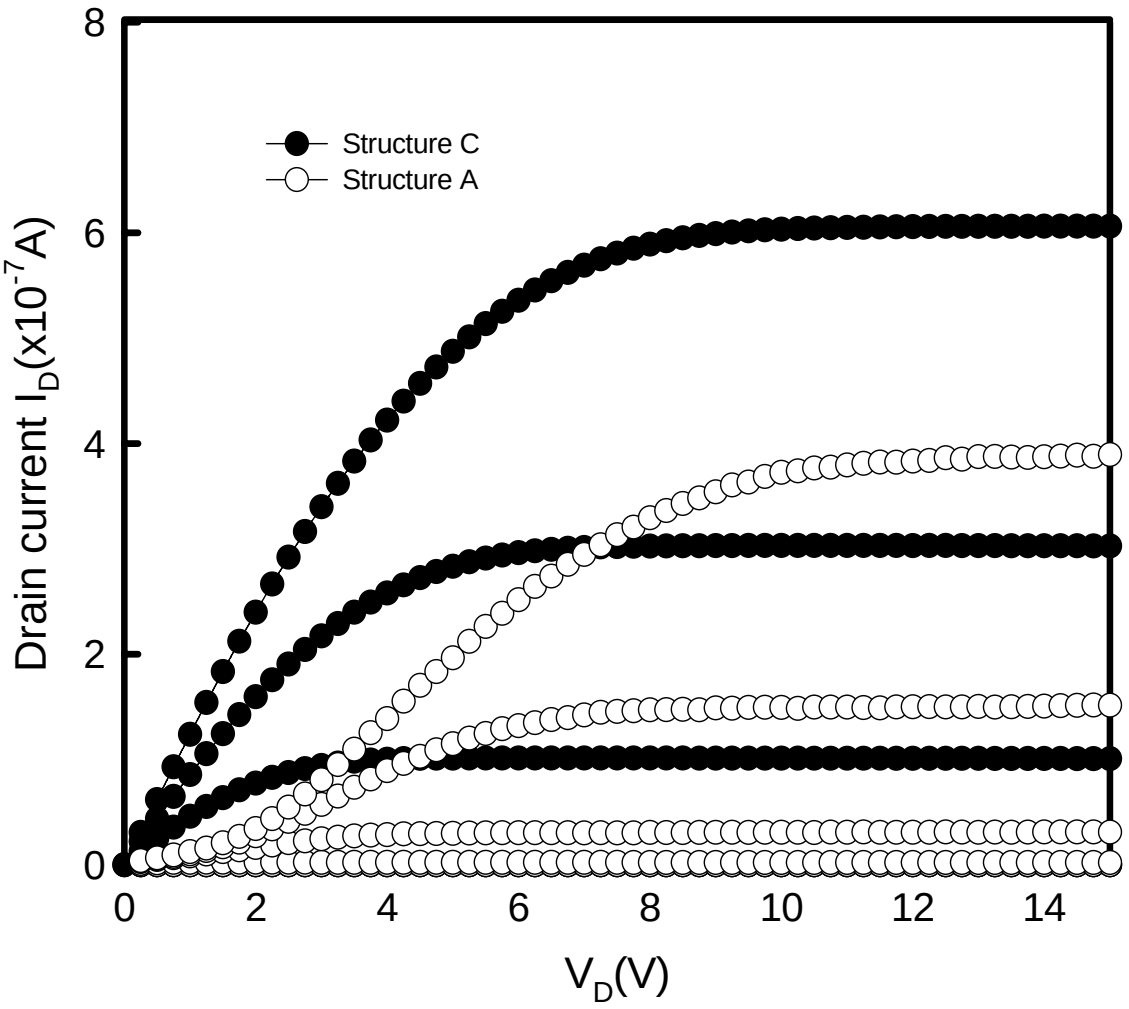

Fig. 2-5 A comparison of output characteristics (I_D-V_D) for the proposed TFT and the conventional inverter-staggered TFT. The current crowding is found in the conventional inverter-staggered TFT, Structure A.

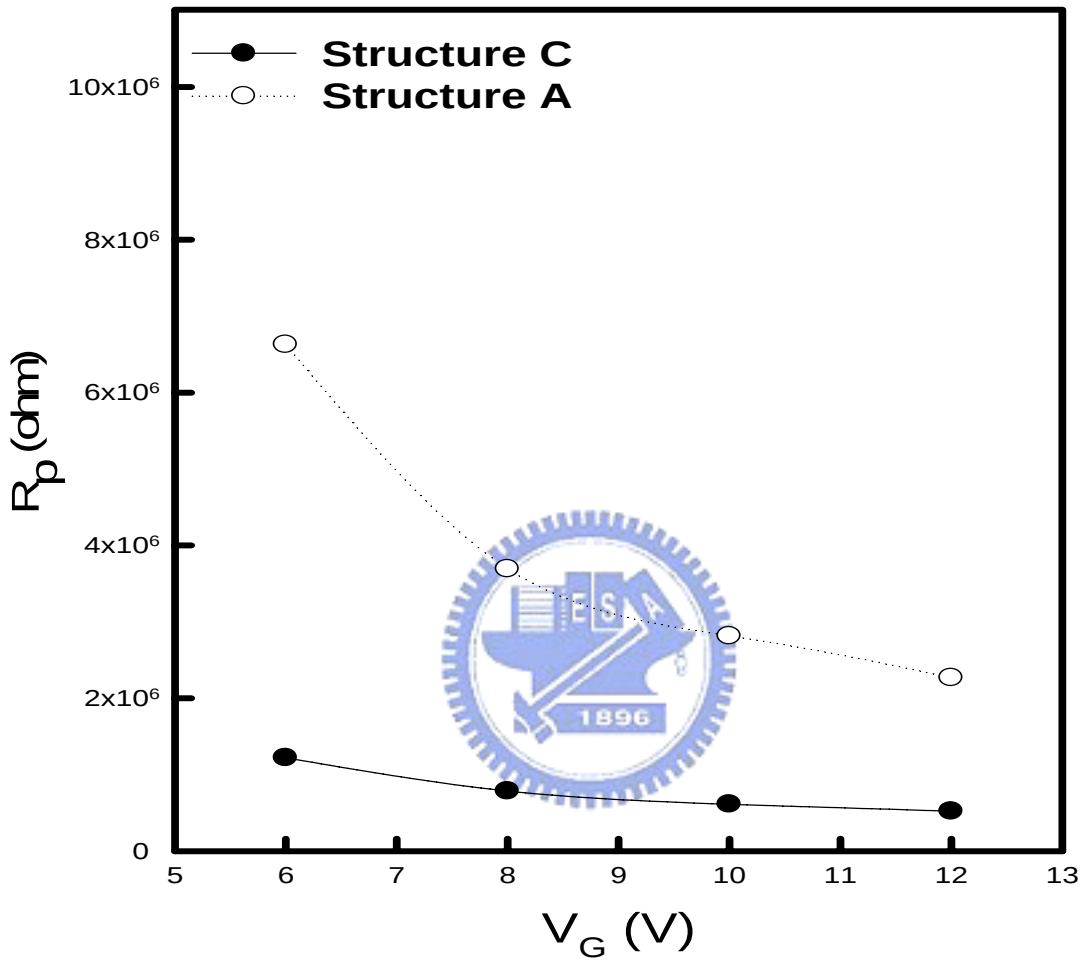

Fig. 2-6 The gate voltage dependence of the parasitic resistance R_p of Structures A and Structure C.

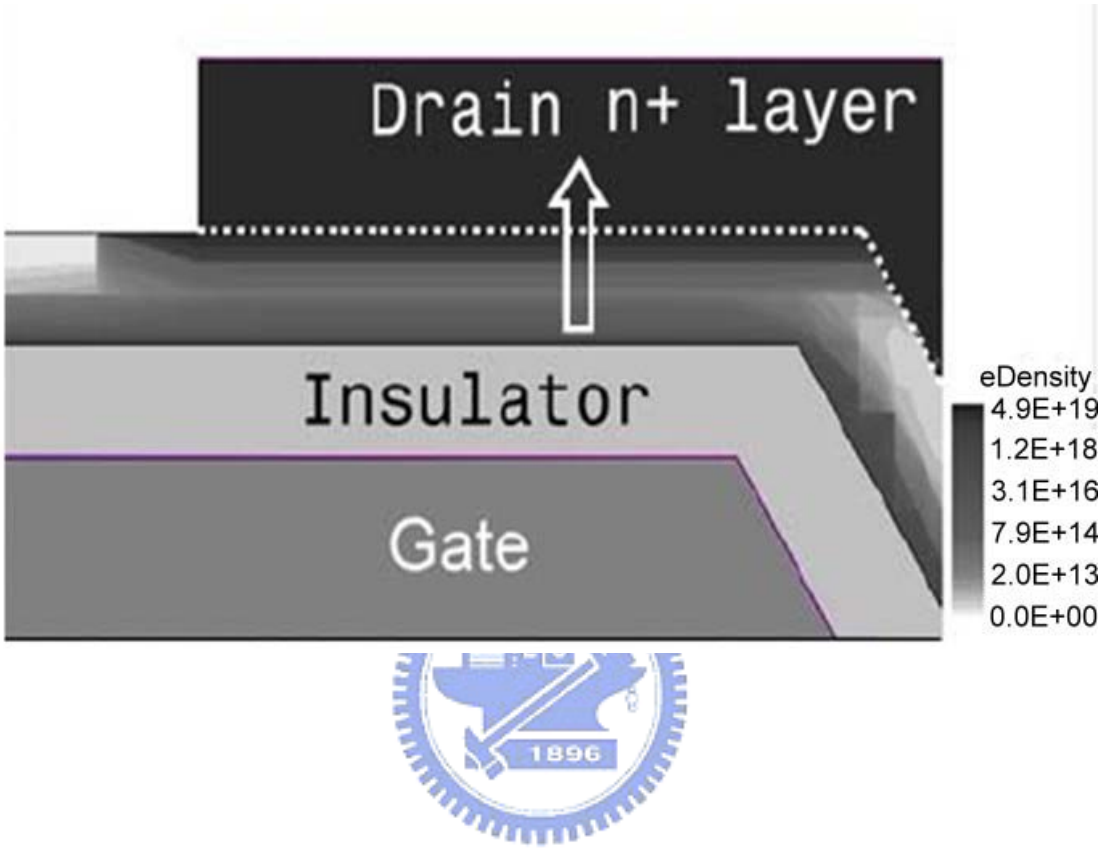

Fig. 2-7 The distribution of electrons near the drain region in the structures A. The arrow heads labeled in the two figures present the carrier transport directions.

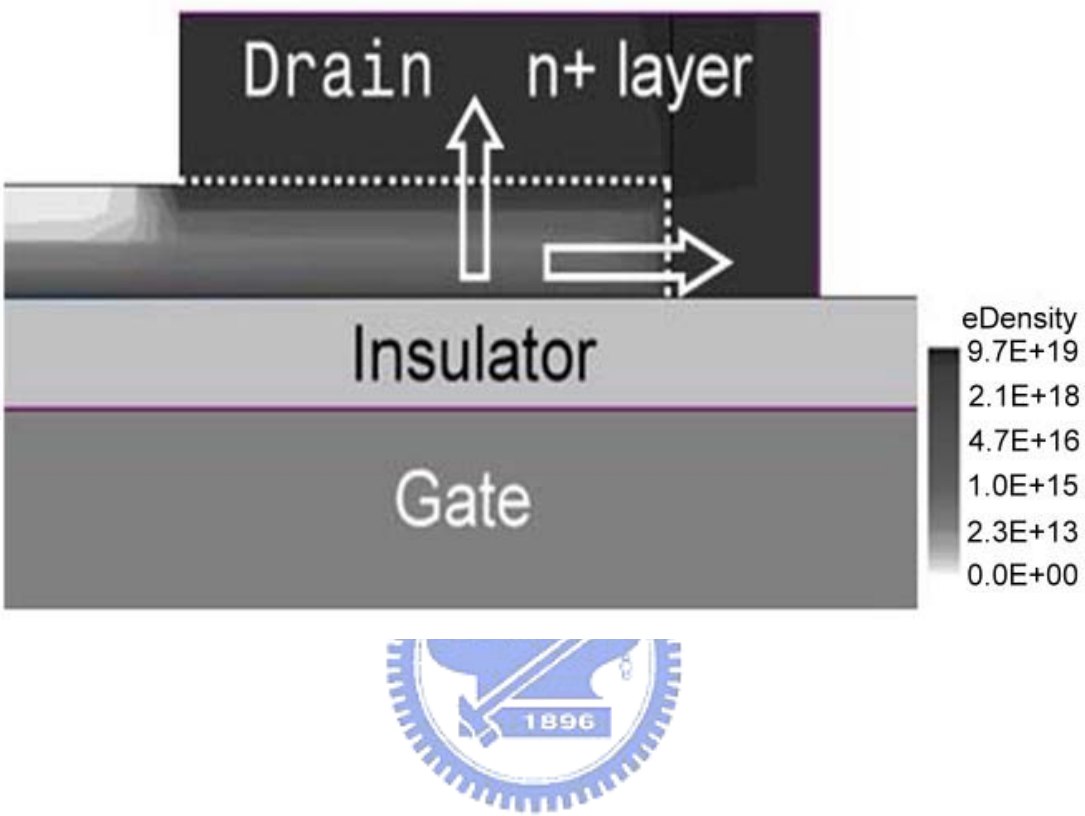

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Fig. 2-8 The distribution of electrons near the drain region in the structures C. In the proposed structure, the electrons can transport though contacts, the side wall and the top contact of drain metal overlap region.

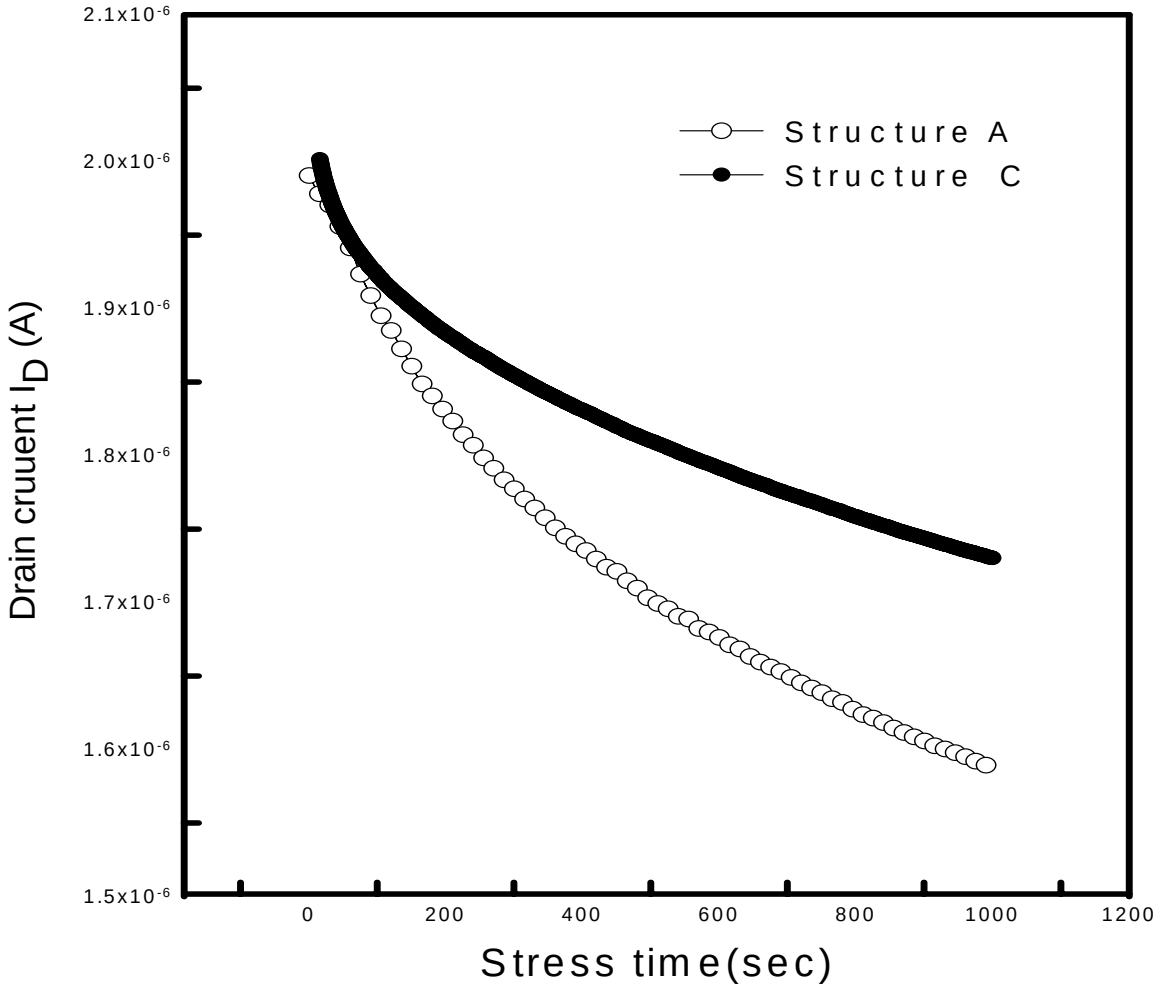


Fig. 2-9 The evolution of conducting currents in TFTs during bias temperature stressing (BTS). The current of 200nA was conducted on Structure A and C at 60^{o}C with the gate bias of 11.25 V and 9V, respectively.

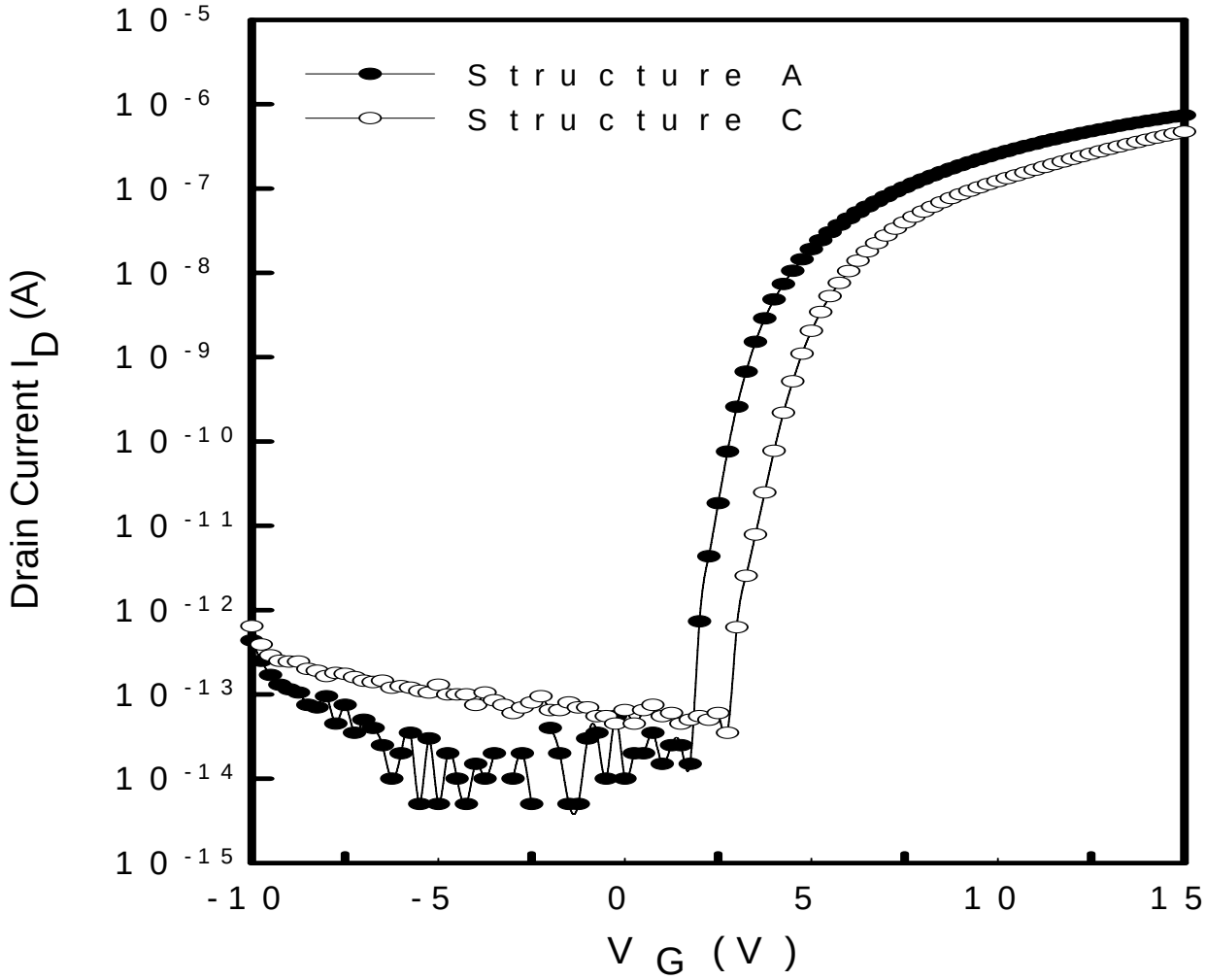


Fig. 2-10 The I_D-V_G relationships of the TFTs after bias temperature stress. The threshold voltage shift of structure A and C is 1.75V and 0.75V, respectively.

Chapter 3

Investigation of Poly-Silicon Thin Film Transistors with/without LDD Structure at Temperatures and under AC stress

3.1 Introduction

Poly-Silicon Thin film transistors (Poly-Si TFTs) have been wily applied on the flat-panel displays like AMLCD and AMOLED. The major advantages of poly-Si TFTs are the higher driving capability than the amorphous silicon devices, and the existence of complementary devices.[3.1-3.5] Taking advantage of these features, poly-Si TFTs can be used to incorporate the integrated peripheral driving circuitry and switching transistor in the same substrate for flat-panel displays.[3.6-3.7] The integration of driver circuits would reduce the assembly complication and cost dramatically. If the mobility of poly-Si TFTs is further increased, this poly-Si technology will realize the system on panel (SOP) which will integrate memory, CPU, and display.[3.8-3.9] TFT devices in functional circuits serve as the switches and suffer the high frequency voltage pulses. Previous research reports have shown a relationship between the creation of states and hot-carriers effect by performing DC stress.[3.10-3.13] The degradation mechanism of n-channel TFT under dynamic voltage stress, however, has not been clarified yet.[3.14-3.16] The degraded TFT will seriously influence the operation of the circuits.

In addition, the dangling bonds in the grain boundaries in the poly-Si film serve as the trapping centers that play a cruel role for the electrical performance of poly-Si TFT. [3.17-3.18] These defect states in energy band gap would enhance the carrier to tunnel at the high field.[3.19-3.20] Therefore, the leakage current due to trap-assisted

tunneling effect is much larger in poly-Si TFTs than in the single crystal MOSFETs. Trap-assisted tunneling effect is known to be strongly dependent on the electrical field. In order to reduce the horizontal electric field around a drain, the lightly doped drain (LDD) structure is widely used for poly-Si TFTs. Some reports have demonstrated that the light-drain doping (LDD) technology can effectively reduce the electric field at the drain region and suppress the leakage current. [3.21-3.22] It also can keep down the kink effect resulted from the impact-ionization of energetic carriers which usually leads to the undesirable effect in electrical characteristics of TFT. The LDD-structure, hence, is necessary for the application of poly-Si TFT, especially for the N-channel TFTs.

Moreover, the large area electronics or the flat-panel displays comprised of poly-Si TFTs are used by peoples at the globe. Thus, the displays should keep the performances well at all kinds of the environments. Temperature usually influences the characteristics of solid-devices, and its relative effects are important for the application of Poly-Si TFT technology. In this chapter, the temperature effects on the n-type poly-Si TFT with/without LDD structure was firstly investigated. Then we observed the AC stress effects on n-channel poly-Si TFTs without LDD to clarify the degradation mechanism.

3.2 Temperature Effects on Poly-Si TFTs

3.2.1 Device Fabrication

Top-gate structured poly-Si TFTs were fabricated on glass substrate by low-temperature processes. Buffer SiO_2 films and 90nm-thick amorphous silicon films were deposited by plasma enhanced chemical vapor deposition (PECVD), and

subsequently, the films were dehydrogenated by furnace annealing. After dehydrogenation, the a-Si films were crystallized by XeCl excimer-laser. [3.23-3.24] The power of the line-shaped beam was 350 mJ/cm^2. Following the laser process, 100nm-thick gate oxide was deposited by PECVD. Then the implantation was adapted to define the LDD region and S/D region. The LDD and S/D region was doped by phosphorous of 1 x 10^{13} atom/cm^2 and 8 x 10^{14} cm^3, respectively. Then MoW was sputtered as a gate metal. The LDD/gate overlap region is 0.75 μm and LDD extends outside the gate 0.75 μm. The dimension of the non-LDD TFTs in this section was W=12μm and L=6μm, the overlap of gate metal and S/D junction is 1μm. The cross section views of TFTs were illustrated in Figs. 3-1(a) and 1(b).

3.2.2 Results & Discussions

Figure 3-2(a) shows the I_D-V_G relations and transconductance, gm, of poly-Si TFT at the temperatures from 50K to 250K. Figure 3-2(b) shows I_D-V_G relations in the linear scale. The conducting current of STD TFT is significantly increased with the decreasing of the temperature. The ON-current of TFT at 250K is 0.825 times that at the 50K. Moreover, the threshold voltage of the TFTs varied from 1.6V to 0.8V, extracted at current density of 10 nA with normalized channel width (W)/channel length (L) ratio. In figures 3-2(b), the maximum value of gm is also raised with the decreasing in temperature. The mobility extracted from the maximum value of gm is 135.8 cm^2/Vs and 106.5 cm^2/Vs at 50K and 250K, respectively. This phenomenon can be explained by the evolutions of the carrier scattering in poly-Si TFT at temperatures. Some reports have shown that the carriers in the MOSFET made on mono-crystalline silicon wafer suffer three types of scatterings, including impurity scattering, surface scattering and the phonon scattering, as shown in Fig. 3-3. [3.25] The phonon

scattering is due to the lattice vibrations and strongly dependent on the temperature. The carrier transport of poly-Si TFT is evidenced to be mainly limited by the grain boundaries in the poly-Si film.[3.26] However, the field effective mobility of carriers should be affected by the phonon scattering within the same boundaries in channel region. At high temperature, the carrier is seriously scattered by the numerous phonon. Accordingly, the effective mobility of carrier is lower at high temperature than that at low temperature. Unlike the MOSFET, the ELA poly-TFT owns lots of grain boundaries in the channel region. Thus, both the grain boundaries and phonons would deeply affect the carrier transport in the poly-Si TFT.

Figure 3-4 illustrates the I_D-V_G relations of LDD-TFT at the temperatures from 50K to 250K. Unlike the non-LDD TFT, the conducting current of LDD TFT is decreased with the decreasing of the temperature. The dominant mechanism in conducting capability of LDD TFT at the low temperature should be different from the non-LDD TFT. To clarify the difference between two devices, the sheet resistances of phosphorous heavily-doped and lightly-doped poly-Si film are measured from 50K to 250K, demonstrated in Figs. 3-5 (a) and (b). It's apparent that the resistivity of heavily-doped film almost keep well as the temperature changed. However, the LDD layer behaves as a temperature-dependent resistor which is a lager resistance at low temperature than at high temperature. The sheet resistivity of LDD at 50K is 4.72 times that at 300K. Since the LDD poly-Si sheet does not achieve the degeneracy doping level, the freeze effect of doped impurity atoms was observed. In addition, the traps of grain boundary play an important role for the conductivity of the poly-Si film. According to the Seto's model, the electrons activated from the doped atoms, Phosphorous, were filled at the trap states at the grain boundaries. For simplify, the amount of free carrier in LDD layers, N_{free}, can be equated to:

$$N_{free} = N_D^{+} - N_T \quad (1),$$

where N_D^{+} is the number of ionized impurities and N_T is the effective trap density. Thus, the conductivity of poly-Si film is proportional to the amount of free carriers. With the decreasing of the temperature, the amounts of activated electrons are decreasing and the ratio of trapped electrons is rising by assuming that the amount of trap states is non-varied. The few free electrons are contributed to the conduction, and thus the conductivity is decayed at low temperature. In heavily-doped poly-Si sheet, the amount of doped atoms is much larger than the trap density. Thus, the amount of activated electrons is much larger than the trap density in heavily-doped poly-Si sheet since the high doping level would lead to the degeneracy. Seto has shown that the resistivity of boron doped poly-Si film as a function of the doping level. At high doping level (Nd>>Nt), resistivity of poly-Si tends to approach the mono-crystalline one while the poly-Si may be degeneracy. Thus, heavily-doped poly-Si sheet exhibits the temperature-independent conducting behavior.

Figure 3-6 schemes that LDD layers extended out the gate overlap region behave as the temperature-dependent resistors and series connecting with the gate control region. Although the conductivity of channel region is reversion to the temperature, the LDD sheets extended outside the gate electrode behave as the large resistors and limit the drain current.

3.3 Electrical Degradation Mechanism of N-Channel Poly-Si TFT under AC Stress

3.3.1 Device Fabrication

Similar to the 3.2.1 section, the N-channel poly-Si TFT with top-gate structure were

fabricated on a glass substrate without lightly doped drain (LDD). The dimensions of TFTs in this work were L=9μm, W=6μm and the overlap of gate metal and S/D junction is 1μm. The cross section views of TFTs were illustrated in Fig. 3-7. The stress pulses were performed on the gate electrode as the dynamic stress and source/drain were grounded, as shown in the inset of Fig. 3-7. As for the stress condition, we used the rectangular pulse with amplifier of ±15V and frequency of 500kHz. Both the rising time (Tr) and falling time (Tf) were 100 ns.

3.3.2 **Results and Discussions**

Figure 3-8 shows the I_D-V_G relationships of n-channel poly-Si TFT (L=9μm) with the dynamic stress times for 10 to 1000 s. The distinct decrease in on-current was found with the increasing stress duration. With the stress duration for 10 and 100 s, respectively, the conducting current of TFT operated at Vg=15V is 90% and 39% times of the magnitude of the initial value. After stressing for 1000 s, the on-current of TFT is degraded to 3% of the magnitude of the initial value. However, both the sub-threshold swing (0.28 V/dec.) and threshold voltage (2.41V) kept well during the stressing. From the evolution of the transfer characteristics at the linear operation region with stress time, it is apparent that the impact of the applied stress leads to a parallel decrease of the on-current operated at the above threshold region of the I_D-V_G characteristics. In poly-Si TFTs, the degradation under DC stress is usually characterized by a decrease of the sub-threshold slope mainly due to the generation of traps at deep states in poly-Si grains and a threshold voltage shift caused by charge trapping in the gate oxide and at the interface states. However, the experimental data showed that both subthreshold slope and threshold voltage remain unchanged in all stressed devices in comparison with the non-stressed device. This indicates that the

degradation of the n-channel poly-Si TFTs is neither occurred by charge trapping in the gate oxide nor by the creation of traps at the deep states. We can infer that the tail states produced by the strained bounding in poly-Si film are responsible for the electrical degradation of TFT.

The I_D-V_D characteristics of TFT with the dynamic stress times are illustrated in Fig. 3-9. It is observed that the current crowding effect on TFT is significantly enlarged with the increase of stress time. Figure 3-9 also indicates parasitic resistance is contributed to the degradation on electrical properties of TFT. The parasitic resistance is dependent on the following several factors, such as the trap states near the source/drain junctions, sheet resistance of n+ poly-Si layer, and source/drain contact quality. For a constant W/L ratio, the effect of parasitic resistance can be clearly seen in the output characteristics of TFTs. The large parasitic resistance would result in the current crowding effect, as shown in Fig. 3-9.

Under the operation of small drain voltages V_D and high gate voltages V_G, it can be assumed that the turn-on resistance R_{on} of TFT device consists of the channel resistance R_{ch} and the parasitic source/drain resistance R_p.

$$R_{on} = R_{ch}+R_p, \text{ and } R_{ch} = \frac{L}{W\mu C_i(V_G - V_T)} \quad (1)$$

where C_i is the gate oxdie capacitance per unit area and W, L, and V_t are the intrinsic device channel width, length, and the threshold voltage, respectively. The parasitic resistance R_P of TFT can be extracted through measuring the ON resistance R_{on} from the linear region of TFT output characteristics and through plotting the $R_{on}W$ against the channel length L. To extract the R_P, we performed the dynamic stresses on the lengths of TFT for 3 μm, 6 μm, 9 μm, 10 μm, 12 μm and 30 μm with the same stress conditions. The degradation phenomena of stressed TFTs are similar to the Figs. 3-8 and 3-9. Figure 3-10 illustrates the typical gate voltage dependence of the

parasitic resistance R_p of TFT with various stressing times, respectively. The R_p value of the un-stressed TFT is significantly lower than that of the stressed ones. Moreover, the R_p of the TFT with 1000 seconds AC stress is strongly dependent on the gate voltages. The value of R_p decreases from 6.29 to 0.80MΩ, when the gate voltage increases from 18V to 30V. By contrast, the gate-voltage dependence of the R_p on un-stressed TFT is weaker and just decreases from 0.14 to 0.12 MΩ.

Since the electrical properties of poly-Si TFT are strongly influenced by the traps in the poly-Si film, the statuses of trap states in both samples should be illustrated. Seto has demonstrated the conduction mechanism of poly film which associates the carrier transport with the trap states. This model showed that carrier trapped in the traps at grain boundary leads to form a potential barrier height. In Seto's model, the dependence of gate bias and trap density on drain current is shown as the following equation,

$$I_D = \left(\frac{W}{L}\right) C_{OX}\left(V_G - V_{FB}\right) V_D \mu_{EF} \exp\left(\frac{-q^2 N_t^2 t_{OX}}{\sqrt{\varepsilon_{Si}\varepsilon_{SiO_2}}\, C_{OX}\left(V_G - V_{FB}\right)^2}\right) \quad (2)$$

where V_{fb} is the flat band voltage of the device, and ε_{Si} and ε_{SiO2} are the dielectric constant for silicon and gate oxide, respectively. C_{OX} and t_{OX} and are the gate oxide capacitance and thickness, respectively. Accordingly, the effective trap state density can be obtained from the slope of the curve $ln[I_D/(V_G\text{-}V_{FB})]$ versus $(V_G\text{-}V_{FB})^{-2}$. Figure 3-11 shows the effective trap state density (N_t), extracted from the *Eqn.* 2 for TFTs after stresses. A larger slope indicates a larger effective trap state density. The effective trap density of TFT is 1.42×10^{12} cm^{-2} before the stress, while the N_t of stressed TFT are 2.42×10^{12} cm^{-2} and 3.14×10^{12} cm^{-2} for 100 s and 1000 s stressing, respectively. The stressed device owns 2.21 times of the magnitude of the N_t for the un-stressed TFT. According to the Figs. 3-8 and 3-9, we believe that the creation of tail states is responsible for the distinct raise of parasitic resistance and the

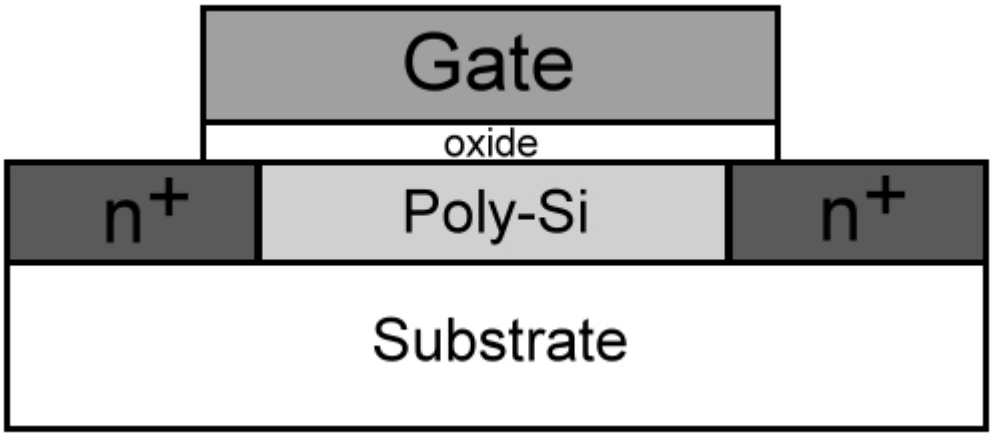
degradation on conducting current. According to the trap density of poly-Si sheet, the whole channel of TFT can be divided into three regions, including damaged source region, intrinsic region, and damaged drain region. The two damaged regions near the source/drain mainly limit the conductivity of TFT. The trap states extracted from the I_D-V_G curves according to Seto's model are principally contributed by the damaged regions.

To clarify the location of damaged regions in the TFT after AC stress, electrical analysis using higher drain voltage was performed. Figure 3-12 shows the I_D-V_G relations with the drain bias of 8V after 1000 s stress. The ON-current at saturation region (V_D=8) is 51% of the magnitude of the initial value which is much better than that at linear region (3%) after 1000 s stress. For the TFT operated at saturation regime ($V_{DS} > V_{GS}-V_T$), the pinch off region will appear near the drain and the depletion region increasingly expands toward to the source with the increasing of the drain voltage. Carriers are swept into the drain by the electrical field when they enter the pinch-off region. It should be noted that the carriers moving into pinch-off region are no longer confined to the inversion layer near the surface, but begin to move away the surface into the bulk. Carriers tend to repel the high-resistivity damaged region at the oxide/poly-Si interface near the drain, as shown in the inset of Fig. 3-12. As a result, the parasitic resistance resulted from the stressing at the drain side is absent under the saturation operation, since the current has already spread out to the bulk in the pinch-off portion of the channel. Thus, the impact of parasitic resistance on the drain becomes weaker. The measured I_D-V_G relations are still similar, while the source and drain side of TFT device are exchanged. This phenomenon verifies that the damaged regions were mainly located near the source/drain regions after AC stress.

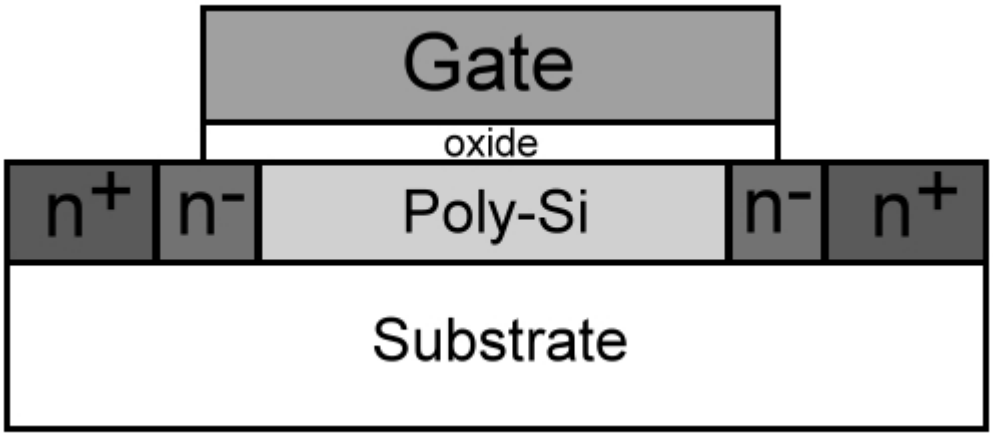
3.4 Conclusions

The temperature and AC stress effects on ELA poly-Si TFT have been demonstrated in this chapter. We find that the conducting current of non-LDD poly-Si TFT is increasing with the decreasing in the temperatures. The phonon scattering is responsible for the evolution of carrier mobility in poly-Si TFT at temperatures. However, the LDD poly-Si TFT is mainly dominated by the LDD layers extended outside the gate electrode. LDD sheet works as a larger resistor at low temperature than that at high temperature. These results can provide the designers to consider the temperature effects for the poly-Si TFT application in a suitable temperature range.

In addition, the distinct decrease in ON-current of n-channel poly-Si TFT was found during the dynamic voltage stress. In spite of electrical degradation appearing at the ON-current of the poly-Si TFT, both the sub-threshold swing and threshold voltage kept in a good condition. This can be inferred that the tail states were produced in ploy-Si film due to the AC stress. Additionally, the current crowding effect was increased with the increasing of stress time. The parasitic resistances extracted from the I_D-V_D curves of poly-Si TFTs were significantly increased after the 1000 s stressing. The effective trap density of poly-Si TFTs stressed for 1000 s was 3.14×10^{12} cm^{-2}, 2.21 times larger than that of the un-stress device. The creation of effective trap density in tail-states is responsible for the raise of the parasitic resistance and the degradation in ON-current of TFT. Moreover, the damaged regions which contain numerous trap states are evidenced to be mainly near the source /drain regions.

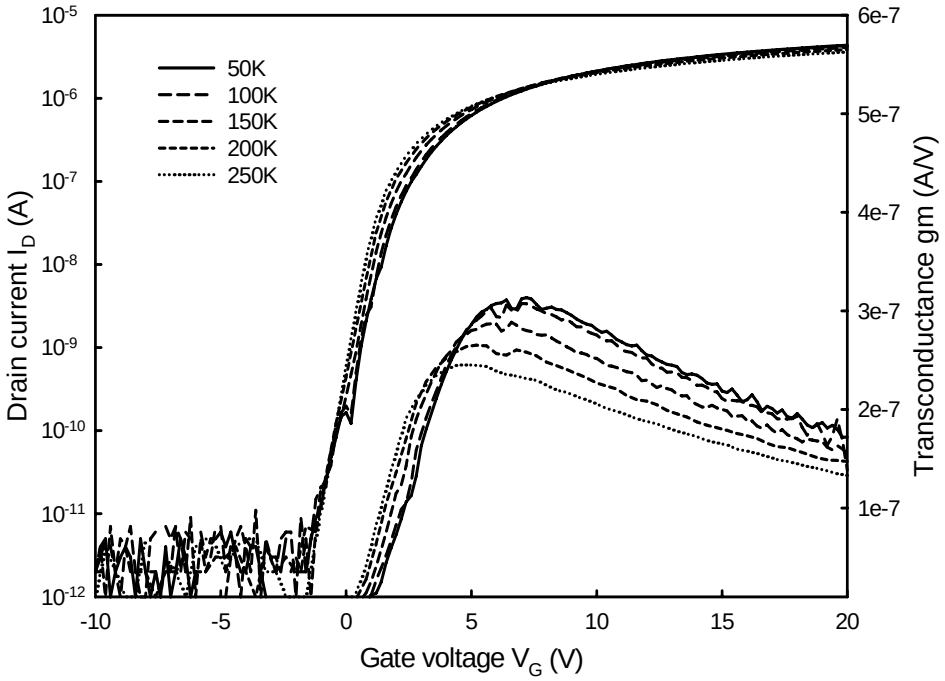


(a)

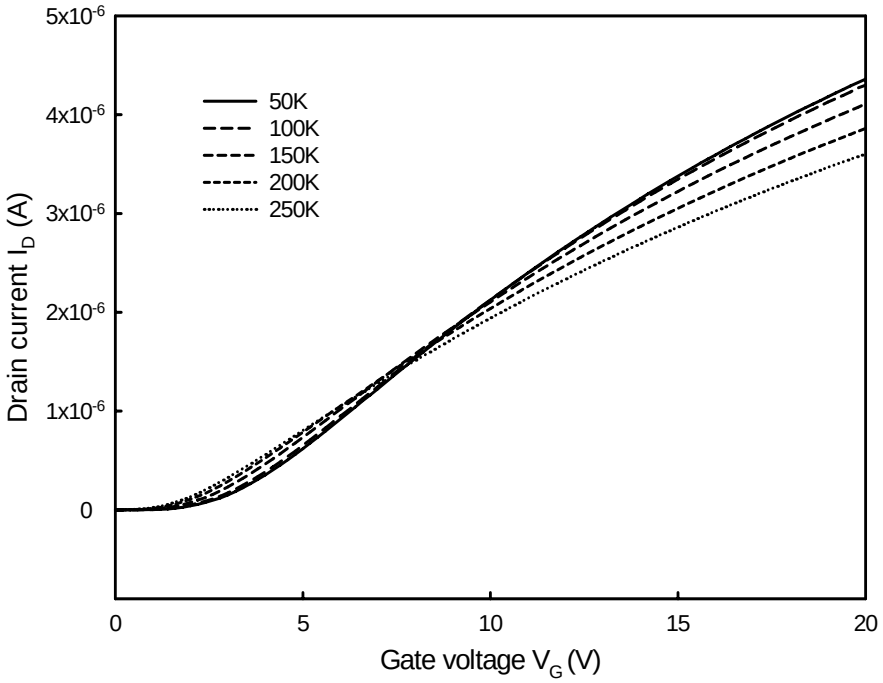


(b)

Fig. 3-1 The cross section view of the TFTs in this work. (a)non-LDD TFT (b)LDD TFT



(a)



(b)

Fig. 3-2 (a)The I_D-V_G relations and transconductance, gm, of poly-Si TFT at the temperatures from 50K to 250K. (b) drain current in linear scale.

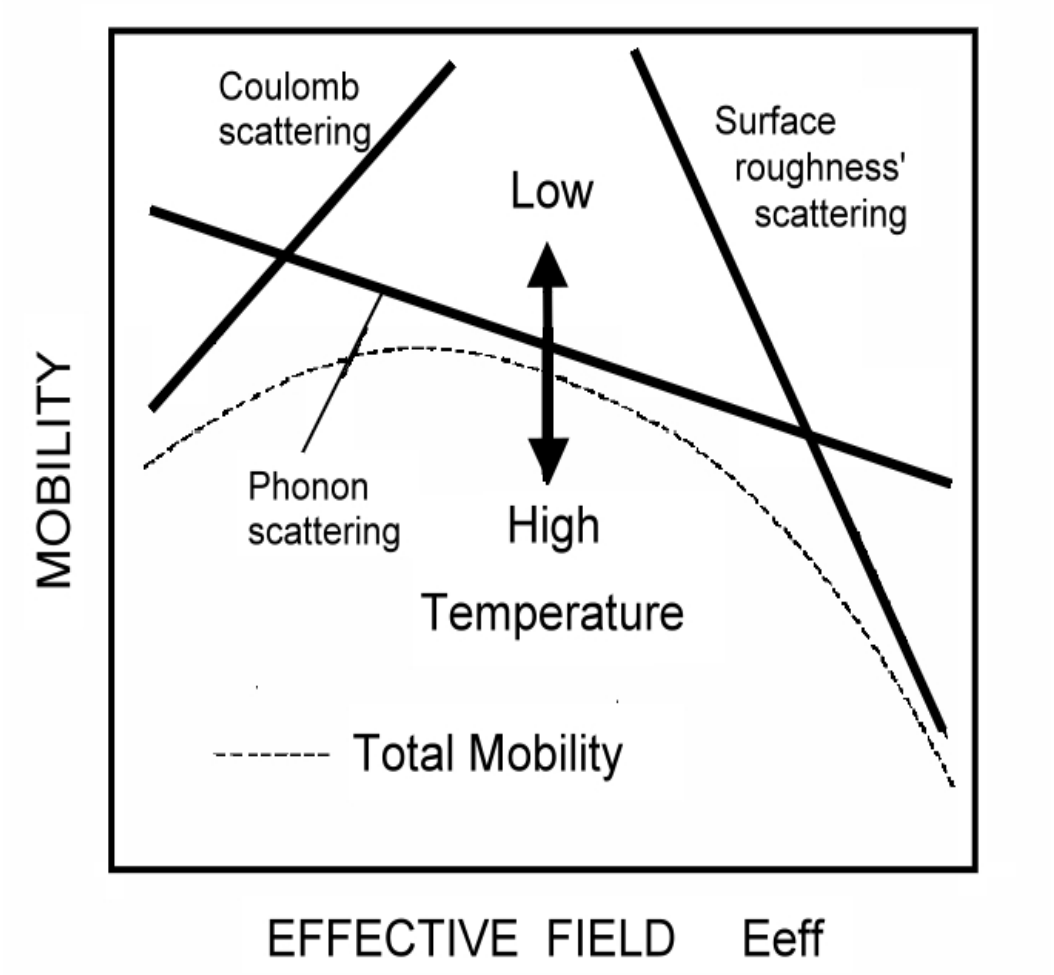


Fig. 3-3 Three types of scatterings in MOSFET devices, including impurity scattering, surface scattering and the phonon scattering.

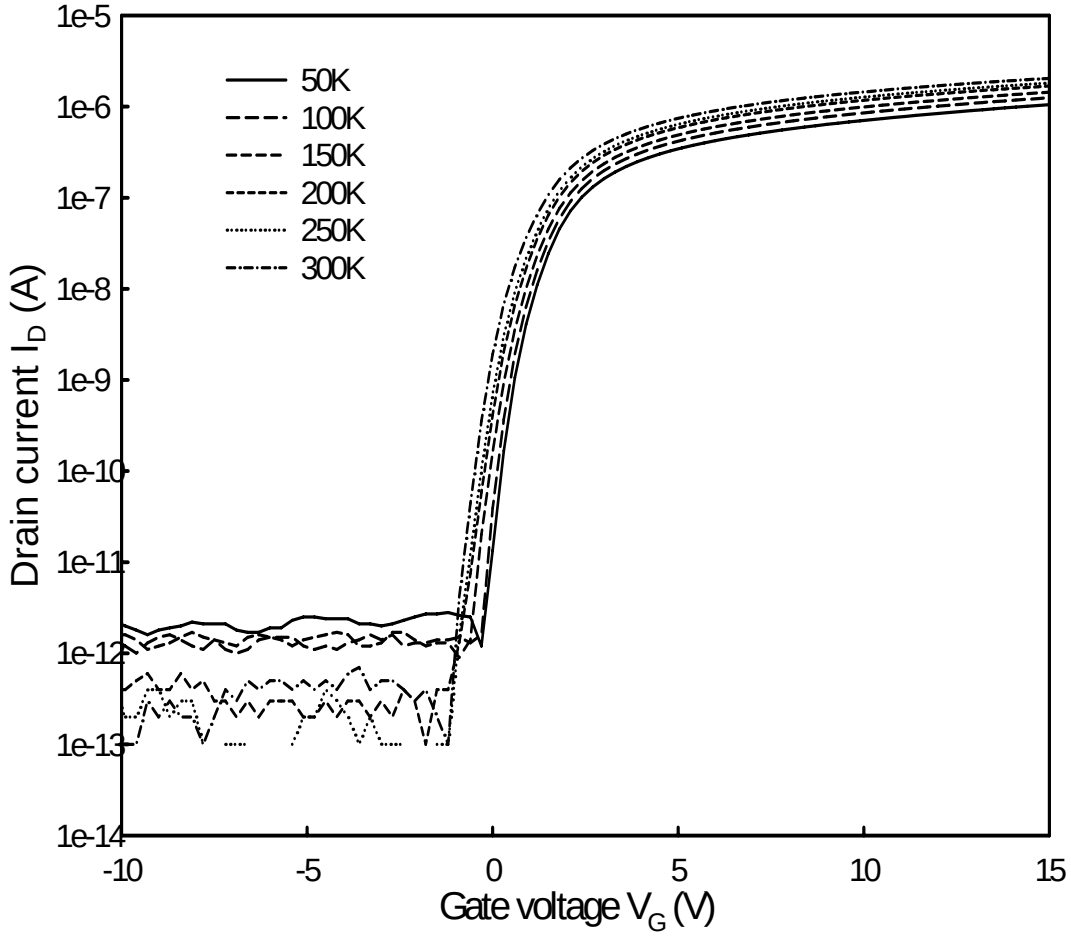
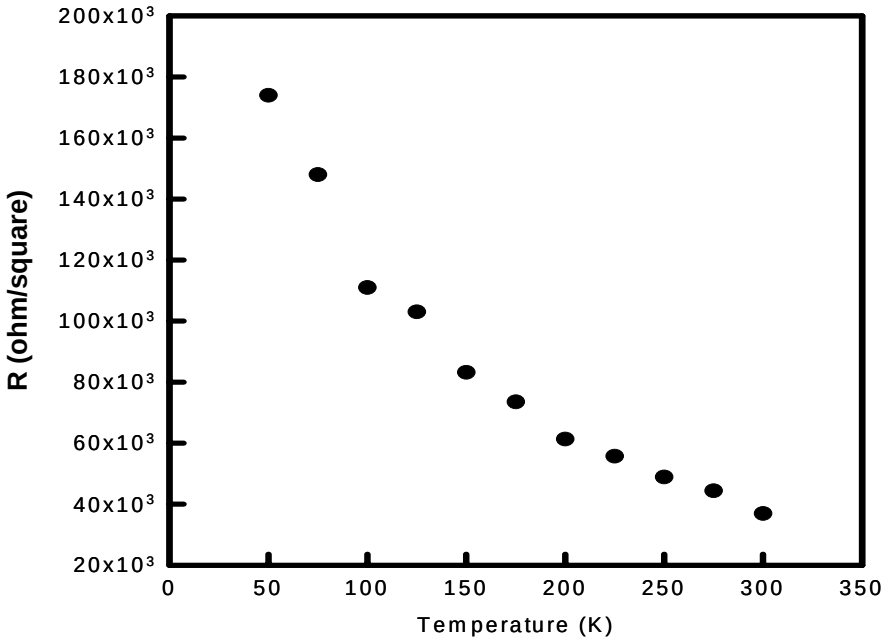
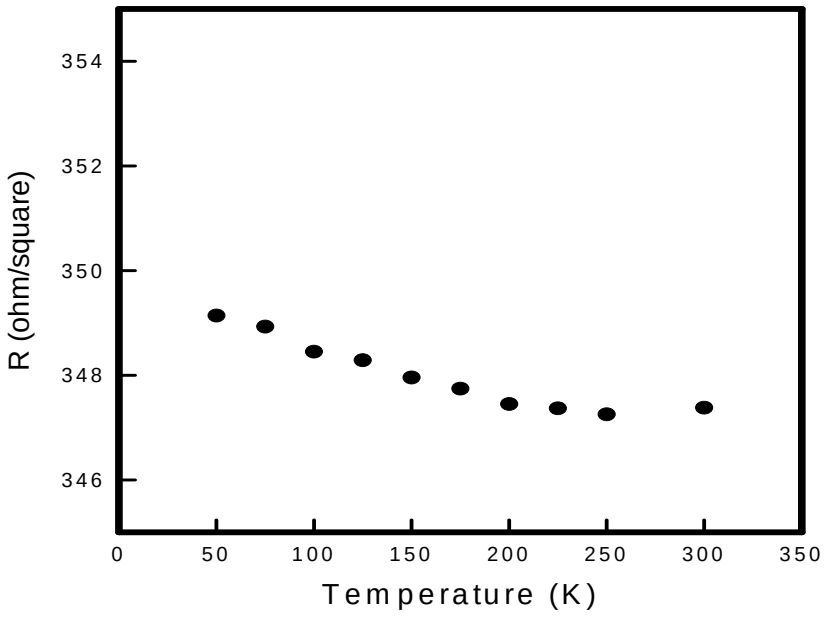


Fig. 3-4. The I_D-V_G relations of LDD-TFT at the temperatures from 50K to 300K.



(a)



(b)

Fig. 3-5 The sheet resistances of phosphorous (a)heavily-doped and (b)light-doped poly-Si film at the temperatures from 50K to 300K.

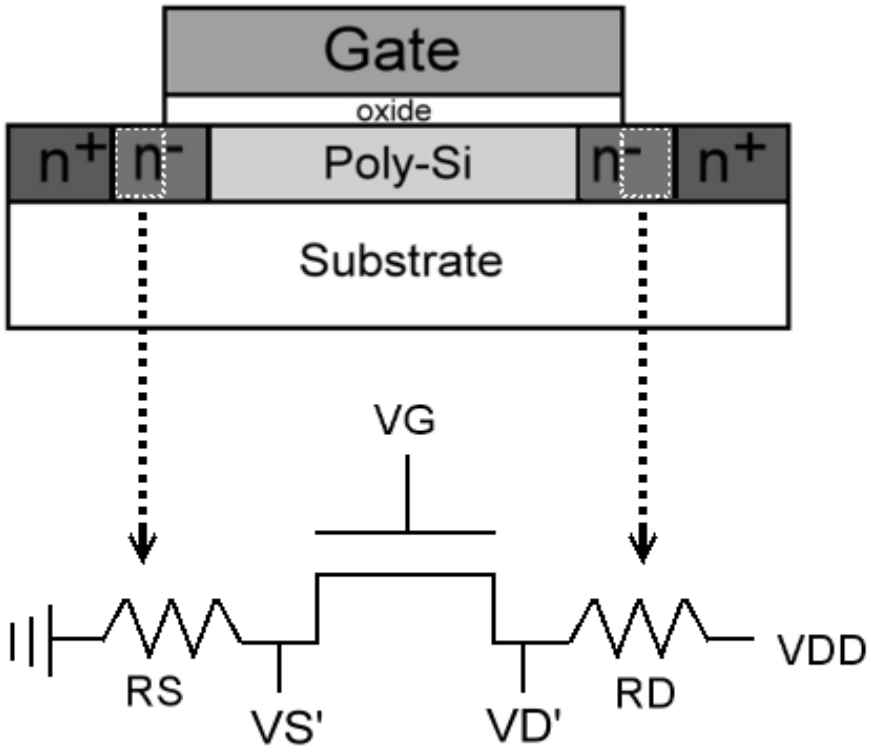


Fig. 3-6 The LDD layers extended out the gate overlap region behave as the temperature-dependent resistors and series connecting with the gate control region.

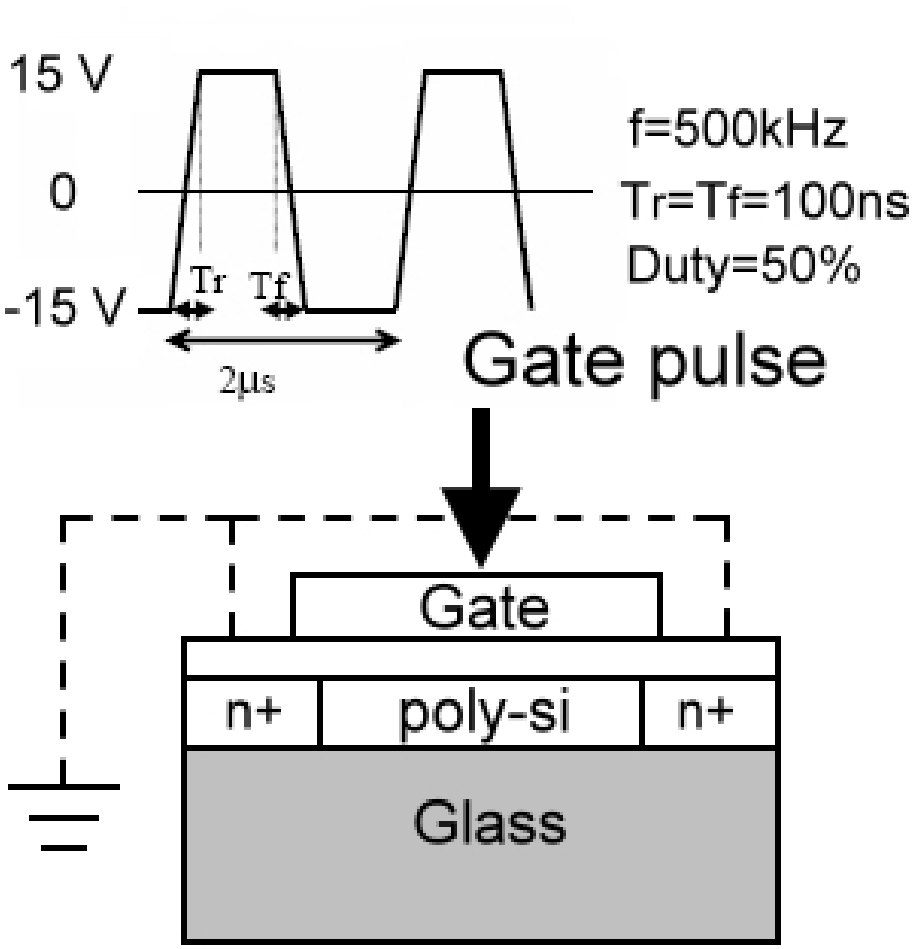


Fig. 3-7 The stress pulses were conducted on the gate electrode as the dynamic stress and source/drain were grounded. The rectangular pulse with amplifier of ±15V and frequency of 500kHz. Both the rising time (Tr) and falling time (Tf) were 100 ns.

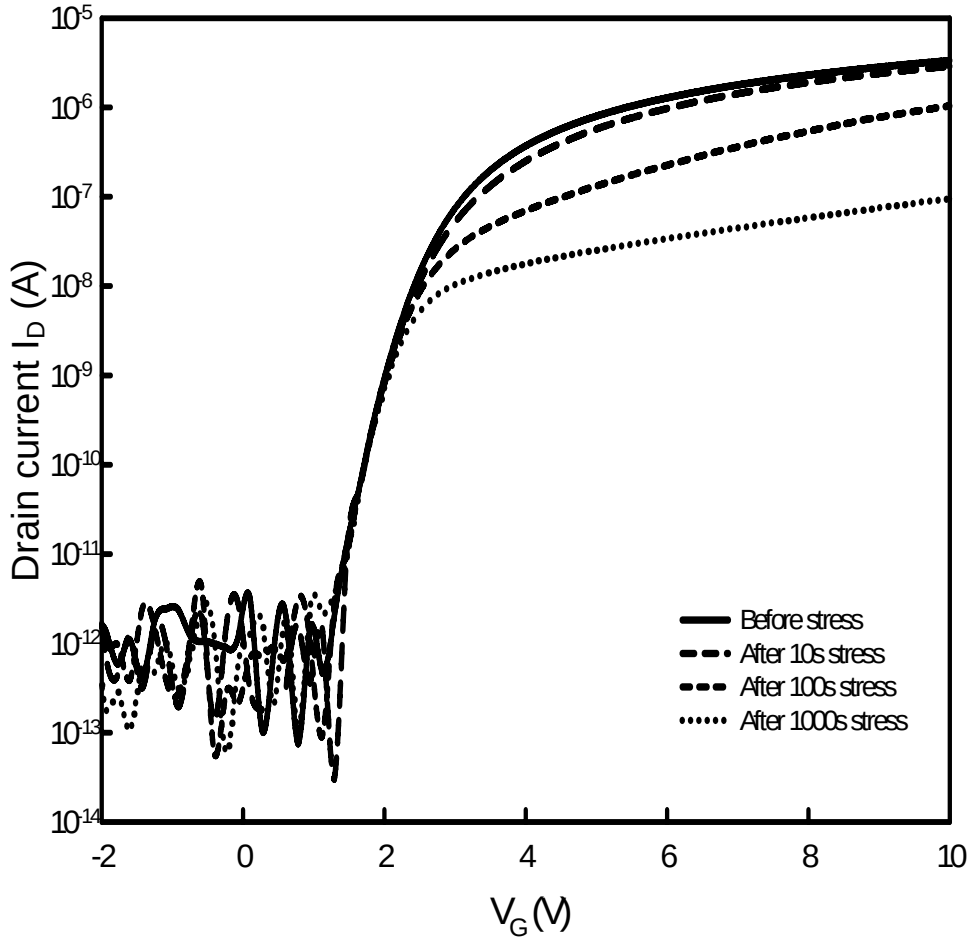


Fig. 3-8 The I_D-V_G relationships of n-channel poly-Si TFT (L=9μm) with the dynamic stress times for 10 to 1000 seconds.

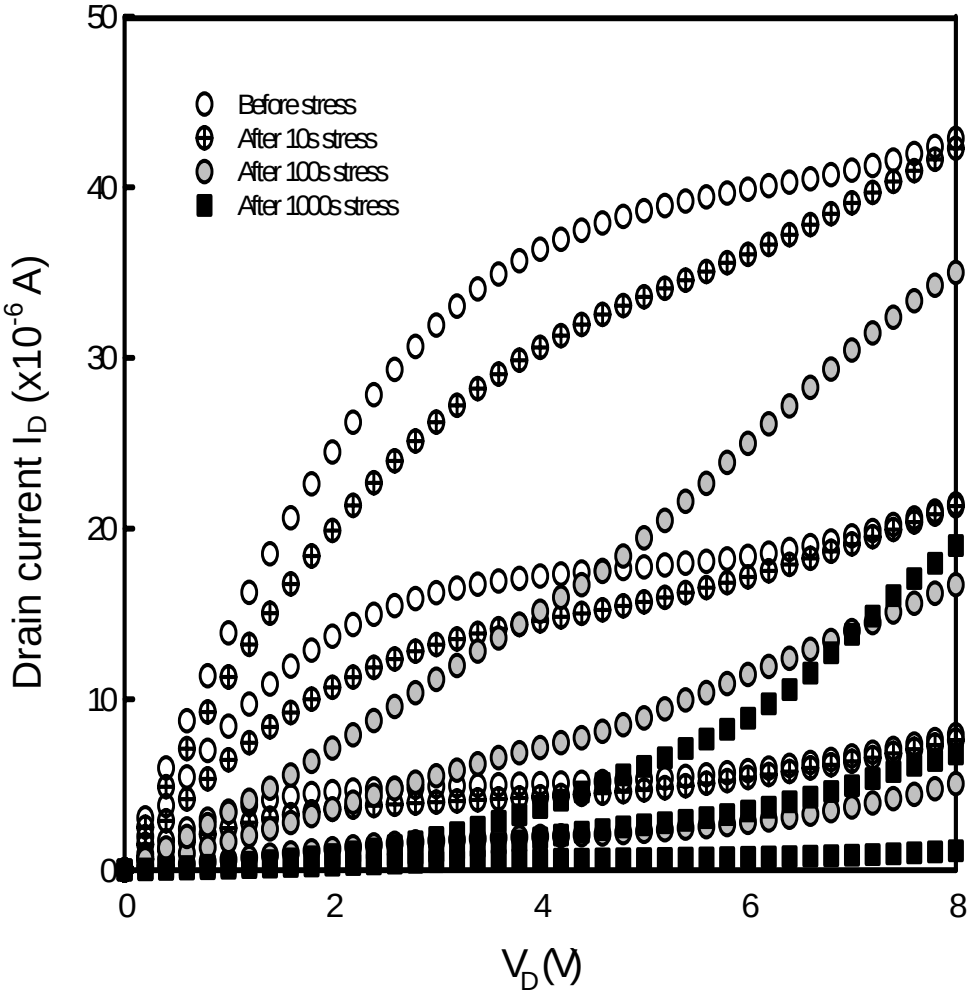


Fig. 3-9 The I_D-V_D characteristics of the TFT with the dynamic stress times.

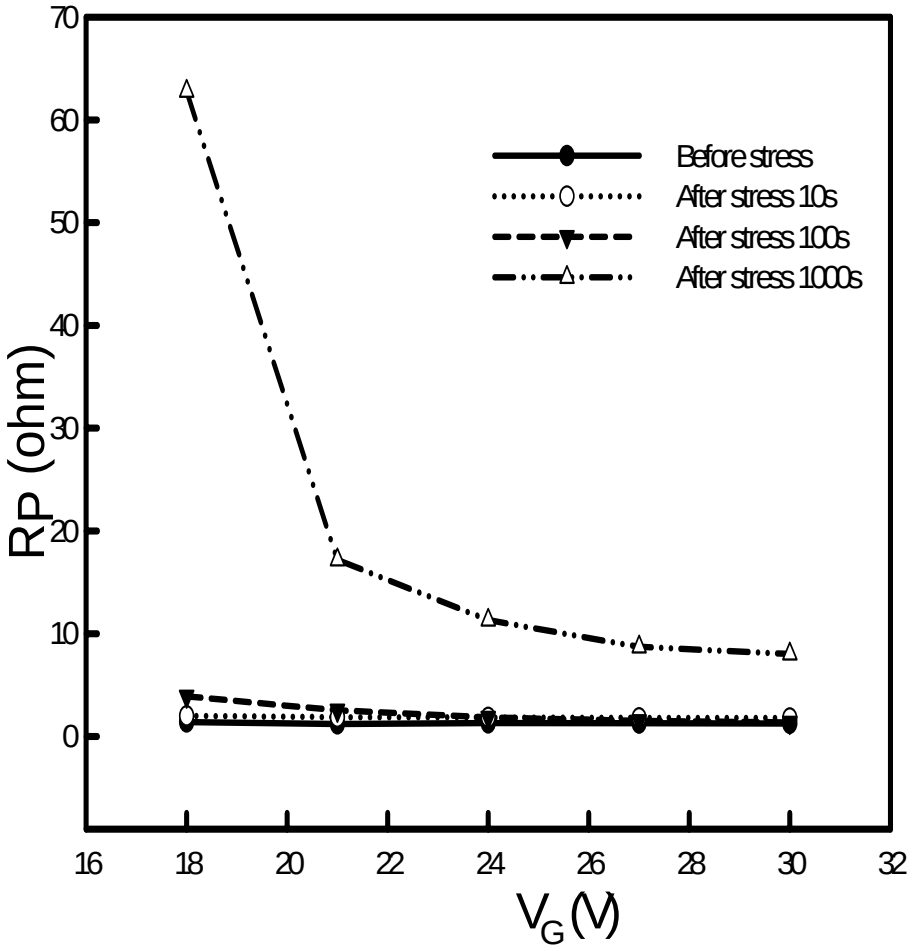


Fig. 3-10 The gate voltage dependence of the parasitic resistance R_p of TFT with various stressing times. There is a distinct raise in R_p of poly-Si TFT after 1000 s.

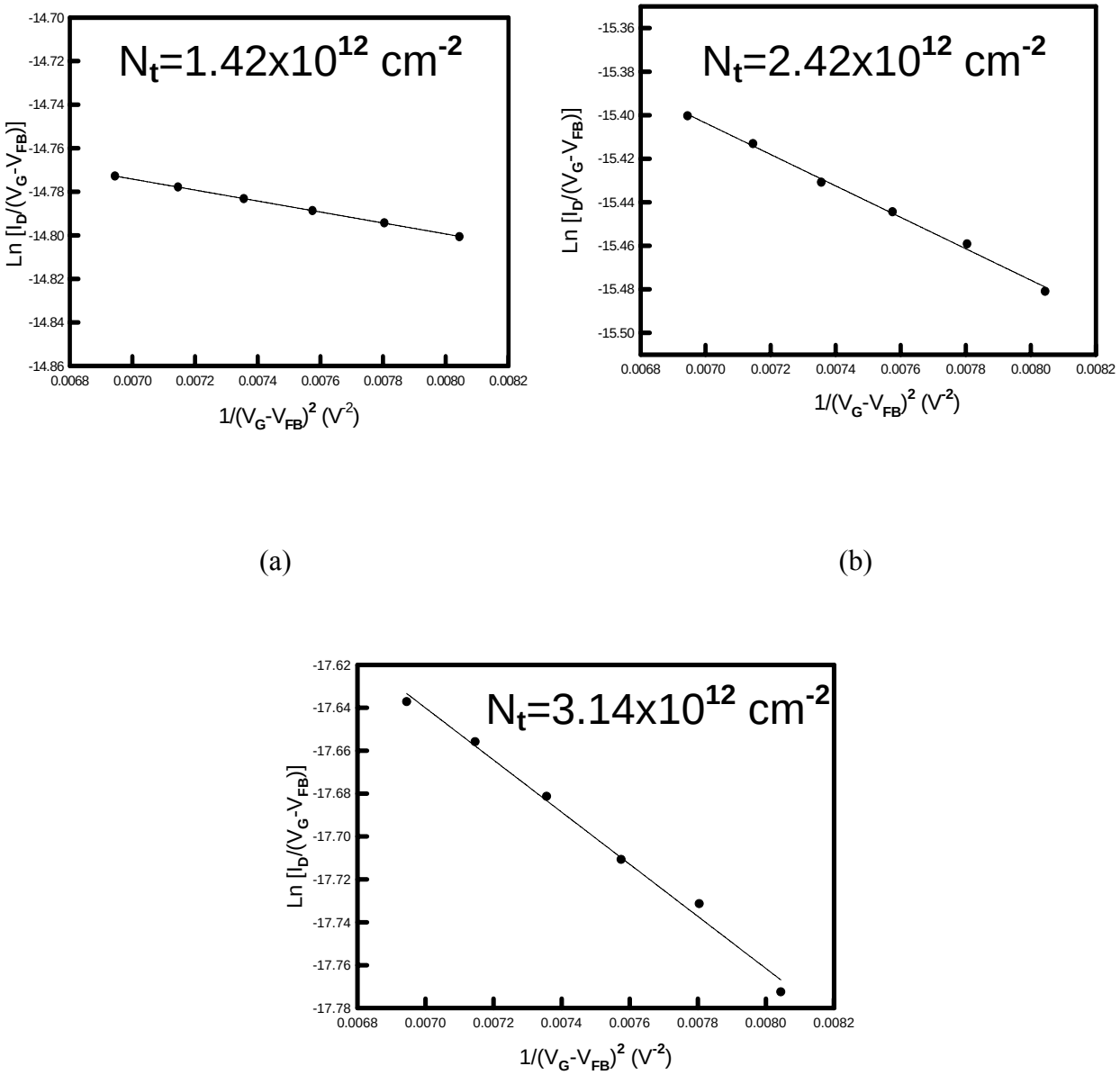


Fig. 3-11 (a), (b), and (c) present the effective trap density (N_t) of poly-Si TFT with AC stress for 0, 100, and 1000 s, respectively. The N_t of the device with 1000 s stress is 2.21 times larger than that of the non-stressed poly-Si TFT.

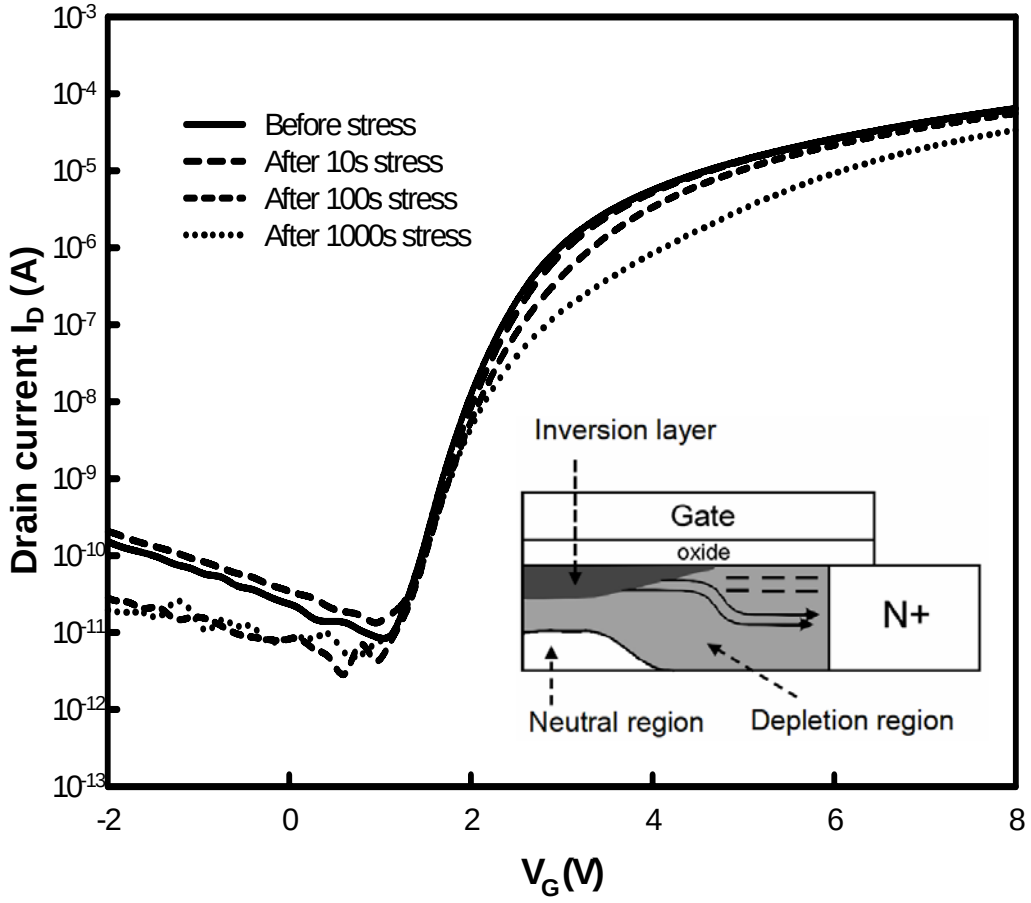


Fig. 3-12 I_D-V_G curves of poly-Si TFT at saturation operation (V_D=8V) with AC stress for 0 to 1000 s. The degradation in ON-current with the high drain bias is much weaker compared to the linear ones. The inset figure indicates that carriers can spread to the bulk at the pinch-off region near the drain electrode.

Chapter 4

The Influence of Grain Boundary Location on Low Temperature Poly-Si Thin-Film Transistors

4.1 Introduction

Poly-Si TFTs are attractive as the active devices in driver circuits of active-matrix liquid-crystal display (AM-LCD) and active-matrix organic light-emitting diode display (AM-OLED). Recently the performance gap between poly-Si TFTs and single-crystalline silicon devices is closer because of the improvement of poly-Si quality. [4.1-4.3] Manufacturers of liquid crystal displays (LCD) are under a constant challenge to produce higher performance displays at lower costs and increasing display size. One of the major advantages of low-temperature polycrystalline silicon thin film transistor (LTPS-TFT) technology is the opportunity to make use of low cost glass substrates due to the low temperature of the excimer laser annealing (ELA) process. [4.4-4.5] Additionally, LTPS-TFT technology achieves higher display performance. The performance of a TFT is linked to electron mobility which is defined in square centimeters per volt-second. Polycrystalline silicon TFT mobility is with 100 to 150 $cm^2/Vsec$ about hundred times better than of amorphous silicon TFT. In order to improve transistor characteristics, there has been a lot of research to enlarge the grain size and control grain boundary location and crystal orientation. [4.6-4.10] An excimer-laser-based crystallization technique that enables controlled periodic placement of high-angle grain boundaries has been developed in order to address the problems associated with the presence of defects within the material

[4.6-4.10]. This crystallization scheme—sequential lateral solidification (SLS)[4.11-4.15]—allows one to manipulate the resulting microstructure of the polycrystalline Si film to yield a wide range of material quality: from large defect-free single-crystal islands to uniform large-grained polycrystalline material.

In an ideal case, the grain size is essentially large, and both of the grain boundary location and crystal orientation are perfectly controlled. The transistor characteristics will be similar to single-crystal Si transistor. However, the grain size is not sufficiently large and the grain boundary location is not easy to control. So in practical case there are a few grain boundaries in a TFT. The device performance may strongly depend on the grain boundary location and performance variations may be quite large. In this chapter, the device characteristics and reliability of poly-Si TFT with different number of grain boundary and its location are investigated. In section 4.3.2, the influences of GB arrangement on electrical performance and stability of poly-silicon TFT have been investigated. The degradation mechanism under dynamic operation for poly-Si n-channel TFT will be investigated by electrical analysis in detail in section 4.3.3. The poly-Si TFT containing GB perpendicular to the channel direction was compared with the counterpart without the arrangement of perpendicular GB within.

4.2 Device Fabrication

Top-gated poly-Si TFTs were fabricated on glass substrate by low-temperature processes. Buffer SiO_2 films and 90-nm-thick amorphous silicon films were deposited by plasma enhanced chemical vapor deposition (PECVD), and subsequently, the films were dehydrogenated by furnace annealing. After dehydrogenation, the a-Si films were crystallized by sequential lateral solidification (SLS) laser annealing process. SLS of the a-Si film was conducted using a system that consisted of 1) a 308-nm

XeCl excimer laser, 2) a reticule mask with chevron-shaped apertures, 3) projection optics, and 4) a high-precision translation system. The SLS process is an excimer-laser projection-based scheme for crystallization of thin films on amorphous substrates. This method can be used to readily produce a wide range of microstructures through manipulation of grain boundary placement within the crystallized material. Following the SLS process, 100-nm-thick gate oxide was deposited by PECVD. MoW was sputtered as a gate electrode and phosphorous ion doping was used to form source and drain (S/D) regions. The dimension of TFTs in this work was 20μm for channel width (W) and 5μm for channel length (L), respectively. The overlap between gate electrode and S/D junction is 1μm.

4.3 Results & Discussions

4.3.1 Electric Properties & DC stress

Figure 4.1(a) shows the top view of a high-resolution scanning electron microscopy (SEM) image of SLS laser annealed poly-Si film. The SLS laser annealed poly-Si thin film includes a domain region containing a mixture of plurality of crystals substantially parallel to the carrier body. The crystals may be columnar or capillary crystals. The grain boundaries present in the SLS laser annealed poly-Si film can be divided into two types, namely main-GB and sub-GB. The orientation of GB which is perpendicular to channel direction is called main-GB, as labeled by the arrowhead in Fig. 4.1(a). Furthermore, the grain boundaries which lie between main-GBs are called sub-GBs and substantially parallel to the transport paths of carriers flow drifted by the electric field of the drain side. The width of each main-GB is about 100 nm and the space between main-GBs is about 10 μm measured by atomic force microscopy (AFM). Figure 4.1(b) shows the AFM image, the height of

protrusion is about 100nm at the grain boundary region. The channel length of TFTs in this study is 5μm for all samples and relatively smaller than the main poly-Si grain (10μm). Therefore, the channel region of TFT may locate entirely inside the main poly-Si grain zone. But some TFT devices would contain a main-GB within the channel. The two kinds of poly-Si TFT were depicted in the Fig. 4.2(a). Figures 4.2(b) and (c) show the microscope picture of the GB and NGB TFT, respectively. An obvious duck-line is placed at the middle of the channel of GB TFT. We named the TFTs with the main-GB GB-TFT, and ones without the main-GB NGB-TFT for short in this study. Figure 4.3 illustrates the transfer curves, I_D-V_G, and linear trans-conductance (g_m) of GB-TFT and NGB-TFT, respectively. The field effect mobility (μ_{FE}) was extracted from a peak linear trans-conductance at V_d = 0.1 V. According to Fig. 4.3, NGB-TFT has higher μ_{FE} of 283.2 cm^2 / Vs than GB-TFT of 262.5 cm^2 / Vs. Additionally, the threshold voltage (V_{th}) and sub-threshold slope (*SS*) of poly-Si TFTs are extracted for discussion. The V_{th} is defined as the gate voltage required to achieve a normalized drain current of $I_D = 10^{-8}$ A at V_d = 0.1 V with a normalized W/L ratio. The V_{th} of NGB and GB TFT is 2.64 and 2.90V, respectively. The NGB TFT owns superior SS value of 0.39V/dec than that of GB TFT, 0.43V/dec. The better conducting characteristics were exhibited in NGB-TFTs. Moreover, the capacitance-voltage (C-V) characteristics of the TFTs were investigated using HP4284, as illustrated in Figs. 4.4. The voltage signals were conducted on the gate electrode of the TFT, and the S/D electrodes were connected together to the ground. It was found that the CV curve of NGB TFT transfers abruptly from the turn-off state to the channel-formation state. The CV transition curve of GB TFT shows a slightly slow in comparison with the NGB TFT as the voltage is increased from -10 to 15V. The existence of the trap numerous region (GB) at the middle of the channel in GB TFT leads to the slow transition of the CV curve. The trap states in the poly-Si film

would be filled by the field-induced carrier, and thus the GB TFT exhibits the slow transition in CV measurement.

In order to examine the GB effects on the TFT reliability characteristics, the hot carrier stressing tests were performed on the poly-Si TFTs. As for the DC stress conditions, a gate voltage of 6V and drain voltage of 12V were applied. Figure 4.5 shows the I_D-V_G characteristics of NGB-TFTs after stress for 10 and 100 s, respectively. It is apparent that with increasing stress time the impact of the applied stress leads to a decrease of on-current in the above threshold region of the I_D-V_G characteristics, while TFT operating in the linear region. The mobility of NGB-TFT is decayed from 283.2 to 46.9 cm^2 / Vs after 100 seconds stress. Moreover, the V_{th} is shift from 2.64 to 4.6V and *SS* is increased to 0.64 V/dec after the stress.

For comparison, figure 4.6 depicts the I_D-V_G relations of GB-TFT after the DC stress for 10 and 100 s. The distinct difference in endurance against the hot carrier stress is demonstrated. The NGB-TFT was degraded rapidly during the DC stressing, but the electrical properties of GB-TFT kept at a good level. For the case of GB-TFT, both threshold voltage and sub-threshold slope almost unchanged, and the mobility was decreased from 262 to 227 cm^2 / Vs after 100 s stress. These results made a remarkable comparison to the intrinsic properties of both devices. Although the GB TFT owns lower current driving capability, it has outstanding endurance against the DC stressing. In poly-Si TFTs the electrical degradation is often characterized by a decrease of the subthreshold slope, mainly due to the generated traps in the grains and a threshold voltage shift caused by charge trapping in the gate oxide and at the interface states, as shown in Fig. 4.5. However, the GB-TFT showed that both subthreshold slope and threshold voltage remain unchanged. This indicates that the degradation of the GB-TFT occurred due to neither charge trapping in the gate oxide

nor the creation of traps at the deep states. We can infer that the tail states produced by the strained bounding are responsible for the degradation of GB-TFT.

To clarify the distinct difference between the TFTs' electrical reliabilities, the effective trap density of the TFTs were extracted. According to Seto's model, the effective trap density (N_T) of NGB and GB TFT is extracted to be 4.95 x10^{17} and 8.64 x10^{17}cm^{-3}, respectively. For brevity, the increasing in N_T of GB-TFT is assumed to be mainly contributed by the 100 nm trap-numerous region in the 5 μm channel. Thus, a 100 nm region with trap concentration of 1.84 x10^{19} cm^{-3} was added in the middle of channel of the GB TFT, while other regions had trap concentration about 5x10^{17} cm^{-3}. The trap concentration of 4.95 x10^{17} cm^{-3}, however, was uniformly distributed in whole channel of the NGB TFT. Then, the electrical field distribution was simulated by a simulation tool ISE-TCAD. The comparison between GB and NGB TFT in electric field is illustrated in Fig. 4.7. It was found that the electric field near the drain region was reduced while GB located in the center of the channel, as shown in Fig. 4.7. For GB-TFT, the maximum of electric field at the drain shows about 27% lower than that without grain boundary in the channel. The reduction of electric field at the drain side effectively contributed to the suppression of hot carrier effects.

4.3.2 AC stress

For logic circuits application, the influences of AC gate pulse on poly-Si TFTs have to be clarified. The dimensions of TFTs in this work were L=9μm, W=6μm and the overlap of gate metal and S/D junction is 1μm. The cross section views of TFTs were illustrated in Fig. 1. The stress pulses were performed on the gate electrode as the dynamic stress and source/drain were grounded, as shown in the inset of Fig. 1. As for

the stress condition, we used the rectangular pulse with amplifier of ±10V and frequency of 500kHz. Both the rising time (Tr) and falling time (Tf) were 100 ns.

Figs. 4.8 and 4.9 present the I_D-V_G relations of GB and NGB TFT with the dynamic stress times for 10 to 1000 s, respectively. The distinct decrease in on-current of the TFTs was found with the increasing stress duration. The mobility of NGB TFT is decayed from 282.9 to 204 cm^2/Vsec after 1000s stress. Both the sub-threshold swing (0.36 V/dec.) and threshold voltage (2.34V) kept well during the stressing. Accordingly, GB TFT possessed the lower value of mobility (136.9 cm^2/Vsec) than the initial mobility (243 cm^2/Vsec). A slight degradation was found in the threshold voltage and subthreshold swing of the GB TFT. From the evolution of the transfer characteristics at the linear operation with stress time, it is apparent that the impact of the applied stress leads to a parallel decrease of the on-current operated at the above threshold region of the I_D-V_G characteristics.

Contrary to the results of DC stress, the NGB devices exhibit better endurance against the AC gate pulse stress. The degradation of AC stress is usually contributed to the occurring of hot carrier near the S/D electrode region, as mentioned in chapter 3. We have known that the impact of hot carrier effect in DC stress on GB TFT is weaker because of the reduction of electric field at the drain region. The damage of GB TFT should be contributed by other factors under AC gate pulse stress. The distinct differences between the NGB and GB device are the existence of GB and the surface roughness of poly-Si film. The NGB TFT owns smooth plane for the channel region, as shown in Fig. 4.1(b). By contrast, an obvious protrusion of 100nm is located at the middle of GB TFT. The thickness of gate oxide at protrusion is thinner than the other region in GB TFT. The simulation tool was performed to understand the difference between two devices in electrical field at the protrusion region. Figs. 4.10(a) and 4.10(b) illustrate the distribution of electrical field at the

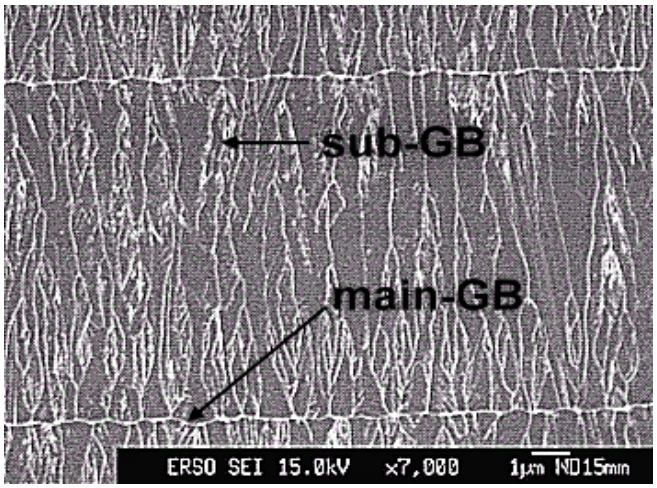
protrusion and smooth plane. The interface of oxide/poly-Si at protrusion is suffered the higher electrical field than that at the smooth plane. The state creation and charge trapping in the oxide at the protrusion should be responsible for the degradation. Thus, the difference in degradation evolutions between GB and NGB TFTs under AC gate bias is properly resulted from the protrusion. Except to the damage region near the S/D junctions, GB TFT possessed the damaged region locating at the protrusion due the high gate bias stress.

4.4 Conclusions

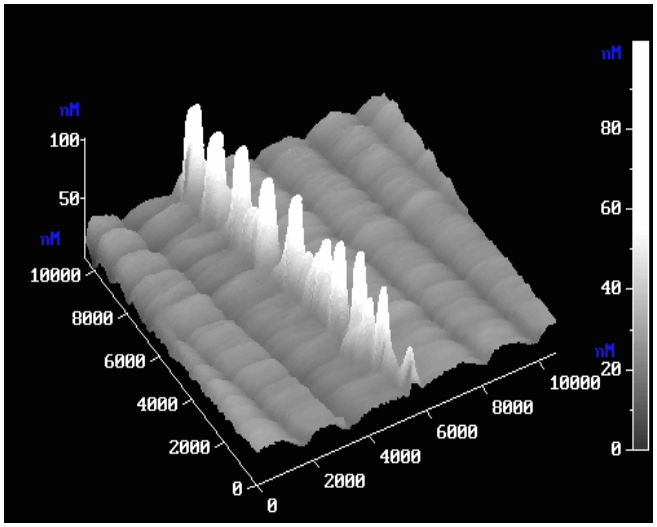
The comparison of electrical stability between GB and NGB-TFT has been shown in this study. The NGB-TFT owns superior conducting ability than the GB TFT which contains a 100-nm trap-numerous region at the middle of the channel. However, the GB-TFT exhibits the better endurance against DC stress than the NGB-TFT. Based on the simulation result, the existence of GB in the middle of channel of poly-Si TFT would reduce the electric field in the drain region significantly. Accordingly, the GB-TFT suffers relatively lighter impact of hot carrier stress and maintains electrical characteristics well during the DC stressing. The NGB-TFT was seriously degraded by the DC stress with the high electric field at the drain side.

Nevertheless, the distinct electrical behaviors of the TFTs were demonstrated under the AC gate bias stress. Due to the existence of protrusion in the channel, GB-TFT shows weaker endurance against the AC gate pulse stress than that of NGB TFT. The magnitude of the vertical field at the protrusion is stronger than the other regions in GB TFT. The strong electric field would lead to the state creation and charge trapping at the protrusion and reduce the device's electrical performance. Consequently, grain

boundaries perpendicular to the channel direction in SLS poly-Si TFT would reduce the horizontal field near the drain side. But the protrusion of grain boundaries of SLS poly-Si film would lead to the larger vertical field. The influences of horizontal and vertical fields can be observed and identified under hot carrier and AC gate stresses.

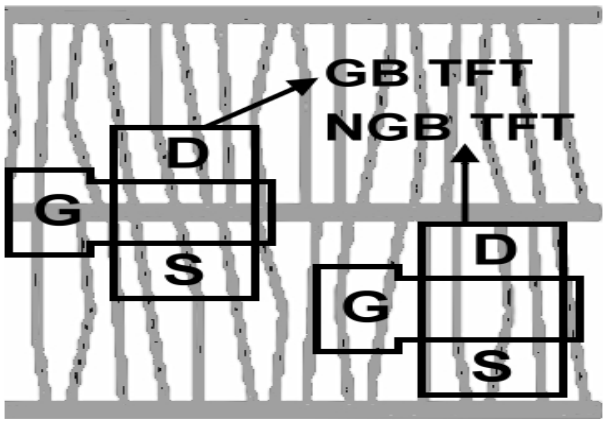


4-1(a)



4-1(b)

Fig. 4-1 (a) The top view of a high-resolution scanning electron microscopy (SEM) image of SLS laser annealed poly-Si film. The orientation of main-GB and sub-GB is perpendicular and parallel to channel direction of the TFTs we utilized, respectively. (b) The AFM image of SLS poly-Si film, the height of protrusion is about 100nm at the grain boundary region



4-2(a)

4-2(b)

4-2(c)

Fig. 4-2 (a) GB-TFT owns a main-GB in the middle of the channel. NGB-TFT lies in the main-GB free region. (b) The microscope picture of GB TFT (c) The microscope picture of NGB TFT

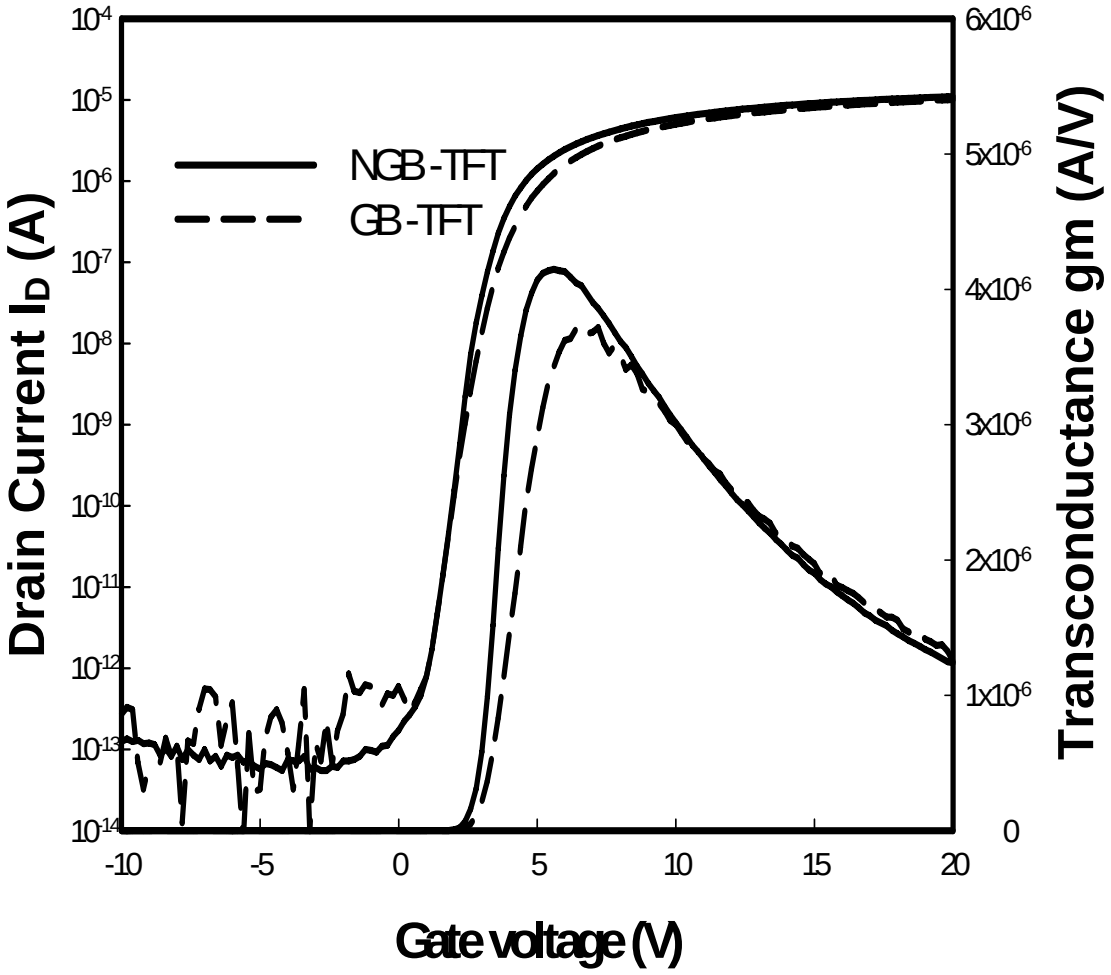


Fig. 4-3 I_D - V_G transfer characteristics of NGB and GB TFTs with the same W / L ratio. The NGB TFT has larger field mobility (283.2 cm^2/Vsec) than that of the GB device (262.5 cm^2/Vsec).

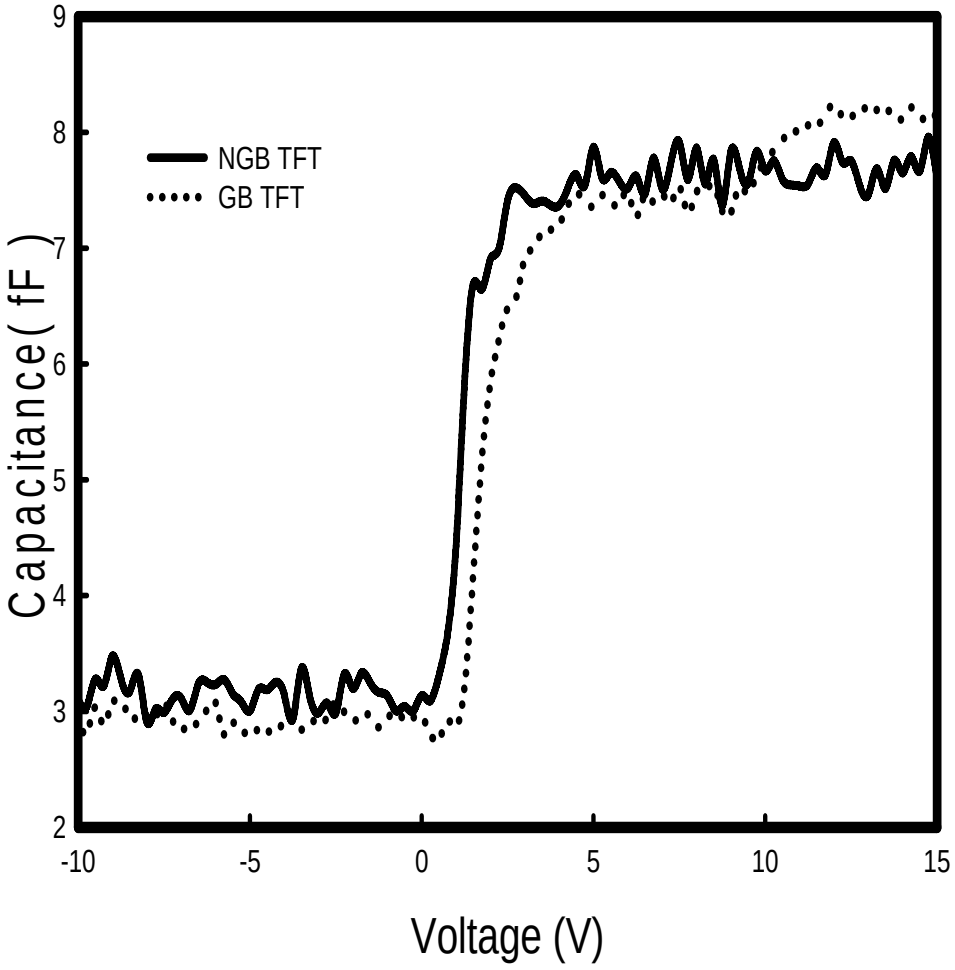


Fig. 4-4 The capacitance-voltage (C-V) characteristics of GB and NGB TFTs. The CV transition curve of GB TFT shows a slightly slow in comparison with the NGB TFT.

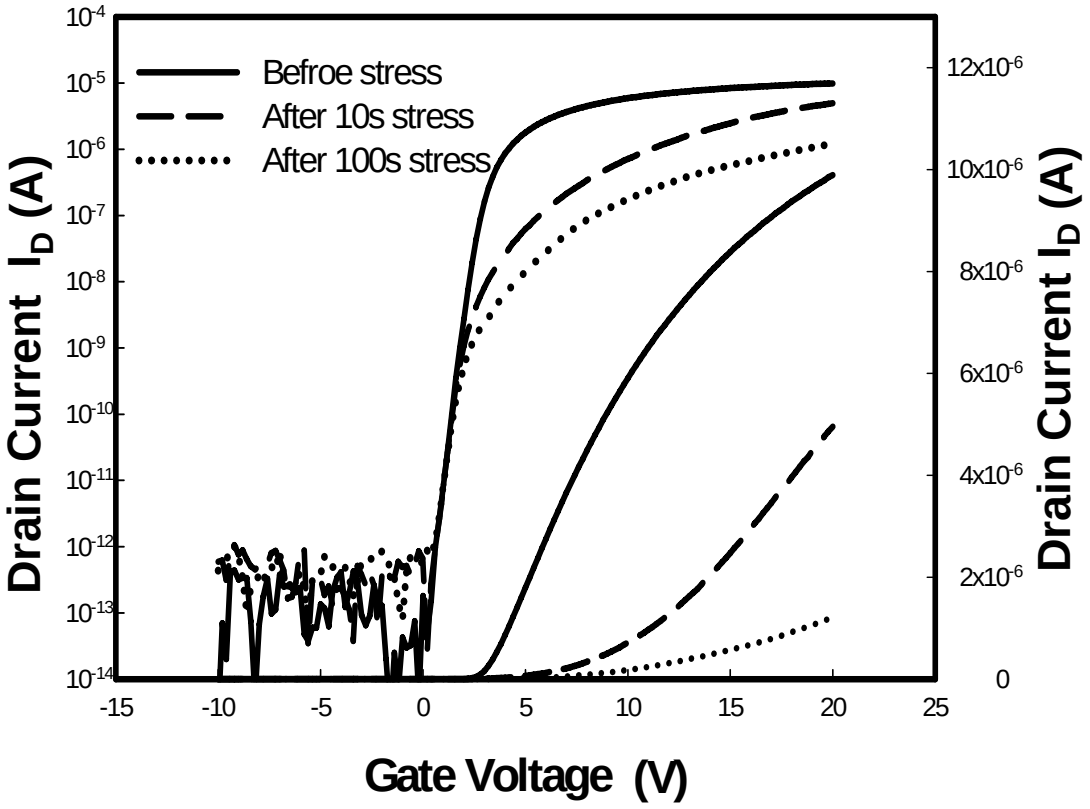


Fig. 4-5 I_D - V_G relations of NGB-TFT in linear and logarithm with the stress for 0, 10, and 100 s. After stressing for 100 s, the on-current of TFT at V_G=20 is degraded to 12% of the magnitude of the initial value.

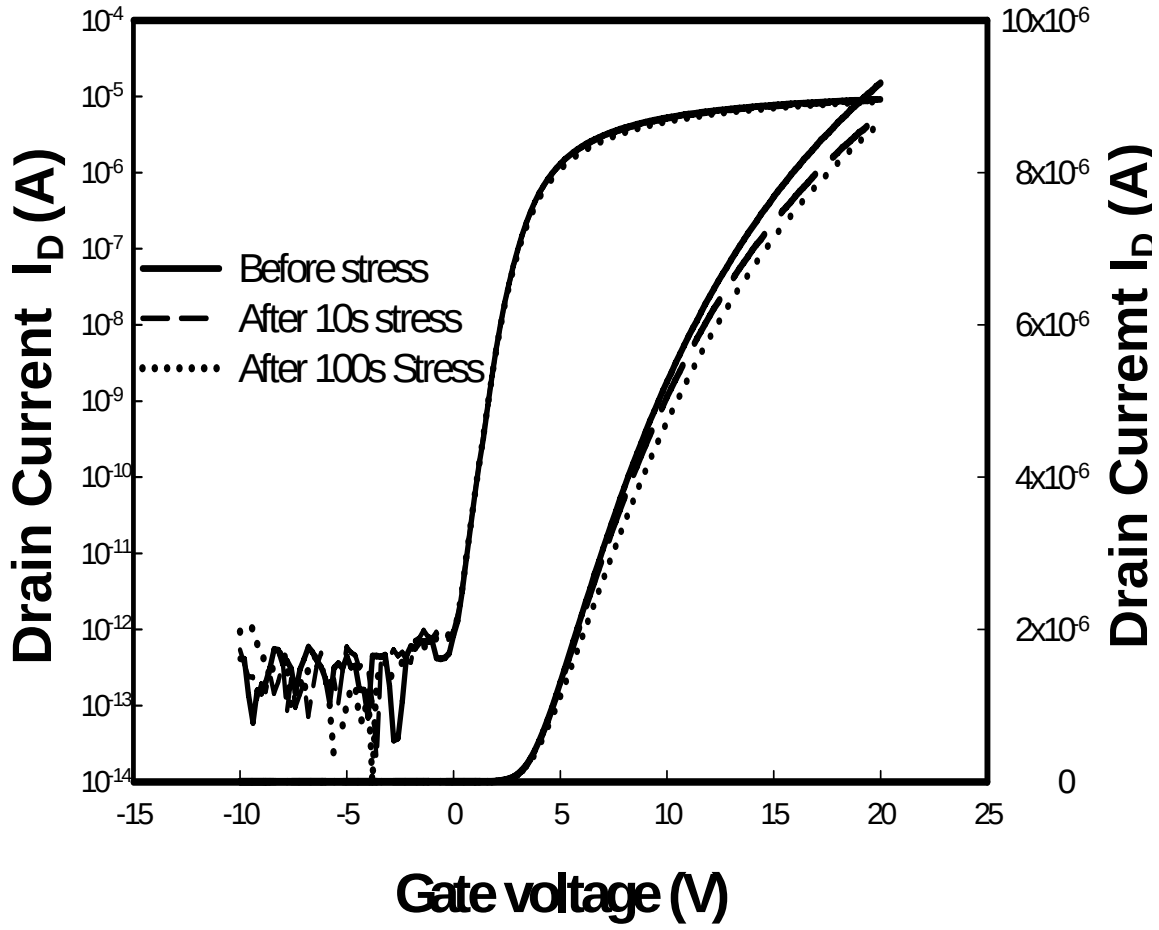


Fig. 4-6 I_D - V_G relations of GB-TFT in linear and logarithm with the stress for 0, 10, and 100 s.

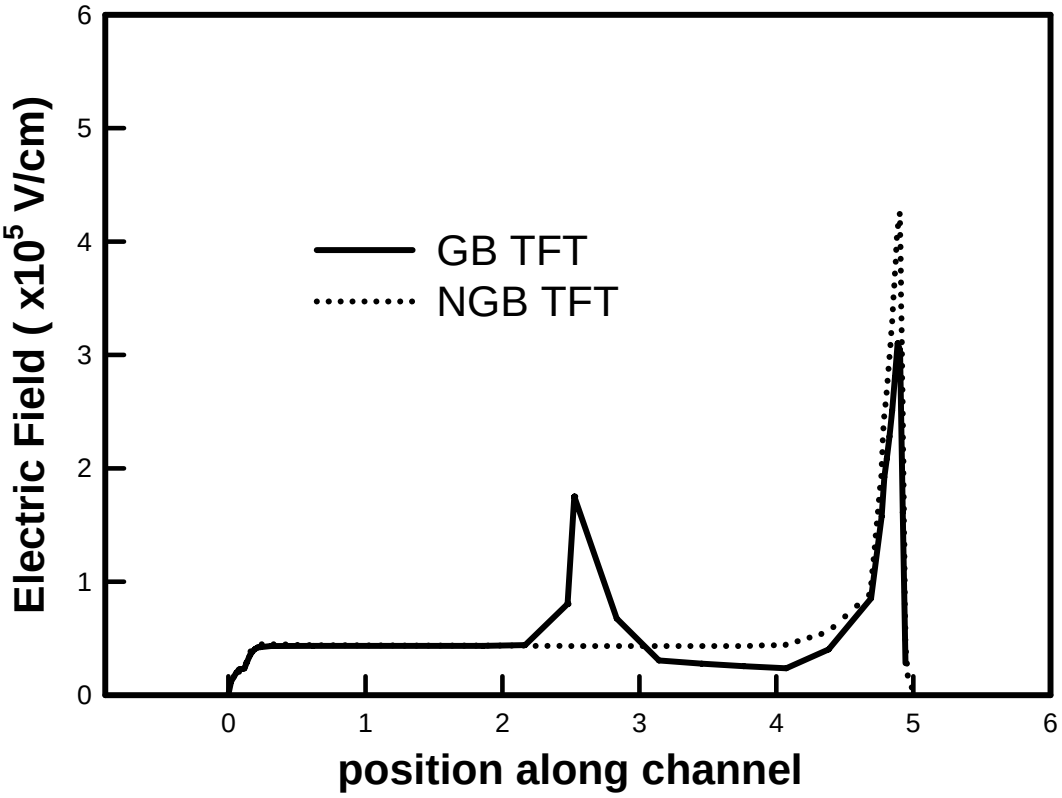


Fig. 4-7 The electric distribution in the channel region of the TFTs under the bias conditions V_G=6V and V_D=12V. The main-grain locates at the center of the channel in GB-TFT. For GB-TFT, the maximum of electric field at the drain shows about 27% lower than that without grain boundary in the channel

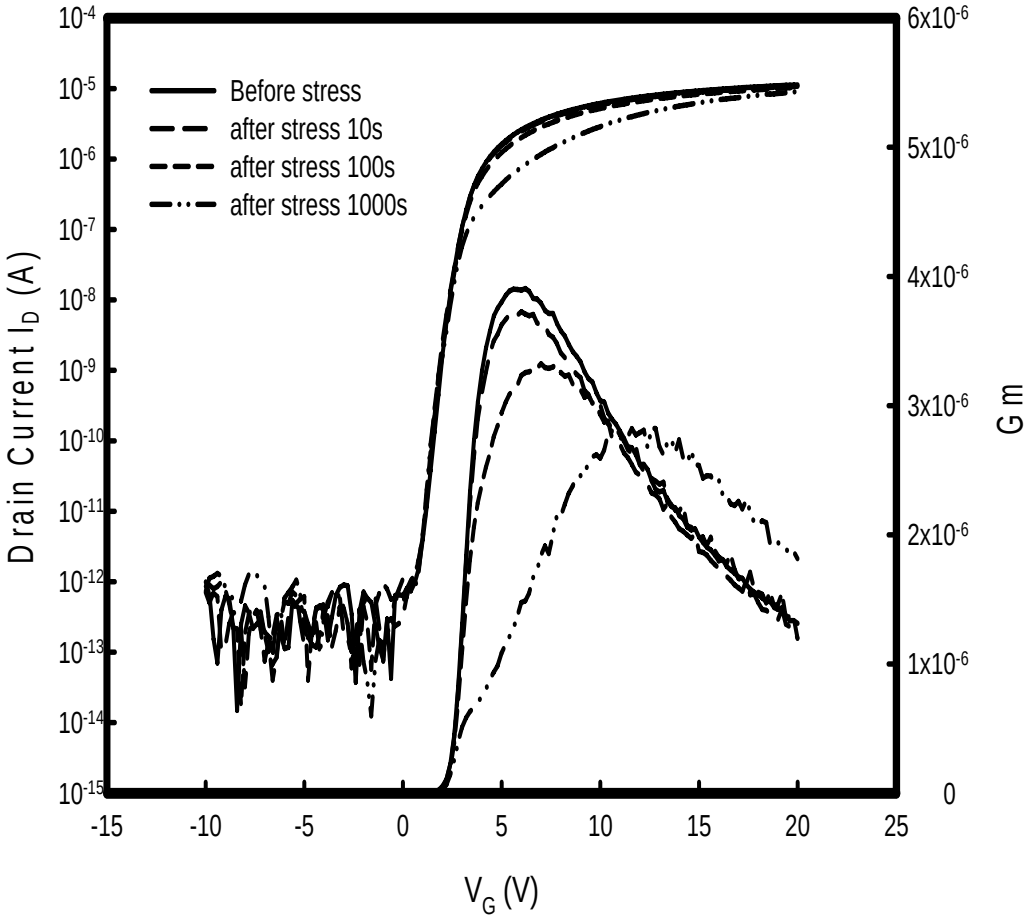


Fig. 4-8 The I_D-V_G relations of NGB TFT with the dynamic stress times for 10 to 1000 s. The mobility of NGB TFT is decayed from 282.9 to 204 cm^2/Vsec after 1000s stress.

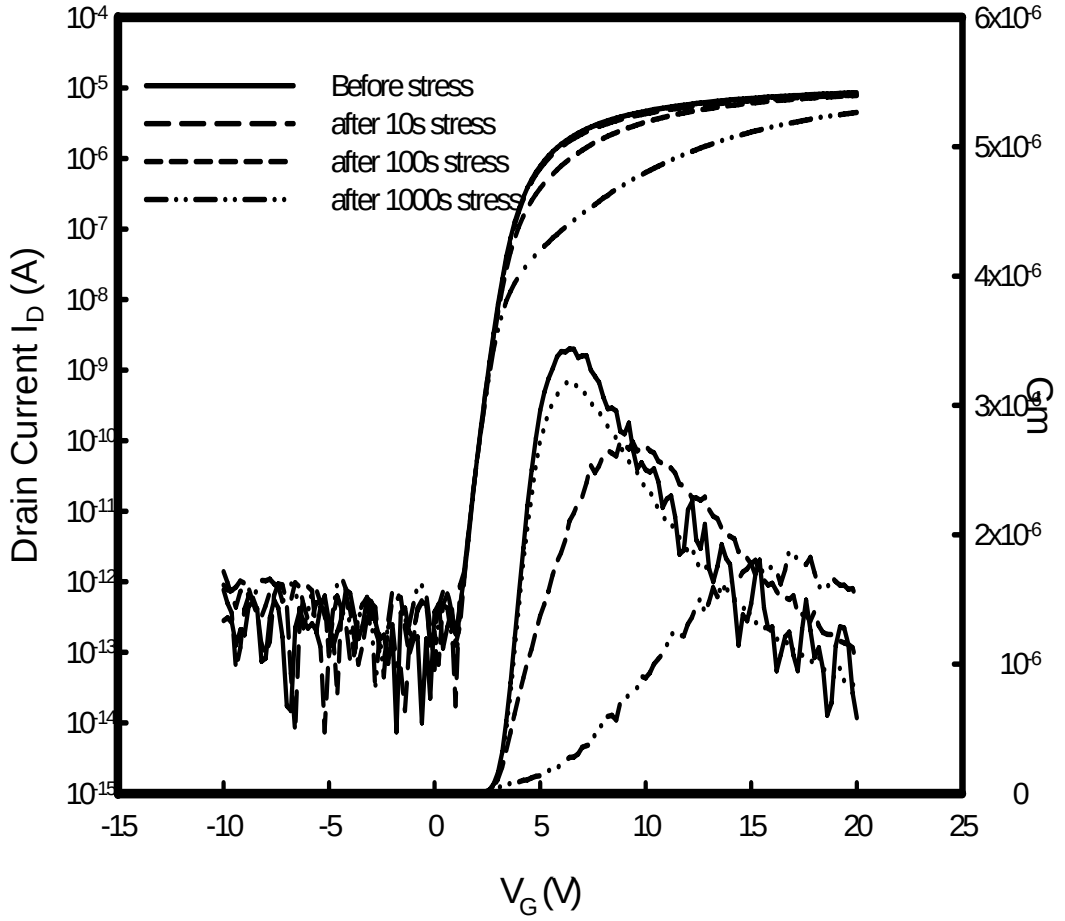


Fig. 4-9 The I_D-V_G relations of GB TFT with the dynamic stress times for 10 to 1000 s. The mobility of GB TFT is decayed from 243 to 136.9 cm^2/Vsec after 1000s stress.

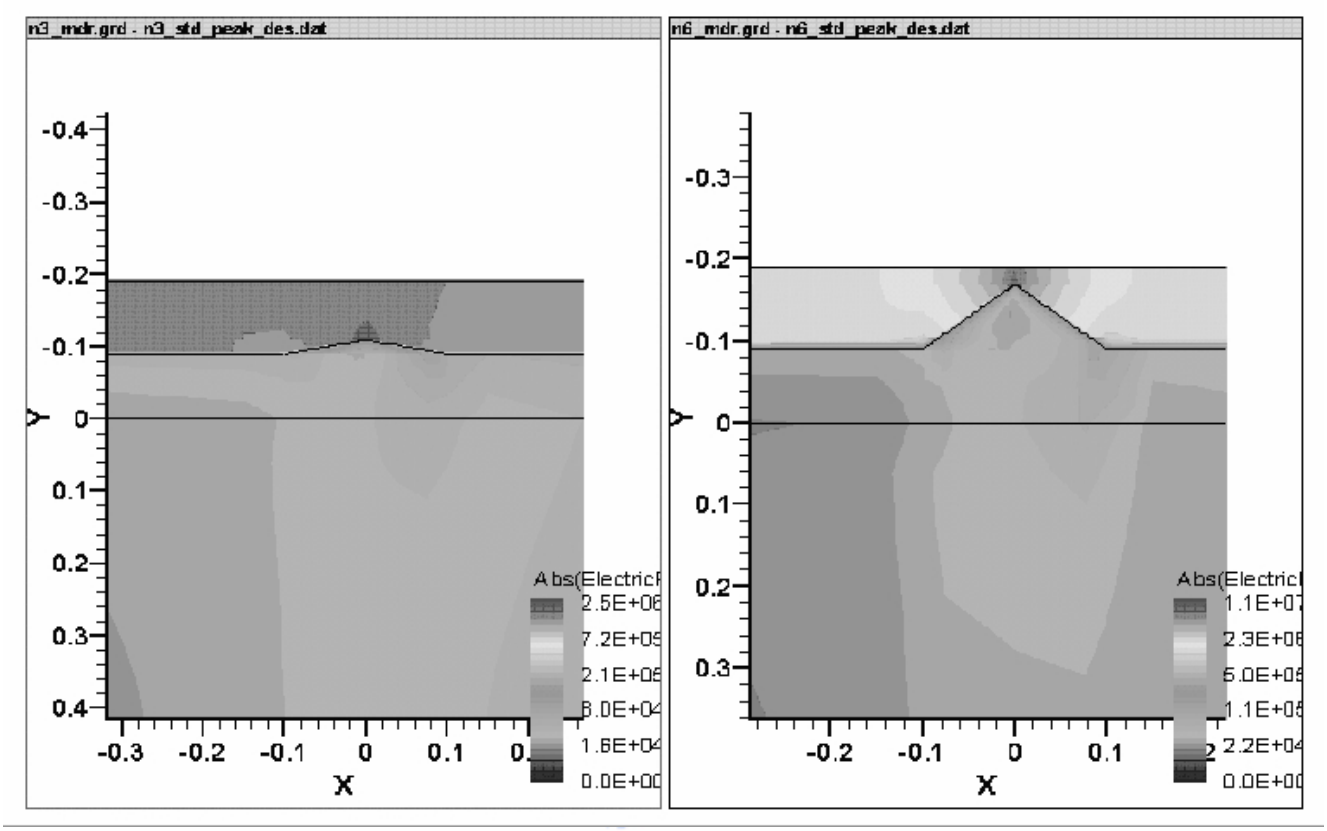


Fig. 4-10 The distribution of electrical field at (a) smooth plane and (b) the protrusion.

Chapter 5

Non-Volatile Memory Devices Fabricated on Glass Substrate Using Low Temperature Poly-Si Technology

5.1 Introduction

In the electrically erasable programmable read only memory (EEPROM) semiconductor device area, there are essentially two dominant technologies which compete for an ever-expanding world market: (1) floating gate EEPROM's and (2) SONOS (historically MNOS) or floating-trap EEPROM's. [5.1-5.5] In 1960's, the electronic industries urgently needed a new kind of memory device to replace the magnetic-core memory due to the high cost, large volume, and high power consumption of the magnetic-core memory. D. Kahng and S. M. Sze invented the floating-gate (FG) nonvolatile semiconductor memory at Bell Labs in 1967 [5.6]. To date, the stacked-gate FG device structure, continues to be the most prevailing nonvolatile-memory implementation, and is widely used in both standalone and embedded memories. The invention of FG memory impacts more than the replacement of magnetic-core memory, and creates a huge industry of portable electronic systems. The most widespread memory array organization is the so-called Flash memory, which has a byte-selectable write operation combined with a sector "flash" erase. However, once the tunnel oxide has been created a leaky path, all the stored charge in the floating gate will be lost. When the tunnel oxide is thinner for the first consideration, the retention characteristics may be degraded. And when the tunnel oxide is made thicker to take the isolation into account, the speed of the operation will be slower. Therefore, there is a tradeoff between speed and reliability

and the thickness of the tunnel oxide is compromised to about 8-11 nm, which is barely reduced over more than five successive generations of the industry.

To overcome the scaling limits of the conventional FG structure, SONOS [5.7-5.9] nonvolatile memory device is mostly mentioned candidate [5.10-5.12]. The nitride layer is used as the charge-trapping element, as for SONOS in Fig. 5-2. The intrinsic distributed storage takes an advantage of the SONOS device over the FG device, its improved endurance, since a single defect will not cause the discharge of the memory. There are a number of applications for SONOS NVSMs, with particular emphasis on "drop-in" modules for the application-specific integrated circuits (ASICs) such as wireless application, embedded NVSM in microcontrollers, and the so-called smart cards. [5.13-5.14] Future smart cars in public transport schemes will be operated using RF data transmission without the need for external contacts and power supplies. SONOS NVSMs may be employed in mobile computing systems such as handheld PCs and notebook and subnotebook PCs; digital still picture cameras; smart digital phones; data acquisition systems for industry, commerce, and military; audio recorders; GPS systems for automobiles, ships, and planes; and communication equipments, including cellular base stations, PBS equipment, and digital routing switches. In addition, it is attractive to fabricate the non-volatile memory devices on insulator substrates, such as glass ones. Smart cards which embed the memory cells may be manufactured using glass substrate for low cost. Moreover, the integration of systems on flat panels using low-temperature poly-silicon technology has been attractive. The high performance of poly-Si TFT processes enables the monolithic integration of analogue and digital display driver circuits as well as other peripheral functions on the active matrix substrate. The degree of circuit integration will continue to increase as device characteristics improve further. In the future, system on panel will be implanted with the advanced poly-Si technology. The nonvolatile

memories devices fabricated on the glass can increase the flexibility of circuits for the display. The previously reported poly-Si TFT EEPROM's using low-temperature poly-Si TFT is composed of two active regions of poly-Si layer[5.15-5.17]. The area of memory device is an important consideration for the high density memory manufacture. In this chapter, we demonstrate two non-volatile memory devices, (1) floating gate EEPROM's and (2) MONOS EEPROM's. The devices were fabricated using a low-temperature poly-Si technology with good characters. The maximum temperature of processing is below 650^{o}C for the glass substrate. We used the metal layer as the floating gate for the EEPROMs. Similar to the silicon/oxide/nitride/oxide/silicon (SONOS) devices in Si technology, the oxide-nitride-oxide (ONO) stack plays as the tunneling oxide/charge storage layer/control oxide. Moreover, the area of this non-volatile memory device is half the prior poly-Si TFT EEPROM. The memory characteristics and reliabilities had also been investigated in this chapter.

5.2 Device Fabrication

5.2.1 Floating-Gate EEPROM

Figs. 5-1(a) show the schematics of the planar poly-Si TFT EEPROM's using p-channel poly-Si TFT's as the control gate electrode in this study. To fabricate poly-Si TFT EEPROM's, an active amorphous silicon film (a-Si) of 100 nm thickness was deposited by plasma enhanced chemical vapor deposition (PECVD). Subsequently, the films were dehydrogenated by furnace annealing. After dehydrogenation, the a-Si films were crystallized by excimer laser annealing process. Following the laser process, 15nm-thick gate oxide was deposited by PECVD. Then the implantation was adopted to define the source/drain (S/D) region. Then an

annealing process was performed to activate the dopant impurities. Mo was sputtered and defined as a floating gate metal of T1 and T2. Then 200nm block oxide was formed by PECVD. The dimensions of T1 in this work were L=6μm, W=16μm and the overlap of gate metal and S/D junction is 1μm. In addition, the length and width of T2 is 6 and 16μm, respectively. To investigate the influence of overlap area of floating gate and S/D in T2, two memory cells A and B were made. The device A is illustrated in Fig. 5-1(b), and overlap length of floating gate and S/D in T2 is 1μm. The T2 region of device B, control gate, is wholly doped with boron of 10^{19} atom/cm^3, as shown in Fig. 5-1(c).

5.2.2 MONOS EEPROM

Figure 5-2(a) shows the MONOS (Metal/Oxide/Nitride/Oxide/Poly-Si) type flash memory. It was fabricated on glass substrate by low temperature poly-silicon processes. Buffer SiO_2 films and 50nm-thick amorphous silicon (a-Si) films were deposited by plasma enhance chemical vapor deposition (PECVD), and subsequently, the films were dehydrogenated by furnace annealing. After dehydrogenation, the a-Si films were crystallized by Excimer Laser Annealing process. The ONO stack structure is formed with 15nm tunnel oxide, 25nm trapping nitride, and 30nm blocking oxide by PECVD. The blocking oxide is utilized to prevent the carriers of the gate electrode from injecting into the charge trapping layer by F-N tunneling. MoW was sputtered as a gate metal and ion doping was used to form source and drain regions. The dimension of MONOS type memory device in this study are W=8μm and L=8μm. The overlap of gate metal and n+ doping is 1μm. Figure 5-2(b) shows the Transmission Electron Microscope (TEM) cross-section of ONO on the poly-Si surface.

5.3Results and Discussions

5.3.1 Floating-Gate EEPROM

Figure 5-3(a) shows the comparison of I_D-V_G relations at V_D=0.1 between the memory devices, A and B. The on-current of device B is 1.09 times the device A at gate bias of 6V. The gate voltage dropped on T1 is proportional to the capacitance ratio, W_2L_2/W_1L_1. Although the areas of T2 in both devices A and B are the same, the device B owns the larger on-current than device A. We can infer that the larger voltage coupled on T1 in the device B since its control gate, T2, is a good conductivity sheet that could efficiently couple the applied gate bias to T1. Figure 5-3(b) shows, respectively, the I_D-V_G relations of the memory device A and B after electrical programming with the gate bias of 18V and erasing with 22V for 10ms. The programming and erasing were performed through the *Fowler-Nordheim* (F-N) tunneling over the entire channel region and at the gate/p^+ overlap region. The transfer characteristics of devices were measured at room temperature with V_D=0.1V, when the gate voltage varied from 0V to 6V. The threshold voltage is defined according to the criteria $I_D=(W/L)\times10^{-8}$ A at V_D=0.1 V. The memory window of device A and B was respectively 4V and 4.8 V under the mentioned programming condition, as illustrated in Fig. 5-3(b). This phenomenon consists with the I_D-V_G relations depicted in Fig. 5-3(a). The lager voltage shift of device B should be contributed by the higher coupled voltage dropped on T1. In addition, it was found that the sub-threshold swing and the mobility kept well during the program and erase operation. We can infer that threshold voltage shift is due to captured charges in the floating gate, not due to the device degradation.

Fig. 5-4 shows the effects of the gate voltage on the programming and erasing

characteristics of poly-Si TFT EEPROM's. The voltage shift of the memory devices is a function of programming time at a fixed gate bias. Both devices exhibit higher efficient programming characteristics at a higher program/erase voltage. The magnitude of voltage shift tends to be saturate with the raising of the programming time. We can find that the device B usually owns lager voltage shift than the device A with the same programming condition. However, the erasing characteristics of the two devices are similar.

Figure 5-5 exhibits the endurance characteristics, after different program/erase (P/E) cycles, of the device B. The P/E of the memory devices can be achieved by applying negative (18V) and positive (-22V) voltage pulses, respectively. It can be seen that the threshold voltage window initially has about 2V at P/E time of 10^{-2} sec. As the number of the P/E cycles increased, the decay in the magnitude of memory window was observed. The floating type memory device maintains a wide threshold voltage window of 1.1V after 10^4 P/E cycles. The difference of threshold voltage, 1.1 V, is large enough for a logic memory circuit. In Fig. 5-6, the threshold-voltage shift is measured with different periods of time when the sample is heated at 60^{o}C. It is found that the proposed device retains a good retention property without a significant decline of the memory window, ΔV_t, up to 60 hours.

5.3.2 MONOS EEPROM

Figure 5-7 shows the I_D-V_G relations of the poly-Si MONOS memory device after electrical programming with the gate bias of 20V for 10 ms. The programming and erasing were performed through the *Fowler-Nordheim* (F-N) tunneling over the entire channel region and at the gate/n^+ overlap region. The transfer characteristics of devices were measured at room temperature with V_D=0.1V, when the gate voltage varied from -5V to +15V. The threshold voltage is defined according to the criteria

$I_D=(W/L)\times10^{-8}$ A at V_D=0.1 V. The threshold voltage shift of device was 1.5V under the mentioned operation, as illustrated in Fig. 2. In addition, it is found that the sub-threshold swing (0.54 dec/V) and the mobility (63.2 cm^2/Vsec) keep well during the program and erase operation. We can infer that threshold voltage shift is due to captured charges in the nitride, not due to the device degradation.

There are two kinds of programming methods for the electrical operation of the non-volatile memories, F-N tunneling and channel hot electron (CHE) injection. [5.18-5.20] Fig. 5-8 illustrates the I_D-V_G relations and linear transconductance, gm, of the device which were programmed by CHE method with the drain bias of 35V and 45V at V_G=25V, respectively. It was observed the distinct degradation in electrical characteristics of poly-Si memory device. The ON-current of the devices programmed using 35V and 40V drain bias at V_G=25V was decayed to 18.5% and 5% of the initial value of the device, respectively. As poly-Si TFTs are biased in the saturation region at large drain voltages, the electric field at the drain end is rather large and generation of electron-hole pairs by impact ionization occurs. CHE method is providing electrons with high energy to pass from the channel into the charge storage layer, SiN_x, which means a high voltage differential between the drain and the control gate. However, partial transporting electrons have enough energy across the tunneling oxide. Meanwhile, the avalanche breakdown is occurring near the drain. Indeed, the poly-Si TFT fabricated on the glass substrate owns the parasitic bipolar transistors (PBT) action that leads to the kink effect, similarly to SOI-devices. This added drain current augments the impact ionization, which in turn drives the floating body harder, thereby causing a regenerative action leading to a premature breakdown. We note that when bias-stressing the device in the kink effect regime (V_{DS}>V_G), impact ionization substantially increases the supply of hot-carriers, leading to a simultaneous injection

into the gate oxide of both hot-holes and hot electrons. The degradation is believed to be mainly contributed by the creation of traps at the interface between the gate oxide and poly-Si layer. The gate oxide of the memory device in this study was deposited using PECVD and inferior than the thermally grown oxide on silicon wafer at high temperature. For low-temperature poly-Si TFT devices, the traps of grain boundaries in the channel play a significant role on the electrical properties. The avalanche multiplication effects in poly-Si TFT is enhanced by the floating substrate. For the nature of poly-Si film, the channel hot electron injection is not suitable for the programming, as shown in Fig. 5-8. F-N tunneling occurring either in the gate/drain overlap region or at the channel region is more suitable for the poly-Si memory devices.

Figure 5-9 exhibits the endurance characteristics, after different program/erase cycles, of the MONOS memory device. The program/erase (P/E) of the memory devices can be achieved by applying positive (+20V) and negative (-40V) voltage pulses, respectively. It can be seen that the threshold voltage window has 1.5V at P/E time of 10^{-2} sec. The difference of threshold voltage, 1.5 V, is large enough for a logic memory circuit. The MONOS type memory device maintains a wide threshold voltage window after 10^4 P/E cycles. However, the device shows some degradation after higher 10^4 P/E circles. The threshold voltage shift up-ward is due to the creation of interface state and the charges trapping in the tunneling oxide. The threshold voltage is depend on the oxide charge and the deep states in the poly-Si film.

In Fig. 5-10, the threshold-voltage shift is measured with different periods of time when the sample is heated at 60 ℃. It is found that the ONO stack retains a good retention property without a significant decline of the memory window, ΔV_t, up to 50 hours, which is robust in the Flash nonvolatile memory technology.

5.4 Conclusions

The characterizations of the non-volatile memory devices fabricated on glass using low-temperature poly-silicon technology were studied. The maximum temperature of processing is below 650^{o}C for the glass substrate. The floating-gate memory device consists of two active regions of poly-Si layer, one behaves as the control gate and the other is the conducting channel region. The device whose control-gate is made of whole heavily-doped poly-Si sheet owns lager on-current and memory windows than the device whose control-gate is a common transistor. In the proposed structure, the applied bias could efficiently couple to the channel. For 10 ms P/E pulse time, the threshold voltage window is 2V for the memory device and it maintains a wide threshold voltage window after 10^4 P/E cycle.

In addition, the characterizations of MONOS type memory on glass using LTPS-TFT with an oxide-nitride-oxide (ONO) stack structure were studied. For 10 ms P/E pulse time, the threshold voltage window is 1.5V for the memory device and it maintains a wide threshold voltage window after 10^4 P/E cycle. The proper operation method for poly-Si memory device is F-N tunneling since a serious degradation in electrical characteristics was found with the CHE programming method.

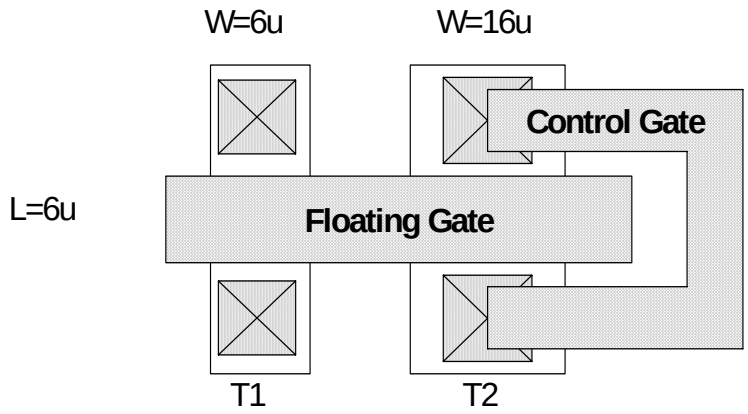
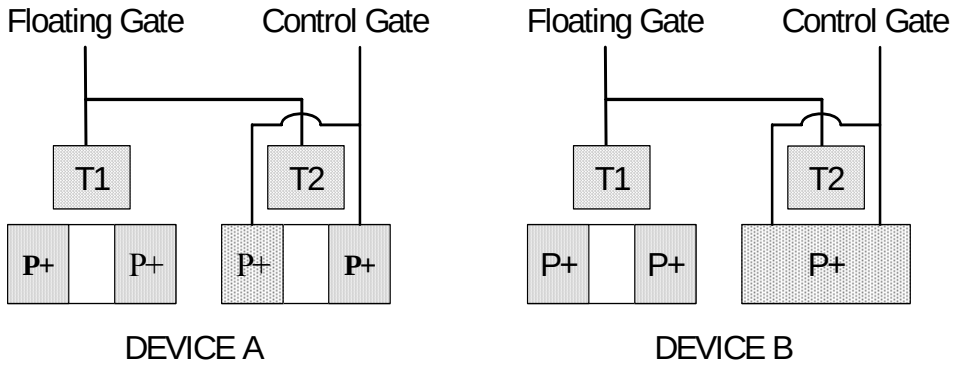
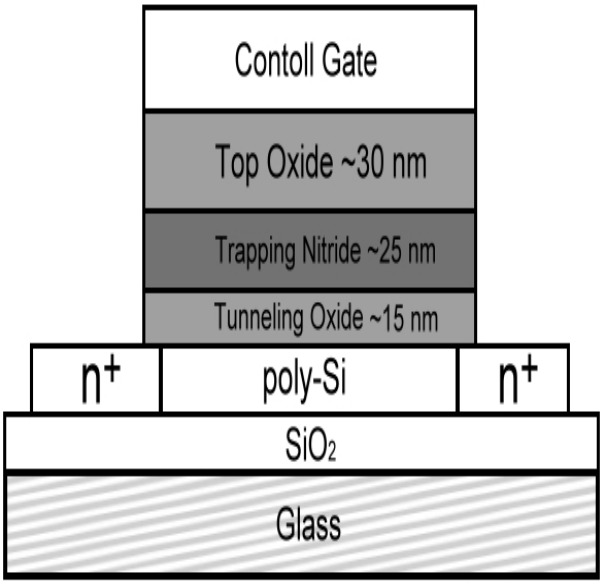


Fig. 5-1 (a)

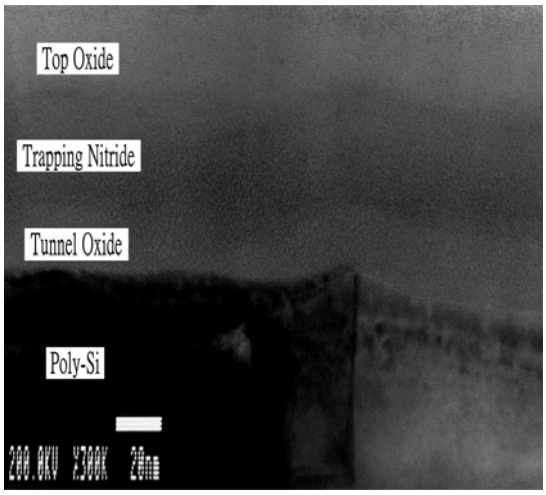


(b) (c)

Fig. 5-1 (a) The planar view of the poly-Si TFT EEPROM which is composed of two active regions, T1 and T2, of poly-Si layer. (b) The cross section of the device A (c) The cross section of the device B. The T2 region of device B, control gate, is wholly doped with heavy dose of boron.

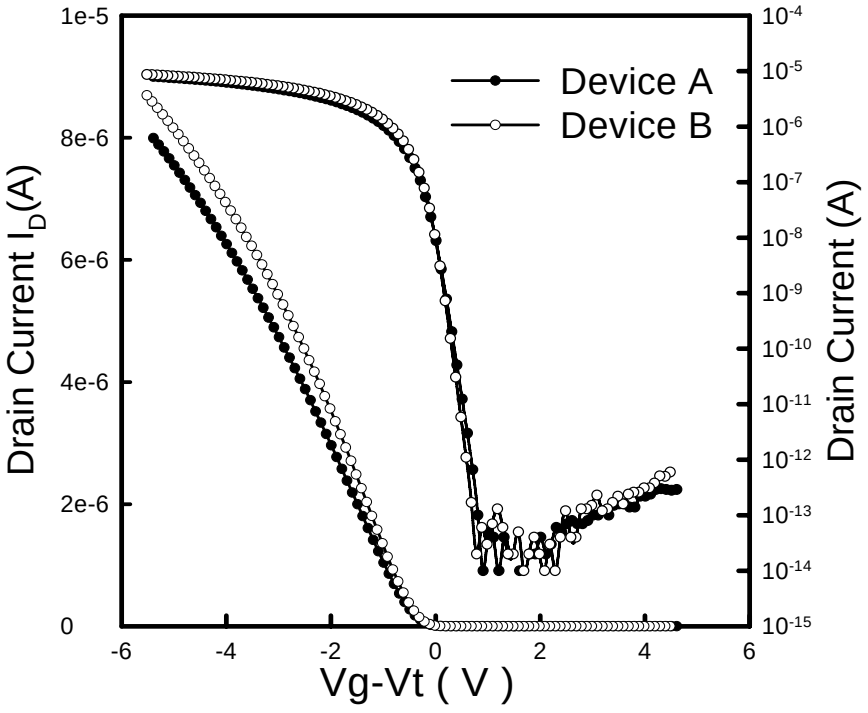


(a)

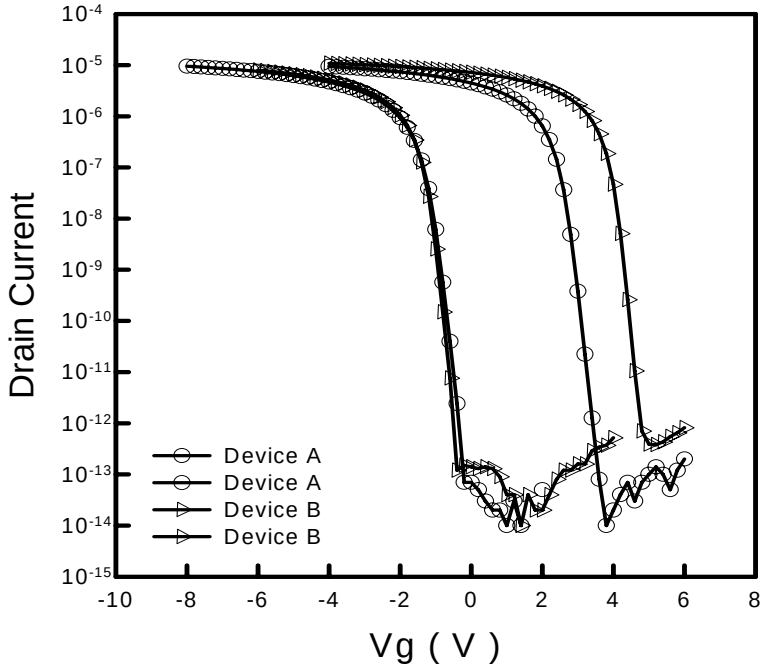


(b)

Fig. 5-2 (a) The scheme of MONOS (Metal/Oxide/Nitride/Oxide/Poly-Si) type flash memory. (b) The Transmission Electron Microscope (TEM) cross-section of ONO on the poly-Si surface.



(a)



(b)

Fig. 5-3 (a) The comparison of I_D-V_G relations at V_D=0.1 between the memory devices, A and B. (b) The I_D-V_G relations of the memory device A and B after electrical programming with the gate bias of 18V and erasing with 22V for 10ms.

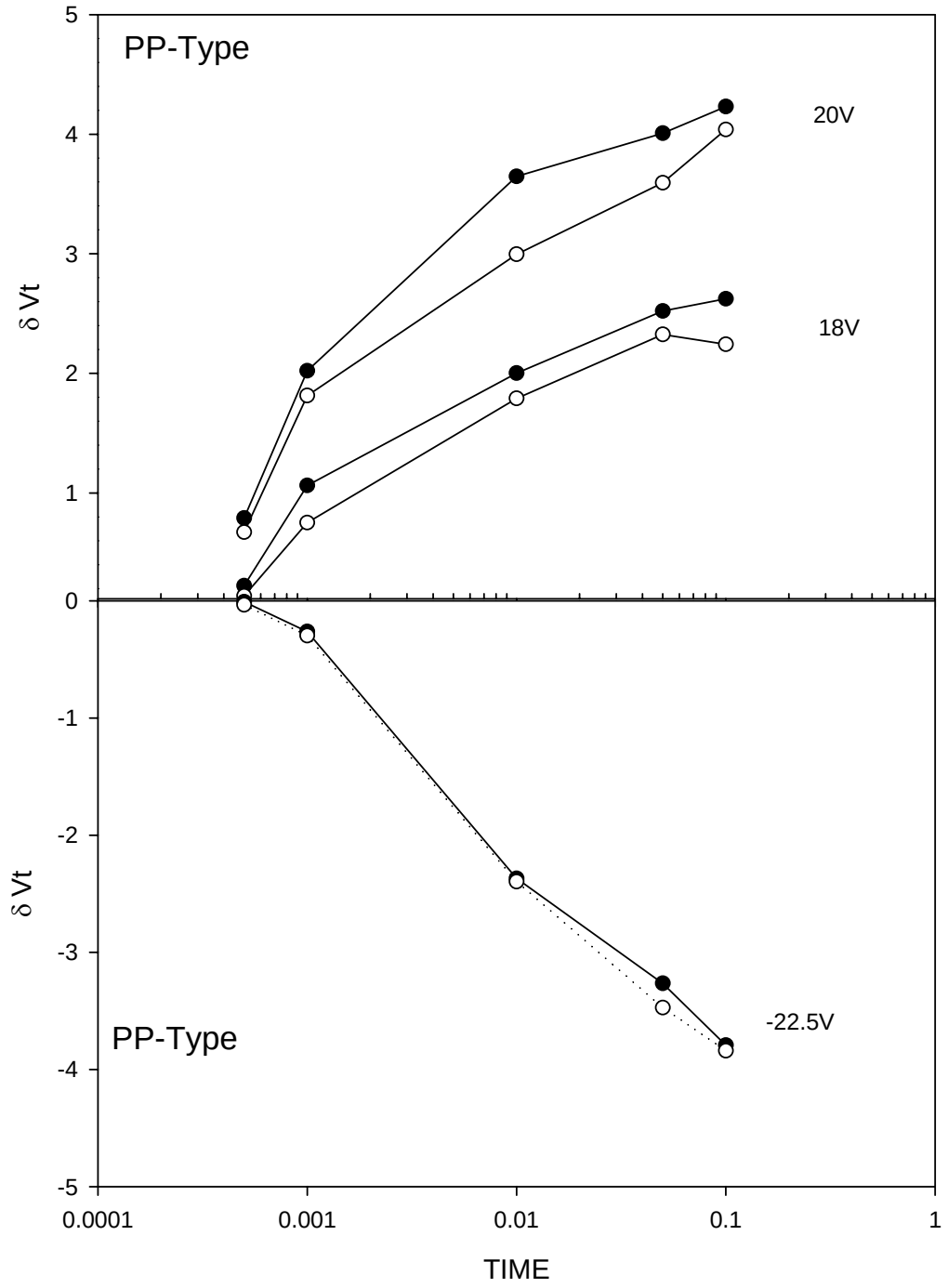


Fig. 5-4 The effects of the gate voltage on the programming and erasing characteristics of poly-Si TFT EEPROM's. The magnitude of voltage shift tends to be saturate with the raising of the programming time.

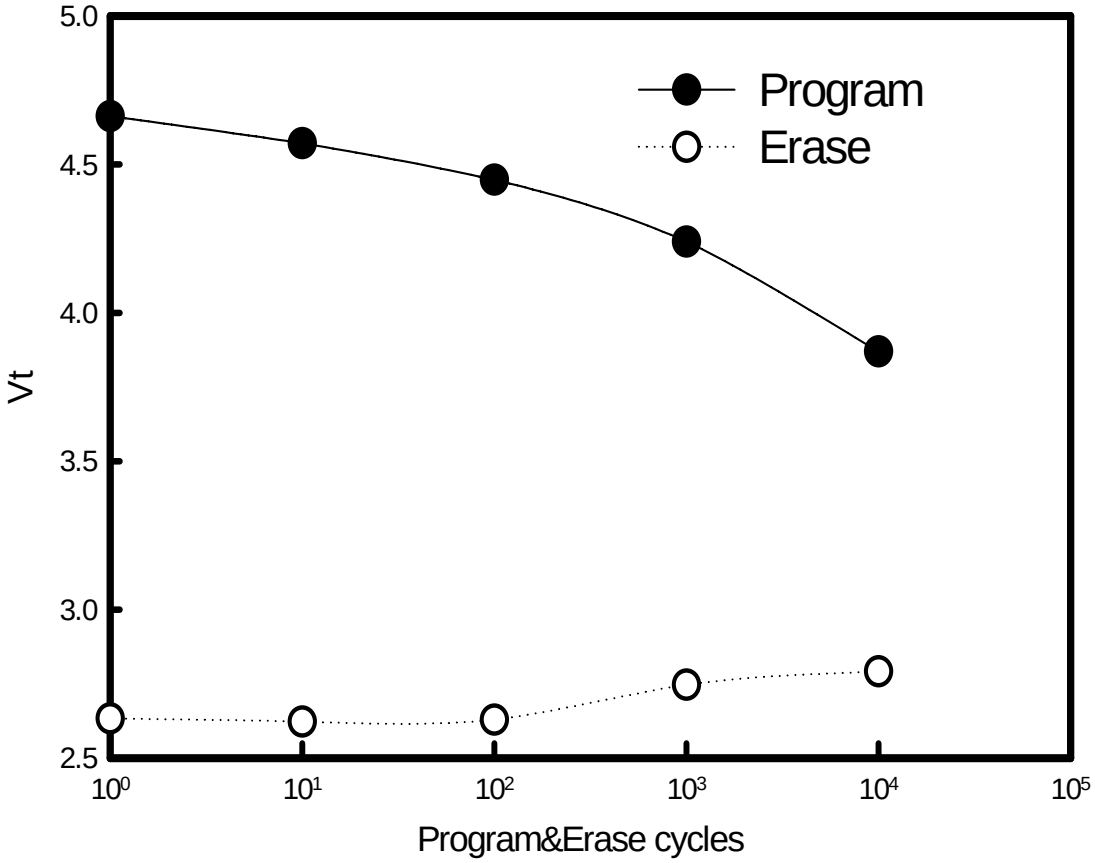


Fig. 5-5 The endurance characteristics, after different program/erase (P/E) cycles, of the device B. The P/E of the memory devices was performed by applying negative (18V) and positive (-22V) voltage pulses, respectively.

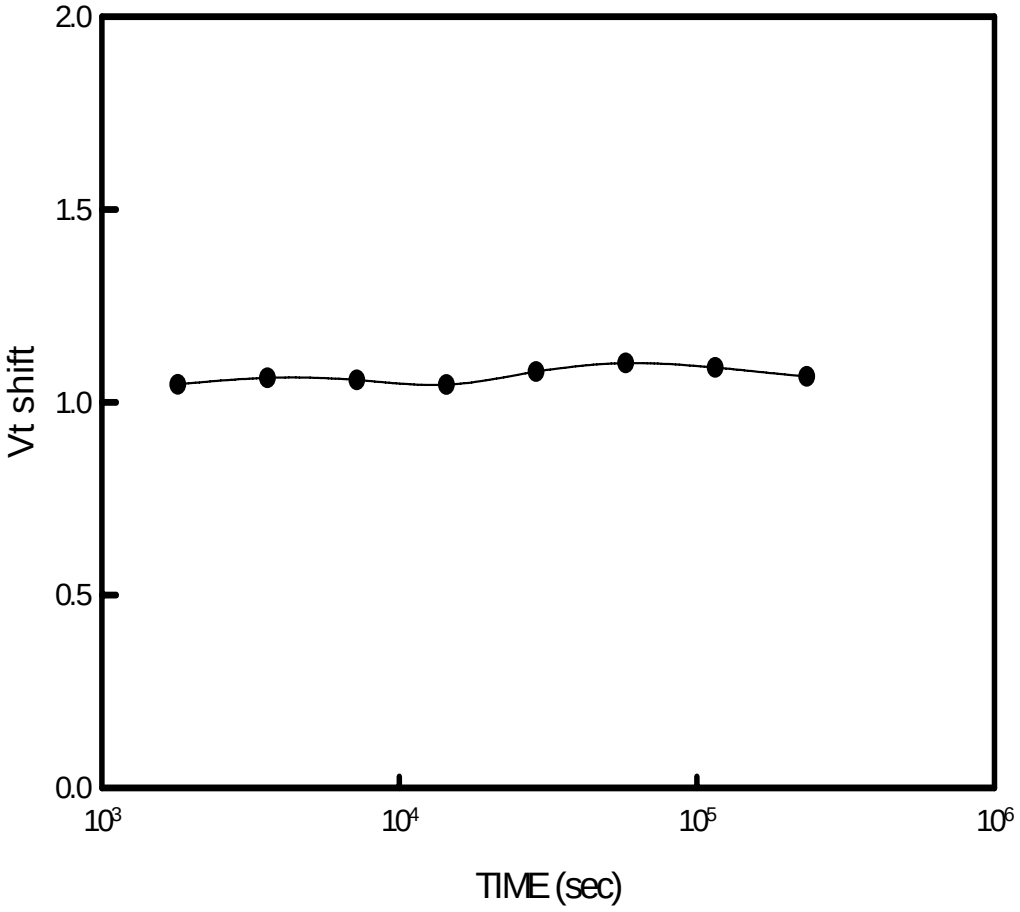


Fig. 5-6 The threshold-voltage shift is measured with different periods of time when the sample is heated at 60°C.

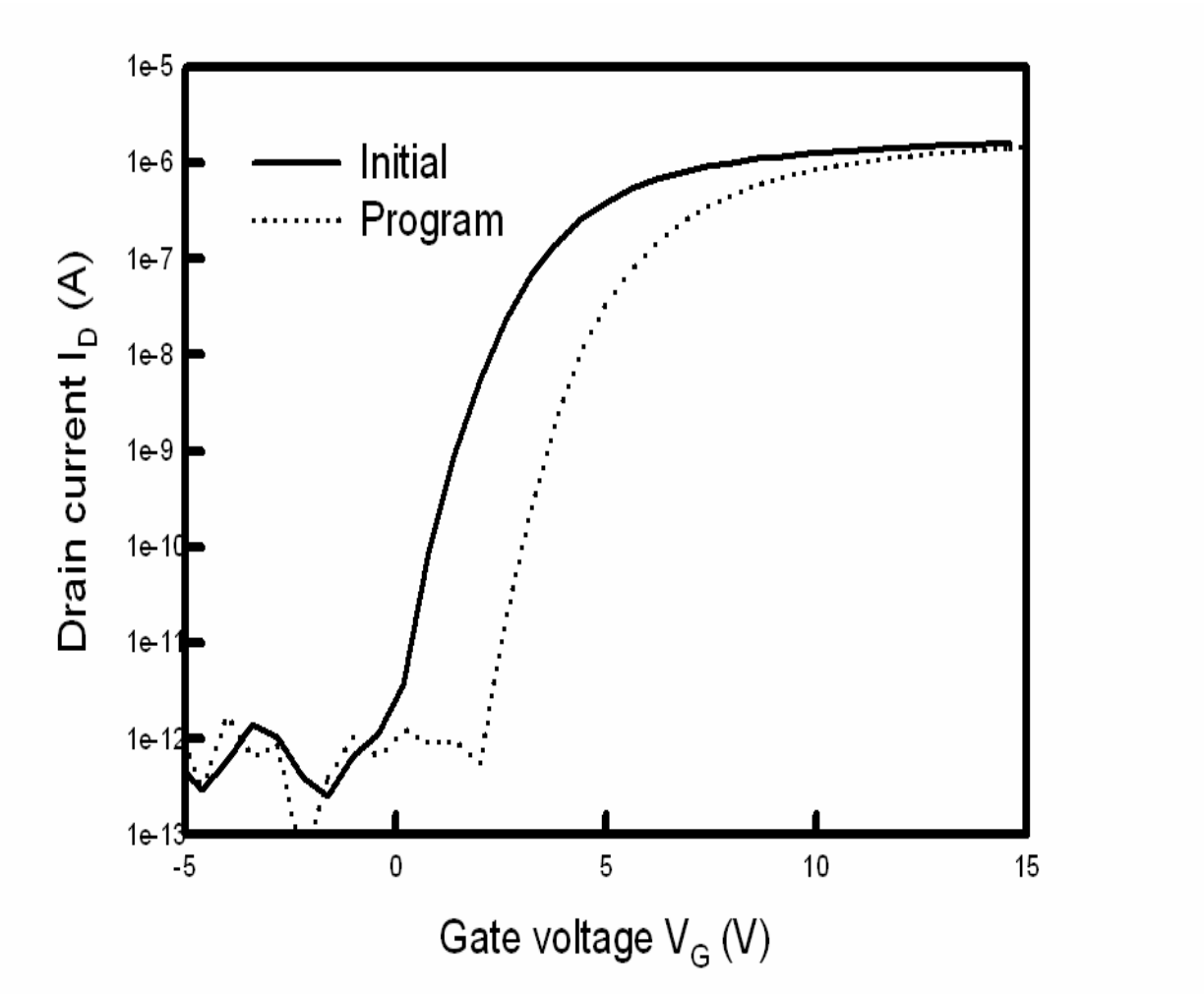


Fig. 5-7 The I_D-V_G relations of the poly-Si MONOS memory device after electrical programming with the gate bias of 20V for 10 ms.

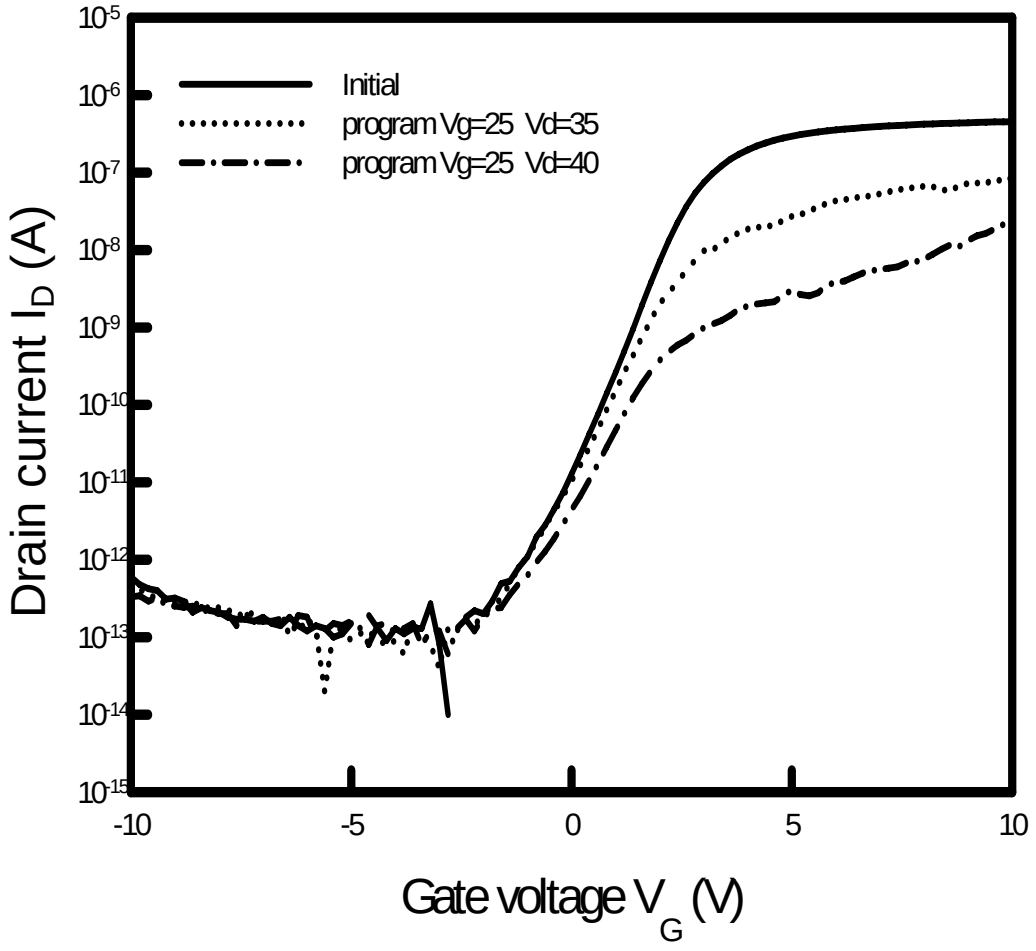


Fig. 5-8 The I_D-V_G relations and linear transconductance gm of the device were after programming using CHE method with the drain bias of 35V and 45V at V_G=25V, respectively.

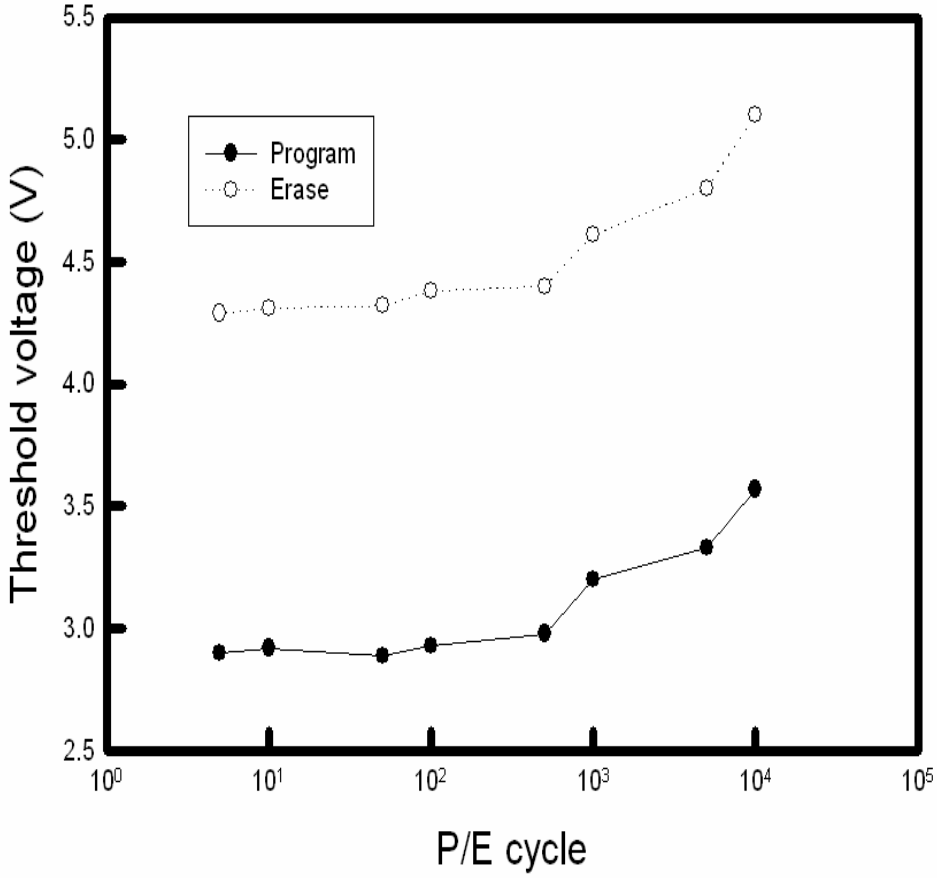


Fig. 5-9 The endurance characteristics, after different program/erase cycles, of the MONOS memory device. The program/erase (P/E) of the memory devices can be achieved by applying positive (+20V) and negative (-40V) voltage pulses, respectively.

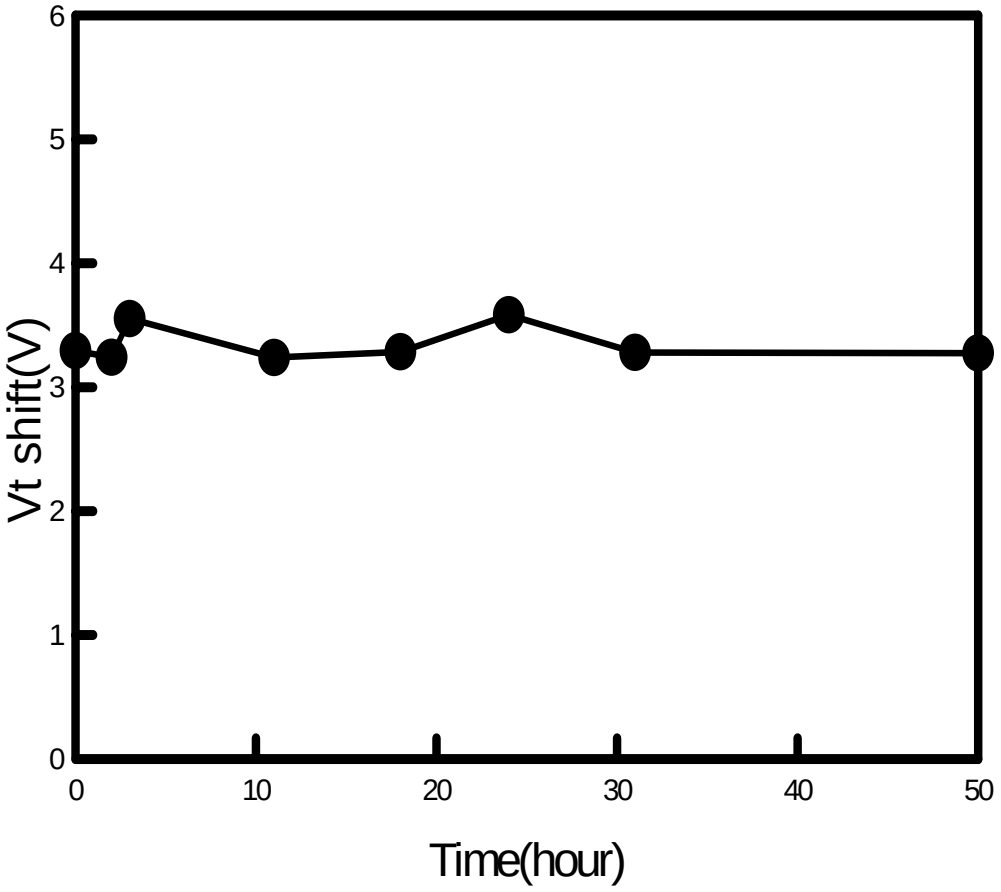


Fig. 5-10 The threshold-voltage shift is measured with different periods of time when the sample is heated at 60℃.

Chapter 6

Investigation of the Nano-Porous Silica for Interconnections with Low-RC Delay

6.1 Introduction

The interconnections with low-RC delay are very attractive in integrated circuits (IC) and large-size AMLCD. [6.1-6.5] Some research reports have shown that the gate pulse delay is getting serious with the increasing of the size of large area AMLCD. [6.6-6.7] The resistance and capacitance (RC) delay of the gate line retards the turnoff of the transistor at the far end of the gate line. The decay of data signal is increased with the increasing of RC value. Thus, low resistivity gate metals are required for large-area AMLCD's. In order to minimize the resistance time capacitance (RC) delay, two approaches can be taken. The first approach is to reduce the resistance part of the RC delay by using low resistivity as the conductor for interconnects. The second approach is to reduce the coupling capacitance between the metal lines and this requires a dielectric material with as low dielectric constant as possible. Manufacturers are beginning to use aluminum (Al) and its alloys, but copper (Cu) is an attractive alternative because of its reliability against hillock formation. [6.8-6.10] However, copper has a resistivity of 1.7 μΩ-cm, which is much lower than that of Al-alloy with a resistivity close to 2.7 μΩ-cm. Additionally, Cu wirings won better electron-migration resistance over current Aluminum (Al) alloys. [6.11-6.14]

The coupling capacitance resulting from pixel electrode and the data and gate line would lead to the cross-talk and signal distortion. To minimize the coupling

capacitance, the low-k materials should be introduced into the interconnection of flat panel display. [6.15-6.16] Also, the implantation of low-k in display can achieve a high aperture ratio for improved light transmittance or image quality. This requires a thick, low dielectric constant (k) material as an inter-level dielectric. In the high-transmittance pixel structure, as shown in Fig. 1-3, the pixel electrodes need to be extended to, and even overlapped with the gate and data signal lines to maximize the aperture ratio. The passivation layer, located between the pixel electrode and the data electrode, must then provide sufficiently low parasitic capacitance and good insulation to reduce crosstalk and signal distortion. The conventional silicon nitride (a-SiN) passivation layer is not suitable for this structure due to its relatively high dielectric constant, slow deposition rate and high residual stress. Efforts have been made to utilize organic insulators as a passivation layer. However, the TFTs having organic passivation often show a high contact resistance between the pixel and the data electrodes, because of the sputter-deposits of the organic material during the subsequent processes. Therefore, an inorganic alternative is desired, which can utilize the same equipments and process flow as the conventional SiN. Silicon carbon-oxide (a-SiCOH) films show a remarkably low dielectric constant and high deposition rate, and has been drawing attention as a good candidate for interlayer dielectrics. [6.17]

The porous materials should catch more attention with the ultra low dielectric constant in the 1.1-2.2 range. In principle, the porous dielectric candidates can be divided roughly into general classes: (i) porous-like materials and (ii) porous organic polymers. Each class of materials has its own potential and weakness. Silicate-like materials show exceptional thermal stability and acceptable electrical properties but often mechanically weak and prone to cracking. On the other hand, high temperature organic polymers are usually mechanically tough but are thermally less robust than the inorganic alternatives. Among various porous low-k dielectrics, nanoporous

organosilica glasses (POSGs) are receiving much attention on ILD applications in IC field [6.18-6.20]. They may be applied on the ICs and high-transmission LTPS AMLCD panel. [6.17]Their adjustable dielectric properties make the nanoporous silicate suitable for different applications. Nevertheless, the adoption of POSGs encounters difficulties due to their large internal surfaces. The high porosity in their structures tends to adsorbing environmental contaminants such as moisture [6.21]. The weak resistance of porous low-k against the reactive plasma and stripper is troublesome for integration with Cu. Comparing with SiO2 or SiN deposited by PECVD, POSG was low density and sensitive due to its high porosity and high surface/volume ratio.The resultant electrical degradation of organosilicate-based porous materials has been proposed in previous researches [6.22-6.23].

In this chapter, the characteristics of intrinsic porous silica (POSG) (k=1.9) were demonstrated. Moreover, the stability of POSG films containing moisture was investigated.

6.2 Experimental procedures

Methyl silsesquioxane resin as the matrix material, which is low molecular weight with a large number of $Si(OH)_x$ and $Si(OC_2H_5)_x$ (x=1-4) groups, was formulated to 30 wt.% solids in a carrier solvent of methylisobutylketone. Poly(methylmethacrylate) polymers (PMMA) with 20 wt.% loading, working as foaming agents, were subsequently added in the MSSQ matrix material to ultimately produce porous organosilicates. As most of PMMA polymers were compatible with MSSQ, a uniform precursor solution of the mixture was obtained immediately. For fabricating porous organosilicate films, the precursor solution was first spin-coated onto 6-in. p-type wafers with (100) orientation. The first-stage spin rate was 450 rpm for 4 s and the second 3000 rpm for 30 s, respectively. The resultant wafers were transferred to a quartz furnace and heated up from room temperature to 400^{o}C at a

ramping rate of 20℃/min. A thermal curing process was then proceeding at 425 °C for 1 h under nitrogen atmosphere, and further forming the POSG films with a thickness of 500 nm.

The relation between residual stresses versus temperatures up to 360℃ was measured by the wafer curvature method [6.14] at a TENCOR thin-film stress measure system. Also, the films were characterized by Fourier transform infrared spectroscopy (FTIR). The refractive index and thickness of the porous silica film were measured with an n&k analyzer. The infrared spectrometry was performed from 4000 to 400 cm^{-1} using a Fourier transform infrared (FTIR) spectrometer calibrated to an unprocessed wafer, for determining the chemical structure of the porous organosilicate (POSG) films.

Electrical characterization was performed on metal-insulator-semiconductor (MIS) structure formed on the p-type heavy doped silicon wafer with a resistivity of 0.01-0.02 cm^{-1}. POSG film of about 800 nm was deposited as an insulator. Aluminum and copper electrodes were evaporated/copper electrodes were separately sputtered on the front surface of the films and aluminum were evaporated on the back surface of the substrate. The area of the gate electrode was 0.00528 cm^2 for C-V analysis. MIS capacitors were used for the determination and evaluation of the permittivity of porous silica films where the dielectric measurements were done by HP-4284 meter. The capacitor was measured at 1 MHz with an AC bias. And current-voltage (I-V) characteristics were also measured using MIS structure with HP-4156C meter. The area of the gate electrode was 0.001244 cm^2 for I-V analysis.

6.3 Results and discussions

Figure 6-1 shows FTIR spectra variation of as-spun porous organosilicate glass

(POSG) after undergoing a series of thermal process. The peak intensity of the Si-OH + H_2O (~3400 cm^{-1}) decrease after a series of thermal process due to the gelation reaction of Si-OH groups. The Si-OH groups in each methyl silicone resins easily react with another Si-OH groups in another methyl silicone resins during gelation. Consequently, many methyl silicone resins can condense each other so that the POSG structure can form three-dimensional (3D) network structure, as shown in figure 6-2. The functional groups in POSG film such as Si-O cage-like group (1144 cm^{-1}), Si-O network group (1049 cm^{-1}), Si-C groups (847, 1277 cm^{-1}) and C-H group (2980 cm^{-1}) are appeared in the FTIR spectra, and these functional groups are similar to that of MSQ film.[6.18-6.23]

As compared with dense dielectric film, porous dielectric film has larger surface, which easily causes moisture uptake in the nanopore surface of POSG film. In order to understand the effect of moisture absorption on porous material, POSG film is further dipped in hot water at 85℃ to carry out the moisture-absorption test. The moisture-absorption test can help us to realize the effect of physical moisture absorption on the POSG film. It is found that the thickness, stress and FTIR spectra have no obvious change after POSG film is dipped in hot water at 85^{o}C for 3 hr. Then, when hot water-dipped POSG comes through 300^{o}C annealing to desorb moisture, the thickness and stress almost maintain at the original values and the intensities of functional groups in FTIR spectra still keep at high levels, as shown in Figs 6-3 to 6-5. Since the POSG possesses superior thermal stability until 550℃, the dipping at 85℃ shall not result in the damage of POSG structure, which consists with the experimental results of material analyses (Figs 6-3 to 6-5). Nevertheless, a little content of moisture absorption in POSG film easily leads to a significant increase of leakage current, although a trace content of moisture is difficult to detect by utilizing material analyses. Figure 6-6 shows that the leakage currents of POSG increase with

the increase of hot water dipping time, whereas the leakage currents decrease obviously after water-dipped POSG film (for 3 hr) undergoes 300℃ furnace annealing. The increase of leakage current is attributed to the fact that the moisture absorption occurs when POSG film undergoes hot water dipping. However, since the moisture can be desorbed from POSG film after 300℃ furnace annealing, the leakage currents of water-dipped POSG film will be decreased. In addition, owing to moisture uptake, the dielectric constant slightly increases with the increase of hot water-dipping time. After the slight moisture is eliminated by utilizing 300℃ furnace annealing, the dielectric constant is reduce to the original value. These results indicate that the moisture uptake in the POSG easily leads to a significant increase of leakage current even though the moisture content of the POSG is very slight.

Bias-temperature stress is usually employed to estimate the stabilities of dielectrics. Application of positive bias on gate of MIS is the most common method to drive the metal ions through the insulator from the metal gate electrode. Also, sampling the dielectrics under high electric field at high temperature could accelerate the metal penetration and dielectric breakdown. However, the ultra large surface area of POSG leads to the moisture absorption resulting the increasing of leakage current in dielectric properties. To observe the moisture-induced degradation on stability, the POSG were stressed with high electric filed at room temperature. It should be noted that the moisture would tend to vaporize from the POSG while the sample is heating beyond 100^{o}C in BST measurement. Fig. 6-7 shows the J-E relations of POSG samples at room temperature. The moisture-containing sample owns the larger leakage current that the STD sample which is moisture-free at the same bias. The thermal desorption spectra of moisture-containing and STD samples was illustrated in figure 6-8. The magnitude of H_2O signal (m/e=18) in moisture-containing sample is

larger than that of STD sample which is moisture-free. Two kinds of metal electrodes, Cu and Al, were employed to investigate the stability since the Cu an Al wiring are the potential candidates for IC and AMLCD applications. Fig. 6-9(a), 6-9(b) presents that the leakage current v.s. time (I-t) characteristics of Cu and Al-electrodes POSG during the bias stress at room temperature and 150^{o}C, respectively. We can find that the similar I-t relations of POSG samples are exhibited at 150^{o}C, even the Cu-gate sample. The leakage current of moisture-containing samples at 150^{o}C are lower than that at room temperature which is dominated by the ionic conduction. Moreover, the different I-t evolutions were demonstrated at the room temperature. The leakage current of Al-gate sample was slightly decreased and tended to saturate with the increasing of the stress time. By contrast, the magnitude of leakage current of Cu-gate sample was increased with the raising of stressing time at room temperature. Comparison with the stressing at 150^{o}C, we can infer that the moisture would enhance the Cu to ionize at the Cu/POSG interface. The Cu may react with moisture and then be oxidized to form CuO. CuO could be easily ionized into Cu ions by the applied field. Then the Cu ions are drift by the high electrical field toward the bottom electrode. The penetration of Cu ions in the POSG may cause the breaking of chemical bonding of POSG and increasing of the leakage current. Additionally, Cu ions existed in insulator are taken as the trapping centers and could enhance the carrier transport. The SIMS spectra was employed to observe the distributions of the metals in the POSG, as shown in Figs. 6-10(a) and (b). Both Al and Cu were observed to be existed in the corresponding POSG film. Nevertheless, the electrical behaviors of the Cu- and Al-electrode samples leakage current were obviously different. The Cu atoms existed in the oxide are usually considered as the trap-center. Although the Al atoms was detected in the stressed POSG film, the Al atoms which are easily oxidized to form AlO_x by the moisture in the POSG. AlO should be a good insulator than the

CuO. Also, the Al ions need more activation energy to ionize from the AlO than the Cu ions ionized from the CuO. According to the evolution of the leakage current, Al plays as an inactive role for the conduction of POSG.

6.4 Conclusions

The moisture-induced instability of POSG has been investigated in this chapter. The lager leakage current is observed in hot water dipped sample. However, there is no distinct change in the material characterizations of POSG even after 3hrs dipping. Thermal desorption spectra evidenced that the moisture really existed in the leaky sample. The leakage current would be increased and dominated by the ionic conduction as the moisture is contained in the POSG. Additionally, the moisture would enhance the Cu ions to penetrate into POSG and cause the raise of the leakage cuurent.

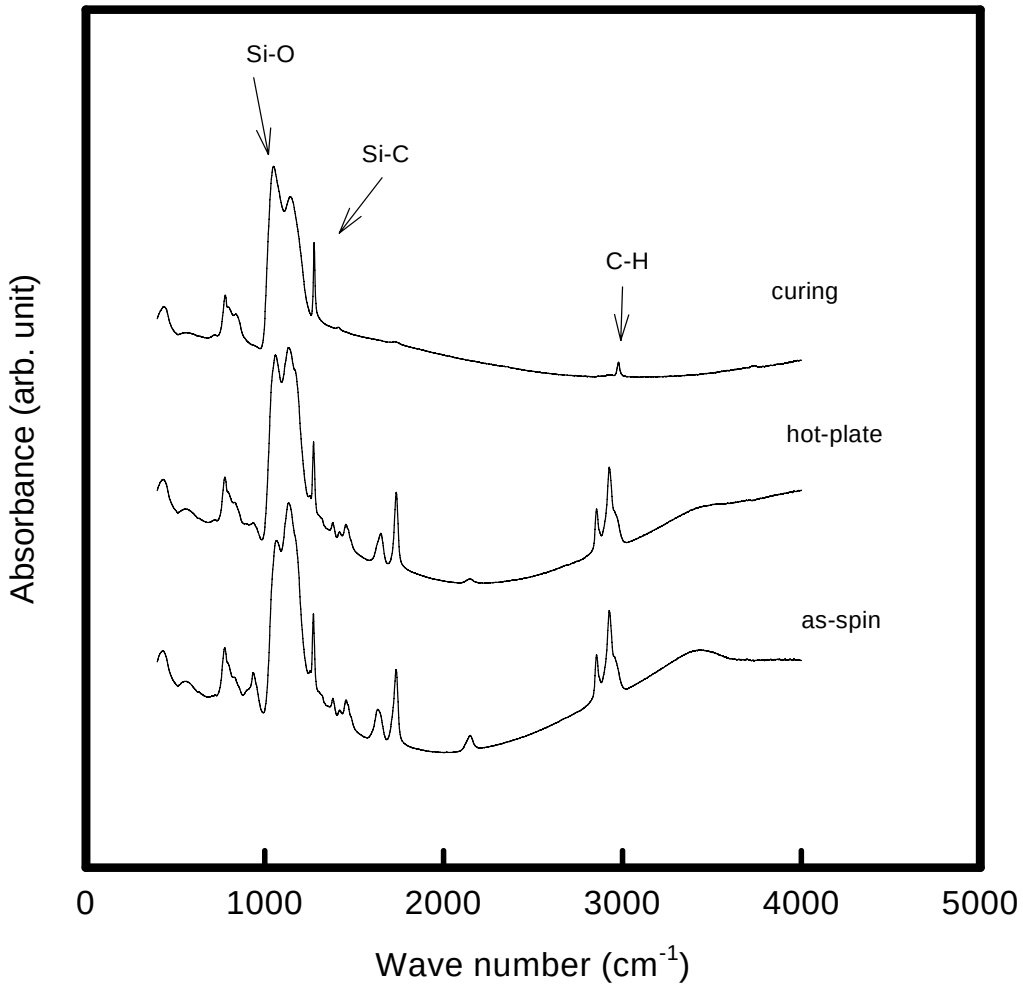


Fig 6-1 The FTIR spectra variation of as-spun porous organosilicate glass (POSG) after undergoing a series of thermal process.

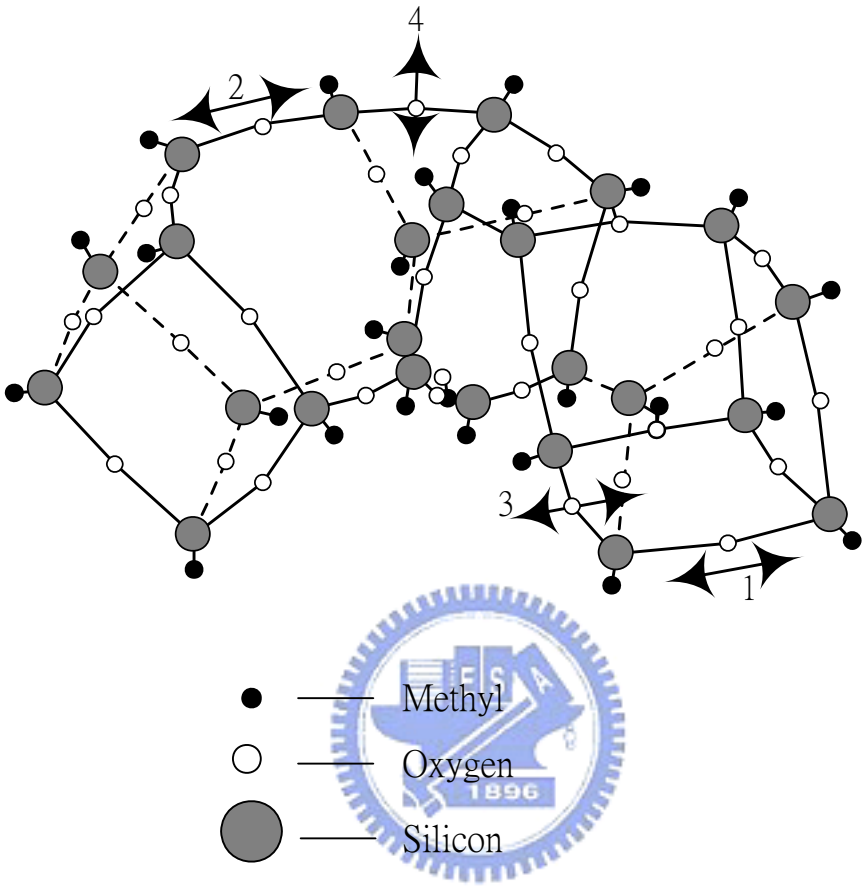


Fig 6-2 Three-dimensional (3D) network structure of POSG.

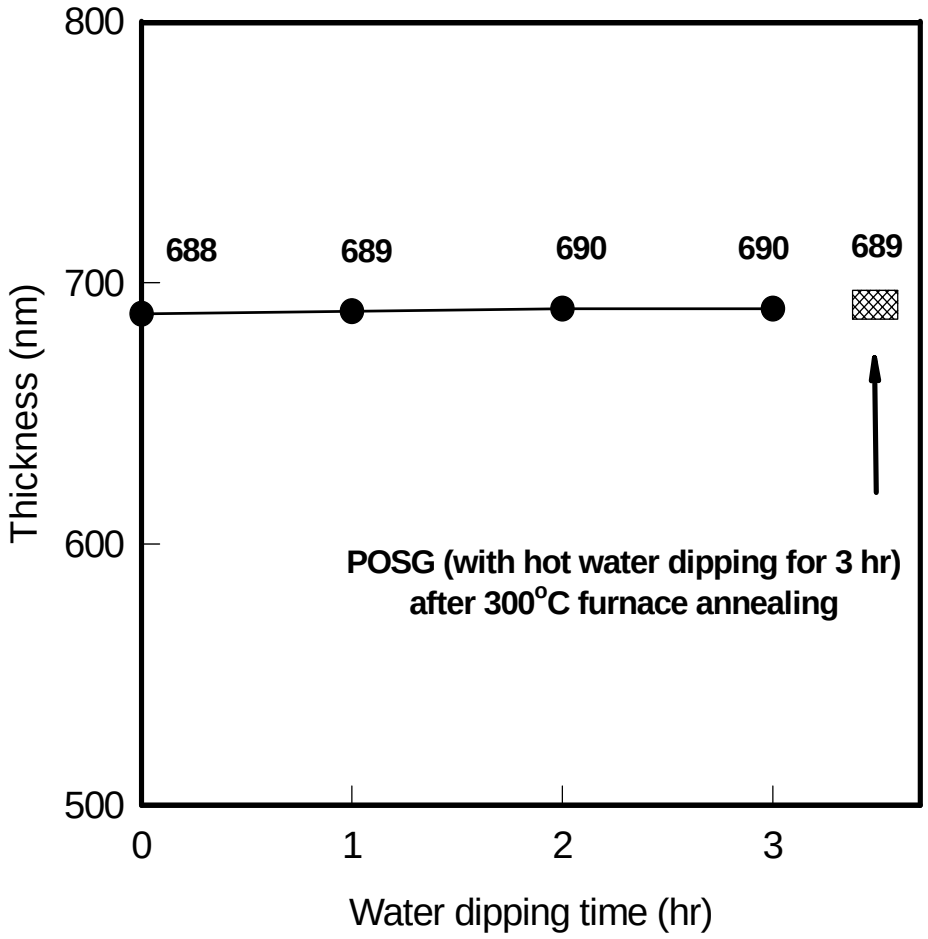


Fig 6-3 The evolution of stress of POSG with the hot-water dipping for 1 to 3 hours.

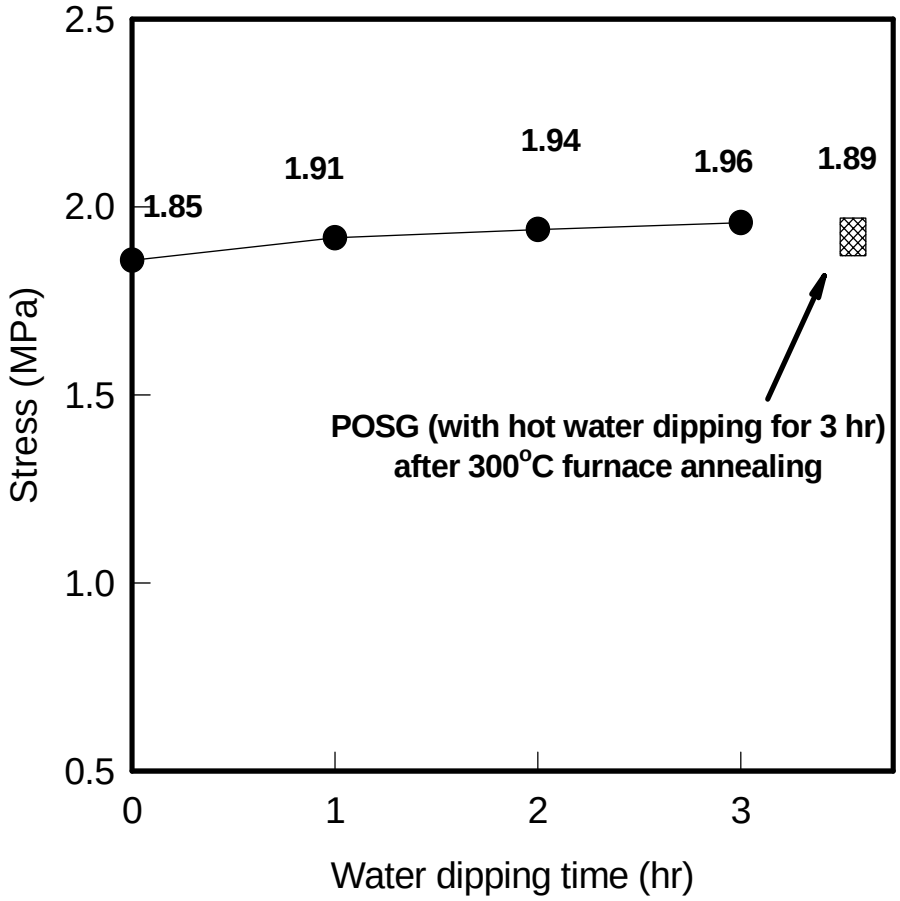


Fig 6-4 The thickness variation of POSG with the hot-water dipping for 1 to 3 hours.

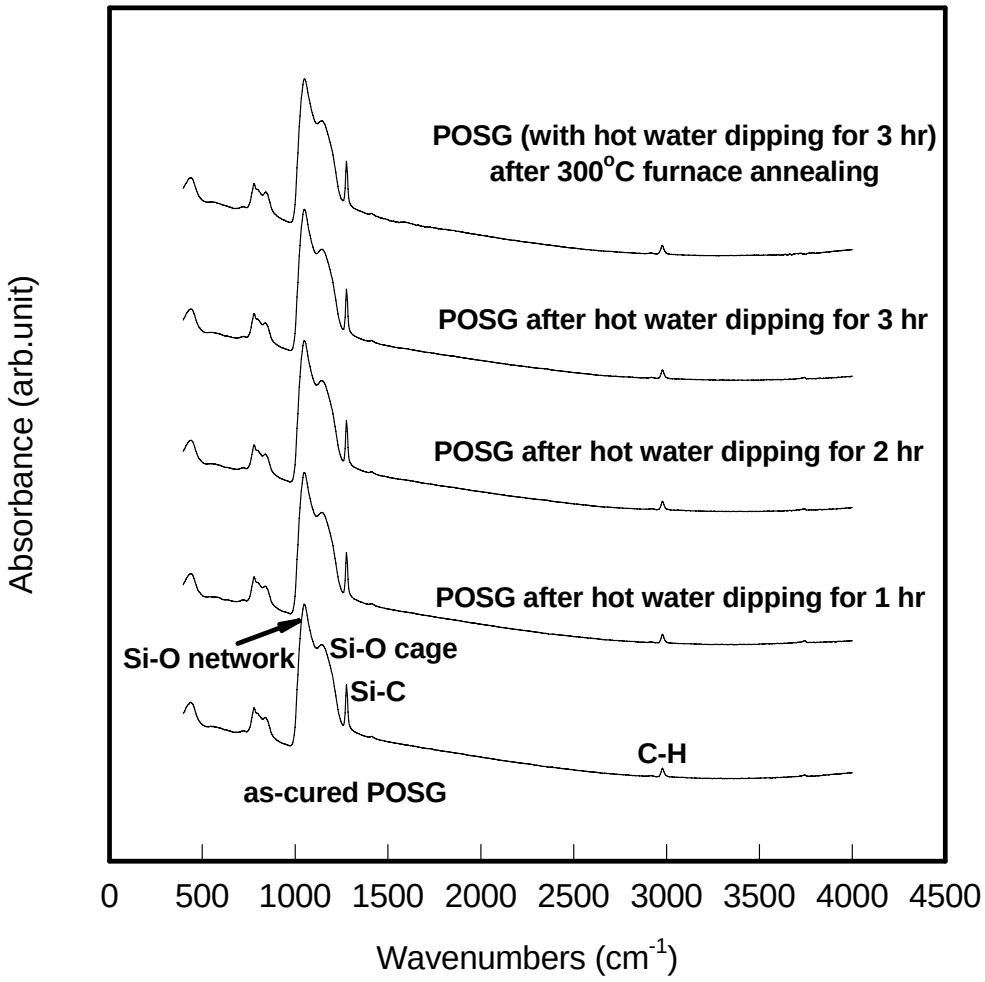


Fig 6-5 The FTIR variation of POSG with the hot-water dipping for 1 to 3 hours.

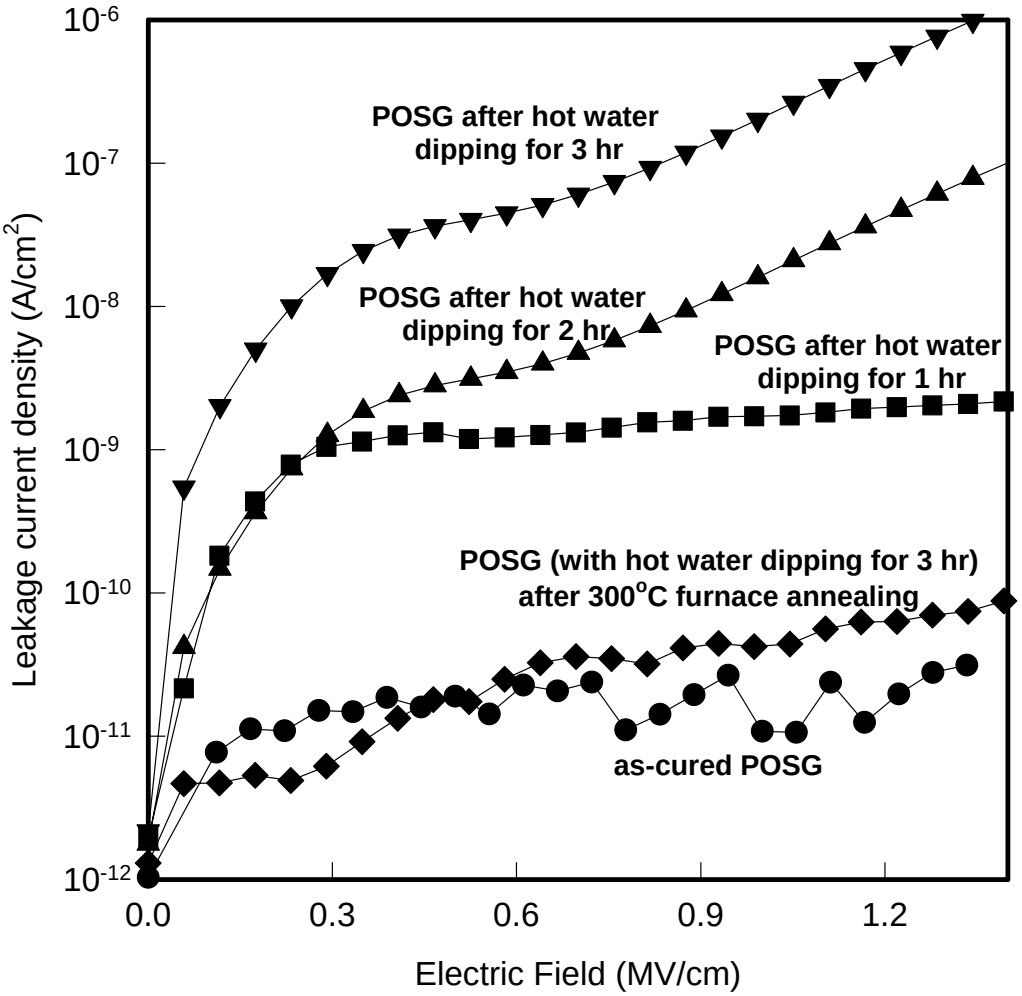


Fig 6-6 The leakage currents of POSG increase with the increase of hot water dipping time, whereas the leakage currents decrease obviously after water-dipped POSG film (for 3 hr) undergoes 300℃ furnace annealing.

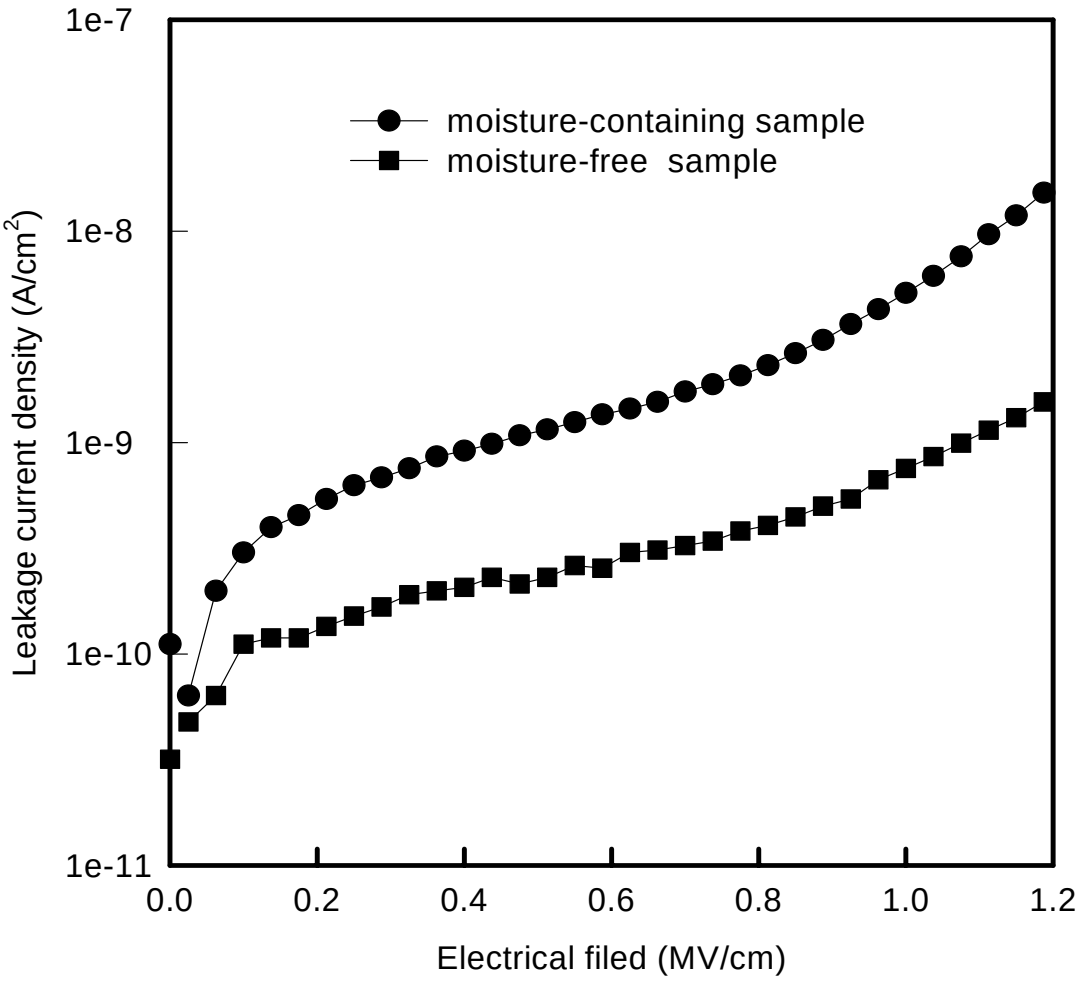


Fig 6-7 The J-E relations of POSG samples at room temperature. The moisture-containing sample owns the larger leakage current that the standard sample which is moisture-free at the same bias.

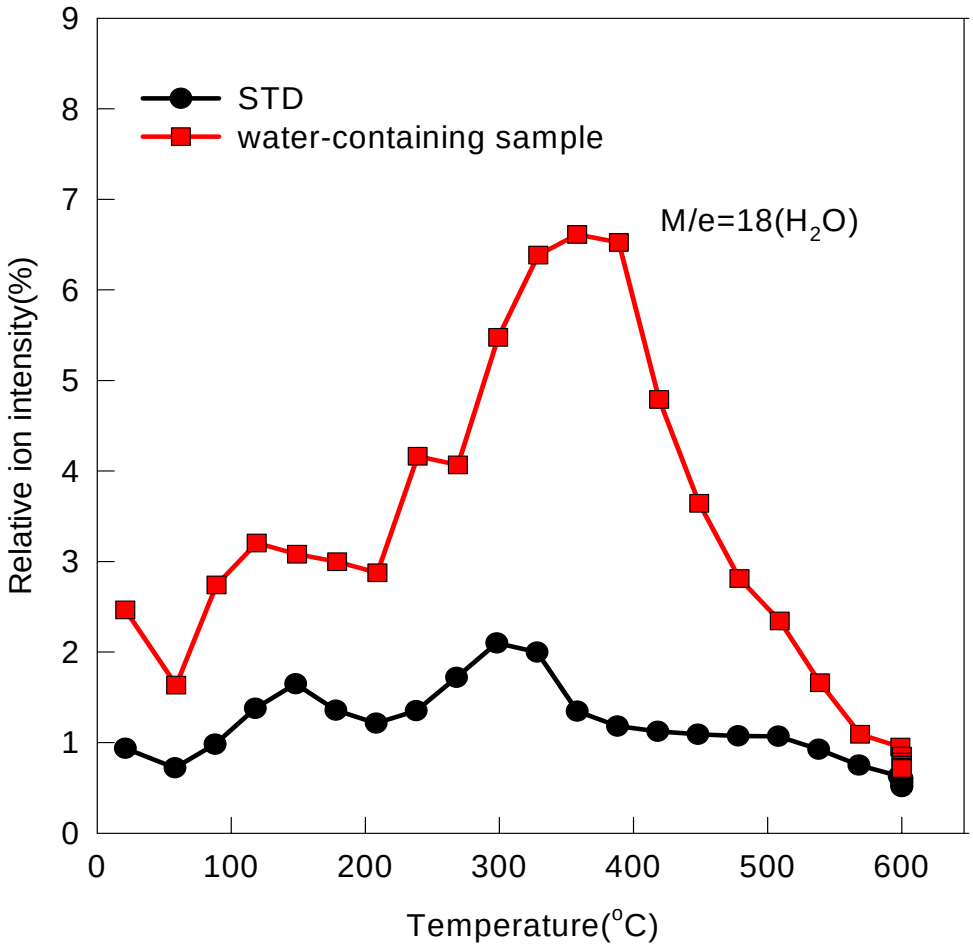
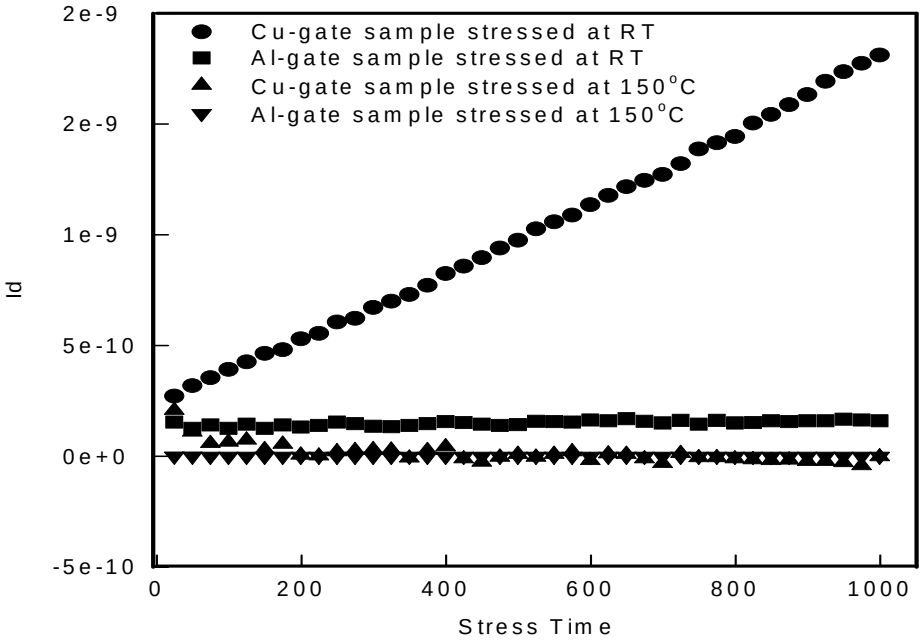
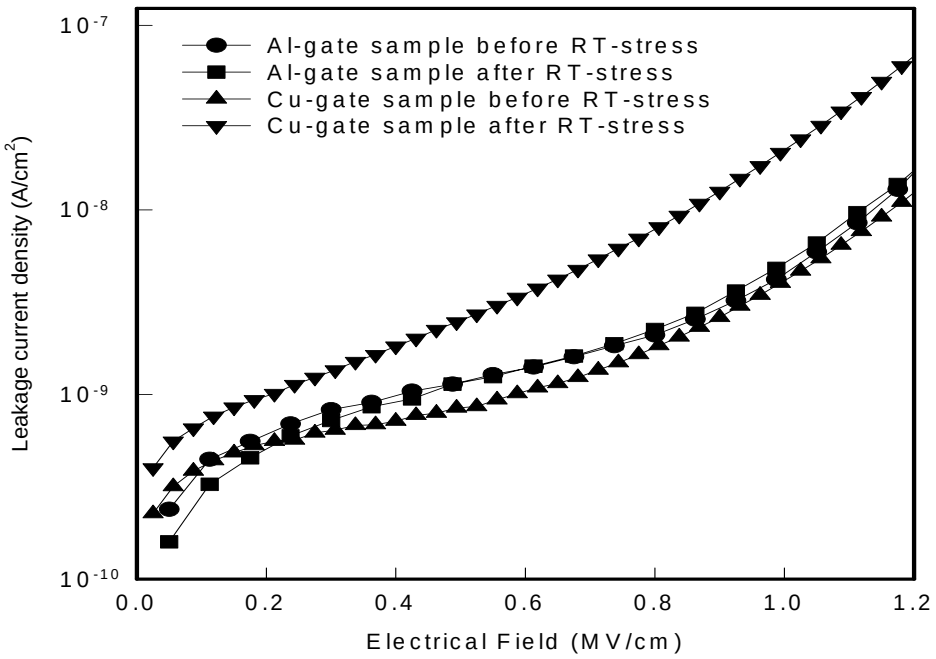


Fig 6-8 The thermal desorption spectra of moisture-containing and STD samples. The magnitude of H_2O signal (m/e=18) in moisture-containing sample is larger than that of STD sample.

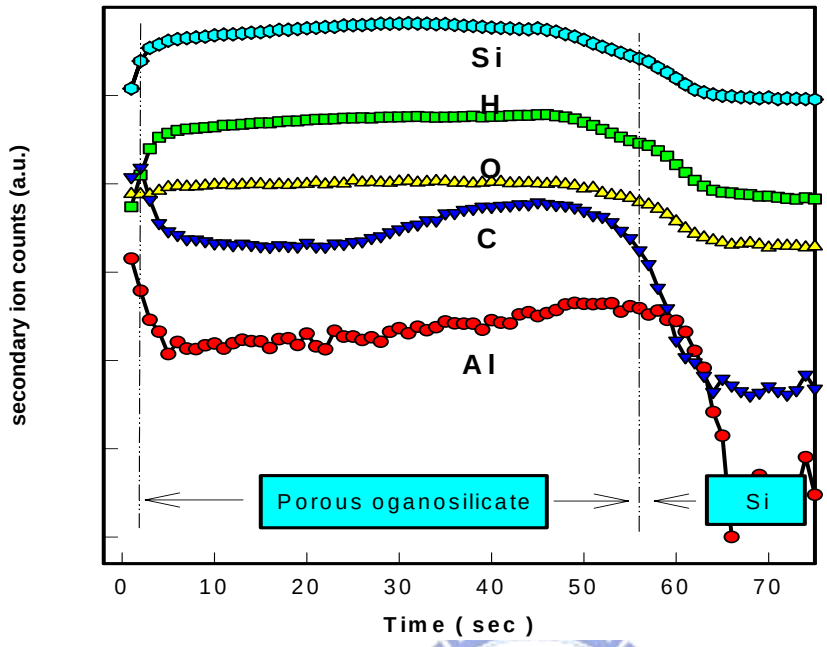


(a)

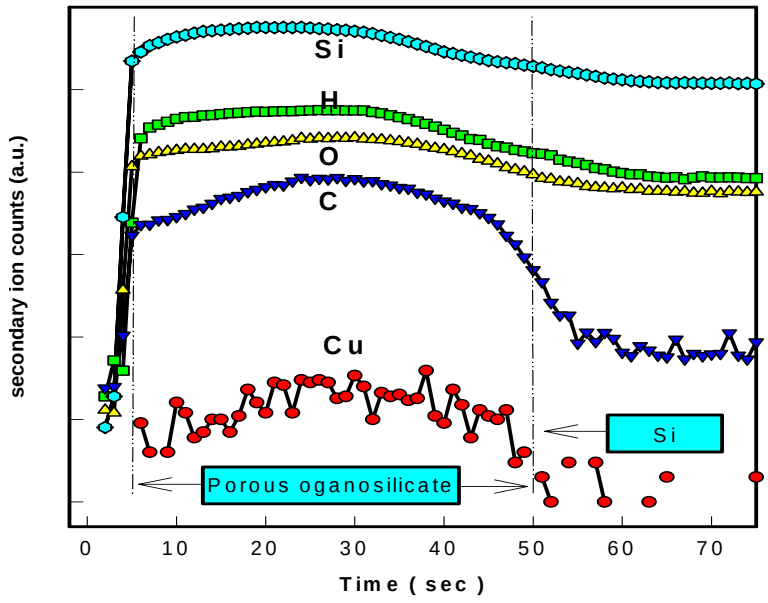


(b)

Fig 6-9 (a) The leakage current v.s. time (I-t) characteristics of Cu and Al-electrodes POSG during the bias stress at room temperature and 150°C, respectively. (b) The J-E curves of Cu and Al-electrodes POSG before and after the RT stress.



(a)



(b)

Fig 6-10 (a) The SIMS spectrum of POSG with Al-electrode after RT stress. (b) The SIMS spectrum of POSG with Cu-electrode after RT stress.

Chapter 7

Investigation of the Electrical Properties and Reliability of Amorphous SiCN

7.1 Introduction

To reduce RC-delay, copper wiring and low-k dielectrics are currently used in ultra large scale integrated (ULSI) circuits and large area AMLCD[7.1]. Compared to Al wiring, Cu has better resistivity toward electromigration. But one of the reliabilities in Cu metallization is dielectric degradation caused by Cu ion drift. Copper diffusion in low-k dielectric introduces deep-level traps in silicon that severely deteriorate the device's electric reliability, resulting in the large injection leakage current and premature dielectric breakdown. The diffusion of copper may because the material with the lower dielectric constant of low-k dielectric material could lead to a less dense structure of the material. Moreover, copper ions could rapidly drift in silica-based low-k during bias-temperature stressing[7.2].A less dense structure results in a lower dielectric constant but as well in a higher copper ion drift rate. Moreover, copper has a poor adhesion to most dielectric materials. Thus, copper interconnect lines must be encapsulated from the surrounding dielectric layers so as to foster adhesion and avoid copper diffusion through the low-k dielectric. And thus obtain a reliable copper damascene architecture. So, copper diffusion in low-k dielectric may give rise to an unanticipated yield or reliability program. Hence, a diffusion/drift barrier layer with stronger electrical characteristic in damascene process is necessary

to prevent copper movement into inter-level and inter-metal dielectric (ILD & IMD). [7.16-7.17]

Therefore, it's necessary to introduce a barrier dielectric between Cu wiring and dielectric insulators to prevent the Cu ion drift/diffusion[7.3-7.4]. The typically used barrier dielectric is SiN, which could efficiently prevent the Cu drift[7.5]. However, the dielectric constant of SiN is lager (~7). To reduce the effective dielectric constant of IMD and ILD, SiN must be substituted[7.6]. Implementations of Cu diffusion barrier with dielectric having a k-value are more effective in reducing interconnect capacitance. Studies on barrier dielectrics which have lower dielectric constants related to SiN would be attractive[7.7-7.8]. Recently, some SiC based materials with k<5 were proposed as barrier dielectrics [7.9-7.10]. In order to solve the issue for integration of low-k dielectric and copper, silicon carbide film has been under intense research [7.3-7.5] since their good electrical properties, good stability under thermal cycles manufacturability, high etch selectivity (with respect to ILD), and successful preparation using the conventional plasma enhanced chemical vapor deposition (PECVD) instrument. Hence, silicon carbide is an important material for potential application as the copper diffusion/drift barrier layer, hard mask, and etch stop layer.

In this chapter, we demonstrate the SiC-based dielectric films with various nitrogen concentrations. Electrical characteristics and material analysis will be used to explore leakage behaviors of barrier dielectrics. We report the conduction behaviors of post-breakdown (P.B.) a-SiCN film due to Cu penetration. Moreover, a physical model to depict the break-down mechanism is proposed according to SIMS and electrical characteristics.

7.2 Experimental procedures

The silicon carbide films with various concentrations of nitrogen were deposited with tri-methyl-silane source using plasma-enhance chemical vapor deposition (PECVD) system. The deposition temperature was 350^{o}C. Various concentrations of nitrogen in the films were obtained by controlling by NH_3 gas flow rate during deposition. The pressure in the chamber is kept at 3 torr during the deposition. The silicon carbide film was deposited on p-type silicon wafer with a resistivity of 15-25 Ω-cm. The code name of the pure silicon carbide film in this study is “SiC”; besides, the code names of silicon carbide films with various flow rate of NH_3 gas are “SiC-N1”, “SiC-N2”, “SiC-N3” and “SiC-N4”. The flow rate of NH_3 gas for SiC-N1, SiC-N2, SiC-N3 and SiC-N4 were increasing from 250 to 500 sccm. The XPS (X-ray photoelectron spectra) was recorded by a VG Escalab MKII spectrometer using Mg Kα (1253.6eV) radiation, and it was employed to observe the composition of silicon carbide films. The infrared spectrometry was performed from 4000 to 400 cm^{-1} using a Fourier transform infrared (FTIR) spectrometer calibrated to an unprocessed bare wafer, for determining the chemical structure of the silicon carbide film. The refractive index and thickness of the silicon carbide with or without nitrogen were measured with an n&k analyzer and SORRA ellipsometer. MIS structures of Cu/silicon carbide/silicon as well as Al/silicon carbide/silicon were used to investigate the behavior of basic electrical characteristics.

The dielectric constants and leakage current of the SiC films were investigated using capacitance-voltage (C-V) and current-voltage (I-V) characteristics measurement on metal-insulator-semiconductor (MIS) capacitor structure. A Keithley Model 82 CV meter at 1 MHz was used to measure the dielectric constant of the film with a gate electrode area of 0.0053 cm^2. The current-voltage (I-V) characteristics of

SiC films were measured by an HP4156. The gate-electrode area of the MIS structure was 0.00133 cm^2 for I-V measurement.

The completed Al and Cu gated MIS capacitors were then bias-temperature-stressed (BTS) at 150^oC with gate electrode biases (V_{gate}). The stress time was 1000 sec, which is long enough for the mobile charges to drift across the stacked insulator layer. The bias was provided by an HP4156B semiconductor parameter analyzer.

7.3 Results and discussions

7.3.1 Intrinsic properties of a-SiCN

Figure 7-1 shows FTIR spectra of silicon carbide films with and without the various flow rate of NH_3 gas during the deposition process, and the important regions of silicon carbide film were labeled in the figure and indicated as follows. The peak at 780 cm^{-1} is identified as Si-C stretching bond. In addition, Si-CH_2-Si rock and C-H wag peak are near 990 cm^{-1}, C-F bending peak is at 1100 cm^{-1}, Si-CH_3 bending peak is at 1245 cm^{-1}, Si-H stretching peak is near 2100 cm^{-1}, and C-H stretching peak is near 2960 cm^{-1}. All of these bonds make the surface of the silicon carbide film hydrophobic. From the figure, the samples, SiC-N1~SiC-N4, have stronger Si-C stretching bonds than the pure silicon carbide, SiC.

XPS spectrum for all of the specimens are shown in Fig. 7-2, and the major peak for Si_{2p} (~115eV), Si_{2s} (~145eV) and C_{1s} (~285eV) of every specimens are clearly evident in it. The peak of N_{1s} (~398eV) appears in SiC-N1~SiC-N4, but was absent in pure silicon carbide, SiC. The enlargements of N_{1s} for all the specimens are shown in Fig. 7-3. It certificates the existence of SiN bonding in SiCN samples. The peak heights of SiC-N1~ SiC-N4 are higher than that of SiC. On the contrary, the carbon

contents of the sample SiC-N1~SiC-N4 are smaller than that of SiC. Moreover, the content of silicon remains constant for all the specimens. The atom percentage of nitrogen content for SiC-N1, SiC-N2, SiC-N3, and SiC-N4 is 14.37%, 15.62%, 16.31%, and 16.64%, respectively. Although the change is not significant, the nitrogen content certainly increases with increasing ammonia flow rate during the deposition.

The dielectric constant (k) values for SiC-N1, SiC-N2, SiC-N3, and SiC-N4 is 4.50, 4.47, 4.34, 4.40, respectively. The pure silicon carbide film had a dielectric constant about 3.8, and the dielectric constants of nitrogen-containing films, SiCN, were higher from 4.3 to 4.5. The increase of dielectric constant is due to the appearance of SiN bonds in a-SiC films. The tetrahedral structure of SiC is distorted with additive of SiN bonds and then polarization chemical structure is raised [7.11].

The leakage current densities for all the films are sketched in Fig 7-4. It shows clearly that the leakage current of pure silicon carbide (SiC) is much lager than the doped films. The samples we study are not crystallized SiC film but amorphous ones. Nitrogen is not an active dopant without activation process. On the contrary, a large mount of SiN bonds which exist randomly in a-SiC films make the structure of a-SiC film more disorderly. In addition, the bonding energy of SiN is higher than SiC bond. The carrier would transport through the SiCN films difficultly. As a result, the leakage currents of a-SiCN films are smaller than a-SiC ones. The curves of SiC-N1~SiCN4 are almost similar so that we can put them on a par. Increasing the temperature increases the leakage current density. Furthermore, the J-E curves are symmetric both in positive and negatives bias, and the mechanism of leakage current is Poole-Frenkel (P-F) emission as the electrical filed is above 2.5MV/cm. Poole-Frenkel (P-F)[7.12-7.13]emission is due to field-enhanced thermal excitation of trapped electrons in the insulator into the conduction band. The current density is

given by:

$$J = J_0 \exp\left(\frac{\beta_{PF} E^{1/2} - \phi_{PF}}{k_B T}\right)$$

where $\beta_{PF} = (e^3/4\pi\varepsilon_0\varepsilon)^{1/2}$, A* effective Richardson constant, ϕ_{PF} the contact potential barrier, k_B the Boltzmann constant, e the electronic charge, E the applied electric field, ε_0 the dielectric constant of free space, and ε the relative dielectric constant. Poole-Frenkel mechanism can be identified by comparing the theoretical value of β_{PF} with the experimental value of β_{exp} obtained by calculating the slope of the curve ln (J/E)-$E^{1/2}$. Figure 7-5 shows that a logarithm of leakage current of samples SiC-N4 is linearly related to the square root of the applied electric field, which is closed to Poole-Frenkel emission. The value of β_{exp}= 5.8×10^{-23} ($Jm^{1/2}/V^{1/2}$) which is close to the theoretical value of β_{PF}= 5.72×10^{-23} ($Jm^{1/2}/V^{1/2}$) as the dielectric constant is 4.4.

The effect of various flow rate of NH_3 on the barrier ability was also investigated. We samples SiC-N1 and SiC-N4 sine the flow rate of NH_3 for SiC-N4 is twice that of SiC-N1. Although the leaky behaviors of both samples are similar, as shown in Fig.7-4, we performed the bias-temperature stress measurement on them. Bias-temperature stressing (BTS) is a typical manner to estimate the barrier ability against the Cu penetration. We find that SiC-N1 and SiC-N4 exhibit excellent electrical stability even after BTS (3MV/cm, 150^{o}C, 1000sec). Figure 7-6 and 7-7 exhibit the I_{gate}-t_{stress} curves of SiC-N1 and SiC-N4 with either Al or Cu gate during BTS measurement in high electric field. It's evident that the leakage current of SiC-N1 was almost one order of magnitude lager than that of SiC-N4. It is worthy to mention that the leakage current is lower and becomes steady in the electric field below 3.50 MV/cm with increasing stress periods. But it goes up for electric field greater than 3.75 MV/cm as shown in Figs. 7-6 and 7-7. The difference between Cu

and Al curves is mainly due to the Cu penetration [7.11]. When Cu ions were drifted in high electrical field at high temperature, the moving Cu ions would produce the ion current. In addition, the Cu ions are regarded as trap centers in dielectrics which could assist the carrier to transport [7.12]. The leakage currents increase abruptly at 4.5 MV/cm for SiC-N1 and 5.0 MV/cm for SiC-N4 indicating breakdown.

The difference between the increasing and decreasing behaviors of leakage currents can be explained by material analysis. Figs. 7-8 and 7-9 illustrated the SIMS spectrum of SiC-N4 with either Cu or Al electrode after BTS measurement in the condition of 3.5 and 5.0 MV/cm for 1000sec at 150^{o}C. It's clear that the copper counts in the SiC-N4 layer of the MIS structure after BTS with 5Mv/cm are much larger than that after BTS with 3.5MV/cm, which almost remains zero. Furthermore, the Al counts remain the same in the silicon carbide layer of the MIS structure after 3.5 MV/cm BTS and 5.0 MV/cm BTS.

7.3.2 Cu-penetration induced breakdown mechanism for a-SiCN

The J-E curves of SiCN-4 with MIS structure, Cu/a-SiCN/Si, after BTS measurement at 150^{o}C in the electric field 5.0MV/cm and the standard (STD) one are demonstrated in Fig. 7-10, respectively. The leakage currents of stressed a-SiCN sample increased abruptly, indicating breakdown. We have reported that the conduction behavior of as-deposited a-SiCN is Poole-Frenkel at high electric field (>2.5MV/cm). Poole-Frenkel (P-F) emission is due to field-enhanced thermal excitation of trapped electrons in the insulator into the conduction band.

Figure 7-9 illustrated the SIMS spectrum of post-breakdown a-SiCN film after BTS. It's clear that the copper counts in the post-breakdown a-SiCN films of the MIS structure. However, the Cu peak was un-detected in as-deposited film. The

distribution profile of Cu in post-breakdown a-SiCN films was numerous near Cu electrode and reduced at silicon interface. In order to investigate the breakdown characteristics, the conduction behavior of the post-breakdown a-SiCN films were measured for temperature between 50K and 298K.

The temperature dependence of post-breakdown SiCN-4 film was displayed in Fig. 7-10. The current density of post-breakdown sample was measured at 298K (curve I), 100K (curve II), and 50K (curve III), respectively. The current of breakdown sample is obviously decreased with decreasing the temperature from 298K to 100K. But the conduction characteristics of 100K and 50K are similar. Also, note that there are two distinct regions in curve II (100K) and III (50K). At medium fields, the current varies exponentially with the field; in high electric fields (>3.3 MV/cm) the characteristic deviates from the exponential dependence.

To realize the current behaviors of post-breakdown film, electrical characteristics are analyzed with typical conduction processes in insulator such as Poole-Frenkel emission, Schottky emission[7.12], space-charge-limited current[7.14-7.15], and Fowler–Nordheim tunneling[7.16-7.17]. We find that the leakage current of post–breakdown a-SiCN at 298K, curve I, is linearly related to square of the applied electric field, which corresponds to space-charge-limited current (SCLC) mechanism. As considering the SCLC conduction, the current density J can be expressed as the following equation,

$$J = \frac{9\varepsilon_0 \varepsilon\ \mu\theta V^2}{8d^3} \propto E^2 \qquad (2)$$

where μ is the free carrier mobility, ε_0 the permittivity of free space, ε the relative dielectric constant of the sample material, d the sample thickness, and θ is the ratio of the free charge carriers to trapped ones, which takes into account the trapping centers (impurity centers) concentration and their distribution. The SCLC

curves are usually interpreted in terms of charge injection and subsequent filling of the impurity/trapping centers giving rise to the progressively square type dependence of the *J-E* characteristics. Figure 7-11, transformed from curve I, shows that J is linearly proportional to E^2 at high electric field. Notably, conduction behaviors at low temperature, 100K and 50K, also obey the SCLC at high fields (>3.3 MV/cm) in curves I and II.

On the other hand, the electrical characteristics of post-breakdown a-SiCN at low temperature, curve II and curve III, follow the Fowler–Nordheim (FN) conduction in medium fields, see Fig. 12. It is generally accepted that the tunneling current through a insulator layer can be represented by the Fowler–Nordheim (FN) expression[7.16]

$$J=K_1E^2\ exp(K_2/E) \qquad (3)$$

where J is the current density, E is the electric field at the insulator, and K_1 and K_2 are two constants dependent on the cathode barrier height, and the electron effective mass. Equation (3) applies to triangular potential barriers pertinent to MIS structures when qVg is greater than barrier height, where q is the electron charge, Vg is the gate voltage.

Based on the observation described herein, we proposed a model to depict the conduction characteristics of breakdown a-SiCN caused by Cu penetration. The Cu ions would ionize from Cu electrode and drift in high electrical field at high temperature during BTS[7.2]. The Cu ions are regarded as trap centers in dielectrics which could assist the carrier to transport [7.1-7.19]. The large amount of traps would induce band-gap narrowing in insulator [7.20]. When the number of traps reaches a critical amount, a conduction filament region which loses its dielectric property is formed and composed of numerous Cu impurity/traps. According to SIMS spectrum, the number of Cu near silicon interface was reduced and assuming an energetic barrier inside the a-SiCN film, a cross-sectional view in real space of post-breakdown is

given in Fig. 13(a). In figure 13(a), the a-SiCN films is divided into two region, a conduction filament region (labeled A)[7.21] and a barrier (labeled B). The real space structure is transformed into energy band-diagram scheme for electrons drawn in Fig. 13(b). Since region A is a conduction filament region, the conduction band is connected smoothly to Fermi-level of Cu electrode. With reducing Cu impurity/traps toward silicon interface, the band-gap is gradually arising and the dielectric property is getting similar to un-degraded sample. However, the band-gap narrowing would appear at a-SiCN/Si interface since the Cu ions penetrated through the film. As a result, the schematic drawing of energy band diagram of breakdown a-SiCN was depicted in Fig. 13(b). It's worthy to mention that greater part of applied voltage should be dropped at barrier region because it plays as the large resistance at low temperature. The effective fields applied on the barrier region must be higher than that we displayed in curves II and III. Consequently, the requirement of F-N tunneling which should occur at high electrical field is achieved. The conduction current in post-breakdown SiCN films can be separated into two components: J1 and J2. The J1 is the thermal emission of traps electrons in insulator. The current J2 is due to tunnel emission of trapped electrons into the conduction band of silicon.

The electrons can easily transport form metal electrode to post-breakdown a-SiCN due to the continuation of conduction band between metal and a-SiCN. In addition, electrons have enough energy to jump across the barrier height between a-SiCN and silicon at 298K. Some transporting electrons are trapped at spatial traps caused by Cu penetration. The dominant characteristic is the SCLC mechanism. With decreasing the temperature, the cooling electrons can't excite across the barrier with loss thermal energy. Then the dominant characteristic is the F-N tunneling in post-breakdown a-SiCN at low temperature. As larger voltage is applied to the trapezoid potential barrier pertinent, the thinner barrier region is needed for the electrons to tunnel

through. Under this situation, the main controller of conduction is trap-filling in bulk and SCLC conduction is dominated. This can explain the reason why the F-N conduction turns into SCLC at high fields at low temperature.

7.4 Conclusion

We have investigated the leaky behavior and barrier characteristics of a-SiCN containing different nitrogen concentrations. The leaky behavior of a-SiCN is Pool-Frenkel in high electric field region. Thermal stabilities of a-SiCN films are good enough to meet the prescription in BOEL fabrication process. We performed the bias-temperature stress (BTS) on a-SiCN films to test the barrier ability against Cu penetration. Experimental results indicate that a-SiCN films containing higher nitrogen concentration exhibited better barrier ability. The dielectric breakdown is due to the penetration of Cu.

The electrical characteristics of post-breakdown a-SiCN caused by Cu penetration are investigated. SIMS spectrum shows that Cu ions can penetrate through the film at 150^{o}C in high fields (5MV/cm). It is observed that the main conduction of post-breakdown a-SiCN at room temperature (298K) is space-charge-limited current (SCLC) due to numerous Cu impurity/traps. Moreover, the characteristics at low temperature can be separated into two distinct stages, Fowler–Nordheim tunneling and SCLC conduction. We propose a physical model which post-breakdown a-SiCN was composed of two different conduction regions. It can well describe the electrical variation resulted from the Cu traps and temperature.

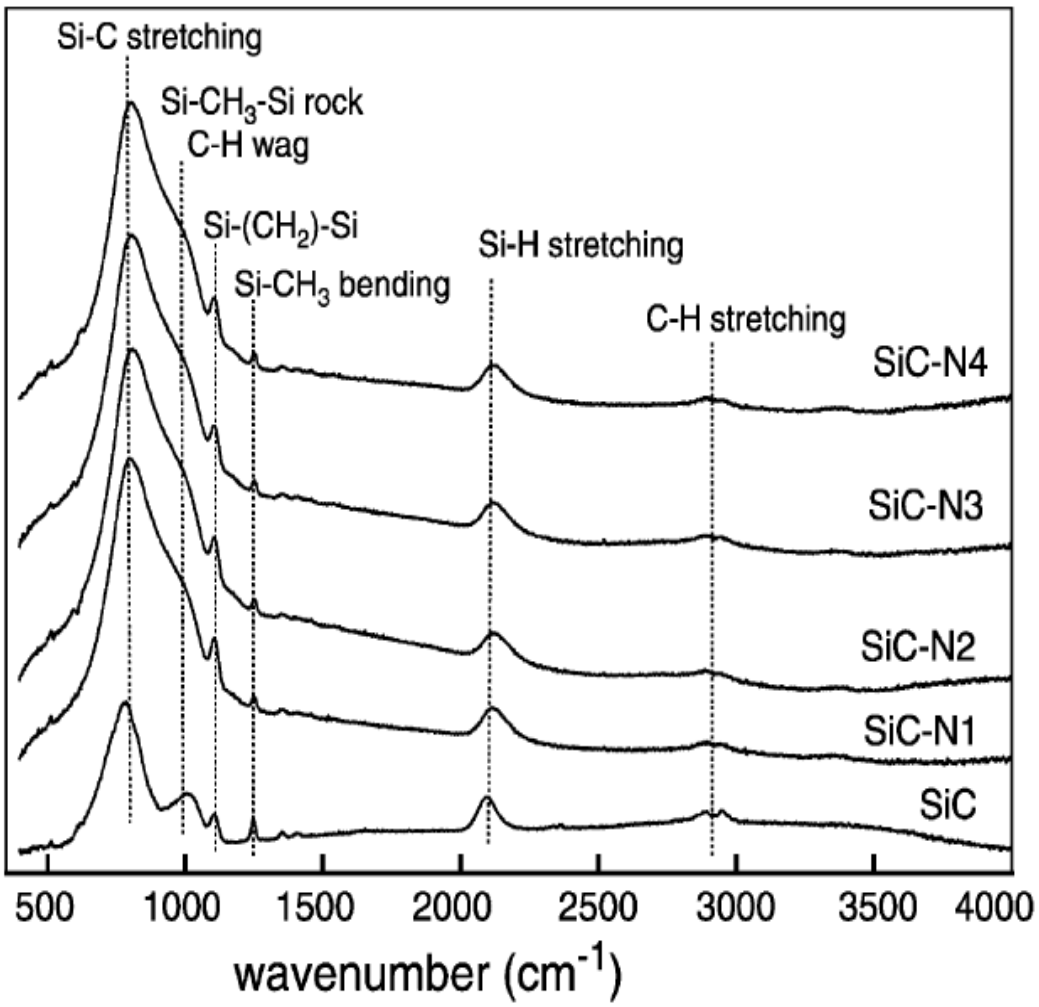


Fig 7-1 FTIR spectrum of silicon carbide with or without NH3 gas flow during deposition process.

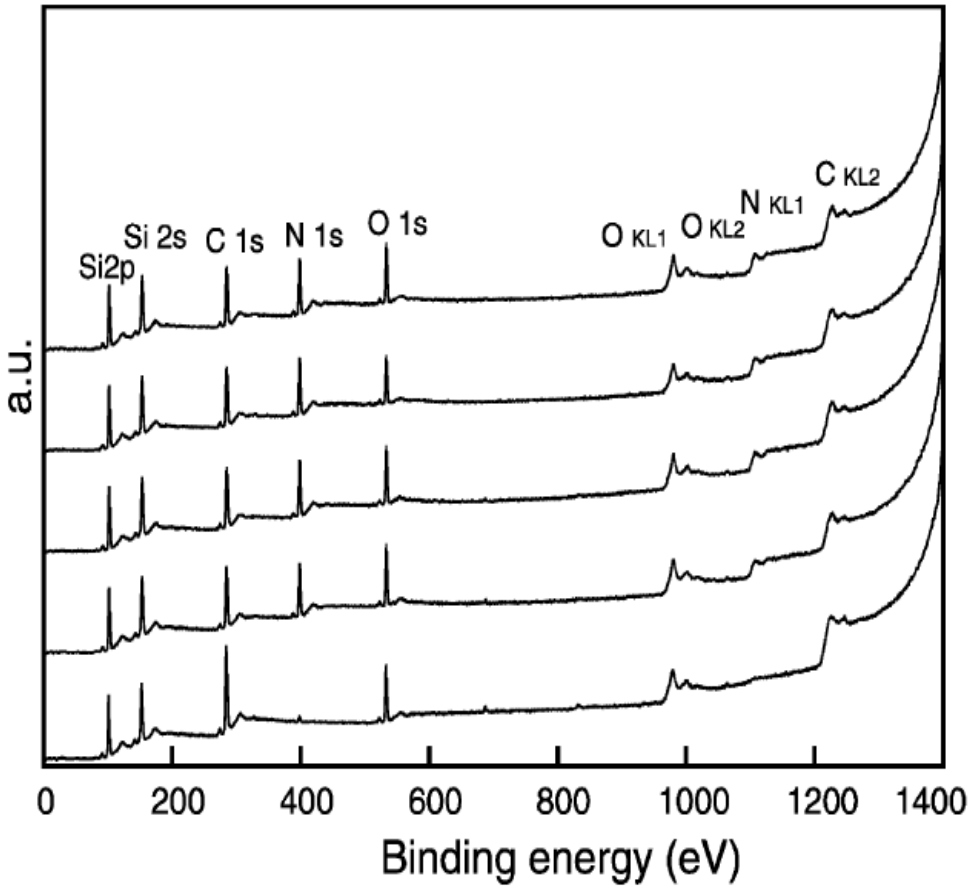


Fig 7-2 XPS (X-ray photoelectron spectra) spectra for all the specimens

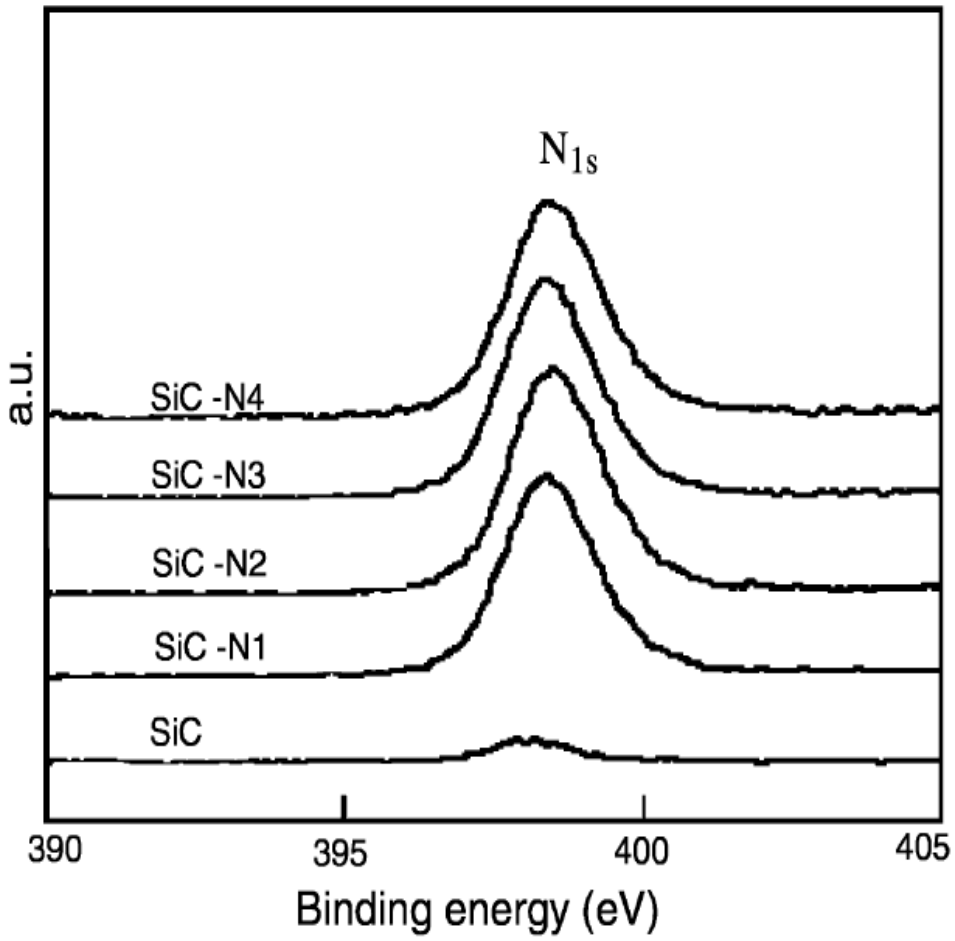


Fig 7-3 Enlargement of XPS spectra of N_{1S} peaks in Fig.2. The atom percentage of nitrogen content for SiC-N1, SiC-N2, SiC-N3, and SiC-N4 is 14.37%, 15.62%, 16.31%, and 16.64%, respectively.

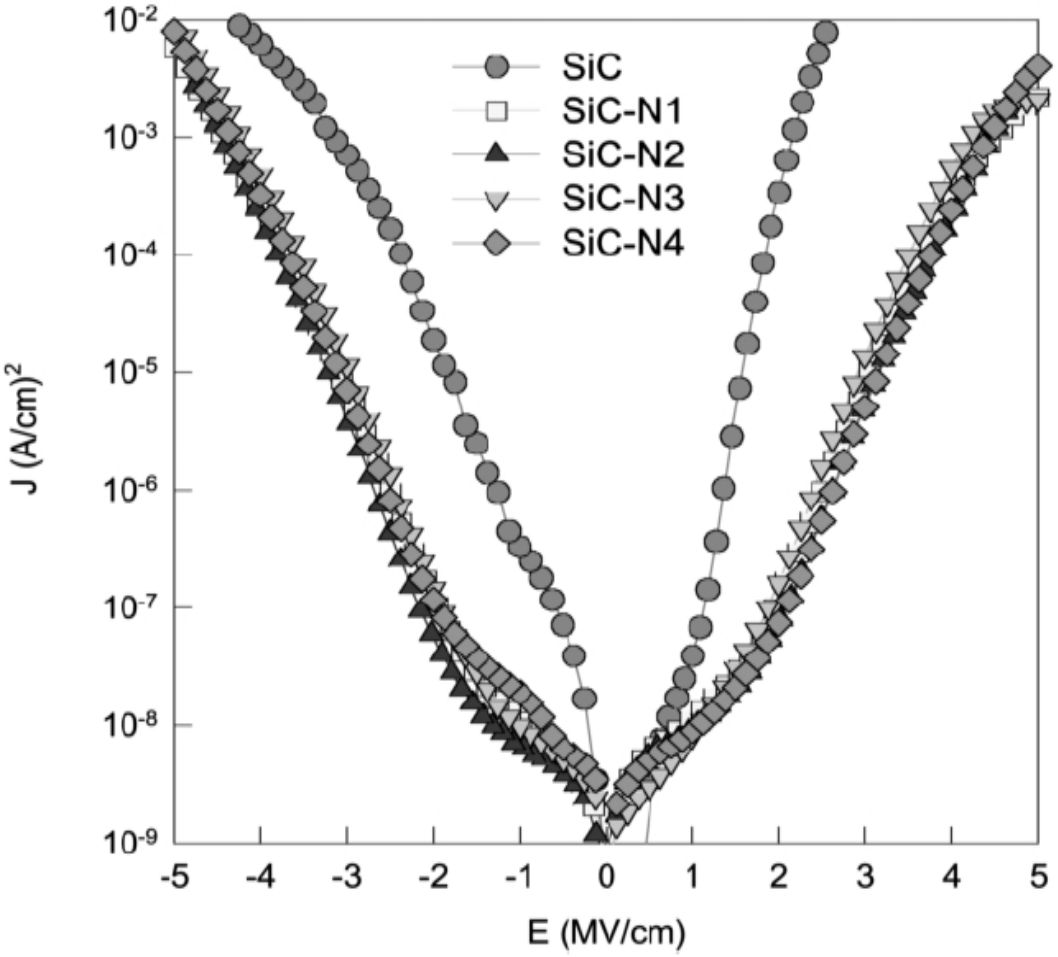


Fig 7-4 J-E curves for all the samples. The area of electrodes we used is 0.00133 cm^2. The leakage current of SiCN based films are lower than the a-SiC films.

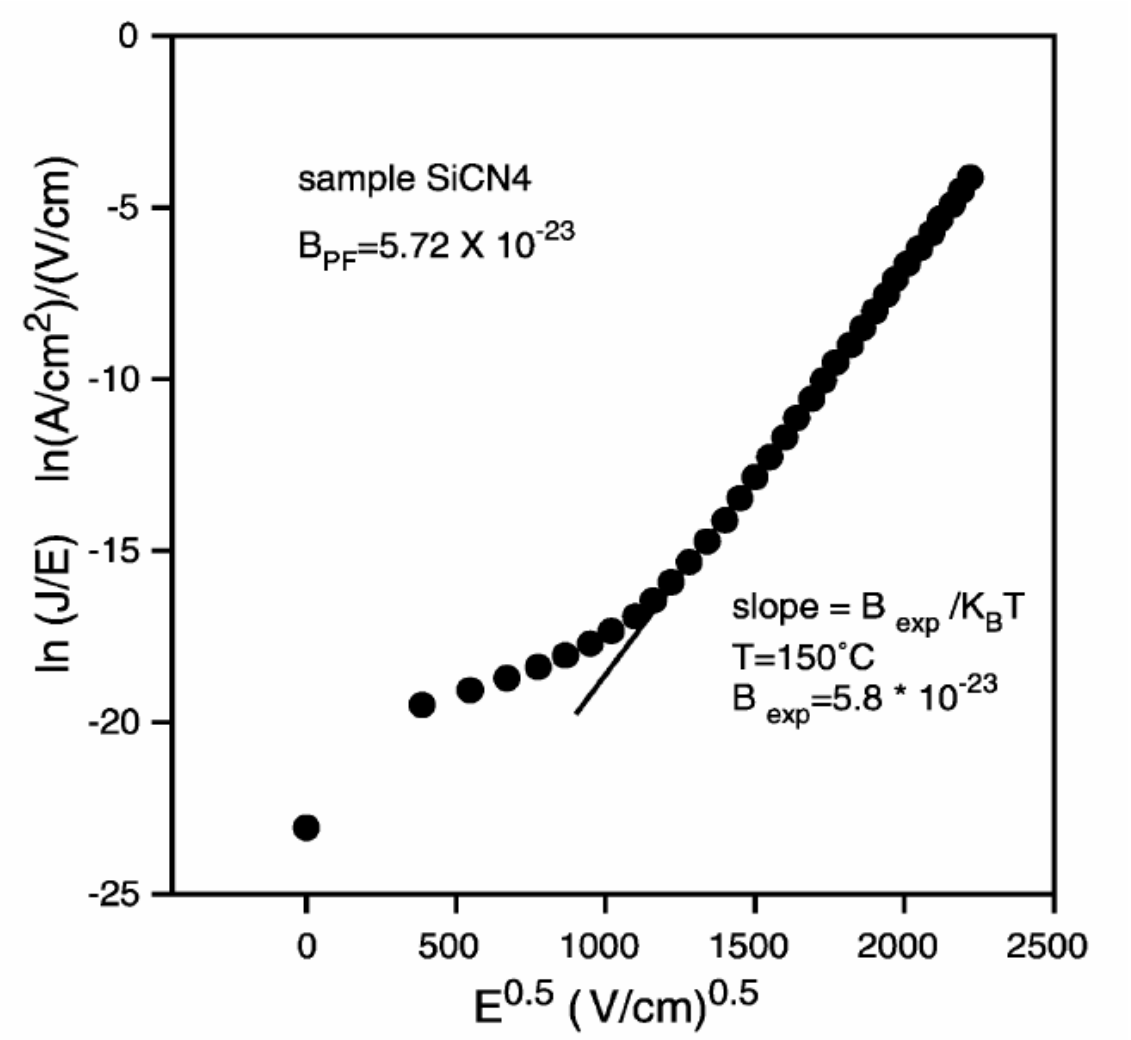


Fig 7-5 J-E curve on a log (J/E) versus E1/2 plot of sample SiC-N4 showing Poole-Fenkel conduction at high electric field region.

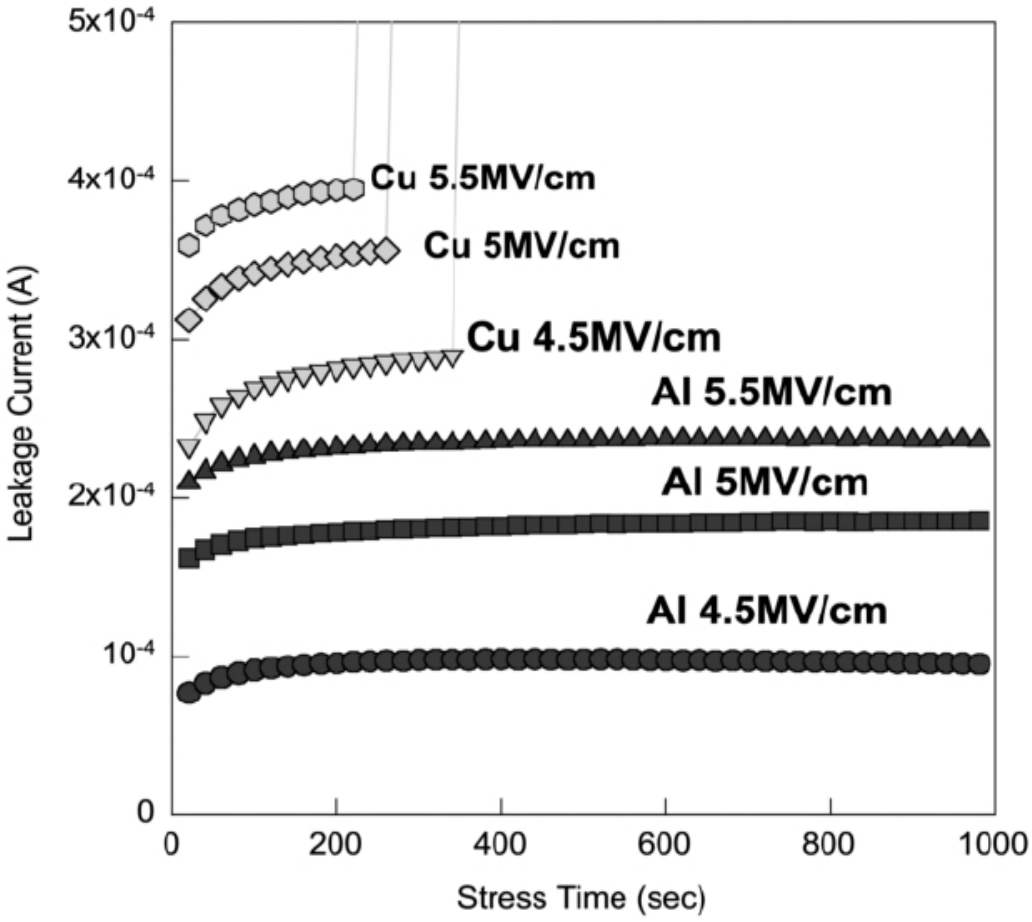


Fig 7-6 The relationship of leakage current and stress time for SiCN1 films with Cu and Al gates during BTS test. BTS tests were conducted at 150^{o}C, with electric fields of 4.5MV and 5.5MV/cm. Dielectric breakdown is easily occurred at Cu electrode samples at critical BTS condition (>4.5MV/cm).

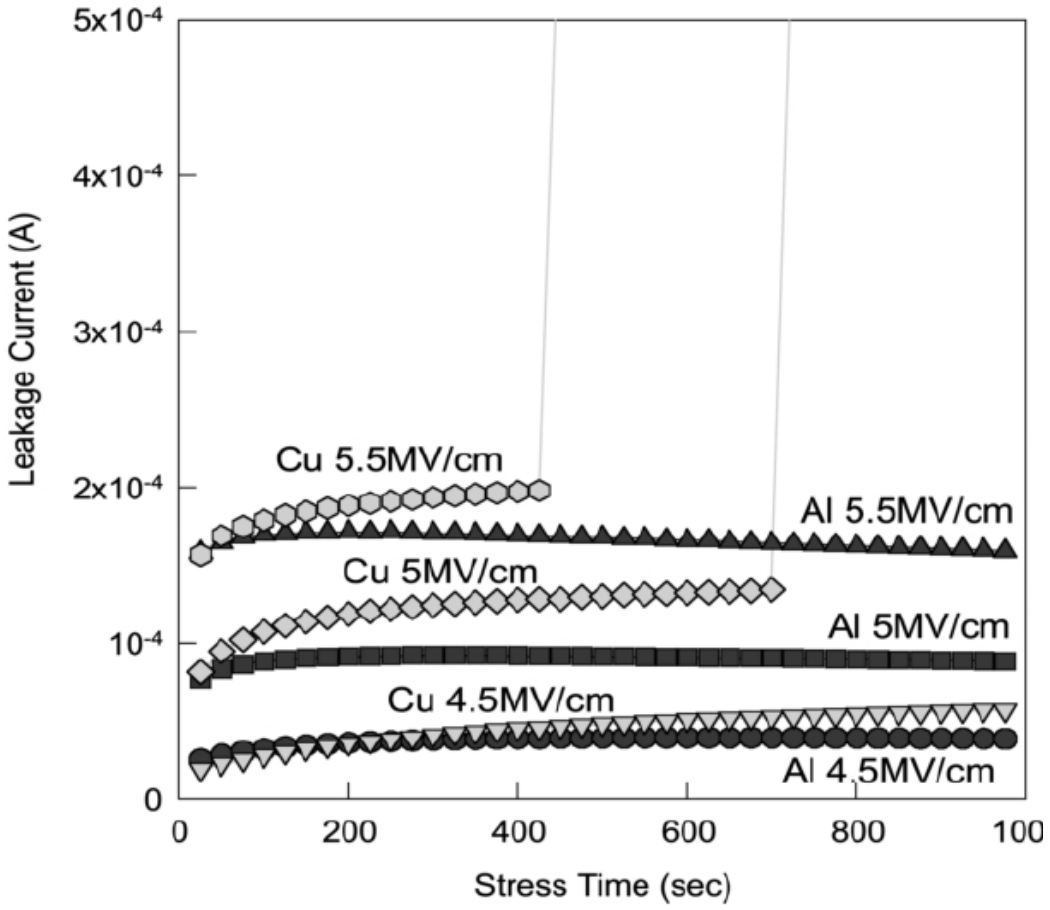


Fig 7-7 Leakage current-stress time curves of SiC-N4 with Cu/Al gates during BTS at 150^{o}C

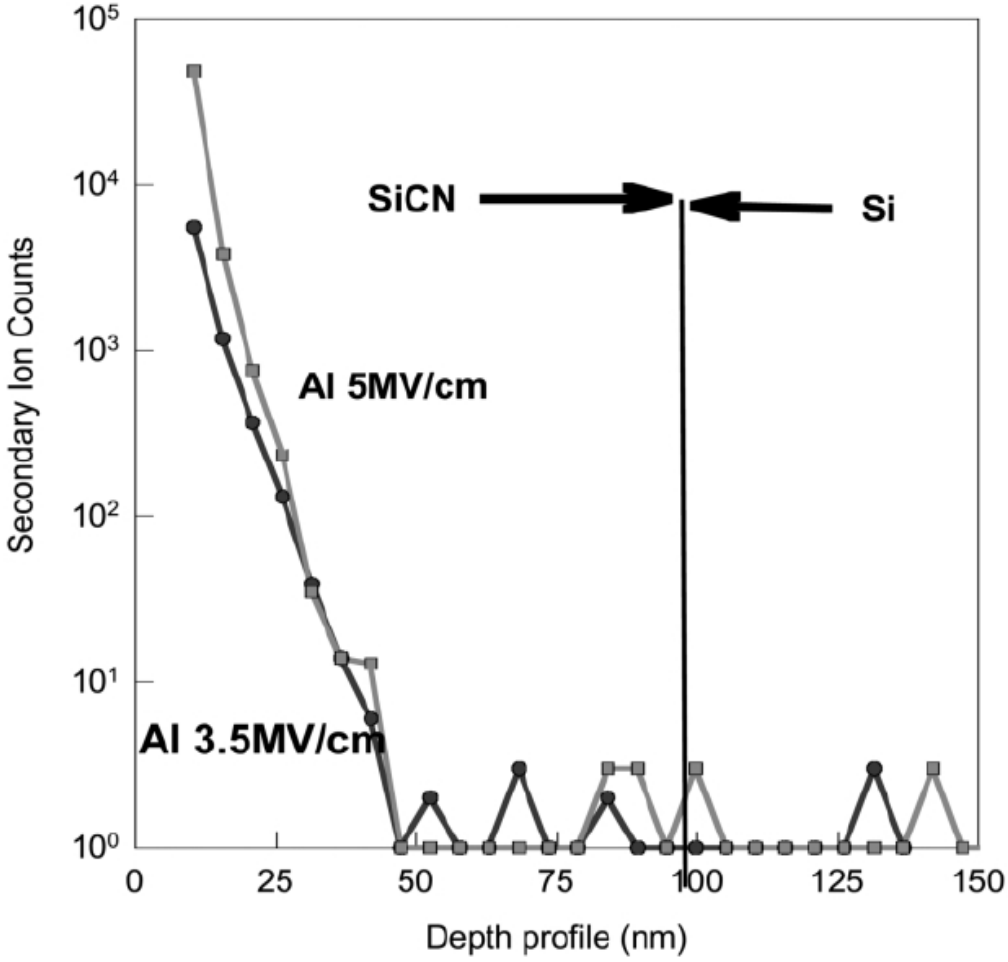


Fig 7-8 SIMS depth profile of SiCN4 with Al gate after BTS measurement (3.5/5 MV/cm, 150^{o}C, 1000sec). The accounts of Al remain at the same magnitude even after BTS with 5MV/cm for 1000sec at 150^{o}C.

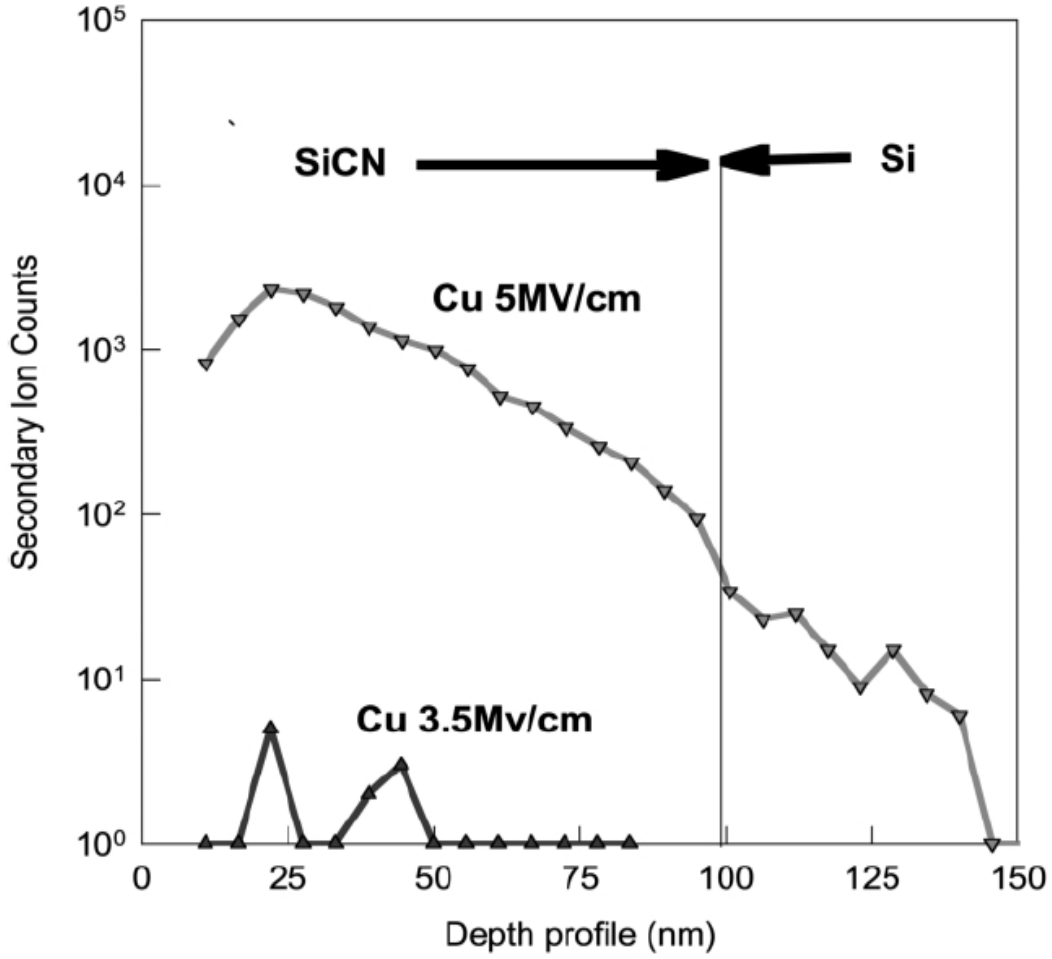


Fig 7-9 SIMS depth profile of SiCN4 with Cu gate after BTS measurement (3.5/5 MV/cm, 150^{o}C, 1000sec). The Cu ions obviously penetrate through the SiCN4 film after BTS with 5 MV/cm.

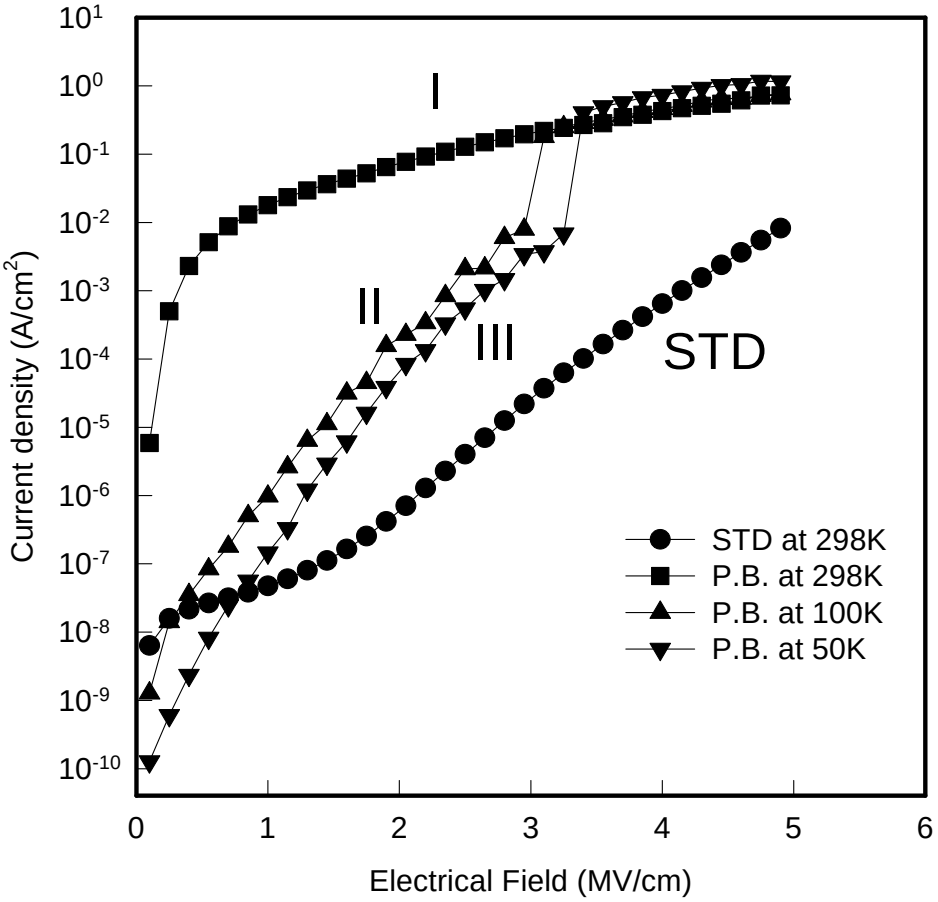


Fig 7-10 The J-E curves of SiCN4 (STD, as-deposited SiN4 sample measured at 298K; curve I, post-breakdown (P.B.) sample measured at 298K; curve II, P.B. sample measured at 100K; curve III, P.B. sample measured at 50K)

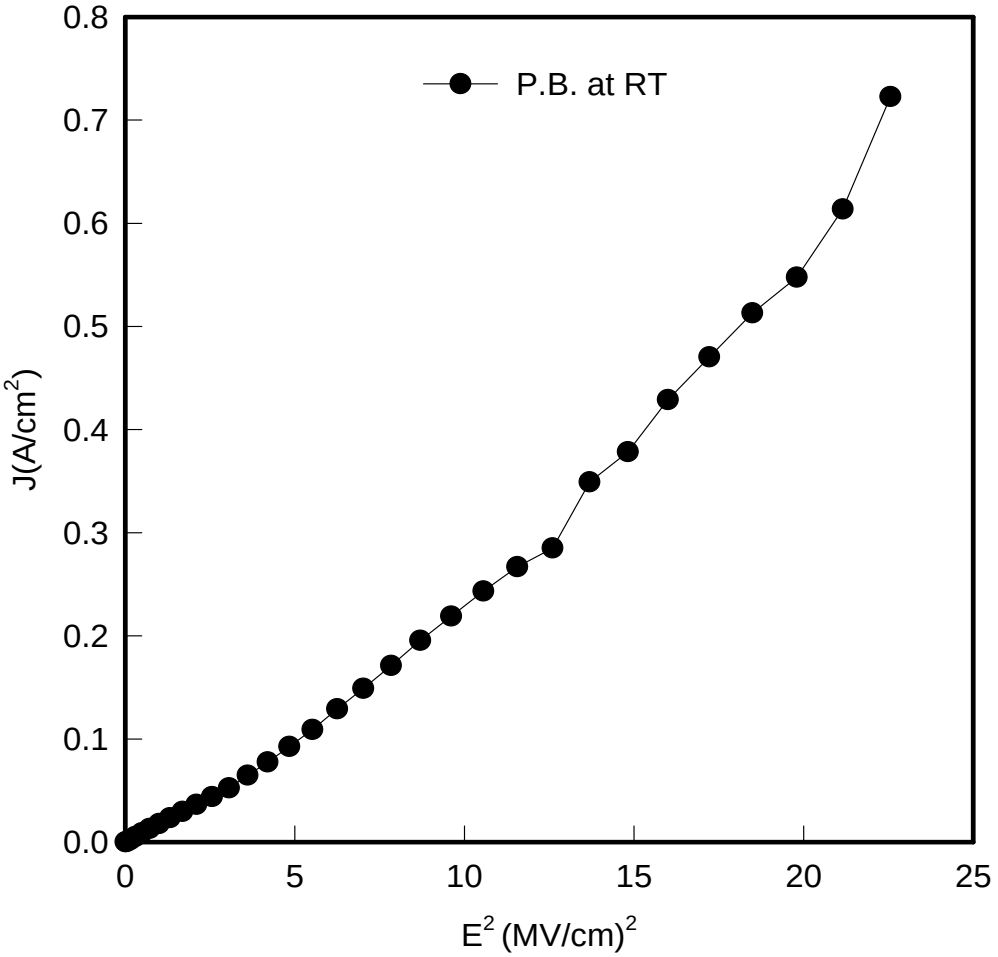


Fig 7-11 J-E^2 characteristic of post-breakdown SiCN4 measured at room temperature.

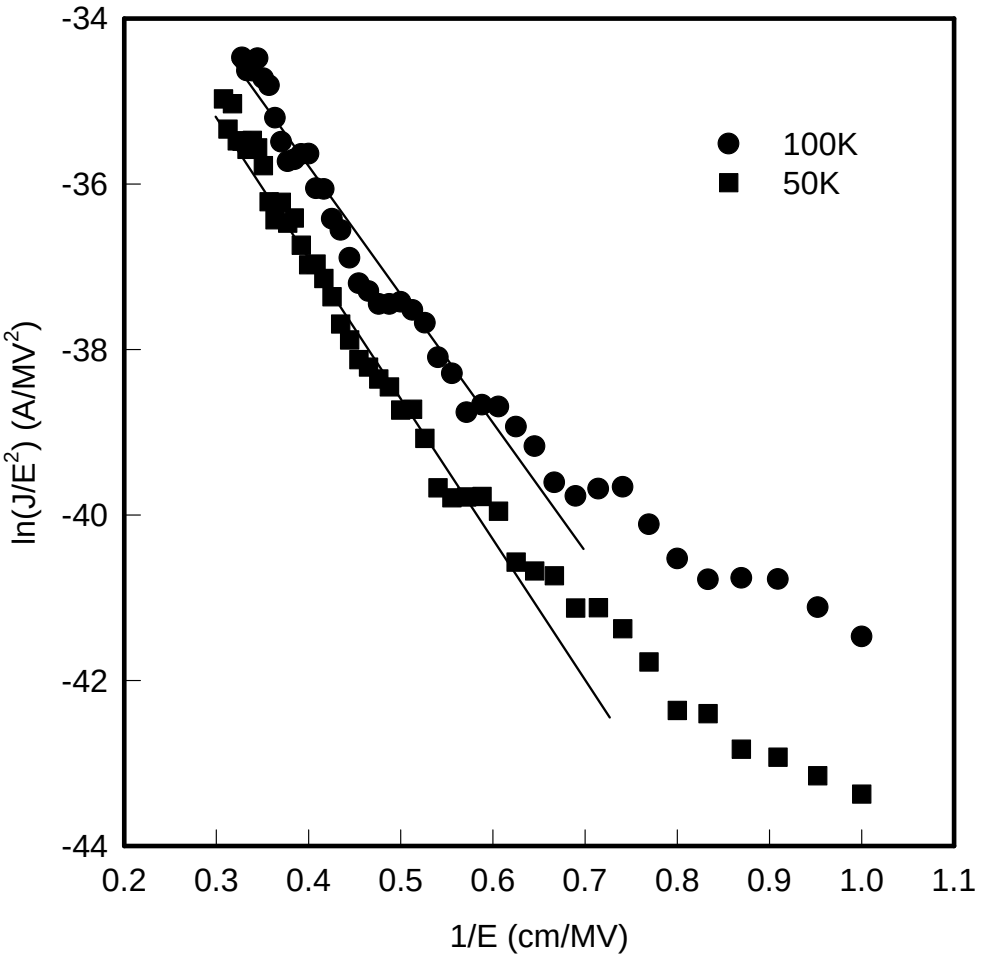
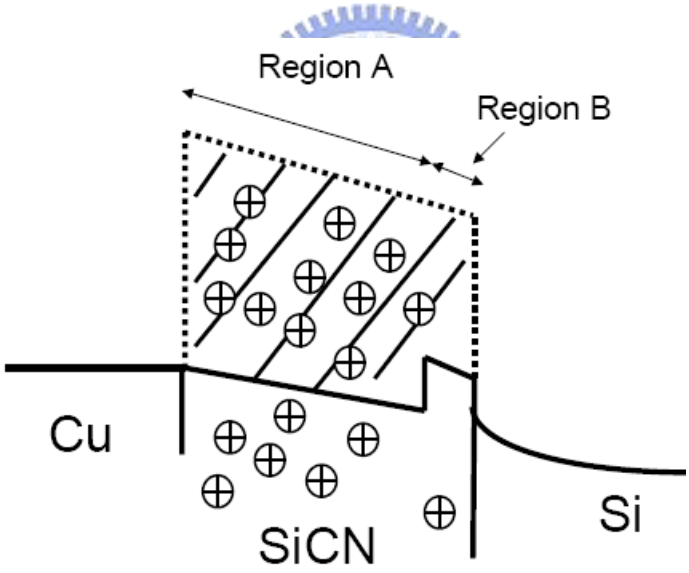


Fig 7-12 The conduction characteristics of post-breakdown a-SiCN at low temperature. $\ln(J/E^2)$ -1/E showing the Fowler–Nordheim (FN) conduction.

(a)



(b)

Fig 7-13 (a) A cross-sectional view in real space of post-breakdown a-SiCN. The post-breakdown sample is composed of two region, conduction filament (labeled A) and barrier (labeled B). (b) energy band-diagram scheme for electrons. At low temperature, electrons are conducted by F-N tunneling at the SiCN/Si interface.

Chapter 8

Conclusions and Suggestions for Future Work

8.1 Conclusions

In this thesis, the new structure of a-Si TFT has been first proposed to improve the on-current and reliability of the BCE device. The AC stress and temperature effects on poly-Si TFT have been investigated for circuit and display applications. The location of the grain boundary in the channel of the SLS poly-Si TFT was also discussed. Moreover, the characterizations of the two non-volatile memory devices fabricated using low-temperature poly-Si technology were demonstrated. Several important results are summarized as following sections.

8.1.1 High Performance amorphous Silicon TFT

A novel technology for manufacturing high-performance hydrogenated amorphous silicon (a-Si:H) TFT has been developed. In the bottom gate light-shield a-Si:H TFT structure, the side edge of a-Si:H island is capped with an extra deposition of heavily phosphorous-doped a-Si layer. Such an ingenuity can effectively eliminate the leakage path between the parasitic contacts between source/drain metal and a-Si:H at the edge of a-Si:H island. The n+ a-Si:H layer can effectively block the hole current when the gate is at negative bias. Under the same applied gate voltages, the leakage current of the proposed structure is as low as two orders of magnitude, compared to the conventional BCE structure. In addition, our proposed a-Si:H TFT device exhibits

superior effective carrier mobility, as high as 1.05 cm^2/Vsec due to the enormous improvement in parasitic resistance. In the proposed structure, the electrons can transport though contacts, the side wall and the top contact of drain metal overlap region. By the contrary, the conventional inverted staggered TFT owns one path for transporting, from the bottom accumulation layer of the a-Si:H layer to the top contact of metal. Hence, the lower parasitic resistance of the proposed TFT results in relatively high mobility and low threshold voltage. We have evidenced that the leakage current of proposed TFT is lower than the conventional BCE device under bottom-side illumination of 6000 nits. It also exhibits the better ability against the DC current stressing. The impressively high performance provides the potential of the proposed a-Si:H TFT to apply for AMLCD and AMOLED technology.

8.1.2 Investigation of Poly-Silicon Thin Film Transistors with/without LDD Structure at Temperatures and under AC stress

The conducting current of non-LDD poly-Si TFT was found to be increased with the decreasing in the temperatures. The phonon scattering is responsible for the evolution of carrier mobility in poly-Si TFT at temperatures. However, the LDD poly-Si TFT is obviously influenced by the LDD layers extended outside the gate electrode. LDD sheet works as a larger resistor at low temperature than that at high temperature. According to the Seto's model, the electrons activated from the doped atoms, Phosphorous, were filled at the trap states at the grain boundaries. For simplify, the amount of free carrier in LDD layers, N_{free}, can be equated to:

$$N_{free} = N_D^{+} - N_T$$

where N_D^{+} is the number of ionized impurities and N_T is the effective trap density. Thus the conductivity of poly-Si film is proportional to the amount of free carriers.

With the decreasing of the temperature, the amounts of activated electrons are decreasing and the ratio of trapped electrons is rising by assuming that the amount of trap states is non-varied. The few free electrons are contributed to the conduction, and thus the conductivity is decayed at low temperature. These results can provide the designers to consider the temperature effects for the poly-Si TFT application in a suitable temperature range.

In addition, the distinct decrease in ON-current of n-channel poly-Si TFT was found during the dynamic voltage stress. In spite of electrical degradation appearing at the ON-current of the poly-Si TFT, both the sub-threshold swing and threshold voltage kept in a good condition. This can be inferred that the tail states were produced in ploy-Si film due to the AC stress. Additionally, the current crowding effect was increased with the increasing of stress time. The parasitic resistances extracted from the I_D-V_D curves of poly-Si TFTs were significantly increased after the 1000 s stressing. The creation of effective trap density in tail-states is responsible for the raise of the parasitic resistance and the degradation in ON-current of TFT. The effective trap density of poly-Si TFTs stressed for 1000 s was 3.14×10^{12} cm^{-2}, 2.21 times the un-stress device.

8.1.3 The Influence of Grain Boundary Location on Low Temperature Poly-Si Thin-Film Transistors

The NGB-TFT owns superior conducting ability than the GB TFT which contains a 100-nm trap-numerous region at the middle of the channel. However, the GB-TFT exhibits the better endurance against DC stress than the NGB-TFT. Based on the simulation result, the existence of GB in the middle of channel of poly-Si TFT would reduce the electric field in the drain region significantly. Accordingly, the GB-TFT suffers relatively lighter impact of hot carrier stress and maintains electrical

characteristics well during the DC stressing. The NGB-TFT was seriously degraded by the DC stress with the high electric field at the drain side. Nevertheless, the distinct electrical behaviors of the TFTs were demonstrated under the AC gate bias stress. Due to the existence of protrusion in the channel, GB-TFT shows weaker endurance against the AC gate pulse stress than that of NGB TFT. The magnitude of the vertical field at the protrusion is stronger than the other regions in GB TFT. The strong electric field would lead to the state creation and charge trapping at the protrusion and reduce the device's electrical performance. Consequently, grain boundaries perpendicular to the channel direction in SLS poly-Si TFT would reduce the horizontal field near the drain side. But the protrusion of grain boundaries of SLS poly-Si film would lead to the larger vertical field. The influences of horizontal and vertical fields can be observed and identified under hot carrier and AC gate stresses.

8.1.4 Non-Volatile Memory Devices Fabricated on Glass Substrate Using Low Temperature Poly-Si Technology

The characterizations of the two non-volatile memory devices fabricated on glass using low-temperature poly-silicon technology were studied. The maximum temperature of processing is below 650^{o}C for the glass substrate. The floating-gate memory device consists of two active regions of poly-Si layer, one behaves as the control gate and the other is the conducting channel region. The device whose control-gate is made of whole heavily-doped poly-Si sheet owns lager on-current and memory windows than the device whose control-gate is a common transistor. In the proposed structure, the applied bias could efficiently couple to the channel. Moreover, the characterizations of MONOS type memory with an oxide-nitride-oxide (ONO) stack structure were studied. For 10 ms P/E pulse time, the threshold voltage window

is 1.5V for the memory device and it maintains a wide threshold voltage window after 10^4 P/E cycle. The proper operation method for poly-Si memory device is F-N tunneling occurred either in SD/gate overlap region or channel region. For the nature of poly-Si film on glass substrate, the channel hot electron injection is not suitable for the programming since the traps at the grain boundary in the poly-Si film would enhance the hot carrier effect and avalanche breakdown resulting in electrical degradation.

8.1.5 Investigation of the Nano-Porous Silica for Interconnections with Low-RC Delay

The moisture-induced instability of POSG has been investigated. The lager leakage current is observed in hot-water dipped sample. However, there is no distinct change in the material characterizations of POSG even after 3hrs dipping. Thermal desorption spectra evidenced that the moisture really existed in the leaky sample. The leakage current would be increased and dominated by the ionic conduction as the moisture is contained in the POSG. Additionally, the moisture would enhance the Cu to penetrate into POSG and cause the raise of the leakage cuurent.

8.1.6 Investigation of the Electrical Properties and Reliability of Amorphous SiCN

The leaky behavior and barrier characteristics of a-SiCN containing different nitrogen concentrations have been detail studied. The leaky behavior of a-SiCN is Pool-Frenkel in high electric field region. Experimental results indicate that a-SiCN films containing higher nitrogen concentration exhibited better barrier ability. The

dielectric breakdown is due to the penetration of Cu. The electrical characteristics of post-breakdown a-SiCN caused by Cu penetration are investigated. SIMS spectrum shows that Cu ions can penetrate through the film at 150^{o}C in high fields (5MV/cm). It is observed that the main conduction of post-breakdown a-SiCN at room temperature (298K) is space-charge-limited current (SCLC) due to numerous Cu impurity/traps. Moreover, the characteristics at low temperature can be separated into two distinct stages, Fowler–Nordheim tunneling and SCLC conduction. We propose a physical model which post-breakdown a-SiCN was composed of two different conduction regions. It can well describe the electrical variation resulted from the Cu traps and temperature.

8.2 Suggestions for Future Work

There are a number of topics relevant to this thesis which deserves further studies. The following topics are suggested for future works.

(1) Integration of low-k passivation capped on the BCE a-Si TFTs.

(2) Electrical characterizations and stabilities of a-Si and poly-Si TFTs under bending stress.

(3) Improvement on the roughness of ELA poly-Si films for poly-Si non-volatile memory devices.

(4) Gate-dielectric engineering of tunneling oxide of poly-Si non-volatile memory devices.

(5) Cu interconnections for AMOLED applications.

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Publication List

International Regular Journals：

[1] **C. W. Chen**, T. C. Chang, P. T. Liu, T. M. Tsai, C. H. Huang, J. M. Chen, T. Y. Tseng, "Investigation of the electrical properties and reliability of amorphous SiCN", Thin Solid Film, **447**, p.632 (2004) (2點)

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